VHDL Programming Assignment

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Questions:

1. Write RTL for a simple memory model that has 4 address locations with the following values on reset:

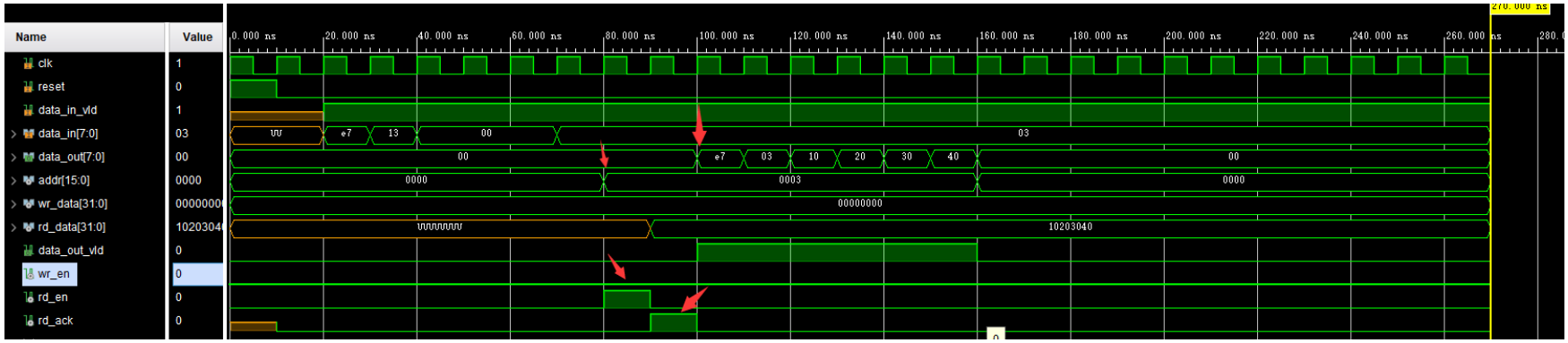
   ```
   0x00 => 0x01234567
   0x01 => 0x89abcde7
   0x02 => 0x0a0b0c0d
   0x03 => 0x10203040
   0xe7 => 0xdeadbeef
   ```

   Read access to locations outside this range should not assert rd_ack.
2. Write RTL for the FSM such that the following input byte streams generate the following output (responses):
   - **a.** input : `0xe7,0x13,0x00,0x00,0x00,0x03`
     output: `0xe7,0x03,0x10,0x20,0x30,0x40`
   - b. input : `0xe7,0x13,0x00,0x00,0x00,0xe7,0xe7`
     output: `0xe7,0x03,0xde,0xad,0xbe,0xef`
   - c. input : `0xe7,0x23,0x00,0x00,0x00,0x02,0xaa,0xe7,0xe7,0x55,0xaa,`
     `0xe7,0x13,0x00,0x00,0x00,0x02`
     output: `0xe7,0x03,0xaa,0xe7,0xe7,0x55,0xaa`
   - d. input : `0xe7,0x23,0x00,0x00,0x00,0x01,0xaa,0xe7,0x55,0xe7,`
     `0x13,0x00,0x00,0x00,0x01`
     output: `0xe7,0x03,0x89,0xab,0xcd,0xe7,0xe7`

Memory content:

```
0x00 => 0x01234567
0x01 => 0x89abcde7
0x02 => 0x0a0b0c0d
0x03 => 0x10203040
0xe7 => 0xdeadbeef
```

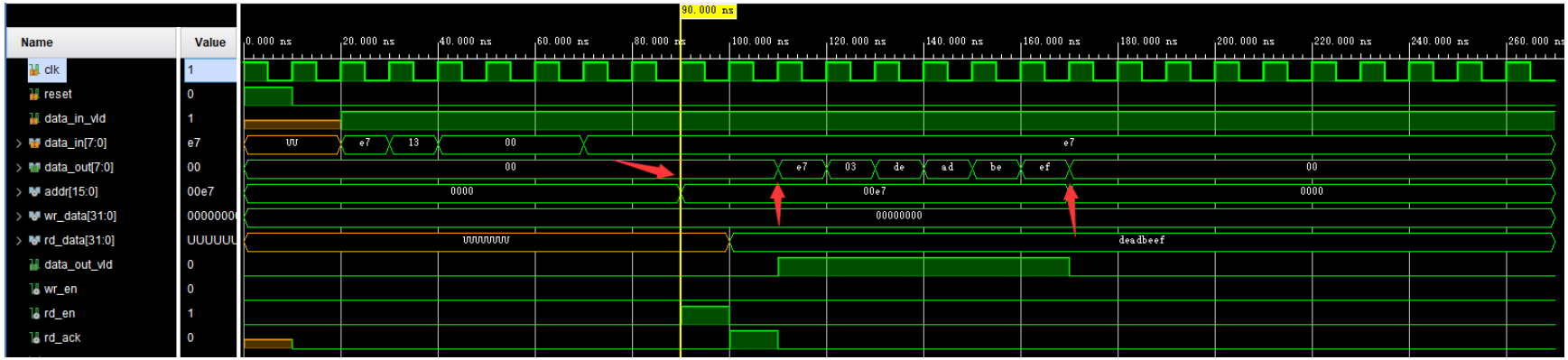
Simulation Result screenshot



CASE1:

IN e7_13_00_00_00_03

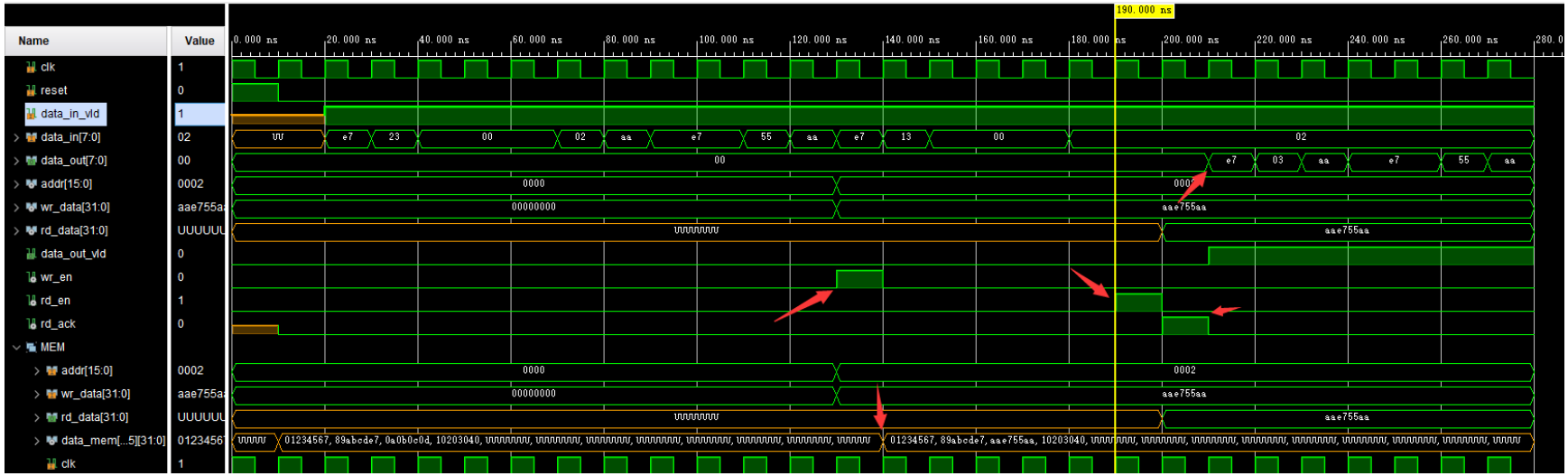
OUT e7_03_10_20_30_40



CASE2:

IN e7_13_00_00_00_e7_e7

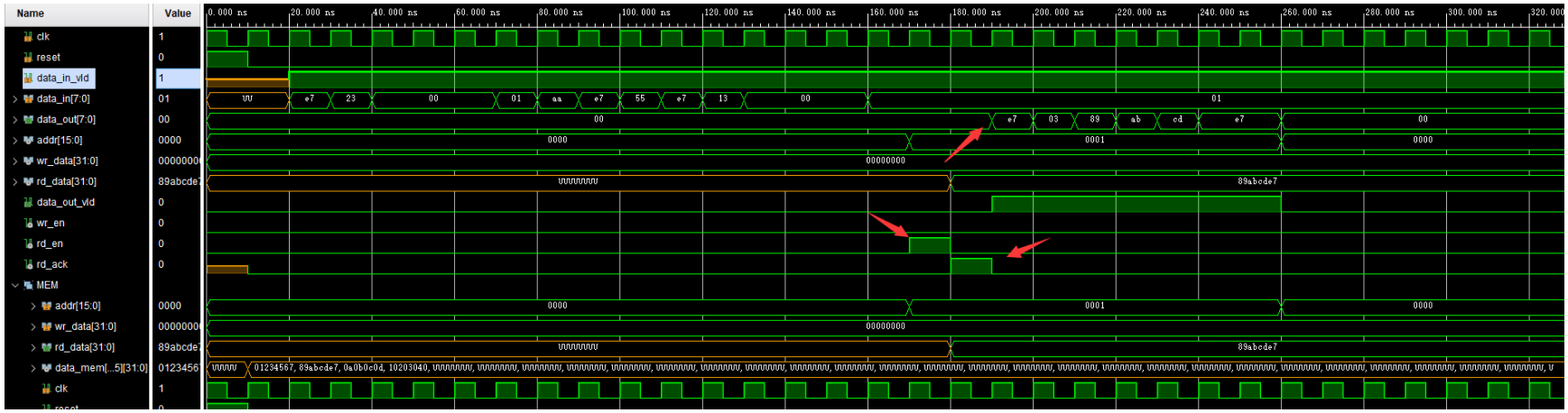
OUT e7_03_de_ad_be_ef



CASE3:

IN e7_23_00_00_00_02_aa_e7_e7_55_aa_e7_13_00_00_00_02

OUT e7_03_aa_e7_e7_55_aa



CASE4:

IN e7_23_00_00_00_01_aa_e7_55_e7_13_00_00_00_01

OUT e7_03_89_ab_cd_e7_e7