02-trans-to-gates-notes

Transistors to Gates

Agenda

- 0. Re-Orienting
- 1. Logic gates
- 2. Building gates from transistors
- 3. Binary (but we likely won't get this far)

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0. Re-Orienting

The computation "stack," from mental model down to the physical universe.

On Monday, we talked about the bottom a bit...

Electricity

1 and 0.

The controlled switch... in solid state!

And... inspiration, from "The Life of Ira Remsen"

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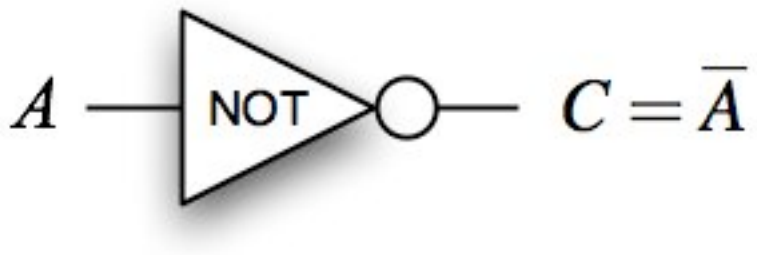
1. Logic gates

(See Sections 2.1.7 and 4.2.1 in the textbook)

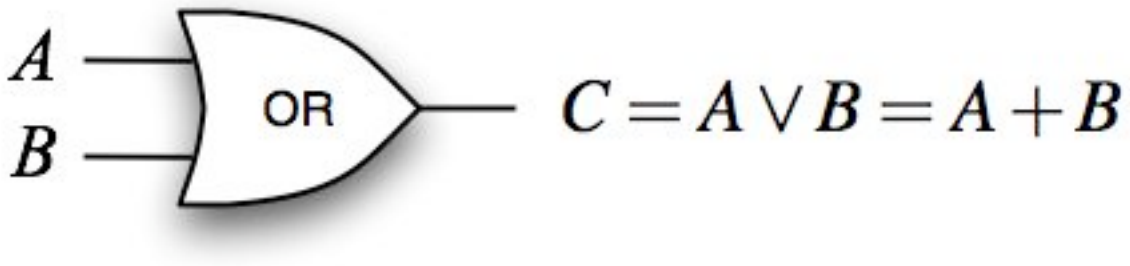
Boolean logic (as we talked about on Monday)

Demo: logic0 and logic1 in [democircs.circ (https://ssl.cs.dartmouth.edu/~sws/cs51-s15/02-trans-to-gates/demo/democircs.zip)](https://ssl.cs.dartmouth.edu/~sws/cs51-s15/02-trans-to-gates/demo/democircs.zip)

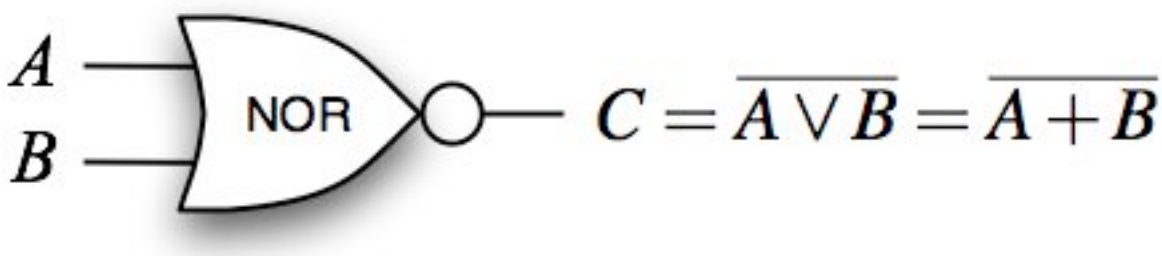
NOT. (AKA "inverter"). Inverts the input.

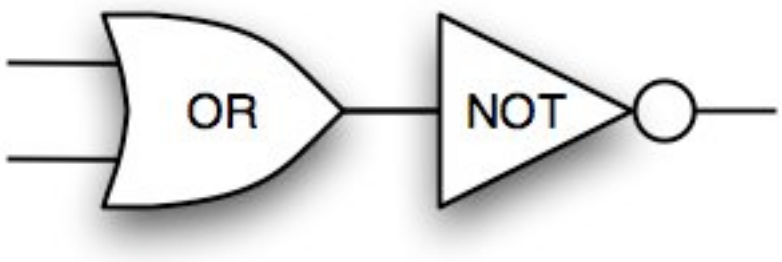


OR. Outputs a 1 if A is one **OR** B is one. (Or both.)

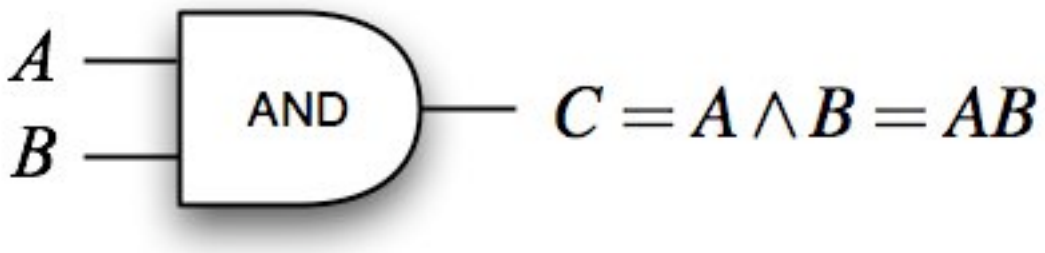


NOR. NOT OR. An OR, with the output inverted. Outputs a 0 if A is one OR B is one. (Or both.)

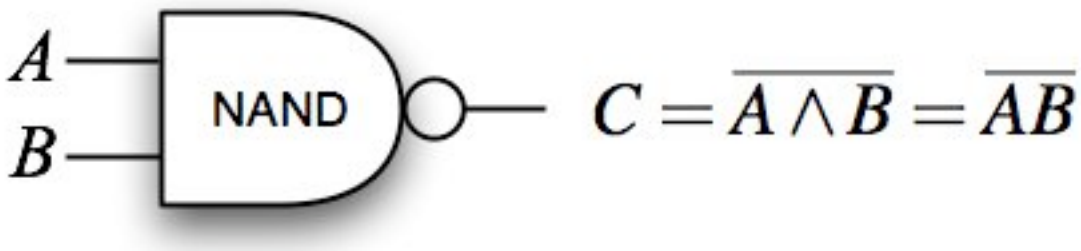


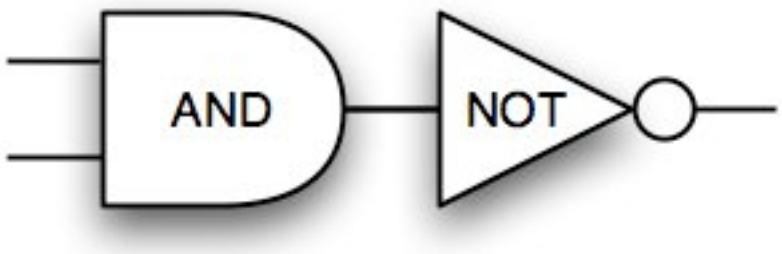


AND. Outputs a 1 only when A is one **AND** B is one.



NAND. NOT AND. An AND, with the output inverted. Outputs a 0 only when A is one AND B is one.





Here's one we didn't get to on Monday: XOR. "Exclusive OR." Outputs a 1 if A is one **OR** B is one (but **not both**)

Details

Note:

- except for NOT, fan-in can be greater than two. see logic2 in [democircs.circ]

(https://ssl.cs.dartmouth.edu/~sws/cs51-s15/02-trans-to-gates/demo/democircs.zip)

- little round circles
- (mention idea of truth tables)

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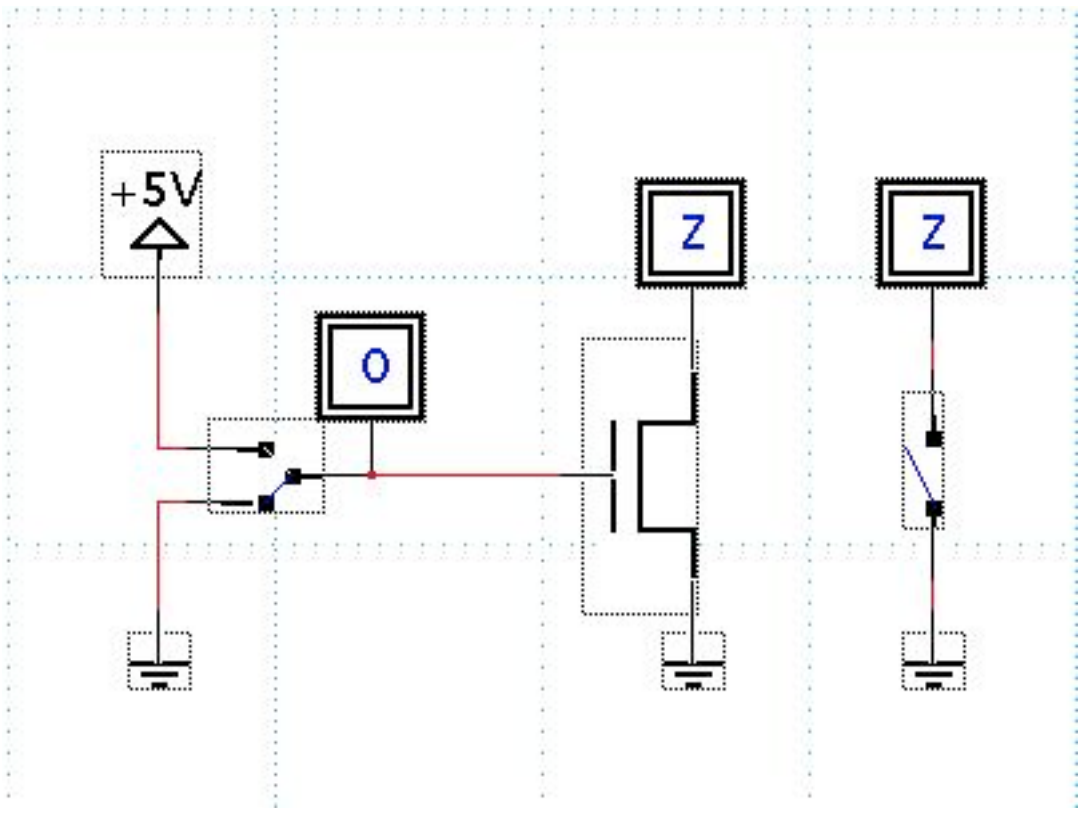
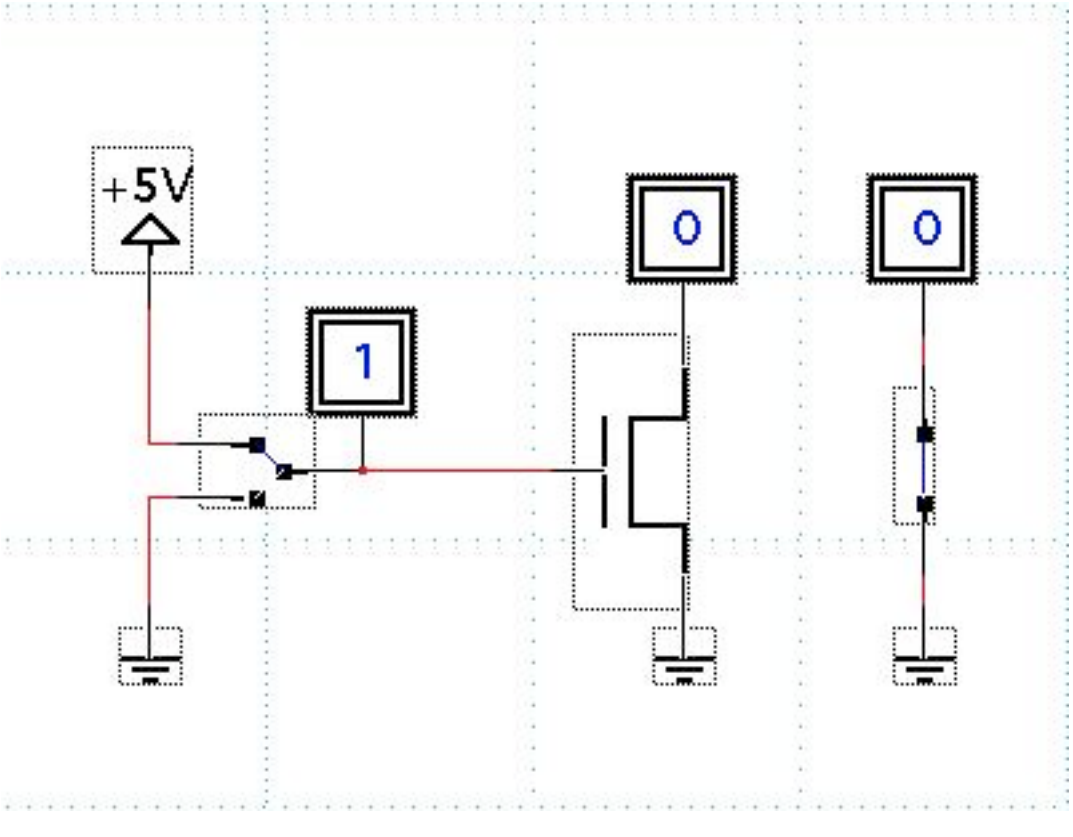
2. Building gates from transistors

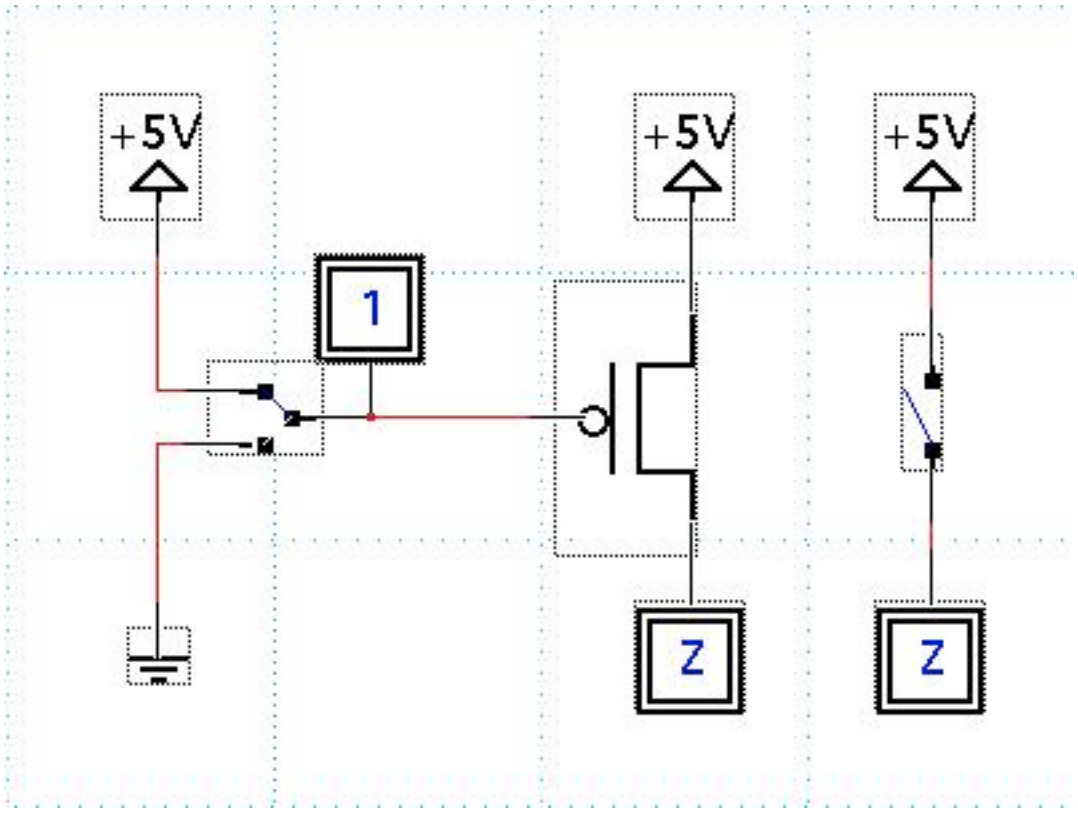
Recall the building blocks

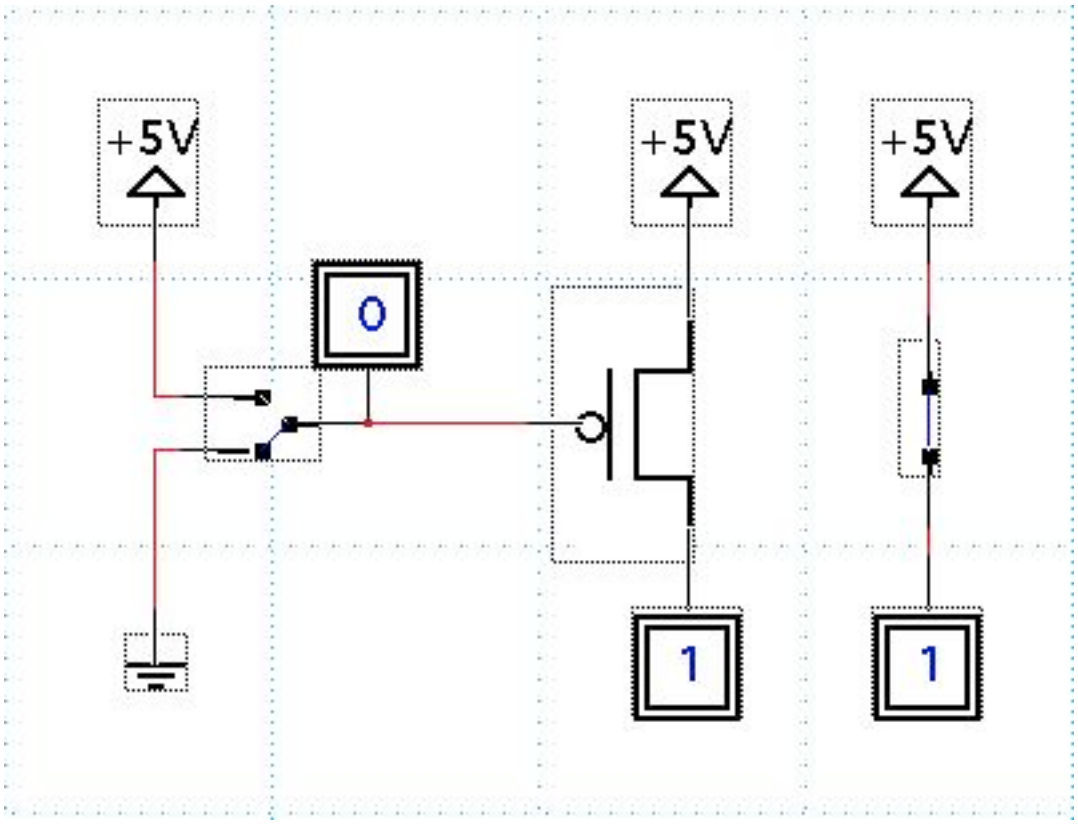
n-type MOS transistor: closes the "switch" when the gate has a sufficiently positive voltage:





p-type MOS transistor: closes the "switch" when the gate has a sufficiently negaive voltage:





Note again that: this just one of many families and types of transistors

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1 and 0

Gates

start with CMOS (Complementary MOS)

- cmos in **tran-gates.circ (https://ssl.cs.dartmouth.edu/~sws/cs51-s15/02-trans-to-gates/demo/tran-gates.zip)**

build NOT

- not in **tran-gates.circ (https://ssl.cs.dartmouth.edu/~sws/cs51-s14/02-trans-to-gates/demo/tran-gates.zip)**

build NOR and discuss intuition

- nor in **tran-gates.circ (https://ssl.cs.dartmouth.edu/~sws/cs51-s15/02-trans-to-gates/demo/tran-gates.zip)**

build NAND and discuss intuition

- nand in **tran-gates.circ (https://ssl.cs.dartmouth.edu/~sws/cs51-s15/02-trans-to-gates/demo/tran-gates.zip)**

Note that there are many other ways of doing this.

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and.... cheap gates with diodes:

- diode-and in **tran-gates.circ (https://ssl.cs.dartmouth.edu/~sws/cs51-s15/02-trans-to-gates/demo/tran-gates.zip)**

If you've read this far

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here's a zipfile with (https://ssl.cs.dartmouth.edu/~sws/cs51-s15/02-trans-to-gates/demo/tran-gates-full.zip)

- tran-gates-full.circ: annotated examples of the NOT, NOT, and NAND gates built out of transistors (and the diode AND too, just for good measure)
- tran-gates-full-buffers.circ: for pedagogical purposes, the above file, but also with LogiSim "buffer gates" and more binary probes inserted, so you can better see the flow of signals through things

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Advertisements!

``If you're interested in ***security research or security in general,*** consider attending ***Security Reading Group!*** In an informal setting, we discuss recent security research papers and tie them in with recent events over some snacks. Please contact **Vijay.H.Kothari.GR@dartmouth.edu (mailto:Vijay.H.Kothari.GR@dartmouth.edu)** if you're interested and he'll add you to the list. (time is tbd)'

``If you're interested in learning about ***hacking*** (in the security sense of the word) then attend ***Hacker Morning***! We

learn about hacking by doing it. If you want to learn about SQL injection, buffer overflows, return-oriented programming, and other hacking techniques, old and new, in a relaxed environment, we invite you to join the security lab (Sudi 045) on Fridays from 11 AM and onwards. If interested, please contact **Stefan.G.Boesen.GR@dartmouth.edu (mailto:Stefan.G.Boesen.GR@dartmouth.edu)** ."