# 07-ram-notes

## ***RAM***

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## Agenda

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- 0. Re-Orienting
- 1. Latches and Flip-flops
- 2. RAM (from the top)
- 3. RAM (from the bottom)
- 4. Dynamic RAM
- 5. If time.... flashy numbers!

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## 0. Re-Orienting

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electricity to gates

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representing numbers as binary

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building circuits that calculate functions on binary numbers

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## 1. Latches and Flip-flops

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putting "feedback" into circuits lets them remember state

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the physical reality of the circuits can affect the logic design. (The abstraction barrier has holes in it!)

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we can use this hole to turn edges into short pulses. (we didn't have time to get to this yesteday---but see the notes!)

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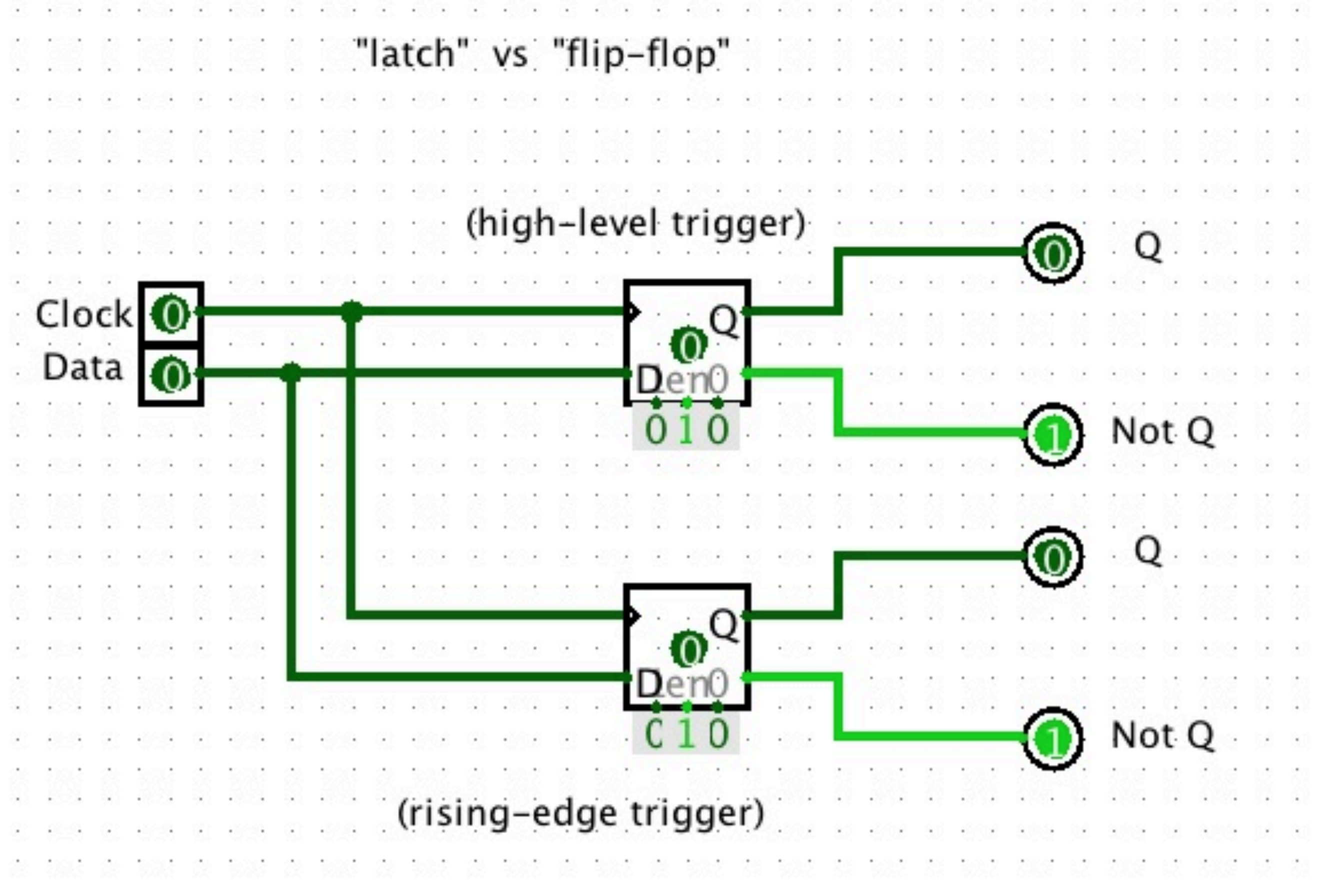
...and thus build

- *latches,* which store a bit on a given clock *level*
- *flip-flops,* which store a bit a given clock *edge*

(Although there are other ways to build in edge-sensitivity)




Recall... "latchflop" in [ram.circ (https://ssl.cs.dartmouth.edu/~sws/cs51-s15/07-ram/demo/ram.zip)](https://ssl.cs.dartmouth.edu/~sws/cs51-s15/07-ram/demo/ram.zip)

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## 2. RAM (from the top)

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Flip-flops/latches REMEMBER things. In the context of computer architecture, probably their most natural application is MEMORY.

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Reviewing (or introducing) the concept of computer memory:

- an array of "slots"
- each slot can hold some unit of data (e.g., a byte)
- each slot has an index number, called an **address**
- in a **read** operation, we specify an address, and the memory spits out the contents of that slot
- in a **write** operation, we specify an address and some new slot contents, and the memory stores those contents in that sot

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As we discussed already....

- This model implicitly makes it possible to touch the memory slots in **any** order
- Hence the term **random access**
- (But the world now uses the term RAM to mean specifically random access memory that is **also** readable and writable.)

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But in the real world, we have some ambiguity: what is the "slot" size?

- generally, it's still a byte
- except the natural data size in standard machines is usually some larger **word**, such as 32 bits.
- so we still number the slots by bytes, but also permit operations to touch the **word** that lives at a specific address
  - that is... the word consisting of the bytes at address A, A+1, A+2, A+3
  - but what if this address is not a multiple of four?
- And as 32-bit machines give way to 64-bit machines, this will get even more fun.

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## 3. RAM (from the bottom)

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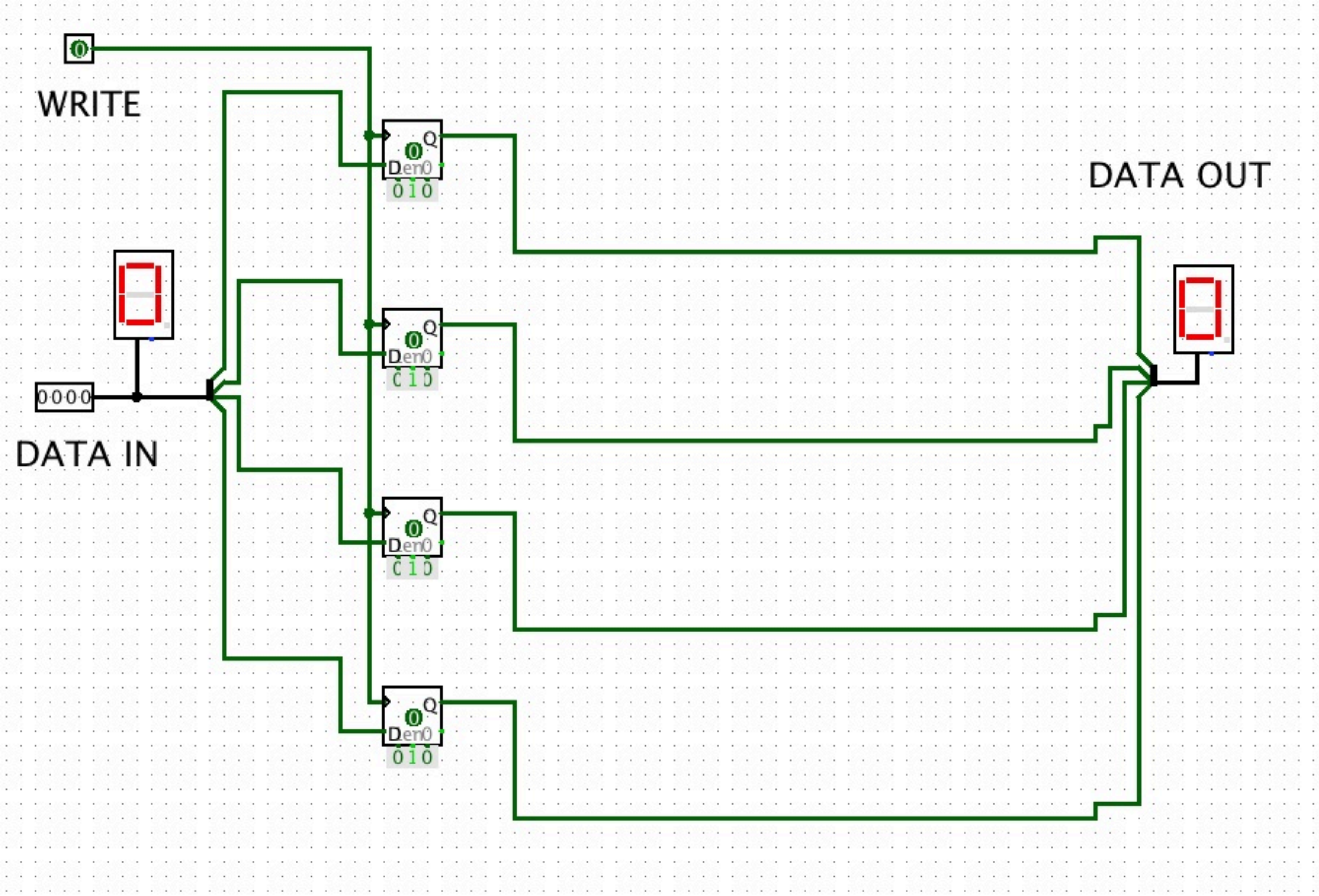
Four 1-bit D flip-flops:




("one-nibble" in ram.circ)

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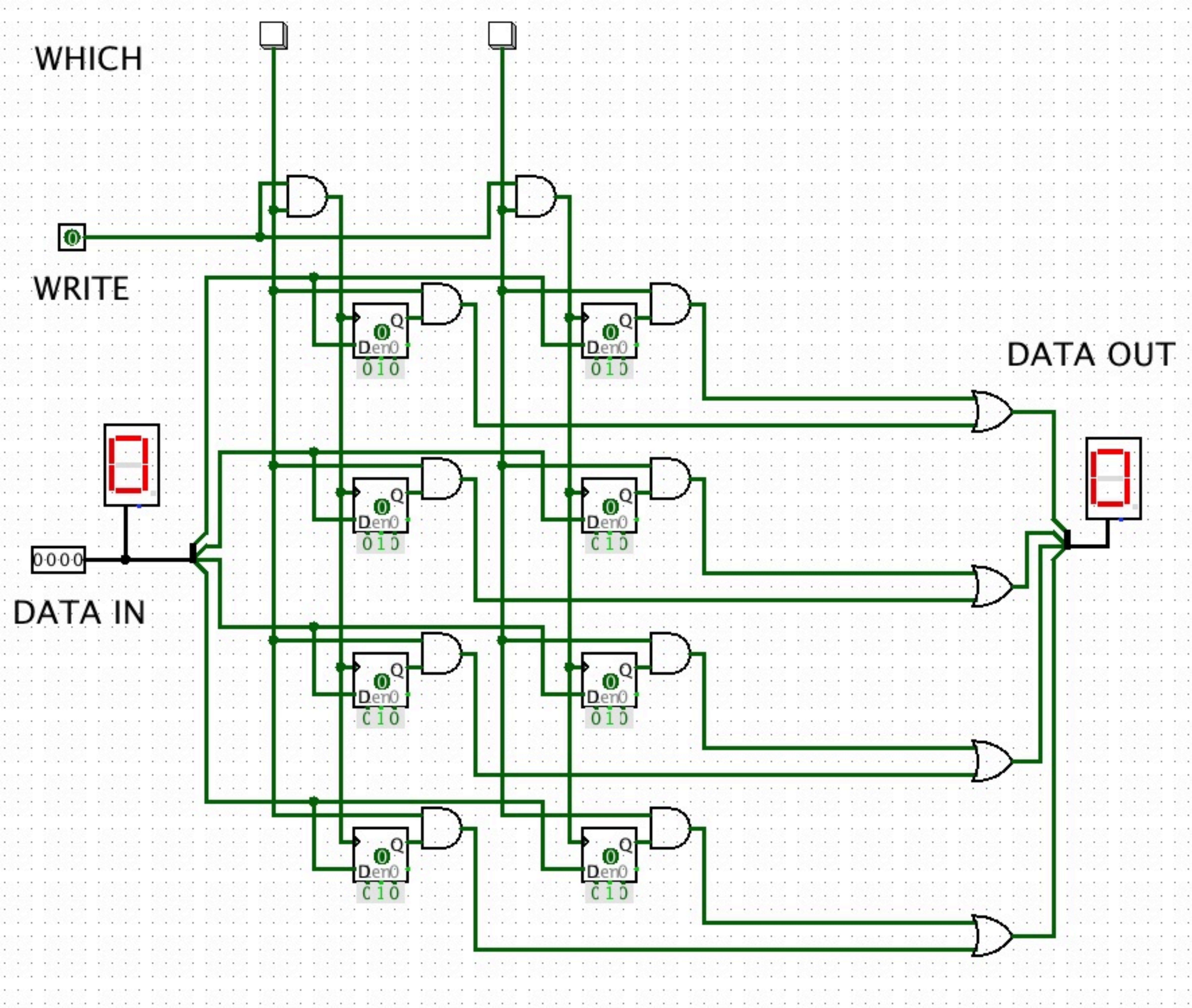
Let's add another, and the interesting one selectable




("two-nibbles" in ram.circ)

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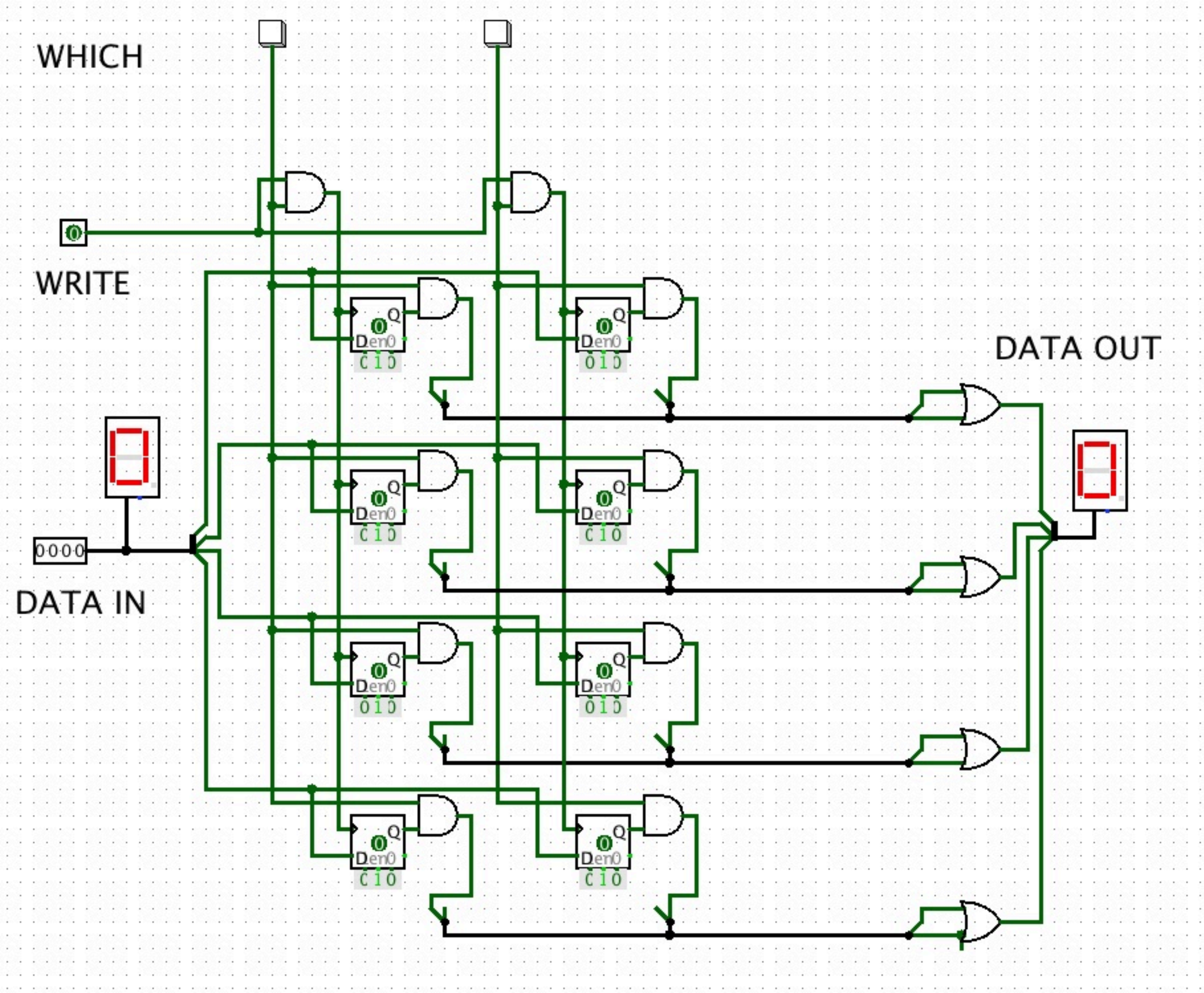
Let's make these parallel lines into a multi-bit wide line




("two-nibbles-bus" in ram.circ)

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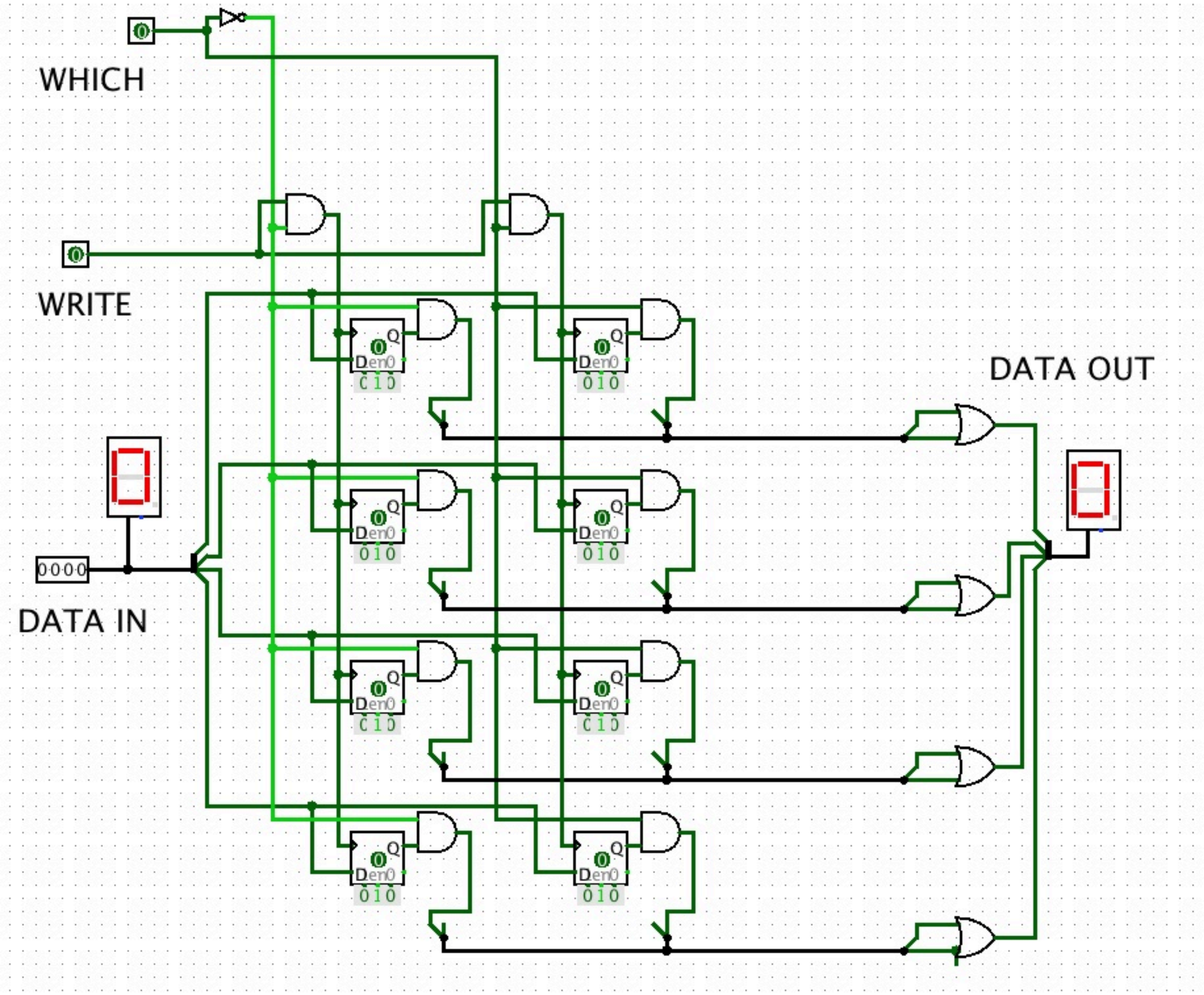
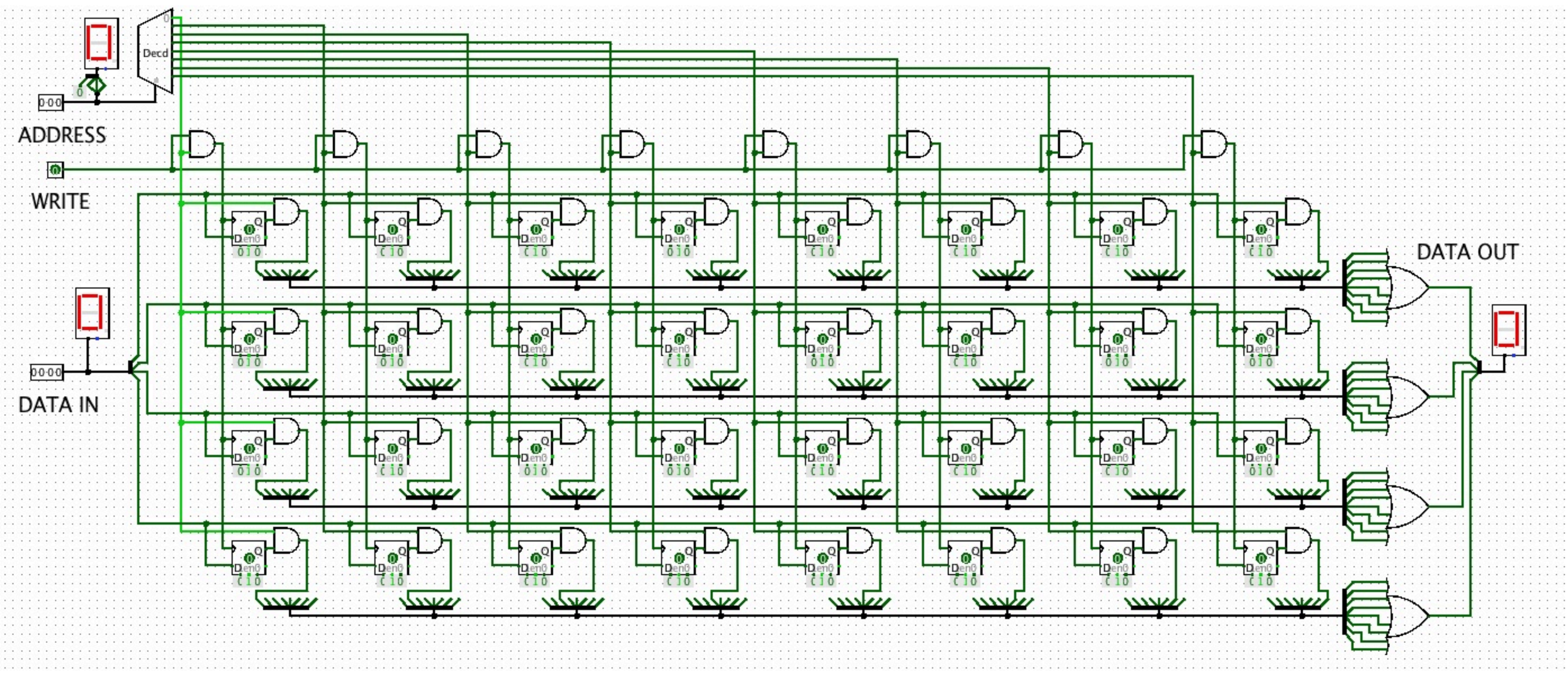
Let's get rid of the pushbuttons, and make it a 1-bit decoder




("two-nibbles-addr-bus" in ram.circ)

And generalize to three bits of address!




("main" in ram.circ)

Gosh, darn: RANDOM ACCESS MEMORY!

(This example uses the "column = word" approach, although I usually like to think of ROWS as words.)

do you understand all the pieces that are in there?

- the decoder
- the gating of the write-enable lines into the clock
- (although note that one may often want to have a master clock-in as well as a master enable)
- the marshaling of the data into the flip-flops
- gating the data out into the giant ORs
- the roles of the splitters in the collection of data out
- the role of the splitters taking the address lines into the address display

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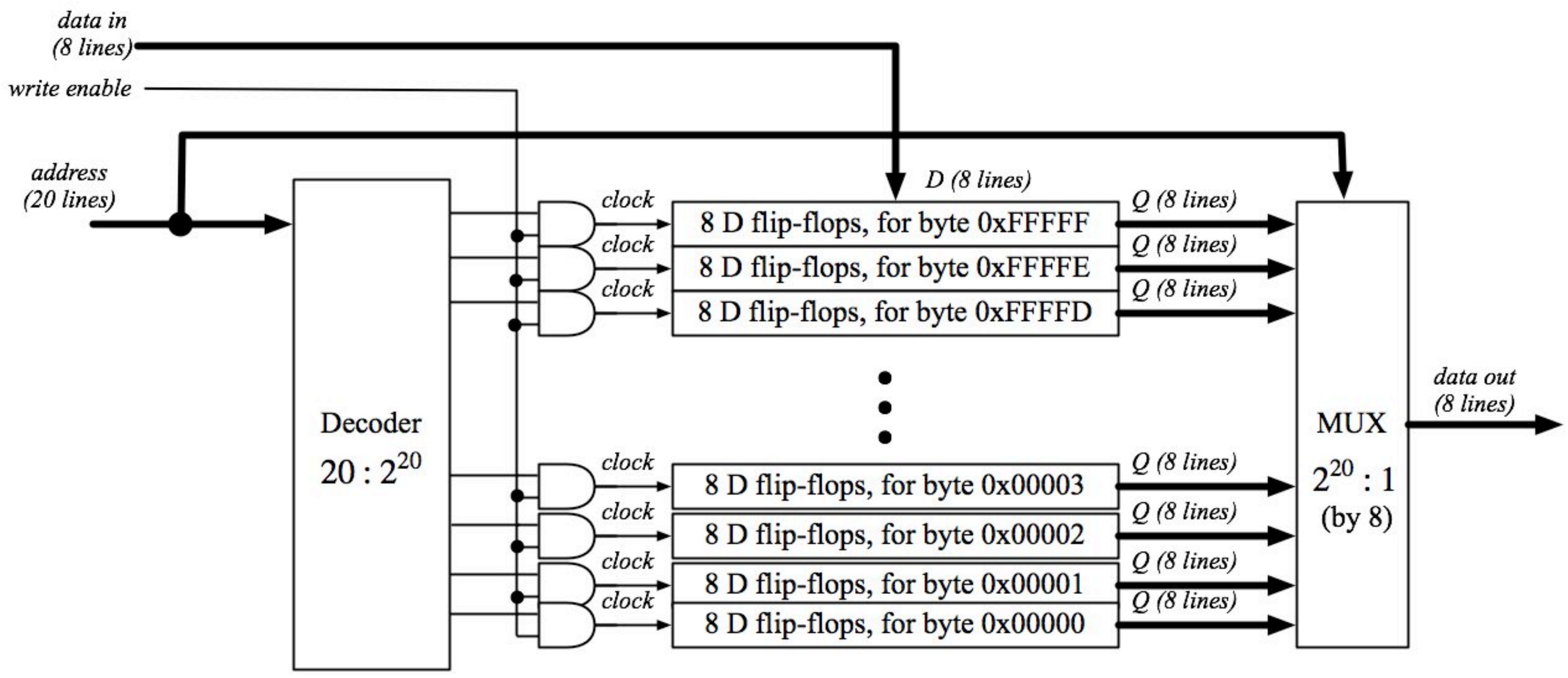
A megabyte of RAM




***1 megabyte of static RAM***

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# 4. Dynamic RAM

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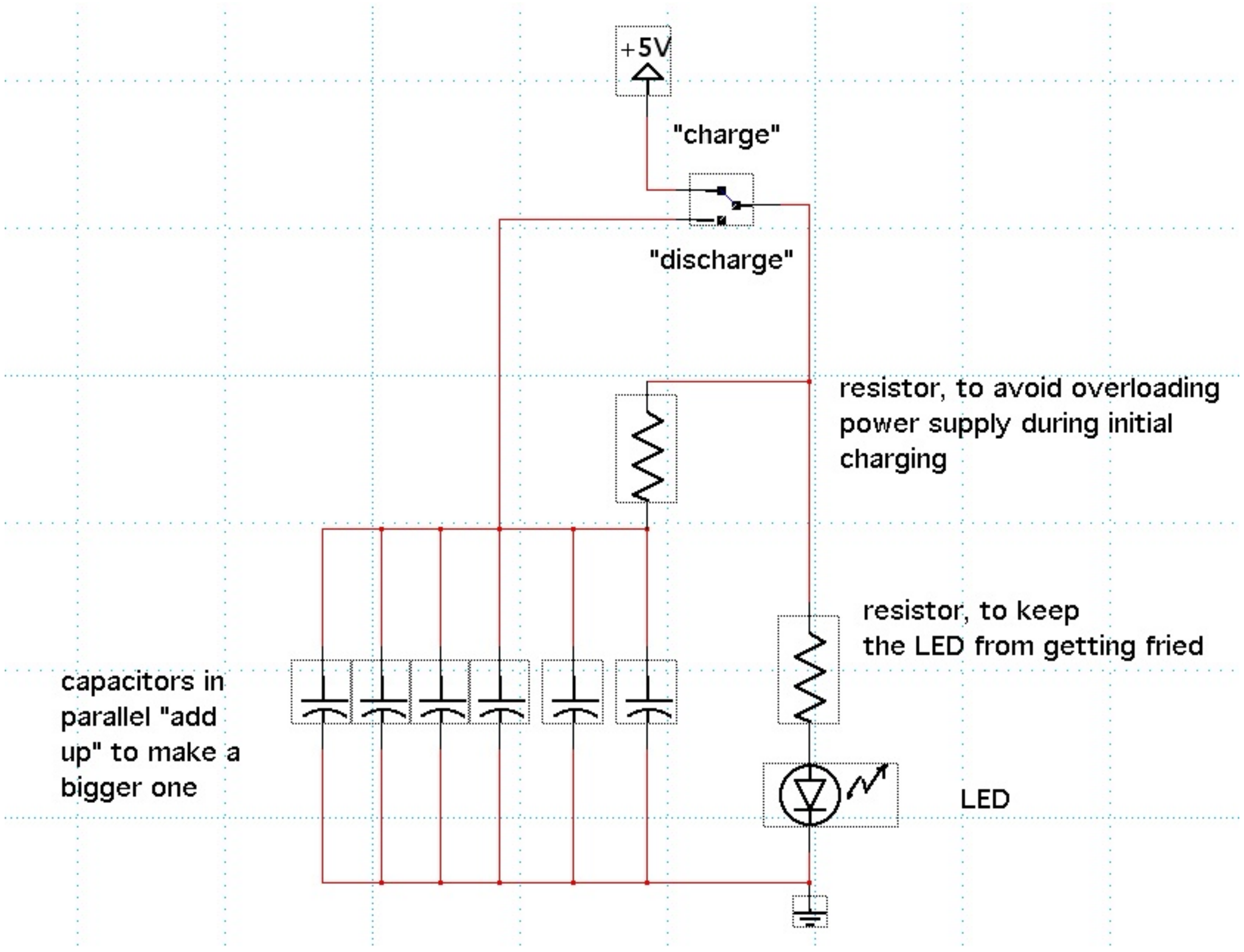
Reality intervenes: using capacitors to build trickier but "sparser" DYNAMIC RAM (DRAM)... enabling much greater densities [http://micro.magnet.fsu.edu/electromag/java/capacitor/](http://micro.magnet.fsu.edu/electromag/java/capacitor/) (http://micro.magnet.fsu.edu/electromag/java/capacitor/)

(real demo)




Why don't we just use a capacitor to store 1 bit?

(There's a catch...and a workaround...)

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What are the problems with building RAM out of capacitors?

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DRAM: with capacitors (dense, higher power consumption)

SRAM: with flip-flops (less dense, but lower power)

(Yes, the textbook claims DRAM has lower power consumption, but I believe that's incorrect, particularly for long-term storage in battery-powered devices. The textbook probably does NOT take into account the cost of DRAM refresh)

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See more discussion in section 6.1 of the textbook.

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