18-uarch-pipeline-notes

Microarchitecture; Pipelining

Agenda

- 0. Re-Orienting
- 1. Microarchitecture: Putting it all together
- 2. Pipelining
- 3. Advantages
- 4. Disdvantages

Reading: 4.4

Here are the slides (https://ssl.cs.dartmouth.edu/~sws/cs51-s15/18-uarch-pipeline/slides.pdf)

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0. Re-Orienting

The human

Programming

Assembly, machine language

the ISA

datapath, control path, microarchitecture

sequential logic

combo logic

gates

transistors

electricity

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1. Microarchitecture: Putting it all together

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connecting...

- instruction
- FSM
- microinstructions
- control ROM
- microsequencer

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2. Pipelining (http://goo.gl/oCzOP1)

Progressing down the Mess/Speed path.

Basic idea:

- in one cycle, combo into register
- chop the combo up and add more registers

How can this ever be a good idea? That's more cycles to get anything done!

Work through demonstrations

Keeping all the piece of the datapath busy all the time

Standard analogies

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3. Advantages

Definitions: delay (latency), throughput

The sequential case

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example: 3-stage pipeline

- longer latency, but
- higher throughput (and give intuition)

Going superscalar!

- e.g.... what if you wanted to add "multiply"?

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4. Disdvantages

Non-uniform delays

Diminishing returns

Data hazards

Control hazards