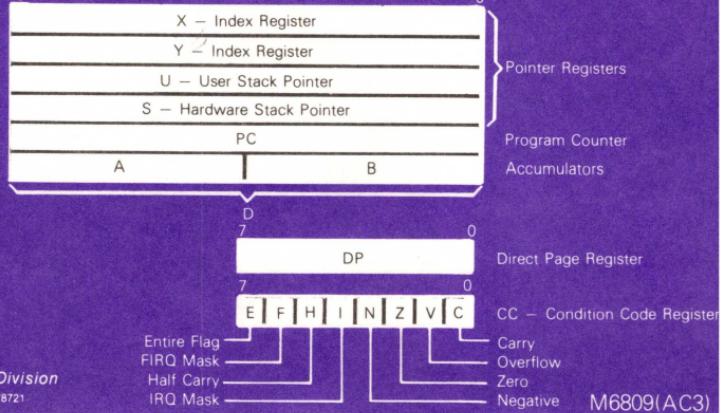


MC6809 — MC6809E

8-bit microprocessor Reference Card

PROGRAMMING MODEL



MOTOROLA INC.

MOS Integrated Circuits Division

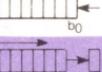
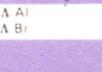
3501 ED BLUESTEIN BLVD AUSTIN, TEXAS 78721

M6809(AC3)

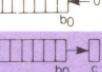
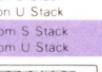
OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#
00	NEG	DIRECT	6	2	1C	ANDCC	IMMED	3	2	2E	BGT	RELATIVE	3	2
03	COM		6	2	1D	SEX	INHERENT	2	1	2F	BLE	RELATIVE	3	2
04	LSR		6	2	1E	EXG	IMMED	8	2	30	LEAX	INDEXED	4	2
06	ROR		6	2	1F	TFR	IMMED	6	2	31	LEAY		4	2
07	ASR		6	2	20	BRA	RELATIVE	3	2	32	LEAS		4	2
08	ASL/LSL		6	2	21	BRN		3	2	33	LEAU	INDEXED	4	2
09	ROL		6	2	22	BHI		3	2	34	PSHS	IMMED	5	2
0A	DEC		6	2	23	BLS		3	2	35	PULS		5	2
0C	INC		6	2	24	BHS/BCC		3	2	36	PSHU		5	2
0D	TST		6	2	25	BLO/BCS		3	2	37	PULU	IMMED	5	2
0E	JMP		3	2	26	BNE		3	2	39	RTS	INHERENT	5	1
0F	CLR	DIRECT	6	2	27	BEO		3	2	3A	ABX		3	1
12	NOP	INHERENT	2	1	28	BVC		3	2	3B	RTI	INHERENT	6/15	1
13	SYNC	INHERENT	4	1	29	BVS		3	2	3C	CWAI	IMMED	20	2
16	LBRA	RELATIVE	5	3	2A	BPL		3	2	3D	MUL	INHERENT	11	1
17	LBSR	RELATIVE	9	3	2B	BMI		3	2	3F	SWI		19	1
19	DAA	INHERENT	2	1	2C	BGE		3	2	40	NEGA		2	1
1A	ORCC	IMMED	3	2	2D	BLT	RELATIVE	3	2	43	COMA	INHERENT	2	1

OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#
44	LSRA	INHERENT	2	1	5D	TSTB	INHERENT	2	1	77	ASR	EXTENDED	7	3
46	RORA		2	1	5F	CLRB	INHERENT	2	1	78	ASL/LSL		7	3
47	ASRA		2	1	60	NEG	INDEXED	6	2	79	ROL		7	3
48	ASLA/LSLA		2	1	63	COM		6	2	7A	DEC		7	3
49	ROLA		2	1	64	LSR		6	2	7C	INC		7	3
4A	DECA		2	1	66	ROR		6	2	7D	TST		7	3
4C	INCA		2	1	67	ASR		6	2	7E	JMP		4	3
4D	TSTA		2	1	68	ASL/LSL		6	2	7F	CLR	EXTENDED	7	3
4F	CLRA		2	1	69	ROL		6	2	80	SUBA	IMMED	2	2
50	NEGB		2	1	6A	DEC		6	2	81	CMPA		2	2
53	COMB		2	1	6C	INC		6	2	82	SBCA		2	2
54	LSRB		2	1	6D	TST		6	2	83	SUBD		4	3
56	RORB		2	1	6E	JMP		3	2	84	ANDA		2	2
57	ASRB		2	1	6F	CLR	INDEXED	6	2	85	BITA		2	2
58	ASLB/LSLB		2	1	70	NEG	EXTENDED	7	3	86	LDA		2	2
59	ROLB		2	1	73	COM		7	3	88	EORA		2	2
5A	DECB		2	1	74	LSR		7	3	89	ADCA		2	2
5C	INC B	INHERENT	2	1	76	ROR	EXTENDED	7	3	8A	ORA	IMMED	2	2

OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#
8B	ADDA	IMMED	2	2	9E	LDX	DIRECT	5	2	B0	SUBA	EXTENDED	5	3
8C	CMPX	IMMED	4	3	9F	STX	DIRECT	5	2	B1	CMPA		5	3
8D	BSR	RELATIVE	7	2	A0	SUBA	INDEXED	4	2	B2	SBCA		5	3
8E	LDX	IMMED	3	3	A1	CMPA		4	2	B3	SUBD		7	3
90	SUBA	DIRECT	4	2	A2	SBCA		4	2	B4	ANDA		5	3
91	CMPA		4	2	A3	SUBD		6	2	B5	BITA		5	3
92	SBCA		4	2	A4	ANDA		4	2	B6	LDA		5	3
93	SUBD		6	2	A5	BITA		4	2	B7	STA		5	3
94	ANDA		4	2	A6	LDA		4	2	B8	EORA		5	3
95	BITA		4	2	A7	STA		4	2	B9	ADCA		5	3
96	LDA		4	2	A8	EORA		4	2	BA	ORA		5	3
97	STA		4	2	A9	ADCA		4	2	BB	ADDA		5	3
98	EORA		4	2	AA	ORA		4	2	BC	CMPX		7	3
99	ADCA		4	2	AB	ADDA		4	2	BD	JSR		8	3
9A	ORA		4	2	AC	CMPX		6	2	BE	LDX		6	3
9B	ADDA		4	2	AD	JSR		7	2	BF	STX	EXTENDED	6	3
9C	CMPX		6	2	AE	LDX		5	2	C0	SUBB	IMMED	2	2
9D	JSR	DIRECT	7	2	AF	STX	INDEXED	5	2	C1	CMPB	IMMED	2	2

Instruction	Forms	Addressing Modes												Description	5 3 2 1 0					
		Immediate			Direct			Indexed ¹			Extended				H	N	Z	V	C	
ABX														3A 3 1	B + X - X (Unsigned)	•	•	•	•	
ADC	ADCA ADCB	89 2 2 99 4 2 A9 4+ 2+ B9 5 3													A + M + C - A	•	1	1	1	
	C9 2 2 D9	E9 4+ 2+ F9 5 3													B + M + C - B	•	1	1	1	
ADD	ADDA ADDB ADDD	8B 2 2 9B 4 2 AB 4+ 2+ BB 5 3													A + M - A	•	1	1	1	
	CB 2 2 DB	EB 4+ 2+ FB 5 3													B + M - B	•	1	1	1	
	C3 4 3 D3	E3 6+ 2+ F3 7 3													D + M + M + 1 - D	•	1	1	1	
AND	ANDA ANDB ANDCC	84 2 2 94 4 2 A4 4+ 2+ B4 5 3													A · M → A	•	1	1	0	
	C4 2 2 D4	E4 4+ 2+ F4 5 3													B · M → B	•	1	1	0	
	1C 3														CC A IMM - CC	•	1	1	1	
ASL	ASLA ASLB ASL															7	1	1	1	
		08 6 2 68 6+ 2+ 78 7 3													48 2 1	7	1	1	1	
															58 2	7	1	1	1	
ASR	ASRA ASRB ASR															7	1	1	1	
		07 6 2 67 6+ 2+ 77 7 3													47 2 1	7	1	1	1	
															57 2	7	1	1	1	
BIT	BITA BITB	85 2 2 95 4 2 A5 4+ 2+ B5 5 3													Bit Test A (M & A)	•	1	1	0	
	C5 2 2 DF	E5 4+ 2+ F5 5 3													Bit Test B (IM & B)	•	1	1	0	
CLR	CLRA CLRB CLR														4F 2 1	0 - A	•	0	1	0
		0F 6 2 6F 6+ 2+ 7F 7 3													5F 2	0 - B	•	0	1	0
																0 - M	•	0	1	0
CMP	CMPA CMPB CMRD	81 2 2 91 4 2 A1 4+ 2+ B1 5 3													Compare M from A	7	1	1	1	
	C1 2 2 D1	E1 4+ 2+ F1 5 3													Compare M from B	7	1	1	1	
	83 4 10 7 3	10 7+ 3+ 10 B 4													Compare M M + 1 from D	•	1	1	1	
	CMPS	11 5 4 11 7 3 11 7+ 3+ 11 8 4													Compare M M + 1 from S	•	1	1	1	
	CMPU	8C 5 4 11 7 3 11 7+ 3+ 11 8 4													Compare M M + 1 from U	•	1	1	1	
	CMPX	8C 4 3 9C 6 2 AC 6+ 2+ BC 7 3													Compare M M + 1 from X	•	1	1	1	
	CMPY	10 5 4 10 7 3 10 7+ 3+ 10 B 4													Compare M M + 1 from Y	•	1	1	1	

Instruction	Forms	Addressing Modes												Description	5 3 2 1 0					
		Immediate			Direct			Indexed ¹			Extended				H	N	Z	V	C	
COM	COMA COMB COM														A → A	•	1	1	0	
		43 2 1													B → B	•	1	1	0	
		53 2 1													M → M	•	1	1	0	
CWAI		3C ≥ 20 2													CC A IMM - CC Wait for Interrupt	7				
DAA															Decimal Adjust A	•	1	1	0	
DEC	DECA DEC B DEC														A - 1 → A	•	1	1	0	
		19 2 1													B - 1 → B	•	1	1	0	
		44 2 1													M - 1 → M	•	1	1	0	
EOR	EORA EORB	88 2 2 98 4 2 A8 4+ 2+ B8 5 3													A ⊜ M → A	•	1	1	0	
	C8 2 2 DB	E8 4+ 2+ FB 5 3													B ⊜ M → B	•	1	1	0	
EXG	R1, R2	1E 8 2													R1 → R2 ²	•	•	•	•	
INC	INCA INC B INC														A + 1 → A	•	1	1	1	
		4C 2 1													B + 1 → B	•	1	1	1	
		5C 2 1													M + 1 → M	•	1	1	0	
JMP		0E 3 2 6E 3+ 2+ 7E 4 3													EA ³ - PC	•	•	•	•	
JSR															Jump to Subroutine	•	•	•	•	
LD	LDA LDB LDD LDS	86 2 2 96 4 2 A6 4+ 2+ B6 5 3													M → A	•	1	1	0	
	C6 2 2 DC	E6 4+ 2+ F6 5 3													B → B	•	1	1	0	
	CC 3 3 DC	EC 5+ 2+ FC 6 3													M · M + 1 → D	•	1	1	0	
	10 4 4 10	10 6+ 3+ 10 7 4													M · M + 1 → S	•	1	1	0	
	CE	EE														M · M + 1 → U	•	1	1	0
	LDU	CE 3 3 DE	5 2 EE 5+ 2+ FE 6 3													MM · M + 1 → X	•	1	1	0
	LDX	BE 3 3 9E 5 2 AE 5+ 2+ BE 6 3														MM · M + 1 → Y	•	1	1	0
	LDY	10 4 4 10 6 3 10 6+ 3+ 10 7 4																		
LEA	LEAS LEAU LEAX LEAY														EA ³ - S	•	•	•	•	
		32 4+ 2+													EA ³ - U	•	•	•	•	
		33 4+ 2+													EA ³ - X	•	•	•	•	
		30 4+ 2+													EA ³ - Y	•	•	•	•	

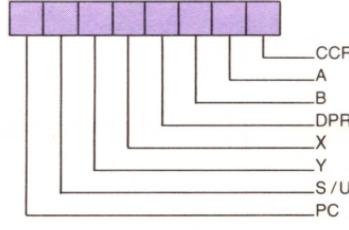
Instruction	Forms	Addressing Modes												Description	5 3 2 1 0					
		Immediate			Direct			Indexed ¹			Extended				H	N	Z	V	C	
LSL	LSLA LSLB LSL															•	1	1	1	
		48 2 1														•	1	1	1	
		58 2 1														•	1	1	1	
LSR	LSRA LSRB LSR															•	0	1	•	
		44 2 1													•	0	1	•	1	
		54 2 1														•	0	1	•	1
MUL															3D 11 1					
NEG	NEGA NEG B NEG														A × B → D (Unsigned)	•	1	1	0	
		40 2 1													A + 1 → A	7	1	1	1	
		50 2 1													B + 1 → B	7	1	1	1	
															M + 1 → M	7	1	1	1	
NOF															No Operation	•	•	•	•	
OR	ORA ORB ORCC	8A 2 2 9A 4 2 AA 4+ 2+ BA 5 3													A ∨ M → A	•	1	1	0	
		42 2 1													B ∨ M → B	•	1	1	0	
		50 2 1													CC V IMM - CC	6				
PSH	PSHS PSHU	34 5+ 2 91 4 2 91 4+ 2+ FF 6 3													Push Registers on S Stack	•	•	•	•	
		35 5+ 2 91 4 2 91 4+ 2+ FF 6 3													Push Registers on U Stack	•	•	•	•	
PUL	PULS PULU	35 5+ 2 91 4 2 91 4+ 2+ FF 6 3													Pull Registers from S Stack	•	•	•	•	
		37 5+ 2 91 4 2 91 4+ 2+ FF 6 3													Pull Registers from U Stack	•	•	•	•	
ROL	ROLA ROLB ROL															•	1	1	1	
		49 2 1														•	1	1	1	
		59 2 1														•	1	1	1	
ROR	RORA RORB ROR															•	1	1	1	
		46 2 1														•	1	1	1	
		56 2 1														•	1	1	1	
RTI															Return From Interrupt	6				
RTS															Return From Subroutine	•	•	•	•	
SBC	SBCA SBCB	82 2 2 92 4 2 A2 4+ 2+ B2 5 3													A - M - C → A	8	1	1	1	
	C2 2 2 D2	E2 4+ 2+ F2 5 3													B - M - C → B	8	1	1	1	
SEX															Sign Extend B into A	•	1	1	0	

| Instruction | Forms | Addressing Modes | | | | | | | | | | | | Description |
<th colspan
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |

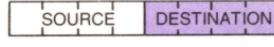
Notes:

- This column gives a base cycle and byte count. To obtain total count, add the values obtained from the INDEXED ADDRESSING MODES table.
- R1 and R2 may be any pair of 8 bit or any pair of 16 bit registers.
- The 8 bit registers are: A, B, CC, DP.
- The 16 bit registers are: X, Y, U, S, D, PC.
- EA is the effective address.
- The PSH and PUL instructions require 5 cycles plus 1 cycle for each byte pushed or pulled.
- SWI sets I and F bits. SWI2 and SWI3 do not affect I and F.
- Conditions Codes set as a direct result of the instruction.
- Value of half-carry flag is undefined.
- Special Case — Carry set if b7 is SET.

PUSH/PULL POST BYTE



TRANSFER/EXCHANGE POST BYTE



REGISTER FIELD (Source or Destination)

0000 = D (A:B)	0101 = PC
0001 = X	1000 = A
0010 = Y	1001 = B
0011 = U	1010 = CCR
0100 = S	1011 = DPR

INDEXED ADDRESSING MODES

Type	Forms	Non Indirect				Indirect			
		Assembler Form	Postbyte OP Code	x	#	Assembler Form	Postbyte OP Code	+	#
Constant Offset From R (twos complement offset)	No Offset	.R	1RR00100	0	0	[R]	1RR10100	3	0
	5 Bit Offset	n. R	0RRnnnnn	1	0	[n, R]	1RR11000	4	1
	8 Bit Offset	n. R	1RR01000	1	1	[n, R]	1RR11001	4	1
	16 Bit Offset	n. R	1RR01001	4	2	[n, R]	1RR11001	7	2
Accumulator Offset From R (twos complement offset)	A — Register Offset	A. R	1RR00110	1	0	[A, R]	1RR10110	4	0
	B — Register Offset	B. R	1RR00101	1	0	[B, R]	1RR10101	4	0
	D — Register Offset	D. R	1RR01011	4	0	[D, R]	1RR11011	7	0
Auto Increment/Decrement R	Increment By 1	.R+	1RR00000	2	0	not allowed			
	Increment By 2	.R++	1RR00001	3	0	[.R+]	1RR10001	6	0
	Decrement By 1	.R-	1RR00010	2	0	not allowed			
	Decrement By 2	.R--	1RR00011	3	0	[.R--]	1RR10011	6	0
Constant Offset From PC (twos complement offset)	8 Bit Offset	n. PCR	1XX01100	1	1	[n, PCR]	1XX11100	4	1
	16 Bit Offset	n. PCR	1XX01101	5	2	[n, PCR]	1XX11101	8	2
Extended Indirect	16 Bit Address	—	—	—	—	[n]	10011111	5	2

R = X, Y, U or S X = 00 Y = 01
X = Don't Care U = 10 S = 11

+ and # Indicate the number of additional cycles and bytes for the particular variation.

BRANCH INSTRUCTIONS

Instruction	Forms	Addressing Mode		Description	5 3 2 1 0				
		OP	Relative		H	N	Z	V	C
BCC	BCC	24	3	2	Branch C = 0	•	•	•	•
	LBCC	24	5(6)	4	Long Branch C = 0	•	•	•	•
BCS	BCS	25	3	2	Branch C = 1	•	•	•	•
	LBCS	10	5(6)	4	Long Branch C = 1	•	•	•	•
BEQ	BEQ	27	3	2	Branch Z = 1	•	•	•	•
	LBEQ	10	5(6)	4	Long Branch Z = 1	•	•	•	•
BGE	BGE	2C	3	2	Branch ≥ Zero	•	•	•	•
	LBGE	10	5(6)	4	Long Branch ≥ Zero	•	•	•	•
BGT	BGT	2E	3	2	Branch > Zero	•	•	•	•
	LBGT	10	5(6)	4	Long Branch > Zero	•	•	•	•
BHI	BHI	22	3	2	Branch Higher	•	•	•	•
	LBHI	10	5(6)	4	Long Branch Higher	•	•	•	•
BHS	BHS	24	3	2	Branch Higher or Same	•	•	•	•
	LBHS	10	5(6)	4	Long Branch Higher or Same	•	•	•	•
BLE	BLE	2F	3	2	Branch ≤ Zero	•	•	•	•
	LBLE	10	5(6)	4	Long Branch ≤ Zero	•	•	•	•
BLO	BLO	25	3	2	Branch lower	•	•	•	•
	LBLO	10	5(6)	4	Long Branch Lower	•	•	•	•

Instruction	Forms	Addressing Mode		Description	5 3 2 1 0				
		OP	Relative		H	N	Z	V	C
BLS	BLS	23	3	2	Branch Lower or Same	•	•	•	•
	LBLS	10	5(6)	4	Long Branch Lower or Same	•	•	•	•
BLT	BLT	2D	3	2	Branch < Zero	•	•	•	•
	LBLT	10	5(6)	4	Long Branch < Zero	•	•	•	•
BMI	BMI	28	3	2	Branch Minus	•	•	•	•
	LBMI	10	5(6)	4	Long Branch Minus	•	•	•	•
BNE	BNE	26	3	2	Branch Z = 0	•	•	•	•
	LBNE	10	5(6)	4	Long Branch Z = 0	•	•	•	•
BPL	BPL	2A	2	2	Branch Plus	•	•	•	•
	LBPL	10	5(6)	4	Long Branch Plus	•	•	•	•
BRA	BRA	20	3	2	Branch Always	•	•	•	•
	LBRA	16	5	3	Long Branch Always	•	•	•	•
BRN	BRN	21	3	2	Branch Never	•	•	•	•
	LBRN	10	5	4	Long Branch Never	•	•	•	•
BSR	BSR	8D	7	2	Branch to Subroutine	•	•	•	•
	LBSR	17	9	3	Long Branch to Subroutine	•	•	•	•
BVC	BVC	28	3	2	Branch V = 0	•	•	•	•
	LBVC	10	5(6)	4	Long Branch V = 0	•	•	•	•
BVS	BVS	29	3	2	Branch V = 1	•	•	•	•
	LBVS	10	5(6)	4	Long Branch V = 1	•	•	•	•

SIMPLE BRANCHES

OP	-	#
BRA	20	3
LBRA	16	5
BRN	21	3
LBRN	1021	5
BSR	8D	7
LBSR	17	9

SIMPLE CONDITIONAL BRANCHES (NOTES 1-4)

Test	True	OP	False	OP
N = 1	BMI	2B	BPL	2A
Z = 1	BEQ	27	BNE	26
V = 1	BVS	29	BVC	28
C = 1	BCS	25	BCC	24

SIGNED CONDITIONAL BRANCHES (NOTES 1-4)

Test	True	OP	False	OP
r > m	BGT	2E	BLE	2F
r ≥ m	BGE	2C	BLT	2D
r = m	BEQ	27	BNE	26
r ≤ m	BLE	2F	BGT	2E
r < m	BLT	2D	BGE	2C

UNSIGNED CONDITIONAL BRANCHES (NOTES 1-4)

Test	True	OP	False	OP
r > m	BHI	22	BLS	23
r ≥ m	BHS	24	BLO	25
r = m	BEQ	27	BNE	26
r ≤ m	BLS	23	BHI	22
r < m	BLO	25	BHS	24

Notes:

- All conditional branches have both short and long variations.
- All short branches are 2 bytes and require 3 cycles.
- All conditional long branches are formed by prefixing the short branch opcode with \$10 and using a 16-bit destination offset.
- All conditional long branches require 4 bytes and 6 cycles if the branch is taken or 5 cycles if the branch is not taken.