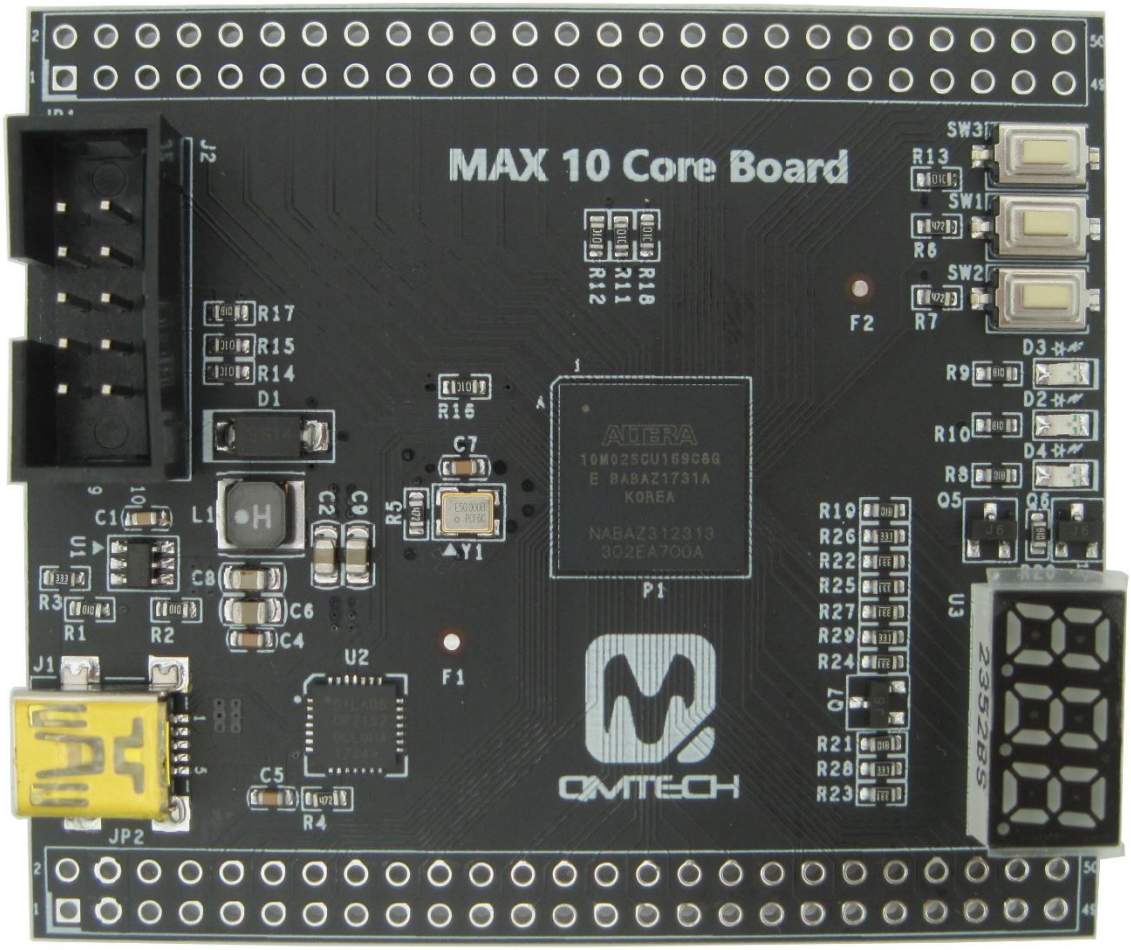
QM_MAX10_10M02SCU169 BOARD

USER MANUAL



Preface

The QM_MAX10_10M02SCU169 development board uses Intel® MAX® 10 FPGAs. MAX 10 FPGAs revolutionize non-volatile integration by delivering advanced processing capabilities in a low-cost, single chip small form factor programmable logic device. Building upon the single chip heritage of previous MAX device families, densities range from 2K – 50K LEs, using either single or dual-core voltage supplies. The MAX 10 FPGA family encompasses both advanced small wafer scale packaging (3 mm x 3 mm) and high I/O pin count packages offerings.

Table of Contents

1. Introduction

1.1 Document Scope

This demo user manual introduces the QM_MAX10_10M02SCU169 development board and describes how to setup the development board running with application software Altera Quartus II 15.1. Users may employee the on board rich logic resource CPLD 10M02SCU169C8G to implement various applications. The core board also has 88 non-multiplexed CPLD IOs for extending customized modules, such as UART module, CMOS/CCD camera module, LCD/HDMI/VGA display module etc.

1.2 Kit Overview

Below section lists the parameters of the QM_MAX10_10M02SCU169:

- On-Board CPLD: 10M02SCU169C8G;
- On-Board CPLD external crystal frequency: 50MHz;
- 10M02SCU169C8G has rich block RAM resource;
- 10M02SCU169C8G has 2K Logic elements;
- QM_MAX10_10M02SCU169 has USB to UART Serial Port by using Silicon Labs' CP2102-GMR chip;
- QM_MAX10_10M02SCU169 has 3.3V power supply by using MP2359 wide input range DC/DC;
- QM_MAX10_10M02SCU169 has two 50p, 2.54mm pitch headers for extending user IOs;
- QM_MAX10_10M02SCU169 has 3 user switches;
- QM_MAX10_10M02SCU169 has 3 user LEDs;
- QM_MAX10_10M02SCU169 has JTAG interface, by using 10p, 2.54mm pitch header;
- QM_MAX10_10M02SCU169 PCB size is 5.7cm x 6.6cm;
- QM_MAX10_10M02SCU169 default power source is provided by Mini-USB cable;

1.3 Kit Top View

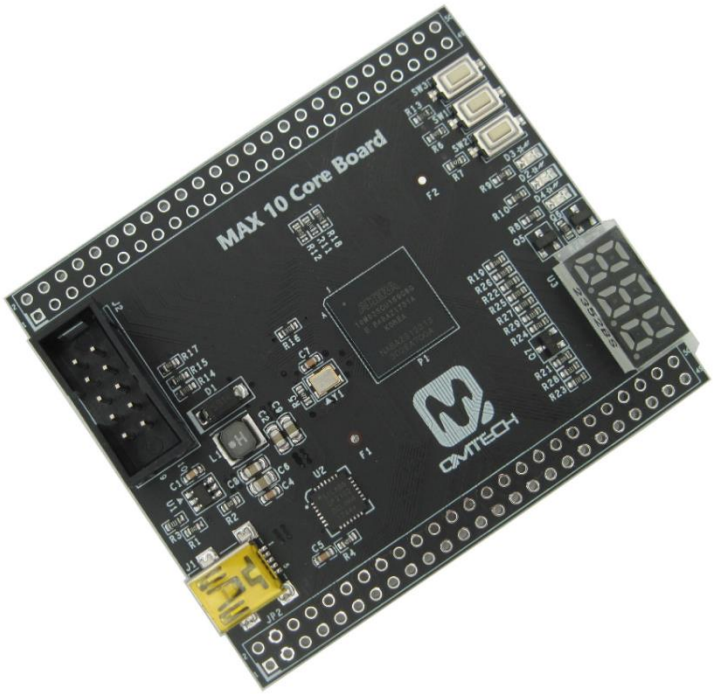


Figure 1-1. QM_MAX10_10M02SCU169 Top View

2. Getting Started

Below image shows the dimension of the QM_MAX10_10M02SCU169 core board: 66.2mm x 57mm. The unit in below image is millimeter(mm).

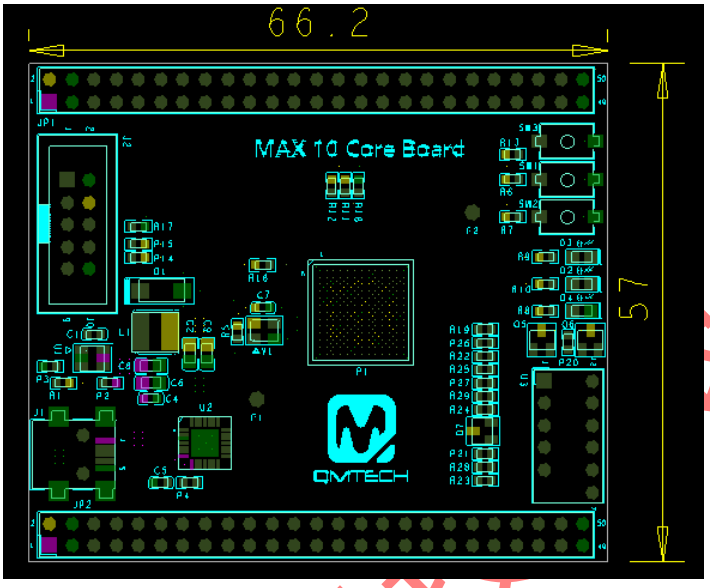
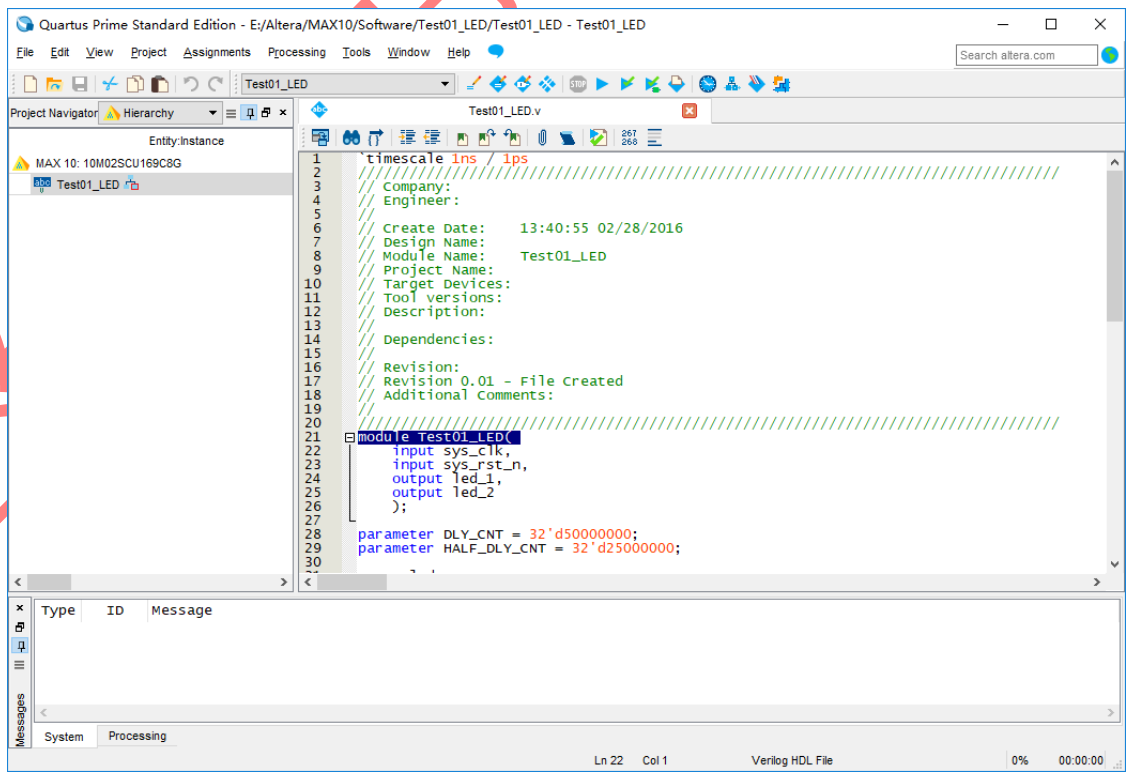


Figure 2-1. QM_MAX10_10M02SCU169 Dimension

The QM_MAX10_10M02SCU169 development board tool chain consists of Altera Quartus II 15.1, Altera USB Blaster cable, 10M02SCU169 development board and Mini-USB cable for power supply. Below image shows the Altera Quartus II 15.1 development environment which could be downloaded from Altera(Intel) office website:



2.2 QM_MAX10_10M02SCU169 Hardware Design

2.2.1 QM_MAX10_10M02SCU169 Power Supply

The development board needs 5V DC input as power supply which could be directly injected from Mini-USB cable or the 50P header JP1/JP2. Users may refer to the hardware schematic for the detailed design. The on board LED D4 indicates the 3.3V supply status, it will be turned on when the 5V power supply is active. In default status, all the CPLD banks IO power level is 3.3V because bank power supply is 3.3V.

Note: the CPLD power supply 3.3V is regulated by MPS DC/DC chip MP2359 which could output maximum 1.2A current.

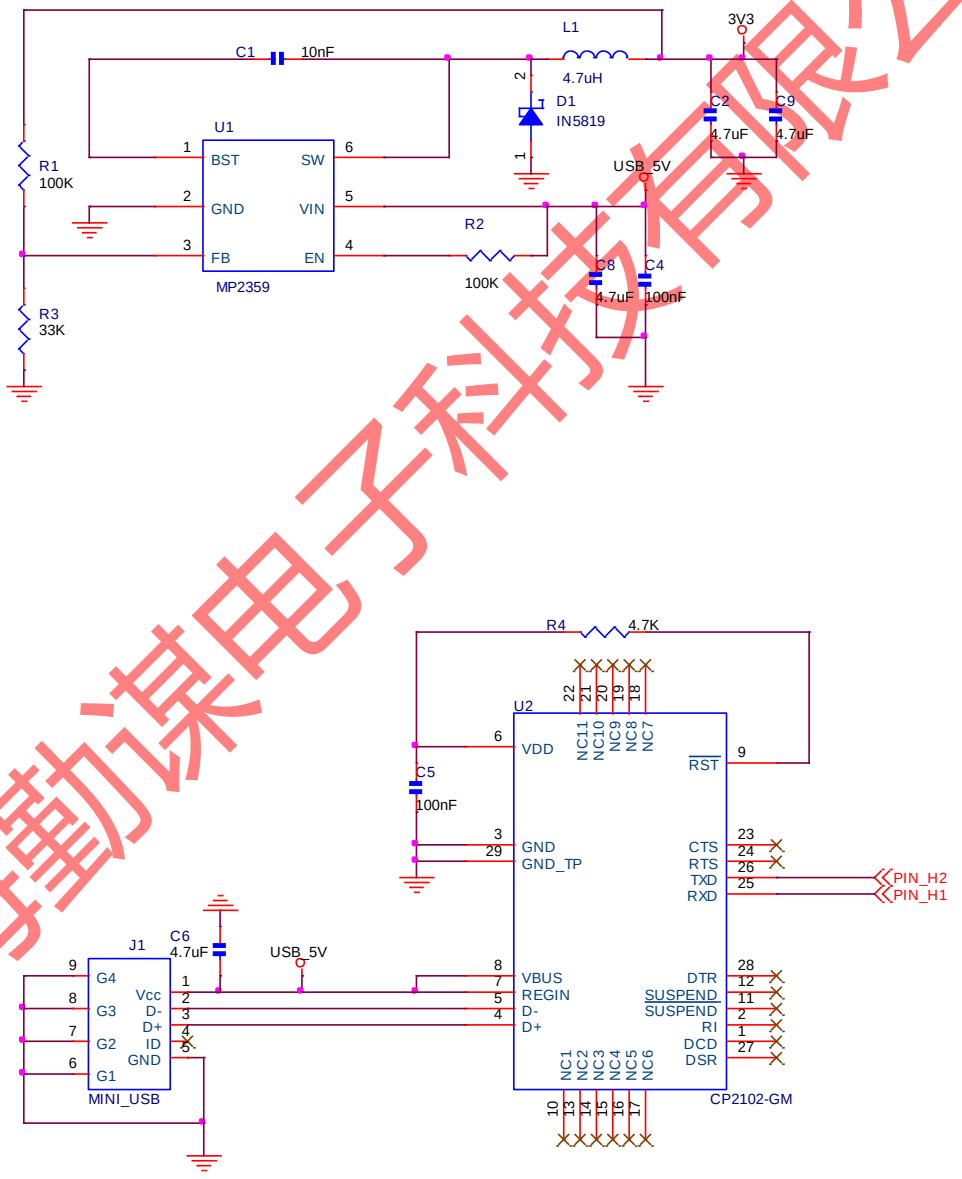


Figure 2-2. Power Supply

2.2.2 QM_MAX10_10M02SCU169 System Clock

The QM_MAX10_10M02SCU169 has system clock frequency 50MHz which is directly provided by external crystal. The crystal is designed with high accuracy and stability with low temperature drift 10ppm/°c. Below image shows the detailed hardware design:

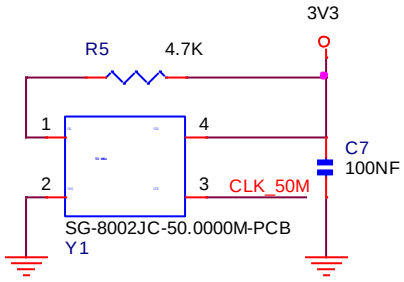


Figure 2-3. 50MHz System Clock

2.2.1 QM_MAX10_10M02SCU169 JTAG Port

The on board JTAG port uses 10P 2.54mm pitch header which could be easily connected to Altera USB blaster cable. Below image shows the hardware design of the JTAG port:

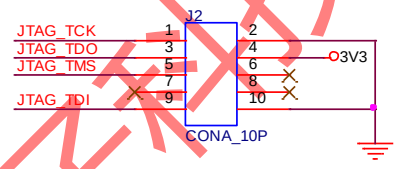


Figure 2-4. JTAG Port

2.2.2 QM_MAX10_10M02SCU169 USB to Serial Port

The CP2102-GMR is an USB 2.0 to serial port bridge chip designed by Silicon Labs. Below figure shows the hardware design of CP2102-GMR on the QM_MAX10_10M02SCU169 development board.

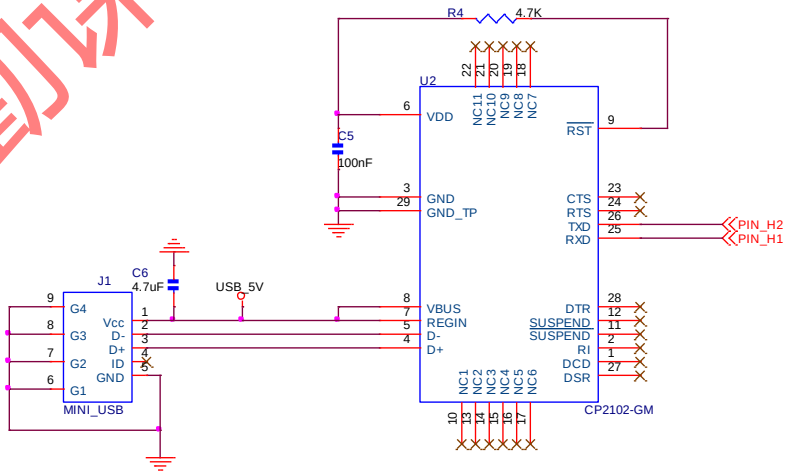


Figure 2-5. CP2102 Hardware Design

2.2.3 QM_MAX10_10M02SCU169 Extension IO

The development board has two 50P 2.54mm pitch headers which are used for extending user modules, such as ADC/DAC module, audio/video module, ethernet module, etc.

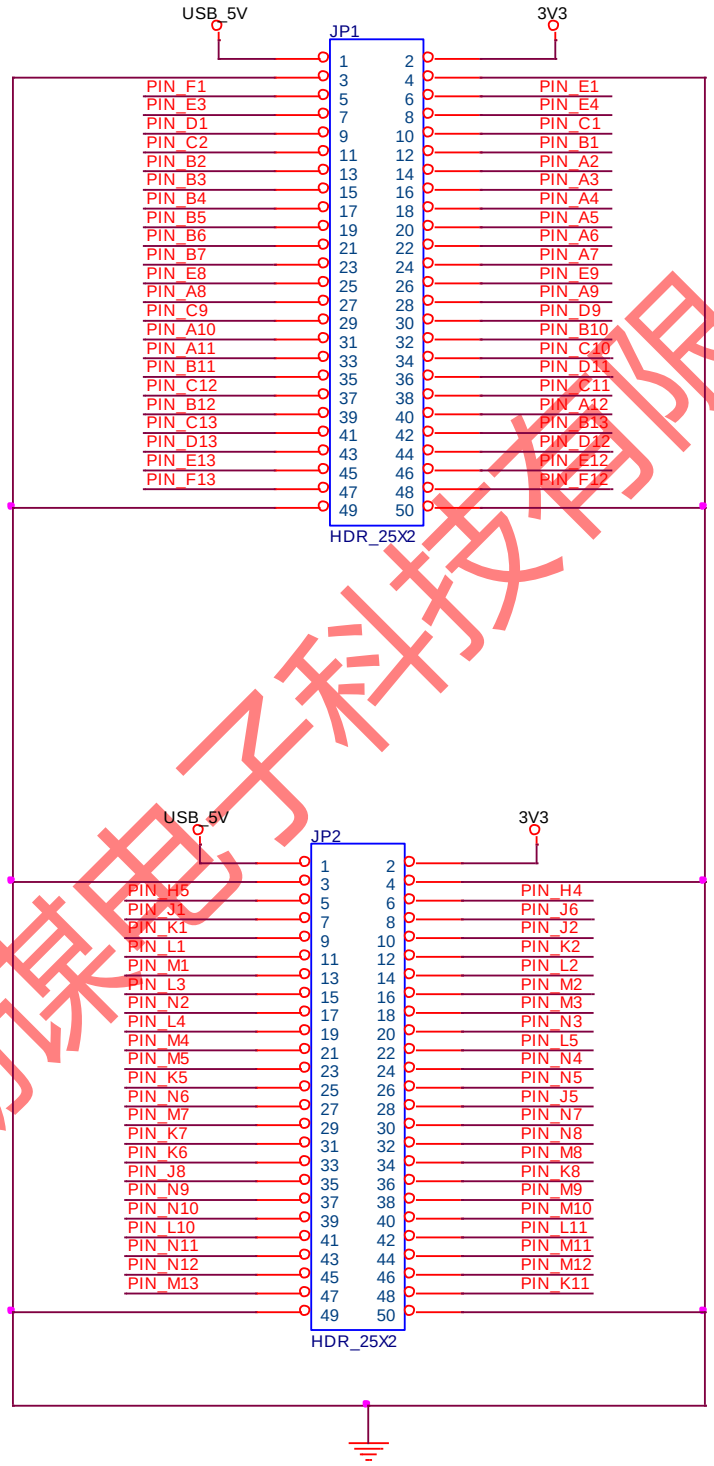


Figure 2-6. Extension IO

2.2.4 QM_MAX10_10M02SCU169 User LED

Below image shows two user LEDs and one 3.3V power supply indicator LED:

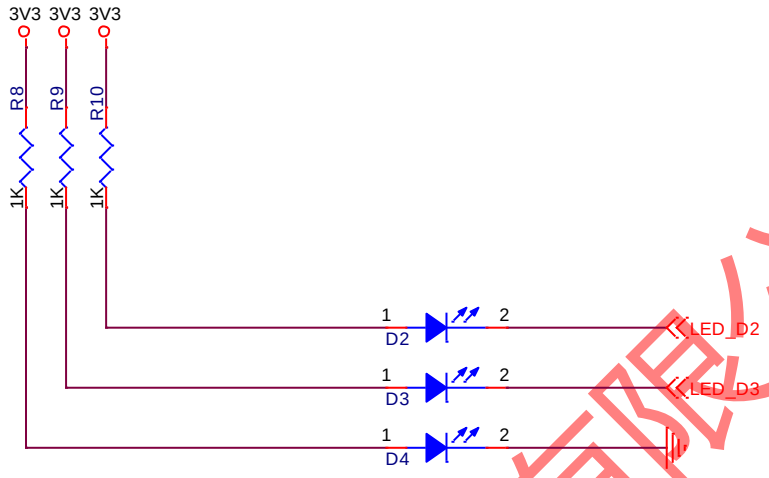


Figure 2-7. User LEDs

2.2.5 QM_MAX10_10M02SCU169C8G User Key

Below image shows the nCONFIG key and two user keys:

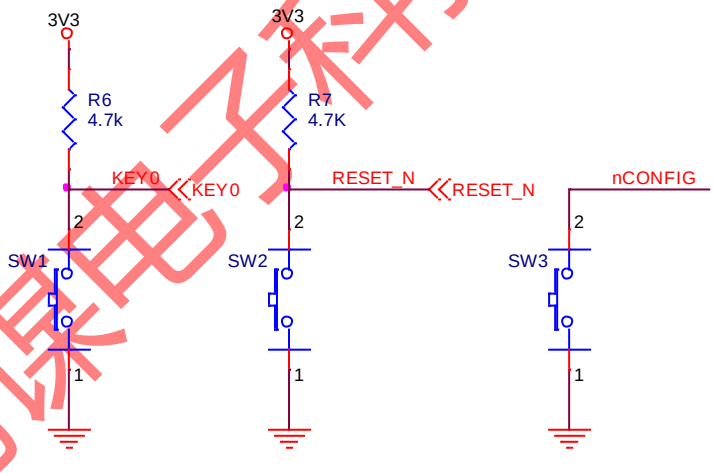


Figure 2-8. 用户按键和复位按键电路

2.2.6 QM_MAX10_10M02SCU169C8G 7-SEG LED

Below image shows three digits 7-SEG LEDs:

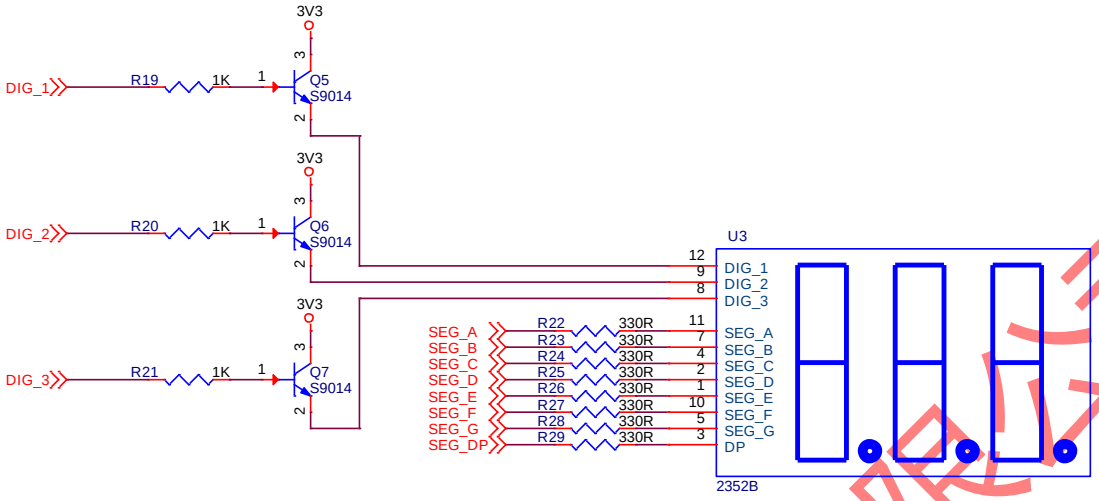


Figure 2-9. 7-SEG LEDs

3. Reference

[1] max10-10m02_08_core_board_v01.pdf
[2] m10_datasheet.pdf
[3] m10_handbook.pdf
[4] m10_overview.pdf
[5] ug_m10_adc.pdf
[6] pcg-01014_Cyclone® V Device Family Pin Connection Guidelines.pdf
[7] Intel® MAX® 10 FPGA Device Family Pin Connection Guidelines

4. Revision

Doc. Rev.	Date	Comments
0.1	01/04/2018	Initial Version.
1.0	22/04/2018	V1.0 Formal Release.