

## 2Gb DDR3 SDRAM

Lead-Free&Halogen-Free

(RoHS Compliant)

H5TQ2G83BFR-xxC

H5TQ2G83BFR-xxI

H5TQ2G83BFR-xxL

H5TQ2G83BFR-xxJ

H5TQ2G63BFR-xxC

H5TQ2G63BFR-xxI

H5TQ2G63BFR-xxL

H5TQ2G63BFR-xxJ

<sup>\*</sup> Hynix Semiconductor reserves the right to change products or specifications without notice.



## **Revision History**

Revision No.	History	Draft Date	Remark
0.1	Initial Release	Dec. 2009	
0.2	Added IDD Specification	Feb. 2010	
1.0	Add supported CL5	Jun. 2010	
1.1	Modify the package outline with x16	Jun. 2010	
1.2	2 Low power added		
1.3	M8 pin ball out update	Sep. 2010	
1.4	Added 1866 speed Suppport	Nov. 2010	
1.5	Added 2133 speed Suppport	Dec. 2010	
1.6	Added IDD Specification(2133 speed)	Dec. 2010	
1.7	Modify OPERATING FREQUENCY Table	Dec. 2010	
1.8	Added J and L-part support	Jul. 2011	

### **Description**

The H5TQ2G83BFR and H5TQ2G63BFR are 2,147,483,648-bit CMOS Double Data Rate III (DDR3) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth. Hynix 2Gb DDR3 SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

#### **Device Features and Ordering Information**

#### **FEATURES**

- VDD=VDDQ=1.5V +/- 0.075V
- Fully differential clock inputs (CK, CK) operation
- Differential Data Strobe (DQS, DQS)
- On chip DLL align DQ, DQS and DQS transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 5, 6, 7, 8, 9, 10, 11, 12, 13 and 14 supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8, 9, 10
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly

- 8banks
- Average Refresh Cycle (Tcase of 0 °C~95 °C)
  - 7.8  $\mu$ s at 0°C ~ 85 °C
- 3.9 μs at 85°C ~ 95 °C Commercial Temperature (0 °C~ 85 °C) Industrial Temperature ( -40°C~ 85 °C)
- · Auto Self Refresh supported
- JEDEC standard 82ball FBGA(x8), 96ball FBGA (x16)
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- · Asynchronous RESET pin supported
- · ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- · Write Levelization supported
- 8 bit pre-fetch

<sup>\*</sup> This product in compliance with the RoHS directive.



#### **ORDERING INFORMATION**

Part No.	Configuration	Power Consumption	Temperature	Package
H5TQ2G83BFR-*xxC		Normal Consumption – 256M x 8  Low Power Consumption		
H5TQ2G83BFR-*xxI	254M v 0			82ball FBGA
H5TQ2G83BFR-*xxL	230W X 6			OZDAII I DGA
H5TQ2G83BFR-*xxJ		(IDD6 Only)	Industrial	
H5TQ2G63BFR-*xxC		Normal Consumption	Commercial	
H5TQ2G63BFR-*xxI	128M x 16	Normal Consumption	Industrial	96ball FBGA
H5TQ2G63BFR-*xxL	120W X 10	Low Power Consumption	Commercial	70Dail FDGA
H5TQ2G63BFR-*xxJ		(IDD6 Only)	Industrial	

<sup>\*</sup> xx means Speed Bin Grade

#### **OPERATING FREQUENCY**

Speed Grade			Remark								
(Marking)	CL5	CL6	CL7	CL8	CL9	CL10	CL11	CL12	CL13	CL14	(CL-tRCD-tRP)
-G7	0	0	0	0							DDR3-1066 7-7-7
-H9	0	0	0	0	0	0					DDR3-1333 9-9-9
-PB	0	0	0	0	0	0	0				DDR3-1600 11-11-11
-RD		0		0		0		0	0		DDR3-1866 13-13-13
-TE	0	0	0	0	0	0	0	0	0	0	DDR3-2133 14-14-14

<sup>\*</sup> xx means Speed Bin Grade



### Package Ballout/Mechanical Dimension

x8 Package Ball out (Top view): 82ball FBGA Package

	1	2	3	4	5	6	7	8	9	10	11	
Α	NC	vss	VDD	NC	]			NF/TDQS	vss	VDD	NC	Α
В		VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ		В
С		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ		С
D		VSSQ	DQ6	DQS				VDD	VSS	VSSQ		D
E		VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ		E
F		NC	VSS	RAS				СК	VSS	NC		F
G		ODT	VDD	CAS				СК	VDD	CKE		G
Н		NC	cs	WE				A10/AP	ZQ	NC		н
J		VSS	BA0	BA2				NC	VREFCA	VSS		J
K		VDD	А3	A0				A12/BC	BA1	VDD		K
L		VSS	A5	A2				A1	A4	VSS		L
M		VDD	A7	A9				A11	A6	VDD		M
N	NC	VSS	RESET	A13				A14	A8	VSS	NC	N
	1	2	3	4	5	6	7	8	9	10	11	

	1 2 3 4	8 9 10 11	
A B C D E F G H J K L M N	000000000000000000000000000000000000000	000000000000000000000000000000000000000	(Tα ○ +

(Top View: See the balls through the Package)

- Populated ball
- + Ball not populated

### x16 Package Ball out (Top view): 96ball FBGA Package

		1	2	3	4	5	6	7	8	9	
	_										
Α		VDDQ	DQU5	DQU7				DQU4	VDDQ	vss	Α
В		VSSQ	VDD	vss				DQSU	DQU6	VSSQ	В
С		VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ	С
D		VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD	D
Е		vss	VSSQ	DQL0				DML	VSSQ	VDDQ	Е
F		VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ	F
G		VSSQ	DQL6	DQSL				VDD	vss	VSSQ	G
Н		VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ	Н
J		NC	vss	RAS				СК	vss	NC	J
K		ODT	VDD	CAS				CK	VDD	CKE	K
L		NC	cs	WE				A10/AP	ZQ	NC	L
М		vss	BA0	BA2				NC	VREFCA	vss	M
N		VDD	А3	A0				A12/BC	BA1	VDD	N
Р		vss	A5	A2				A1	A4	vss	Р
R		VDD	A7	A9				A11	A6	VDD	R
Т		vss	RESET	A13				NC	A8	vss	Т
	_										
		1	2	3	4	5	6	7	8	9	

	1 2 3	7 8 9	_
Α	00	000	
В	000	000	
С	000	000	
D	000	000	
Ε	000	000	
F	000	000	
G	000	000	(Top View: Se
Н	000	000	
J	000	000	<ul> <li>Populated b</li> </ul>
K	000	000	+ Ball not pop
L	000	000	
M	000	000	
N	000	000	
Р	000	000	
R	000	000	
T	000	000	

see the balls through the Package)

- ball
- pulated



### **Pin Functional Description**

Symbol	Туре	Function
CK, CK	Input	Clock: CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{\text{CK}}$ .
CKE, (CKE0), (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{\text{CK}}$ , ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS, (CS0), (CS1), (CS2), (CS3)	Input	Chip Select: All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT, (ODT0), (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS and DM/TDQS, NU/TDQS (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration, ODT is applied to each DQ, DQSU, DQSU, DQSL, DQSL, DMU, and DML signal. The ODT pin will be ignored if MR1 is programmed to disable ODT.
RAS. CAS. WE	Input	Command Inputs: $\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$ ) define the command being entered.
DM, (DMU), (DML)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/TDQS is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.
A0 - A15	Input	Address Inputs: Provide the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC have additional functions, see below).  The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC	Input	Burst Chop: A12 / $\overline{BC}$ is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.



Symbol	Туре	Function
RESET	Input	Active Low Asynchronous Reset: Reset is active when RESET is LOW, and inactive when RESET is HIGH. RESET must be HIGH during normal operation.  RESET is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of V <sub>DD</sub> , i.e. 1.20V for DC high and 0.30V for DC low.
DQ	Input / Output	Data Input/ Output: Bi-directional data bus.
DQU, DQL, DQS, DQS, DQSU, DQSU, DQSL, DQSL	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS, DQSL, and DQSU are paired with differential signals DQS, DQSL, and DQSU, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
TDQS, TDQS	Output	Termination Data Strobe: TDQS/ $\overline{\text{TDQS}}$ is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/ $\overline{\text{TDQS}}$ that is applied to DQS/ $\overline{\text{DQS}}$ . When disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and $\overline{\text{TDQS}}$ is not used. x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
NC		No Connect: No internal electrical connection is present.
NF		No Function
V <sub>DDQ</sub>	Supply	DQ Power Supply: 1.5 V +/- 0.075 V
V <sub>SSQ</sub>	Supply	DQ Ground
V <sub>DD</sub>	Supply	Power Supply: 1.5 V +/- 0.075 V
V <sub>SS</sub>	Supply	Ground
V <sub>REFDQ</sub>	Supply	Reference voltage for DQ
V <sub>REFCA</sub>	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

#### Note:

Input only pins (BA0-BA2, A0-A15, RAS, CAS, WE, CS, CKE, ODT, DM, and RESET) do not supply termination.



#### **ROW AND COLUMN ADDRESS TABLE**

#### 2Gb

Configuration	256Mb x 8	128Mb x 16
# of Banks	8	8
Bank Address	BAO - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP
BL switch on the fly	A12/BC	A12/BC
Row Address	A0 - A14	A0 - A13
Column Address	A0 - A9	A0 - A9
Page size <sup>1</sup>	1 KB	2 KB

**Note1:** Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated as follows:

page size =  $2^{COLBITS} * ORG \div 8$ 

where COLBITS = the number of column address bits, ORG = the number of I/O (DQ) bits



### **Absolute Maximum Ratings**

#### **Absolute Maximum DC Ratings**

#### **Absolute Maximum DC Ratings**

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 0.4 V ~ 1.975 V	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.4 V ~ 1.975 V	V	1,3
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pin relative to Vss	- 0.4 V ~ 1.975 V	V	1
T <sub>STG</sub>	Storage Temperature	-55 to +100	°C	1, 2

#### Notes:

- 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- 3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6XVDDQ,When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

# DRAM Component Operating Temperature Range Temperature Range

Symbol	Parameter	Rating	Units	Notes
	Normal Operating Temperature Range	0 to 85	°C	1,2
OPER	Extended Temperature Range (Optional)	85 to 95	°C	1,3

#### Notes:

- 1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
- 2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 85°C under all operating conditions.
- 3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
  - a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to  $3.9 \, \mu s$ . It is also possible to specify a component with 1X refresh (tREFI to  $7.8 \mu s$ ) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability
  - b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).



### **AC & DC Operating Conditions**

### **Recommended DC Operating Conditions**

#### **Recommended DC Operating Conditions**

	_		Rating			
Symbol	Parameter	Min.	Тур.	Max.	Units	Notes
VDD	Supply Voltage	1.425	1.500	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.500	1.575	V	1,2

#### Notes:

- 1. Under all conditions, VDDQ must be less than or equal to VDD.
- 2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.



# IDD and IDDQ Specification Parameters and Test Conditions IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. Figure 1. shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Attention: IDDQ values cannot be directly used to calculate IO power of the DDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 2. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply:

- "0" and "LOW" is defined as VIN <= V<sub>ILAC(max)</sub>.
- "1" and "HIGH" is defined as VIN >= V<sub>IHAC(max)</sub>.
- "MID\_LEVEL" is defined as inputs are VREF = VDD/2.
- Timing used for IDD and IDDQ Measurement-Loop Patterns are provided in Table 1.
- Basic IDD and IDDQ Measurement Conditions are described in Table 2.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 3 through Table 10.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting

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RON = RZQ/7 (34 Ohm in MR1);

Qoff = O_B (Output Buffer enabled in MR1);

RTT_Nom = RZQ/6 (40 Ohm in MR1);

RTT_Wr = RZQ/2 (120 Ohm in MR2);

TDQS Feature disabled in MR1
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- Attention: The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D =  $\{\overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE}\}:= \{HIGH, LOW, LOW, LOW\}$
- Define  $\overline{D} = {\overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE}} := {HIGH, HIGH, HIGH}$

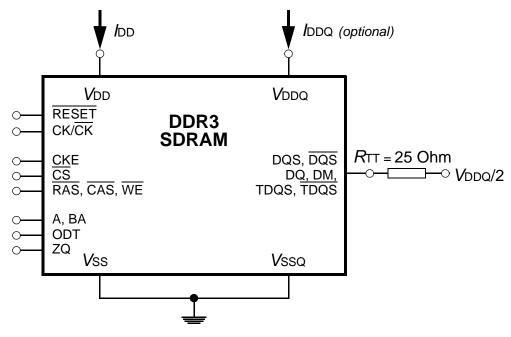


Figure 1 - Measurement Setup and Test Load for IDD and IDDQ (optional) Measurements [Note: DIMM level Output test load condition may be different from above]

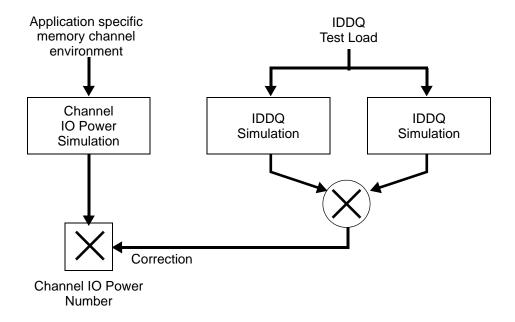


Figure 2 - Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement



Table 1 -Timings used for IDD and IDDQ Measurement-Loop Patterns

Symbol		DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Limit
	Symbol	7-7-7	9-9-9	11-11-11	13-13-13	14-14-14	Unit
$t_{CK}$		1.875	1.5	1.25	1.07	0.935	ns
CL		7	9	11	13	14	nCK
$n_{\rm RCD}$		7	9	11	13	14	nCK
$n_{\rm RC}$		27	33	39	45	50	nCK
$n_{RAS}$		20	24	28	32	36	nCK
$n_{\rm RP}$		7	9	11	13	14	nCK
n	1KB page size	20	20	24	26	27	nCK
n <sub>FAW</sub>	2KB page size	27	30	32	33	38	nCK
-	1KB page size	4	4	5	5	6	nCK
$n_{\rm RRD}$	2KB page size	6	5	6	6	7	nCK
n <sub>RFC</sub> -	512Mb	48	60	72	85	97	nCK
n <sub>RFC</sub> -	l Gb	59	74	88	103	118	nCK
n <sub>RFC</sub> -	2 Gb	86	107	128	150	172	nCK
n <sub>RFC</sub> -		160	200	240	281	321	nCK
n <sub>RFC</sub> -	8 Gb	187	234	280	328	375	nCK

Table 2 -Basic IDD and IDDQ Measurement Conditions

Symbol	Description
	Operating One Bank Active-Precharge Current
	CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 1; BL: 8 <sup>a</sup> ); AL: 0; CS: High between ACT
/	and PRE; Command, Address, Bank Address Inputs: partially toggling according to Table 3; Data IO:
/ <sub>DD0</sub>	MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2, (see
	Table 3); Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0; Pattern Details:
	see Table 3.
	Operating One Bank Active-Precharge Current
	CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 1; BL: 8 <sup>a</sup> ); AL: 0; CS: High between
I <sub>DD1</sub>	ACT, RD and PRE; Command, Address; Bank Address Inputs, Data IO: partially toggling according to
<b>7</b> DD1	Table 4; DM: stable at 0; Bank Activity: Cycling with on bank active at a time: 0,0,1,1,2,2, (see Table
	4); Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0; Pattern Details: see
	Table 4.

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Symbol	Description
	Precharge Standby Current
	CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; CS: stable at 1; Command, Address,
/ <sub>DD2N</sub>	Bank Address Inputs: partially toggling according to Table 5; Data IO: MID_LEVEL; DM: stable at 0;
	Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable
	at 0; Pattern Details: see Table 5.
	Precharge Standby ODT Current
	CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a</sup> ); AL: 0; CS: stable at 1; Command, Address,
I <sub>DD2NT</sub>	Bank Address Inputs: partially toggling according to Table 6; Data IO: MID_LEVEL; DM: stable at 0;
	Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: tog-
	gling according to Table 6; Pattern Details: see Table 6.
	Precharge Power-Down Current Slow Exit
	CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{\text{CS}}$ : stable at 1; Command, Address,
I <sub>DD2P0</sub>	Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed;
	Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0; Precharge Power Down
	Mode: Slow Exit <sup>c)</sup>
	Precharge Power-Down Current Fast Exit
	CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; CS: stable at 1; Command, Address,
I <sub>DD2P1</sub>	Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed;
	Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0; Precharge Power Down
	Mode: Fast Exit <sup>c)</sup>
	Precharge Quiet Standby Current
I <sub>DD2Q</sub>	CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a</sup> ); AL: 0; CS: stable at 1; Command, Address,
DDZQ	Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed;
	Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0
	Active Standby Current
	CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a</sup> ); AL: 0; CS: stable at 1; Command, Address,
/ <sub>DD3N</sub>	Bank Address Inputs: partially toggling according to Table 5; Data IO: MID_LEVEL; DM: stable at 0;
	Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable
	at 0; Pattern Details: see Table 5.

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Symbol	Description
	Active Power-Down Current
I <sub>DD3P</sub>	CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks open;
	Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0
	Operating Burst Read Current
<b>J</b> <sub>DD4R</sub>	CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a</sup> ); AL: 0; CS: High between RD; Command, Address, Bank Address Inputs: partially toggling according to Table 7; Data IO: seamless read data burst with different data between one burst and the next one according to Table 7; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,(see Table 7); Output Buffer and RTT: Enabled in Mode Registers <sup>b</sup> ); ODT Signal: stable at 0; Pattern Details: see Table 7.
	Operating Burst Write Current
/ <sub>DD4W</sub>	CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a</sup> ); AL: 0; CS: High between WR; Command, Address, Bank Address Inputs: partially toggling according to Table 8; Data IO: seamless read data burst with different data between one burst and the next one according to Table 8; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,(see Table 8); Output Buffer and RTT: Enabled in Mode Registers <sup>b</sup> ); ODT Signal: stable at HIGH; Pattern Details: see Table 8.
	Burst Refresh Current
/ <sub>DD5B</sub>	CKE: High; External clock: On; tCK, CL, nRFC: see Table 1; BL: 8 <sup>a</sup> ); AL: 0; $\overline{\text{CS}}$ : High between REF; Command, Address, Bank Address Inputs: partially toggling according to Table 9; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: REF command every nREF (see Table 9); Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0; Pattern Details: see Table 9.
	Self-Refresh Current: Normal Temperature Range
/ <sub>DD6</sub>	<b>7</b> <sub>CASE</sub> : 0 - 85 °C; Auto Self-Refresh (ASR): Disabled <sup>d)</sup> ; Self-Refresh Temperature Range (SRT): Normal <sup>e)</sup> ; CKE: Low; External clock: Off; CK and $\overline{CK}$ : LOW; CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ , Command, Address, Bank Address Inputs, Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: MID_LEVEL
	Self-Refresh Current: Extended Temperature Range (optional) <sup>f)</sup>
/ <sub>DD6ET</sub>	<b>7</b> <sub>CASE</sub> : 0 - 95 °C; Auto Self-Refresh (ASR): Disabled <sup>d)</sup> ; Self-Refresh Temperature Range (SRT): Extended <sup>e)</sup> ; CKE: Low; External clock: Off; CK and $\overline{CK}$ : LOW; CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ , Command, Address, Bank Address Inputs, Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: MID_LEVEL

Symbol	Description
	Auto Self-Refresh Current (optional) <sup>f)</sup>
	T <sub>CASE</sub> : 0 - 95 °C; Auto Self-Refresh (ASR): Enabled <sup>d)</sup> ; Self-Refresh Temperature Range (SRT): Normal <sup>e)</sup> ;
/ <sub>DD6TC</sub>	CKE: Low; External clock: Off; CK and CK: LOW; CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; CS, Command, Address,
	Bank Address Inputs, Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: Auto Self-Refresh operation;
	Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: MID_LEVEL
	Operating Bank Interleave Read Current
	CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, NRRD, nFAW, CL: see Table 1; BL: 8 <sup>a), f)</sup> ; AL: CL-
	1; CS: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling accord-
I <sub>DD7</sub>	ing to Table 10; Data IO: read data burst with different data between one burst and the next one
	according to Table 10; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0,
	1,7) with different addressing, wee Table 10; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ;
	ODT Signal: stable at 0; Pattern Details: see Table 10.

- a) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B
- b) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT\_Nom enable: set MR1 A[9,6,2] = 011B; RTT\_Wr enable: set MR2 A[10,9] = 10B
- c) Precharge Power Down Mode: set MRO A12=0B for Slow Exit or MRO A12 = 1B for Fast Exit
- d) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature
- e) Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for normal or 1B for extended temperature range
- f) Read Burst Type: Nibble Sequential, set MRO A[3] = OB



Table 3 - IDD0 Measurement-Loop Pattern<sup>a)</sup>

CK, CK	CKE	Sub-Loop	Cycle Number	Command	<u>SS</u>	RAS	CAS	WE	ОБТ	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>b)</sup>
		0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	D, D	1	1	1	1	0	0	00	0	0	0	0	-
				repeat	patte	n 1	4 unti	InRAS	S - 1, 1	trunca	te if n	ecess	ary			
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
				repeat	patte	rn 1	4 unti	I nRC	- 1, tr	uncate	e if ne	cessa	ry			
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1, 2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
пg	High		1*nRC+3, 4	D, D	1	1	1	1	0	0	00	0	0	F	0	-
toggling	tic F			repeat	patte	rn 1	4 unti	l 1*nF	RC + r	RAS -	1, tru	ıncate	if nec	essary	'	
ţ.	Static		1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
				repeat	patte	rn 1	4 unti	l 2*nF	RC - 1,	trunc	ate if	neces	sary			
		1	2*nRC	repeat	Sub-L	.oop 0	), use	BA[2:	0] = 1	inste	ad					
		2	4*nRC	repeat	Sub-L	.oop 0	), use	BA[2:	0] = 2	inste	ad					
		3	6*nRC	repeat	Sub-L	.oop 0	), use	BA[2:	0] = 3	inste	ad					
		4	8*nRC	repeat	Sub-L	.oop 0	), use	BA[2:	0] = 4	inste	ad					
		5	10*nRC	repeat	Sub-L	.oop 0	), use	BA[2:	0] = 5	inste	ad					
		6	12*nRC	repeat	Sub-L	.oop 0	), use	BA[2:	0] = 6	inste	ad					
		7	14*nRC	repeat	Sub-L	.oop 0	), use	BA[2:	0] = 7	' inste	ad					

a) DM must be driven LOW all the time. DQS,  $\overline{\mbox{DQS}}$  are MID-LEVEL.

b) DQ signals are MID-LEVEL.



Table 4 - IDD1 Measurement-Loop Patterna)

CK, CK	CKE	Sub-Loop	Cycle	Command	SS	RAS	CAS	WE	ООТ	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>b)</sup>
		0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	D, D	1	1	1	1	0	0	00	0	0	0	0	-
				repeat	patte	rn 1	4 unti	l nRCI	O - 1, 1	trunca	ite if n	ecess	ary			
			nRCD	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
				repeat	patte	rn 1	4 unti	l nRAS	S - 1, t	runca	te if n	ecessa	ary			
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
				repeat	patte	rn 1	4 unti	l nRC	- 1, tr	uncate	e if ne	cessar	У			
	Static High		1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1,2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
ng			1*nRC+3,4	D, D	1	1	1	1	0	0	00	0	0	F	0	-
toggling	tic F			repeat	patte	rn nR(	C + 1,	4 ur	ntil nR	C + n	RCE -	1, trui	ncate	if nece	ssary	
to	Sta		1*nRC+nRCD	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
				repeat	patte	rn nR(	C + 1,	4 ur	ntil nR	C + n	RAS -	1, trui	ncate	if nece	ssary	
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
				repeat	patte	rn nR(	C + 1,	4 ur	ntil *2	nRC -	1, tru	ncate	if nec	essary	1	
		1	2*nRC	repeat	Sub-L	.oop 0	), use	BA[2:	0] = 1	inste	ad					
		2	4*nRC	repeat	Sub-L	.oop 0	), use	BA[2:	0] = 2	inste	ad					
		3	6*nRC	repeat	Sub-L	.oop 0	), use	BA[2:	0] = 3	inste	ad					
		4	8*nRC	repeat	Sub-L	.oop 0	), use	BA[2:	0] = 4	inste	ad					
		5	10*nRC	repeat	Sub-L	oop C	), use	BA[2:	0] = 5	inste	ad					
		6	12*nRC	repeat	Sub-L	oop C	), use	BA[2:	0] = 6	inste	ad					
		7	14*nRC	repeat	Sub-L	.oop 0	), use	BA[2:	0] = 7	inste	ad					

a) DM must be driven LOW all the time. DQS,  $\overline{\text{DQS}}$  are used according to RD Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID\_LEVEL.



Table 5 - IDD2N and IDD3N Measurement-Loop Patterna)

CK, CK	CKE	Sub-Loop	Cycle Number	Command	SS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>b)</sup>
		0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	
			2	D	1	1	1	1	0	0	0	0	0	F	0	-
			3	D	1	1	1	1	0	0	0	0	0	F	0	-
bu	High	1	4-7	repeat	Sub-L	.oop 0	, use	BA[2:0	)] = 1	instea	d					
toggling		2	8-11	repeat	Sub-L	.oop 0	, use	BA[2:0	)] = 2	instea	d					
t	Static	3	12-15	repeat	Sub-L	oop 0	, use	BA[2:0	0] = 3	instea	d					
		4	16-19	repeat	Sub-L	.oop 0	, use	BA[2:0	)] = 4	instea	d					
		5	20-23	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	24-17	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	28-31	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS,  $\overline{DQS}$  are MID-LEVEL.

Table 6 - IDD2NT and IDDQ2NT Measurement-Loop Patterna)

CK, CK	CKE	Sub-Loop	Cycle Number	Command	<u> S</u>	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>b)</sup>
		0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	D	1	1	1	1	0	0	0	0	0	F	0	-
			3	D	1	1	1	1	0	0	0	0	0	F	0	-
Вu	High	1	4-7	repeat	Sub-L	.oop C	, but	ODT =	= 0 and	d BA[2	2:0] =	1				
toggling		2	8-11	repeat	Sub-L	.oop C	, but (	ODT =	= 1 and	d BA[2	2:0] =	2				
\$	Static	3	12-15	repeat	Sub-L	oop C	, but (	ODT =	= 1 and	d BA[2	2:0] =	3				
		4	16-19	repeat	Sub-L	.oop C	, but	ODT =	= 0 and	d BA[2	2:0] =	4				
		5	20-23	repeat	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5											
		6	24-17	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6												
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS,  $\overline{\text{DQS}}$  are MID-LEVEL.

b) DQ signals are MID-LEVEL.

b) DQ signals are MID-LEVEL.



Table 7 - IDD4R and IDDQ4R Measurement-Loop Patterna)

CK, CK	CKE	Sub-Loop	Cycle Number	Command	SS	RAS	CAS	WE	TGO	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>b)</sup>
		0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2,3	D,D	1	1	1	1	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	00	0	0	F	0	-
bu	High		6,7	D,D	1	1	1	1	0	0	00	0	0	F	0	-
toggling		1	8-15	repeat	Sub-L	.oop 0	, but	BA[2:0	)] = 1							
t	Static	2	16-23	repeat	Sub-L	.oop 0	, but	BA[2:0	)] = 2							
		3	24-31	repeat	Sub-L	.oop 0	, but	BA[2:0	0] = 3							
		4	32-39	repeat	Sub-L	oop 0	, but	BA[2:0	0] = 4							
	5 40-47 repeat Sub-Loop 0, but BA[2:0] = 5															
		6	48-55	repeat	Sub-L	oop 0	, but	BA[2:0	0] = 6							
		7	56-63	repeat	Sub-L	oop 0	, but	BA[2:0	0] = 7							

a) DM must be driven LOW all the time. DQS,  $\overline{\text{DQS}}$  are used according to RD Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.



Table 8 - IDD4W Measurement-Loop Patterna)

CK, CK	CKE	Sub-Loop	Cycle	Command	<u>S3</u>	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>b)</sup>
		0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	00	0	0	0	0	-
			2,3	D,D	1	1	1	1	1	0	00	0	0	0	0	-
			4	WR	0	1	0	0	1	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	00	0	0	F	0	-
ng	High		6,7	D,D	1	1	1	1	1	0	00	0	0	F	0	-
toggling		1	8-15	repeat	Sub-L	.oop 0	, but	BA[2:0	)] = 1							
\$	Static	2	16-23	repeat	Sub-L	.oop 0	, but	BA[2:0	)] = 2							
		3	24-31	repeat	Sub-L	.oop 0	, but	BA[2:0	0] = 3							
		4	32-39	repeat	Sub-L	.oop 0	, but	BA[2:0	)] = 4							
		5	40-47	repeat	Sub-L	.oop 0	, but	BA[2:0	)] = 5							
		6	48-55	repeat	Sub-L	.oop 0	, but	BA[2:0	)] = 6							
		7	56-63	repeat	Sub-L	.oop 0	, but	BA[2:0	)] = 7							

a) DM must be driven LOW all the time. DQS, DQS are used according to WR Commands, otherwise MID-LEVEL.

Table 9 - IDD5B Measurement-Loop Patterna)

CK, CK	CKE	Sub-Loop	Cycle	Command	<u>S3</u>	RAS	CAS	WE	DDT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>b)</sup>
		0	0	REF	0	0	0	1	0	0	0	0	0	0	0	-
		1	1.2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	D, D	1	1	1	1	0	0	00	0	0	F	0	-
			58	repeat	cycles	3 14	, but I	3A[2:0	)] = 1							
Вu	High		912	repeat	cycles	3 14	, but I	3A[2:0	)] = 2							
toggling			1316	repeat	cycles	3 14	, but I	3A[2:0	)] = 3							
\$	Static		1720	repeat	cycles	3 14	, but I	3A[2:0	)] = 4							
			2124	repeat	cycles	3 14	, but I	3A[2:0	)] = 5							
			2528	repeat	cycles	3 14	, but I	3A[2:0	0] = 6							
			2932	repeat	cycles	3 14	, but I	3A[2:0	)] = 7							
		2	33nRFC-1	repeat	Sub-L	.oop 1	, until	nRFC	- 1. T	runca	te, if n	ecessa	ary.			

a) DM must be driven LOW all the time. DQS, DQS are MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are MID-LEVEL.

b) DQ signals are MID-LEVEL.



### Table 10 - IDD7 Measurement-Loop Patterna)

ATTENTION! Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, CK	CKE	Sub-Loop	Cycle Number	Command	<u>cs</u>	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>b)</sup>
		0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	00	0	0	0	0	-
				repeat	above	D C	omma	nd ur	ntil nR	RD - 1		-				-
			nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	-
		1	nRRD+1	RDA	0	1	0	1	0	1	00	1	0	F	0	00110011
		1	nRRD+2	D	1	0	0	0	0	1	00	0	0	F	0	-
				repeat	above	e D C	omma	nd ur	itil 2*	nRRD	- 1		I	I		'
		2	2*nRRD	repeat	Sub-l	oop (	), but	BA[2	:0] =	2						
		3	3*nRRD	repeat	Sub-l	oop ´	1, but	BA[2	:0] =	3						
		4	4*nRRD	D	1	0	0	0	0	3	00	0	0	F	0	-
		4		Assert	and r	epeat	abov	e D C	omma	nd un	til nF	٠ W	1, if n	ecessa	ary	
		5	nFAW	repeat	Sub-l	oop (	), but	BA[2	:0] =	4						
		6	nFAW+nRRD	repeat	Sub-l	oop ´	1, but	BA[2	:0] =	5						
		7	nFAW+2*nRRD	repeat	Sub-l	oop (	), but	BA[2	:0] =	6						
		8	nFAW+3*nRRD	repeat	Sub-l	oop ´	1, but	BA[2	:0] =	7					0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
	ηί	9	nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	F	0	-
toggling	Static High	7		Assert	and r	epeat	abov	e D C	omma	nd un	til 2*	nFAW	<i>l</i> - 1,	if nece	essary	
ogo	atic		2*nFAW+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
-	St	10	2*nFAW+1	RDA	0	1	0	1	0	0	00	1	0	F	0	00110011
		10	2&nFAW+2	D	1	0	0	0	0	0	00	0	0	F	0	-
			ZXIII AVV + Z	Repeat	abov	e D C	omm	and u	ntil 2*	nFAV	V + n	RRD -	1			
			2*nFAW+nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	-
		11	2*nFAW+nRRD+1	RDA	0	1	0	1	0	1	00	1	0	0	0	00000000
			2&nFAW+nRRD+	D	1	0	0	0	0	1	00	0	0	0	0	-
			2	Repeat							V + 2	* nRR	D - 1			
		12	2*nFAW+2*nRRD	repeat		•		-	-							
		13	2*nFAW+3*nRRD	repeat	Sub-l	oop ´	11, bu	it BA[:	2:0] =	: 3						
		14	2*nFAW+4*nRRD	D	1	0	0	0	0	3	00	0	0	0 if pos	-	-
		15	2*~ [ 0.10/			•					1111 3	HEAV	/ - 1,	ппес	essaiy	
		15	3*nFAW	repeat repeat												
		16	3*nFAW+nRRD	_												
		17	3*nFAW+2*nRRD	repeat												
		18 19	3*nFAW+3*nRRD 3*nFAW+4*nRRD	repeat D	1	0	0	0	0	7	00	0	0	0		-
		.,		Assert	and r	epeat	abov	e D C	omma	nd un	ıtil 4*	nFAW	<i>I</i> - 1,	if nece	essary	

a) DM must be driven LOW all the time. DQS,  $\overline{DQS}$  are used according to RD Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.



#### **IDD Specifications**

IDD values are for full operating range of voltage and temperature unless otherwise noted.

#### **IDD** Specification

Speed Grade Bin	DDR3 - 1066 7-7-7	DDR3 - 1333 9-9-9	DDR3 - 1600 11-11-11	DDR3 - 1866 13-13-13	DDR3 - 2133 14-14-14	Unit	Notes
Symbol	Max.	Max.	Max.	Max.	Max.		
,	45	50	55	61	TBD	mA	х8
/ <sub>DD0</sub>	60	65	65	68	85	mA	x16
,	55	60	65	70	TBD	mA	х8
/ <sub>DD01</sub>	70	75	75	80	85	mA	x16
/ <sub>DD2P0</sub>	12	12	12	12	12	mA	X8/X16
/ <sub>DD2P1</sub>	15	15	15	15	17	mA	X8/X16
/ <sub>DD2N</sub>	25	30	30	32	35	mA	X8/X16
,	35	40	40	46	TBD	mA	х8
/ <sub>DD2NT</sub>	35	40	45	45	52	mA	x16
/ <sub>DD2Q</sub>	25	30	32	34	38	mA	X8/X16
/ <sub>DD3P</sub>	22	22	25	25	30	mA	X8/X16
/ <sub>DD3N</sub>	30	35	40	50	58	mA	X8/X16
,	80	95	105	120	TBD	mA	x4/x8
/ <sub>DD4R</sub>	105	130	140	180	210	mA	x16
,	85	98	110	124	TBD	mA	х8
/ <sub>DD4w</sub>	105	130	150	190	220	mA	x16
,	165	165	170	179	TBD	mA	х8
/ <sub>DD5B</sub>	165	170	170	175	180	mA	x16
/ <sub>DD6</sub>	12	12	12	12	12	mA	X8/X16,1
/ <sub>DD6ET</sub>	15	15	15	15	15	mA	X8/X16,2
/ <sub>DD6TC</sub>	15	15	15	15	15	mA	X8/X16,3
/ <sub>DD6 Low power</sub>	6.5	6.5	6.5	6.5	6.5	mA	X8/X16,1
	110	135	145	160	TBD	mA	x8
/ <sub>DD7</sub>	160	190	210	240	285	mA	x16

#### Notes:

- 1. Applicable for MR2 settings A6=0 and A7=0. Temperature range for IDD6 is 0 85°C.
- 2. Applicable for MR2 settings A6=0 and A7=1. Temperature range for IDD6ET is  $0 95^{\circ}C$ .
- 3. Applicable for MR2 settings A6=1 and A7=0. IDD6TC is measured at 95°C



## Input/Output Capacitance

Parameter	Symbol	DDR3	8-800	DDR3	-1066	DDR3	-1333	DDR3	-1600	DDR3	-1866	DDR3	-2133	Units	Notes
Farameter	Symbol	Min	Max	Ullits	Motes										
Input/output capacitance (DQ, DM, DQS, DQS, TDQS, TDQS)	C <sub>IO</sub>	1.5	3.0	1.5	2.7	1.5	2.5	1.5	2.3	1.4	2.2	1.4	2.1	pF	1,2,3
Input capacitance, CK and CK	C <sub>CK</sub>	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	0.8	1.3	0.8	1.3	pF	2,3
Input ca <u>pa</u> citance delta CK and CK	C <sub>DCK</sub>	0	0.15	0	0.15	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,4
Input cap <u>acita</u> nce delta, DQS and DQS	C <sub>DDQS</sub>	0	0.20	0	0.20	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,5
Input capacitance (All other input-only pins)	C <sub>I</sub>	0.75	1.4	0.75	1.35	0.75	1.3	0.75	1.3	0.75	1.2	0.75	1.2	pF	2,3,6
Input capacitance delta (All CTRL input-only pins)	C <sub>DI_CTR</sub> L	-0.5	0.3	-0.5	0.3	-0.4	0.2	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2,3,7,8
Input capacitance delta (All ADD/CMD input-only pins)	C <sub>DI_ADD</sub> _CMD	-0.5	0.5	-0.5	0.5	-0.4	0.4	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2,3,9,10
Input/output capacitance delta (DQ, DM, DQS, DQS)	C <sub>DIO</sub>	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,11
Input/output capacitance of ZQ pin	C <sub>ZQ</sub>	-	3	-	3	-	3	-	3	-	3	-	3	pF	2,3,12



Parameter	Svmbol	DDR3	8-800	DDR3	-1066	DDR3	-1333	DDR3	-1600	DDR3	-1866	DDR3			Notes
Faranietei	Зуппоот	Min	Max	Min	Max	Offics	NOTES								

#### Notes:

- 1. Although the DM, TDQS and  $\overline{\text{TDQS}}$  pins have different functions, the loading matches DQ and DQS.
- 2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with VDD, VDDQ, VSS,VSSQ applied and all other pins floating (except the pin under test, CKE, RESET and ODT as necessary). VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.
- 3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
- 4. Absolute value of  $C_{CK}$ - $C_{\overline{CK}}$ .
- 5. Absolute value of  $C_{IO}(DQS)-C_{IO}(\overline{DQS})$ .
- 6. C<sub>I</sub> applies to ODT,  $\overline{\text{CS}}$ , CKE, A0-A15, BA0-BA2,  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ .
- 7.  $C_{DL\ CTR}$  applies to ODT,  $\overline{CS}$  and CKE.
- 8.  $C_{DI CTRL} = C_I(CNTL) 0.5 * C_I(CLK) + C_I(\overline{CLK})$
- 9. C<sub>DL ADD CMD</sub> applies to A0-A15, BA0-BA2, RAS, CAS and WE.
- 10.  $C_{DI ADD CMD} = C_I(ADD\_CMD) 0.5*(C_I(CLK) + C_I(\overline{CLK}))$
- 11.  $C_{DIO} = C_{IO}(DQ) 0.5*(C_{IO}(DQS) + C_{IO}(\overline{DQS}))$
- 12. Maximum external load capacitance an ZQ pin: 5 pF.

### **Standard Speed Bins**

DDR3L SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

#### **DDR3-800 Speed Bins**

For specific Notes See "Speed Bin Table Notes" on page 32.

Speed Bin		DDF	23-800E		
CL - nRCD - nRP		6	-6-6	Unit	Notes
Parameter	Symbol	min	max		
Internal read command to first data	t <sub>AA</sub>	15	20	ns	
ACT to internal read or write delay time	t <sub>RCD</sub>	15	_	ns	
PRE command period	t <sub>RP</sub>	15	_	ns	
ACT to ACT or REF command period	t <sub>RC</sub>	52.5	_	ns	



#### For specific Notes See "Speed Bin Table Notes" on page 32.

ACT to P	RE command period	t <sub>RAS</sub>	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	t <sub>CK(AVG)</sub>	3.0	3.3	ns	1, 2, 3, 4, 12
CL = 6	CWL = 5	t <sub>CK(AVG)</sub>	2.5	3.3	ns	1, 2, 3
	Supported CL Settings			5, 6	$n_{\rm CK}$	12
5	Supported CWL Settings			5	$n_{\rm CK}$	

### **DDR3-1066 Speed Bins**

For specific Notes See "Speed Bin Table Notes" on page 32.

	Speed Bin		DDR3-	1066F		
C	L - nRCD - nR	Р	7-7	7-7	Unit	Note
Par	ameter	Symbol	min	max		
	ad command to st data	$t_{AA}$	13.125	20	ns	
	iternal read or delay time	$t_{RCD}$	13.125	_	ns	
PRE com	nmand period	$t_{RP}$	13.125	_	ns	
	ACT or REF and period	$t_{\rm RC}$	50.625	_	ns	
ACT to PRE command period		t <sub>RAS</sub>	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{\rm CK(AVG)}$	3.0	3.3	ns	1, 2, 3, 4, 6, 12
CL = 3	CWL = 6	t <sub>CK(AVG)</sub>	Rese	erved	ns	4

CL = 6	CWL = 5	t <sub>CK(AVG)</sub>	2.5	3.3	ns	1, 2, 3, 6
OL - O	CWL = 6	t <sub>CK(AVG)</sub>	Rese	erved	ns	1, 2, 3, 4
CL = 7	CWL = 5	t <sub>CK(AVG)</sub>	Rese	erved	ns	4
OL - /	CWL = 6	t <sub>CK(AVG)</sub>	1.875	< 2.5	ns	1, 2, 3, 4
CL = 8	CWL = 5	t <sub>CK(AVG)</sub>	Rese	erved	ns	4
OL - O	CWL = 6	t <sub>CK(AVG)</sub>	1.875	< 2.5	ns	1, 2, 3
Sup	ported CL Setti	ings	5, 6	, 7, 8	n <sub>CK</sub>	12
Sup	ported CWL Set	tings	5,	6	n <sub>CK</sub>	

### **DDR3-1333 Speed Bins**

For specific Notes See "Speed Bin Table Notes" on page 32.

	Speed Bin		D	DR3-1333H	11	NI-4-
С	L - nRCD - nl	RP		9-9-9	Unit	Note
Par	ameter	Symbol	min	max		
	rnal read d to first data	t <sub>AA</sub>	13.5 (13.125) <sup>8</sup>	20	ns	
	ternal read or delay time	$t_{RCD}$	13.5 (13.125) <sup>8</sup>	_	ns	
PRE com	nmand period	$t_{RP}$	13.5 (13.125) <sup>8</sup>	_	ns	
	ACT or REF and period	$t_{\rm RC}$	49.5 (49.125) <sup>8</sup>	_	ns	
	RE command period	t <sub>RAS</sub>	36	9 * tREFI	ns	
CL = 5	CWL = 5	t <sub>CK(AVG)</sub>	3.0	3.3	ns	1, 2, 3, 4, 7, 12
	CWL = 6, 7	t <sub>CK(AVG)</sub>		Reserved	ns	4

	CWL = 5	t <sub>CK(AVG)</sub>	2.5	3.3	ns	1, 2, 3, 7
CL = 6	CWL = 6	t <sub>CK(AVG)</sub>		Reserved	ns	1, 2, 3, 4, 7
	CWL = 7	t <sub>CK(AVG)</sub>		Reserved	ns	4
	CWL = 5	t <sub>CK(AVG)</sub>		Reserved	ns	4
CL = 7	CWL = 6	tourne	1.875	< 2.5	ns	1, 2, 3, 4, 7
CL = 7	CVVL - 0	t <sub>CK(AVG)</sub>		(Optional) <sup>5</sup>	113	1, 2, 3, 4, 7
	CWL = 7	t <sub>CK(AVG)</sub>		Reserved	ns	1, 2, 3, 4
	CWL = 5	t <sub>CK(AVG)</sub>		Reserved	ns	4
CL = 8	CWL = 6	t <sub>CK(AVG)</sub>	1.875	< 2.5	ns	1, 2, 3, 7
	CWL = 7	t <sub>CK(AVG)</sub>		Reserved	ns	1, 2, 3, 4
CL = 9	CWL = 5, 6	t <sub>CK(AVG)</sub>		Reserved	ns	4
CL - 7	CWL = 7	t <sub>CK(AVG)</sub>	1.5	<1.875	ns	1, 2, 3, 4
	CWL = 5, 6	t <sub>CK(AVG)</sub>		Reserved	ns	4
CL = 10	CWL = 7	t <sub>CK(AVG)</sub>	1.5	<1.875	ns	1, 2, 3
	OVVL - 7	*CK(AVG)		(Optional)	ns	5
Sup	ported CL Set	tings	5, 6	6, 8, (7), 9, (10)	n <sub>CK</sub>	
Supp	orted CWL Se	ttings		5, 6, 7	n <sub>CK</sub>	

### **DDR3-1600 Speed Bins**

For specific Notes See "Speed Bin Table Notes" on page 32.

	Speed Bin		D	DR3-1600K		
С	L - nRCD - nl	RP		11-11-11	Unit	Note
Par	ameter	Symbol	min	max		
	rnal read d to first data	t <sub>AA</sub>	13.75 (13.125) <sup>5</sup>	20	ns	
	ternal read or delay time	$t_{RCD}$	13.75 (13.125) <sup>5</sup>	_	ns	
PRE com	mand period	t <sub>RP</sub>	13.75 (13.125) <sup>5</sup>	_	ns	
	ACT or REF and period	$t_{\rm RC}$	48.75 (48.125) <sup>5</sup>	_	ns	
	RE command eriod	t <sub>RAS</sub>	35	9 * tREFI	ns	
CL = 5	CWL = 5	t <sub>CK(AVG)</sub>	3.0	3.3	ns	1, 2, 3, 4, 8, 12
CL = 5	CWL = 6, 7	t <sub>CK(AVG)</sub>		Reserved	ns	4

					•	
CL = 6	CWL = 5	t <sub>CK(AVG)</sub>	2.5	3.3	ns	1, 2, 3, 8
	CWL = 6	t <sub>CK(AVG)</sub>	Reserved		ns	1, 2, 3, 4, 8
	CWL = 7	t <sub>CK(AVG)</sub>	Reserved		ns	4
	CWL = 5	t <sub>CK(AVG)</sub>	Reserved		ns	4
	CWL = 6	<i>t</i>	1.875	< 2.5	ns	1, 2, 3, 4, 8
CL = 7		t <sub>CK(AVG)</sub>	(Optional) <sup>5</sup>		113	1, 2, 3, 4, 6
	CWL = 7	t <sub>CK(AVG)</sub>	Reserved		ns	1, 2, 3, 4, 8
	CWL = 8	t <sub>CK(AVG)</sub>	Reserved		ns	4
	CWL = 5	t <sub>CK(AVG)</sub>	Reserved		ns	4
CL = 8	CWL = 6	t <sub>CK(AVG)</sub>	1.875	< 2.5	ns	1, 2, 3, 8
CL = 0	CWL = 7	t <sub>CK(AVG)</sub>	Reserved		ns	1, 2, 3, 4, 8
	CWL = 8	t <sub>CK(AVG)</sub>	Reserved		ns	1, 2, 3, 4
	CWL = 5, 6	t <sub>CK(AVG)</sub>	Reserved		ns	4
CL = 9	CWL = 7	t <sub>CK(AVG)</sub>	1.5	<1.875	nc	1 2 2 4 9
CL = 9			(Optional) <sup>5</sup>		ns	1, 2, 3, 4, 8
	CWL = 8	t <sub>CK(AVG)</sub>	Reserved		ns	1, 2, 3, 4
	CWL = 5, 6	t <sub>CK(AVG)</sub>	Reserved		ns	4
CL = 10	CWL = 7	t <sub>CK(AVG)</sub>	1.5	<1.875	ns	1, 2, 3, 8
	CWL = 8	t <sub>CK(AVG)</sub>	Reserved		ns	1, 2, 3, 4
CL = 11	CWL = 5, 6,7	t <sub>CK(AVG)</sub>	Reserved		ns	4
CL = 11	CWL = 8	t <sub>CK(AVG)</sub>	1.25	<1.5	ns	1, 2, 3
Sup	Supported CL Settings		5, 6, (7), 8, (9), 10, 11		$n_{\rm CK}$	
Supported CWL Settings			5, 6, 7, 8		$n_{\rm CK}$	
					•	

### DDR3-1866 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 32.

Speed Bin		D	Unit	Note		
C	CL - nRCD - nRP				11000	
Pa	rameter	Symbol	min	max		
	read command first data	$t_{AA}$	13.91	20	ns	
	nternal read or delay time	$t_{\rm RCD}$	13.91	_	ns	
PRE cor	mmand period	$t_{RP}$	13.91	_	ns	
	PRE command period	$t_{RAS}$	34	9 * tREFI	ns	
ACT to ACT or PRE command period		$t_{\rm RC}$	47.91	-	ns	
CL = 5	CWL = 5	t <sub>CK(AVG)</sub>	Reserved		ns	1, 2, 3, 4, 9
CL = 3	CWL = 6,7,8,9	t <sub>CK(AVG)</sub>	Reserved		ns	4

				<del>                                     </del>	I	
CL = 6	CWL = 5	<i>t</i> <sub>CK(AVG)</sub>	2.5	3.3	ns	1, 2, 3, 9
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 9
	CWL = 7.8.9	t <sub>CK(AVG)</sub>	Reserved		ns	4
	CWL = 5	t <sub>CK(AVG)</sub>	Reserved		ns	4
CL = 7	CWL = 6	t <sub>CK(AVG)</sub>	Reserved		ns	1, 2, 3, 4, 9
	CWL = 7.8.9	t <sub>CK(AVG)</sub>	Reserved		ns	4
	CWL = 5	$t_{\rm CK(AVG)}$	Reserved		ns	4
CL = 8	CWL = 6	$t_{\rm CK(AVG)}$	1.875	< 2.5	ns	1, 2, 3, 9
CL = 0	CWL = 7	$t_{\rm CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 9
	CWL = 8,9	t <sub>CK(AVG)</sub>		Reserved	ns	4
	CWL = 5, 6	t <sub>CK(AVG)</sub>	Reserved		ns	4
CL = 9	CWL = 7	t <sub>CK(AVG)</sub>	Reserved		ns	1, 2, 3, 4, 9
CL = 9	CWL = 8	$t_{\rm CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 9
	CWL = 9	$t_{\rm CK(AVG)}$	Reserved		ns	4
	CWL = 5, 6	t <sub>CK(AVG)</sub>	Reserved		ns	4
CL = 10	CWL = 7	t <sub>CK(AVG)</sub>	1.5	<1.875	ns	1, 2, 3, 9
	CWL = 8	t <sub>CK(AVG)</sub>	Reserved		ns	1, 2, 3, 4, 9
	CWL = 5,6,7	t <sub>CK(AVG)</sub>	Reserved		ns	4
CL = 11	CWL = 8	t <sub>CK(AVG)</sub>	Reserved		ns	1, 2, 3, 4, 9
	CWL = 9	t <sub>CK(AVG)</sub>	Reserved		ns	1, 2, 3, 4
CL = 12	CWL = 5,6,7,8	t <sub>CK(AVG)</sub>	Reserved		ns	4
CL = 12	CWL = 9	t <sub>CK(AVG)</sub>	Reserved		ns	1,2,3,4
Cl 12	CWL = 5,6,7,8	t <sub>CK(AVG)</sub>	Reserved		ns	4
CL = 13	CWL = 9	t <sub>CK(AVG)</sub>	1.07	<1.25	ns	1, 2, 3
Supported CL Settings			6, 8, 10, 12, 13		$n_{\rm CK}$	
Supported CWL Settings			5, 6, 7, 8, 9		$n_{\rm CK}$	

### **DDR3-2133 Speed Bins**

For specific Notes See "Speed Bin Table Notes" on page 32.

Speed Bin			D	Unit		
CL - nRCD - nRP			14-14-14			Note
P	Parameter	Symbol	min	max		
Internal read command to first data		t <sub>AA</sub>	13.09	20.0	ns	
ACT to internal read or write delay time		$t_{\rm RCD}$	13.09	_	ns	
PRE command period		$t_{RP}$	13.09	_	ns	
ACT to PRE command period		$t_{RAS}$	33.0	9 * tREFI	ns	
ACT to ACT or PRE command period		$t_{\rm RC}$	46.09	-	ns	
CL = 5	CWL = 5	t <sub>CK(AVG)</sub>	Reserved		ns	1, 2, 3, 4, 10
CL - 3	CWL = 6,7,8,9,10	t <sub>CK(AVG)</sub>	Reserved		ns	4
	CWL = 5	t <sub>CK(AVG)</sub>	2.5	3.3	ns	1, 2, 3, 10
CL = 6	CWL = 6	t <sub>CK(AVG)</sub>	Reserved		ns	1, 2, 3, 4, 10
	CWL = 7.8,910	t <sub>CK(AVG)</sub>		Reserved	ns	4

	CWL = 5	t <sub>CK(AVG)</sub>		Reserved	ns	4
CL = 7	CWL = 6	t <sub>CK(AVG)</sub>	1.875	< 2.5	ns	1, 2, 3, 10
	CWL = 7	t <sub>CK(AVG)</sub>		Reserved	ns	1, 2, 3, 4, 10
	CWL = 8,9,10	t <sub>CK(AVG)</sub>		Reserved	ns	4
	CWL = 5	t <sub>CK(AVG)</sub>		Reserved	ns	4
CL = 8	CWL = 6	t <sub>CK(AVG)</sub>	1.875	< 2.5	ns	1, 2, 3, 10
CL - 0	CWL = 7	t <sub>CK(AVG)</sub>		Reserved	ns	1, 2, 3, 4, 10
	CWL = 8,9,10	t <sub>CK(AVG)</sub>		Reserved	ns	4
	CWL = 5, 6	t <sub>CK(AVG)</sub>		Reserved	ns	4
CL = 9	CWL = 7	t <sub>CK(AVG)</sub>	1.5	<1.875	ns	1, 2, 3, 10
CL = 7	CWL = 8	t <sub>CK(AVG)</sub>	Reserved		ns	1, 2, 3, 4, 10
	CWL = 9,10	t <sub>CK(AVG)</sub>		Reserved	ns	4
	CWL = 5, 6	t <sub>CK(AVG)</sub>		Reserved	ns	4
	CWL = 7	t <sub>CK(AVG)</sub>	1.5	<1.875	ns	1, 2, 3, 9
CL = 10	CWL = 8	t <sub>CK(AVG)</sub>		Reserved	ns	1, 2, 3, 4, 9
	CWL = 9	t <sub>CK(AVG)</sub>		Reserved	ns	4
	CWL = 10	t <sub>CK(AVG)</sub>		Reserved	ns	4
	CWL = 5,6,7	t <sub>CK(AVG)</sub>		Reserved	ns	4
CL = 11	CWL = 8	t <sub>CK(AVG)</sub>	1.25	<1.5	ns	1, 2, 3, 10
	CWL = 9	t <sub>CK(AVG)</sub>	Reserved		ns	1, 2, 3, 4, 10
	CWL = 10	t <sub>CK(AVG)</sub>	Reserved		ns	1, 2, 3, 4
CL = 12	CWL = 5,6,7,8	t <sub>CK(AVG)</sub>	Reserved		ns	4
	CWL = 9	t <sub>CK(AVG)</sub>	Reserved		ns	1,2,3,4, 10
	CWL = 10	$t_{\rm CK(AVG)}$		Reserved	ns	4
	CWL = 5,6,7,8	t <sub>CK(AVG)</sub>		Reserved	ns	4
CL = 13	CWL = 9	t <sub>CK(AVG)</sub>	1.07	<1.25	ns	1, 2, 3, 10
	CWL = 10	t <sub>CK(AVG)</sub>	Reserved			1, 2, 3, 4
CL = 14	CWL = 5,6,7,8,9	t <sub>CK(AVG)</sub>	Reserved		ns	4
	CWL = 10	t <sub>CK(AVG)</sub>	0.935	<1.07	ns	1, 2, 3
Supported CL Settings			5, 6, 7, 8, 9, 10, 11, 12, 13, 14		$n_{\rm CK}$	
St	ıpported CWL Settir	ngs	5, 6, 7, 8, 9, 10		$n_{\rm CK}$	

#### **Speed Bin Table Notes**

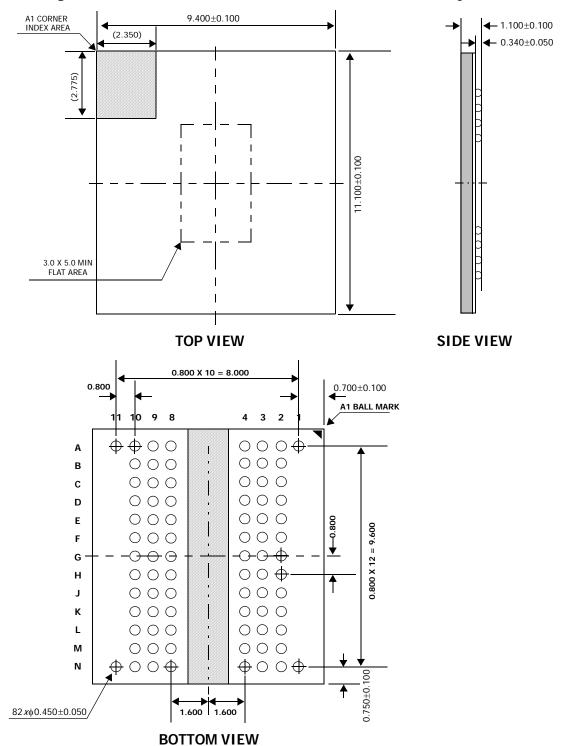
Absolute Specification ( $T_{OPER}$ ;  $V_{DDQ} = V_{DD} = 1.5V +/- 0.075 V$ );

- 1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
- 2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog data and strobe output are synchronized by the DLL all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (3.0, 2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 5 calculation.
- 3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
- 4. 'Reserved' settings are not allowed. User must program a different value.
- 5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a man-

- datory feature. Refer to Hynix DIMM data sheet and/or the DIMM SPD information if and how this setting is supported.
- 6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- 7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- 8. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- 9. Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- 10. Any DDR3-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- 11. Hynix DDR3 SDRAM devices supporting optional down binning to CL=7 and CL=9, and tAA/tRCD/tRP must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1333H devices supporting down binning to DDR3-1066F should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600K devices supporting down binning to DDR3-1333H or DDR3-1600F should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accordingly. For example, 49.125ns (tRASmin + tRPmin = 36 ns + 13.125 ns) for DDR3-1600K.
- 12. For CL5 support, refer to DIMM SPD information. DRAM is required to support CL5. CL5 is not mandatory in SPD coding.

### **Package Dimensions**

### Package Dimension(x8): 82Ball Fine Pitch Ball Grid Array Outline



### Package Dimension(x16): 96Ball Fine Pitch Ball Grid Array Outline

