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RT307x_RT357x EEPROM Format V1.62

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Update history

Version	Date	Description	Modified by
0.1	2008/4/11	1. Initial version	Gary
1.0	2008/6/9	1. Delete 5G portion. 2. Add “Antenna Diversity” function in 0x37h. 3. Take off “Double Delete Line” on V0.1.	Vincent
1.1	2008/7/15	1. Add 3071, 3072 portion 2. Change file name	Vincent
1.2	2008/8/25	1. Add CountryRegion code #31 for 2.4G	Rory
1.3	2008/11/26	1. Modify the description of register @ 4Eh~4Fh. Change register “Maximum TX Power for 2.4GHz band” to “EIRP TX Power for 2.4GHz band”	Vincent
1.4	2008/12/5	1. Add TX mixer gain setting for 2.4GHz band (48h)	Gary
1.5	2008/11/26	1. Add register definition for RT357X 2. Add 5G portion. 3. Add CountryRegion code #14 for 5G	Vincent
1.6	2008/12/23	1. Add TX mixer gain setting for RT3572 (48h/4Ch)	Gary
1.61	2009/02/16	1. Add CountryRegion code #15 (38h) for 5GHz 2. Add channel 169, 173 in CountryRegion code #7 (38h)	Rory
1.62	2009/04/20	1. Add CountryRegion code #16 (38h) for 5GHz 2. Remove channel 169, 173 in CountryRegion code #7 (38h)	Rex

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Contents

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1. General Description

The EEPROM layout is split into two parts. The first one (up to 0x200) is common for all interfaces; the second part (after 0x200) is only valid to USB.
The following table summarizes EEPROM used in RT3070 configuration.

	EEPROM Type	EEPROM size (in byte)
USB	AT25080 Compatible (SPI)	1024 (0x400)

2. RT307x_357x EEPROM Layout

Offset	Default (hex)	b15 ~b8	b7 ~ b0
00h	307x 2070 357x	Chip ID	
02h	0000	EEPROM Version	
04h		Mac Address [15:0]	
06h		Mac Address [31:16]	
08h		Mac Address [47:32]	
0Ah	FFFF	Reserved	
0Ch	FFFF	Reserved	
0Eh	FFFF	Reserved	
10h	FFFF	Reserved	
12h	FFFF	Reserved	
14h	FFFF	Reserved	
16h	FFFF	Reserved	Reserved
18h	FFFF	Reserved	
1Ah	FFFF	Reserved	
1Ch	FFFF	Reserved	
...	FFFF	ASIC Reserved	
24h	FFFF	Reserved	Reserved
26h	FFFF	Reserved	Reserved
28h	FFFF	Reserved	Reserved
2Ah	FFFF	Reserved	Reserved
2Ch	FFFF	Reserved	Reserved
2Eh	FFFF	Reserved	Reserved
30h	FFFF	Reserved	Reserved
32h	FFFF	Reserved	Reserved
34h	FFFF	NIC Configuration 0	
36h	FFFF	NIC Configuration 1	
38h	FFFF	Country Region 2.4G band	Country Region 5G band

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Offset	Default (hex)	b15 ~b8	b7 ~ b0
3Ah	FFFF	LED Mode	Frequency offset
3Ch	FFFF	LED A/G Configuration	
3Eh	FFFF	LED ACT Configuration	
40h	FFFF	LED A/G/ACT Polarity	
42h	FFFF	NIC Configuration 2	
44h	FFFF	External LNA gain for 5G Band (CH36~CH64)	External LNA gain for 2.4G Band
46h	0000	2.4G RSSI1 offset	2.4G RSSI0 offset
48h	0000	External LNA gain for 5G Band (CH100~CH128)	TX mixer gain setting for 2.4Ghz Band
4Ah	0000	5G RSSI1 offset	5G RSSI0 offset
4Ch	0000	External LNA gain for 5G Band (CH132~CH165)	TX mixer gain setting for 5Ghz Band
4Eh	FFFF	EIRP TX Power for for 5GHz band	EIRP TX Power for for 2.4GHz band
50h	FFFF	20M/40M BW Power delta for 5G band	20M/40M BW Power delta for 2.4G band
52h	FFFF	Channel 2 TX0 power	Channel 1 TX0 power
54h	FFFF	Channel 4 TX0 power	Channel 3 TX0 power
56h	FFFF	Channel 6 TX0 power	Channel 5 TX0 power
58h	FFFF	Channel 8 TX0 power	Channel 7 TX0 power
5Ah	FFFF	Channel 10 TX0 power	Channel 9 TX0 power
5Ch	FFFF	Channel 12 TX0 power	Channel 11 TX0 power
5Eh	FFFF	Channel 14 TX0 power	Channel 13 TX0 power
60h	FFFF	Channel 2 TX1power	Channel 1 TX1 power
62h	FFFF	Channel 4 TX1 power	Channel 3 TX1 power
64h	FFFF	Channel 6 TX1 power	Channel 5 TX1 power
66h	FFFF	Channel 8 TX1 power	Channel 7 TX1 power
68h	FFFF	Channel 10 TX1 power	Channel 9 TX1 power
6Ah	FFFF	Channel 12 TX1 power	Channel 11 TX1 power
6Ch	FFFF	Channel 14 TX1 power	Channel 13 TX1 power
6Eh	FFFF	2.4G TX power –3 TSSI boundary	2.4G TX power –4 TSSI boundary
70h	FFFF	2.4G TX power –1 TSSI boundary	2.4G TX power –2 TSSI boundary
72h	FFFF	2.4G TX power +1 TSSI boundary	2.4G TX power ±0 TSSI boundary
74h	FFFF	2.4G TX power +3 TSSI boundary	2.4G TX power +2 TSSI boundary
76h	FFFF	2.4G TX ALC step value	2.4G TX power +4 TSSI boundary
78h	FFFF	**Channel 38 TX0 power**	Channel 36 TX0 power
7Ah	FFFF	Channel 44 TX0 power	Channel 40 TX0 power
7Ch	FFFF	Channel 48 TX0 power	**Channel 46 TX0 power**
7Eh	FFFF	**Channel 54 TX0 power**	Channel 52 TX0 power

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Offset	Default (hex)	b15 ~b8	b7 ~ b0
80h	FFFF	Channel 60 TX0 power	Channel 56 TX0 power
82h	FFFF	Channel 64 TX0 power	**Channel 62 TX0 power**
84h	FFFF	Channel 102 TX0 power	Channel 100 TX0 power
86h	FFFF	Channel 108 TX0 power	Channel 104 TX0 power
88h	FFFF	Channel 112 TX0 power	**Channel 110 TX0 power**
8Ah	FFFF	**Channel 118 TX0 power**	Channel 116 TX0 power
8Ch	FFFF	Channel 124 TX0 power	Channel 120 TX0 power
8Eh	FFFF	Channel 128 TX0 power	**Channel 126 TX0 power**
90h	FFFF	**Channel 134 TX0 power**	Channel 132 TX0 power
92h	FFFF	Channel 140 TX0 power	Channel 136 TX0 power
94h	FFFF	**Channel 151 TX0 power**	Channel 149 TX0 power
96h	FFFF	Channel 157 TX0 power	Channel 153 TX0 power
98h	FFFF	Channel 161 TX0 power	**Channel 159 TX0 power**
9Ah	FFFF	Reserved	Channel 165 TX0 power
9Ch	FFFF	Reserved	Reserved
9Eh	FFFF	Reserved	Reserved
A0h	FFFF	Reserved	Reserved
A2h	FFFF	Reserved	Reserved
A4h	FFFF	Reserved	Reserved
A6h	FFFF	**Channel 38 TX1 power**	Channel 36 TX1 power
A8h	FFFF	Channel 44 TX1 power	Channel 40 TX1 power
AAh	FFFF	Channel 48 TX1 power	**Channel 46 TX1 power**
ACh	FFFF	**Channel 54 TX1 power**	Channel 52 TX1 power
AEh	FFFF	Channel 60 TX1 power	Channel 56 TX1 power
B0h	FFFF	Channel 64 TX1 power	**Channel 62 TX1 power**
B2h	FFFF	**Channel 102 TX1 power**	Channel 100 TX1 power
B4h	FFFF	Channel 108 TX1 power	Channel 104 TX1 power
B6h	FFFF	Channel 112 TX1 power	**Channel 110 TX1 power**
B8h	FFFF	**Channel 118 TX1 power**	Channel 116 TX1 power
BAh	FFFF	Channel 124 TX1 power	Channel 120 TX1 power
BCh	FFFF	Channel 128 TX1 power	**Channel 126 TX1 power**
BEh	FFFF	**Channel 134 TX1 power**	Channel 132 TX1 power
C0h	FFFF	Channel 140 TX1 power	Channel 136 TX1 power
C2h	FFFF	**Channel 151 TX1 power**	Channel 149 TX1 power
C4h	FFFF	Channel 157 TX1 power	Channel 153 TX1 power
C6h	FFFF	Channel 161 TX1 power	**Channel 159 TX1 power**

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Offset	Default (hex)	b15 ~b8	b7 ~ b0
C8h	FFFF	Reserved	Channel 165 TX1 power
CAh	FFFF	Reserved	Reserved
CCh	FFFF	Reserved	Reserved
CEh	FFFF	Reserved	Reserved
D0h	FFFF	Reserved	Reserved
D2h	FFFF	Reserved	Reserved
D4h	FFFF	5G TX power –3 TSSI boundary	5G TX power –4 TSSI boundary
D6h	FFFF	5G TX power –1 TSSI boundary	5G TX power –2 TSSI boundary
D8h	FFFF	5G TX power +1 TSSI boundary	5G TX power ±0 TSSI boundary
DAh	FFFF	5G TX power +3 TSSI boundary	5G TX power +2 TSSI boundary
DCh	FFFF	5G TX ALC step value	5G TX power +4 TSSI boundary
DEh	6666	TX power for CCK 5.5M/11M	TX power for CCK 1M/2M
E0h	6666	TX power for OFDM 12M/18M	TX power for OFDM 6M/9M
E2h	6666	TX power for OFDM 48M/54M	TX power for OFDM 24M/36M
E4h	6666	TX power for HT MCS=2,3	TX power for HT MCS=0,1
E6h	6666	TX power for HT MCS=6,7	TX power for HT MCS=4,5
E8h	6666	TX power for HT MCS10,11	TX power for HT MCS8,9
EAh	6666	TX power for HT MCS14,15	TX power for HT MCS12,13
ECh	6666	TX power for STBC MCS2,3	TX power for STBC MCS0,1
EEh	6666	TX power for STBC MCS6,7	TX power for STBC MCS4,5
F0h	FFFF	Reserved	Reserved
F2h	FFFF	Reserved	Reserved
F4h	FFFF	Reserved	Reserved
F6h	FFFF	Reserved	Reserved
F8h	FFFF	Reserved	Reserved
FAh	FFFF	Reserved	Reserved
FCh	FFFF	Reserved	Reserved
FEh	FFFF	Reserved	Reserved

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USB Specific Contents

Offset	Content	Value
High Speed Wireless Descriptor		
200h	Device Descriptor	12 01 00 02 00 00 00 40 VV VV[1] PP PP[1] RR RR[1] 01 02 03[2] 01
212h	Device Qualifier	0A 06 00 02 00 00 00 40 01 00
21Ch	Configuration Descriptor	09 02 43 00 01 01 04[2] 80 PP[3]
225h	Interface Descriptor	09 04 00 00 07 FF FF FF 05[2]
22Eh	EP 1 IN Descriptor	07 05 81 02 00 02 00
235h	EP 1 OUT Descriptor	07 05 01 02 00 02 00
23Ch	EP 2 OUT Descriptor	07 05 02 02 00 02 00
243h	EP 3 OUT Descriptor	07 05 03 02 00 02 00
24Ah	EP 4 OUT Descriptor	07 05 04 02 00 02 00
251h	EP 5 OUT Descriptor	07 05 05 02 00 02 00
258h	EP 6 OUT Descriptor	07 05 06 02 00 02 00
High Speed CD-ROM Identification(Auto-run)		
260h	Vendor Name	52 61 6C 69 6E 6B 20 20 *(Ralink)*
268h	Product Name	57 69 72 65 6c 65 73 73 20 31 31 6E 20 20 20 20 *(Wireless 11n)*
278h	Version Number	31 2E 30 30 *(1.00)*
High Speed CD-ROM Descriptor(Auto-run)		
280h	Device Descriptor	12 01 00 02 00 00 00 40 VV VV[1] PP PP[1] RR RR[1] 06 07 08[2] 01
292h	Device Qualifier	0A 06 00 02 00 00 00 40 01 00
29Ch	Configuration Descriptor	09 02 20 00 01 01 09[2] 80 PP[3]
2A5h	Interface Descriptor	09 04 00 00 02 08 06 50 0A[2]
2AEh	EP 1 IN Descriptor	07 05 81 02 00 02 00
2B5h	EP 1 OUT Descriptor	07 05 01 02 00 02 00
Other Device Configuration		
2E0h	Device Configuration	(See following description)
2E1h	(For F/W internal use)	00
2E2h	NOR Flash Size	(Flash size in 64KB)-1
String Descriptor Address		
2F0h	String Desc. Start Addr[4]	00 S1 S2 S3 S4 S5 S6 S7 S8 S9 SA SB SC SD SE SF
String Descriptor		
300h	String Descriptor 0	04 03 09 04
…		

[1] Vendor ID, product ID and revision ID respectively
[2] String descriptor index. 00 if not available.
[3] Maximum power consumption. The unit is 2mA.
[4] Corresponding string descriptor starts at 0x300+Sn

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2.1 E2PROM layout version # (02h)

Value	Description
0	Version 0.
1 ~ 255	Invalid version. Treat as version 0.

2.2 ASIC reserved (1Eh ~ 23h)

Field	Description
15:0	Reserved.

2.3 NIC Configuration 0 (0x34)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				RFIC Type				TX Path setting				RX Path setting			
Reserved				1: RT2820 (2.4G 2T3R) 2: RT2850 (2.4G/5G 2T3R) 3: RT2720 (2.4G 1T2R) 4: RT2750 (2.4G/5G 1T2R) 5: RT3020 (2.4G, 1T1R, inside RT3070) 6: RT2020 (2.4G, 1T1R, inside RT2070) 7: RT3021 (2.4G 1T2R,inside RT3071) 8: RT3022 (2.4G 2T2R, inside RT3072) 9: RT3052 (2.4G/5G 2T2R, inside RT3572)				1: 1TX 2: 2TX				1: 1RX 2: 2RX			

NIC Configuration 0 Register Bit Fields Description

Offset	Field	Description
34h	3:0	RX front-end architecture in the system. 0 (0000): Reserved. 1 (0001): 1 RX front-end in the system. 2 (0010): 2 RX front-end in the system. 3 ~ F (0011 ~ 1111): Reserved.
	7:4	TX front-end architecture in the system. 0 (0000): Reserved. 1 (0001): 1 TX front-end in the system. 2 (0010): 2 TX front-end in the system. 3~ F (0011 ~ 1111): Reserved.

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Offset	Field	Description
35h	11:8	RF transceiver IC type. 0 (0000): Reserved 1 (0001): RF IC type is RT2820 (2.4GHz, 2T3R) (Reserved) 2 (0010): RF IC type is RT2850 (2.4/5GHZ, 2T3R) (Reserved) 3 (0011): RF IC type is RT2720 (2.4GHz, 1T2R). (Reserved) 4 (0100): RF IC type is RT2750 (2.4/5GHz, 1T2R) (Reserved) 5 (0101): RF IC type is RT3020 (2.4GHz, 1T1R, inside RT3070) 6 (0110): RF IC type is RT2020 (2.4GHz, 1T1R, inside RT2070) 7 (0111): RF IC type is RT3021 (2.4GHz, 1T2R) 8 (1000): RF IC type is RT3022 (2.4GHz, 2T2R) 9 (1001): RF IC type is RT3522(2.4GHz/5G, 2T2R) A~F(1010~1111): Reserved
	15:12	Reserved.

2.4 NIC Configuration 1 (0x36)

Bit[7:0]=0xFF will be treated as INVALID and used Default Value.
Bit[15:8]=0xFF will be treated as INVALID and used Default Value

7	6	5	4	3	2	1	0
WPS PBC	5G side band for 40M BW	2.4G side band for 40M BW	Proprietary Test bit	EXT LNA 5G	EXT LNA 2.4G	TX ALC	HW CTRL
0: off (D) 1: on	0: off(D) 1: on	0: off 1: on(D)	0: off(D) 1: on	0: off 1: on	0: off 1: on	0: off(D) 1: on	0: off(D) 1: on

15	14 ~ 12	11	10	9	8
DAC test bit	Reserved	Antenna Diversity	Broadband EXT LNA	40M BW in 5G band	40M BW in 2.4G band
0: off (D) 1: on		0: off (D) 1: on	0: off 1: on	0: on (D) 1: off	0: on (D) 1: off

NIC Configuration 1 Register Bit Fields Description

Offset	Field	Description
36h	0	Hardware Radio Control. 0: disable hardware radio control (default value). 1: enable hardware radio control. When “hardware radio control” bit is enabled (=1), the driver will read MAC’s GPIO[2] status. When GPIO[2] pin is low, the radio is disabled. When GPIO[2] pin is high, the radio is enabled. The Radio ON/OFF is controlled by both software UI and MAC’s GPIO[2] pin.
	1	TX Auto Level Control. 0: disable TX ALC function (default value). 1: enable TX ALC function. When the TX ALC function is enabled (=1), the driver will automatic compensate TX power varied due to temperature variation. It also needs to fill the register “Tx ALC step value for 2.4GHz (77h)” for the TX ALC function.

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Offset	Field	Description
	2	External 2.4GHz band LNA. 0: Board without external LNA for 2.4GHz band must set this bit to 0. 1: Board with external LNA for 2.4GHz band must set this bit to 1 (default value).
	3	External 5GHz band LNA. 0: Board without external LNA for 5GHz band must set this bit to 0. 1: Board with external LNA for 5GHz band must set this bit to 1.
	4	Proprietary TEST BIT. For debug purpose. Default value is 0.
	5	2.4GHz side band for 40MHz BW. For debug purpose.
	6	5G side band for 40M BW For debug purpose.
	7	WPS Push Button Configuration control. 0: disable WPS PBC control (default value). 1: enable WPS PBC control. The WPS PBC function is controlled through GPIO[3]. If LED mode set to “Signal strength”(64), WPS PBC will be disabled.
37h	8	40M BW in 2.4GHz band. 0: enable 40MHz bandwidth for 2.4GHz band 1: disable 40MHz bandwidth for 2.4GHz band
	9	40M BW in 5G band 0: enable 40MHz bandwidth for 5GHz band. 1: disable 40MHz bandwidth for 5GHz band.
	10	Broadband EXT LNA 0: Board without external LNA must set this bit to 0. 1: Board with external LNA must set this bit to 1.
	11	Antenna Diversity control. 0: disable diversity function (default value). 1: enable diversity function.
	14:12	Reserved
	15	DAC test bit 0: Disable DAC test. 1: Enable DAC test.

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2.5 NIC Configuration 2 (0x42)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TX Stream				RX Stream			
								1: 1 Stream 2: 2 Stream				1: 1 Stream 2: 2 Stream			

Note:

1. The 1 stream support MCS0~MCS7. The 2 stream support MCS0~MCS15.
2. Stream setting should be equal or less than path setting of EEPROM (0x34)
3. Default=0xFF means that based on the path setting (0x34) for MAX capability.

NIC Configuration 2 Register Bit Fields Description

Offset	Field	Description
42h	3:0	RX stream. 0 (0000): Reserved 1 (0001): 1 RX stream 2 (0010): 2 RX stream 3 ~ F (0011 ~ 1111): Reserved.
	7:4	TX stream. 0 (0000): Reserved 1 (0001): 1 TX stream 2 (0010): 2 TX stream 3 ~ F (0011 ~ 1111): Reserved.
43h	15:8	Reserved.

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2.6 Country Region Code for 5G band (0x38)

Default value = FFh, which means read from INF and registry, more flexible than reading from EEPROM, this is our current InstallShield CCS implementation. We do not recommend customers to read SKU from EEPROM. therefore, FFh is our default value.
CountryCode— Specify the domain code, can be FFh or one of the followings,

Index	Support Channels
0	36, 40, 44, 48, 52, 56, 60, 64, 149, 153, 157, 161, 165
1	36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140
2	36, 40, 44, 48, 52, 56, 60, 64
3	52, 56, 60, 64, 149, 153, 157, 161
4	149, 153, 157, 161, 165
5	149, 153, 157, 161
6	36, 40, 44, 48
7	36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165
8	52, 56, 60, 64
9	36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 132, 136, 140, 149, 153, 157, 161, 165
10	36, 40, 44, 48,149, 153, 157, 161, 165
11	36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 149, 153, 157, 161
12	36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140
13	52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161
14	36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 136, 140, 149, 153, 157, 161, 165
15	149, 153, 157, 161, 165, 169, 173
16	36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165, 169, 173

Note: 1.) If set to Index #12, it will also turn on 802.11h and Carrier Detection by default

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2.7 Country Region Code for 2.4G band (0x39)

Default value = FFh, which means read from INF and registry, more flexible than reading from EEPROM, this is our current InstallShield CCS implementation. We do not recommend customers to read SKU from EEPROM. Value FFh is the default value.
CountryCode— Specify the domain code, can be FFh or one of the followings,

Index	Support Channels
0	CH 1 ~ 11
1	CH 1 ~ 13
2	CH 10 ~ 11
3	CH 10 ~ 13
4	CH 14
5	CH 1 ~ 14
6	CH 3 ~ 9
7	CH 5 ~ 13
31	CH1 ~ 14 (CH1 ~ 11 active scan, CH12 ~ 14 passive scan)

Notes: If set to read SKU from EEPROM, only available if 2.4G Country Region code registers are programmed.

2.8 Frequency offset (0x3A)

Used for crystal calibration.

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2.9 LED Mode Setting (0x3B)

7	6	5	4	3	2	1	0
GPIO Polarity	LED control mode						

Offset	Field	LED Mode		Description
3Bh	[6:0]	0	HW control	The default mode. Driver sets MAC register and MAC controls LED.
		1	FW default mode	The firmware controls how LED blinks.
		2	8sec scan	Same as LED mode 1 except that fast blink for 8sec when doing scanning.
		3-63	-	Reserved.
		64	Signal strength setting	Besides mode 1, additionally set LED signal strength. LedParam1[0] = GPIO polarity (0 is negative) LedParam0 = Signal strength (Valid value are 0, 1, 3, 7, 15, 31. Where value 0 is the weakest signal strength.)
	7	GPIO Polarity		0: Negative polarity 1: Positive polarity

GPIO 0-4 will be used as signal strength indicator only in **Mode 64**.

signal strength	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Very Strong	on	on	on	on	on
Good	off	on	on	on	on
Average	off	off	on	on	on
Weak	off	off	off	on	on
Very Weak	off	off	off	off	on
not linked	off	off	off	off	off

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2.10 LED A/G Configuration (3Ch~3Dh)

7	6	5	4	3	2	1	0
LED A		LED G		Reserved		LED G	
Radio on and link down				Radio off			

15	14	13	12	11	10	9	8
LED A		LED G		LED A		LED G	
Radio on and link to A				Radio on and link to G			

Offset	States	Field	RDY A/G	LED_RDYG behavior
3Ch	Radio off	[1:0]	LED G	00: Reserved 01: Solid on 10: Slow blink 11: Fast blink
		[3:2]	LED A	
	Radio on and link down	[5:4]	LED G	00: Reserved 01: Solid on 10: Slow blink 11: Fast blink
		[7:6]	LED A	
3Dh	Radio on and link to G	[9:8]	LED G	00: Reserved 01: Solid on 10: Slow blink 11: Fast blink
		[11:10]	LED A	
	Radio on and link to A	[13:12]	LED G	00: Reserved 01: Solid on 10: Slow blink 11: Fast blink
		[15:14]	LED A	

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2.11 ACT Configuration (3Eh~3Fh)

7	6	5	4	3	2	1	0
Radio on and link down				Radio off			

15	14	13	12	11	10	9	8
Radio on and link to A				Radio on and link to G			

Offset	States	Field	LED_ACT behavior
3Eh	Radio off	[1:0]	00: Reserved 01: Solid on 10: Blink when transmitting data and management packet 11: Blink when transmitting data, management packet and beacon
		2	0: Solid on when no traffic 1: Slow blink when no traffic
		3	Reserved
	Radio on but link down	[5:4]	00: Reserved 01: Solid on 10: Blink when transmitting data and management packet 11: Blink when transmitting data, management packet and beacon
		6	0: Solid on when no traffic 1: Slow blink when no traffic
		7	Reserved
3Fh	Radio on and link to G	[9:8]	00: Reserved 01: Solid on 10: Blink when transmitting data and management packet 11: Blink when transmitting data, management packet and beacon
		10	0: Solid on when no traffic 1: Slow blink when no traffic
		11	Reserved
	Radio on and link to A	[13:12]	00: Reserved 01: Solid on 10: Blink when transmitting data and management packet 11: Blink when transmitting data, management packet and beacon
		14	0: Solid on when no traffic 1: Slow blink when no traffic
		15	Reserved

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2.12 LED A/G/ACT Polarity (40h~41h)

7	6	5	4	3	2	1	0
Reserved	LED ACT	LED A	LED G	Reserved	LED ACT	LED A	LED G
Radio on and link down				Radio off			

15	14	13	12	11	10	9	8
Reserved	LED ACT	LED A	LED G	Reserved	LED ACT	LED A	LED G
Radio on and link to A				Radio on and link to G			

Offset	States	Field	LED behavior	
40h	Radio off	0	LED G	1: Positive polarity 0: Negative polarity
		1	LED A	
		2	LED ACT	
		3	Reserved	Reserved and must be filled as 1.
	Radio on but link down	4	LED G	1: Positive polarity 0: Negative polarity
		5	LED A	
		6	LED ACT	
		7	Reserved	Reserved and must be filled as 1.
41h	Radio on and link to G	8	LED G	1: Positive polarity 0: Negative polarity
		9	Reserved	
		10	LED ACT	
		11	Reserved	Reserved and must be filled as 1.
	Radio on and link to A	12	LED G	1: Positive polarity 0: Negative polarity
		13	LED A	
		14	LED ACT	
		15	Reserved	Reserved and must be filled as 1.

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2.13 External LNA gain for 2.4GHz Band (44h)

External LNA gain for 2.4GHz Band Register Bit Fields Description

Offset	Field	Description
44h	7:0	External LNA gain for 2.4G Band. 1 step = 1 dB Example: Value: 0000 0000 → LNA gain (dB): 0 Value: 0000 0001 → LNA gain (dB): 1 Value: 0000 1010 → LNA gain (dB): 10

2.14 TX mixer gain setting for 2.4GHz band (48h)

TX mixer gain setting for 2.4GHz band Register Bit Fields Description (For RT307x only)

Offset	Field	Description
48h	7:0	This register is for RT307x TX mixer gain setting. 2 (010)= +0dB (Default), 0x00 and 0xFF are invalid that will apply to default setting. 3 (011)= +1dB 4 (100)= +2.5dB

TX mixer gain setting for 2.4GHz band Register Bit Fields Description (For RT3572 only)

Offset	Field	Description
48h	7:0	This register is for RT3572 2.4GHz TX mixer gain setting. 1 (001)= +1.5dB 2 (010)= +3dB 4 (100)= +4dB (Default)

2.15 TX mixer gain setting for 5GHz band (4Ch)

TX mixer gain setting for 5GHz band Register Bit Fields Description (For RT3572 only)

Offset	Field	Description
4Ch	7:0	This register is for RT3572 5GHz TX mixer gain setting. 1 (001)= +1dB 2 (010)= +4dB (Default) 4 (100)= +7dB

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2.16 External LNA gain for 5GHz Band (45h, 49h, 4Dh)

External LNA gain for 5GHz Band Register Bit Fields Description

<table>
<tr><th>Offset</th><th>Field</th><th>Description</th></tr>
<tr><td>45h,</td><td>7:0</td><td>External LNA gain for 5GHz Band for channel 36 to 64.
1 step = 1dB.
Example:
<table>
<tr><td>Value</td><td>LNA gain (dB)</td></tr>
<tr><td>0000 0000</td><td>0</td></tr>
<tr><td>0000 0001</td><td>1</td></tr>
<tr><td>0000 1010</td><td>10</td></tr>
</table></td></tr>
<tr><td>49h</td><td>7:0</td><td>External LNA gain for 5GHz Band for channel 100 to 128.
1 step = 1dB.
Example:
<table>
<tr><td>Value</td><td>LNA gain (dB)</td></tr>
<tr><td>0000 0000</td><td>0</td></tr>
<tr><td>0000 0001</td><td>1</td></tr>
<tr><td>0000 1010</td><td>10</td></tr>
</table></td></tr>
<tr><td>4Dh</td><td>7:0</td><td>External LNA gain for 5GHz Band for channel 132 to 165.
1 step = 1dB.
Example:
<table>
<tr><td>Value</td><td>LNA gain (dB)</td></tr>
<tr><td>0000 0000</td><td>0</td></tr>
<tr><td>0000 0001</td><td>1</td></tr>
<tr><td>0000 1010</td><td>10</td></tr>
</table></td></tr>
</table>

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2.17 EIRP TX Power for 2.4GHz & 5GHz band (4E~4Fh)

The register is intended to limit the TX power for different countries in one SKU.

EIRP TX Power for 2.4GHz & 5GHz band Register Bit Fields Description

Offset	Field	Description
4Eh	7:0	2.4GHz maximum TX power. The register value is the board's EIRP value. The driver will compare the board's EIRP with each country allow TX power automatically if this function is enabled. FF (1111 1111): disable the maximum TX power comparison function. Example: 08 (0000 1000): TX power limit is 8dBm 10 (0001 0000): TX power limit is 16dBm 12 (0001 0010): TX power limit is 18dBm
4Fh	15:8	5GHz maximum TX power. The register value is the board's EIRP value. The driver will compare the board's EIRP with each country allow TX power automatically if this function is enabled. FF (1111 1111): disable the maximum TX power comparison function. Example: 08 (0000 1000): TX power limit is 8dBm 10 (0001 0000): TX power limit is 16dBm 12 (0001 0010): TX power limit is 18dBm

Example:

If antenna gain is 3dBi, board's maximum TX power is 17dBm. The Equivalent isotropically radiated power (EIRP) is 17+3=20dBm. The value of offset 4Eh is 14 (0001 0100).

Following table is based on the maximum TX power comparison function is enabled.

Country	Allowed TX power of the country (dBm)	Offset 4Eh = 14	Exact maximum EIRP (dBm)
A	20	20	20
B	16	20	16
C	18	20	18
D	23	20	20

Note:

If allowed country power is greater than the TX power setting of offset 4Eh, then the board maximum EIRP is the TX power setting of offset 4Eh.

If allowed country power is less than the TX power setting of offset 4Eh, then the board maximum EIRP is the country's allowed TX power.

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2.18 20M/40M BW Power Delta for 2.4GHz band (50h)

Driver compensates the TX power value of 40M BW with this configured value.

2.4GHz TX power delta configuration Register Bit Fields Description

Offset	Field	Description
50h	5:0	40M BW TX power delta value (MAX=4). 000001: 1dBm 000010: 2dBm 000011: 3dBm 000100: 4dBm
	6	1: increase 40M BW TX power with the delta value. 0: decrease 40M BW TX power with the delta value.
	7	1: enable TX power compensation.

Example:
Originally, 40M BW TX power= 14dBm and 20M BW TX power = 14dBm when TX power delta configuration is not enabled.
If want keep 20M BW TX power in 14dBm and reduce 40M BW TX power to 10dBm (delta=4dBm), set 50h = 84h (1000 0100), set 51h = 84h (1000 0100).

2.19 20M/40M BW Power Delta for 5GHz band (51h)

5GHz TX power delta configuration Register Bit Fields Description

Offset	Field	Description
51h	5:0	40M BW TX power delta value (MAX=4). 000001: 1dBm 000010: 2dBm 000011: 3dBm 000100: 4dBm
	6	1: increase 40M BW TX power with the delta value. 0: decrease 40M BW TX power with the delta value.
	7	1: enable TX power compensation.

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2.20 2.4G band TX0 & TX1 Power (52h~6Dh)

To prevent reading from EMPTY E2PROM, driver treats these “Channel xx Tx Power” value 0 and any value > =0x20 as invalid. That is, only bit [0..4] in each byte contains valid data, [bit 5..7] MUST be 0.

2.4GHz TX0 & TX1 power setting register

Offset	b15 ~b8	b7 ~ b0
52h	Channel 2 TX0 power	Channel 1 TX0 power
54h	Channel 4 TX0 power	Channel 3 TX0 power
56h	Channel 6 TX0 power	Channel 5 TX0 power
58h	Channel 8 TX0 power	Channel 7 TX0 power
5Ah	Channel 10 TX0 power	Channel 9 TX0 power
5Ch	Channel 12 TX0 power	Channel 11 TX0 power
5Eh	Channel 14 TX0 power	Channel 13 TX0 power
60h	Channel 2 TX1power	Channel 1 TX1 power
62h	Channel 4 TX1 power	Channel 3 TX1 power
64h	Channel 6 TX1 power	Channel 5 TX1 power
66h	Channel 8 TX1 power	Channel 7 TX1 power
68h	Channel 10 TX1 power	Channel 9 TX1 power
6Ah	Channel 12 TX1 power	Channel 11 TX1 power
6Ch	Channel 14 TX1 power	Channel 13 TX1 power

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2.21 5G band TX0 & TX1 Power (78h~9Ah, A6h~C8h)

To prevent reading from EMPTY E2PROM, driver treats these “Channel xx Tx Power” value 0 and any value > =0x20 as invalid. That is, only bit[0..4] in each byte contains valid data, bit [5..7] MUST be 0.

5GHz TX0 power setting register

Offset	b15 ~b8	b7 ~ b0
78h	**Channel 38 TX0 power**	Channel 36 TX0 power
7Ah	Channel 44 TX0 power	Channel 40 TX0 power
7Ch	Channel 48 TX0 power	**Channel 46 TX0 power**
7Eh	**Channel 54 TX0 power**	Channel 52 TX0 power
80h	Channel 60 TX0 power	Channel 56 TX0 power
82h	Channel 64 TX0 power	**Channel 62 TX0 power**
84h	**Channel 102 TX0 power**	Channel 100 TX0 power
86h	Channel 108 TX0 power	Channel 104 TX0 power
88h	Channel 112 TX0 power	**Channel 110 TX0 power**
8Ah	**Channel 118 TX0 power**	Channel 116 TX0 power
8Ch	Channel 124 TX0 power	Channel 120 TX0 power
8Eh	Channel 128 TX0 power	**Channel 126 TX0 power**
90h	**Channel 134 TX0 power**	Channel 132 TX0 power
92h	Channel 140 TX0 power	Channel 136 TX0 power
94h	**Channel 151 TX0 power**	Channel 149 TX0 power
96h	Channel 157 TX0 power	Channel 153 TX0 power
98h	Channel 161 TX0 power	**Channel 159 TX0 power**
9Ah	Reserved	Channel 165 TX0 power

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5GHz TX1 power setting register

Offset	b15 ~b8	b7 ~ b0
A6h	**Channel 38 TX1 power**	Channel 36 TX1 power
A8h	Channel 44 TX1 power	Channel 40 TX1 power
AAh	Channel 48 TX1 power	**Channel 46 TX1 power**
ACh	**Channel 54 TX1 power**	Channel 52 TX1 power
AEh	Channel 60 TX1 power	Channel 56 TX1 power
B0h	Channel 64 TX1 power	**Channel 62 TX1 power**
B2h	**Channel 102 TX1 power**	Channel 100 TX1 power
B4h	Channel 108 TX1 power	Channel 104 TX1 power
B6h	Channel 112 TX1 power	**Channel 110 TX1 power**
B8h	**Channel 118 TX1 power**	Channel 116 TX1 power
BAh	Channel 124 TX1 power	Channel 120 TX1 power
BCh	Channel 128 TX1 power	**Channel 126 TX1 power**
BEh	**Channel 134 TX1 power**	Channel 132 TX1 power
C0h	Channel 140 TX1 power	Channel 136 TX1 power
C2h	**Channel 151 TX1 power**	Channel 149 TX1 power
C4h	Channel 157 TX1 power	Channel 153 TX1 power
C6h	Channel 161 TX1 power	**Channel 159 TX1 power**
C8h	Reserved	Channel 165 TX1 power

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2.22 Tx Power delta TSSI Boundary of 2.4GHz & 5GHz (6Eh ~ 76h, D4h ~ DCh)

Driver compares current TSSI value (from BBP R49) with this TSSI reference value as a base to decide if real-time TX power compensation is required. 0xFF will be treated as invalid value. This function is controlled by 'TXALC' bit in NIC configuration1 bit1.

2.4GHz Tx Power delta TSSI Boundary

Offset	b7 ~ b0
6Eh	2.4G TX power –4 TSSI boundary
6Fh	2.4G TX power –3 TSSI boundary
70h	2.4G TX power –2 TSSI boundary
71h	2.4G TX power –1 TSSI boundary
72h	2.4G TX power ±0 TSSI boundary
73h	2.4G TX power +1 TSSI boundary
74h	2.4G TX power +2 TSSI boundary
75h	2.4G TX power +3 TSSI boundary
76h	2.4G TX power +4 TSSI boundary

5GHz Tx Power delta TSSI Boundary

Offset	b7 ~ b0
D4h	2.4G TX power –4 TSSI boundary
D5h	2.4G TX power –3 TSSI boundary
D6h	2.4G TX power –2 TSSI boundary
D7h	2.4G TX power –1 TSSI boundary
D8h	2.4G TX power ±0 TSSI boundary
D9h	2.4G TX power +1 TSSI boundary
DAh	2.4G TX power +2 TSSI boundary
DBh	2.4G TX power +3 TSSI boundary
DCh	2.4G TX power +4 TSSI boundary

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2.23 Tx ALC step value for 2.4GHz & 5G band (77h, DDh)

Delta value for Tx Power step up/down(1 step=0.5dBm) auto-calibration.
Driver reads this value as delta value when doing real-time TX calibration. 0xFF will be treated as invalid value. This function controlled by 'TXALC' bit in NIC configuration1 bit1.

<table>
<tr><th>Offset</th><th>Field</th><th>Description</th></tr>
<tr><td>77h,DD</td><td>7:0</td><td>TX ALC step value for 2.4G & 5G Band.
1 step = 0.5 dBm
Example:
<table>
<tr><td>Value</td><td>LNA gain (dBm)</td></tr>
<tr><td>0000 0000</td><td>0</td></tr>
<tr><td>0000 0001</td><td>0.5</td></tr>
<tr><td>0000 1010</td><td>5</td></tr>
</table></td></tr>
</table>

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2.24 TX rate power configuration (DEh~EFh)

Default value=0x66, low byte for TX power0 setting, High byte for TX power1 (1 step=1dBm)

The 1 step=1dBm.

Offset	Default Value	Description	Bit [7:4]	Bit [3:0]
DEh	66	TX power for CCK 1M/2M	TX1 power setting	TX0 power setting
DFh	66	TX power for CCK 5.5M/11M	TX1 power setting	TX0 power setting
E0h	66	TX power for OFDM 6M/9M	TX1 power setting	TX0 power setting
E1h	66	TX power for OFDM 12M/18M	TX1 power setting	TX0 power setting
E2h	66	TX power for OFDM 24M/36M	TX1 power setting	TX0 power setting
E3h	66	TX power for OFDM 48M/54M	TX1 power setting	TX0 power setting
E4h	66	TX power for HT MCS=0,1	TX1 power setting	TX0 power setting
E5h	66	TX power for HT MCS=2,3	TX1 power setting	TX0 power setting
E6h	66	TX power for HT MCS=4,5	TX1 power setting	TX0 power setting
E7h	66	TX power for HT MCS=6,7	TX1 power setting	TX0 power setting
E8h	66	TX power for HT MCS=8,9	TX1 power setting	TX0 power setting
E9h	66	TX power for HT MCS=10,11	TX1 power setting	TX0 power setting
EAh	66	TX power for HT MCS=12,13	TX1 power setting	TX0 power setting
EBh	66	TX power for HT MCS=14,15	TX1 power setting	TX0 power setting
ECh	66	TX power for STBC MCS=0,1	TX1 power setting	TX0 power setting
EDh	66	TX power for STBC MCS=2,3	TX1 power setting	TX0 power setting
EEh	66	TX power for STBC MCS=4,5	TX1 power setting	TX0 power setting
EFh	66	TX power for STBC MCS=6,7	TX1 power setting	TX0 power setting

Example:
If the calibrated TX0 & TX1 power =15dBm for MCS 14 & MCS 15 = 0x66 (offset = EBh).
Want to set both TX0 & TX1 power to 19dBm for MCS 0 & MCS 1 (offset = E4h).
The power difference is 4dBm (19-15). It need to increase register value from 6 to A (4dBm = 4 step).
i.e. setting E4h=0xAAh can meet the power requirement.

2.25 BBP Instructions (total 8 instructions) (F0h ~ FEh)

8 spare BBP instructions are reserved in E2PROM; each instruction is a <BBP register ID, BBP register value> pair which instructs device driver to initialize the specified BBP register with the specified value upon NIC initialization.

BBP instructions with value <FF, FF> or <00,00> are considered invalid and will be ignored.

2.26 Serial Number for Customer (110h ~ 117h)

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2.27 Device Configuration (2E0h)

7	6	5	4	3	2	1	0
Reserved				Force Timer0 enable	NOR flash type	8051 power management status	

[Note] b0 and b1 are one-hot.

Device Configuration Register Bit Fields Description

Field	Description
1:0	8051 power management status 00: AWAKE. Always on 01: DOZE. Allow 8051 to enter low power mode only when there is no active task 10: SLEEP. Deeper sleep mode for 8051. Active tasks are serviced every 40us.
2	NOR flash type. 0: MX29LV033A or AT49BV322A compatible 1: Reserved
3	Force Timer0 enable
7:4	Reserved

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