OLinuXino EEPROM content

Olimex Ltd.

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Contents

1 Introduction

This document applies for all Olimex-made boards with Allwinner A20 chip and EEPROM memory. The EEPROM memory blocks eight (8) I2C addresses from 0x50 to 0x57; consider that when using the same I2C/TWI line for other peripherals.

2 Memory layout

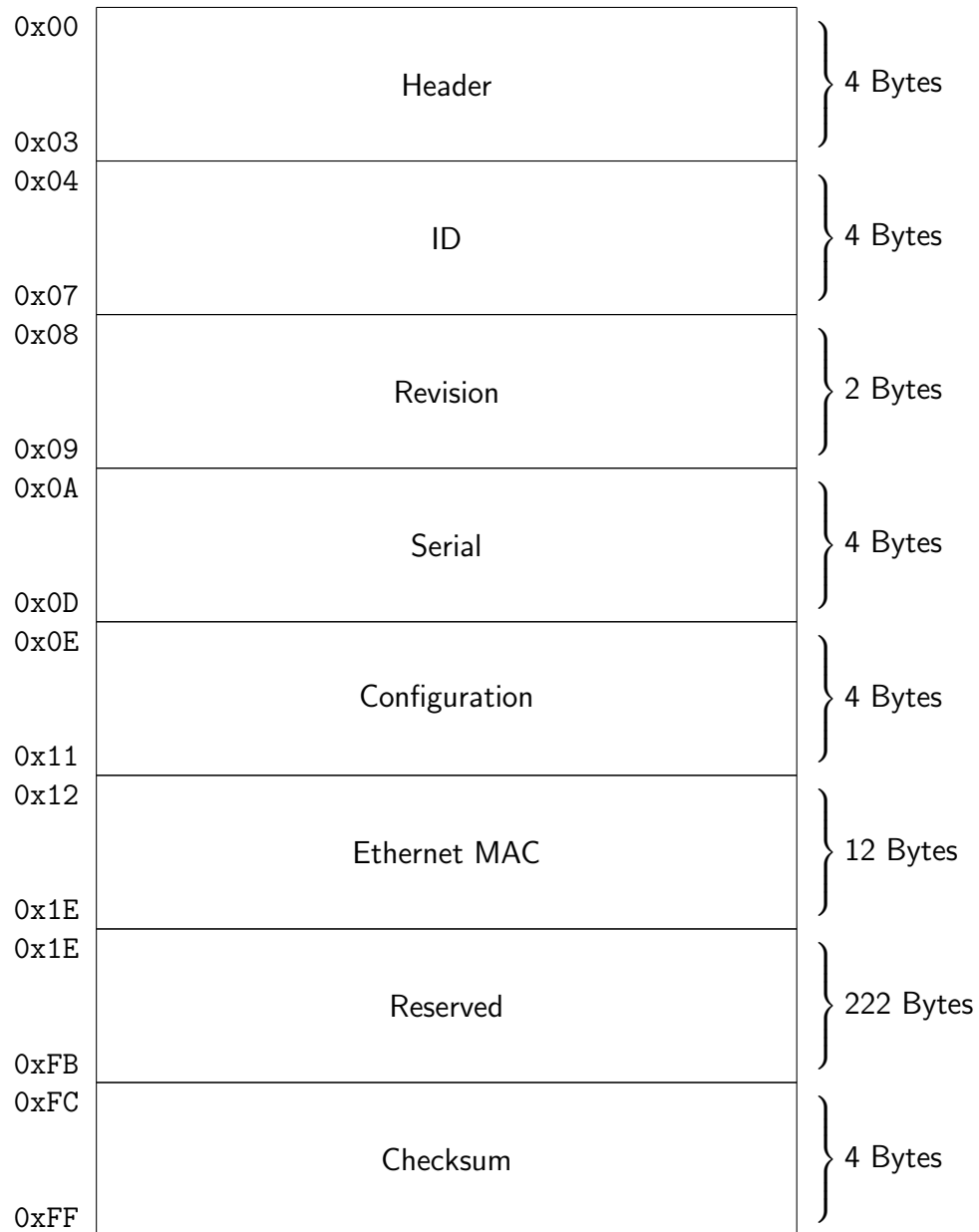|		
0x00	Header	4 Bytes
0x03		
0x04	ID	4 Bytes
0x07		
0x08	Revision	2 Bytes
0x09		
0x0A	Serial	4 Bytes
0x0D		
0x0E	Configuration	4 Bytes
0x11		
0x12	Ethernet MAC	12 Bytes
0x1E		
0x1E	Reserved	222 Bytes
0xFB		
0xFC	Checksum	4 Bytes
0xFF		

Figure 1: Memory layout schematic

2.1 Header

Header is 4 bytes long. It marks the beginning of configuration page. It is hard-coded and always should be the same.

0x00	0x55	
0x01	0xAA	0x4F4CAA55
0x02	0x4C	
0x03	0x4F	

2.2 ID

ID field is 4 bytes long. Value is stored as unsigned int. Board ID is unique.

0x04	Byte0	
0x05	Byte1	8918
0x06	Byte2	
0x07	Byte3	

2.3 Revision

This section is 2 bytes long. It stores board revision number in ASCII code: *C*, *J1*, etc.

0x08	Major	"G5"
0x09	Minor	

Where:

- **Major** - General revision of the board, when there are big changes. For example: *A*, *B*, *C*, etc.

- **Minor** - When PCB is the same, but some values differ - resistors, capacitors, etc. If not used should be *00h*.

2.4 Serial

Serial number is hold as hexadecimal unsigned long int. It's sequential number.

```
0x0A  |   Byte0   |  ⎫
0x0B  |   Byte1   |  ⎬  0x12345678
0x0C  |   Byte2   |  ⎪
0x0D  |   Byte3   |  ⎭
```

2.5 Configuration

This section is 4 bytes long. Here is stored board configuration - *NAND*, *eMMC*, etc.

```
0x0E  |  Storage  |  ⎫
0x0F  |   Size    |  ⎬  0x4E03
0x10  |   RAM     |  ⎪
0x11  |  Grade    |  ⎭
```
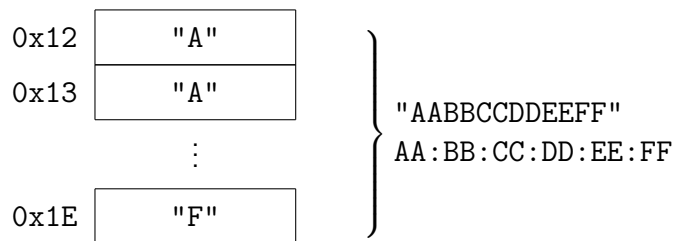
Where:

- **Storage** - Describes if there is external storage chip.

- **Size** - Capacity of the device. Usable only if "Storage" is different from 0xFF.

- **RAM** - RAM capacity.

- **Grade** - Board grade.

2.6 Ethernet MAC

The thernet MAC address is stored as ASCII chars in 12 bytes. Each board is given unique MAC address, related to the unique ID.

Important: The EEPROM memories of A20-SOM boards are an exceptions, since A20-SOM has no Ethernet chip on-board! These A20-SOM EEPROM memories are not loaded with valid Ethernet MAC addresses, but just FFFFFFFFFFFF.

```
0x12  |   "A"   |
0x13  |   "A"   |       "AABBCCDDEEFF"
        :                AA:BB:CC:DD:EE:FF
0x1E  |   "F"   |
```

3 Codes

Code	Description
0x00	Default value. No external storage.
0x45	eMMC chip.
0x4E	NAND chip.
0x53	SPI flash.

Table 1: Storage configuration codes

Code	Description
00	Size is 1B.
01	Size is 2B.
...	
10	Size is 1KB.
...	
20	Size is 1MB.
...	
30	Size is 1GB.
...	

Table 2: Size configuration codes

Code	Description
00	RAM is 1B.
01	RAM is 2B.
...	
10	RAM is 1KB.
...	
20	RAM is 1MB.
...	
30	RAM is 1GB.
...	

Table 3: RAM configuration codes

Code	Description
0x00	Commercial grade.
0x01	Industrial grade.

Table 4: Grade configuration codes

4 Revision

- Rev.A - 2 May 2017

- – Initial release

- Rev.B - 1 September 2017

  - – Reworked layout

- Rev.C - 7 December 2017

  - – Add Ethernet MAC node

- Rev.D - 9 October 2019

  - – Update description