

# Data Sheet

Customer Name :  
Customer P/N :  
Customer Project :  
Model Name : R8M  
Aptos P/N :

SALES MANAGER SIGNATURE	SALES SIGNATURE
CUSTOMER APPROVAL	



LEVEL  
3



# **R8M Datasheet**

**R8 + 64Gb NAND Flash/4Gb DDR3  
Memory MCP Module**

---

## DOCUMENT HISTORY

The next table gives an overview of the changes to the document

DATE	VERSION	STATUS	AUTHOR	CHANGE
Nov. 19. 2014	0.1	Draft	Allen Chang	Initial draft
Dec. 15. 2014	0.2	Draft	Allen Chang	Modify DDR3 Memory Size

## TABLE OF CONTENTS

<b>1</b>	<b>OVERVIEW.....</b>	<b>5</b>
1.1	INTRODUCTION.....	5
1.2	KEY FEATURES.....	5
1.2.1	CPU.....	5
1.2.2	GPU (3D Graphic Engine).....	5
1.2.3	VPU.....	5
1.2.4	Display Processing Ability .....	5
1.2.5	Display Output Ability.....	5
1.2.6	Image Input Ability.....	5
1.2.7	Memory.....	5
1.2.8	Peripherals.....	6
1.2.9	System.....	6
1.2.10	Security .....	6
1.2.11	Package .....	6
1.3	APPLICATION.....	7
1.4	FUNCTIONAL BLOCK DIAGRAM.....	8
<b>2</b>	<b>PIN DEFINITION .....</b>	<b>9</b>
2.1	PIN MAP .....	9
2.2	PIN DIMENSION .....	9
2.3	PIN DESCRIPTION .....	10
<b>3</b>	<b>GENERAL SPECIFICATION.....</b>	<b>13</b>
3.1	ABSOLUTE MAXIMUM RATING.....	13
3.2	RECOMMENDED OPERATION RATING .....	13
3.3	DC ELECTRICAL CHARACTERISTICS.....	13
<b>4</b>	<b>CLOCK SPECIFICATION .....</b>	<b>14</b>
4.1	24MHz OSCILLATOR SPECIFICATIONS .....	14

# **1 OVERVIEW**

## **1.1 INTRODUCTION**

This document describes the application information of R8M Module that includes Allwinner Tech's high performance processor R8 and 64Gb NAND Flash/4Gb DDR3 memory MCP. R8M is highly integrated, low power consumption, lower system cost module, which is designed for Android tablets and all high performance portable device.

## **1.2 KEY FEATURES**

### **1.2.1 CPU**

- Allwinner Tech R8 high performance CPU (ARM Cortex-A8 Core)
- 32KB I-Cache/32KB D-Cache/256KB L2 Cache
- Using NEON for video, audio, and graphic workloads eases the burden of supporting more dedicated accelerators across the SoC and enables the system to support the standards of tomorrow
- RCT JAVA-Accelerations to optimize just in time(JIT) and dynamic adaptive compilation(DAC), and reduces memory footprint up to three times

### **1.2.2 GPU (3D Graphic Engine)**

- Support Open GL ES 1.1/ 2.0 and open VG 1.1

### **1.2.3 VPU**

- Video Decoding (FULL HD)
  - Support all popular video formats, including VP6/8, AVS, H.264, H.263 , MPEG-1/2/4,etc
  - Support 1920\*1080@ 30fps in all formats
- Video encoding
  - Support encoding in H.264 MP format
  - Up to 1920\*1080@30fps

### **1.2.4 Display Processing Ability**

- Four moveable and size-adjustable layers
- Support multi-format image input
- Support image enhancement processor
- Support Alpha blending /anti-flicker
- Support Hardware cursor
- Support output color correction (luminance / hue / saturation etc)

### **1.2.5 Display Output Ability**

- Flexible LCD interface (CPU / Sync RGB )

### **1.2.6 Image Input Ability**

- Camera sensor interface (CSI)

### **1.2.7 Memory**

- Build in DDR3 4Gb (256Mx16) and NAND Flash 64Gb (MLC)

### **1.2.8 Peripherals**

- One USB 2.0 OTG controller for general application and one USB EHCI/OHCI controller for host application
- Three high-speed memory controllers supporting SD version 3.0 and eMMC version 4.3
- One UART with only TX/RX and one UART with RTS/CTS
- Three SPI controllers
- Three Two-Wire Interfaces
- IR controller supporting CIR remoter
- 6-bit LRADC for line control
- Internal 4-wire touch panel controller with pressure sensor and 2-point touch
- Internal 24-bit Audio Codec for 2-Ch headphone and 1-Ch microphone
- PWM controller

### **1.2.9 System**

- 8-Ch normal DMA and 8-Ch dedicated DMA
- Internal 48K SRAM on chip
- 6 asynchronous timers, 2 synchronic timers, 1 watchdog, and 2 AVS counters

### **1.2.10 Security**

- Security System
- Support DES/3DES/AES encryption and decryption
- Support SHA-1, MD5 message digest
- Support 160-bit hardware PRNG with 192-bit seed
- 128-bit EFUSE chip ID

### **1.2.11 Package**

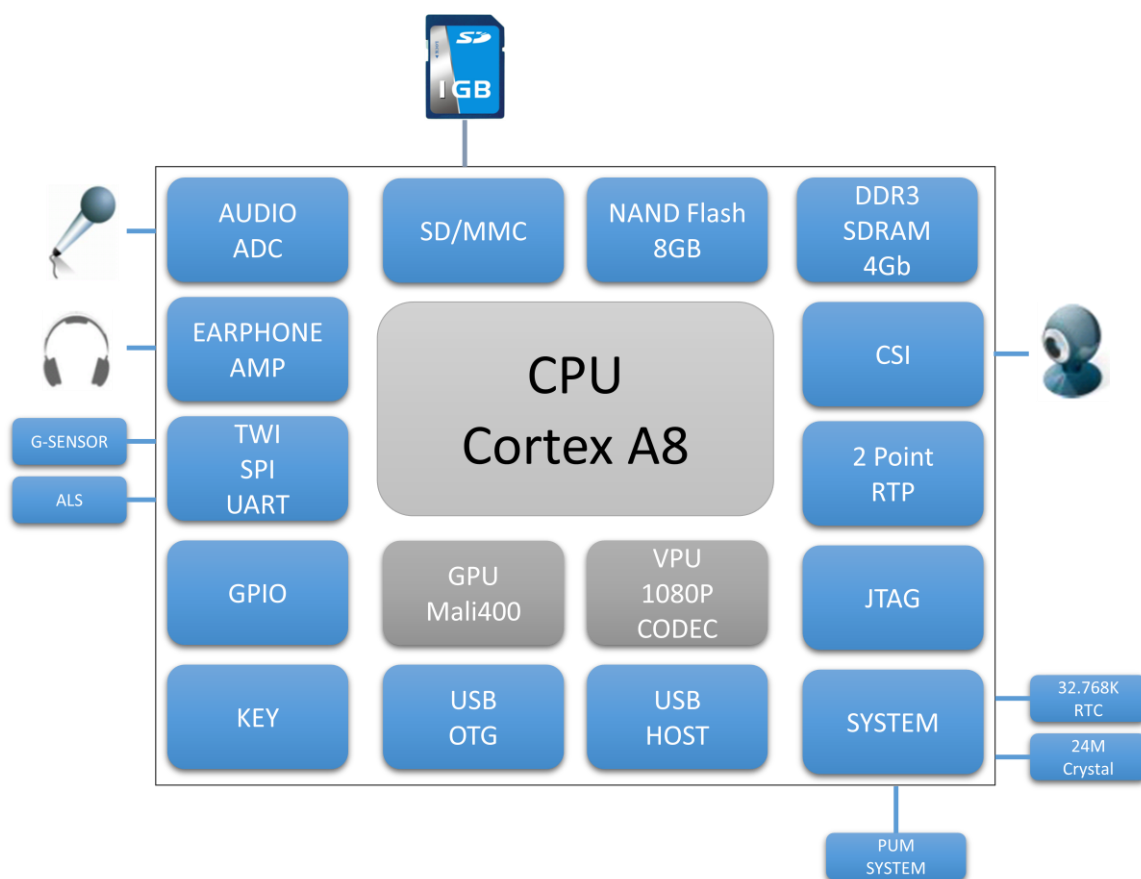
- LGA128 package

### **1.3 APPLICATION**

- Tablet and phablet
- Portable navigation devices
- High performance CPU application portable device

## 1.4 FUNCTIONAL BLOCK DIAGRAM

The functional block diagram of R8M module is shown in the figure below.





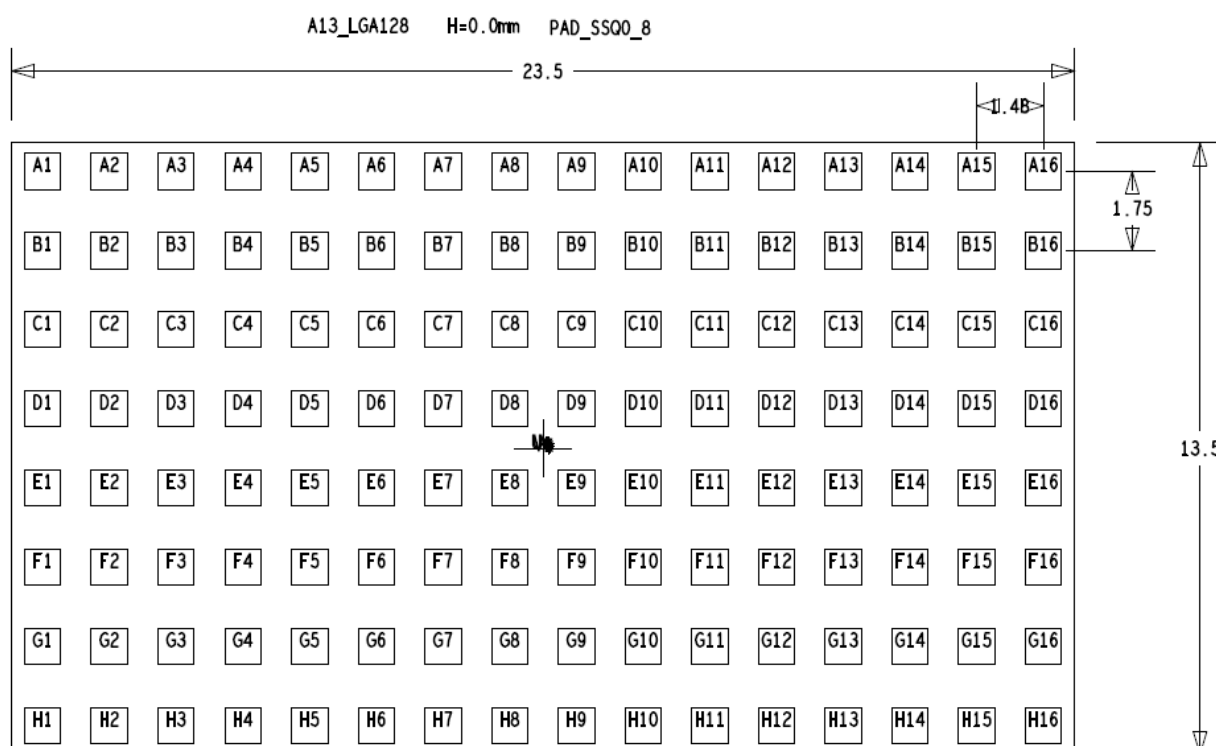
## 2 PIN DEFINITION

### 2.1 PIN MAP

TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	TPY2	VRA2	HPOUTL	HPCOM	HPOUTR	PB2	TVOUT0	PE3	X24MOUT	X24MIN	UDM0	UDP0	UDM1	UDP1	GND
B	TPY1	TPX1	TPX2	VRA1	MICIN1	VRP	AGND	PD26	PD24	PE9	PF5	PF0	LRADC	PD23	PD21	PD14
C	PF1	PE4	VCC_DRAM	VCC_DRAM	PE7	VMIC	PE5	PE1	PB15	PF3	AVCC	PB0	VDD_INT	VDD_INT	VCC	PD10
D	PE6	PE10	VCC_DRAM	VCC_DRAM	PD27	PD19	PE11	GND	GND	GND	PD22	PD20	VDD_INT	VDD_INT	VCC	PD3
E	GND	PB16	PF2	PB1	PD15	GND	GND	GND	GND	GND	PD18	PD12	GND	GND	UBOOT	PD5
F	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	PB4	PD2	GND	VDD_CPU	VDD_CPU	PB3
G	GND	GND	PB10	PG9	PG11	PG12	PG10	PG0	PG4	PD11	PD4	PG2	HMI_N	VDD_CPU	VDD_CPU	RESET_N
H	GND	GND	PE0	PF4	PD13	PE2	PE8	PD25	PD6	PB17	PC19	PB18	PD7	PG1	PG3	GND

### 2.2 PIN DIMENSION



## 2.3 PIN DESCRIPTION

PIN NO	Name	Type	Description
A1	GND	-	Ground
A2	TPY2	I	Touch Panel ADC input Y2
A3	VRA2	A	Audio reference voltage 0V
A4	HPOUT	O	Headphone Left channel output
A5	HPCOM	O	Headphone amplifier output
A6	HPOUTR	O	Headphone Right channel output
A7	PB2	I/O	PWM/EINT16/PB2
A8	TVOUT0	O	TV Output
A9	PE3	I/O	CSI_VSYNC/SPI2_MISO/PE3
A10	X24MOUT	O	Main 24MHz crystal Output for internal OSC
A11	X24MIN	I	Main 24MHz crystal Input for internal OSC
A12	UDM0	I/O	USB OTG D-
A13	UDP0	I/O	USB OTG D+
A14	UDM1	I/O	USB Host D-
A15	UDP1	I/O	USB Host D+
A16	GND	-	Ground
B1	TPY1	I	Touch Panel ADC input Y1
B2	TPX1	I	Touch Panel ADC input X1
B3	TPX2	I	Touch Panel ADC input X2
B4	VRA1	A	Audio reference voltage 1.5V
B5	MICIN1	I	microphone input
B6	VRP	A	Audio reference voltage 3.3V
B7	AGND	-	Analog Ground
B8	PD26	I/O	LCD_HSYNC/PD26
B9	PD24	I/O	LCD_CLK/PD24
B10	PE9	I/O	CSI_D5/SDC2_CLK/PE9
B11	PF5	I/O	SDC0_D2/PF5
B12	PF0	I/O	SDC0_D1/PF0
B13	LRADC	I	Low resolution ADC input
B14	PD23	I/O	LCD_D23/PD23
B15	PD21	I/O	LCD_D21/PD21
B16	PD14	I/O	LCD_D14/PD14
C1	PF1	I/O	SDC0_D0/PF1
C2	PE4	I/O	CSI_D0/SDC2_D0/PE4
C3	VCC_DRAM	P	DC Supply Voltage for DRAM Part
C4	VCC_DRAM	P	DC Supply Voltage for DRAM Part
C5	PE7	I/O	CSI_D3/SDC2_D3/PE7
C6	VMIC	P	Microphone power output
C7	PE5	I/O	CSI_D1/SDC2_D1/PE5
C8	PE1	I	CSI_MCLK/SPI2_CLK/EINT15/PE1
C9	PB15	I/O	TWI1_SCK/PB15
C10	PF3	I/O	SDC0_CMD/PF3
C11	AVCC	P	ANALOG POWER 3.0V INPUT
C12	PB0	I/O	TWI0_SCK/PB0
C13	VDD_INT	P	DC Supply Voltage for Internal Digital Logic

C14	VDD_INT	P	DC Supply Voltage for Internal Digital Logic
C15	VCC	P	DC Supply Voltage for I/O
C16	PD10	I/O	LCD_D10/PD10
D1	PE6	I/O	CSI_D2/SDC2_D2/PE6
D2	PE10	I/O	CSI_D6/UART1_TX/PE10
D3	VCC_DRAM	P	DC Supply Voltage for DRAM Part
D4	VCC_DRAM	P	DC Supply Voltage for DRAM Part
D5	PD27	I/O	LCD_VSYNC/PD27
D6	PD19	I/O	LCD_D19/PD19
D7	PE11	I/O	CSI_D7/UART1_RX/PE11
D8	GND	-	Ground
D9	GND	-	Ground
D10	GND	-	Ground
D11	PD22	I/O	LCD_D22/PD22
D12	PD20	I/O	LCD_D20/PD20
D13	VDD_INT	P	DC Supply Voltage for Internal Digital Logic
D14	VDD_INT	P	DC Supply Voltage for Internal Digital Logic
D15	VCC	P	DC Supply Voltage for Analog Part
D16	PD3	I/O	LCD_D3/PD3
E1	GND	-	Ground
E2	PB16	I/O	TWI1_SDA/PB16
E3	PF2	I/O	SDC0_CLK/PF2
E4	PB1	I/O	TWI0_SDA/PB1
E5	PD15	I/O	LCD_D15/PD15
E6	GND	-	Ground
E7	GND	-	Ground
E8	GND	-	Ground
E9	GND	-	Ground
E10	GND	-	Ground
E11	PD18	I/O	LCD_D18/PD18
E12	PD12	I/O	LCD_D12/PD12
E13	GND	-	Ground
E14	GND	-	Ground
E15	UBOOT	I/O	Boot Mode selection
E16	PD5	I/O	LCD_D5/PD5
F1	GND	-	Ground
F2	GND	-	Ground
F3	GND	-	Ground
F4	GND	-	Ground
F5	GND	-	Ground
F6	GND	-	Ground
F7	GND	-	Ground
F8	GND	-	Ground
F9	GND	-	Ground
F10	GND	-	Ground
F11	PB4	I/O	PB4/IR_RX/EINT18
F12	PD2	I/O	LCD_D2/PD2
F13	GND	-	Ground

F14	VDD_CPU	P	DC Supply Voltage for CPU
F15	VDD_CPU	P	DC Supply Voltage for CPU
F16	PB3	I/O	PB3/IR_TX/EINT17
G1	GND	-	Ground
G2	GND	-	Ground
G3	PB10	I/O	PB10/SPI2_CS1/EINT24
G4	PG9	I/O	PG9/SPI1_CS0/UART3_TX/EINT9
G5	PG11	I/O	PG11/SPI1_MOSI/UART3_CTS/EINT11
G6	PG12	I/O	PG12/SPI1_MISO/UART3_RTS/EINT12
G7	PG10	I/O	PG10/SPI1_CLK/UART3_RX/EINT10
G8	PG0	I/O	PG0/EINT0
G9	PG4	I/O	PG4/UART1_RX/EINT4
G10	PD11	I/O	LCD_D11/PD11
G11	PD4	I/O	LCD_D4/PD4
G12	PG2	I/O	PG2/EINT2
G13	NMI_N	A	External Fast Interrupt Request
G14	VDD_CPU	P	DC Supply Voltage for CPU
G15	VDD_CPU	P	DC Supply Voltage for CPU
G16	RESET_N	A	System Reset Input
H1	GND	-	Ground
H2	GND	-	Ground
H3	PE0	I	CSI_PCLK/SPI2_CS0/EINT14/PE0
H4	PF4	I/O	SDC0_D3/PF4
H5	PD13	I/O	LCD_D13/PD13
H6	PE2	I	CSI_HSYNC/SPI2_MOSI/PE2
H7	PE8	I/O	CSI_D4/SDC2_CMD/PE8
H8	PD25	I/O	LCD_DE/PD25
H9	PD6	I/O	LCD_D6/PD6
H10	PB17	I/O	TWI2_SCK/PB17
H11	PC19	I/O	NDQS/PC19
H12	PB18	I/O	TWI2_SDA/PB18
H13	PD7	I/O	LCD_D7/PD7
H14	PG1	I/O	PG1/EINT1
H15	PG3	I/O	PG3/UART1_TX/EINT3
H16	GND	-	Ground

### 3 GENERAL SPECIFICATION

#### 3.1 ABSOLUTE MAXIMUM RATING

Symbol	Parameters	Min.	Typ.	Unit
TS	Storage Temperature	-20	125	℃
VCC	DC Supply Voltage for I/O	2.7	3.3	V
VDD_INT	DC Supply Voltage for Internal Digital Logic	1.0	1.3	V
VDD_CPU	DC Supply Voltage for CPU	1.0	1.3	V
AVCC	DC Supply Voltage for Analog Part	2.7	3.3	V
VCC_DRAM	DC Supply Voltage for DRAM Part	1.3	2.0	V

#### 3.2 RECOMMENDED OPERATION RATING

Parameters	Parameters	Min.	Typ.	Max.	Unit
Ta	Operating Temperature[Commercial]	-25		+85	℃
	Operating Temperature[Extended]	-40		+85	℃
GND	Ground	0	0	0	V
VCC	DC Supply Voltage for I/O	/	3.3	/	V
VDD_INT	DC Supply Voltage for Internal Digital Logic	/	1.2	/	V
VDD_CPU	DC Supply Voltage for CPU	/	1.2	/	V
AVCC	DC Supply Voltage for Analog Part	/	3.0	/	V
VCC_DRAM	DC Supply Voltage for DRAM Part	/	1.5/1.8	/	V

#### 3.3 DC ELECTRICAL CHARACTERISTICS

Symbol	Parameters	Min.	Typ.	Max.	Unit
VIH	High-Level input voltage	2.4	3.0	3.3	V
VIL	Low-Level input voltage	0	0.5	1	V
VOH	High-Level output voltage	3.3	3.3	3.3	V
VOL	Low-Level output voltage	0	0	0	V

## **4 CLOCK SPECIFICATION**

### **4.1 24MHz OSCILLATOR SPECIFICATIONS**

<b>Symbol</b>	<b>Parameters</b>	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>	<b>Unit</b>
1/(tCPMAIN)	Crystal Oscillator Frequency Range		24.000		MHz
	Frequency Tolerance at 25°C	-50	-	+50	ppm
	Maximum change over temperature range	-50	-	+50	ppm
PON	Drive level	-	-	50	uW