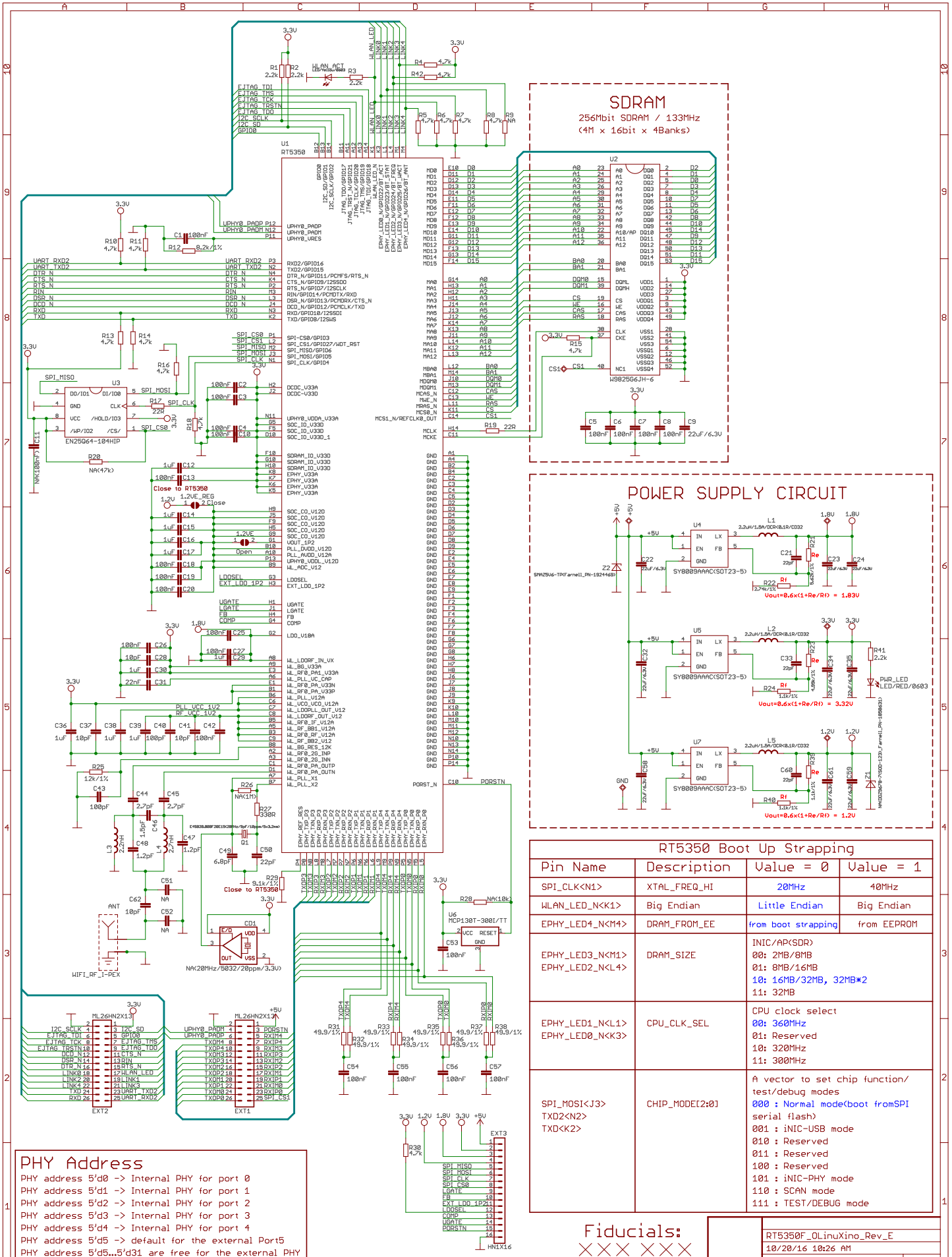

RT5350 Boot Up Strapping

Pin Name	Description	Value = 0	Value = 1
SPI_CLK<N1>	XTAL_FREQ_HI	20MHz	40MHz
WLAN_LED_N<K1>	Big Endian	Little Endian	Big Endian
EPHY_LED4_N<M4>	DRAM_FROM_EE	from boot strapping	from EEPROM
EPHY_LED3_N<M1> EPHY_LED2_N<L4>	DRAM_SIZE	INIC/AP(SDR) 00: 2MB/8MB 01: 8MB/16MB 10: 16MB/32MB, 32MB*2 11: 32MB	
EPHY_LED1_N<L1> EPHY_LED0_N<K3>	CPU_CLK_SEL	CPU clock select 00: 360MHz 01: Reserved 10: 320MHz 11: 300MHz	
SPI_MOSI<J3> TXD2<N2> TXD<K2>	CHIP_MODE[2:0]	A vector to set chip function/ test/debug modes 000 : Normal mode(boot fromSPI serial flash) 001 : iNIC-USB mode 010 : Reserved 011 : Reserved 100 : Reserved 101 : iNIC-PHY mode 110 : SCAN mode 111 : TEST/DEBUG mode	

PHY Address

PHY address 5'd0 -> Internal PHY for port 0
PHY address 5'd1 -> Internal PHY for port 1
PHY address 5'd2 -> Internal PHY for port 2
PHY address 5'd3 -> Internal PHY for port 3
PHY address 5'd4 -> Internal PHY for port 4
PHY address 5'd5 -> default for the external Port5
PHY address 5'd5...5'd31 are free for the external PHY

Fiducials:
XXX XXX

RT5350F_OLinuXino_Rev_E
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Sheet: 1/1