Errata

Title & Document Type: **1925A Word Generator Operating and Service Manual**

Manual Part Number: **01925-90901**

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HP References in this Manual

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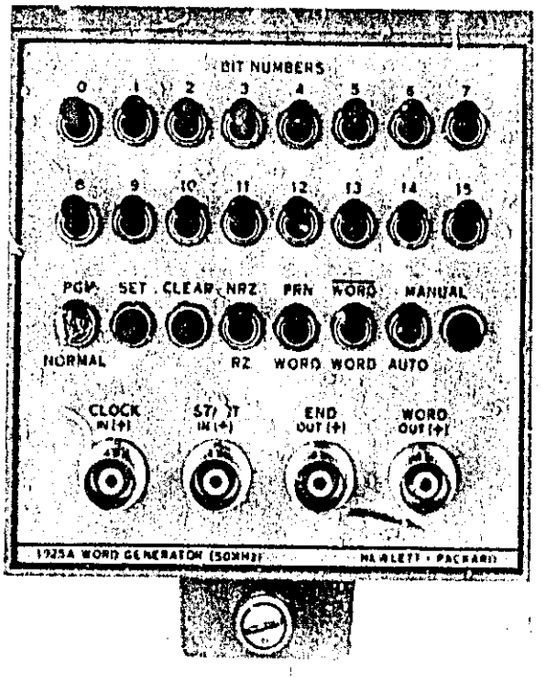
OPERATING AND SERVICE MANUAL

WORD GENERATOR 1925A



HEWLETT hp PACKARD

HP 1925A

OPERATING AND SERVICE MANUAL

MODEL 1925A
WORD GENERATOR

SERIALS PREFIXED: 920–

Refer to Section VII for Instruments Wi h Other Serial Prefixes

HEWLETT-PACKARD COMPANY/COLORADO SPRINGS DIVISION
1900 GARDEN OF THE GODS ROAD, COLORADO SPRINGS, COLORADO U.S.A.

02669-1

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Table 1-1. Specifications

FUNCTIONS

WORD LENGTH
2 to 16 bits, set by internal switches; not programable.

WORD CONTENT
Set by front-panel switches or external programing.

WORD FORMAT
NRZ/RZ, selectable from front panel or external program. RZ pulse width less than 1/2 clock period or 15 ns (whichever is smaller). $\overline{\text{WORD}}$/WORD selectable from front-panel switch.

WORD CYCLING
Automatic (continuous with one clock period delay between words), external start command, or manual pushbutton.

MANUAL/AUTO
Selectable from front-panel switch or external program. In AUTO mode, word continuously recycles with one clock period delay between words. In program mode, content of each word corresponds to the previous parallel word input that existed during END. In manual mode, a word starts after receiving an external start signal or pressing MANUAL pushbutton.

END OUT
Available from front-panel BNC corresponding to end-of-word.

SET
Serially loads 1's into shift regist r. Output word bits are all 1's after 16 clock pulses. Used to start the PRN sequence.

CLEAR
Parallel reset of shift register. Output word bits are all zero. Used to manually load the beginning of the PRN sequence if desired.

PSEUDO-RANDOM NOISE
Provides a linear shift-register sequence of 32 767 bits. The sequence starts with the last 16-bit word in shift register. Maximum clock rate is 30 MHz.

PROGRAMING
All data bits, NRZ/RZ, PRN/WORD, and MANUAL/AUTO.

INTERFACE

CLOCK INPUT
Repetition Rate:
0 to 50 MHz, 15 to 35°C.
0 to 45 MHz, 0 to 50°C.

Amplitude:
> 0.9V, < 4V.

Width:
> 4 ns, < 18 ns at + 0.6V.

Input Impedance:
50 ohms, dc-coupled.

START INPUT
Period:
> Word length plus 30 ns.

Amplitude:
> 0.9V, < 4V.

Width:
> 5 ns.

Input Impedance:
50 ohms, dc-coupled.

PROGRAMING INPUTS

True: Contact closure, saturated DTL or voltage source (TTL) < +0.2V.

False: Open, off DTL or voltage source (TTL) > 2.5V, < 4.0V.

Noise Immunity:
> 0.7V pk-pk, When True < 0.2V, False > 3.5V.

Noise Bandwidth:
< 15 MHz

WORD and END OUTPUT
True: 40 ± 10 mA current source or 2.0 ±0.5V into 50 ohms.

False:
< 1 mA

Risetime and Falltime:

< 4 ns (10% to 90%)

Perturbations:

< 15%

Source Impedance:

Unterminated current source.

WEIGHT

Net: 2.4 lbs (1,9 kg).
Shipping: 6 lbs (2,72 kg).

SECTION I

GENERAL INFORMATION

1-1. DESCRIPTION.

1-2. The HP Model 1925A Word Generator, shown in Figure 1-1, is a digital bit-generating plug-in unit designed for use in the 1900-series mainframe. The Model 1925A Word Generator (hereafter referred to as the Model 1925A) generates a variable length, dc-to-50 MHz, digital word. A word is a series of bits which are serially transmitted during a preset period of time. The bits are arranged in specific formats. Operating modes that are available are return-to-zero (RZ) or non-return-to-zero (NRZ) format, complementary output, command or automatic word recycling, and electronic programing. In addition, a long pseudo-random sequence (32 767 bits) is provided for testing communications channels and LSI memories. The internal register may be set or cleared from the front panel to establish reference levels and sequences. Emitter-coupled integrated circuits are used in the Model 1925A. The digital word is generated from either the front-panel switches or from an external program source. The digital word is generated by first loading it (in parallel) into an open-end shift register. The word is then serially transferred from the register in synchronism with the clock input. The shift register output is controlled to produce the desired modes of operation.

1-3. The Model 1925A is designed primarily to interface with the 1900-series plug-in instruments. It will accept clock pulses from the Model 1905A and Model 1906A Rate Generators. It will supply compatable trigger pulses to the Model 1915A and Model 1917A Variable Transition Time Output Generators. When used with the 1900-series plug-in units, the Word Generator System is extremely useful in the following applications:

a. testing digital communications systems.

b. interface between digital instruments.

c. testing memory circuitry.

d. testing logic circuitry.

1-4. EQUIPMENT AVAILABLE BUT NOT SUPPLIED.

1-5. A complete line of electronic test equipment is available from the Hewlett-Packard Company for making test measurements and maintaining the Model 1925A. Also available are cables, connectors, adapters, extenders and other accessory items for use in various test and measurement applications. For information on specific items, refer to the HP catalog or contact the nearest Hewlett-Packard Sales/Service Office.

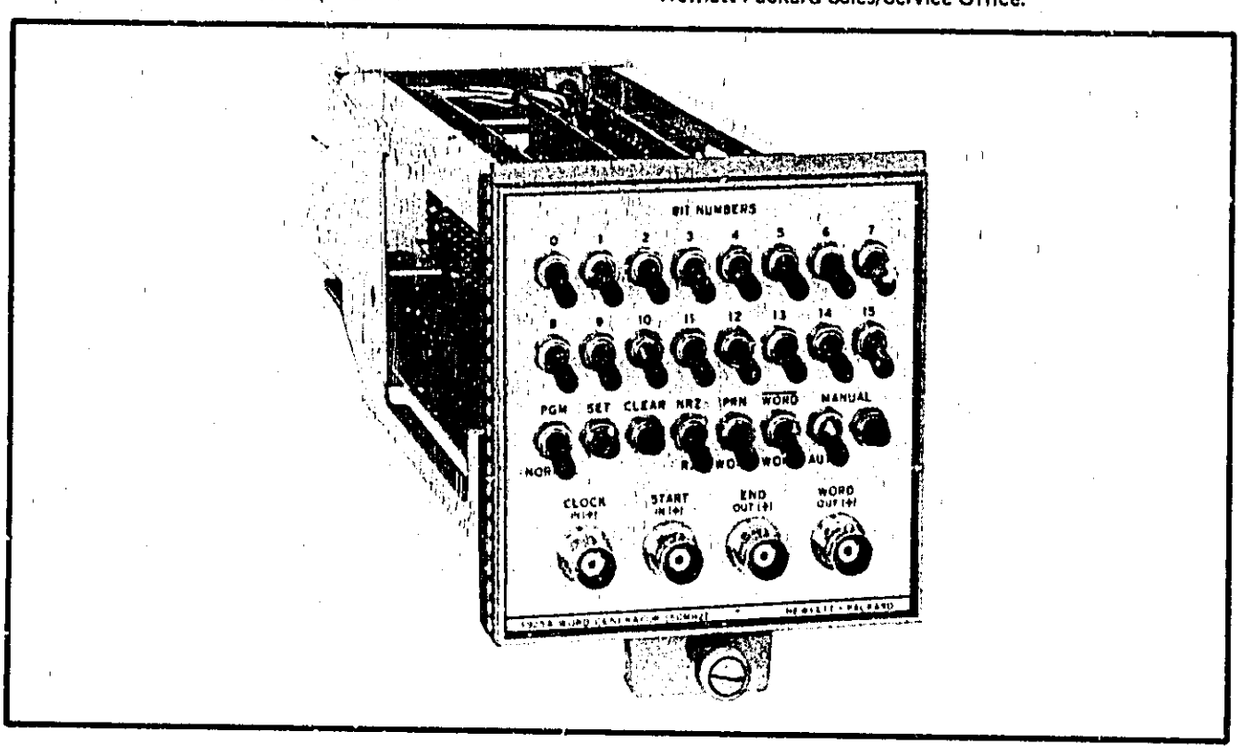


Figure 1-1. Model 1925A Word Generator

1-6. INSTRUMENT IDENTIFICATION.

1-7. This manual applies directly to Model 1925A instruments with a serial prefix as listed on the title page. The serial prefix is the first three digits of the eight-digit serial number (000-00000) used to identify each HP instrument.

1-8. MANUAL CHANGES.

1-9. As changes or refinements are made in the Model 1925A, newer instruments may have different serial prefixes assigned. Check the serial prefix of the instrument. If the serial prefix of the instrument is different from that listed on the title page, a MANUAL CHANGES sheet will be provided to update the manual to correspond with the newer instrument. If manuals are received for older type instruments, refer to SECTION VII for backdating information.

1-10. Any known corrections to the manual due to errors that existed when it was printed are called errata. These corrections (if any) will also appear on a MANUAL CHANGES sheet.

1-11. INQUIRIES.

1-12. Refer any questions regarding MANUAL CHANGES sheets, the manual, or the instrument in general to the nearest HP Sales/Service Office. Always identify the instrument by both model number and complete serial number (eight digits) in all correspondence. Refer to the inside rear cover of the manual for a world-wide listing of HP Sales/Service Offices.

SECTION II

INSTALLATION

2-1. INITIAL INSPECTION.

2-2. MECHANICAL CHECK. Inspect the Model 1925A upon receipt for any damage which may have occurred in transit. Check for external damage such as broken switches, bent or broken connectors, and dents or scratches on the panel surface. If damage is found, refer to Paragraph 2-6 for recommended claim procedure. Retain packaging material for possible future use.

2-3. ELECTRICAL CHECK. Check the electrical performance of the Model 1925A as soon as possible after receipt (refer to Section V for recommended performance checks). These checks verify that the Model 1925A is operating within the specifications listed in Table 1-1. The performance check is a good test procedure for incoming quality-control inspection. Initial performance and accuracy of the instrument are certified as stated on the inside front cover of this manual. If the Model 1925A does not operate as specified, refer to Paragraph 2-6 for the claim procedure.

2-4. PREPARATION FOR USE.

2-5. The Model 1925A may be installed in any of the four compartments of the 1900-series mainframe. It is normally placed in the left-center compartment when used with other 1900-series plug-in units to form a word generator set. To install the Model 1925A, insert the instrument into the guide rails of the appropriate mainframe compartment and carefully slide the chassis into place. Ensure that the mating connectors on the instrument are properly joined to the mainframe compartment connectors. Secure the Model 1925A by tightening the locking knob located below the front panel of the instrument. All required operating power is supplied by the 1900-series mainframe. When removing the Model 1925A from the 1900-series mainframe, unscrew the locking knob, grip it firmly, and pull the unit straight out. Never use the unit control switches or jacks as handles for removing the unit.

2-6. CLAIMS.

2-7. The warranty statement applicable to all Hewlett-Packard Company instruments and products is provided inside the front cover of this manual. If physical damage is found or if operation is not as specified when the instrument is first received, notify the carrier and the nearest Hewlett-Packard Sales/Service Office immediately (see list in back of manual for addresses). The HP Sales/Service Office will arrange for repair or replacement without waiting for settlement of the claim with the carrier.

2-8. REPACKAGING FOR SHIPMENT.

2-9. If the Model 1925A is to be shipped to a Hewlett-Packard Sales Office for service or repair, attach a tag showing owner (with address), instrument serial number (all eight digits), and a description of the service or repair required.

2-10. The original shipping carton and packaging material may be reusable. The HP Sales/Service Office will provide information and recommendations on materials to be used if the original packaging material is not available. Materials used for shipping an instrument should include the following:

a. a double-walled carton; refer to Table 2-1 for test strength required.

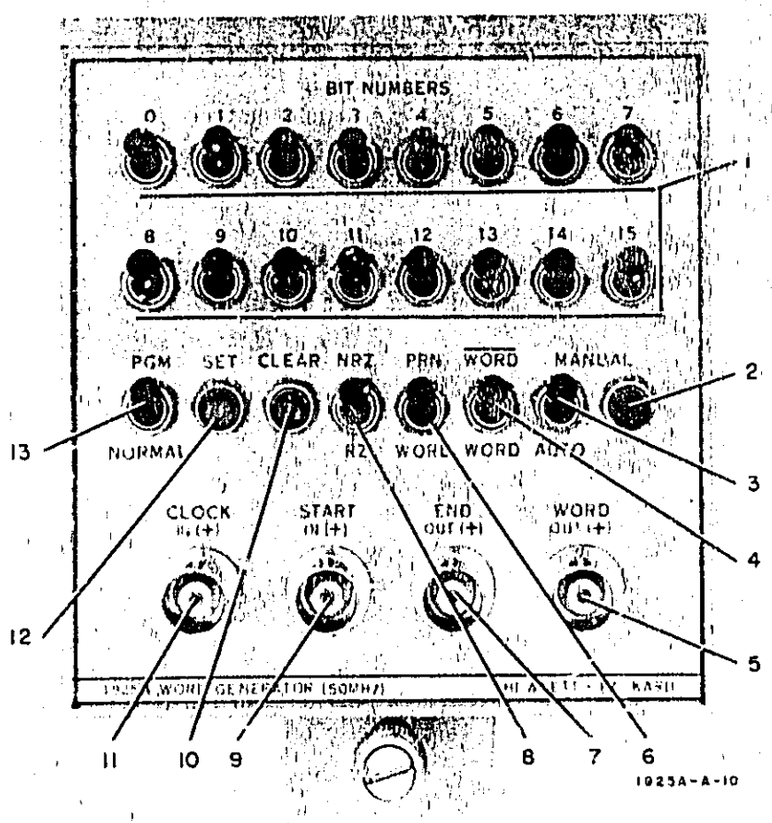
b. heavy paper or sheets of cardboard to protect all instrument surfaces; use a non-abrasive material such as polyurethane or cushioned paper such as Kimpak around all projecting parts.

c. a minimum of 4 inches of tightly-packed, industry-approved, shock-absorbing material, such as extra-firm polyurethane foam.

d. heavy-duty shipping tape to secure the outside of the carton.

Table 2-1. Shipping Carton Strength

Gross Weight (lbs)	Carton Strength (Test lbs)
up to 10	200
10 to 30	275
30 to 120	350
120 to 140	500
140 to 160	600



1. BIT NUMBERS. Selects desired bit of information required.

2. MANUAL. Cycles instrument when operating in the MANUAL mode of operation.

3. MANUAL/AUTO. Selects either manual or automatic word recycling.

4. $\overline{\text{WORD}}$/WORD. $\overline{\text{WORD}}$ produces the complementary output of WORD.

5. WORD OUT (+) Output connector for generated WORD.

6. PRN/WORD Selects either psuedo-random-noise sequence or WORD mode of operation.

7. END OUT (+) Output connector for signal that indicates end of WORD.

8. NRZ/RZ Selects method of output pulse format. In the RZ position, all bit pulses are returned to a 0-volt level. In the NRZ position, the voltage level is not returned to zero between consecutive bit pulses.

9. START IN (+). Input connector for external start command.

10. CLEAR Pushbutton switch for manually resetting the flip-flops in the shift register.

11. CLOCK IN (+) Input connector for external clock signal.

12. SET Used to start pseudo-random-noise sequence if all the flip-flops in the shift register are in the reset state. Will set all flip-flops.

13. PGM/NORMAL Instrument is controlled from an external source when in the PGM position. NORMAL operation uses the front-panel controls. (Program all bits plus NRZ/RZ, PRN/WORD, MANUAL/AUTO)

Figure 3-1. Front-Panel Controls and Connectors

SECTION III

OPERATION

3-1. INTRODUCTION.

3-2. This section contains information covering the functions of the front-panel switches and connectors of the Model 1925A Word Generator. It also provides instructions for operating the instrument.

3-3. CONTROLS AND CONNECTORS.

3-4. The connectors and switches on the front panel of the Model 1925A are identified and described in Figure 3-1. A detailed description of each connector and switch is given in the following paragraphs.

3-5. BIT NUMBERS. The bit number switches are used to load the shift register with information. A maximum of 16 bits may be temporarily stored. When the instrument is operated in the PGM (external program) mode, the bit switches are disabled. In the NORMAL mode of operation, the bit switches override any information that may be present on the external program input lines.

3-6. MANUAL. In the MANUAL mode of operation, the MANUAL pushbutton switch is used to cycle the instrument through one word sequence.

3-7. MANUAL/AUTO. The control of the Model 1925A is accomplished by a flip-flop which determines the WORD state. When the WORD state is false, the shift register is loaded with incoming data and the counter is preset to the desired word length. In the AUTO mode of operation, the above sequence is accomplished during one clock period. On the next clock pulse, the WORD state becomes true. The information stored in the shift register is automatically transmitted in serial form to the output circuit. In the MANUAL mode of operation, the WORD state remains false until the receipt of an external START signal or a command from the MANUAL pushbutton switch.

3-8. $\overline{\text{WORD}}$/WORD. When the instrument is operated in the $\overline{\text{WORD}}$ position, a complementary output of the stored data will be generated. In the WORD position, the true state of the stored data will be generated

3-9. WORD OUT (+). The information generated by the bit number switches or from an external source is temporarily stored in the shift register. This information is transferred from the shift register in serial format. The output of the shift register is amplified and applied to the WORD OUT (+) connector.

3-10. PRN/WORD. In the pseudo-random-noise mode of operation, the WORD state never becomes false. In this mode of operation, a feedback circuit is energized which applies a variable bit sequence to the shift register. This results in a maximum-length linear sequence of 32 767 bits. The sequence starts from the point coinciding with the data stored in the shift register. This feature may be used to construct special codes. To start the PRN sequence at a particular word, accomplish the following:

a. Set the front-panel MANUAL/AUTO switch to MANUAL.

b. Set the front-panel PRN/WORD switch to WORD.

c. Reset shift register (CLEAR).

d. Load data.

e. Set the front-panel PRN/WORD switch to PRN.

f. Set the front-panel MANUAL/AUTO switch to AUTO. PRN starts on loaded word and continues as long as clock pulses are provided.

3-11. END OUT (+). The END output is the logical complement of the WORD state. It is logically true between output words. The signal is available at the END OUT (+) connector. It is used for synchronizing external equipment or for commanding a new word from an external program source.

3-12. NRZ/RZ. The non-return-to-zero or return-to-zero mode of operation presents the desired pulse train in the output circuit. In the non-return-to-zero mode of operation, consecutive bit pulses are not returned to a zero voltage level between bits. They remain at a constant level. In the return-to-zero mode of operation, all bit pulses are returned to a zero voltage level prior to the next bit pulse being generated. When using the NRZ format, the output amplifier (Model 1915A or Model 1917A) must be in the external pulse width mode of operation. When using the RZ format, the output amplifier must be in the internal pulse width mode of operation.

3-13. START IN (+). In the manual mode of operation, a start pulse from an external source is required to cycle the word generator. The start pulse serves the same function as the MANUAL cycle pushbutton switch on the front panel. The leading edge of the start pulse is differentiated to cycle the word generator. The start pulse can be of any width between 10 nanoseconds and the period of the word cycle.

3-14. CLEAR. The CLEAR pushbutton switch is used to clear the shift register of any information that may have been stored previously. When the CLEAR pushbutton is pressed, all flip-flops in the shift register are reset.

Table 3-1. PGM Input Logic

P2 Pin Connectio..	Function	Input required
1	Bit 0	True: grd or 0 volts False: open or +4 volts
2	Bit 1	True: grd or 0 volts False: open or +4 volts
3	Bit 2	True: grd or 0 volts False: open or +4 volts
4	Bit 3	True: grd or 0 volts False: open or +4 volts
5	Bit 4	True: grd or 0 volts False: open or +4 volts
6	Bit 5	True: grd or 0 volts False: open or +4 volts
7	Bit 6	True: grd or 0 volts False: open or +4 volts
8	Bit 7	True: grd or 0 volts False: open or +4 volts
9	Bit 8	True: grd or 0 volts False: open or +4 volts
10	Bit 9	True: grd or 0 volts False: open or +4 volts
11	Bit 10	True: grd or 0 volts False: open or +4 volts
12	Bit 11	True: grd or 0 volts False: open or +4 volts
13	Bit 12	True: grd or 0 volts False: open or +4 volts
14	Bit 13	True: grd or 0 volts False: open or +4 volts
15	Bit 14	True: grd or 0 volts False: open or +4 volts
16	Bit 15	True: grd or 0 volts False: open or +4 volts
17	NRZ/RZ	RZ: grd or 0 volts NRZ: open or +4 volts
18	PRN/WORD	PRN: grd or 0 volts WORD: open or +4 volts
19	MANUAL/AUTO	AUTO: grd or 0 volts MANUAL: open or +4 volts

3-15. CLOCK IN (+). An external clock is required when operating the Model 1925A. The clock input circuit is terminated in a 50 ohm load and designed to receive a 1-volt or a 20-milliampere signal.

3-16. SET. The SET pushbutton switch is used primarily during pseudo-random-noise mode of operation. When the flip-flops in the shift register are reset, no information will be generated in the PRN mode of operation. Pressing the SET pushbutton switch will initiate the random noise sequence.

3-17. PGM/NORMAL. In the NORMAL mode of operation, information is furnished to the instrument by the front-panel controls. In the PGM mode of operation, the front-panel bit switches are back biased. Programing is accomplished by an interface network which transforms contact-closure, DTL, or TTL type inputs to the proper voltage level. When rapid programing is desired, the inputs should be connected by transmission lines (twisted pairs). Refer to Table 3-1 for PGM Input logic.

3-18. OPERATING CONSIDERATIONS.

3-19. CLOCK IN (+).

3-20. The Model 1925A requires an external clock source. The instrument is designed to operate with HP type Rate Generators and is sensitive to pulse width. The width of the clock pulse must be less than 10 nanoseconds. Clock sources that are capable of producing pulses with the width specified in Table 1-1 may be used.

3-21. EXTERNAL PROGRAMING.

3-22. There are two methods of external programing that are useful. The most expeditious method is to reprogram at the start of each word. This permits the maximum possible time for the programing lines to settle to their new values. The second programing method is to strobe the data into the word generator during END. The data gates to the shift register are enabled during END and the shift register flip-flops will set on the strobed data bits. The time constant of the interface network is 100 nanoseconds. The advantage of the latter technique is that it will eliminate the need for buffer storage of the parallel programing data.

3-23. INTERFACE SWITCHES.

3-24. The instrument is equipped with four interface switches (Figure 3-2). The switches permit routing of input and output signals through selectable 1900-series mainframe transmission lines instead of the front-panel connectors. When the interface switches are set in the forward position, the associated Model 1925A input and output signals are applied to the front-panel connectors. When the interface switches are set to the rear position, the input or output signals are routed through the plug-in connector of the instrument and the 1900-series mainframe inter-compartment coaxial connectors.

Note

Do not operate the Model 1925A with the interface switches in the rear position unless the 1900-series mainframe inter-compartment coaxial cabling is properly connected. Refer to the 1900-series mainframe manual for information covering cabling configurations.

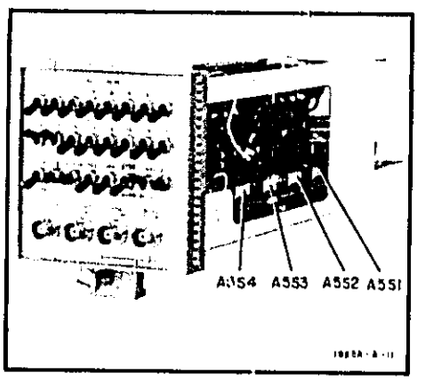


Figure 3-2. Model 1925A Interface Switches

3-25. OPERATING PROCEDURES.

3-26. To operate the Model 1925A, proceed as follows:

a. Connect an external clock source to the Model 1925A CLOCK IN (+) circuit (front-panel connector or interface routing).

b. Set the PGM/NORMAL switch to the desired position.

c. Connect the WORD OUT (+) circuit (front-panel connector or interface routing) to an appropriate variable transition time generator such as a Hewlett-Packard Model 1915A or 1917A.

d. Connect the END OUT (+) circuit (front-panel connector or interface routing) to an oscilloscope (for synchronization) or to an external program source.

Note

Since the different outputs of the Model 1925A are designed to drive input circuits of other 1900-series instruments, they are not internally terminated. To drive input circuits that are not terminated or AC terminated loads (such as some oscilloscope input circuits) END OUT (+) and WORD OUT (+) must be terminated with 50 ohms at the unit or at the load (whichever is most convenient).

e. If external programing is used, connect the START IN (+) circuit (front-panel connector or interface routing) to the external source of control.

3-27. When using the Model 1925A to generate information of less than its maximum word length (16 bits), the counter circuit must be preset to the desired count. Refer to Section IV of this manual for the proper setting of the internal divide-by switches.

3-28. There are numerous system configurations where the Model 1925A is extremely adaptable. For example, it may be used in a system configuration that requires a return-to-zero format, having 11 bits of data with a bit width T_1 and a synchronization bit of width T_2. This can be provided by using a Model 1901A low-power mainframe containing a Model 1905A Rate Generator and two Model 1925A Word Generators. The word generators, depending upon configuration requirements, could feed the following output stage combinations.

a. A Model 1901A mainframe with two Model 1920A instruments for ultra-fast risetime applications.

b. A Model 1900A mainframe and two Model 1915A or Model 1917A instruments for generating bipolar outputs. By using Model 1915A or Model 1917A instruments, the pulse width, risetime, falltime, amplitude, current offset and polarity can be independently controllable and programable.

c. Another configuration will permit elaborate and predictable testing of digital communications systems with pseudo-random-noise from a Model 1915A or Model 1917A. This configuration permits independent control of risetime, falltime, amplitude, current offset and pulse width (in the return-to-zero mode of operation). An important feature of this configuration is that the output stages are not duty-cycle limited when in the external pulse width mode of operation.

d. Refer to Table 3-2 for the Model 1925A Compatibility Chart.

Table 3-2. Model 1925A Compatibility Chart

Clock Source	Fan In	Output Stage	Fan Out
Model 1905A Rate Generator	3	Model 1915A or Model 1917A NRZ: External RZ: Internal	2
Model 1906A Rate Generator	3	Model 1920A Fast Rise (RZ only)	2
Model 1908A Delay Generator	3	Model 1908A Delay Generator (RZ only)	2
		Model 1910A Delay Generator (RZ only)	2
Model 1910A Delay Generator	3	Model 1921A Output Stage	2
		Model 1922A Output Stage	2
Model 1927A Fan-in Amplifier	2	Model 1927A Fan-in Amplifier	2
Model 1928A Fan-out Amplifier	8	Model 1928A Fan-out Amplifier	2

Fan In indicates the number of Model 1925A units that can be driven from the indicated Clock Source.

Fan Out indicates number of output stages that can be driven by one Model 1925A.

3-29. The word generators may be ganged in either series or parallel arrangements. A common clock should be used. To operate several instruments in the ganged configuration, proceed as follows:

a. Serial operation:

(1) Operate all generators in the , ode of operation.

(2) Connect the END output from one generator to the START IN (+) connector of the next generator.

(3) Connect the END output of the last generator in the series to the START IN (+) connector of the first generator.

(4) OR the WORD outputs of all the word generators with a Model 1927A Fan-in Amplifier.

(5) To start the loop operating properly, break the loop in one place. Reconnect the loop and press the MANUAL pushbutton on one Model 1925A until the loop sequences properly.

b. Parallel operation:

(1) Operate the first word generator in the AUTO recycle mode. Connect the END output of this generator to the START IN (+) connectors of the other word generators(slaves).

(2) Use a Model 1928A Fan-out Amplifier if there is more than three slaves.

(3) The output of the slave generators will correspond to the information stored by their front-panel switches.

(4) The output of the slave generators will be delayed by one bit time from the master word generator.

(5) Use a common clock for all the word generators. If the clock fan-out is greater than three units, use a Model 1928A Fan-out Amplifier.

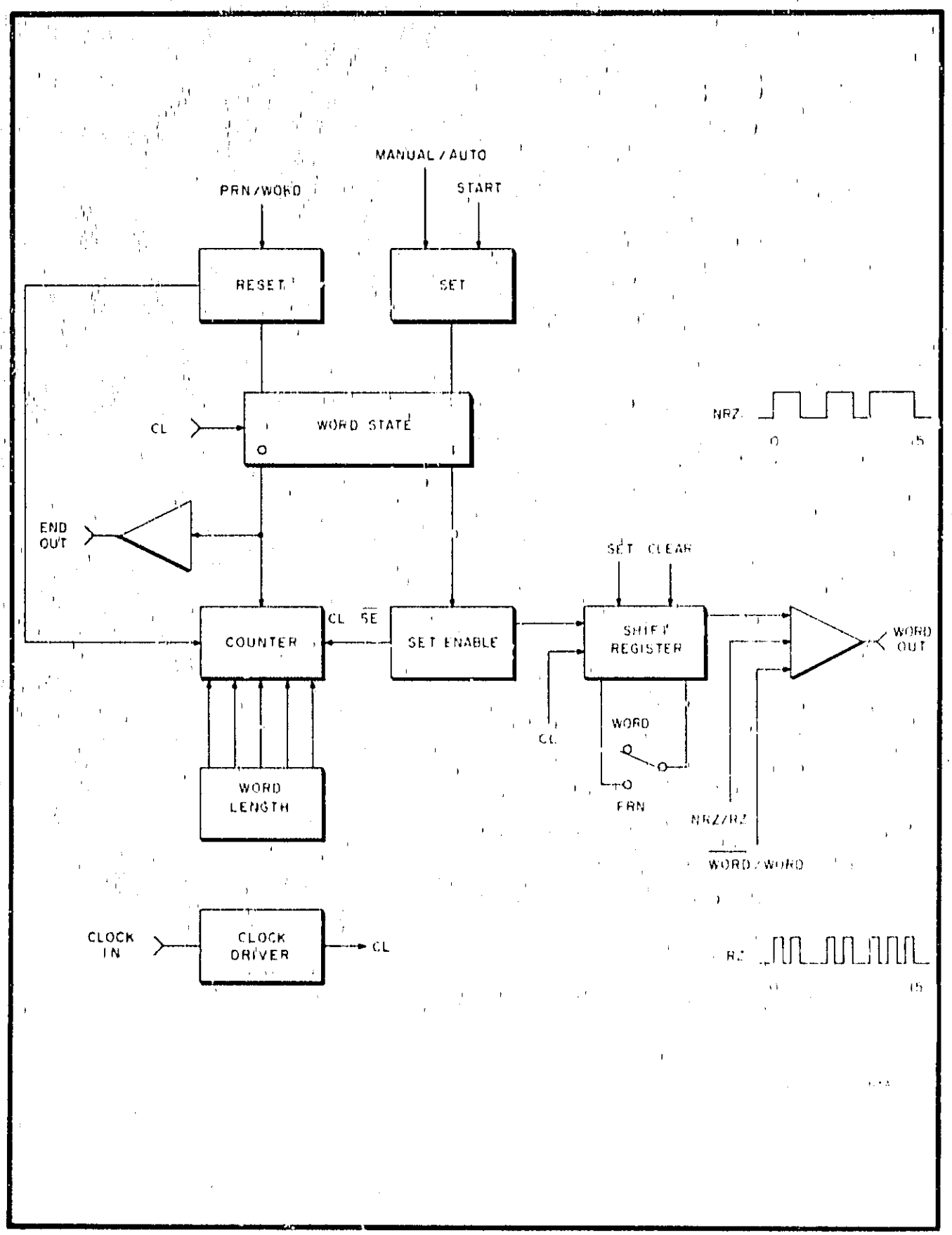


Figure 4-1. Model 1925A Block Diagram

SECTION IV

PRINCIPLES OF OPERATION

4-1. INTRODUCTION.

4-2. This section provides circuit theory analysis of the Model 1925A. Due to the complexity of the instrument, circuit theory will first be covered on a general basis, followed by a block diagram explanation and circuit details referenced to the schematics. The schematics are located in Section VIII (rear of manual). Each diagram can be unfolded and used for reference while reading the applicable text.

4-3. GENERAL THEORY.

4-4. The Model 1925A is a word generator designed for testing digital logic circuitry and integrated circuits. It can be used as a programing instrument or serve as a buffer stage between digital systems. The circuit description is arranged to present the organization and intent of circuitry in the Model 1925A. A complete and thorough study of each individual circuit is not essential to understand the instrument. The schematics in Section VIII have been drawn using logic symbols as opposed to detailed circuitry. The conventional symbology used for flip-flops, NOR gates, and inverter may be found in Table 8-1. The detailed circuitry of the flip-flops, NOR gates and inverters is not shown. An integrated circuit must be replaced as a unit when replacement is necessary.

4-5. The integrated circuits are of the emitter-coupled logic design. The typical circuit uses a differential amplifier as the input circuit with an internal bias reference and emitter-follower outputs to restore the dc level. J-K flip-flop circuits perform the sequential logic in the Model 1925A. Refer to Table 4-1 for the truth table covering J-K flip-flops.

4-6. BLOCK DIAGRAM DESCRIPTION.

4-7. Figure 4-1 is a simplified block diagram of the Model 1925A. The main circuits are the clock driver, WORD state, counter, shift register, and output circuits.

4-8. A 16-bit word can be generated from the controls on the front panel of the instrument or from an external source. When operating from an external source (PGM mode of operation) bit controls on the front panel are disabled.

Table 4-1. Clocked $\overline{J}$-$\overline{K}$ Truth Table.

Input $\overline{J}$ (Pin 3,4,5,6)	Input $\overline{K}$ (Pin 8,9,10,11)	Input CL	Output Q^n (Pin 13)
0	0	1	$\overline{Q}^n$ (changes state)
0	1	1	1
1	0	1	0
1	1	1	Q^n (no change)

Note

1. CL (Clock in): $\overline{J}$-$\overline{K}$ input tied together.

2. −0.7 Vdc nominal is defined as logic 1 or high level. −1.6 Vdc nominal is defined as logic 0 or low level.

3. The four $\overline{J}$ inputs are arranged in an OR-gate configuration. $\overline{J}$ logic input is defined as logic 0 only if all $\overline{J}$ inputs are logic 0. The same applies for $\overline{K}$ logic inputs.

4. All unused inputs are connected to logic 0.

4-9. An external clock signal is applied to the clock-driver circuit. This circuit is used to convert the clock pulses to the proper logic level required to operate the instrument. The output of the clock-driver circuit is applied to the WORD state flip-flop which controls the WORD-END logic. It is also applied to the shift register. The WORD state flip-flop controls the operation of the counter and shift register. When the WORD state is logic 1, an enable circuit is used to energize the shift register and counter. The counter operates for the number of bits established by the word-length circuitry. After counting the number of bits required, the counter resets the WORD state flip-flop. When the WORD state flip-flop is logic 0, the counter is stopped, and the set-enable signal disables the clock signal to the shift register. In addition, the set-enable signal activates the input gates to the shift register, permitting storage of new information.

4-10. The shift register stores input information when the WORD state is logic 0. When the WORD state is logic 1, the clock signal to the shift register is enabled. The shift register, operating on the clock pulses, transfers the information in serial form to the output circuit where it is amplified. The amplified bits are connected to the output jack on the front panel.

4-11. The counter is preset before the start of each count. It is preset to the predetermined count required for the selected word length. The word length is variable from 2 to 16 bits by switch action. This feature adapts the Model 1925A to most external system requirements.

4-12. CIRCUIT DETAILS.

4-13. The following functional description provides a detailed explanation of the operation of the circuits in the Model 1925A. Use the schematics as an aid in understanding the circuit description.

4-14. CLOCK DRIVER.

4-15. An external clock signal is needed to operate the Model 1925A. The clock signal may be connected to the CLOCK IN (+) connector J1 on the front panel or may be applied through the interface circuit of the 1900-series mainframe. Although the Model 1925A is designed to operate with HP 1900-series Rate Generators, other instruments which meet the input specifications may be used. Refer to Table 1-1 for specifications. The repetition rate of the clock signal may be any frequency between dc and 50 megahertz.

4-16. The clock is applied to an emitter-follower amplifier circuit consisting of transistors A1Q3 and A1Q4. The input signal is terminated by resistor A1R1. The collector voltage of A1Q3 and A1Q4 is controlled by clock-bias transistor A1Q7. A voltage divider network consisting of potentiometer A1R17 and fixed resistors A1R16 and A1R18 controls the current flow in the base of A1Q7. Potentiometer A1R17 is adjusted to maintain approximately −1.4 volts in the emitter circuit of A1Q7. This voltage is applied to the collector circuits of A1Q3 and A1Q4. With no clock signal applied, A1Q3 is conducting and the voltage drop across resistor A1R2 holds the collector at −0.2 volt dc. When a positive clock pulse is applied to the base of A1Q3, conduction ceases and the voltage on the collector becomes the clock bias voltage. The inverted clock signal ($\overline{CL}$) from the collector of A1Q3 is applied to the base of transistor A1Q2. Transistor A1Q2 operates as an emitter follower. The emitter output is applied to the clock circuitry of the instrument. Transistor A1Q1 is used to shape the clock pulses.

4-17. The clock signal is distributed to board assembly A3 through isolating resistor A1R12, and to board assembly A2 through isolating resistor A1R11. On board assembly A3 the clock pulse is used in a number of ways. It is applied to NOR gate A3A9 (pin 4). The output of A3A9 provides a clock (CL) for the return-to-zero function in the WORD output circuitry (board assembly A1). Refer to Table 4-2 for the truth logic of NOR gates used in the instrument. The clock is also applied to two sections of NOR gate A3A10. One section (input pin 10 and output pin 8) is used to control the WORD state flip-flop A3A6. The clock signal that is applied to the second section of A3A10 (pin 5) is used to control the sequential operation of the flip-flops in the counter circuit.

Table 4-2. NOR Gate Truth Logic

Input A	Input B	Output
0	0	1
1	0	0
0	1	0
1	1	0

Note

1. −0.7 volt is defined as logic 1 or high level. −1.6 volt is defined as logic 0 or low level.

2. All unused inputs are connected to logic 0 (low level).

4-18. The inverted clock signal ($\overline{CL}$) at resistor A1R11 is applied to the shift register circuitry on board assembly A2. This signal is used to transfer the stored information from the shift register to the output circuit.

4-19. WORD STATE CIRCUIT.

4-20. The WORD state of the Model 1925A is controlled by a J-K flip-flop. One of the two operating states of the instrument is storing data in the shift register with the

WORD output circuit decoupled. The other operating state is transferring data from the shift register to the output circuit. Control of the operating state of the Model 1925A is the function of J-K flip-flop A3A6. When the WORD state is logic 0 (A3A6 in the reset condition), the shift register is loaded with data from either the front-panel switches or from an external program source (PGM mode of operation). In the AUTO recycle mode of operation, the shift register is loaded during one clock period and then the stored information is automatically transferred to the WORD output circuit. In the MANUAL mode, the WORD state flip-flop remains reset until an external start signal is received or until a command is generated from the MANUAL pushbutton switch on the front panel.

4-21. The external start signal can be applied through the START IN (+) connector on the front panel or through the interface routing circuit of the 1900-series mainframe. The external start signal is terminated in resistor A1R9 (50 ohm load). The positive input signal is applied to the base of transistor A1Q6. Transistor A1Q6 is turned off by the positive start signal. With A1Q6 not conducting, a positive voltage is applied to the emitter of A1Q5 through the RC network of A1R7 and A1C4. The RC network limits the current pulse through A1Q5 to 120 nanoseconds. The positive pulse that is developed by A1Q5 is applied to the base of A1Q8. Transistor A1Q8 operates as an emitter-follower. The voltage drop across resistor A1R14 increases and a logic 1 signal is applied to the set-input terminal of WORD state flip-flop A3A6. With flip-flop A3A6 in the set condition, the data stored in the shift register is transferred to the WORD output circuit. The same sequential operation occurs when the MANUAL pushbutton switch on the front panel is pressed. Pressing the pushbutton switch grounds the anode of A1CR4. With ground applied, a 100-nanosecond pulse is developed by resistor A1R13 and capacitor A1C5. The differentiated pulse is applied to the base of transistor A1Q9. The increased voltage drop across A1R14 results in logic 1 being applied to the set terminal of flip-flop A3A6. The output of WORD state flip-flop A3A6 becomes true and

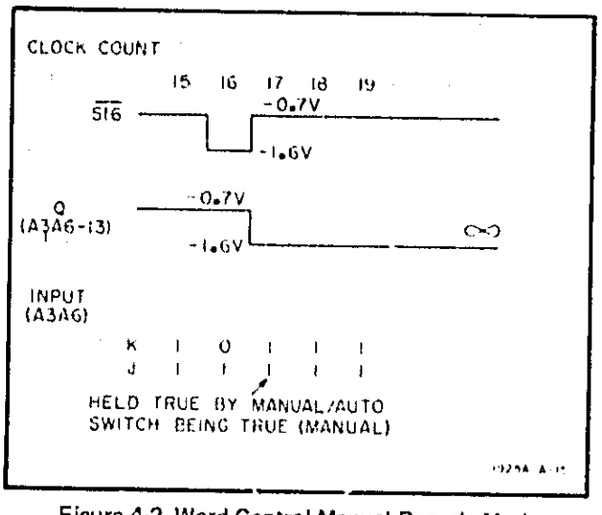


Figure 4-2. Word Control Manual Recycle Mode

the data stored in the shift register is transferred to the WORD output circuit.

4-22. The operation of the input and output circuits of the WORD state flip-flop A3A6 is as follows:

a. When the MANUAL/AUTO switch on the front panel is in the MANUAL position, logic 1 is applied continuously to J input (pin 5) of A3A6. This prevents the flip-flop from setting automatically (Figure 4-2). When the instrument is operated in the AUTO mode of operation, logic 0 is applied to J input (pin 5) of A3A6. With logic 0 now applied to all the J inputs, the flip-flop will be set automatically by the clock (Figure 4-3).

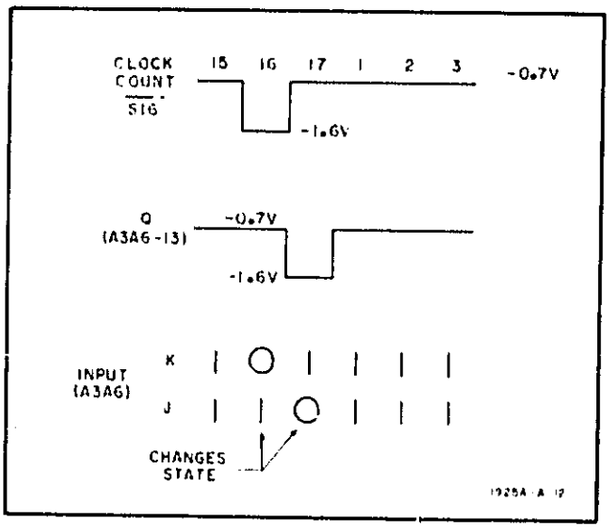


Figure 4-3. Word Control Auto Recycle Mode

b. The Q output of A3A6 (pin 13) is applied to two sections of NOR gate A3A12. The dual outputs from A3A12 (pin 3 and pin 11) produce set-enable signals SE1 and SE2. These signals, along with the clock, control the operation of the shift register. The outputs from A3A12 are the complements of the output from A3A6.

c. The END state of the instrument is the complement of the WORD state. When the A3A6 flip-flop is in the set condition, the output of $\overline{Q}$ (pin 1) is logic 0. When A3A6 is reset, the output of $\overline{Q}$ is logic 1. The $\overline{Q}$ output of A3A6 is one of the signals used to control the counter circuit. The $\overline{Q}$ output is applied to a J input (pin 5) and a K input (pin 9) of flip-flop A3A2 in the counter circuit. With logic 0 applied to these inputs, A3A2 functions normally in the count sequence. When the WORD state is false, logic 1 is applied to the inputs, and A3A2 is prevented from changing states. Further, the $\overline{Q}$ output is applied to NOR gate A3A9 (pin 2). The output of A3A9 controls word-length NOR gate A3A8. When the $\overline{Q}$ output of A3A6 is logic 0, the logic 1 output of A3A9 disables the four sections of A3A8. This prevents a change in the word length while the counter is counting. When $\overline{Q}$ output is logic 1 (END state), the inverted output of A3A9 permits the word-length switches to activate the different sections of A3A8. The outputs from A3A8 advance the counter flip-flops to the preset word count.

d. The $\overline{Q}$ output of A3A6 is also used in the control of the END and WORD output circuits. The $\overline{Q}$ output is applied to a section of NOR gate A3A9 (pin 13). The complementary output of A3A9 ($\overline{END}$) is applied to amplifier A1A2 (pin 1). Amplifier A1A2 amplifies the signal and produces a NOR and an OR output. The outputs of A1A2 (pin 5 and pin 6) are applied to the END output driver circuit. Transistors A1Q12 and A1Q13 have the outputs of A1A2 applied to their separate bases. Operating differentially, they drive output transistors A1Q10 and A1Q11. The END output is routed by switch A5S3 to either the interface routing circuit of the 1900-series mainframe or to the END OUT (+) connector J3 on the front panel.

Note

The END and WORD outputs are from current sources and cannot be damaged by an open circuit. Both outputs must be terminated in a 50-ohm load to function according to specifications.

e. The $\overline{Q}$ outputs of the counter flip-flops, A3A1 through A3A4, are applied to the four inputs of one section of OR gate A3A5. During the counting sequence, at least one $\overline{Q}$ output is logic 1. With logic 1 applied to any input, the output of A3A5 (STATE 16) is held to logic 1. When the output of A3A5 (logic 1) is applied to the K input (pin 9) of WORD state flip-flop A3A6, the flip-flop is prevented from resetting. At count 16, all $\overline{Q}$ outputs from the counter flip-flops are logic 0. The output of A3A5 is now logic 0. With logic 0 applied to the K input (pin 9) of A3A6, the flip-flop resets on the next clock pulse (provided all other K inputs are logic 0). When operating in the AUTO mode, A3A6 will change states on the next clock pulse and the cycle will be repeated.

4-23. COUNTER CIRCUIT.

4-24. The counter circuit consists of flip-flops A3A1 through A3A4 with their associated NOR gates. The counter is designed to provide a maximum of 16 counts. To sequence a word which has less than 16 bits of information, the counter is advanced to the appropriate start count during END state.

4-25. The counter flip-flops are J-K type but are connected to perform only two of the four functions of the truth logic shown in Table 4-1. The functions are as follows:

a. When the $\overline{J}$ and $\overline{K}$ inputs are logic 0 and the clock input is logic 1, the flip-flop changes states.

b. When the $\overline{J}$ and $\overline{K}$ inputs are logic 1 and the clock input is logic 1, there is no change in the state of the flip-flop.

c. The set and reset functions operate normally.

4-26. The divide network of the counter determines the number of bits that will transfer from the shift register. When a word of less than 16 bits is desired, switches A1S1 through A1S4 must be used in various combinations to establish the proper length. A word of less than 16 bits is generated by presetting the counter to compensate for the shorter count required. Prior to the start of a count for a 16-bit word, the counter flip-flops are as follows: A3A1 - reset, A3A2 - set, A3A3 - set, and A3A4 - set. Switches A1S1 through A1S4 may be used to alter the set-reset condition of the flip-flops. By arranging the switches in combinations indicated in Table 4-3, any word length from 2 to 16 bits may be selected. For example, if a word length of nine is required, proceed as follows:

a. Subtract the desired word length from 17. In this example: 17 – 9 = 8

b. Take the binary compliment of count 8 which is 1 0 0 0 (Refer to Table 4-3).

c. Invert the least significant figure = 1 0 0 1.

d. NOR with binary END state: 1 1 1 0 – 1 0 0 1 = 0 1 1 1.

e. Set divide switches (A1S1 through A1S4) for binary 0 1 1 1.

4-27. SHIFT REGISTER.

4-28. The shift register is used for temporary storage of input data. The data is applied in parallel form. Upon command, the stored data is transferred serially to the output circuit. The shift register consists of flip-flops and NOR gate assemblies A2A1 through A2A24.

4-29. Information is automatically stored in the shift register during the END state of flip-flop A3A6. The Q output of A3A6 (pin 13) is applied to two sections of NOR gate A3A12 at pin 2 and pin 13. The outputs from A3A12 furnish set-enable signals SE1 and SE2 which control the shift register operation.

4-30. The set-enable signal (SE1) and the clock complement ($\overline{CL}$) are applied to NOR gates A2A6 and A2A18. When the set-enable signal is logic 1 (A3A6 in the reset state), the outputs of NOR gates A2A6 and A2A18 are at logic 0. This prevents the clock from sequencing the shift-register flip-flops. When the set-enable signal is logic 0, the output of A2A6 and A2A18 is the clock signal. The clock outputs from these NOR gates trigger the shift-register flip-flops at a clock rate. This results in the stored information being serially transferred to the output circuit.

4-31. Set-enable signal (SE2) is used for storing information in the shift register. The signal is applied to four sections of NOR gate A2A7. The outputs of A2A7 are complements of the inputs. When the set-enable signal is logic 1, the outputs of A2A7 are logic 0. The outputs

Table 4-3. Word Length Switch Settings

Switch Position					Truth Table Output (Q)				
Word Length	S1	S2	S3	S4	A4	A3	A2	A1	Count Sequence
16	Down	Down	Down	Up	1	1	1	0	1
15	Down	Down	Up	Down	1	1	0	1	2
14	Down	Down	Up	Up	1	1	0	0	3
13	Down	Up	Down	Down	1	0	1	1	4
12	Down	Up	Down	Up	1	0	1	0	5
11	Down	Up	Up	Down	1	0	0	1	6
10	Down	Up	Up	Up	1	0	0	0	7
9	Up	Down	Down	Down	0	1	1	1	8
8	Up	Down	Down	Up	0	1	1	0	9
7	Up	Down	Up	Down	0	1	0	1	10
6	Up	Down	Up	Up	0	1	0	0	11
5	Up	Up	Down	Down	0	0	1	1	12
4	Up	Up	Down	Up	0	0	1	0	13
3	Up	Up	Up	Down	0	0	0	1	14
2	Up	Up	Up	Up	0	0	0	0	15
	Down	Down	Down	Down	1	1	1	1	16

Note

Switch Position	Voltage Applied
Up	−5.2V
Down	GRD

are applied to four NOR gates A2A1, A2A12, A2A13, and A2A24. The other inputs to these NOR gates are the bit information to be stored. Since storage of bit information is identical for all 16 bits, only the bit-15 NOR gate (one section of A2A13) and flip-flop A2A17 will be discussed. When no WORD is being transferred from the shift register, the SE2 signal that is applied to NOR gate A2A7 (pin 5) is logic 1. The complementary output of A2A7 is applied to each section of A2A13. When bit 15 is selected by either the bit-15 switch on the front panel or by a PGM input, logic 0 is applied to pin 13 of NOR gate A2A13. With a logic 0 applied to both inputs, the output of the NOR gate (pin 11) becomes logic 1. This signal is applied to the set input of flip-flop A2A17. The setting of the flip-flop stores the information. When a bit 15 is not selected by the front-panel switch or a PGM input, a logic 1 is applied to A2A13 (pin 13). With logic 1 applied to one of its inputs, the output of A2A13 is logic 0. Flip-flop A2A17 remains in the reset state and no information is stored. During word transfer out of the shift register, set-enable signal SE2 is logic 0. With the output of NOR gate A2A7 logic 1, all outputs of NOR gates A2A1, A2A12, A2A13, and A2A24 are logic 0. This prevents information from being stored in the shift register during this period.

4-32. The information that is stored in the shift register is transferred to the output circuit in a serial format. Operation of the shift register is as follows:

a. Refer to Table 4-1. Only the logic of the two middle sets apply to the shift register. When $\overline{J}$ input is logic 0 and $\overline{K}$ input is logic 1, the flip-flop will set on the clock pulse. When $\overline{J}$ input is logic 1 and $\overline{K}$ input is logic 0, the flip-flop will reset on the clock pulse.

b. Each flip-flop of the shift register has its Q-$\overline{Q}$ outputs connected to the following flip-flop. The outputs of the flip-flops are cross-coupled (Q output to $\overline{K}$ input and $\overline{Q}$ output to $\overline{J}$ input). On the clock pulse, each flip-flop assumes the set or reset condition as dictated by the signals on its $\overline{J}$-$\overline{K}$ inputs. In this manner the state of the preceding flip-flop is transferred to the following flip-flop. To illustrate, assume the situation where the bit 15 flip-flop A2A17 is in the set condition and the bit 14 flip-flop A2A16 is in the reset condition. With the WORD state true, the clock signal is applied to the shift register flip-flops through NOR gates A2A6 and A2A18. With the bit 14 flip-flop A2A16 reset, the output $\overline{Q}$ (pin 1) is logic 1 and the output Q (pin 13) is logic 0. These outputs are applied to the $\overline{J}$ and $\overline{K}$ inputs of flip-flop A2A15. Logic 1 applied to the $\overline{J}$ input and logic 0 applied to the $\overline{K}$ input results in flip-flop A2A15 resetting on the clock pulse. In the case of A2A16, signals from A3A17 are applied to its inputs. Logic 0 is applied to $\overline{J}$ input and logic 1 is applied to $\overline{K}$ input. On the same clock pulse that resets A2A15, A2A16 will set. Notice that flip-flop A2A15 assumed the state of flip-flop A2A16 and flip-flop A2A16 assumed the state of flip-flop A2A17. The shifting of bit information from flip-flop to flip-flop occurs simultaneously on each clock pulse (Figure 4-4).

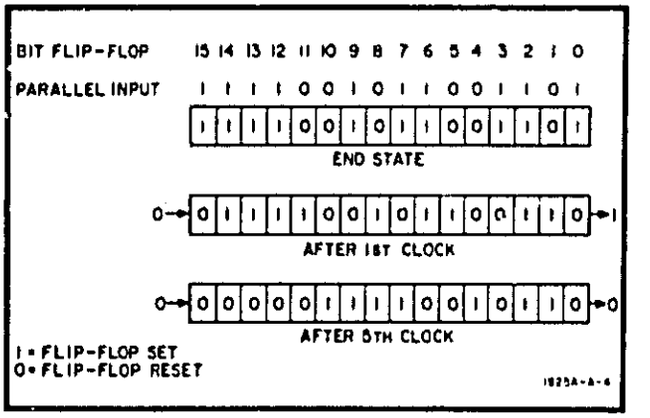


Figure 4-4. Shift Register Operation

c. The configuration of the shift register is such that the first bit of information transferred to the output circuit is that which is stored in flip-flop A2A20 (bit 0). For a 16-bit word, the last bit transferred will be that which is stored in A2A17 (bit 15). If the word length is less than 16 bits, the clock pulse train will contain only the correct number of clock pulses to coincide with the word length.

Note

When a word length is less than 16 bits, all unused bit switches on the front panel must be set to logic 0.

4-33. When the PRN/WORD switch on the front panel is in the WORD position, logic 1 is applied to NOR gate A3A12 (pin 5). This holds the output of A3A12 to logic 0. The output of A3A12 is applied to NOR gate A3A5 (pin 3). The second input to A3A5 (pin 4) is from the SET pushbutton switch on the front panel. The SET switch is required in PRN (Pseudo-Random-Noise) mode of operation and, when not engaged, applies logic 0 to the input of A3A5. NOR gate A3A5 has both a NOR and an OR output. With both inputs at logic 0, the output of A3A5 at pin 5 is logic 1 and the output at pin 6 is logic 0. The two outputs are applied to the $\overline{J}$ input and $\overline{K}$ input of flip-flop A2A17 in the shift register. With logic 1 applied to the $\overline{J}$ input and logic 0 applied to the $\overline{K}$ input, the flip-flop resets on the clock pulse. As the bit information is transferred from the shift register, the flip-flops are sequentially triggered to the reset state. As a result, the shift register is ready to receive new information when the WORD state flip-flop (A3A6) resets.

4-34. The information transferred from the shift register is applied to Exclusive NOR gate A3A11. Refer to Table 4-4 for the truth logic of Exclusive NOR gates.

Table 4-4. Truth Logic for Exclusive NOR Gate

Input A	Input B	Output (+)
0	0	1
0	1	0
1	0	0
1	1	1

4-35. The Exclusive NOR gate is used to generate the WORD output complement. When the $\overline{\text{WORD}}$/WORD switch on the front panel is in the WORD position, logic 1 is applied to pin 4 of A3A11. The serial-bit information from the shift register is applied to pin 6. The information from the shift register is the complement of the bit information stored (output from flip-flop A2A20 is $\overline{Q}$). With logic 1 applied to pin 4, the output of A3A11 (pin 5) is the same as the bit information received from A2A20. The output of A3A11 is applied to NOR gate A1A2 in the output circuit. When the $\overline{\text{WORD}}$/WORD switch is in the $\overline{\text{WORD}}$ position, logic 0 is applied to pin 4 of A3A11. The Exclusive NOR action of A3A11 results in the output word being the complement of the word received from A2A20 (refer to Table 4-4 for truth logic).

4-36. NOR gates A1A1 and A1A2 are used to amplify the bit information from the shift register and gate it to the WORD OUT circuitry. The END output logic from NOR gate A3A9 is applied to one section of A1A2. The complementary output ($\overline{\text{END}}$) of A1A2 is applied to an input on the second section of A1A2. When the WORD state flip-flop (A3A6) is reset, the output of the first section of A1A2 is logic 1. With this signal applied to the second section of A1A2 (pin 12), the output of the second section is held to logic 0. This prevents any bit information from being generated in the output section while the WORD state flip-flop is reset. A second signal which is applied to an input on the second section of A1A2 controls the NRZ/RZ (non-return-to-zero/return-to-zero) mode of operation. When the NRZ/RZ switch on the front panel is in the NRZ position, logic 1 is applied to NOR gate A1A1 (pin 10). The signal is inverted by the NOR action of the gate and applied to A1A2 (pin 10). With logic 0 applied to pin 10 and pin 12 ($\overline{\text{END}}$), the output of the second section of A1A2 is controlled by the input (pin 11) from Exclusive NOR gate A3A11. When consecutive bits of information are present in the shift register, the output of flip-flop A2A20 will remain constant (since its state will not change) during consecutive bit transfer. The signal from Exclusive NOR gate A3A11 will be a constant voltage for consecutive bits of information. With a constant logic 0 applied to pin 10 and pin 12 (A1A2), the non-return-to-zero format results. When the NRZ/RZ switch is in the RZ position, logic 0 is applied to A1A1 (pin 10). With logic 0 applied to one input, the output of A1A1 will be the inverted clock signal which is applied at pin 9. A clock signal is now applied to A1A2 (pin 10). This results in each bit of information being returned to a zero level prior to the next being generated. The outputs of A1A2 (pin 8 and pin 9) are applied to the WORD output drivers. Transistors A1Q14 and A1Q15 have the output of A1A2 applied to their respective bases. Operating differentially they drive output transistors A1Q16 and A1Q17. The WORD output is routed by switch A5S4 to either the interface circuit of the 1900-series mainframe or to the WORD OUT (+) connector J4 on the front panel.

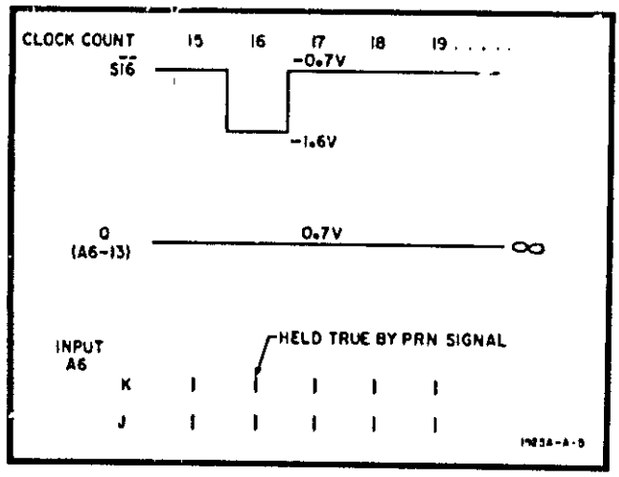


Figure 4-5. Word Control PRN Mode of Operation

4-37. PSEUDO RANDOM NOISE OPERATION.

4-38. In pseudo-random-noise (PRN) mode of operation, the PRN/WORD switch on the front panel applies logic 0 to NOR gate A3A12 (two sections). The WORD state flip-flop (A3A6) is prevented from resetting and the END state remains logic 0 (Figure 4-5). In the PRN mode of operation, a digital feedback circuit is enabled and the shift register is connected into a sequence generator. The feedback circuit samples the Q outputs of flip-flops A2A21 and A2A22. This results in a maximum random sequence of $2^{15}-1$ or 32 767 bits. The sequence properties are such that 1 and 0 occur equally often. After a run of 1's and 0's there is a fifty percent chance the run will end with the next bit (all shift register flip-flops in the reset condition). It is impossible to predict an entire sequence from any partial sequence. The runs of 1's and

0's are useful for investigating duty-cycle problems. In this sequence there are 4096 runs of length one, 2048 runs of length two, 1024 runs of length three, etc., one run of fourteen 0's and one run of fifteen 1's. The sequence will continuously recycle.

4-39. The monitored signals from flip-flop A2A21 and A2A22 are applied to Exclusive NOR gate A3A11 at pin 8 and pin 10. As the random bit information is transferred through the shift register, the output of A3A11 (filtered by resistor A3R2 and capacitor A3C1) is applied to NOR gate A3A12 (pin 4). Since A3A12 is enabled by the PRN/WORD switch on the front panel, its output will be the complement of the Exclusive NOR gate output. The output of A3A12 is applied to pin 3 of NOR gate A3A5. The OR and NOR outputs from A3A5 are applied to the $\overline{J}$ and $\overline{K}$ inputs of flip-flop A2A17 in the shift register, completing the feedback loop.

Note

When all flip-flops in the shift register are in the reset condition, the PRN mode of operation will not start automatically. To initiate the PRN sequence, press the SET pushbutton switch on the front panel.

4-40 EXTERNAL PROGRAMING.

4-41. The Model 1925A can be programed from an external source. The program information is applied through the program connectors on the 1900-series mainframe (Figure 4-6). When operating from an external source, the PGM/NORMAL switch on the front panel of the instrument must be placed in the PGM position. In the

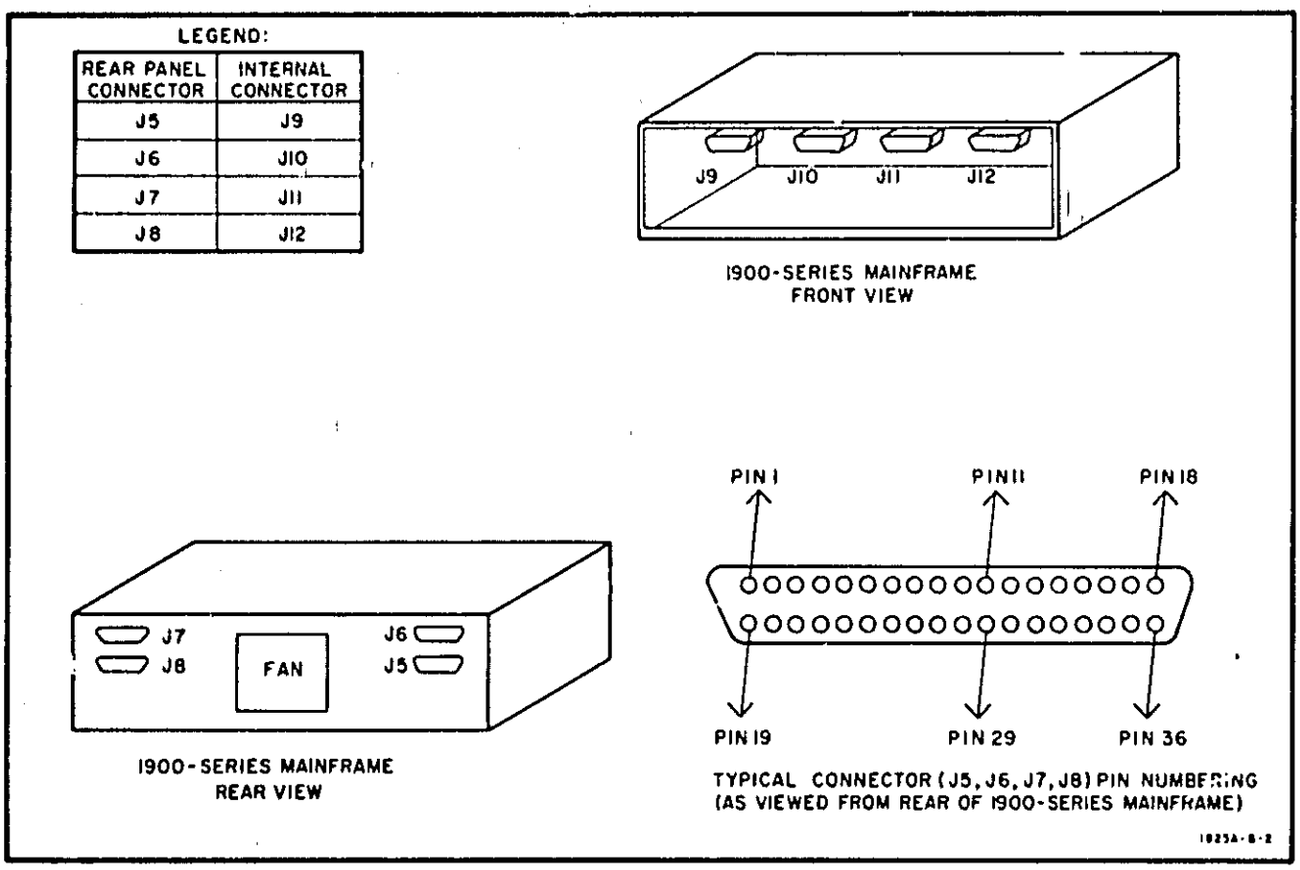


Figure 4-6. 1900-series Mainframe Connectors

PGM position, the control diodes of the front-panel switches are back biased. The only switches that are operational from the front panel in the PGM mode of operation are the CLEAR, SET, MANUAL and WORD/WORD switches. A ground input on any program line results in that function being initiated. See Figure 4-7 for a typical PGM input circuit.

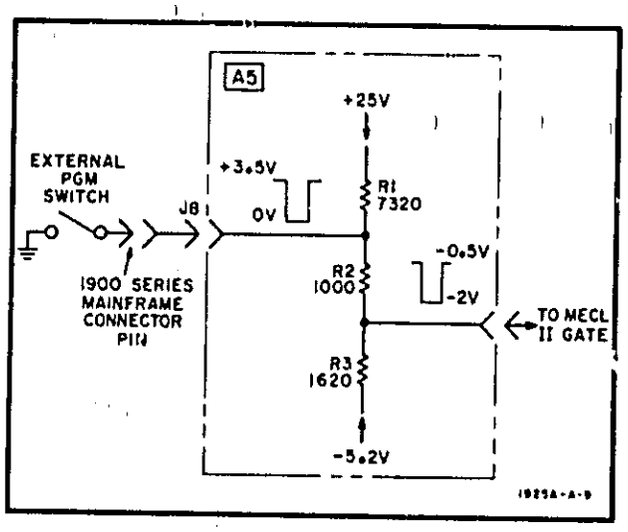


Figure 4-7. Typical PGM Input Circuit

4-42. VOLTAGE REGULATOR.

4-43. The −5.2 volts dc that is required to operate the integrated circuits is furnished by transistor Q1 mounted on the chassis of the Model 1925A. The emitter output of Q1 is monitored by a dual differential amplifier circuit consisting of A1Q18 through A1Q21. Variations in the output of Q1 are sensed by A1Q21. These variations on the base of A1Q21 change the voltage drop across A1R35. Since the voltage on the base of transistor A1Q20 is held constant by breakdown diode A1VR2, the voltage variations across resistor A1R35 are reflected in the collector circuit of A1Q20. The collector of A1Q20 is connected to the base of transistor A1Q18. As the conduction through A1Q18 changes, the voltage drop across the emitter-collector circuit resistors A1R36 and A1R34 also change. This voltage change is applied to the base of transistor A1Q22. Transistor A1Q22 is an emitter-follower and the voltage change reflected in its emitter circuit is applied to the base of Q1. The voltage applied to the base of Q1 controls the −5.2 volts dc used for logic power. A1Q23 is a current-limiting circuit. When the current drain of Q1 increases, the voltage drop across resistor A1R40 increases. This change in voltage (less negative) is applied to the base of A1Q23 and conduction increases. This drain on the current supply limits the current flow in the base-collector circuit of Q1.

Table 5-1. Test Equipment Required

Recommended Instrument		Required Characteristic	Use
Type	Model		
High-frequency Oscilloscope	HP 140A Mainframe HP 1410A Vert Ampl HP 1425A Time Base	Bandwidth: 1 GHz	Performance Check and Troubleshooting
Real-time Oscilloscope	HP 180A Mainframe HP 1801A Vert Ampl HP 1821A Time Base	Bandwidth; 50 MHz	Performance Check and Troubleshooting
HF Signal Generator	HP 606B	Freq Range: 65 MHz	Performance Check
DC Volt-Ohm-Ammeter	HP 412A	Resistance Range: 1 to 10k ohms	Troubleshooting
Mainframe	HP 1900-series	Power Source: ±25V dc; −10 Vdc	Performance Check and Troubleshooting
Rate Generator	Model 1905A	Clock Signal	Performance Check and Troubleshooting
Extender Plug-in	HP 10484A	Extend plug-in units from 1900-series mainframe	Performance Check
50-ohm load (2 Required)	HP 10100A	Output termination	Performance Check and Troubleshooting
50-ohm Tee Connector	No. 1250-0781	BNC Connection	Performance Check and Troubleshooting
Adapter Type GR Female to BNC Male	No. 1250-0850	Non-reactive connector	Performance Check and Troubleshooting
Cables, 50-ohm w/BNC connectors	HP 10503A	Non-reactive connectors	Performance Check and Troubleshooting
Digital Voltmeter	HP 3440A w/ HP 3441A	−10 Vdc	Adjustment
BNC Adapter	HP 10218A	Adapt probe to BNC	Troubleshooting
Filter		0.3 millisecond See Figure 5-5.	Performance Check

SECTION V

PERFORMANCE CHECK AND ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section provides adjustment procedures and a performance check for the Model 1925A. The performance check may be used as an incoming inspection, or after repairs or adjustments have been made, to verify that the instrument meets the specifications listed in Table 1-1. When the initial performance check is made, record the indications on the Performance Check Record. These indications may be used for comparison with equipment performance at a later date.

5-3. REQUIRED TEST EQUIPMENT.

5-4. Test equipment recommended for both the performance check and adjustments is listed in Table 5-1. Similar equipment may be substituted provided it has the required characteristics listed in the table.

5-5. PERFORMANCE CHECK.

5-6. INITIAL CONTROL SETTINGS.

5-7. Before attempting the performance checks, set up the equipment as follows:

a. Set the four interface switches located on the top of Board Assembly A5 to the forward position.

b. Ensure that the four word-length switches on Board Assembly A1 are in the following positions:

A1S1 ..... down
A1S2 ..... down
A1S3 ..... down
A1S4 ..... up

c. Install the Model 1925A in a 1900-series mainframe along side of a Model 1905A Rate Generator using Extender, HP Part No. 10484A.

d. Apply power to the plug-in units.

5-8. WORD PULSE AMPLITUDE.

a. Connect the equipment and accessories as shown in Figure 5-1. Ensure that the outputs of Model 1925A are terminated in 50-ohm loads either at the instrument or at the high-frequency oscilloscope.

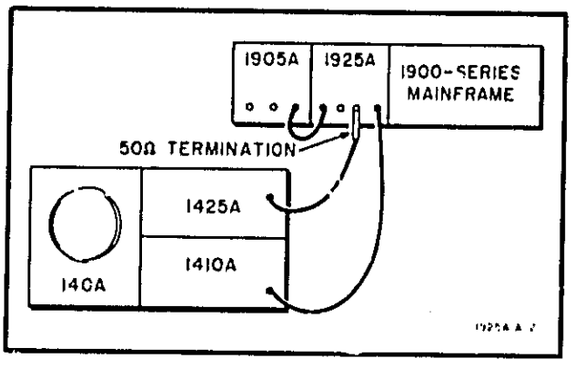


Figure 5-1. Word Pulse Amplitude Test Setup

b. Set the Model 1925A controls as follows:

Bit switch 0, 2, 4 ..... on
All other bit switches ..... off
PGM/NORMAL .....NORMAL
NRZ/RZ ..... RZ
PRN/WORD ..... WORD
$\overline{\text{WORD}}$/WORD ..... WORD
MANUAL/AUTO ..... AUTO

c. Set the Model 1905A controls as follows:

RATE SOURCE ..... INT
RATE Hz ..... 2.5 - 25 MHz
INC ..... 10 MHz
GATED/NORMAL .....NORMAL

d. Set the high-frequency oscilloscope controls as follows:

Sweep Trigger ..... +, external, normal
Time per division ..... 1 microsecond
Sweep Mode ..... normal

e. Measure the amplitude of the bit pulses. They should be +2.0 ±0.5 volts.

f. Check the width of one pulse. The width should be less than 15 nanoseconds.

g. Increase the MAIN SWEEP MAGNIFIER on the oscilloscope until a clear display is presented of the leading edge of one bit pulse. Check the risetime of the pulse. It should be less than 4 nanoseconds between 10% and 90% of the amplitude.

h. Adjust the oscilloscope until a clear display is presented of the trailing edge of one bit pulse. Check the falltime of the pulse. It should be less than 4 nanoseconds between 90% and 10% of the amplitude.

5-9. END PULSE AMPLITUDE.

a. Connect the equipment and accessories as shown in Figure 5-2.

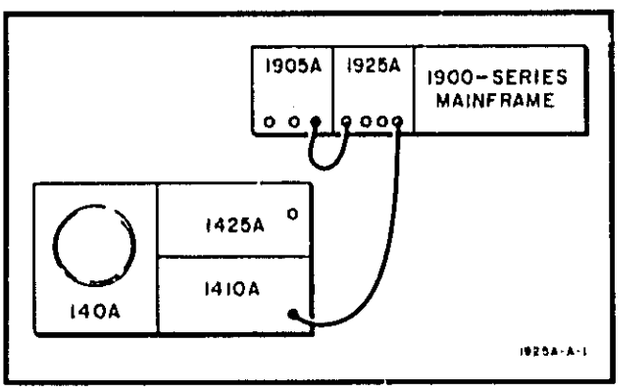


Figure 5-2. End Pulse Amplitude Test Setup

b. Set the Model 1925A front-panel controls as follows:

Bit switches ..... off
PGM/NORMAL ..... NORMAL
NRZ/RZ ..... RZ
PRN/WORD ..... WORD
$\overline{\text{WORD}}$/WORD ..... WORD
MANUAL/AUTO ..... AUTO

c. Set the Model 1905A front-panel controls as follows:

RATE SOURCE ..... INT
RATE Hz ..... 2.5 - 25 MHz
INC ..... 10 MHz
GATED/NORMAL ..... NORMAL

d. Set the high-frequency oscilloscope controls as follows:

Sweep Trigger ..... +, internal, normal
Scanning ..... normal
Sweep ..... main

e. Measure the amplitude of the END pulse. It should be +2.0 ±0.5 volts.

f. Increase the main sweep magnifier on the oscilloscope until a clear display is presented of the leading edge of the END pulse. Check the risetime of the pulse. It should be less than 4 nanoseconds between 10% and 90% of the pulse amplitude.

g. Adjust the high-frequency oscilloscope until a clear display is presented of the trailing edge of the END pulse. The falltime should be less than 4 nanoseconds between 90% and 10% of the pulse amplitude.

5-10. WORD OUTPUT.

a. Connect the equipment and accessories as shown in Figure 5-3.

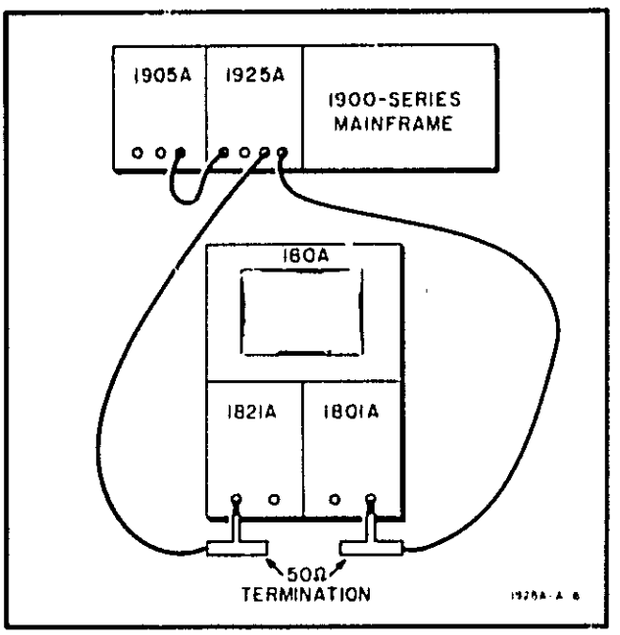


Figure 5-3. Word Output Test Setup

b. Set the Model 1925A controls as follows:

Bit switches ..... off
PGM/NORMAL ..... NORMAL
NRZ/RZ ..... RZ
PRN/WORD ..... WORD
$\overline{\text{WORD}}$/WORD ..... WORD
MANUAL/AUTO ..... AUTO

c. Set the Model 1905A front-panel controls as follows:

RATE SOURCE ..... INT
Rate Hz ..... 2.5 - 25 MHz
INC ..... 10 MHz
GATED/NORMAL ..... NORMAL

d. Set the real-time oscilloscope controls as follows:

Trigger ..... +, external, ac
Volts per cm 0.1
Sweep Mode ..... normal
Time per division ..... 0.2 microsecond

e. Energize each bit-number switch and observe the pulses on the real-time oscilloscope CRT. When all bit switches are energized, a pulse train of 16 bits should be observed.

f. Set all bit-number switches to the off position. Press the SET pushbutton switch on the front panel of the Model 1925A. A 16-bit pulse sequence should be observed.

g. Set the bit-number switches on the Model 1925A to a logic sequence of 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0. Observe the pulse pattern on the real-time oscilloscope CRT.

h. Set the NRZ/RZ switch on the front panel of the Model 1925A to the NRZ position. Observe the pulse pattern on the oscilloscope CRT. Consecutive bit pulses should appear as one pulse.

i. Set the $\overline{\text{WORD}}$/WORD switch on the front panel of the Model 1925A to the $\overline{\text{WORD}}$ position. The pulse pattern should be the complement of the pattern observed in step h above.

5-11. VARIABLE WORD LENGTH.

a. Connect the equipment and accessories as indicated in Figure 5-3.

b. Set the Model 1905A front-panel controls as follows:

RATE SOURCE	INT
RATE Hz	2.5 - 25 MHz
INC	10 MHz
GATED/NORMAL	NORMAL

c. Set the real-time oscilloscope controls as follows:

Trigger	+, external, ac
Sweep Mode	normal
Time per division	0.2 microsecond

d. Set the Model 1925A front-panel controls as follows:

PGM/NORMAL	NORMAL
NRZ/RZ	RZ
PRN/WORD	WORD
$\overline{\text{WORD}}$/WORD	WORD
MANUAL/AUTO	AUTO

e. Set bit-number switch 0 and bit-number switch 8 to the on position. All other bit-number switches should be in the off position.

f. Set the word-length switches on Board Assembly A1 of the Model 1925A to the following positions:

A1S1	up
A1S2	down
A1S3	down
A1S4	down

g. See Figure 5-4 (A). A similar display should be observed on the oscilloscope CRT. The bit-number 0 pulse should follow immediately after the bit-number 8 pulse, indicating a nine-bit word length.

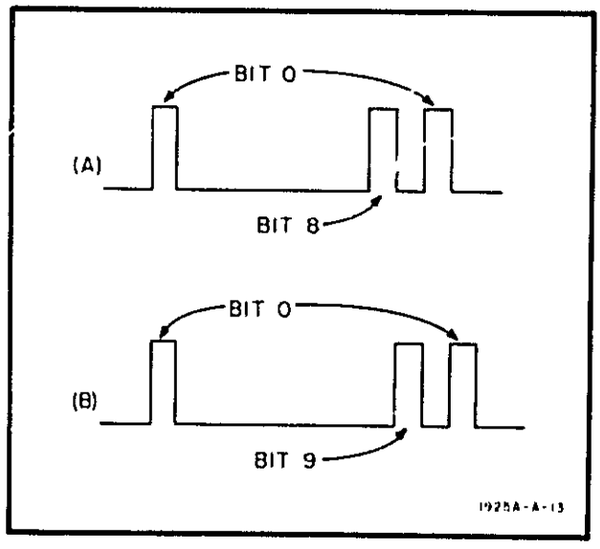


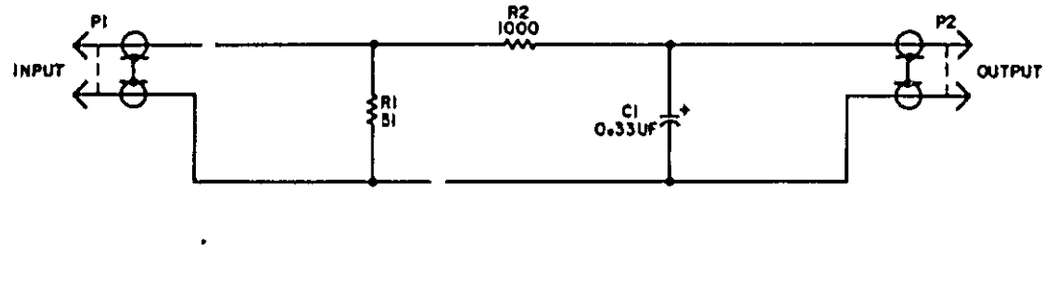
Figure 5-4. Word Length Check

h. Set bit-number switch 0 and bit-number switch 9 to the on position. All other bit-number switches should be in the off position.

i. Set the word-length switches on Board Assembly A1 of the Model 1925A to the following positions:

A1S1	down
A2S2	up
A1S3	up
A1S4	up

j. See Figure 5-4 (B). A similar display should be observed on the oscilloscope CRT. Bit-number 0 pulse should follow immediately after bit-number 9 pulse indicating a ten-bit word length.



Ref Desig	HP Part No.	TQ	Description (See Table 6-1.)
C1	0160-0137	1	C: fxd cer 0.33 uF 20% 25 wVdc
P1	1250-0118	2	Conn: rf Series BNC
P2	1250-0118		Conn: rf Series BNC
R1	0757-0893	1	R: fxd metflm 51 ohms 2% 1/4W
R2	0757-0924	1	R: fxd metflm 1000 ohms 2% 1/4W

Figure 5-5. Test Filter

5-12. PSEUDO RANDOM NOISE CHECK.

a. Construct a 0.3 millisecond filter as shown in Figure 5-5.

b. Connect the equipment and accessories as shown in Figure 5-6.

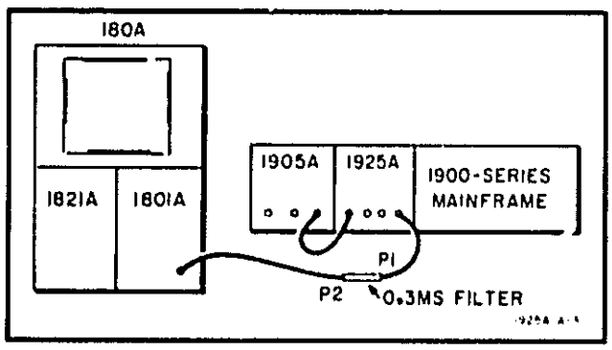


Figure 5-6. PRN Test Setup

c. Set the Model 1905A front-panel controls as follows:

RATE SOURCE ..... INT
RATE Hz ..... 2.5 - 25 MHz
INC ..... 10 MHz
GATED/NORMAL .....NORMAL

d. Set the Model 1925A front-panel controls as follows:

PGM/NORMAL .....NORMAL
NRZ/RZ .....NRZ
PRN/WORD .....PRN
$\overline{\text{WORD}}$/WORD .....WORD
MANUAL/AUTO ..... AUTO

e. Set the real-time oscilloscope controls as follows:

Trigger ..... +, internal, ac
Sweep Mode .....normal
Time per division ..... 1 millisecond
Volts per cm ..... .01

Note

The PRN sequence will cease if all flip-flops in the shift register of the Model 1925A are in the reset state. To start the sequence, press the SET pushbutton switch on the front panel.

f. Observe the waveform on the real-time oscilloscope CRT. It should be comparable to the waveform shown in Figure 5-7.

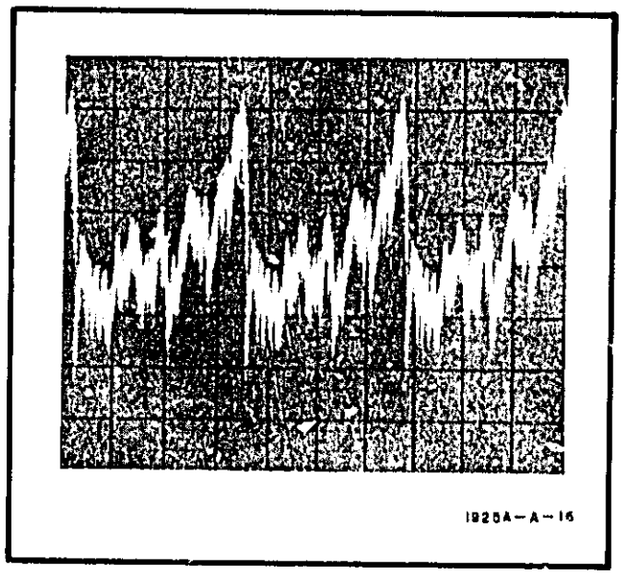


Figure 5-7. PRN Waveform

5-13. FREQUENCY CHECK.

a. Connect the equipment and accessories as shown in Figure 5-8.

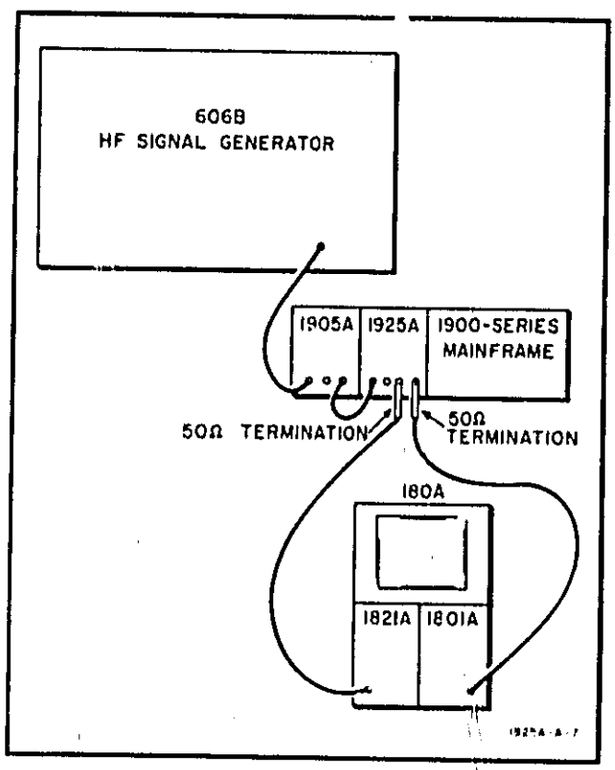


Figure 5-8. Frequency Check Test Setup

b. Set the Model 606B front-panel controls as follows:

RANGE ..... 19-65 MC
ATTENUATOR ..... 3V rms

c. Set the Model 1905A front-panel controls as follows:

RATE SOURCE ..... EXT +
GATED/NORMAL .....NORMAL

d. Set the Model 1925A front-panel controls as follows:

Bit switch logic 1 1 1 0 1 1 1 0 0 0 0 1 1 1 0 1
PGM/NORMAL .....NORMAL
NRZ/RZ .....NRZ
PRN/WORD .....WORD
$\overline{\text{WORD}}$/WORD .....WORD
MANUAL/AUTO ..... AUTO

e. Set the real-time oscilloscope controls as follows:

Trigger ..... +, external, ac
Sweep Mode ..... normal
Volts per cm 5
Time per division ..... .2 microsecond

f. Vary the output frequency of the Model 606B between 19 MHz and 50 MHz. The pattern displayed on the real-time oscilloscope CRT should be independent of the repetition rate. If the pattern changes, adjust the clock-bias potentiometer A1R17 for a correct pattern.

5-14. PGM CHECK.

a. Set the equipment and accessories as indicated in Figure 5-9.

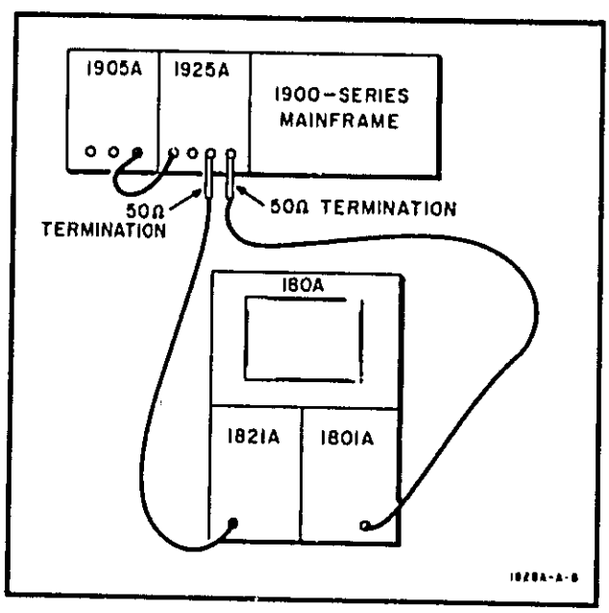


Figure 5-9. PGM Check Test Setup

b. Set the Model 1905A controls as follows:

RATE SOURCE . . . . . INT
RATE Hz . . . . . 2.5 - 25 MHz
INC . . . . . 10 MHz
GATED/NORMAL . . . . . .NORMAL

c. Set the real-time oscilloscope controls as follows:

Trigger . . . . . +, external, ac
Sweep Mode . . . . . normal

d. Set the Model 1925A front-panel controls as follows:

PGM/NORMAL . . . . . .PGM
$\overline{\text{WORD}}$/WORD . . . . . .WORD

e. Refer to Table 5-2 for input programing and the function that is initiated. Using the table, check out the PGM circuitry.

5-15. ADJUSTMENTS.

5-16. The only adjustment in the Model 1925A is the clock bias adjustment. The normal voltage at Test Point 3 on Board Assembly A1 is −1.8 volts. This voltage will vary slightly between instruments after adjustments are made for maximum frequency operation. Refer to Paragraph 5-13 f.

Performance Check Record
Serial Number_____

Paragraph Reference	Check	Reference Standard	
		Required	Actual
5-8e	Pulse Amplitude	+2.0 Vdc ± 0.5 Vdc	
5-8f	RZ Pulse Width	< 15 ns	
5-8g	WORD Pulse Risetime	< 4 ns (10% to 90% pulse amplitude)	
5-8h	WORD Pulse Falltime	< 4 ns (90% to 10% pulse amplitude)	
5-9e	END Pulse Amplitude	+2.0 Vdc ± 0.5 Vdc	
5-9f	END Pulse Risetime	< 4 ns (10% to 90% pulse amplitude)	
5-9g	END Pulse Falltime	< 4 ns (90% to 10% pulse amplitude)	
5-10e	Bit Pulses	16	
5-10h	NR2/RZ Output	In NRZ mode, consecutive bits are not returned to zero voltage level.	
5-10i	$\overline{\text{WORD}}$ Output	Complement of 5-10h above.	
5-11g,j	Variable WORD Length	Last bit of word length should be followed by bit number 0.	
5-12f	PRN	Waveform of Figure 5-9.	
5-13f	Frequency Check	Stable pattern with variable input frequency to 50 MHz.	
5-14e	PGM Check	Perform PGM functions with proper inputs.	

CUT ALONG DOTTED LINE

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering replacement parts. Table 6-2 lists the parts in alphanumeric order by reference designation. All chassis-mounted parts (assemblies and parts not mounted on assemblies) appear first, followed by each assembly with sub-assemblies (if any) and components mounted on that assembly. Reference designations for groups of identical items may be shown as TP1 - TP9 followed by a single part number and description indicating that TP1 through TP9 are separate but identical parts.

6-3. Parts consisting of several smaller, yet separately replaceable parts such as jacks or relays have all sub-parts listed so that partial replacement of these items can be accomplished. Miscellaneous parts which are not assigned reference designations appear at the end of the chassis parts listing and at the end of each assembly listing.

6-4. ORDERING INFORMATION.

6-5. Many parts used in Hewlett-Packard equipment are manufactured by HP or are selected by HP under specifications more rigid than the manufacturer's standard specifications. These parts may be ordered directly from Hewlett-Packard Company. Information concerning standard replaceable parts will be supplied upon request to allow procurement directly from the manufacturers. Contact the local HP Sales/Service Office for details.

6-6. To obtain replacement parts from HP, address order or inquiry to the nearest Hewlett-Packard Sales/Service Office (names and addresses in rear of manual), and supply the following information:

a. HP part number of item(s).

b. Model number and eight-digit serial number of instrument.

c. Quantity of part(s) desired.

6-7. To order a part not listed in the table, provide the following information:

a. Model number and eight-digit serial number of the instrument.

b. Description of the part including function and location in the instrument.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	E	= misc. electronic part	M	= meter	TB	= terminal board
AT	= attenuator, resistive termination	F	= fuse	MP	= mechanical part	TP	= test point
B	= motor, fan	FL	= filter	P	= plug	U	= microcircuit(non-repairable)
C	= capacitor	H	= hardware	PS	= power supply	V	= vacuum tube, neon bulb, photocell, etc.
CP	= coupling	IC	= integrated circuit	Q	= transistor		
CR	= diode	J	= jack	R	= resistor	VR	= voltage regulator (diode)
DL	= delay line	K	= relay	RT	= thermistor	W	= cable
DS	= device signaling (lamp)	L	= inductor	S	= switch	X	= socket
		LS	= speaker	T	= transformer	Y	= crystal

ABBREVIATIONS

A	= ampere(s)	Ge	= germanium	mmat	= miniature	s-b	= slow-blow
ampl	= amplifier(s)	G	= giga (10^9)	mom.	= momentary	Se	= selenium
assy	= assembly	gl	= glass	mtg	= mounting	sect	= section(s)
		gnd	= ground(ed)	my.	= mylar	semicon	= semiconductor(s)
bd	= board(s)					Si	= silicon
bp	= bandpass	H	= henry(ies)	n	= nano (10^{-9})	sil	= silver
		Hg	= mercury	n/c	= normally closed	sl	= slide
c	= centi (10^{-2})	hr	= hour(s)	Ne	= neon	sp	= single pole
car.	= carbon	HP	= Hewlett-Packard	n/o	= normally open	spl	= special
ccw	= counterclockwise	Hz	= hertz	npo	= negative-positive-zero (zero temperature coefficient)	st	= single throw
cer	= ceramic					std	= standard
coax.	= coaxial	IF	= intermediate freq				
coef	= coefficient	impg	= impregnated	nsr	= not separately replaceable	Ta	= tantalum
com	= common	incd	= incandescent			td	= time delay
comp	= composition	incl	= include(s)			TD	= tunnel diode(s)
conn	= connector(s)	ins	= insulation(ed)	obd	= order by description	tgl	= toggle
CRT	= cathode-ray tube	int	= internal	ox	= oxide	Ti	= titanium
cw	= clockwise					tol	= tolerance
d	= deci (10^{-1})	k	= kilo (10^3)	p	= pico (10^{-12})	trmr	= trimmer
depc	= deposited carbon			pc	= printed (etched) circuit(s)		
dp	= double pole	lb	= pound(s)	PGM	= program	u	= micro (10^{-6})
dt	= double throw	lev	= lever	piv	= peak inverse voltage(s)		
		lin	= linear taper	p/o	= part of	V	= volt(s)
elect.	= electrolytic	log.	= logarithmic taper	poly	= polystyrene	var	= variable
encap	= encapsulated	lpf	= low-pass filter(s)	pore	= porcelain		
ext	= external			pos	= position(s)	W	= watt(s)
		m	= milli (10^{-3})	pot.	= potentiometer(s)	w/	= with
F	= farad(s)	M	= mega (10^6)	pk-pk	= peak-to-peak	w/o	= without
fet	= field-effect transistor(s)	metflm	= metal film	rect	= rectifier(s)	wVdc	= dc working volt(s)
fxd	= fixed	metox	= metal oxide	rf	= radio frequency	ww	= wirewound

Table 6-2. Replaceable Parts

Ref Desig	HP Part No.	TQ	Description (See Table 6-1.)
			CHASSIS
J1-J4	1250-0083	4	Conn: BNC, bulkhead mtg jack
P2	1251-0483	1	Conn: PGM 36 pin
Q1	1850-0098	1	Q: Ge pnp 2N1136
			MISCELLANEOUS
E1	1200-0043	1	E: Insulator, transistor mtg
H1	0590-0836	24	H: Nut, switch
L1	9170-0058	2	L: Core, ferrite
MP1	1390-0160	1	MP: Fastner, panel assembly
MP2	01925-01101	1	MP: Heat sink
MP3	01900-60503	1	MP: Gusset, right assembly
MP4	01900-60504	1	MP: Gusset, left assembly
W1	01901-61604	1	W: Cable assembly, Coaxial, Clock (short)
W2	01925-61603	1	W: Cable assembly, Coaxial, WORD OUT (+)
W3	01925-61604	1	W: Cable assembly, Coaxial, END OUT (+)
W4	01925-61605	1	W: Cable assembly, Coaxial, START IN (+)
W5	01925-61606	1	W: Cable assembly, Coaxial, CLOCK IN (+)
W6	01925-61607	1	W: Cable assembly, Coaxial, Clock (long)
W7	01925-61601	1	W: Cable assembly, main
W8	01925-61602	1	W: Cable assembly, PGM
			A1
A1	01925-66501	1	A: Board Assembly, Drivers
A1	1820-0145	11	IC: ECL Quad NOR Motorola MC 1010P
A2	1820-0142	2	IC: ECL Dual OR/NOR Motorola MC1004P
C1	0160-3443	1	C: fxd 0.1 uF 50 wVdc
C2	0180-2203	10	C: fxd Ta 1 uF 20% 35 wVdc
C3	0180-2203		C: fxd Ta 1 uF 20% 35 wVdc
C4	0160-2204	1	C: fxd mica 100 pF 5% 300 wVdc
C5	0150-0115	2	C: fxd cer 27 pF 10% 500 wVdc
C6	0180-2203		C: fxd Ta 1 uF 20% 35 wVdc
C7	0160-2261	1	C: fxd cer 15 pF 5% 500 wVdc
C8	0180-2204	2	C: fxd Ta 10 uF 20% 10 wVdc
C9	0180-2204		C: fxd Ta 10 uF 20% 10 wVdc
C10	0150-0093	6	C: fxd cer .01 uF +80–20% 100 wVdc

Table 6-2. Replaceable Parts (Cont'd)

Ref Desig	HP Part No.	TQ	Description (See Table 6-1.)
A1 (cont'd)			
C11	0150-0093		C: fxd cer .01 uF +80–20% 100 wVdc
C12	0150-0093		C: fxd cer .01 uF +80–20% 100 wVdc
C13	0180-2203		C: fxd Ta 1 uF 20% 35 wVdc
C14	0180-2203		C: fxd Ta 1 uF 20% 35 wVdc
C15	0180-2203		C: fxd Ta 1 uF 20% 35 wVdc
CR1	1901-0538	2	CR: dual MSD 6150
CR2	1901-0040	2	CR: Si
CR3	1901-0538		CR: dual MSD 6150
CR4	1901-0040		CR: Si
L1	9100-2258	4	L: fxd 1.20 uH 10%
L2	9100-2258		L: fxd 1.20 uH 10%
L3	9100-2258		L: fxd 1.20 uH 10%
Q1	1853-0011	1	Q: Si pnp 2N2894
Q2	1854-0019	3	Q: Si npn 2N2369
Q3	1853-0015	4	Q: Si pnp 2N3640
Q4	1853-0015		Q: Si pnp 2N3640
Q5	1853-0015		Q: Si pnp 2N3640
Q6	1853-0015		Q: Si pnp 2N3640
Q7	1853-0036	2	Q: Si pnp 2N3906
Q8	1854-0019		Q: Si npn 2N2369
Q9	1854-0019		Q: Si npn 2N2369
Q10	1853-0203	4	Q: Si pnp
Q11	1853-0203		Q: Si pnp
Q12	1854-0092	4	Q: Si npn 2N3563
Q13	1854-0092		Q: Si npn 2N3563
Q14	1854-0092		Q: Si npn 2N3563
Q15	1854-0092		Q: Si npn 2N3563
Q16	1853-0203		Q: Si pnp
Q17	1853-0203		Q: Si pnp
Q18	1854-0071	3	Q: Si npn
Q19	1854-0071		Q: Si npn
Q20	1853-0020	2	Q: Si pnp 2N3702
Q21	1853-0020		Q: Si pnp 2N3702
Q22	1853-0010	1	Q: Si pnp 2N3251
Q23	1854-0071		Q: Si npn
Q24	1853-0036		Q: Si pnp 2N3906
R1	0757-0893	2	R: fxd metflm 51 ohms 2% 1/8W
R2	0757-0898	1	R: fxd metox 82 ohms 2% 1/4W
R3	0757-0078	2	R: fxd metox 2200 ohms 2% 1/2W
R4	0758-0042	1	R: fxd metflm 1300 ohms 5% 1/4W
R5	0757-0934	1	R: fxd metox 2700 ohms 2% 1/4W

Table 6-2. Replaceable Parts (Con 'd)

Ref Desig	HP Part No.	TQ	Description (See Table 6-1.)
A1 (cont'd)			
R6	0757-0901	1	R: fxd metox 110 ohms 2% 1/4W
R7	0757-0926	2	R: fxd metox 1200 ohms 2% 1/4W
R8	0757-0078		R: fxd metox 2200 ohms 2% 1/2W
R9	0757-0893		R: fxd metflm 51 ohms 2% 1/8W
R10	0757-0916	1	R: fxd metox 470 ohms 2% 1/4W
R11	0698-7029	2	R: fxd metflm 39 ohms 2% 1/8W
R12	0698-7029		R: fxd metflm 39 ohms 2% 1/8W
R13	0757-0904	1	R: fxd metox 150 ohms 2% 1/4W
R14	0757-0919	2	R: fxd metox 620 ohms 2% 1/4W
R15	0684-1061	1	R: fxd car 10 megohms 10% 1/4W
R16	0757-0919		R: fxd metox 620 ohms 2% 1/4W
R17	2100-2632	1	R: var, comp 100 ohms 30% 1/2W
R18	0757-0910	1	R: fxd metox 270 ohms 2% 1/8W
R19	0684-1221	4	R: fxd car 1200 ohms 10% 1/4W
R20	0684-1221		R: fxd car 1200 ohms 10% 1/4W
R21	0684-1221		R: fxd car 1200 ohms 10% 1/4W
R22	0684-1221		R: fxd car 1200 ohms 10% 1/4W
R23	0761-0057	1	R: fxd metox 560 ohms 5% 1/4W
R24	0757-0902	4	R: fxd metox 120 ohms 2% 1/4W
R25	0757-0915	2	R: fxd metox 430 ohms 2% 1/4W
R26	0761-0008	2	R: fxd metox 510 ohms 5% 1W
R27	0757-0902		R: fxd metox 120 ohms 2% 1/4W
R28	0757-0902		R: fxd metox 120 ohms 2% 1/4W
R29	0757-0915		R: fxd metox 430 ohms 2% 1/4W
R30	0761-0008		R: fxd metox 510 ohms 5% 1W
R31	0757-0902		R: fxd metox 120 ohms 2% 1/4W
R32	0758-0003	1	R: fxd metflm 1000 ohms 5% 1/4W
R33	0757-0951	2	R: fxd metox 13k ohms 2% 1/4W
R34	0757-0931	3	R: fxd metox 2000 ohms 2% 1/4W
R35	0757-0932	1	R: fxd metox 2200 ohms 2% 1/4W
R36	0757-0931		R: fxd metox 2000 ohms 2% 1/4W
R37	0757-0931		R: fxd metox 2000 ohms 2% 1/4W
R38	0757-0951		R: fxd metox 13k ohms 2% 1/4W
R39	0757-0900	2	R: fxd metox 100 ohms 2% 1/4W
R40	0811-1553	1	R: fxd ww .68 ohm 5% 2W
R41	0698-6746	1	R: fxd metflm 43 ohms 5% 1/8W
R42	0757-0913	1	R: fxd metox 360 ohms 2% 1/8W
R43	0757-0895	1	R: fxd metox 62 ohms 2% 1/8W

Table 6-2. Replaceable Parts (Cont'd)

Ref Desig	HP Part No.	TQ	Description (See Table 6-1.)
A1 (cont'd)			
S1	3101-0973	4	S: slide dpdt
S2	3101-0973		S: slide dpdt
S3	3101-0973		S: slide dpdt
S4	3101-0973		S: slide dpdt
VR1	1902-3048	1	VR: breakdown 3.48V 5% 400 mW
VR2	1902-3097	1	VR: breakdown 5.23V 2% 400 mW
			A2
A2	01925-66502	1	A: Board Assembly Shift Register
A1	1820-0145		IC: ECL Quad NOR Motorola MC1010P
A2	1820-0102	21	IC: J-K flip-flop Motorola MC1013P
A3	1820-0102		IC: J-K flip-flop Motorola MC1013P
A4	1820-0102		IC: J-K flip-flop Motorola MC1013P
A5	1820-0102		IC: J-K flip-flop Motorola MC1013P
A6	1820-0157	3	IC: ECL Clock Driver Motorola MC1023P
A7	1820-0145		IC: ECL Quad NOR Motorola MC1010P
A8	1820-0102		IC: J-K flip-flop Motorola MC1013P
A9	1820-0102		IC: J-K flip-flop Motorola MC1013P
A10	1820-0102		IC: J-K flip-flop Motorola MC1013P
A11	1820-0102		IC: J-K flip-flop Motorola MC1013P
A12	1820-0145		IC: ECL Quad NOR Motorola MC1010P
A13	1820-0145		IC: ECL Quad NOR Motorola MC1010P
A14	1820-0102		IC: J-K flip-flop Motorola MC1013P
A15	1820-0102		IC: J-K flip-flop Motorola MC1013P
A16	1820-0102		IC: J-K flip-flop Motorola MC1013P
A17	1820-0102		IC: J-K flip-flop Motorola MC1013P
A18	1820-0157		IC: ECL Clock Driver Motorola MC1023P
A19	1820-0145		IC: ECL Quad NOR Motorola MC1010P
A20	1820-0102		IC: J-K flip-flop Motorola MC1013P
A21	1820-0102		IC: J-K flip-flop Motorola MC1013P
A22	1820-0102		IC: J-K flip-flop Motorola MC1013P
A23	1820-0102		IC: J-K flip-flop Motorola MC1013P
A24	1820-0145		IC: ECL Quad NOR Motorola MC1010P
C1	0150-0093		C: fxd cer .01 uF +80–20% 100 wVdc
C2	0160-3470	1	C: fxd cer .02 uF 50 wVdc
C3	0180-2203		C: fxd Ta 1 uF 20% 35 wVdc
L1	01925-82701	1	L: filter
R1	0698-7482	5	R: fxd car 1200 ohms 10% 1/8W
R2	0698-7482		R: fxd car 1200 ohms 10% 1/8W
R3	0698-7482		R: fxd car 1200 ohms 10% 1/8W
R4	0698-7482		R: fxd car 1200 ohms 10% 1/8W
R5	0698-5075	4	R: fxd car 130 ohms 10% 1/8W

Table 6-2. Replaceable Parts (Cont'd)

Ref Desig	HP Part No.	TQ	Description (See Table 6-1.)
A2 (cont'd)			
R6	0698-7483	4	R: fxd car 82 ohms 10% 1/8W
R7	0698-5075		R: fxd car 130 ohms 10% 1/8W
R8	0698-7483		R: fxd car 82 ohms 10% 1/8W
R9	0698-5075		R: fxd car 130 ohms 10% 1/8W
R10	0698-7483		R: fxd car 82 ohms 10% 1/8W
R11	0698-5075		R: fxd car 130 ohms 10% 1/8W
R12	0698-7483		R: fxd car 82 ohms 10% 1/8W
			A3
A3	01925-66503	1	A: Board Assembly Counter
A1	1820-0102		IC: J-K flip-flop Motorola MC1013P
A2	1820-0102		IC: J-K flip-flop Motorola MC1013P
A3	1820-0102		IC: J-K flip-flop Motorola MC1013P
A4	1820-0102		IC: J-K flip-flop Motorola MC1013P
A5	1820-0142		IC: ECL Dual OR/NOR Motorola MC1004P
A6	1820-0102		IC: J-K flip-flop Motorola MC1013P
A7			Not used
A8	1820-0145		IC: ECL Quad NOR Motorola MC1010P
A9	1820-0145		IC: ECL Quad NOR Motorola MC1010P
A10	1820-0157		IC: ECL Clock Driver Motorola MC1023P
A11	1820-0235	1	IC: Quad Exclusive OR Motorola MC1031P
A12	1820-0145		IC: ECL Quad NOR Motorola MC1010P
C1	0150-0115		C: fxd cer 27 pF 10% 500 wVdc
C2	0180-2203		C: fxd Ta 1 uF 20% 35 wVdc
C3	0150-0093		C: fxd cer .01 uF +80–20% 100 wVdc
C4	0150-0093		C: fxd cer .01 uF +80–20% 100 wVdc
L1	9100-2258		L: fxd 1.20 uH 10%
R1	0757-0926		R: fxd car 1200 ohms 10% 1/8W
R2	0757-0900		R: fxd metox 100 ohms 5% 1/4W
			A4
A4	01925-66505	1	A: Board Assembly Front Panel
CR1-CR38	1901-0040	38	CR: Si
S1	3101-1220	1	S: toggle, dpdt
S2-S17	3101-1219	20	S: toggle, spdt
S18-S19	3101-1221	3	S: push, momentary spdt
S20-S23	3101-1219		S: toggle, spdt
S24	3101-1221		S: push, momentary spdt

Table 6-2. Replaceable Parts (Cont'd)

Ref Desig	HP Part No.	TQ	Description (See Table 6-1.)
			A5
A5	01925-66504		A: Board Assembly, Interconnect
C1	0180-2203		C: fxd Ta 1 uF 20% 35 wVdc
C2	0180-2203		C: fxd Ta 1 uF 20% 35 wVdc
J1-J4	1250-1042	4	J: min rf, pc board
J5-J7	1251-1887	3	J: conn, 44 pin
P1	1251-2090	1	P: conn, pc 15 pin
R1	0698-3518	20	R: fxd metflm 7320 ohms 1% 1/8W
R2	0757-0280	20	R: fxd metflm 1000 ohms 1% 1/8W
R3	0757-0428	20	R: fxd metflm 1620 ohms 1% 1/8W
R4	0698-3518		R: fxd metflm 7320 ohms 1% 1/8W
R5	0757-0280		R: fxd metflm 1000 ohms 1% 1/8W
R6	0757-0428		R: fxd metflm 1620 ohms 1% 1/8W
R7	0698-3518		R: fxd metflm 7320 ohms 1% 1/8W
R8	0757-0280		R: fxd metflm 1000 ohms 1% 1/8W
R9	0757-0428		R: fxd metflm 1620 ohms 1% 1/8W
R10	0698-3518		R: fxd metflm 7320 ohms 1% 1/8W
R11	0757-0280		R: fxd metflm 1000 ohms 1% 1/8W
R12	0757-0428		R: fxd metflm 1620 ohms 1% 1/8W
R13	0698-3518		R: fxd metflm 7320 ohms 1% 1/8W
R14	0757-0280		R: fxd metflm 1000 ohms 1% 1/8W
R15	0757-0428		R: fxd metflm 1620 ohms 1% 1/8W
R16	0698-3518		R: fxd metflm 7320 ohms 1% 1/8W
R17	0757-0280		R: fxd metflm 1000 ohms 1% 1/8W
R18	0757-0428		R: fxd metflm 1620 ohms 1% 1/8W
R19	0698-3518		R: fxd metflm 7320 ohms 1% 1/8W
R20	0757-0280		R: fxd metflm 1000 ohms 1% 1/8W
R21	0757-0428		R: fxd metflm 1620 ohms 1% 1/8W
R22	0698-3518		R: fxd metflm 7320 ohms 1% 1/8W
R23	0757-0280		R: fxd metflm 1000 ohms 1% 1/8W
R24	0757-0428		R: fxd metflm 1620 ohms 1% 1/8W
R25	0698-3518		R: fxd metflm 7320 ohms 1% 1/8W
R26	0757-0280		R: fxd metflm 1000 ohms 1% 1/8W
R27	0757-0428		R: fxd metflm 1620 ohms 1% 1/8W
R28	0698-3518		R: fxd metflm 7320 ohms 1% 1/8W
R29	0757-0280		R: fxd metflm 1000 ohms 1% 1/8W
R30	0757-0428		R: fxd metflm 1620 ohms 1% 1/8W

Table 6-2. Replaceable Parts (Cont'd)

Ref Desig	HP Part No.	TQ	Description (See Table 6-1.)
A5 (cont'd)			
R31	0698-3518		R: fxd metflm 7320 ohms 1% 1/8W
R32	0757-0280		R: fxd metflm 1000 ohms 1% 1/8W
R33	0757-0428		R: fxd metflm 1620 ohms 1% 1/8W
R34	0698-3518		R: fxd metflm 7320 ohms 1% 1/8W
R35	0757-0280		R: fxd metflm 1000 ohms 1% 1/8W
R36	0757-0428		R: fxd metflm 1620 ohms 1% 1/8W
R37	0698-3518		R: fxd metflm 7320 ohms 1% 1/8W
R38	0757-0280		R: fxd metflm 1000 ohms 1% 1/8W
R39	0757-0428		R: fxd metflm 1620 ohms 1% 1/8W
R40	0698-3518		R: fxd metflm 7320 ohms 1% 1/8W
R41	0757-0280		R: fxd metflm 1000 ohms 1% 1/8W
R42	0757-0428		R: fxd metflm 1620 ohms 1% 1/8W
R43	0698-3518		R: fxd metflm 7320 ohms 1% 1/8W
R44	0757-0280		R: fxd metflm 1000 ohms 1% 1/8W
R45	0757-0428		R: fxd metflm 1620 ohms 1% 1/8W
R46	0698-3518		R: fxd metflm 7320 ohms 1% 1/8W
R47	0757-0280		R: fxd metflm 1000 ohms 1% 1/8W
R48	0757-0428		R: fxd metflm 1620 ohms 1% 1/8W
R49	0698-3518		R: fxd metflm 7320 ohms 1% 1/8W
R50	0757-0280		R: fxd metflm 1000 ohms 1% 1/8W
R51	0757-0428		R: fxd metflm 1620 ohms 1% 1/8W
R52	0698-3518		R: fxd metflm 7320 ohms 1% 1/8W
R53	0757-0280		R: fxd metflm 1000 ohms 1% 1/8W
R54	0757-0428		R: fxd metflm 1620 ohms 1% 1/8W
R55	0698-3518		R: fxd metflm 7320 ohms 1% 1/8W
R56	0757-0280		R: fxd metflm 1000 ohms 1% 1/8W
R57	0757-0428		R: fxd metflm 1620 ohms 1% 1/8W
R58	0757-0924	3	R: fxd metflm 1000 ohms 2% 1/8W
R59	0757-0924		R: fxd metflm 1000 ohms 2% 1/8W
R60	0757-0924		R: fxd metflm 1000 ohms 2% 1/8W
R61	0757-0912	1	R: fxd metflm 330 ohms 2% 1/8W
R62	0698-3518		R: spare
R63	0757-0280		R: spare
R64	0757-0428		R: spare
S1-S4	3101-0973	4	S: slide dpdt

SECTION VII

MANUAL CHANGES AND OPTIONS

7-1. MANUAL CHANGES.

7-2. This manual applies directly to the standard Model 1925A Word Generator having a serial prefix as listed on the title page of this manual. The following paragraphs provide instructions for modifying the manual to cover older instruments. Refer to the separate MANUAL CHANGES sheet supplied with this manual for newer instruments a errata.

7-3. OLDER INSTRUMENTS.

7-4. Table 7-1 lists the changes required to adapt this manual to an older instrument. Check Table 7-1 for the proper instrument serial prefix and make the changes indicated. Note that these changes adapt the manual to cover a particular instrument as manufactured and do not apply to an instrument subsequently modified in the field.

7-5. OPTIONS.

7-6. Options for an HP instrument are standard modifications installed at the factory. At the present time, no options are offered for the Model 1925A.

7-7. SPECIAL INSTRUMENTS.

7-8. Modified versions (per customer's specifications) of any HP instrument are available on special order. The manual for these special instruments (having electrical modifications) will include a separate insert sheet that describes the modification and any special manual changes in addition to the MANUAL CHANGES sheet (if applicable). Contact the nearest HP Sales/Service Office if either of these sheets is missing from the manual of a special instrument. Be sure to refer to the instrument by its full specification name and number.

Table 7-1. Manual Changes

Serial Prefix	Make Changes
No backdating changes are applicable at this time.	

Table 8-1. Schematic Notes

Refer to MIL-STD-15-1A for schematic symbols not list. this table.

= Etched circuit board

= Front-panel marking

= Rear-panel marking

= Front-panel control

= Screwdriver adjustment

P/O = Part of

CW = Clockwise end of variable resistor

N C = No connection

= Waveform test point (with number)

= Common electrical point (with letter) not necessarily ground

= Single pin connector on board

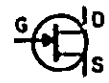
= Pin of a plug-in board (with letter or number)

= Main signal path

= Primary feedback path

= Secondary feedback path

* = Optimum value selected at factory, average value shown; part may have been omitted.



= Field-effect transistor (N-channel)

= Breakdown diode

= Tunnel diode

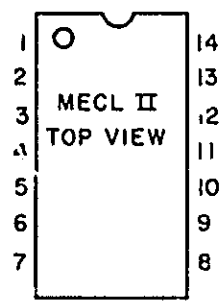
= Step-recovery diode

= Circuits or components drawn with dashed lines (phantom) show function only and are not intended to be complete. The circuit or component is shown in detail on another schematic.

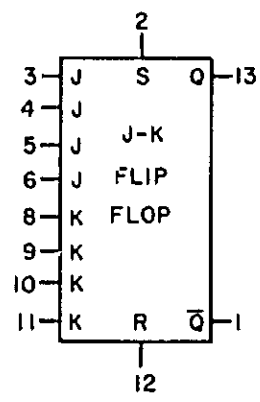
Unless otherwise indicated:
resistance in ohms
capacitance in picofarads
inductance in microhenries

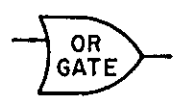
Wire colors are given by numbers in parentheses using the resistor color code [(925) is wht-red-grn].

0 - Black	5 - Green
1 - Brown	6 - Blue
2 - Red	7 - Violet
3 - Orange	8 - Gray
4 - Yellow	9 - White

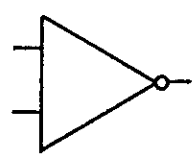


PIN CONNECTION





INVERTER
AMPLIFIER



SECTION VIII

SCHEMATICS AND TROUBLESHOOTING

8-1. INTRODUCTION.

8-2. This section contains schematics, repair and replacement information, component identification illustrations and troubleshooting tips. Table 8-1 defines symbols and conventions used on the schematics.

8-3. REFERENCE DESIGNATIONS.

8-4. The unit system of reference designations used in this manual is in accordance with provisions of the USA Standard Reference Designations for Electrical and Electronics Parts and Equipment, dated March, 1968. Minor variations due to design and manufacturing practices not specifically covered by the standard may be noted.

8-5. Each electrical component is identified by a class letter and number. This letter-number combination is the basic designation for each component. Components which are separately replaceable and are part of an assembly have, in addition to the basic designation, a prefix designation indicating the assembly on which the component is physically located. Components not located on an assembly will have only the basic designation and are listed in the replaceable parts list (Section VI) under Chassis Parts.

8-6. All components within the shaded area on the schematics are physically located on etched circuit boards and should be prefixed with the assembly number assigned to the particular board (e.g. resistor R23 on assembly A2 is referred to as A2R23). There may also be an R23 on several other assemblies but the assembly designation will always be different (A3R23, A9R23, etc.).

8-7. PLUG-IN CIRCUIT BOARDS.

8-8. The following paragraphs provide information regarding component identification, board removal, pin numbering systems, use of heat sinks, and special soldering considerations.

8-9. BOARD CONNECTIONS.

8-10. Circuit connections to the plug-in boards are of four general types: direct wire, coaxial cables to snap-on jacks, coaxial cable soldered directly to the board, and from the pins at the bottom of the board to the jack on the main chassis. The pins are not identified on the circuit board, but the connections on the mating jack are coded with either a number or a letter. To avoid confusion with the wire color-coding number, the wire color code is enclosed in parenthesis. Figure 8-1 shows the four types of board connections used in the Model 1925A.

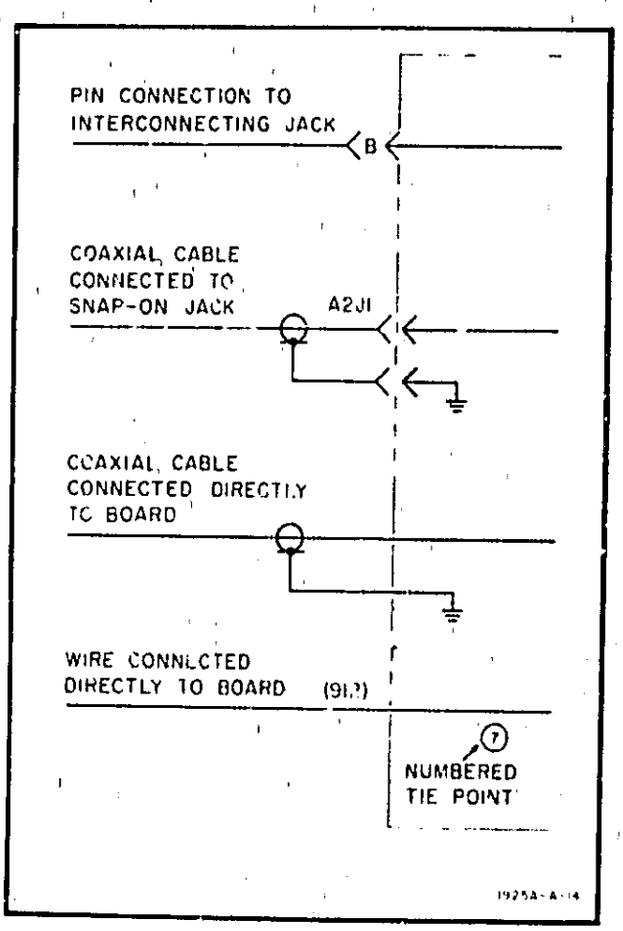


Figure 8-1. Circuit Board Connections

8-11. COMPONENT IDENTIFICATION.

8-12. Locations of components on etched circuit boards are illustrated in paragraphs adjacent to the schematics. Since the schematics are drawn to show function, a particular etched circuit board assembly may be shown on several schematics. The component-identification photograph is located next to the schematic that shows most of the circuitry on the board.

8-13. REPAIR AND REPLACEMENT.

8-14. Most electrical components are accessible from the component side of the etched circuit board. Section VI provides a detailed parts list for use in ordering replacement parts. If satisfactory repairs cannot be made, contact the nearest Hewlett-Packard Sales/Service Office. If shipment for repair is recommended, refer to Section II for repackaging and shipping instructions.

8-15. SERVICING ETCHED CIRCUIT BOARDS.

8-16. The Model 1925A has the plated-through type etched circuit boards. When servicing this type of board, components may be removed or replaced by unsoldering from either side of the board. When removing large components such as potentiometers, rotate the soldering iron tip from lead to lead and remove the solder with a desoldering tool. HP Service Note M-20D contains additional information on the repair of etched circuit boards. The important considerations are as follows:

a. Do not apply excessive heat.

b. Apply heat to component lead and remove lead with a straight pull away from the board.

c. Use a toothpick or wooden splinter to clean hole.

d. Do not force leads of replacement components into holes.

CAUTION

When removing MECL II integrated circuits from the etched circuit board, a desoldering tool must be used to avoid damage to the board assembly. A desoldering tool similar to the deluxe model Soldapullt produced by Edsyn Company of California is recommended.

8-17. If the plated metal surface (conductor) lifts from the board, it may be cemented back with a quick-drying acetate-base cement (used sparingly) having good insulating properties. An alternate method of repair is to solder a good conducting wire along the damaged area.

8-18. TROUBLESHOOTING.

8-19. The most important prerequisite for successful troubleshooting is an understanding of how the instrument is designed to operate and correct usage of front-panel controls. Often suspected malfunctions are caused by improper control settings or circuit connections. Operation Section III which provides an explanation of controls and connectors and general operating considerations, and Principles of Operation Section IV which explains circuit theory are intended to satisfy this information requirement.

8-20. The following paragraphs outline procedures for locating and clearing problems in the Model 1925A.

8-21. PRELIMINARY CHECKOUT.

8-22. An indication of a malfunction may occur due to improper operating procedures, marginal operation of the instrument, or complete failure of a circuit component. To help in isolating the malfunction, perform the following check-out procedures:

a. Check for improper control settings (refer to Section III).

b. Visually inspect the instrument for loose wire and cable connections.

c. Visually inspect for burned, broken or chaffed wires, charred or discolored components, and any other indication of physical damage.

d. Check the input voltages to the Model 1925A at the plug-in connector.

e. Check for correct internal logic voltages at the following test points on board assembly A1:

TP1 ..... −1.8 wVdc (Clock Bias)
TP2 ..... −5.2 wVdc ±0.5 wVdc (Logic Power)
TP3 ..... −0.3 wVdc (Current Limiting)

8-23. DETAILED CHECKOUT.

8-24. If the malfunction is not resolved by performing the preliminary check-out procedures, a detailed check out of the electrical circuits is necessary. Refer to Section IV, Principles of Operation, as an aid in diagnosing circuit malfunctions.

8-25. TEST EQUIPMENT. A detailed check-out of the instrument's electrical circuits can be accomplished using the test equipment listed in Table 5-1. No additional test equipment or accessories are required.

8-26. TEST SETUP. To troubleshoot the Model 1925A, set up the instrument as follows:

a. Remove the Rate Generator and the Model 1925A Word Generator from the 1900-series mainframe.

b. Connect HP Extender, Part Number 10484A, between the Rate Generator and Model 1925A to the 1900-series mainframe compartment connectors.

c. Set the mainframe power switch to the on position.

8-27. As an aid in isolating an instrument malfunction to a circuit stage, refer to the troubleshooting tree covered in Figure 8-2. Using the front-panel controls, attempt to isolate the malfunction to a particular circuit. After locating the faulty circuit stage, check the dc voltages of the circuit to determine the defective components. Since most of the circuits are of the integrated circuit type, malfunctions can normally be isolated by comparing output to input functions. When checking dc voltages of the integrated circuits, use a 1000-ohm resistor in series with the Digital Voltmeter probe. Attempting direct voltage measurements with a DVM or other type voltmeter will result in erroneous measurements due to random changes in states of the integrated circuits. Faulty integrated circuits must be replaced in their entirety. Care should be taken when removing and replacing them. When an integrated circuit assembly is replaced, the Performance Check as outlined in Section V must be accomplished.

Note

The three board assemblies (A1, A2 and A3) cannot be placed on extenders as the added stray capacitance will result in erroneous operations. In order to check components on these boards, use an extension to the test probe tip. Care should be exercised so that the extension does not short the mounted components.

8-28. DC VOLTAGES. DC voltages are indicated on some of the schematics for active components (transistors, etc). Control conditions for making the voltage measurements are listed adjacent to the schematics. Since the conditions for making these measurements may differ from one circuit to another, always check the specific conditions listed.

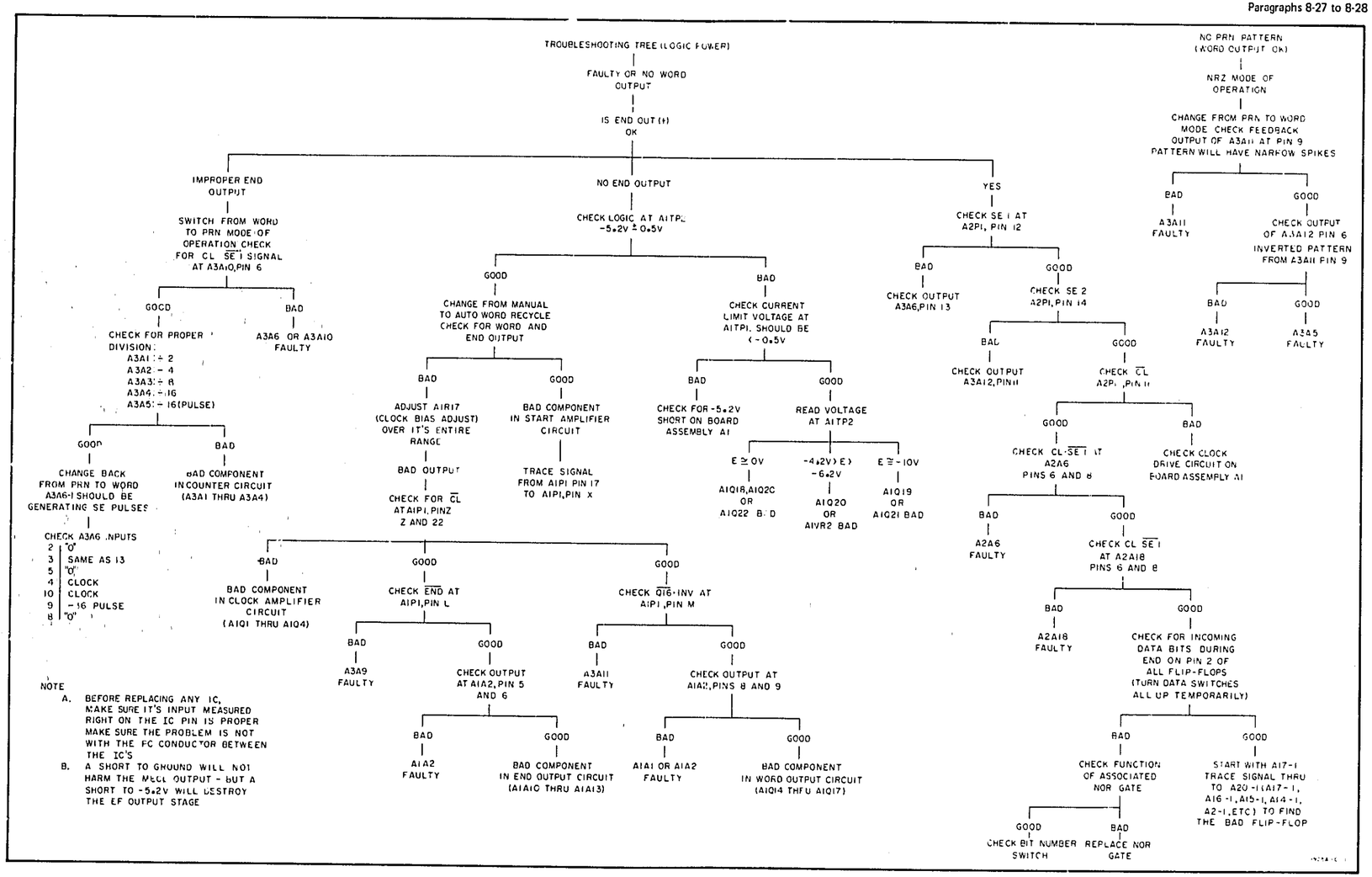


Figure 8-2. Troubleshooting Tree

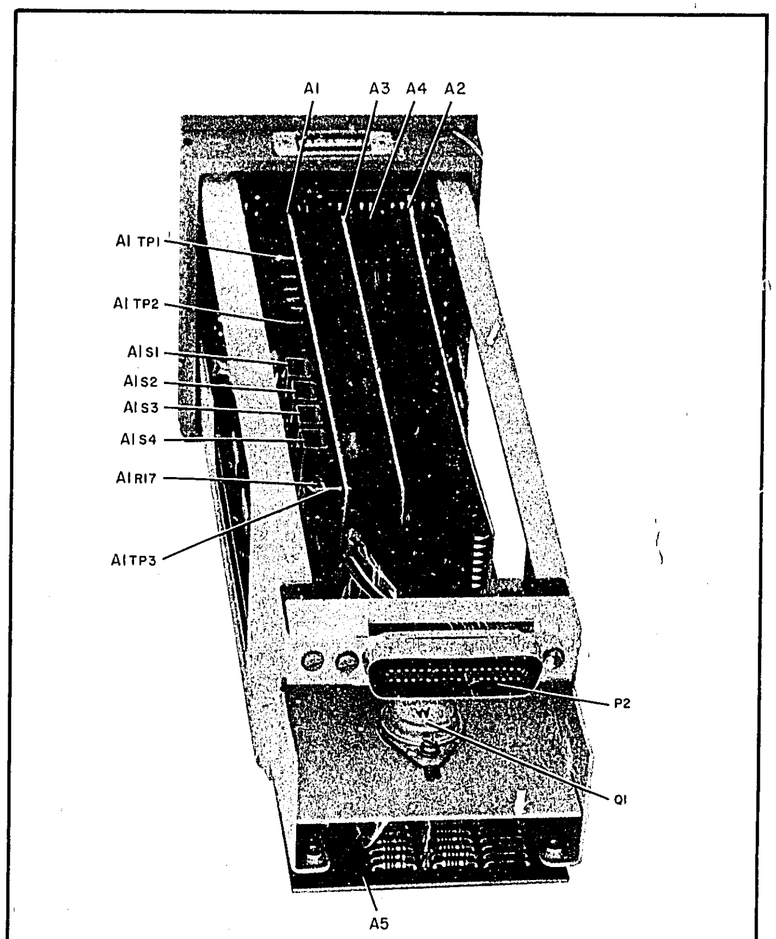


Figure 8-3. Chassis Parts Identification (Part I)

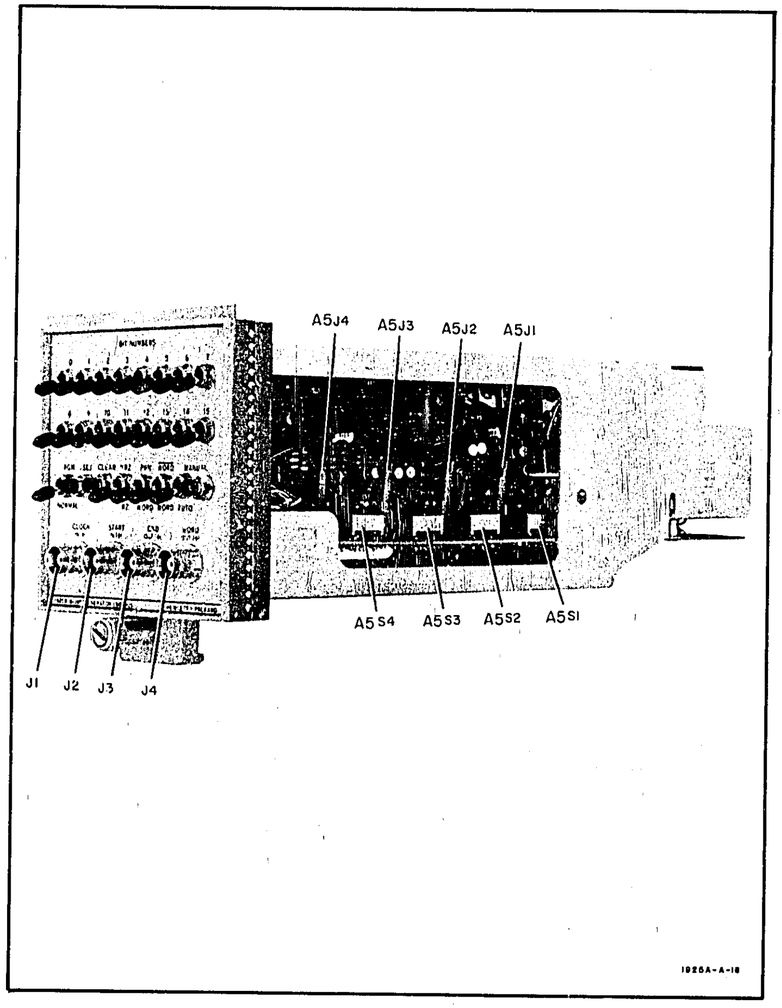
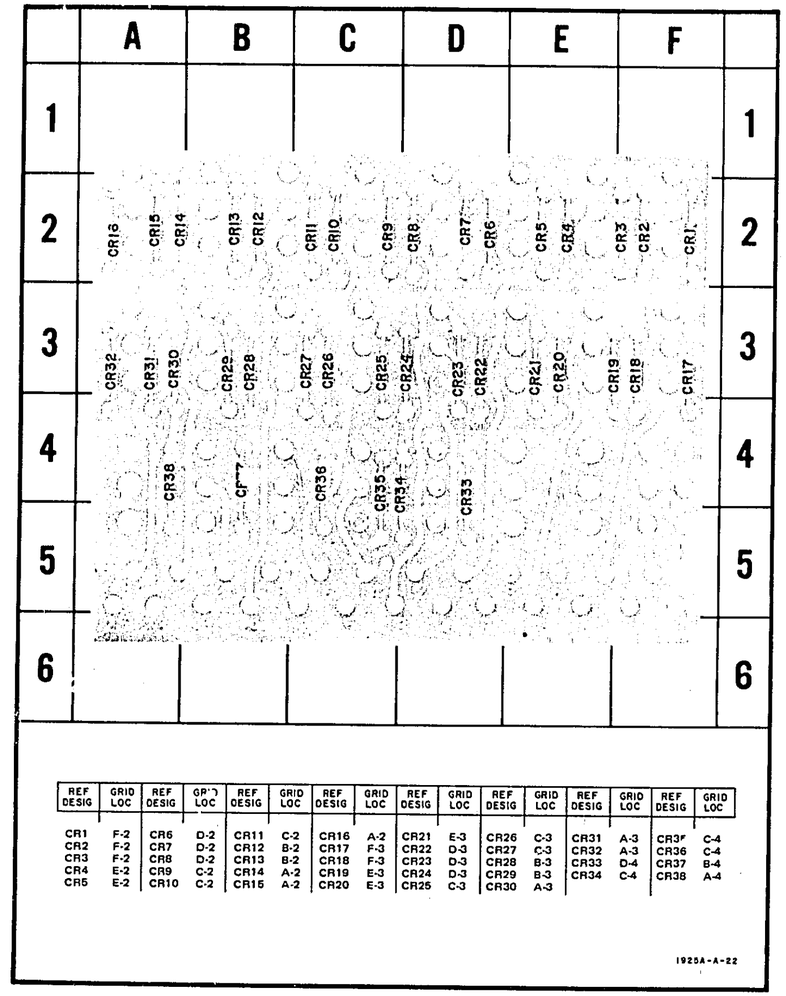
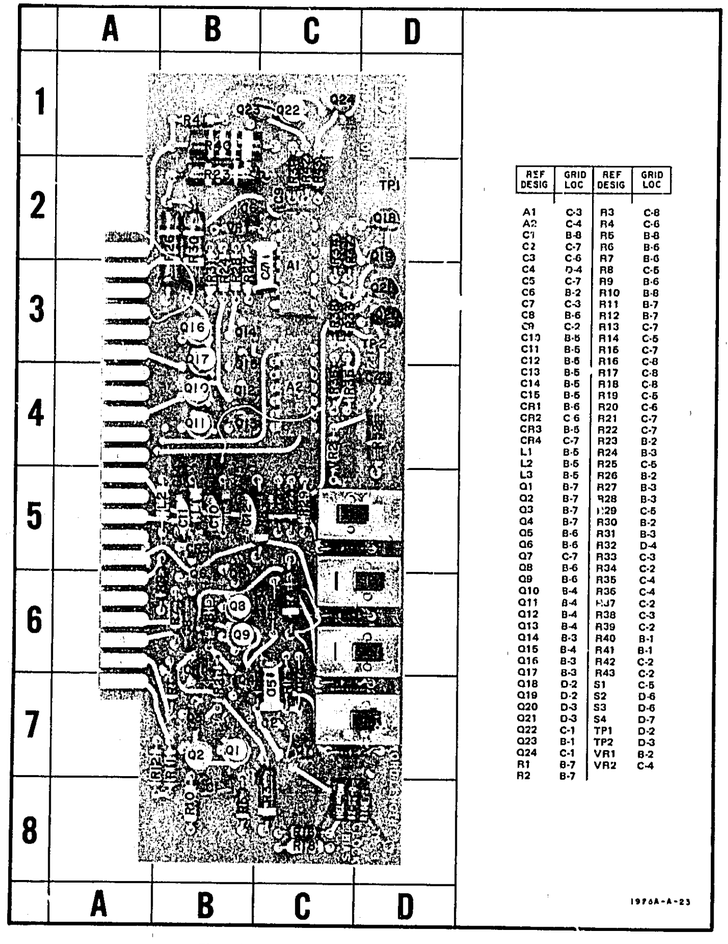


Figure 8-4. Chassis Parts Identification (Part II)



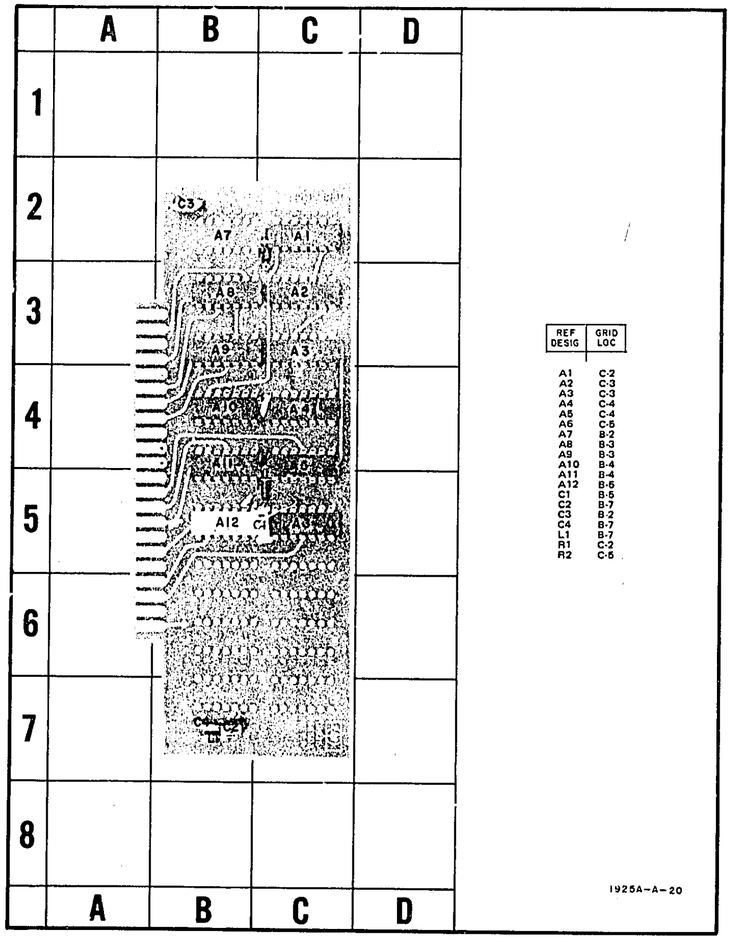
REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
CR1	F-2	CR6	D-2	CR11	C-2	CR16	A-2	CR21	E-3	CR26	C-3	CR31	A-3	CR35	C-4
CR2	F-2	CR7	D-2	CR12	B-2	CR17	F-3	CR22	D-3	CR27	C-3	CR32	A-3	CR36	C-4
CR3	F-2	CR8	D-2	CR13	B-2	CR18	F-3	CR23	D-3	CR28	B-3	CR33	D-4	CR37	B-4
CR4	E-2	CR9	C-2	CR14	A-2	CR19	E-3	CR24	D-3	CR29	B-3	CR34	C-4	CR38	A-4
CR5	E-2	CR10	C-2	CR15	A-2	CR20	E-3	CR25	C-3	CR30	A-3				

Figure 8-5. Board Assembly A4 Component Identification



REF DESIG	GRID LOC	REF DESIG	GRID LOC
A1	C-3	R3	C-8
A2	C-4	R4	C-6
C1	B-8	R5	B-8
C2	C-7	R6	B-6
C3	C-6	R7	B-6
C4	D-4	R8	C-5
C5	C-7	R9	B-6
C6	B-2	R10	B-8
C7	C-3	R11	B-7
C8	B-6	R12	B-7
C9	C-2	R13	C-7
C10	B-5	R14	C-5
C11	B-5	R15	C-7
C12	B-8	R16	C-8
C13	B-5	R17	C-8
C14	B-5	R18	C-8
C15	B-5	R19	C-5
CR1	B-6	R20	C-6
CR2	C-6	R21	C-7
CR3	B-5	R22	C-7
CR4	C-7	R23	B-2
L1	B-5	R24	B-3
L2	B-5	R25	C-5
L3	B-5	R26	B-2
Q1	B-7	R27	B-3
Q2	B-7	R28	B-3
Q3	B-7	R29	C-5
Q4	B-7	R30	B-2
Q5	B-6	R31	B-3
Q6	B-6	R32	D-4
Q7	C-7	R33	C-3
Q8	B-6	R34	C-2
Q9	B-6	R35	C-4
Q10	B-4	R36	C-4
Q11	B-4	R37	C-2
Q12	B-4	R38	C-3
Q13	B-4	R39	C-2
Q14	B-3	R40	B-1
Q15	B-4	R41	B-1
Q16	B-3	R42	C-2
Q17	B-3	R43	C-2
Q18	D-2	S1	C-5
Q19	D-2	S2	D-6
Q20	D-3	S3	D-6
Q21	D-3	S4	D-7
Q22	C-1	TP1	D-2
Q23	B-1	TP2	D-3
Q24	C-1	VR1	B-2
R1	B-7	VR2	C-4
R2	B-7		

Figure 8-8. Board Assembly A1 Component Identification



REF DESIG	GRID LOC
A1	C-2
A2	C-3
A3	C-3
A4	C-4
A5	C-4
A6	C-5
A7	B-2
A8	B-3
A9	B-3
A10	B-4
A11	B-4
A12	B-5
C1	B-5
C2	B-7
C3	B-2
C4	B-7
L1	B-7
R1	C-2
R2	C-5

Figure 8-9. Board Assembly A3 Component Identification

Table 8-2. Clock Driver Measurements

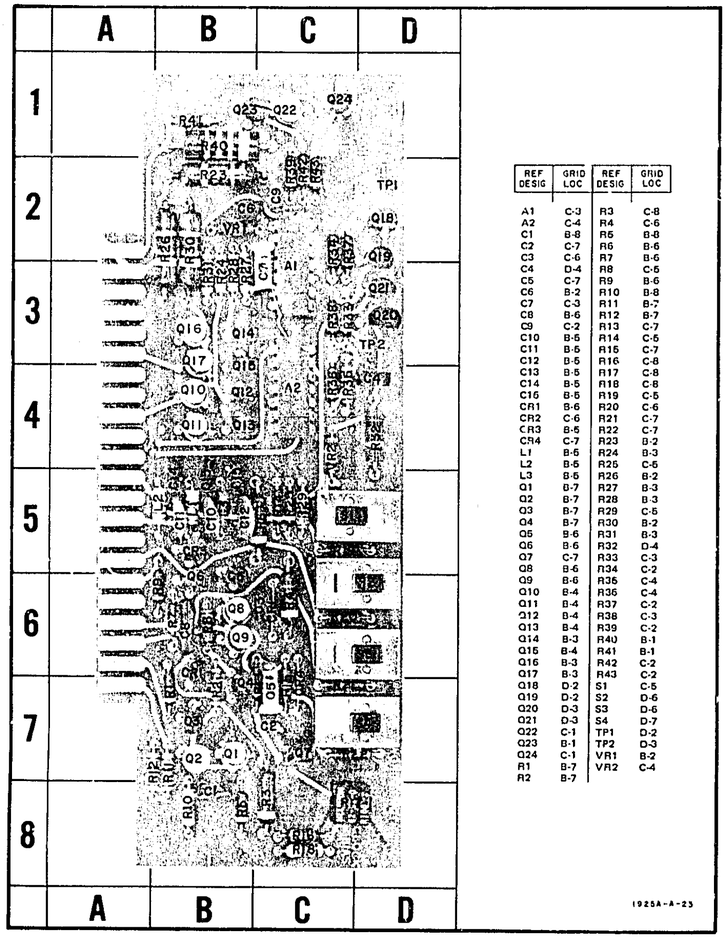
DC VOLTAGE MEASUREMENT CONDITIONS

Model 1905A		Model 1925A	
		All bit switches	off
RATE SOURCE	INT	PGM/NORMAL	NORMAL
		NRZ/RZ	RZ
RATE HZ	2.5M - 25M	PRN/WORD	WORD
INC	10 MHz	WORD/WORD	WORD
GATED/NORMAL	NORMAL	MANUAL/AUTO	MANUAL

Voltages may vary slightly from one instrument to another. Normal variations to 15% are permissible. Unless otherwise indicated, all voltage on board assembly A1 are taken with a digital voltmeter and measured to ground (chassis). All voltages on board assembly A3 are taken with an oscilloscope using a X10 probe.

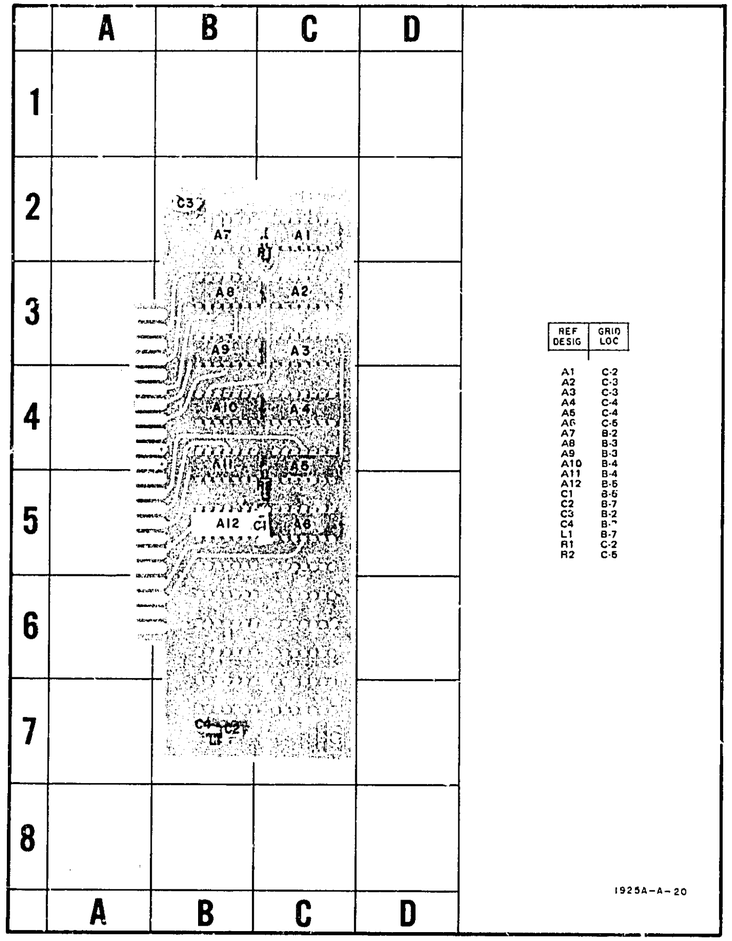
WAVEFORM MEASUREMENT CONDITIONS

Model 1905A		Model 1925A	
RATE SOURCE	INT		
		All bit switches	on
RATE HZ	2.5M-25M	PGM/NORMAL	NORMAL
INC	10 MHz		
GATED/NORMAL	NORMAL	NRZ/RZ	RZ
Real-Time Oscilloscope		PRN/WORD	WORD
Sweep	main		
Time/div	.5 usec	WORD/WORD	WORD
Volts/div	.02	MANUAL/AUTO	AUTO



REF DESIG	GRID LOC	REF DESIG	GRID LOC
A1	C-3	R3	C-8
A2	C-4	R4	C-6
C1	B-8	R5	B-8
C2	C-7	R6	B-6
C3	C-6	R7	B-6
C4	D-4	R8	C-5
C5	C-7	R9	B-6
C6	B-2	R10	B-8
C7	C-3	R11	B-7
C8	B-6	R12	B-7
C9	C-2	R13	C-7
C10	B-5	R14	C-6
C11	B-5	R15	C-7
C12	B-5	R16	C-8
C13	B-5	R17	C-8
C14	B-5	R18	C-8
C16	B-5	R19	C-5
CR1	B-6	R20	C-6
CR2	C-6	R21	C-7
CR3	B-5	R22	C-7
CR4	C-7	R23	B-2
L1	B-5	R24	B-3
L2	B-5	R25	C-6
L3	B-5	R26	B-2
Q1	B-7	R27	B-3
Q2	B-7	R28	B-3
Q3	B-7	R29	C-5
Q4	B-7	R30	B-2
Q5	B-6	R31	B-3
Q6	B-6	R32	D-4
Q7	C-7	R33	C-3
Q8	B-6	R34	C-2
Q9	B-6	R35	C-4
Q10	B-4	R36	C-4
Q11	B-4	R37	C-2
Q12	B-4	R38	C-3
Q13	B-4	R39	C-2
Q14	B-3	R40	B-1
Q15	B-4	R41	B-1
Q16	B-3	R42	C-2
Q17	B-3	R43	C-2
Q18	D-2	S1	C-5
Q19	D-2	S2	D-6
Q20	D-3	S3	D-6
Q21	D-3	S4	D-7
Q22	C-1	TP1	D-2
Q23	B-1	TP2	D-3
Q24	C-1	VR1	B-2
R1	B-7	VR2	C-4
R2	B-7		

Figure 8-8. Board Assembly A1 Component Identification



REF DESIG	GRID LOC
A1	C-2
A2	C-3
A3	C-3
A4	C-4
A5	C-4
A6	C-5
A7	B-2
A8	B-3
A9	B-3
A10	B-4
A11	B-4
A12	B-5
C1	B-6
C2	B-7
C3	B-2
C4	B-7
L1	B-7
R1	C-2
R2	C-5

Figure 8-9. Board Assembly A3 Component Identification

Table 8-2. Clock Driver Measurements

DC VOLTAGE MEASUREMENT CONDITIONS

Model 1905A		Model 1925A	
		All bit switches	off
RATE SOURCE	INT	PGM/NORMAL	NORMAL
		NRZ/RZ	RZ
RATE HZ	2.5M - 25M	PRN/WORD	WORD
INC	10 MHz	$\overline{\text{WORD}}$/WORD	WORD
GATED/NORMAL	NORMAL	MANUAL/AUTO	MANUAL

Voltages may vary slightly from one instrument to another. Normal variations to 15% are permissible. Unless otherwise indicated, all voltage on board assembly A1 are taken with a digital voltmeter and measured to ground (chassis). All voltages on board assembly A3 are taken with an oscilloscope using a X10 probe.

WAVEFORM MEASUREMENT CONDITIONS

Model 1905A		Model 1925A	
RATE SOURCE	INT		
		All bit switches	on
RATE HZ	2.5M-25M	PGM/NORMAL	NORMAL
INC	10 MHz		
GATED/NORMAL	NORMAL	NRZ/RZ	RZ
Real-Time Oscilloscope			
Sweep	main	PRN/WORD	WORD
Time/div	.5 usec	$\overline{\text{WORD}}$/WORD	WORD
Volts/div	.02	MANUAL/AUTO	AUTO

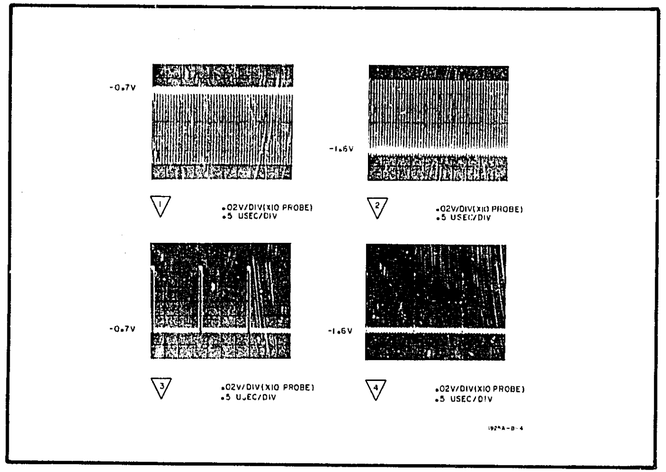
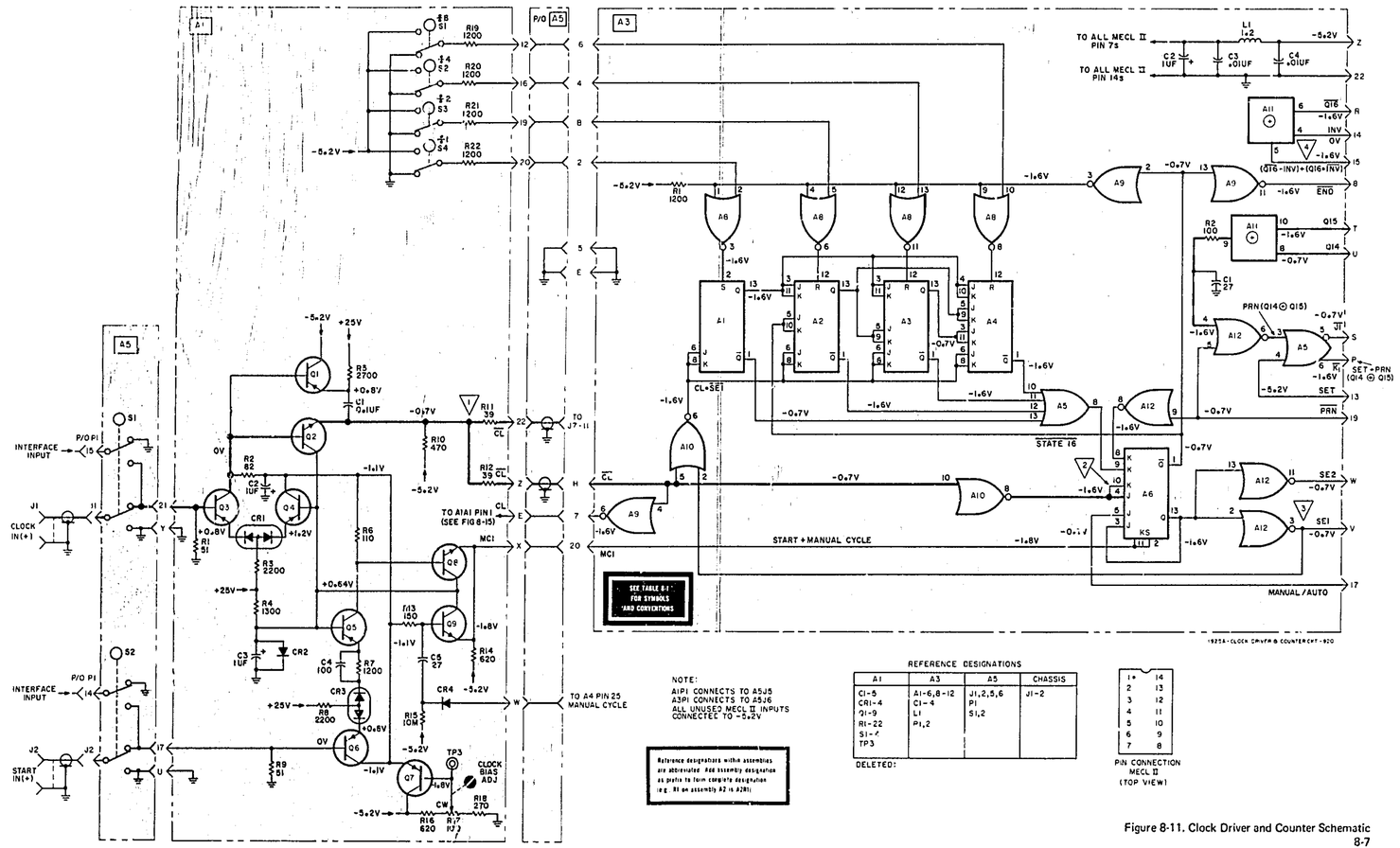


Figure 8-10. Test Point Waveforms (Part I)



NOTE:
A1P1 CONNECTS TO A5J5
A3P1 CONNECTS TO A5J6
ALL UNUSED MECL II INPUTS CONNECTED TO -5.2V

Reference designators within assemblies are abbreviated. Add assembly designation as prefix to form complete designation (eg., R1 on assembly A2 is A2R1).

REFERENCE DESIGNATIONS

A1	A3	A5	CHASSIS
C1-5	A1-6,8-12	J1,2,5,6	J1-2
CR1-4	C1-4	P1	
Q1-9	L1	S1,2	
R1-22	P1,2		
S1-4			
TP3			

DELETED:

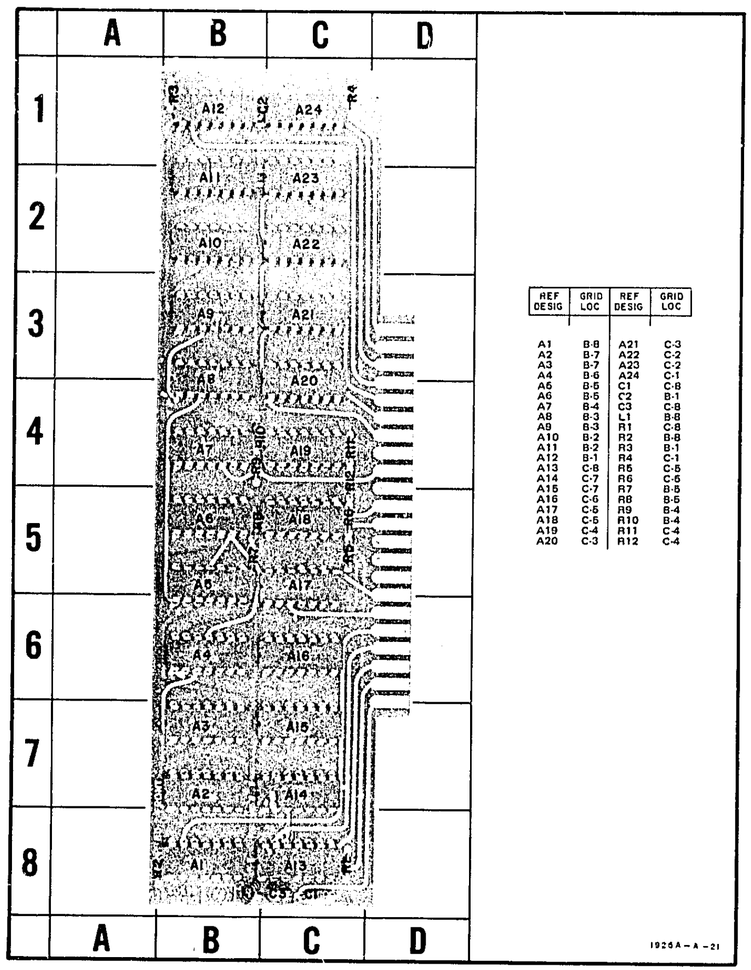
PIN CONNECTION MECL II (TOP VIEW)

Figure 8-11. Clock Driver and Counter Schematic

For Figure 8-13 refer to:

Waveform Measurement Conditions - Table 8-2.

DC Voltage Measurement Conditions - Table 8-2.



REF DESIG	GRID LOC	REF DESIG	GRID LOC
A1	B-8	A21	C-3
A2	B-7	A22	C-2
A3	B-7	A23	C-2
A4	B-6	A24	C-1
A5	B-5	C1	C-8
A6	B-5	C2	B-1
A7	B-4	C3	C-8
A8	B-3	L1	B-8
A9	B-3	R1	C-8
A10	B-2	R2	B-8
A11	B-2	R3	B-1
A12	B-1	R4	C-1
A13	C-8	R5	C-5
A14	C-7	R6	C-5
A15	C-7	R7	B-5
A16	C-6	R8	B-5
A17	C-5	R9	B-4
A18	C-5	R10	B-4
A19	C-4	R11	C-4
A20	C-3	R12	C-4

Figure 8-12. Board Assembly A2 Component Identification

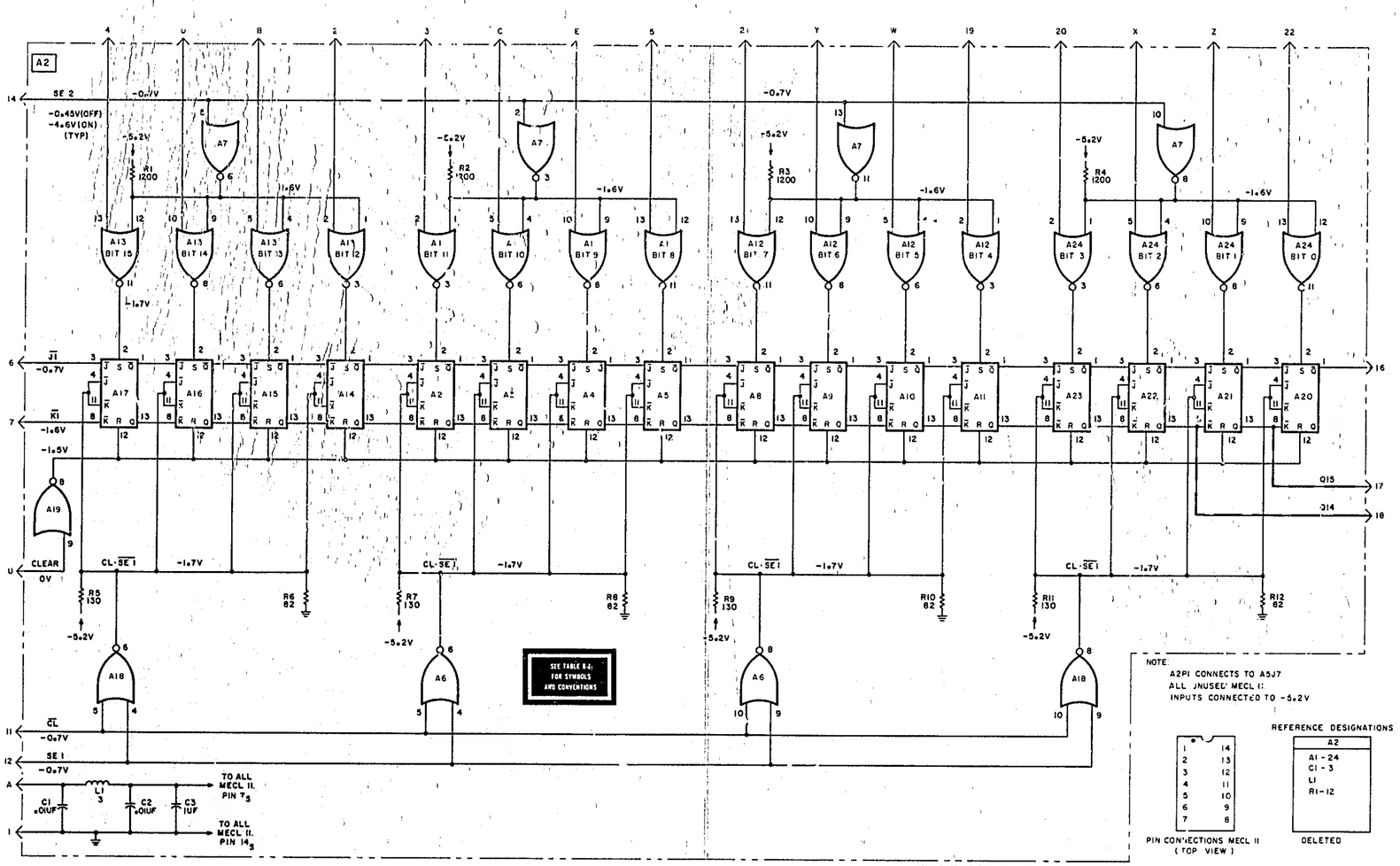


Figure 8-13. Shift Register Schematic

See Figure 8-8 for Board Assembly A1 Component Identification.

Table 8-3. Output Circuit Measurements

DC VOLTAGE MEASUREMENT CONDITIONS

Model 1905A		Model 1925A	
RATE SOURCE	INT	All Bit switches	off
RATE HZ	2.5M-25M	PGM/NORMAL	NORMAL
INC	10 MHz	NRZ/RZ	RZ
GATED/NORMAL	NORMAL	PRN/WORD	WORD
		$\overline{\text{WORD}}$/WORD	WORD
		MANUAL/AUTO	MANUAL

Voltages may vary slightly from one instrument to another. Normal variations to 15% are permissible. Unless otherwise indicated, all voltages are taken with a digital voltmeter to ground (chassis).

WAVEFORM MEASUREMENT CONDITIONS

Model 1905A		Model 1925A	
RATE SOURCE	INT		
RATE HZ	2.5M-25M	All bit switches	on
INC	10 MHz	PGM/NORMAL	NORMAL
GATED/NORMAL	NORMAL		
Real-Time Oscilloscope		NRZ/RZ	RZ
Time/div	.5 usec		
Volts/div	.02	PRN/WORD	WORD
TRIGGER			
WORD OUT	Use END out of Model 1925A	$\overline{\text{WORD}}$/WORD	WORD
END OUT	Internal	MANUAL/AUTO	AUTO

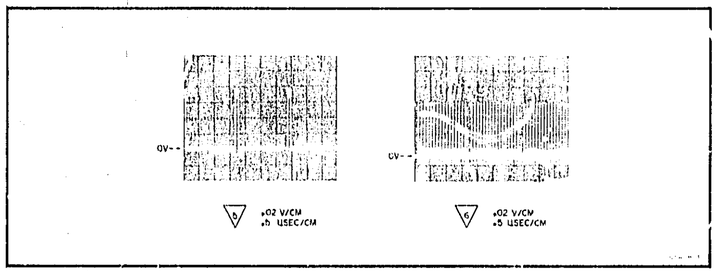
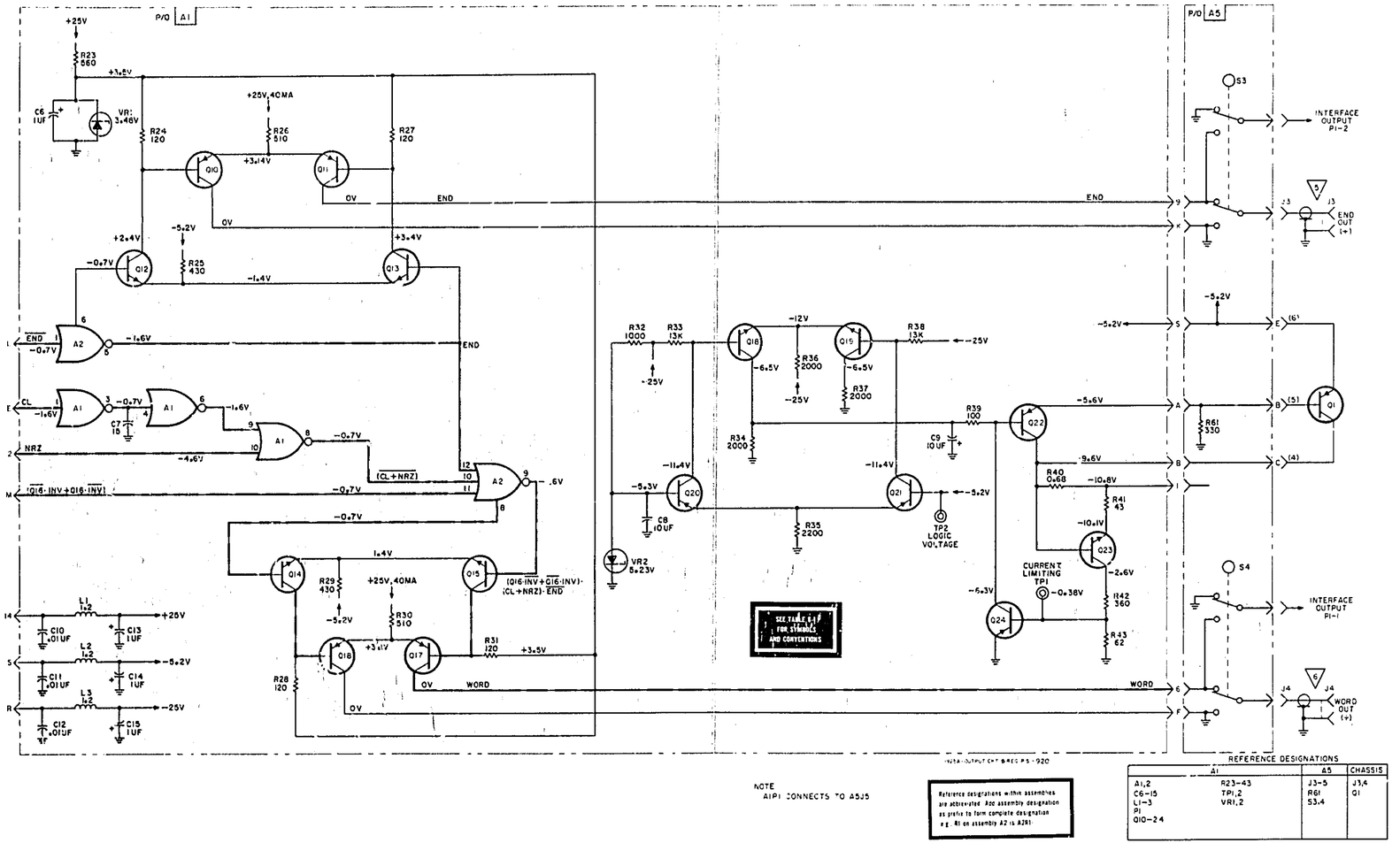


Figure 8-14. Test Point Waveforms (Part II)



NOTE
A1P1 CONNECTS TO A5J5

Reference designations within assemblies are abbreviated. Add assembly designation as prefix to form complete designation e.g., R1 on assembly A2 is A2R1.

REFERENCE DESIGNATIONS

A1		A5	CHASSIS
A1,2	R23-43	J3-5	J3,4
C6-15	TP1,2	R61	Q1
L1-3	VR1,2	S3,4	
P1			
Q10-24			

Figure 8-15. Output Circuit and Power Supply Schematic

MANUAL CHANGES

MODEL 1925A

WORD GENERATOR

Manual Serials Prevised: 920–
Manual Printed: June 1969

Make all changes listed below as Errata. Check the following table for your instrument serial prefix and/or serial number and make listed change(s) to the manual.

Serial Prefix or Number	Make Changes	Serial Prefix or Number	Make Changes
953–	1	1422A	1 thru 5
954– and 955–	1, 2		
1205A	1, 2, 3		
1232A	1, 2, 3, 4		

ERRATA

Page 1-0, Table 1-1,
PSUEDO-RANDOM NOISE
Maximum clockrate is 25 MHz.

Page 5-3, Paragraph 5-11 I,
Change: A2S2 to read A1S2.

Page 5-2, Figure 5-2,
Connection from Model 1410A to Model 1925A:
Move to second BNC from right on Model 1925A.

Pages 5-3 through 5-6,
Replace with pages 5-3 through 5-6 attached to this manual changes sheet.

Table 6-2, Chassis,
J1-J4: Change to HP Part No. 1250-0001; TQ4;
Connector: BNC bulkhead mounting.

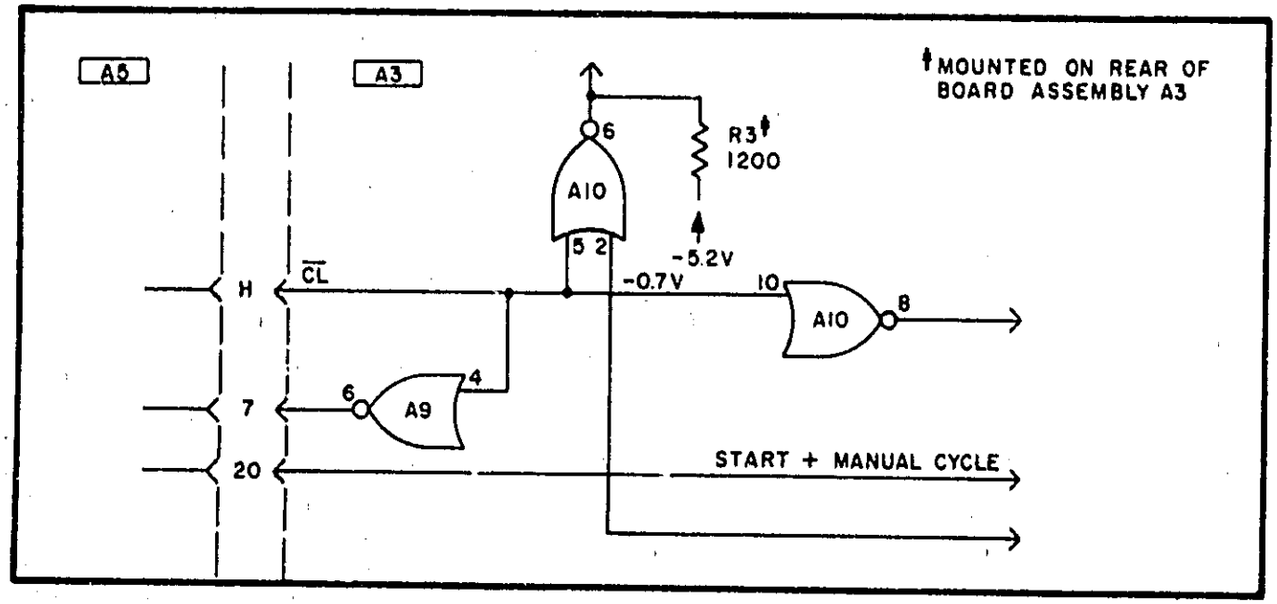


Figure 1.

2 April 1976
Δ = Latest additions to this change sheet.
This change sheet supersedes all prior change sheets for this manual.

Supplement A for
01925-90901

ERRATA (Cont'd)

Table 6-2, MISCELLANEOUS.
Add: MP5; HP Part No. 01925-60201; TQ1; Panel; front, mint-gray.
Add: MP5; HP Part No. 01925-00201; TQ1; Panel; front, anodized (Option X95).
Add: MP6; HP Part No. 01925-20202; TQ1; Frame; front panel, mint-gray (Option X95).
Table 6-2, A1 Board Assembly,
C7: Change to HP Part No. 0150-0115, C:fxd cer 27 pF 10% 500 wVdc (for units before serial prefix 1422A).
Add: C18, HP Part No. 0160-3739, C:fxd cer 18 pF 10% 100 wVdc.
R41: Change to HP Part No. 0757-0392, R: fxd metflm 43.2 ohms 1% 1/8W.
Table 6-2, A2 Board Assembly,
Add: R13, HP Part No. 0698-7482; R:fxd cer 1200 ohms 10% 1/8W.
R1: Change TQ column to 7.
Table 6-2, A5 Board Assembly,
Add: W1, HP Part No. 01934-61608; W: Cable assembly, CLOCK interface.
Add: W2, HP Part No. 01930-61602; W: Cable assembly, START interface.

Page 7-1/7-2,
Replace page 7-1/7-2 with new page 7-1/7-2 attached.
Page 8-5, Figure 8-7,
A5: Change schematic designation J6-2 to J6-7.
Page 8-6, Figure 8-8,
Reverse locations of C4 and C8.
Page 8-7, Figure 8-11,
Add resistor A3R3. See Figure 1.
Add A5W1 (84) between A5P1 pin 15 and A5S1.
Add A5W2 (85) between A5P1 pin 14 and A5S2.
Page 8-9, Figure 8-13,
Add resistor A2R13. See Figure 2.
Page 8-11, Figure 8-15,
A1C7: Change value to 27 (for units before serial prefix 1422A).
Add: C18 (18 pF) from A1 pin 9 to ground.
A1R41: Change value to 43.2 ohms.

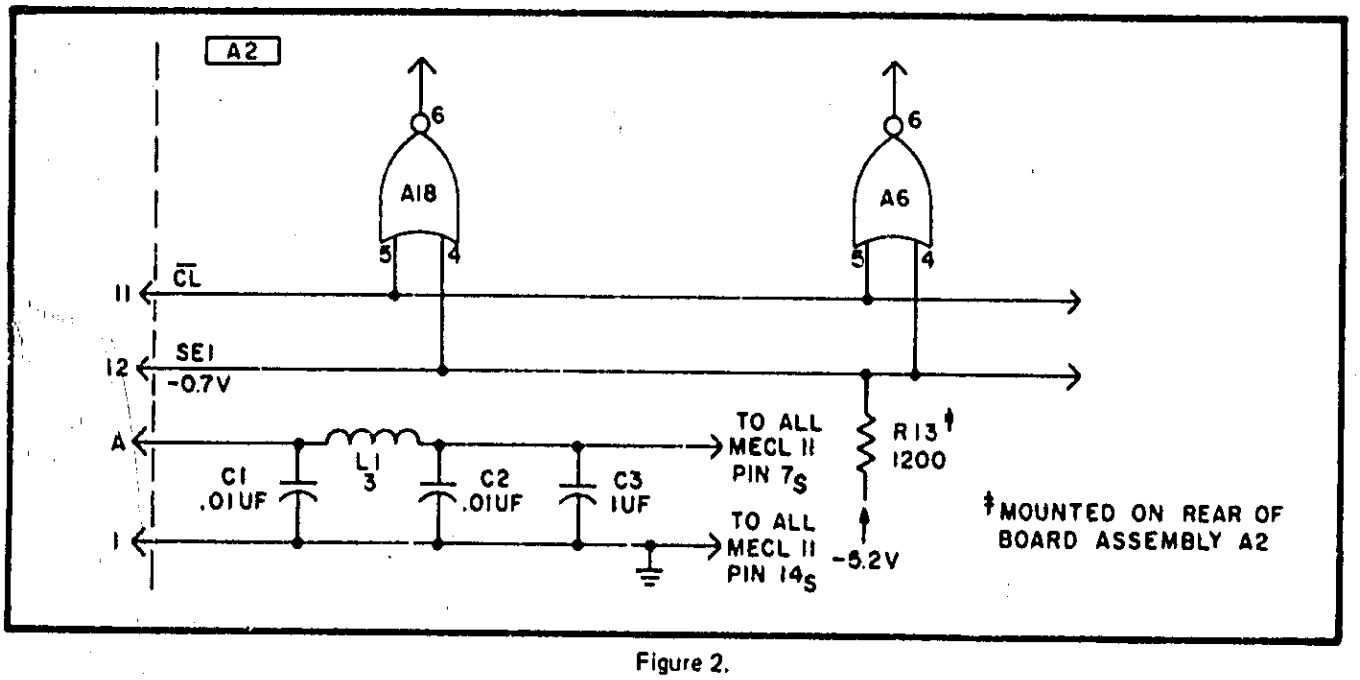


Figure 2.

CHANGE 1

Table 6-2, A3 Board Assembly,
Add: C5 HP Part No. 0160-3448, C:fxd cer 1000 pF 10% 1000 wVdc.

Page 8-7, Figure 8-11,
Add: C5, a 1000-pF capacitor, connected from A6-5 to ground.

CHANGE 2

Table 6-2, A1 Board Assembly,
Add: C16; HP Part No. 0150-0115; C: fxd cer 27 pF 10% 500 wVdc. (factory selected value).
Add: C17; HP Part No. 0150-0115; C: fxd cer 27 pF 10% 500 wVdc. (factory selected value).
CR2: Change to HP Part No. 1910-0016; CR: Ge.
R40: Change to HP Part No. 0811-0929; R: fxd ww .50 ohm 5% 2W.

Table 6-2, A2 Board Assembly,
Add: C4; HP Part No. 0150-0093; C: fxd cer .01 uF 100 wVdc.
Page 8-9, Figure 8-13,
Add: A2C4 (.01 uF) from A2A5 pin 12 to ground.
Page 8-11, Figure 8-15,
Add A1C16* (27 pF) from A1A1 pin 6 to ground.
Add A1C17* (27 pF) from A1A2 pin 6 to ground.
A1R40: Change value to 0.5 ohm.

CHANGE 3

Table 1-1, Page 1-0,
PSEUDO-RANDOM NOISE: Change to PSEUDO-RANDOM BINARY SEQUENCE.
Figure 1-1, Page 1-1,
Change front-panel PRN switch call out PRBS.

Change all manual references from PSEUDO-RANDOM NOISE (PRN) to PSEUDO-RANDOM BINARY SEQUENCE (PRBS).

CHANGE 4

Table 6-2,
W8: Change to HP Part No. 01925-61608; W: Cable assembly, PGM.

CHANGE 5

Table 6-2,
Add: A3A13, HP Part No. 1820-0102, IC: J-K flip-flop Motorola MC 1013P.
Add: A3A14, HP Part No. 1820-0145, IC: ECL Quad NOR motorola MC1010P.
A1C7: Change to HP Part No. 0160-3799, C: fxd cer 18 pF 10% 100 wVdc.

Page 8-7, Figure 8-11,
Add: Figure 3 of this manual changes sheet.
Pages 8-7 and 8-9, Figures 8-11 and 8-13,
Add: Figure 4 of this manual changes sheet.
Page 8-11, Figure 8-15,
A1C7: Change value to 18 pF.

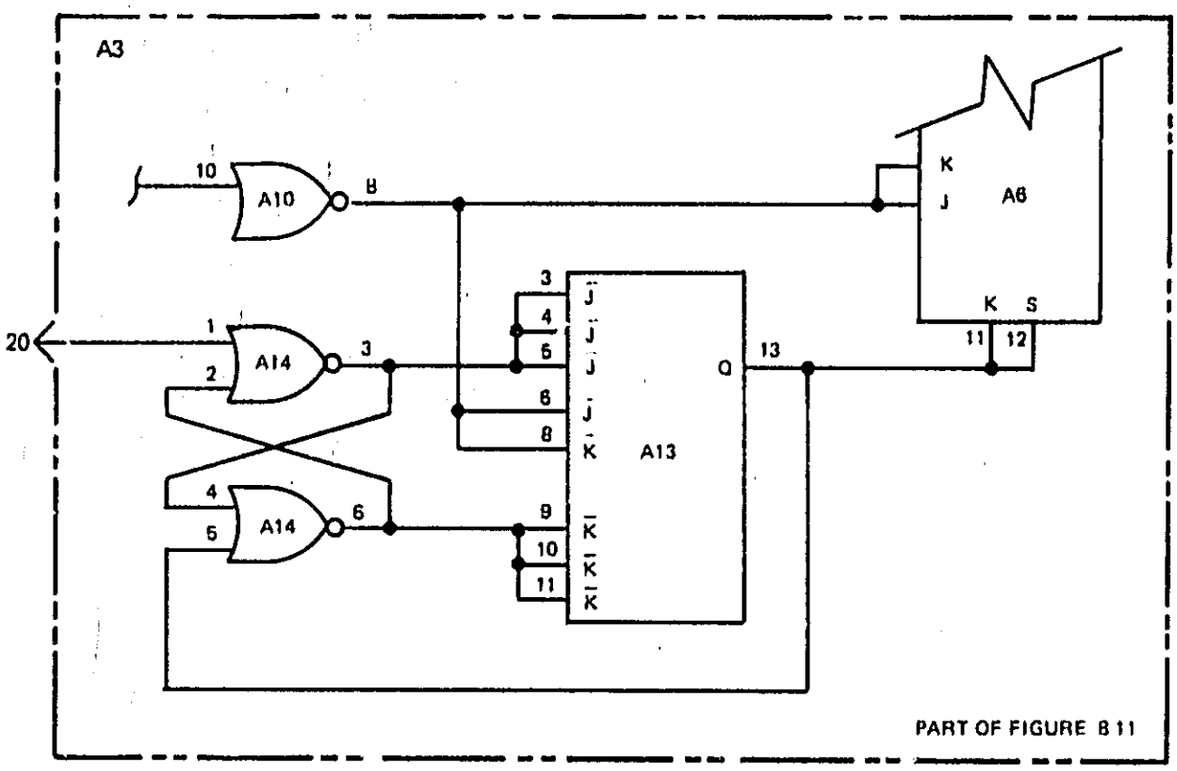


Figure 3. Synchronize EXT START with Clock Circuit

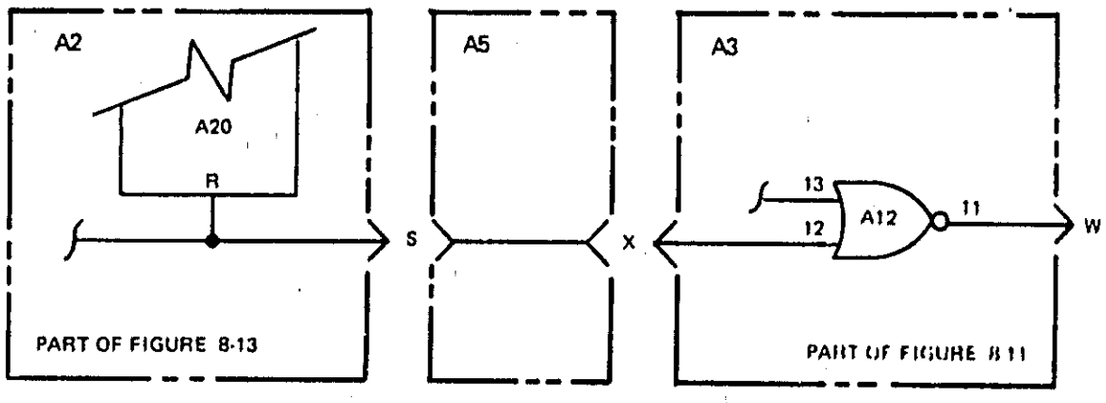


Figure 4. CLEAR Zero Bit Circuit

e. Energize each bit-number switch and observe the pulses on the real-time oscilloscope CRT. When all bit switches are energized, a pulse train of 16 bits should be observed.

f. Set all bit-number switches to the off position. Press the SET pushbutton switch on the front panel of the Model 1925A. A 16-bit pulse sequence should be observed.

g. Set the bit-number switches on the Model 1925A to a logic sequence of 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0. Observe the pulse pattern on the real-time oscilloscope CRT.

h. Set the NRZ/RZ switch on the front panel of the Model 1925A to the NRZ position. Observe the pulse pattern on the oscilloscope CRT. Consecutive bit pulses should appear as one pulse.

i. Set the $\overline{\text{WORD}}$/WORD switch on the front panel of the Model 1925A to the $\overline{\text{WORD}}$ position. The pulse pattern should be the complement of the pattern observed in step h above.

5-11. VARIABLE WORD LENGTH.

a. Connect the equipment and accessories as indicated in Figure 5-3.

b. Set the Model 1905A front-panel controls as follows:

RATE SOURCE	INT
RATE Hz	2.5 - 25 MHz
INC	10 MHz
GATED/NORMAL	NORMAL

c. Set the real-time oscilloscope controls as follows:

Trigger	+, external, ac
Sweep Mode	normal
Time per division	0.2 microsecond

d. Set the Model 1925A front-panel controls as follows:

PGM/NORMAL	NORMAL
NRZ/RZ	RZ
PRN/WORD	WORD
$\overline{\text{WORD}}$/WORD	WORD
MANUAL/AUTO	AUTO

e. Set bit-number switch 0 and bit-number switch 8 to the on position. All other bit-number switches should be in the off position.

f. Set the word-length switches on Board Assembly A1 of the Model 1925A to the following positions:

A1S1	up
A1S2	down
A1S3	down
A1S4	down

g. See Figure 5-4 (A). A similar display should be observed on the oscilloscope CRT. The bit-number 0 pulse should follow immediately after the bit-number 8 pulse, indicating a nine-bit word length.

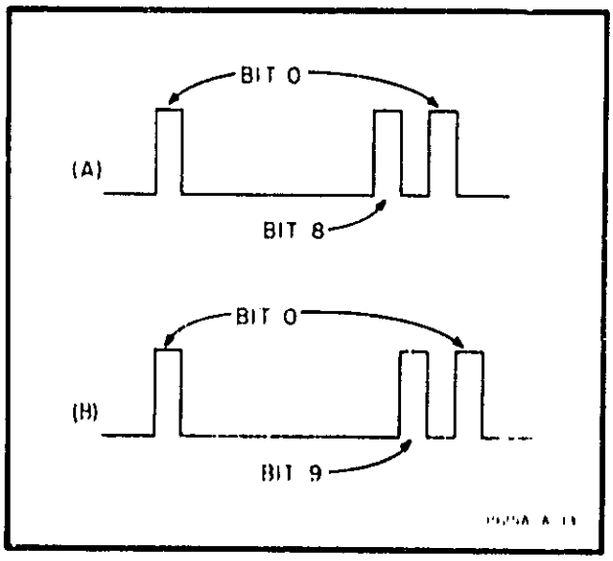


Figure 5-4. Word Length Check

h. Set bit-number switch 0 and bit-number switch 9 to the on position. All other bit-number switches should be in the off position.

i. Set the word-length switches on Board Assembly A1 of the Model 1925A to the following positions:

A1S1	down
A1S2	up
A1S3	up
A1S4	up

j. See Figure 5-4 (B). A similar display should be observed on the oscilloscope CRT. Bit-number 0 pulse should follow immediately after bit-number 9 pulse indicating a ten-bit word length.

5-12. PSEUDO RANDOM BINARY SEQUENCE CHECK.

a. Connect the equipment and accessories as shown in Figure 5-5.

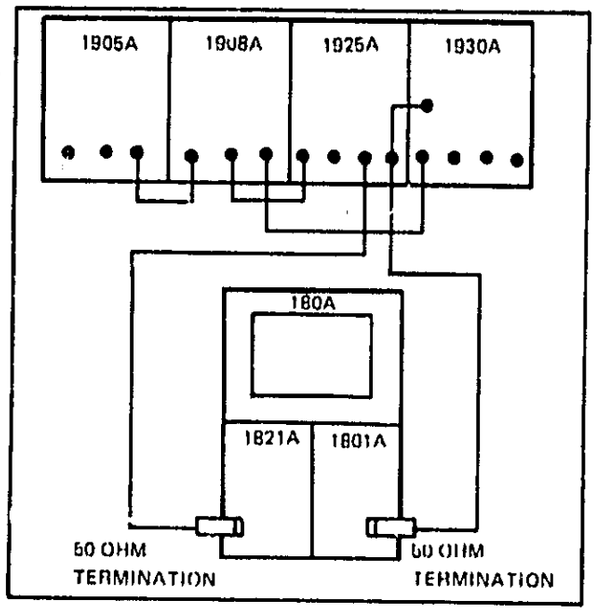


Figure 5-5. PRBS Test Setup

b. Set the Model 1905A front-panel controls as follows:

RATE SOURCE	INT
RATE Hz	2.5 - 25 MHz
INC	20 MHz
GATED/NORMAL	NORMAL

c. Set the Model 1925A front-panel controls as follows:

PGM/NORMAL	NORMAL
NRZ/RZ	RZ
PRBS/WORD	PRBS
WORD/WORD	WORD
MANUAL/AUTO	AUTO

d. Set the Model 1930A front-panel controls as follows:

PRBS/WORD	PRBS
MULTIPLY/NORM/ DIVIDE	NORM
REGISTER LENGTH	15

Δ e. Set the Model 1908A front-panel controls as follows:

DRIVE OUTPUT	DELAY
TIME INTERVAL	.01 - .1
TIME INTERVAL vernier	25 ns approx

f. Set the real-time oscilloscope controls as follows:

Trigger	+, external, ac
Sweep Mode	normal
Time per division	5 usec/div
Volts per division	2 V/div

g. Make sure that the DATA SYNC lamp on the Model 1930A is out.

h. On the Model 1930A, press the DATA SYNC push button. The DATA SYNC lamp should light and stay on.

i. If the DATA SYNC lamp does not light and stay on, press the CLEAR and then the SET push buttons on the Model 1925A. Then press the DATA SYNC pushbutton on the Model 1930A. Delay may also be adjusted slightly. Nominal delay is from 15 ns to 40 ns. (Avoid excessive delay.) The DATA SYNC lamp should light and stay on.

5-13. FREQUENCY CHECK.

a. Connect the equipment and accessories as shown in Figure 5-6.

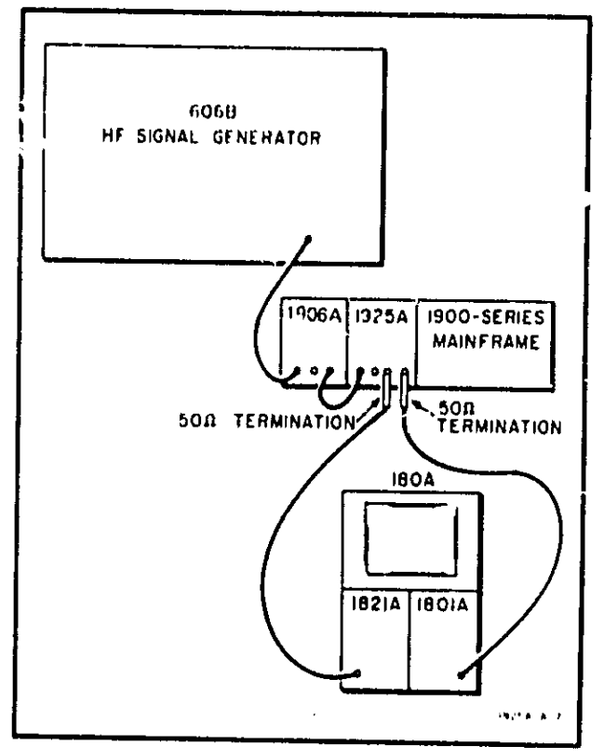


Figure 5-6. Frequency Check Test Setup

b. Set the Model 606B front-panel controls as follows

RANGE	19-65 MC
ATTENUATOR	3V rms

c. Set the Model 1906A front-panel controls as follows:

RATE SOURCE	EXT +
GATED/NORMAL	NORMAL

d. Set word-length switches on board assembly A1 to following positions:

A1S1 ..... down
A1S2 ..... down
A1S3 ..... down
A1S4 ..... up

e. Set the Model 1925A front-panel controls as follows:

Bit switch logic .. 1110;11000011101
PGM/NORMAL ..... NORMAL
NRZ/RZ ..... NRZ
PRN/WORD ..... WORD
$\overline{\text{WORD}}$/WORD ..... WORD
MANUAL/AUTO ..... AUTO

f. Set the real-time oscilloscope controls as follows:

Trigger ..... +, external, ac
Sweep Mode ..... normal
Volts per cm 5
Time per division ..... .2 microsecond

g. Vary the output frequency of the Model 606B between 19 MHz and 50 MHz. The pattern displayed on the real-time oscilloscope CRT should be independent of the repetition rate. If the pattern changes, adjust the clock-bias potentiometer A1R17 for a correct pattern.

5-14. PGM CHECK.

a. Set the equipment and accessories as indicated in Figure 5-7.

b. Set the Model 1905A controls as follows:

RATE SOURCE ..... INT
RATE Hz ..... 2.5 - 25 MHz
INC ..... 10 MHz
GATED/NORMAL ..... NORMAL

c. Set the real-time oscilloscope controls as follows:

Trigger ..... +, external, ac
Sweep Mode ..... normal

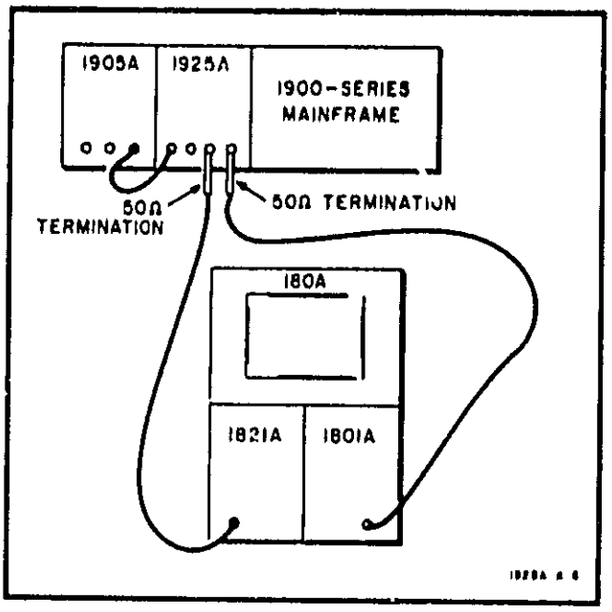


Figure 5-7. PGM Check Test Setup

d. Set the Model 1925A front-panel controls as follows:

PGM/NORMAL ..... PGM
$\overline{\text{WORD}}$/WORD ..... WORD

e. Refer to Table 3-1 for input programing and the function that is initiated. Using the table, check out the PGM circuitry.

5-15. ADJUSTMENTS.

5-16. The only adjustment in the Model 1925A is the clock bias adjustment. The normal voltage at Test Point 3 on Board Assembly A1 is −1.8 volts. This voltage will vary slightly between instruments after adjustments are made for maximum frequency operation. Refer to Paragraph 5-13g.

SECTION VII

MANUAL CHANGES AND OPTIONS

7-1. INTRODUCTION.

7-2. This section contains information required to backdate or update this manual for a specific instrument. Description of special options and standard options are also in this section.

7-3. MANUAL CHANGES.

7-4. This manual applies directly to the instrument having the same serial prefix shown on the manual title page. If the serial prefix of the instrument is not the same as the one on the title page, find your serial prefix in table 7-1 and make the changes to the manual that are listed for that serial prefix. When making changes listed in table 7-1, make the change with the highest number first. Example: if backdating changes 1, 2, and 3 are required for your serial prefix, do change 3 first, then change 2, and finally change 1. If the serial prefix of the instrument is not listed either in the title page or in table 7-1, refer to an enclosed MANUAL CHANGES sheet for updating information. Also, if a MANUAL CHANGES sheet is supplied, make all indicated ERRATA corrections.

Table 7-1. Manual Changes

Serial Prefix	Make Changes
No backdating changes are required at this time.	

7-5. SPECIAL OPTIONS.

7-6. Most customer special application requirements and/or specifications can be met by factory modification of a standard instrument. A standard instrument modified in this way will carry a special option number, such as Model 000A/Option C01.

7-7. An operating and service manual and a manual insert are provided with each special option instrument. The operating and service manual contains information about the standard instrument. The manual insert for the special option describes the factory modifications required to produce the special option instrument. Amend the operating and service manual by changing it to include all manual insert information (and MANUAL CHANGES sheet information, if applicable). When these changes are made, the operating and service manual will apply to the special option instrument.

7-8. If you have ordered a special option instrument and the manual insert is missing, notify the nearest Hewlett-Packard Sales/Service Office. Be sure to give a full description of the instrument, including the complete serial number and special option number.

7-9. STANDARD OPTIONS.

7-10. Standard options are modifications installed on HP instruments at the factory and are available on request. The following standard options are available with Model 1925A. Contact the nearest Hewlett-Packard Sales/Service Office for further information concerning standard options.

7-11. OPTION 005.

7-12. Model 1925A Option 005 provides facilities for digitally programming Model 1925A from an external source. The option is covered by a separate operating note supplied with each Option 005 instrument.

7-13. OPTION X95.

7-14. Model 1925A Option X95 is a standard Model 1925A whose external parts match the Hewlett-Packard blue-gray color scheme. To adapt this manual to cover the option X95, change table 6-2 as follows:

a. MP5: Change to HP Part No. 01925-00201, PANEL: FRONT ANODIZED.

b. MP6: Change to HP Part No. 01925-20201, FRAME: FRONT PANEL LIGHT GRAY.