HP 5480A
DSA

Contents

Notes

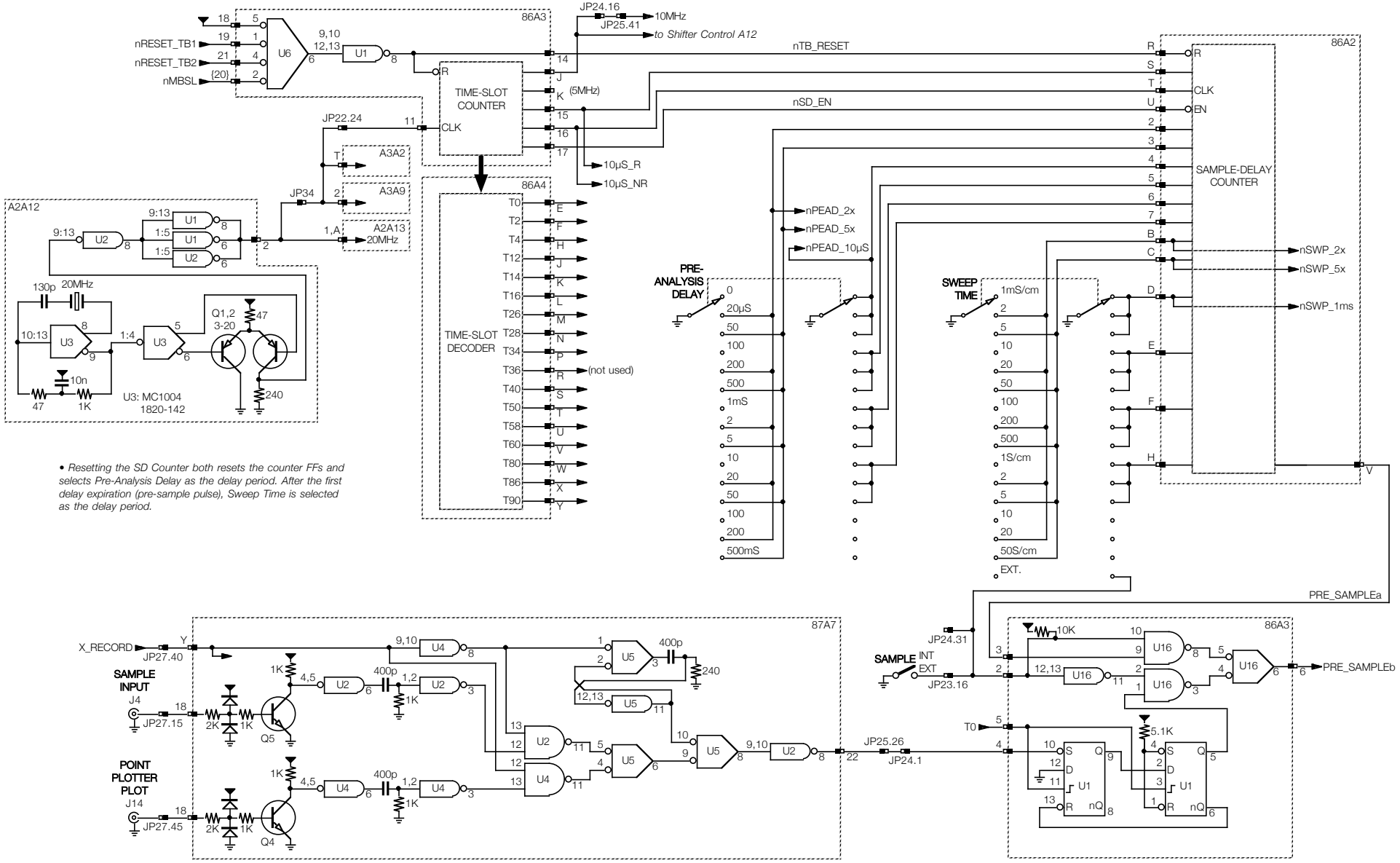
- The symbol  denotes a physical connector pin, where *c*=connector and *p*=pin. Solid black end is the male side of the connector. White end is the female side of the connector.
- The symbol ▼ without an additional label denotes +5V.
- Capacitance in microfarads unless otherwise indicated.
- *OUT: Several circuits have outputs tied together for a wired-AND function, however the outputs are totem-pole outputs, not open-collector.
- This drawing is based primarily on the manufacturer' s schematic, with additional observation of Unit 171. Many signals are renamed for greater consistency.
- ICs are identified by a prefix "U" rather than "IC" of the original schematic.
- Some signal connections which 'go nowhere' are not shown in this document. For example, many timing-slot signals are distributed to pins on more boards than shown but are not used on those boards.

Log

- 2022 May Initial drawing started / bhilpert.

ASSEMBLY	SCH	ASSEMBLY	SCH
5480 A1: DISP		5480 A4:	
1	√	1	√
2	√		
3	√	5480 A5: PS	
4	√	1	√
		2	√
5480 A2: MEM			
1	B	5486: CTL	
2	B	1	√
3	B	2	√
4	B	3	√
5	B	4	√
6	B	5	√
7	B	6	√
8	B	7	√
9	√	8	√
10	√	9	√
11	√	10	√
12	√	11	√
13	B	12	√
14	√	13	√
5480 A3: ACC,AR		5487: ANA	
1	√	1	DF
2	√	2	√
3	√	3	√
4	√	4	√
5	√	5	DF
6	√	6	0.5
7	√	7	√
8	√		
9	√		
10	√		
11	√		
12	√		

NEW SIG NAME	HP SIG NAME
F_AVE	SW AVE
F_SUM	SW SUM
F_HGM	SW HIST
F_MCS	SW MCS
F_HFREQ	FREQ HIST
F_HTIME	TIME HIST
X_RUN	L START
X_STOP	L STOP
X_DISP	L DISPLAY
X_RECORD	L RECORD
P_AVE	AVE
P_SUM	SUM
P_HBEG	HGM BEGIN
P_HEND	HGM END
P_MCS	MCS
P_DISP	DISPLAY
P_PREP	PREPARE
SAMPLE_P	SAMPLE
nSAMPLE_P	START
PROCESS_P	PROCESS
NON_PROCESS_P	NON PROCESS
PAR_SET1020	SET PAR
DAR_SET1020	SET DAR
MAR_LD	SET HORIZ
R_MAR_MOD	MOD HOLD
VHR_LD	SET VERT
AR1000	PSD1
AR1020	PSD2
nT0	OUTPUT MPX



- *Resetting the SD Counter both resets the counter FFs and selects Pre-Analysis Delay as the delay period. After the first delay expiration (pre-sample pulse), Sweep Time is selected as the delay period.*

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Section: Timebase
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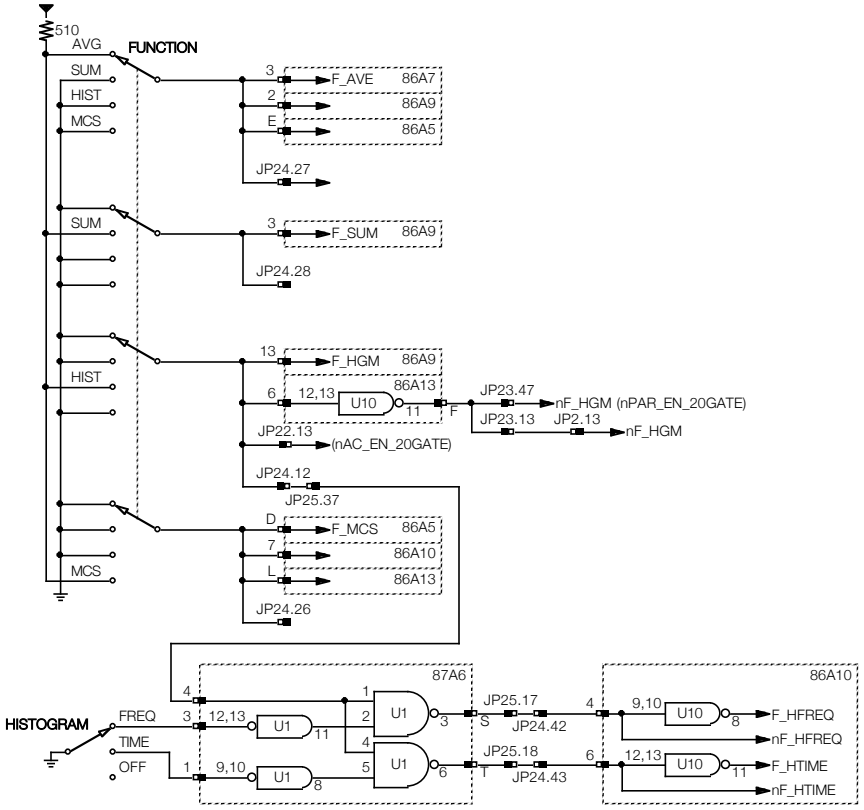

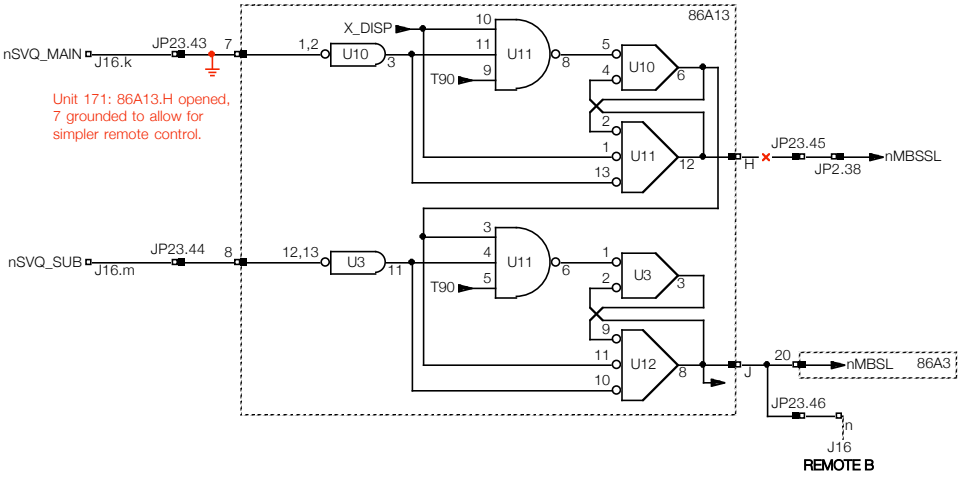

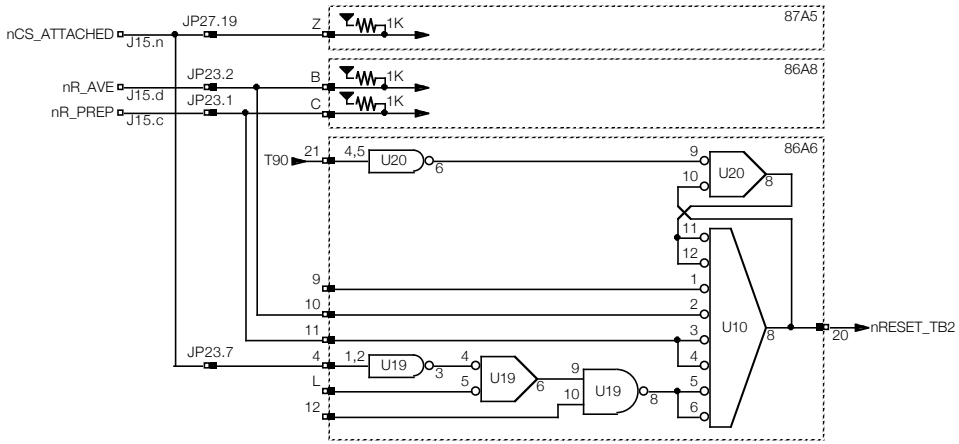

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Section: Function Selection & Remote Control
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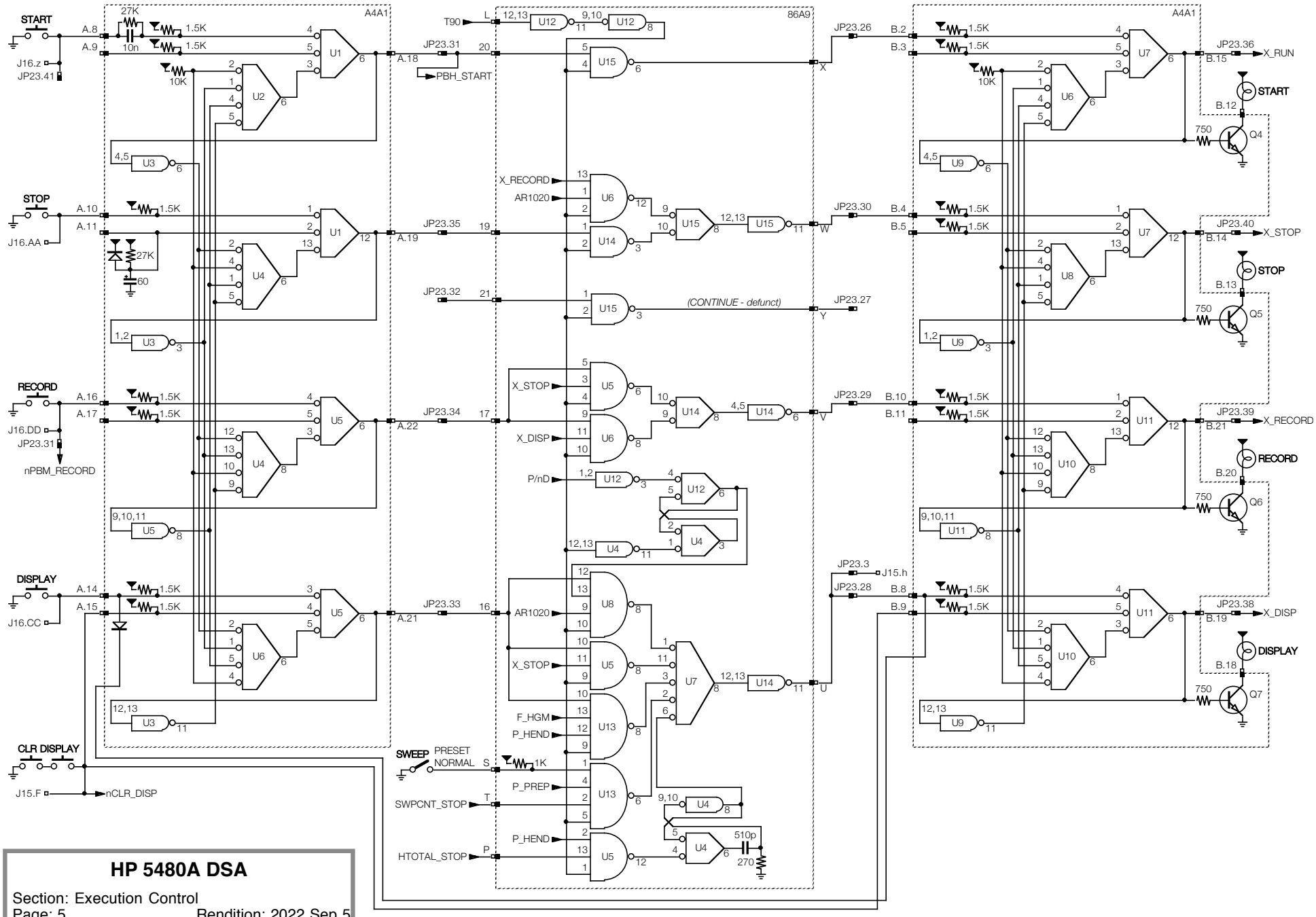

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Section: Execution Control
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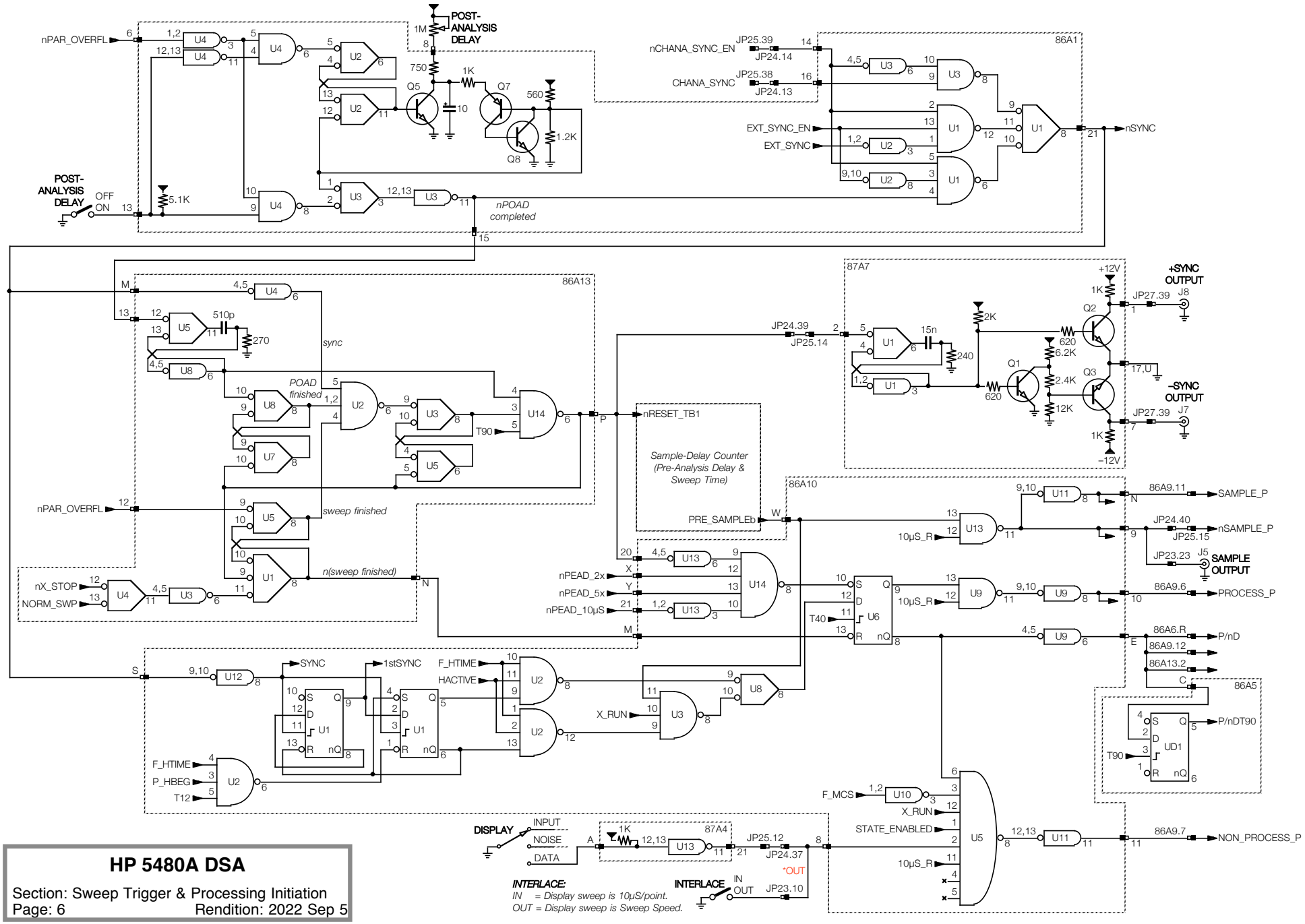

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Section: Sweep Trigger & Processing Initiation
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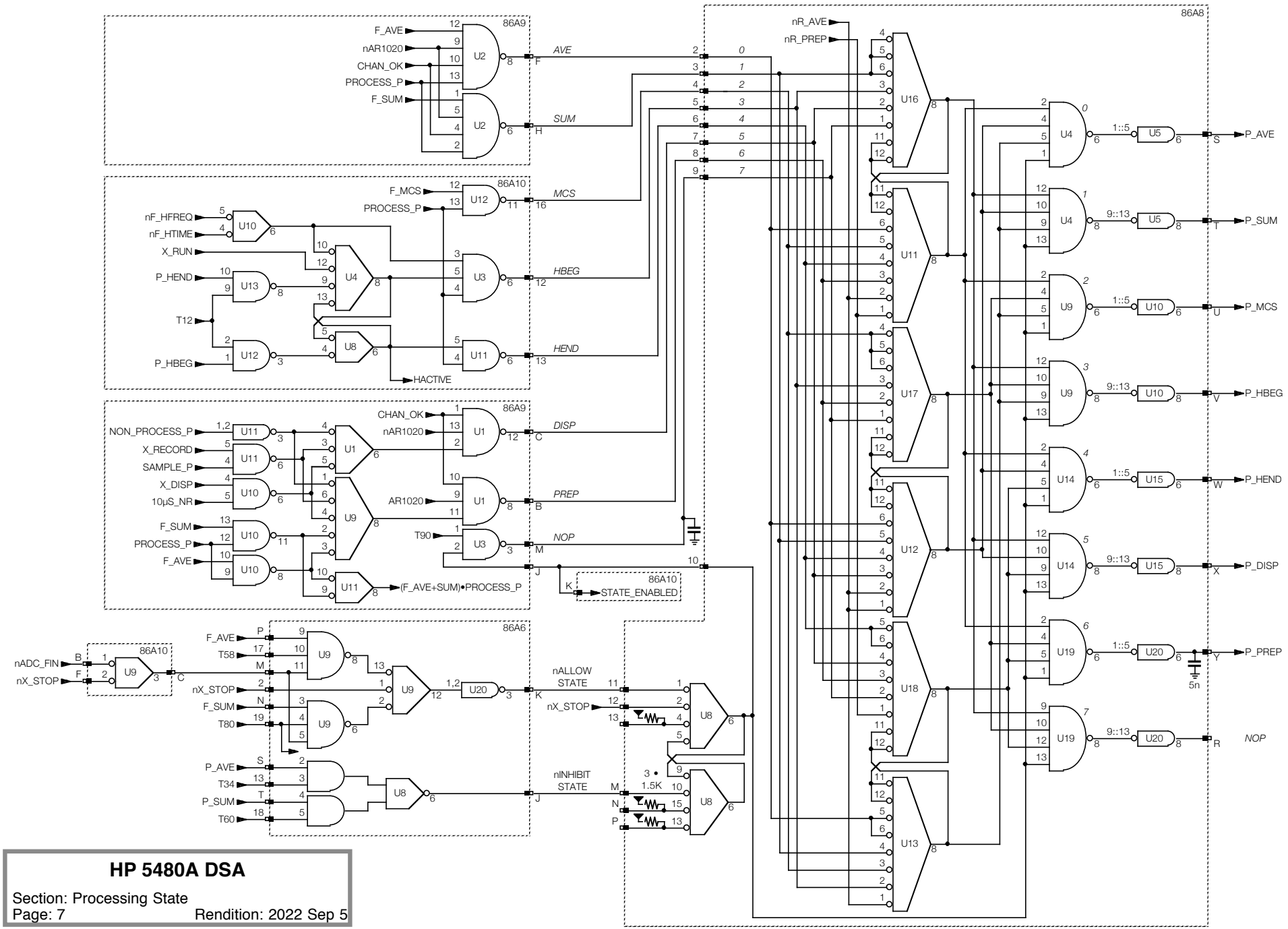

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Section: Processing State
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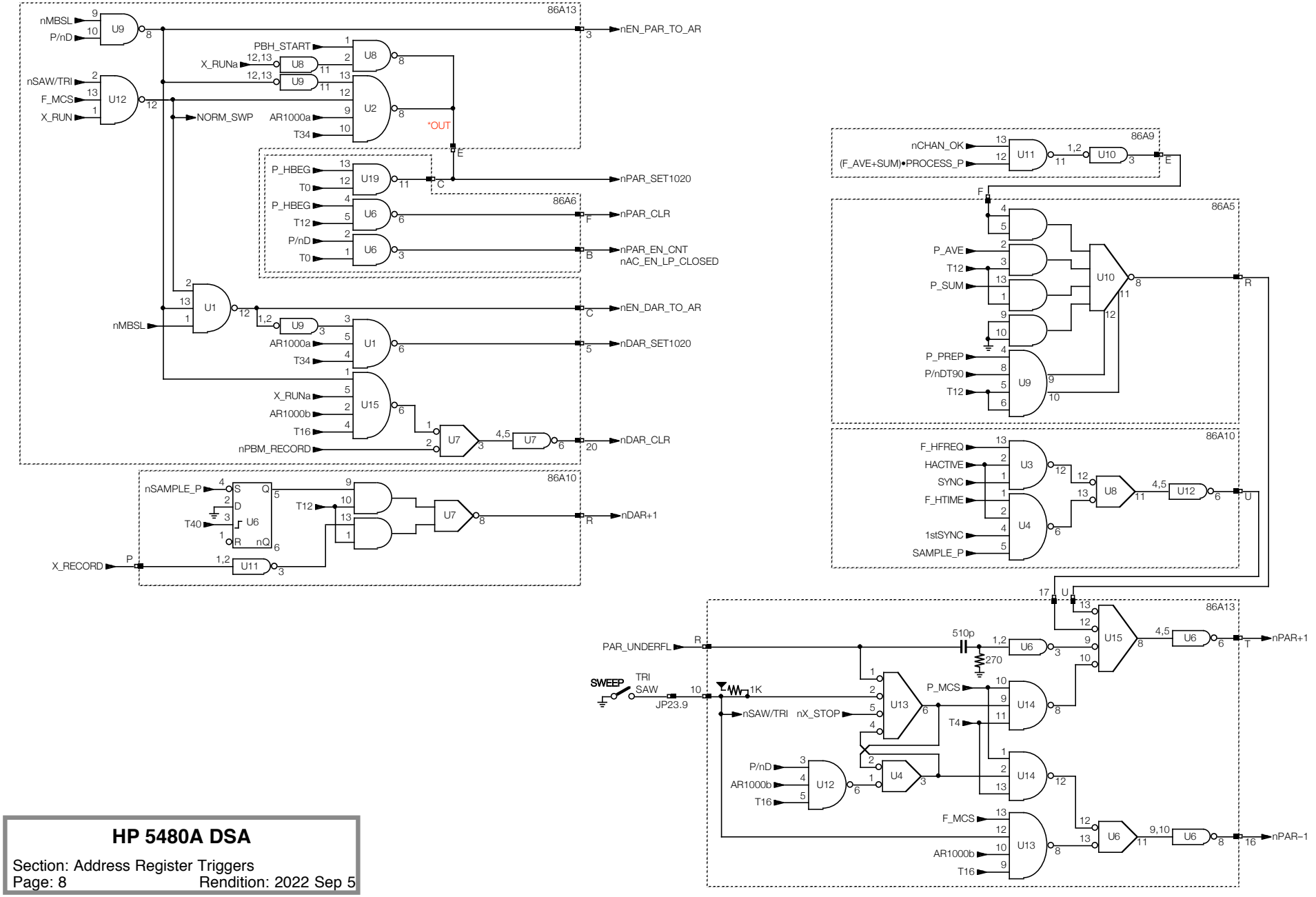

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Section: Address Register Triggers
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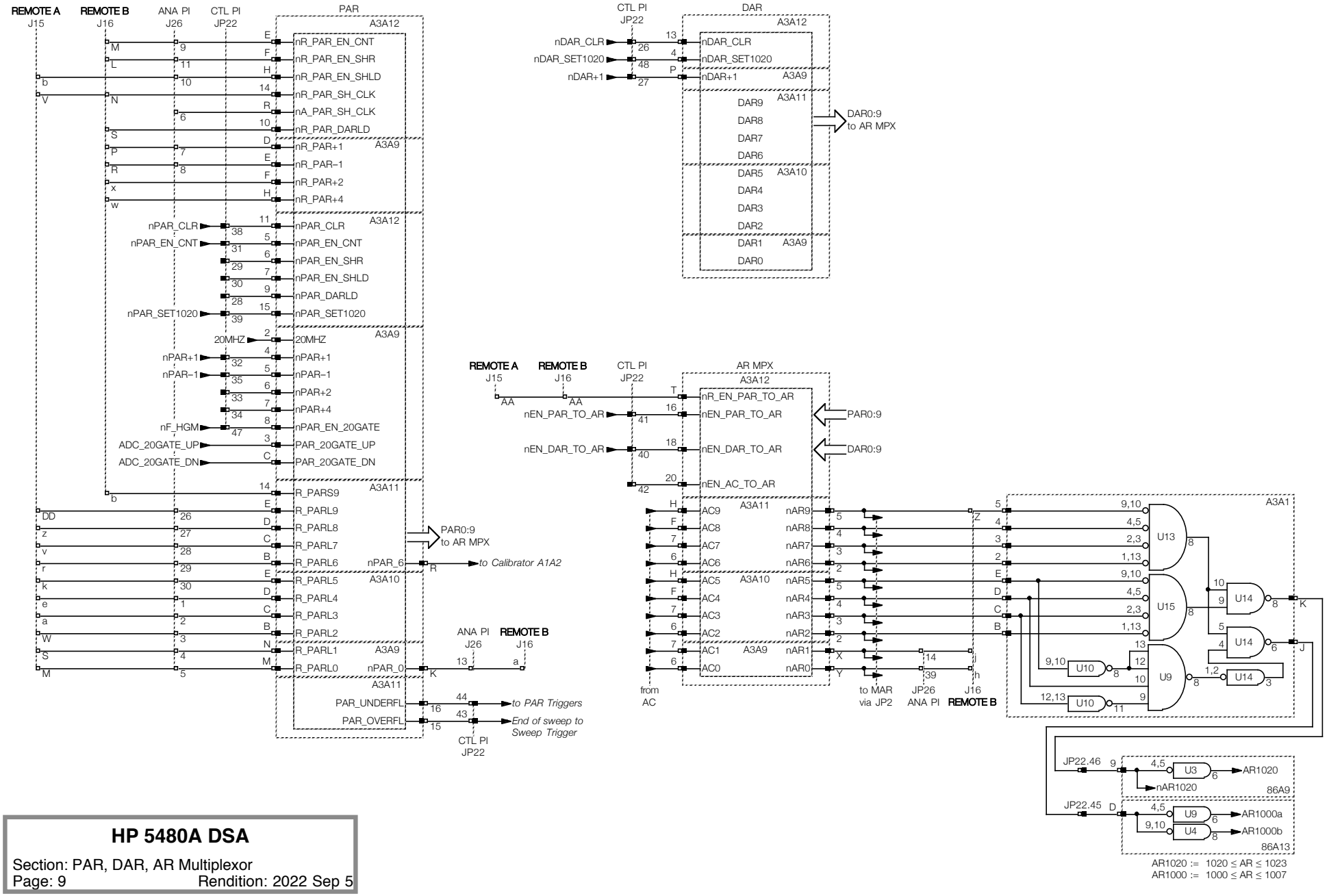

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Section: PAR, DAR, AR Multiplexor
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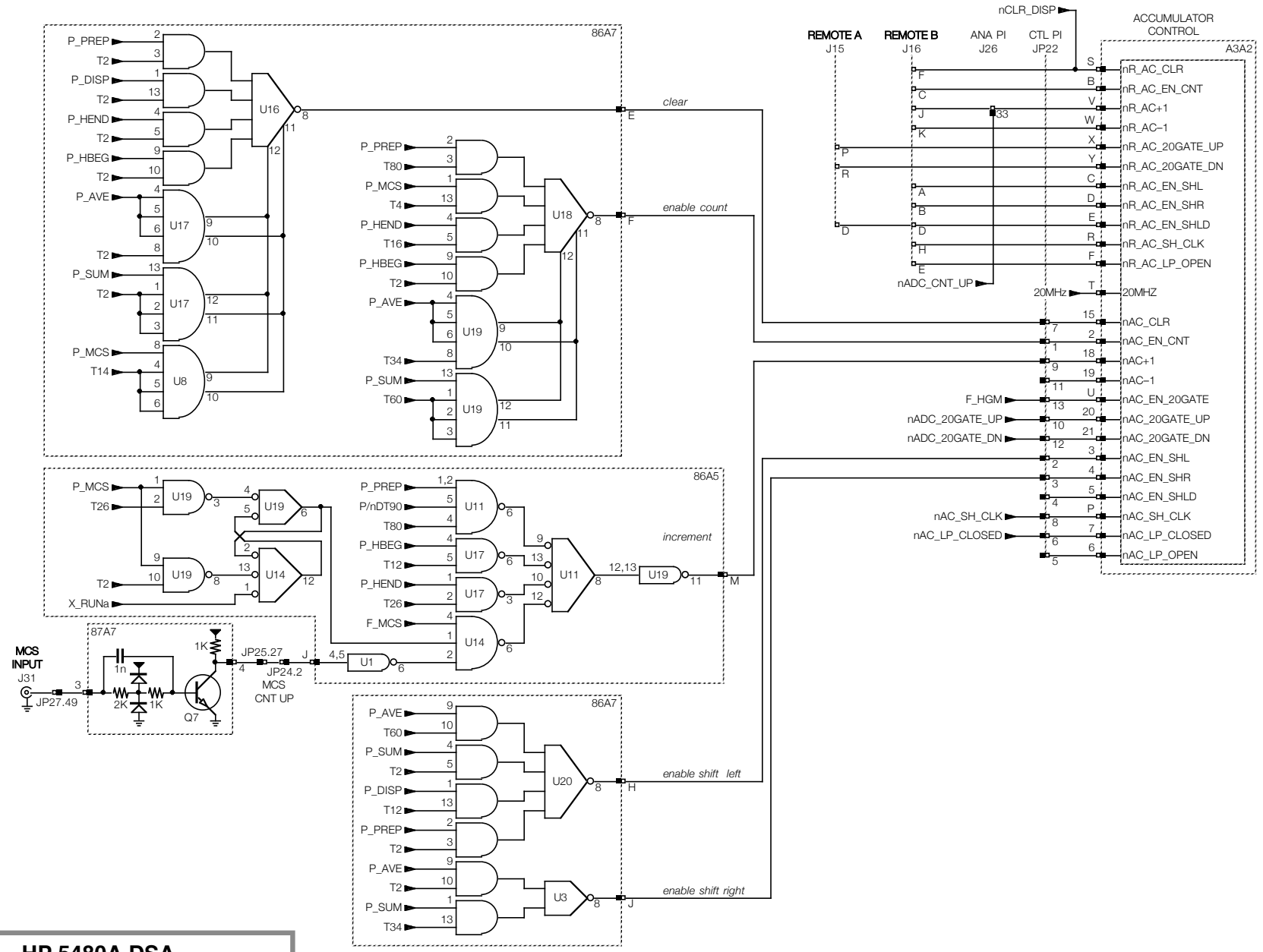

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Section: Accumulator Triggers & Control
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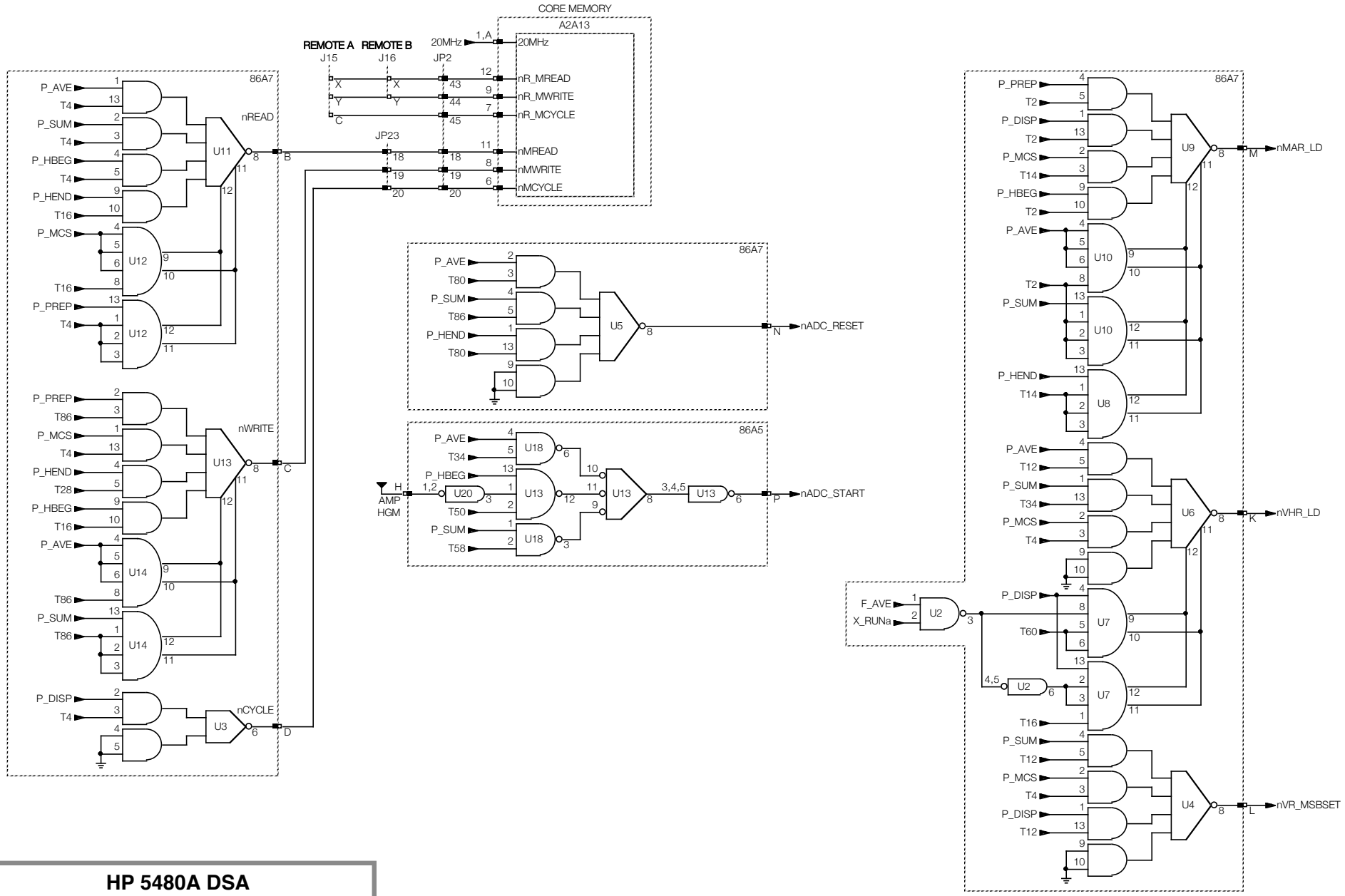

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Section: Memory Control, MAR, ADC, DAC Triggers
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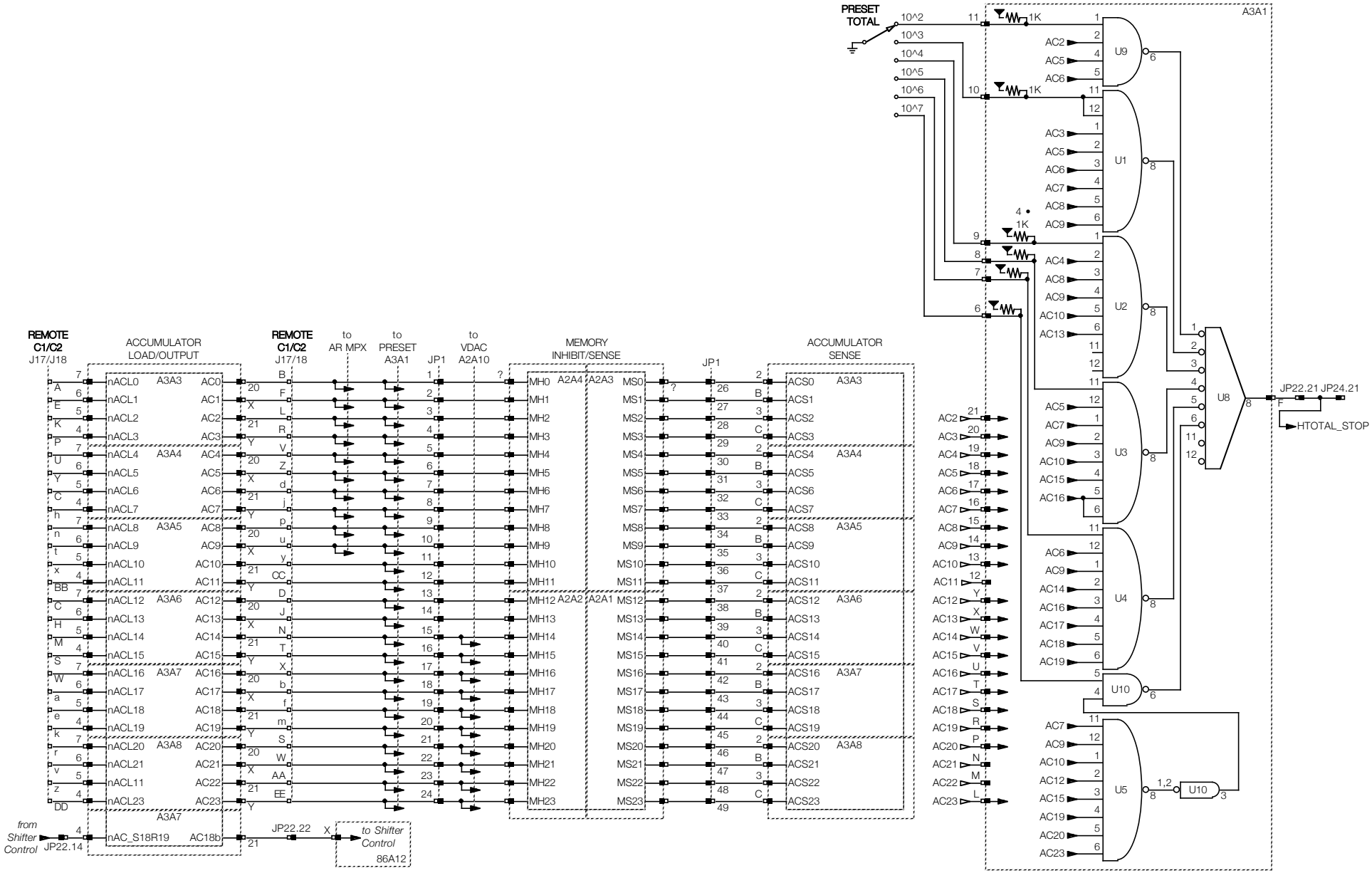

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Section: Accumulator & Memory Data
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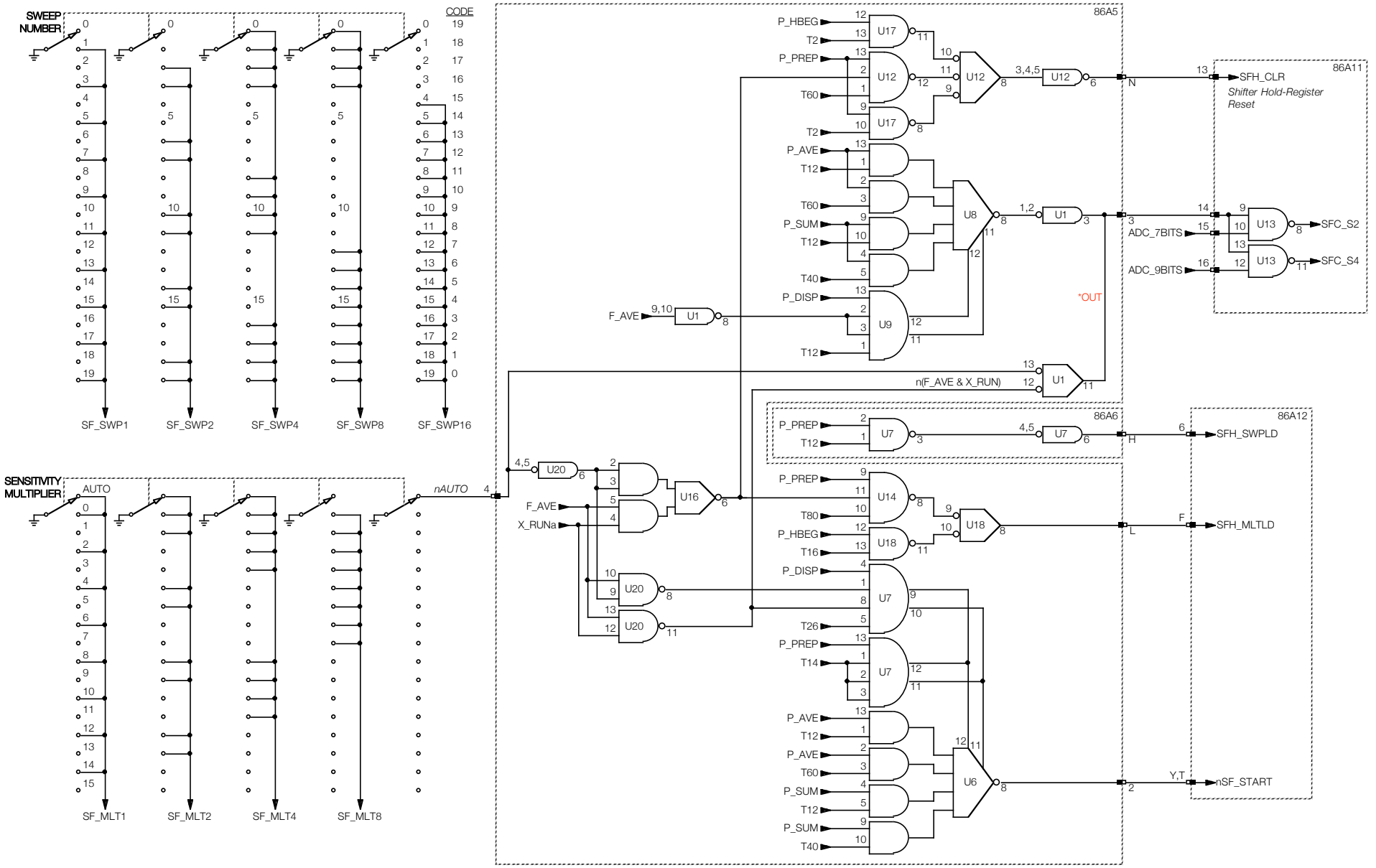

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Section: Shifter Triggers
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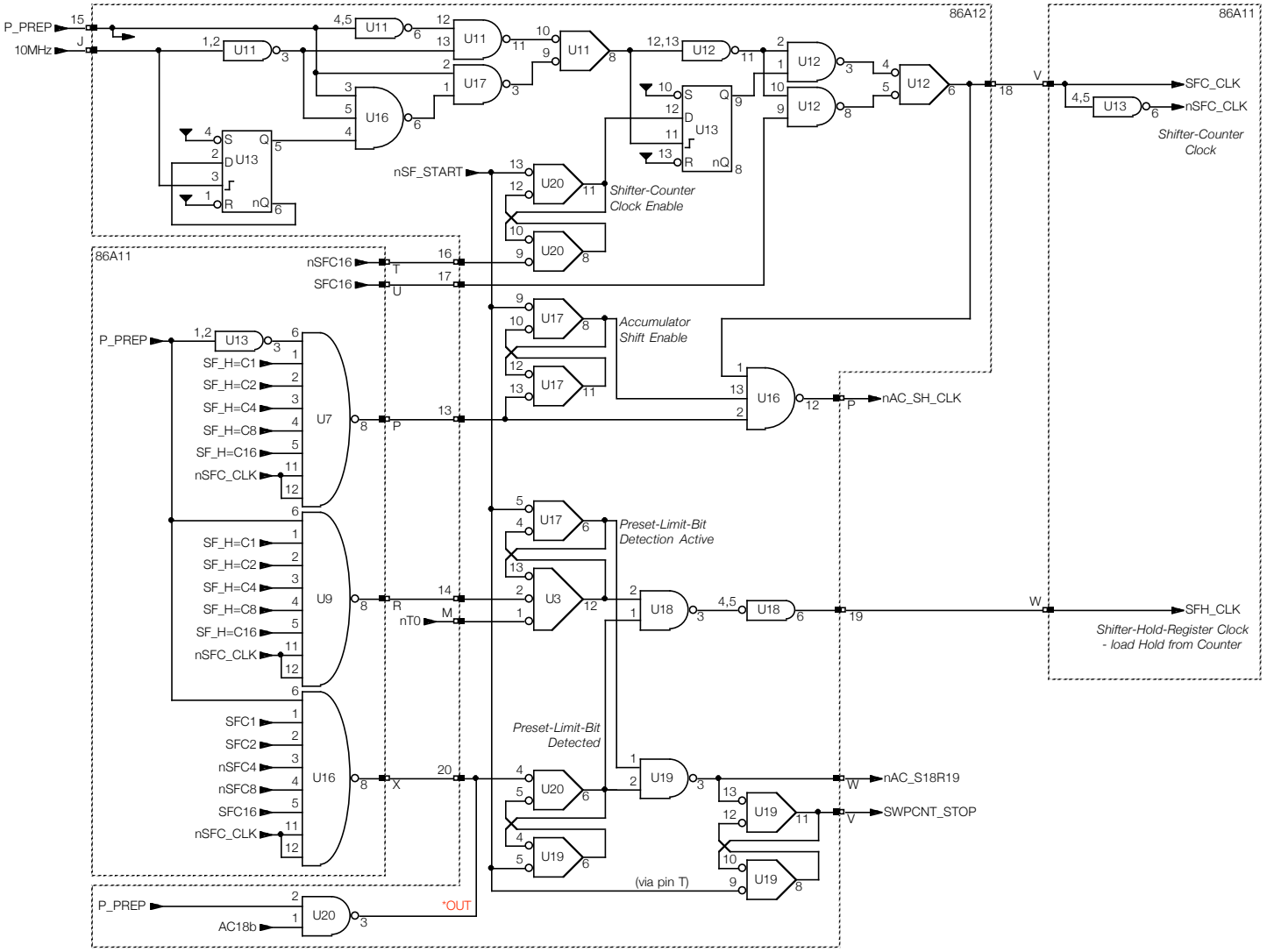

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Section: Shifter Control
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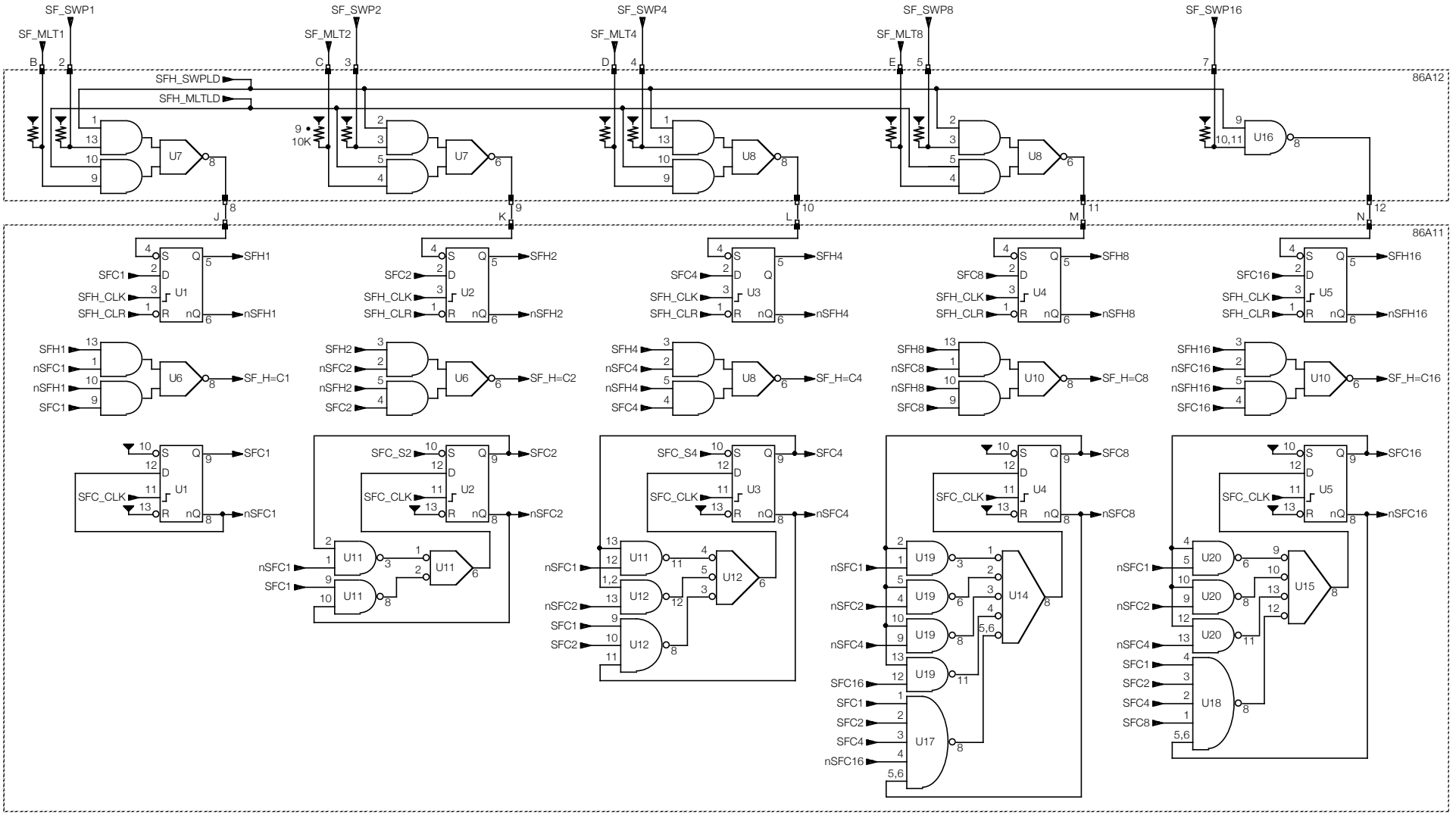

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Section: Shifter Counter & Hold Register
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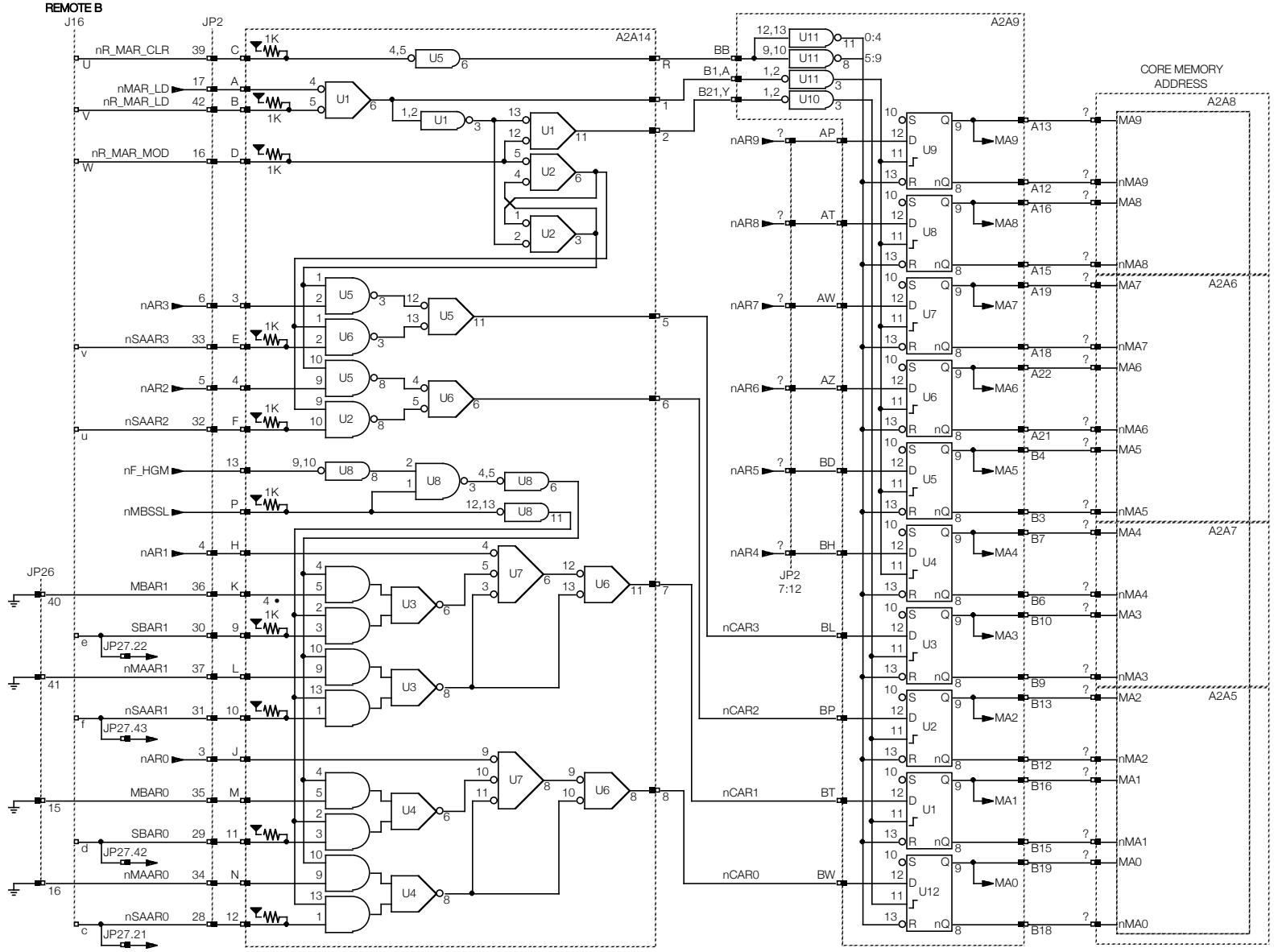

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Section: MAR & Memory Address
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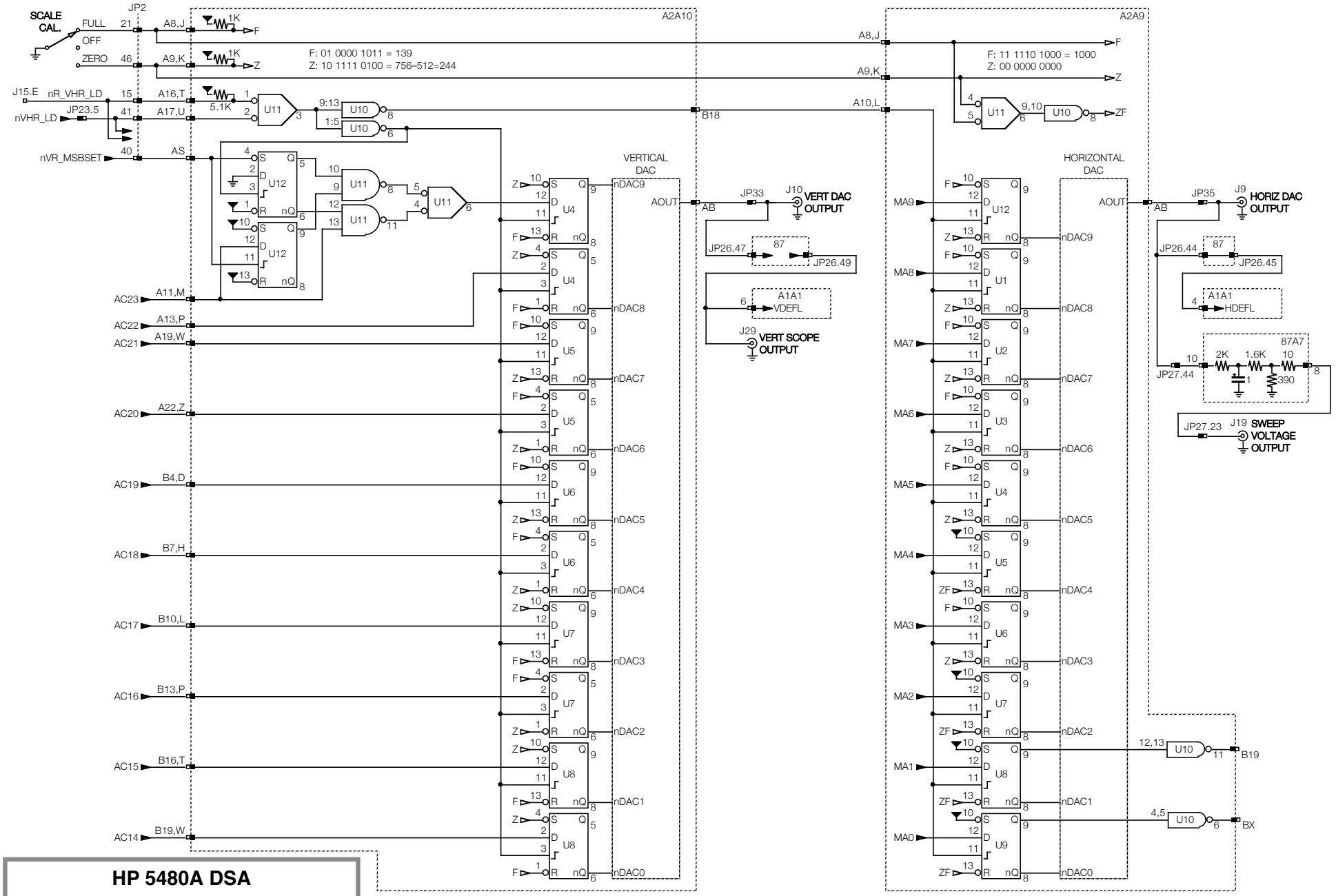

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Section: V, H Registers & DACs
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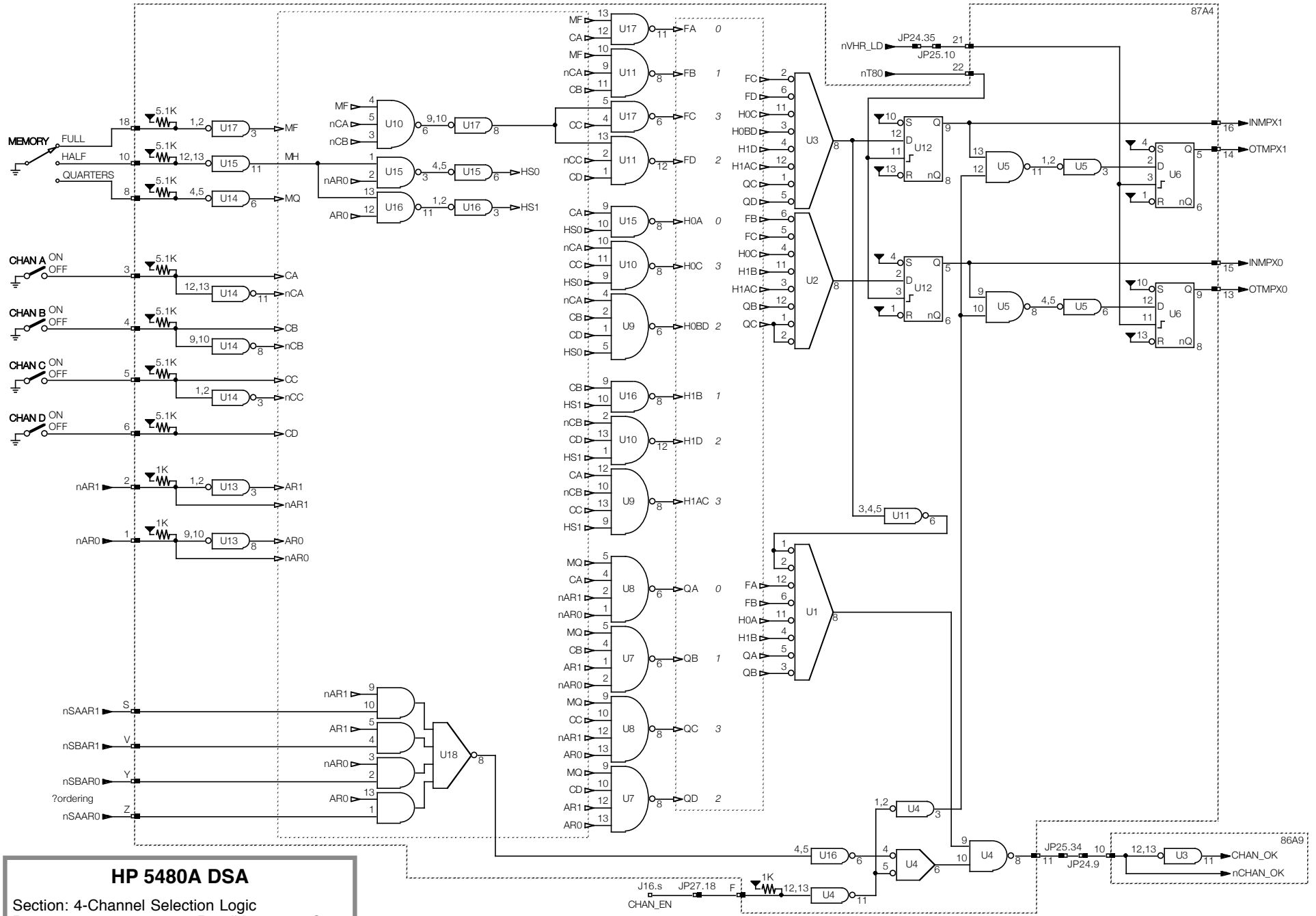

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Section: 4-Channel Selection Logic
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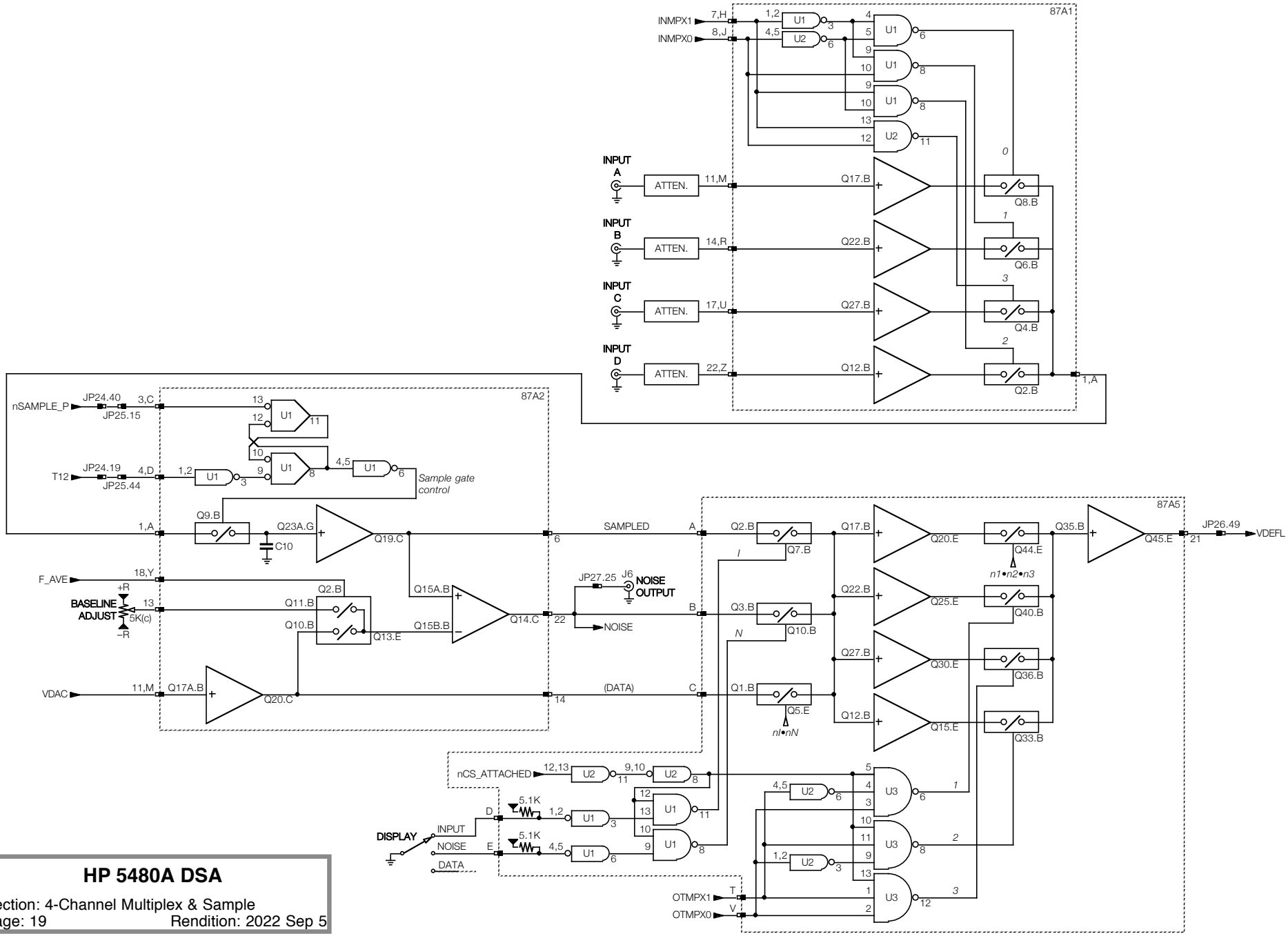

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Section: 4-Channel Multiplex & Sample
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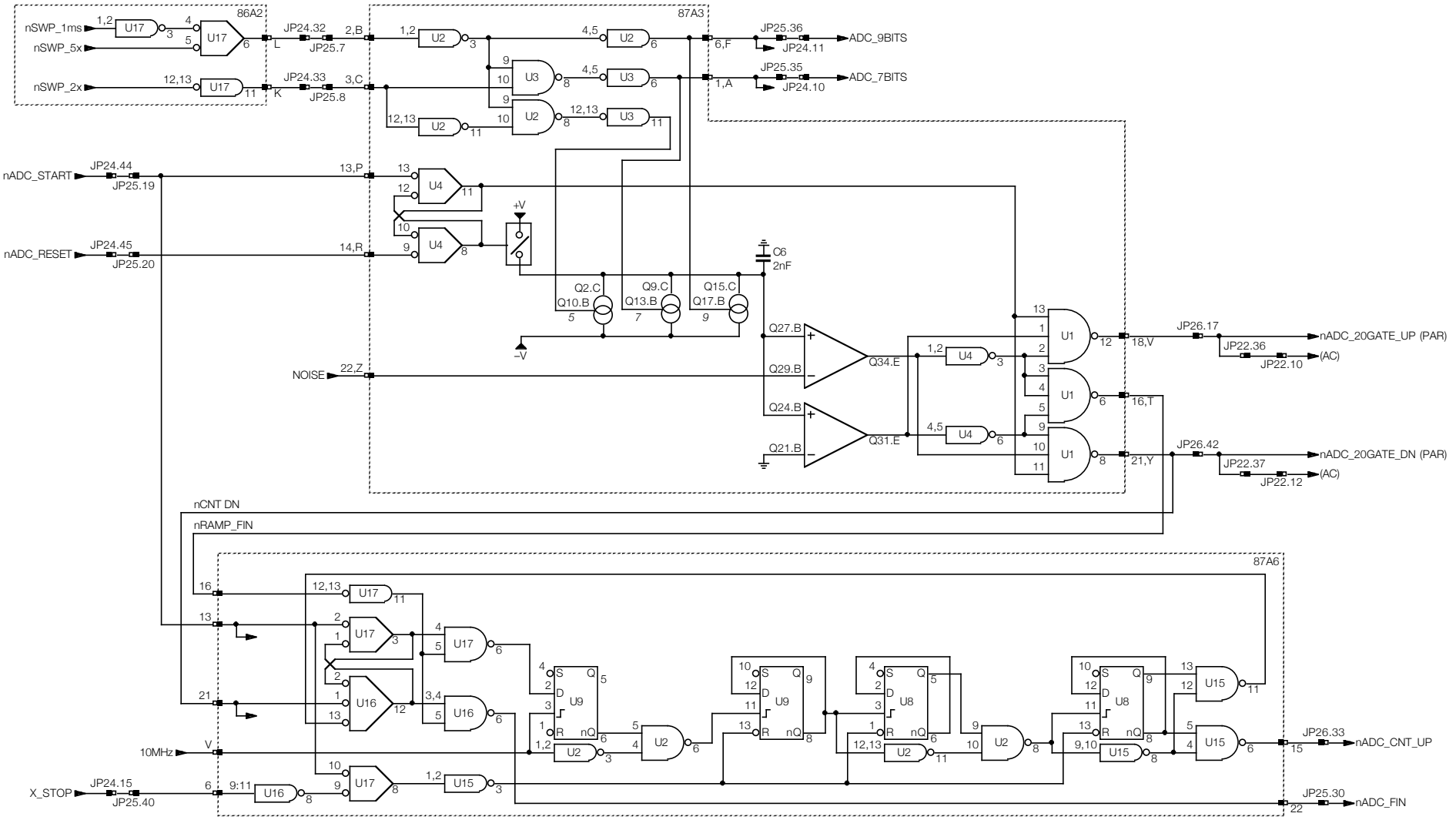

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Section: ADC
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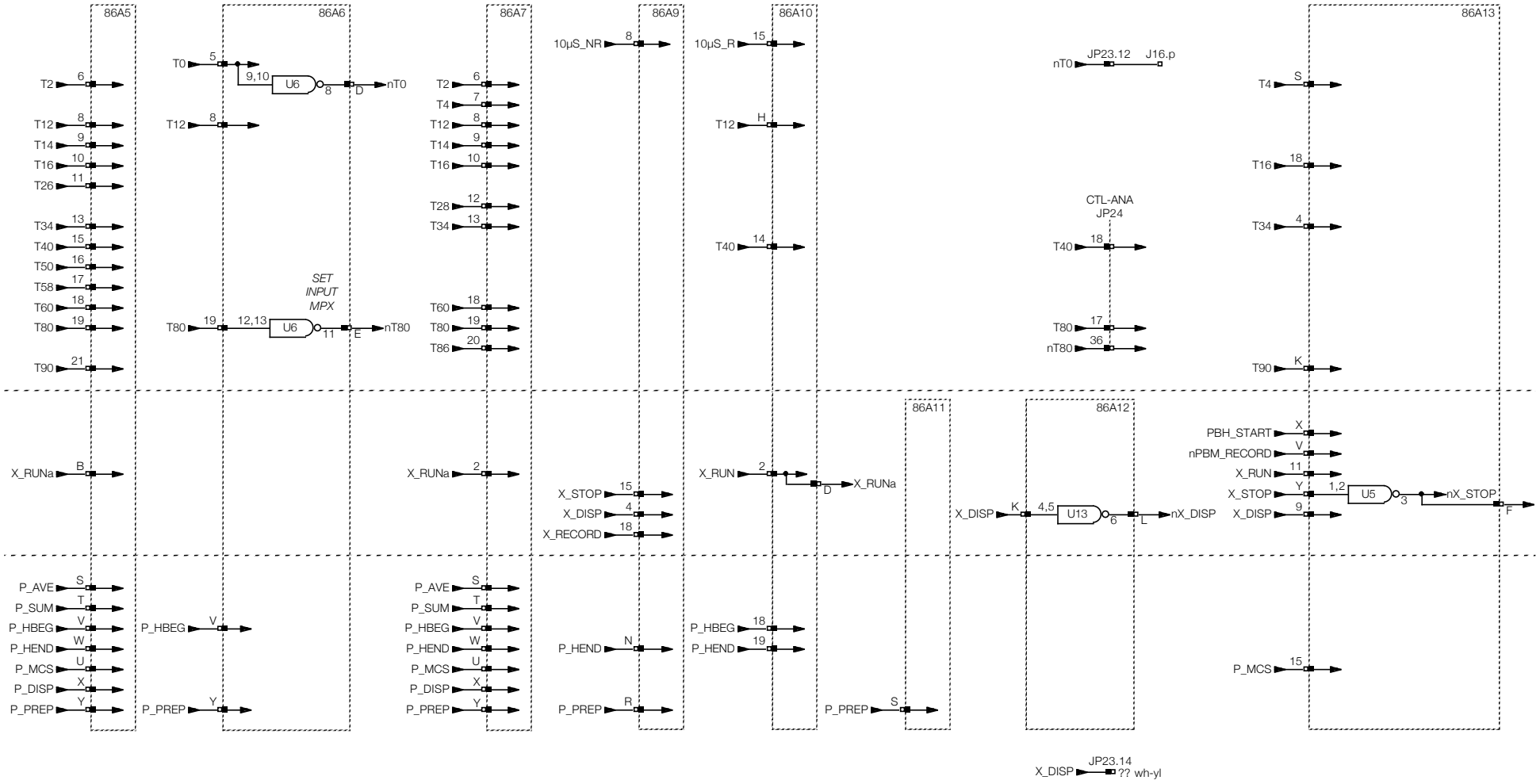

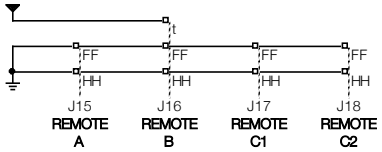

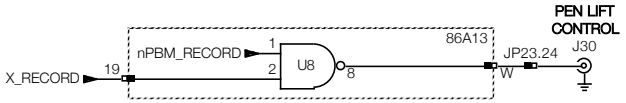

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Section: Misc. Signal Distribution
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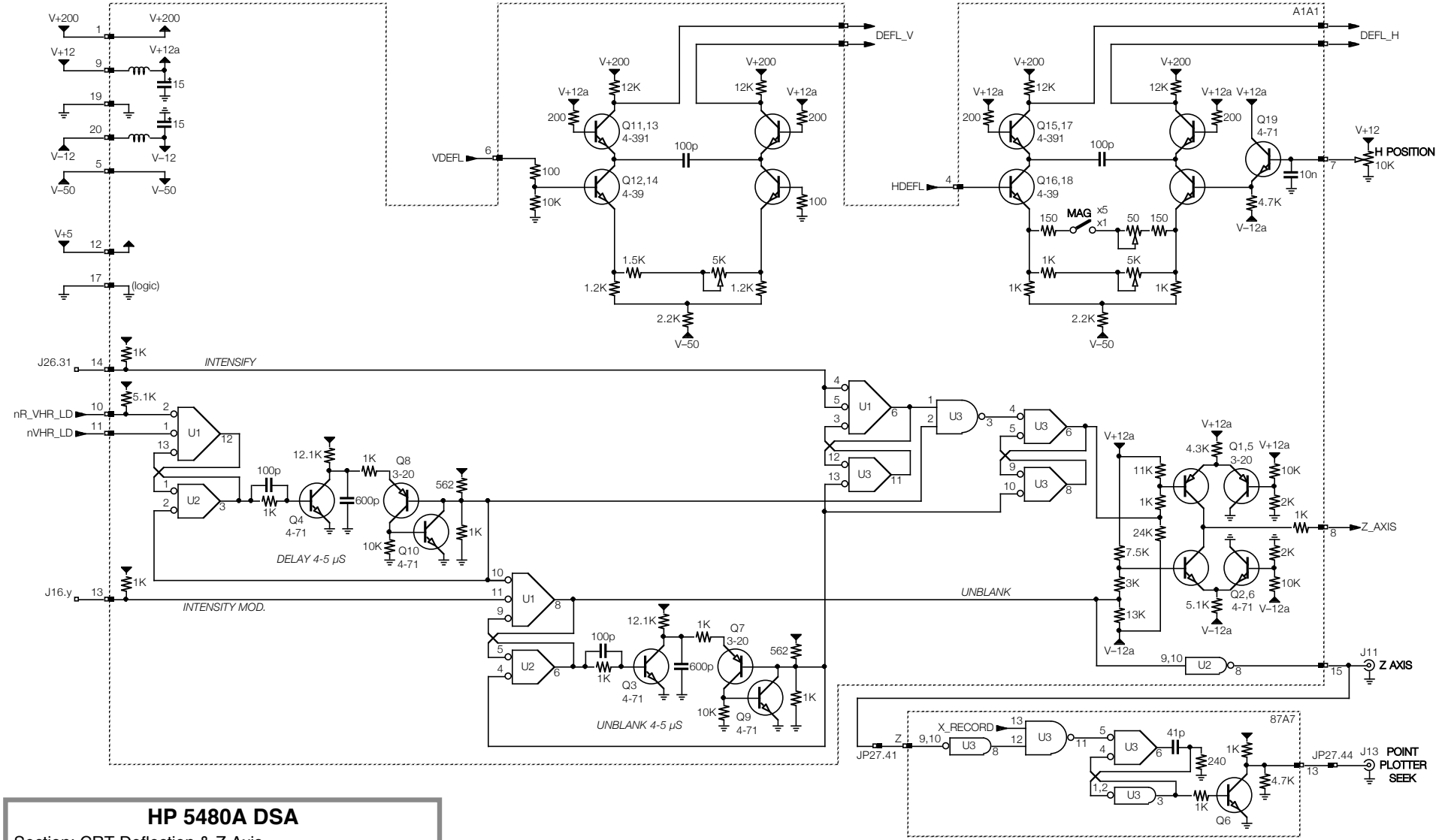

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Section: CRT Deflection & Z Axis

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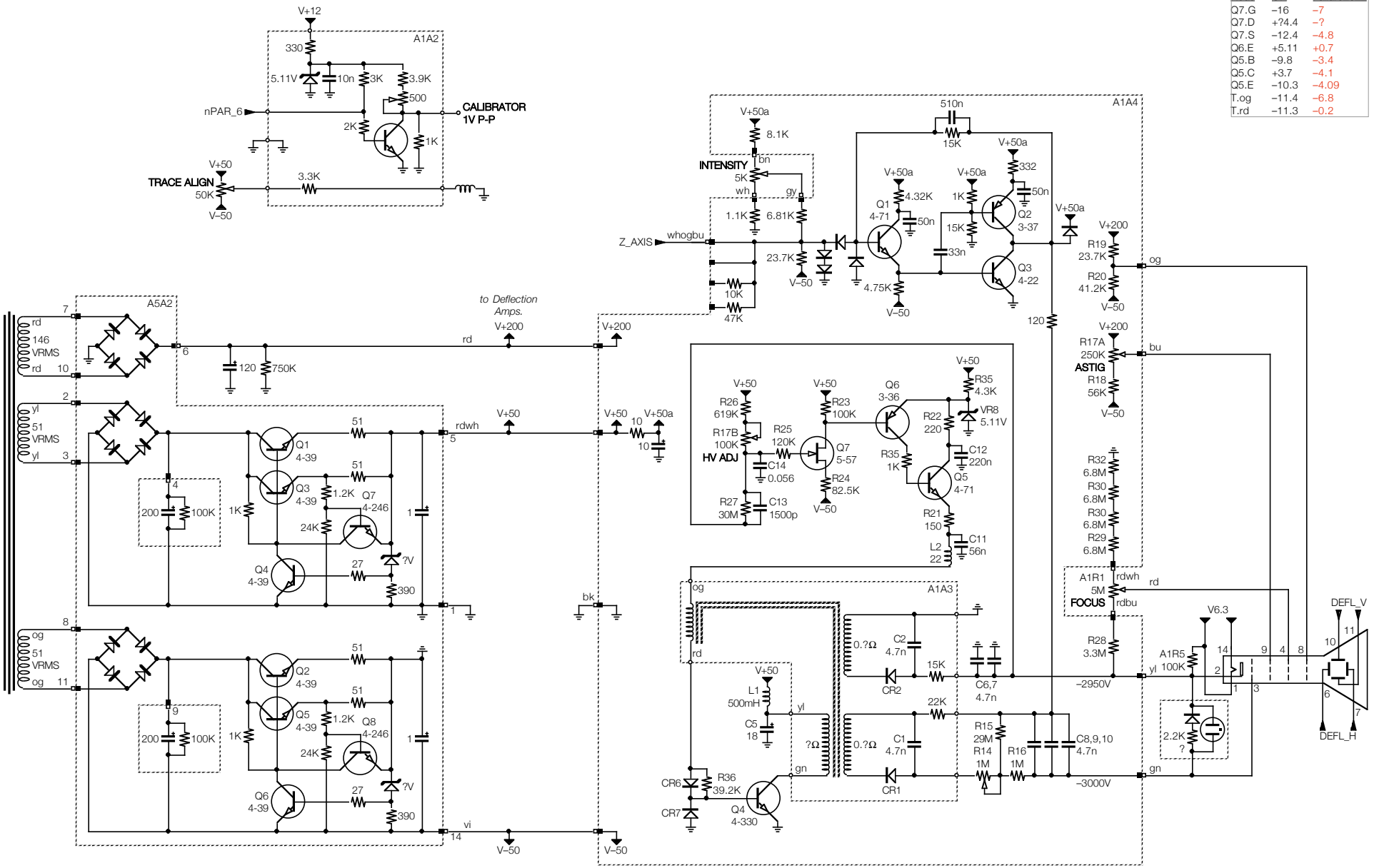
Node	OK	Failure2022
Q7.G	−16	−7
Q7.D	+?4.4	−?
Q7.S	−12.4	−4.8
Q6.E	+5.11	+0.7
Q5.B	−9.8	−3.4
Q5.C	+3.7	−4.1
Q5.E	−10.3	−4.09
T.og	−11.4	−6.8
T.rd	−11.3	−0.2



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Section: CRT Power Supply

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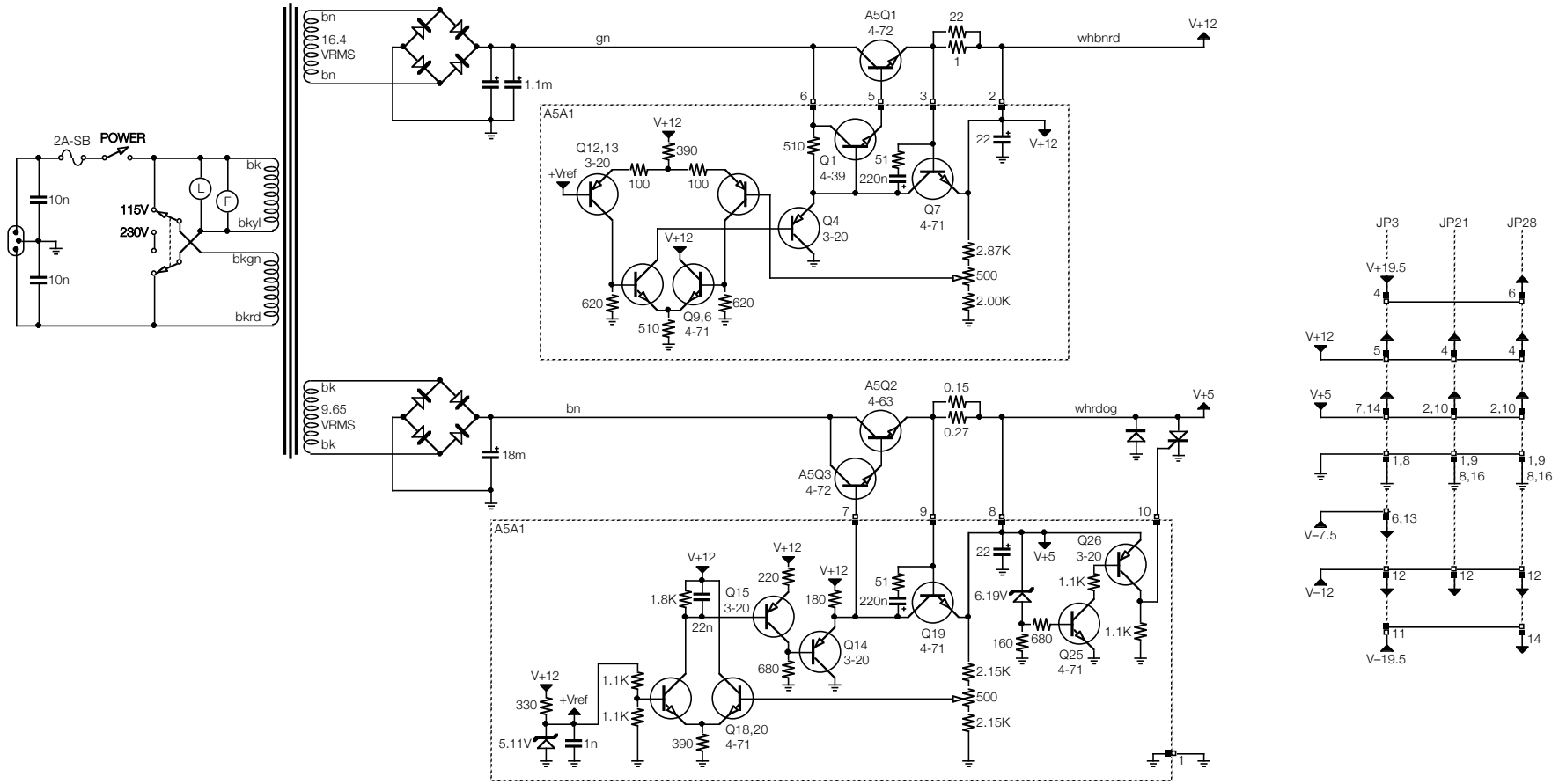
• Date code on one capacitor on A1A4 is 7435.



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Section: Power Supply: V+5, V+12

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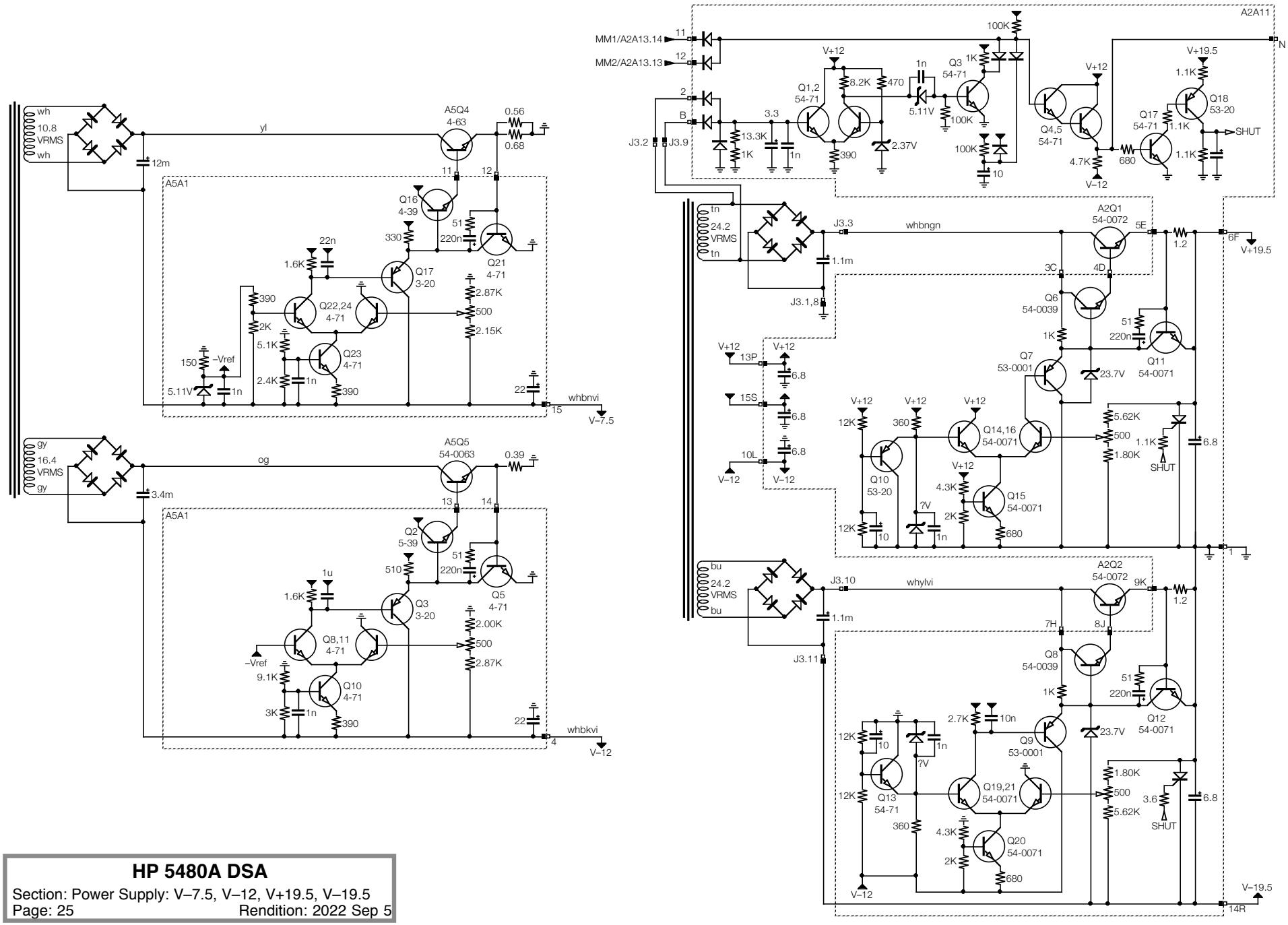

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Section: Power Supply: V–7.5, V–12, V+19.5, V–19.5

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J15 REMOTE A

	1 2 3 4	Signal	I/O
1	A	-	
	B	-	
2	C	nR_MCYCLE	IP
	D	nR_AC_EN_SH_LD	IP
3	E	nR_VHR_LD	IP
	F	nR_AC_CLR	IP
4	H	nR_AC_SH_CLK	IP
	J	-	
5	K	-	
	L	-	
6	M	nR_PARL0	IL
	N	nR_PAR_SH_CLK	IP
7	P	nR_AC_20GATE_UP	IL
	R	nR_AC_20GATE_DN	IL
8	S	nR_PARL1	IL
	T	nR_PAR_CLR	IP
9	U	nR_DAR_SET1020	IP
	V	nR_MAR_LD	IP
10	W	nR_PARL2	IL
	X	nR_MREAD	IP
11	Y	nR_MWRITE	IP
	Z	-	
12	a	nR_PARL3	IL
	b	nR_PAR_EN_SHLD	IP
13	c	nR_PREP	IL
	d	nR_AVE	IL
14	e	nR_PARL4	IL
	f	-	
15	h	nSET_X_DISP	OP
	j	nADC_START	OP
16	k	nR_PARL5	IL
	m	-	
17	n	nCS_ATTACHED	IL
	p	nX_STOP	OL
18	r	nR_PARL6	IL
	s	-	
19	t	-	
	u	-	
20	v	nR_PARL7	IL
	w	-	
21	x	-	
	y	-	
22	z	nR_PARL8	IL
	AA	nR_EN_PAR_TO_AR	
23	BB	-	
	CC	-	
24	DD	nR_PARL9	IL
	EE	-	
25	FF	GND	
	HH	GND	

IL = Input, Level
IP = Input, Pulse
OL= Output, Level

J16 REMOTE B

	1 2 3 4	Signal	I/O
1	A	nR_AC_EN_SHL	IP
	B	nR_AC_EN_SHR	IP
2	C	nR_AC_EN_CNT	IP
	D	nR_AC_EN_SHLD	IP
3	E	nR_AC_EN_LPOPEN	IP
	F	nR_AC_CLR	IP
4	H	nR_AC_SH_CLK	IP
	J	nR_AC+1	IP
5	K	nR_AC-1	IP
	L	nR_PAR_EN_SHR	IP
6	M	nR_PAR_EN_CNT	IP
	N	nR_PAR_SH_CLK	IP
7	P	nR_PAR+1	IP
	R	nR_PAR-1	IP
8	S	nR_EN_PAR_TO_AR	IP
	T	nR_PAR_CLR	IP
9	U	nR_DAR_SET1020	IP
	V	nR_MAR_LD	IP
10	W	nR_MAR_MOD	
	X	nR_MREAD	IP
11	Y	nR_MWRITE	IP
	Z	nAR9	OL
12	a	nPAR0	OL
	b	R_PARS9	IL
13	c	nSAAR0	IL
	d	nSBAR0	IL
14	e	nSBAR1	IL
	f	nSAAR1	IL
15	h	nAR0	OL
	j	nAR1	OL
16	k	nSVQ_MAIN	IL
	m	nSVQ_SUB	IL
17	n	nMBSL	OL
	p	nT0	OP
18	r	nX_DISP	OL
	s	CHAN_EN	IL
19	t	+5V	OL
	u	nSAAR2	IL
20	v	nSAAR3	IL
	w	nR_PAR+4	IP
21	x	nR_PAR+2	IP
	y	INTENS MOD	
22	z	nPBM_START	I/O-P
	AA	nEN_PAR_TO_AR	IP
23	BB	nPBM_STOP	I/O-P
	CC	nPBM_DISPLAY	I/O-P
24	DD	nPBM_RECORD	I/O-P
	EE	nCLR_DISP	I/O-P
25	FF	GND	
	HH	GND	

IL = Input, Level
IP = Input, Pulse
OL= Output, Level

J17,J18 REMOTE C1,C2

	1 2 3 4	Signal	I/O
1	A	nR_ACL0	IL
	B	AC0	OL
2	C	nR_ACL12	IL
	D	AC12	OL
3	E	nR_ACL1	IL
	F	AC1	OL
4	H	nR_ACL13	IL
	J	AC13	OL
5	K	nR_ACL2	IL
	L	AC2	OL
6	M	nR_ACL14	IL
	N	AC14	OL
7	P	nR_ACL3	IL
	R	AC3	OL
8	S	nR_ACL15	IL
	T	AC15	OL
9	U	nR_ACL4	IL
	V	AC4	OL
10	W	nR_ACL16	IL
	X	AC16	OL
11	Y	nR_ACL5	IL
	Z	AC5	OL
12	a	nR_ACL17	IL
	b	AC17	OL
13	c	nR_ACL6	IL
	d	AC6	OL
14	e	nR_ACL18	IL
	f	AC18	OL
15	h	nR_ACL7	IL
	j	AC7	OL
16	k	nR_ACL19	IL
	m	AC19	OL
17	n	nR_ACL8	IL
	p	AC8	OL
18	r	nR_ACL20	IL
	s	AC20	OL
19	t	nR_ACL9	IL
	u	AC9	OL
20	v	nR_ACL21	IL
	w	AC21	OL
21	x	nR_ACL10	IL
	y	AC10	OL
22	z	nR_ACL22	IL
	AA	AC22	OL
23	BB	nR_ACL11	IL
	CC	AC11	OL
24	DD	nR_ACL23	IL
	EE	AC23	OL
25	FF	GND	
	HH	GND	

IL = Input, Level
OL= Output, Level

JP1 A2 Memory <=> Mainframe

P J		50 25		J P	
		49 24			
		48 23			
		47 22			
SCALE CAL ZERO	C C	46 21	C C		SCALE CAL FULL
nR_MCYCLE	C C	45 20	C C		nMCYCLE
nR_MWRITE	C C	44 19	C C		nMWRITE
nR_MREAD	C C	43 18	C C		nMREAD
nR_MAR_LD	C C	42 17	C C		nMAR_LD
nVHR_LD	C C	41 16	C C		nR_MAR_MOD
nVR_MSBSET	C C	40 15	C C		nR_VHR_LD
nR_MAR_CLR	C C	39 14			
nMBSSL	C C	38 13	C C		nF_HGM
nMAAR1	C C	37 12	C C		nAR?
MBAR1	C C	36 11	C C		nAR?
MBAR0	C C	35 10	C C		nAR?
nMAAR0	C C	34 9	C C		nAR?
nSAAR3	C C	33 8	C C		nAR?
nSAAR2	C C	32 7	C C		nAR?
nSAAR1	C C	31 6	C C		nAR3
SBAR1	C C	30 5	C C		nAR2
SBAR0	C C	29 4	C C		nAR1
nSAAR0	C C	28 3	C C		nAR0
		27 2			
		26 1			

JP2 A2 Memory <=> Mainframe

P J		50 25		J P	
		49 24			
		48 23			
		47 22			
ACS23	C C	49 24	C C		AC23
ACS22	C C	48 23	C C		AC22
ACS21	C C	47 22	C C		AC21
ACS20	C C	46 21	C C		AC20
ACS19	C C	45 20	C C		AC19
ACS18	C C	44 19	C C		AC18
ACS17	C C	43 18	C C		AC17
ACS16	C C	42 17	C C		AC16
ACS15	C C	41 16	C C		AC15
ACS14	C C	40 15	C C		AC14
ACS13	C C	39 14	C C		AC13
ACS12	C C	38 13	C C		AC12
ACS11	C C	37 12	C C		AC11
ACS10	C C	36 11	C C		AC10
ACS9	C C	35 10	C C		AC9
ACS8	C C	34 9	C C		AC8
ACS7	C C	33 8	C C		AC7
ACS6	C C	32 7	C C		AC6
ACS5	C C	31 6	C C		AC5
ACS4	C C	30 5	C C		AC4
ACS3	C C	29 4	C C		AC3
ACS2	C C	28 3	C C		AC2
ACS1	C C	27 2	C C		AC1
ACS0	C C	26 1	C C		AC0

JP22	CTL <=> A3 (AC & ARs)						
	P	J			J	P	
GND	G	G	50	25	G	G	GND
-	-	-	49	24	C	C	20MHz
nDAR_SET1020	C	C	48	23	-	-	-
nPAR_EN_20GATE	C	C	47	22	C	C	AC18b
nAR1020	C	C	46	21	C	C	HTOTAL_STOP
nAR1000	C	C	45	20	C	C	HTOTAL_7
nPAR_20GATE_DN	C	C	44	19	C	C	HTOTAL_6
nPAR_20GATE_UP	C	C	43	18	C	C	HTOTAL_5
nAC_TO_AR	-	C	42	17	C	C	HTOTAL_4
nPAR_TO_AR	C	C	41	16	C	C	HTOTAL_3
nDAR_TO_AR	C	C	40	15	C	C	HTOTAL_2
nPAR_SET1020	C	C	39	14	C	C	nAC_S18C19
nPAR_CLR	C	C	38	13	C	C	nAC_EN_20GATE
nADC_20GATE_DN	C	C	37	12	C	C	nAC_20GATE_DN
nADC_20GATE_UP	C	C	36	11	C	-	nAC-1
nPAR-1	C	C	35	10	C	C	nAC_20GATE_UP
nPAR+4	-	C	34	9	C	C	nAC+1
nPAR+2	-	C	33	8	C	C	nAC_SH_CLK
nPAR+1	C	C	32	7	C	C	nAC_CLR
nPAR_EN_CNT	C	C	31	6	C	C	nAC_LOOP_CLOSED
nPAR_EN_SHLD	-	C	30	5	C	-	nAC_LP_OPEN
nPAR_EN_SHR	-	C	29	4	C	-	nAC_EN_SHLD
nPAR_DARLD	-	C	28	3	C	C	nAC_EN_SHR
nDAR+1	C	C	27	2	C	C	nAC_EN_SHL
nDAR_CLR	C	C	26	1	C	C	nAC_EN_CNT

JP23	CTL <=> Mainframe, Rear						
	P	J			J	P	
GND	G	G	50	25	G	G	GND
-	-	-	49	24	C	C	PEN_LIFTER
-	-	-	48	23	C	C	nSAMPLE_P
PBM_RECORD	C	C	47	22	-	-	-
nMBSL	C	C	46	21	-	-	-
nMBSSL	C	C	45	20	C	C	nMCYCLE
nSVQ_SUB	C	C	44	19	C	C	nMWRITE
nSVQ_MAIN	C	C	43	18	C	C	nMREAD
(to 86A6.3 n.c.)	C	-	42	17	C	C	nMAR_LD
PBM_START	-	C	41	16	C	C	nSWP_EXT
X_STOP	C	C	40	15	-	-	-
X_RECORD	C	C	39	14	C	C	X_DISP
X_DISP	C	C	38	13	C	C	nF_HGM
(L CONTINUE)	C	C	37	12	C	C	nT0
X_START	C	C	36	11	C	C	nX_DISPLAY
PBH_STOP	C	C	35	10	C	C	DISP_DEFEAT
PBH_RECORD	C	C	34	9	C	C	nSAW/TRI
PBH_DISP	C	C	33	8	C	C	X_STOP
(PBH CONTINUE)	C	-	32	7	C	C	nCS_ATTACHED
PBH_START	C	C	31	6	C	C	nADC_START
nSET_X_STOP	C	C	30	5	C	C	nVHR_LD
nSET_X_RECORD	C	C	29	4	C	C	nVR_SETMSB
nSET_X_DISP	C	C	28	3	C	C	nSET_X_DISP
(nSET_CONTINUE)	C	-	27	2	C	C	nR_AVE
nSET_X_START	C	C	26	1	C	C	nR_PREP

JP24, JP25	CTL <=> ANA								
			5		4	4		5	
GND	G	25	G	50	25	G	50	G	GND
-	-	24	-	49	24	-	49	-	-
-	-	23	-	48	23	-	48	-	-
-	-	22	-	47	22	-	47	-	-
-	-	21	-	46	21	C	46	-	HTOTAL_STOP
nADC_RESET	C	20	C	45	20	-	45	-	-
nADC_START	C	19	C	44	19	C	44	C	T12
nF_HTIME	C	18	C	43	18	C	43	-	T40
nFHFREQ	C	17	C	42	17	C	42	-	T80
(nAMP_HIST)	-	16	C	41	16	C	41	C	10MHz
nSAMPLE_P	C	15	C	40	15	C	40	C	X_STOP
nRESET_TB1	C	14	C	39	14	C	39	-	nCHAN_A_SYNC
-	-	13	-	38	13	C	38	-	CHAN_A
DISP_DEFEAT	C	12	C	37	12	C	37	C	F_HGM
nT80	C	11	C	36	11	C	36	C	ADC_9BITS
nVHR_LD	C	10	C	35	10	C	35	C	ADC_7BITS
nX_STOP	-	9	C	34	9	C	34	C	nCHAN_OK
SWP_2x	C	8	C	33	8	-	33	-	-
SWP_5x+n1mS	C	7	C	32	7	-	32	-	-
nSWP_EXT	-	6	C	31	6	-	31	-	-
X_DISP	-	5	C	30	5	C	30	C	nADC_FIN
-	-	4	-	29	4	-	29	-	-
F_SUM	-	3	C	28	3	-	28	-	-
F_AVE	C	2	C	27	2	C	27	C	MCS_CNT_UP
F_MCS	-	1	C	26	1	C	26	C	PRE_SAMPLE_EXT

JP21 CTL Power			
GND	16	8	GND
-	15	7	-
-	14	6	-
-	13	5	-
-12V	12	4	+12V
-	11	3	LINE SYNC
+5V	10	2	+5V
GND	9	1	GND

JP28 ANA Power			
GND	16	8	GND
-	15	7	-
-19.5V	14	6	+19.5V
-	13	5	-
-12V	12	4	+12V
-	11	3	-
+5V	10	2	+5V
GND	9	1	GND

JP3 MEM Power			
V+5	14	7	V+5
V-7.5	13	6	V-7.5
V-12	12	5	V+12
V-19.5	11	4	V+19.5
-19.5 +UNREG	10	3	+19.5 +UNREG
PFSENSE	9	2	PFSENSE
GND	8	1	GND

JP26	ANA <=> A3 (AC &ARs)						
	P	J			J	P	
GND	G		50	25		G	GND
VDEFL	C		49	24		G	GND
	-		48	23		G	GND
VDAC	C		47	22		G	GND
GND	G		46	21		G	GND
	-		45	20		G	GND
HDAC	C		44	19		G	GND
GND	G		43	18		G	GND
nADC_20GATE_DN	C		42	17		C	nADC_20GATE_UP
nMAAR1	C		41	16		C	nMAAR0
MBAR1	G		40	15		G	MBAR0
nAR0	C		39	14		C	nAR1
	-		38	13		-	nPAR0
AC23 ??	-		37	12		-	
	-		36	11		-	nR_PAR_EN_SHR
	-		35	10		-	nR_PAR_EN_SHLD
	-		34	9		-	nR_PAR_EN_CNT
nR_AC+1	C		33	8		-	nR_PAR-1
	-		32	7		-	nR_PAR+1
	-		31	6		-	nA_PAR_SH_CLK
R_PARL9	-	C	30	5	C	-	R_PARL0
R_PARL8	-	C	29	4	C	-	R_PARL1
R_PARL7	-	C	28	3	C	-	R_PARL2
R_PARL6	-	C	27	2	C	-	R_PARL3
R_PARL5	-	C	26	1	C	-	R_PARL4

JP27	ANA <=> Mainframe, Rear						
	P	J			J	P	
GND	G		50	25	G	G	GND
MCS_INPUT	C		49	24		-	
	-		48	23		C	SWP_VOLTAGE
	-		47	22		C	nSBAR1
VARIANCE	C		46	21		C	nSAAR0
PLOT	C		45	20		-	
SEEK	C		44	19		C	nCS_ATTACHED
nSAAR1	C		43	18		C	CHAN_EN
nSBAR0	C		42	17		-	
Z_AXIS_L	C		41	16		-	
X_RECORD	C		40	15		C	R_SAMPLE
SYNC_OUT_POS	C		39	14		C	SYNC_OUT_NEG
	-		38	13		-	
J12.24	-	C	37	12	C	-	J12.1
J12.23	-	C	36	11	C	-	J12.2
J12.22	-	C	35	10	C	-	J12.3
J12.21	-	C	34	9	C	-	J12.4
J12.20	-	C	33	8	C	-	J12.5
J12.19	-	C	32	7	C	-	J12.6
J12.18	-	C	31	6	C	-	J12.7
J12.17	-	C	30	5	C	-	J12.8
J12.16	-	C	29	4	C	-	J12.9
J12.15	-	C	28	3	C	-	J12.10
J12.14	-	C	27	2	C	-	J12.11
J12.13	-	C	26	1	C	-	J12.12