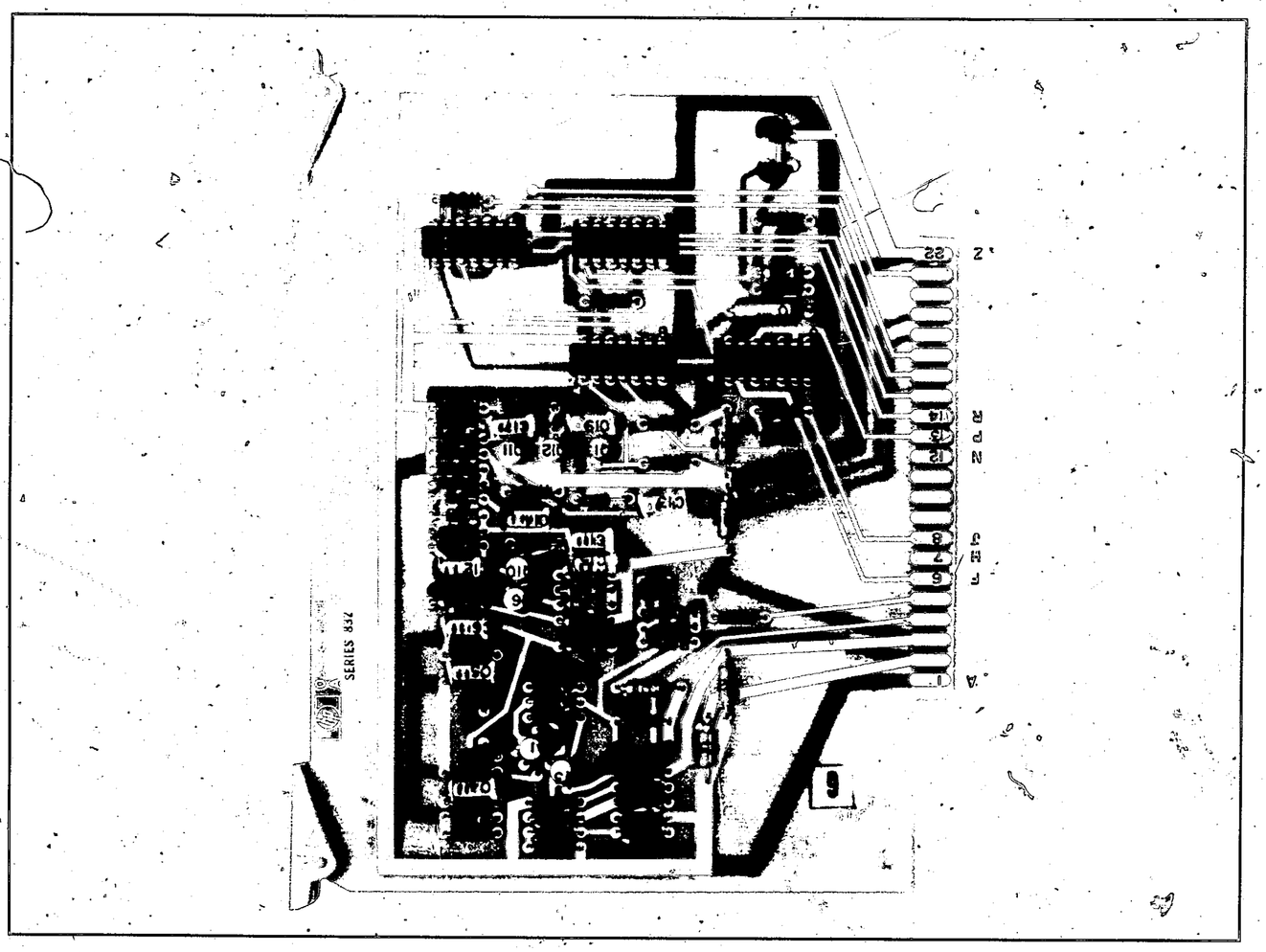
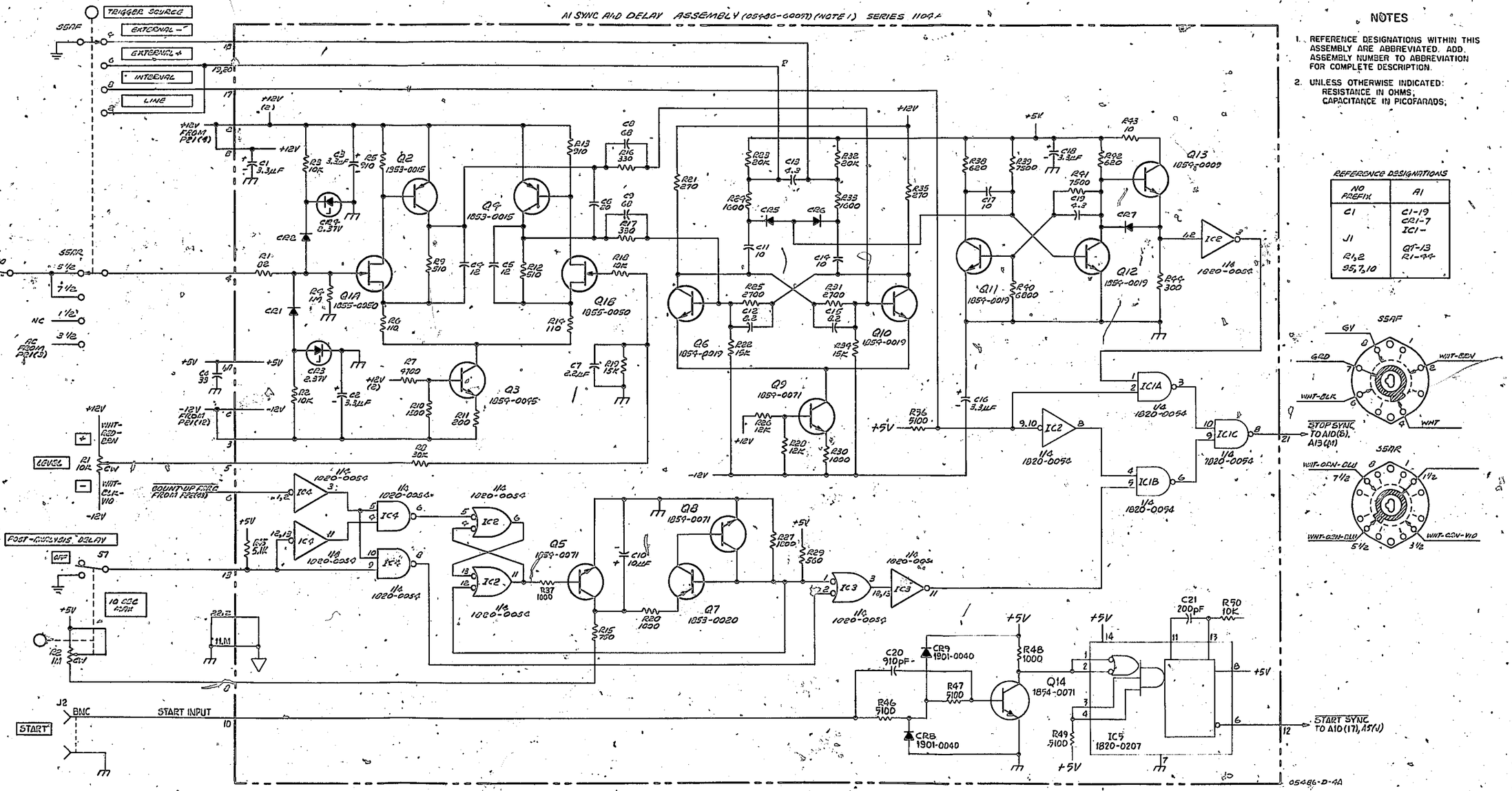

SERIES 854



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;

REFERENCE DESIGNATIONS

NO PREFIX	A1
C1	C1-19
	CR1-7
	IC1-
J1	
R1,2	Q1-13
95,7,10	R1-44

Figure 4-4
A1 Input Buffer and Trigger Series 852, 832

A2 TIME BASE "B" (05486-60010)

LOGIC AND DESCRIPTION

The function of the 05486-60010 TIME BASE "B" is to divide the 100 kHz input from 05486-60009 by the appropriate factor to obtain pulses at a rate determined by the Sweep Time and/or the Preanalysis Delay switch.

At beginning of each sweep, all decades (IC's 1, 12, 13, 14, 15) are reset to zero via CLEAR on pin R (buffered version of reset time base command). Also, IC4(6) and IC5(3) are set so as to look at PREANALYSIS DELAY switch. The decades count pulses from 10 μs B (pin T), and PRESAMPLE A (pin U) goes high just before the preanalysis delay is complete.

The next pulse at 10 μs A (pin S) sets IC4(6) and IC5(3) so as to look at the SWEEP TIME switch, and resets the decades to zero. Prior to the next 10 μs B pulse, the decade reset condition is reset via RESET (pin U).

The decades now count 10 μs B pulses, causing PRESAMPLE A to go high when a sample pulse is due (10 microseconds inadvance). The actual sampl pulse is created on the A10 board, by gating PRESAMPLE A with 10 μs A. Each sample in turn resets the decades, starting the cycle anew.

Truth Tables for Preanalysis Delay and Sweep Time

NOTES: 1. Low state enables.
2. Thus, samples every 50 msec requires low states for ÷5 and ÷1000 (from 10 μs to 500 μs), and high states for ÷1, ÷2, ÷10, ÷100.

Delay	Sweep Time	÷2	÷5	÷1	÷10	÷100	÷1000	TBB1	TBB2
0	1 ms	1	1	0	1	1	1	0	0
20μs	2	0	1	0	1	1	1	0	1
50	5	1	0	0	1	1	1	1	0
100	10	1	1	1	0	1	1	1	0
200	20	0	1	1	0	1	1	1	1
500	50	1	0	1	0	1	1	1	0
1ms	100	1	1	1	1	0	1	1	0
2	200	0	1	1	1	0	1	1	1
5	500	1	0	1	1	0	1	1	0
10	1 sec	1	1	1	1	1	0	1	0
20	2	0	1	1	1	1	0	1	1
50	5	1	0	1	1	1	0	1	0
100	10	1	1	1	1	1	1	1	0
200	20	0	1	1	1	1	1	1	1
500	50	1	0	1	1	1	1	1	0
	EXT	1	1	1	1	1	1	1	0

Delay Output Pins	(2)	(3)	(4)	(5)	(6)	(7)	9 Bits
Sweep Time Output Pins	(B)	(C)	(D)	(E)	(F)	(H)	

7 Bits = $\overline{TTB1}$ - TBB2

DECADE OPERATION ON A2 TIME BASE B (05486-60010)

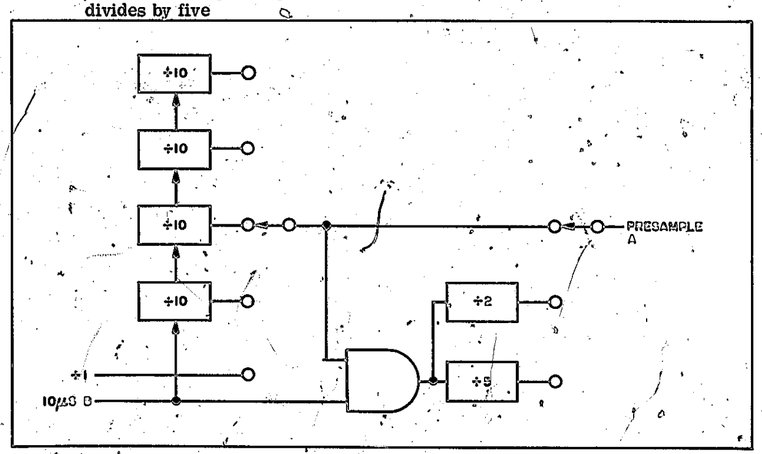
IC12, IC13, IC14, IC15 are hooked up to be BCD counters. Internally, the decades go through the following states:

Counts at Pin 14	Pin 11 D	Pin 8 C	Pin 9 B	Pin 12 A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

When Pin 11 and Pin 12 are high, the decade contains nine (9) counts

Pin 12 on IC16 goes high after Pin 14 receives one count – it divides by two.

Pin 11 on IC16 goes high after Pin 1 receives four counts – it divides by five

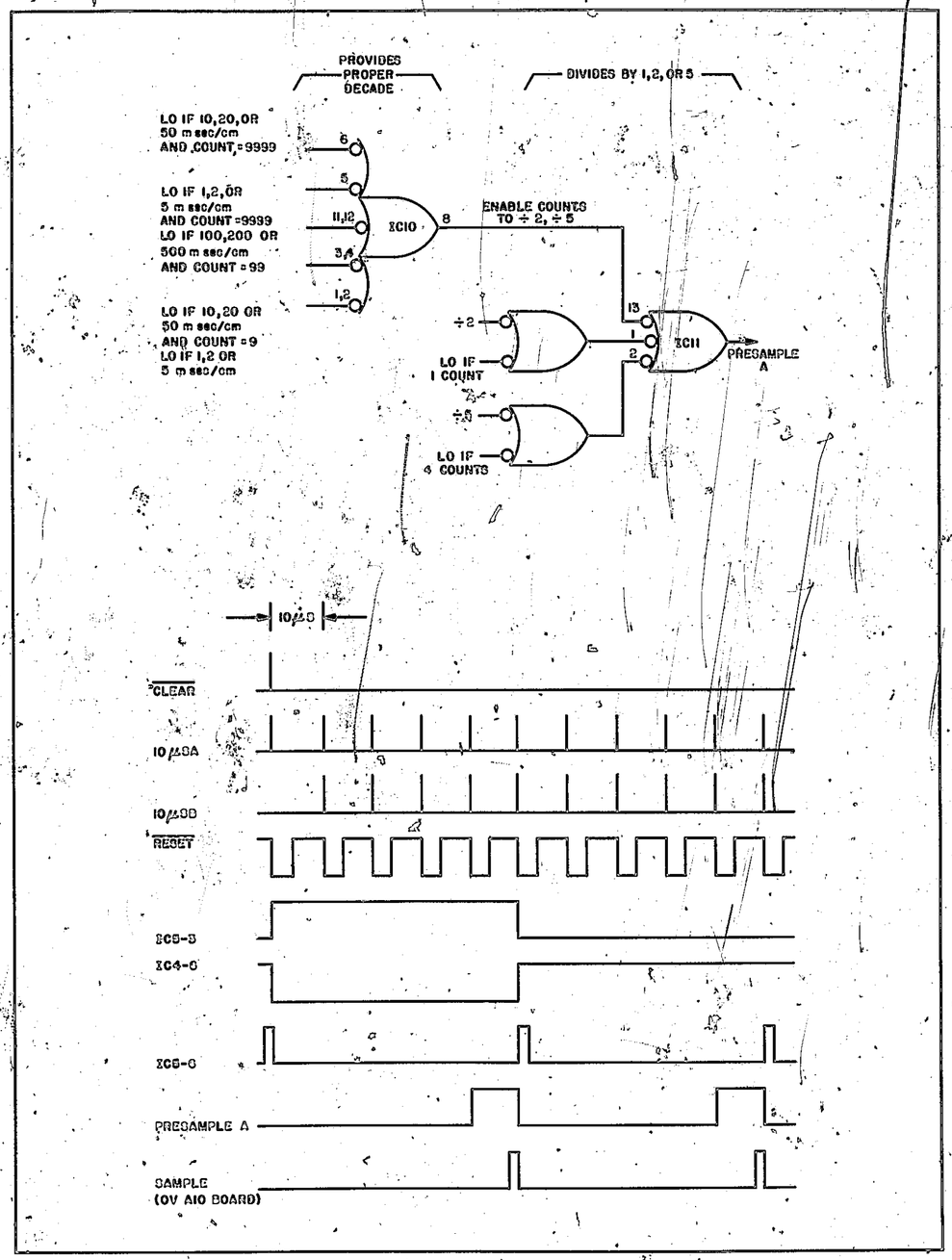


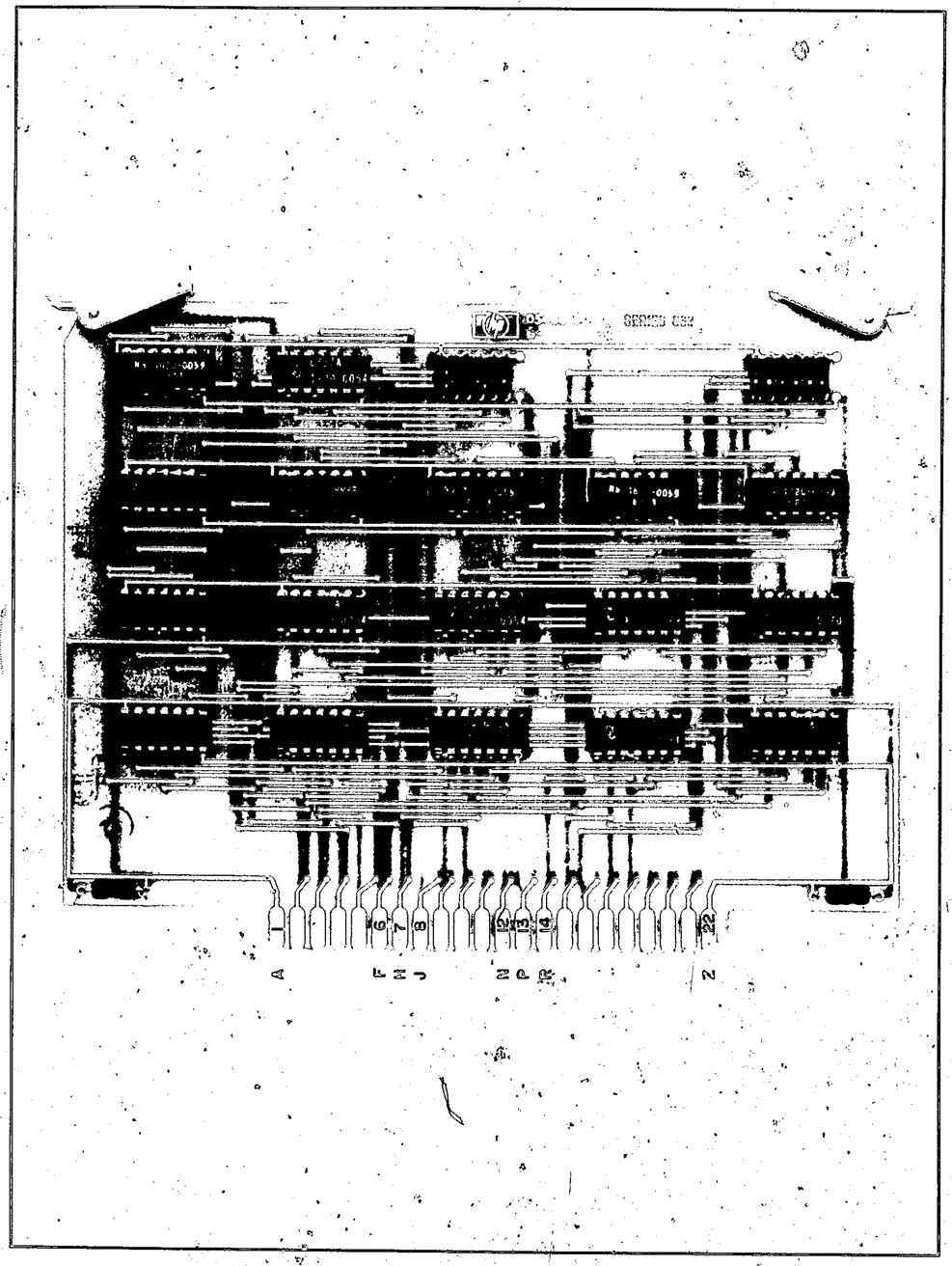
Presample A is anded with 10 μs B on A10 board to form sample pulse.

Decades initialized at start of Preanal Delay (CLEAR) and with every sample pulse.

Figure 4-4
A1 INPUT BUFFER AND TRIGGER
SERIES 852, 832

(See Page 4-9)


PROVIDES PROPER DECADE
DIVIDES BY 1, 2, OR 5
LO IF 10,20,OR 50 m sec/cm AND COUNT=9999
LO IF 1,2,OR 5 m sec/cm AND COUNT=9999
LO IF 100,200 OR 500 m sec/cm AND COUNT=99
LO IF 10,20 OR 50 m sec/cm AND COUNT=9
LO IF 1,2 OR 5 m sec/cm
8
5
11,12
3,4
1,2
XC10
8
ENABLE COUNTS TO ÷ 2, ÷ 5
÷2
LO IF 1 COUNT
÷5
LO IF 4 COUNTS
13
1
2
XC11
PRESAMPLE A
10 μsec
CLEAR
10 μsec A
10 μsec B
RESET
XC5-3
XC4-0
XC5-0
PRESAMPLE A
SAMPLE (0V AIO BOARD)



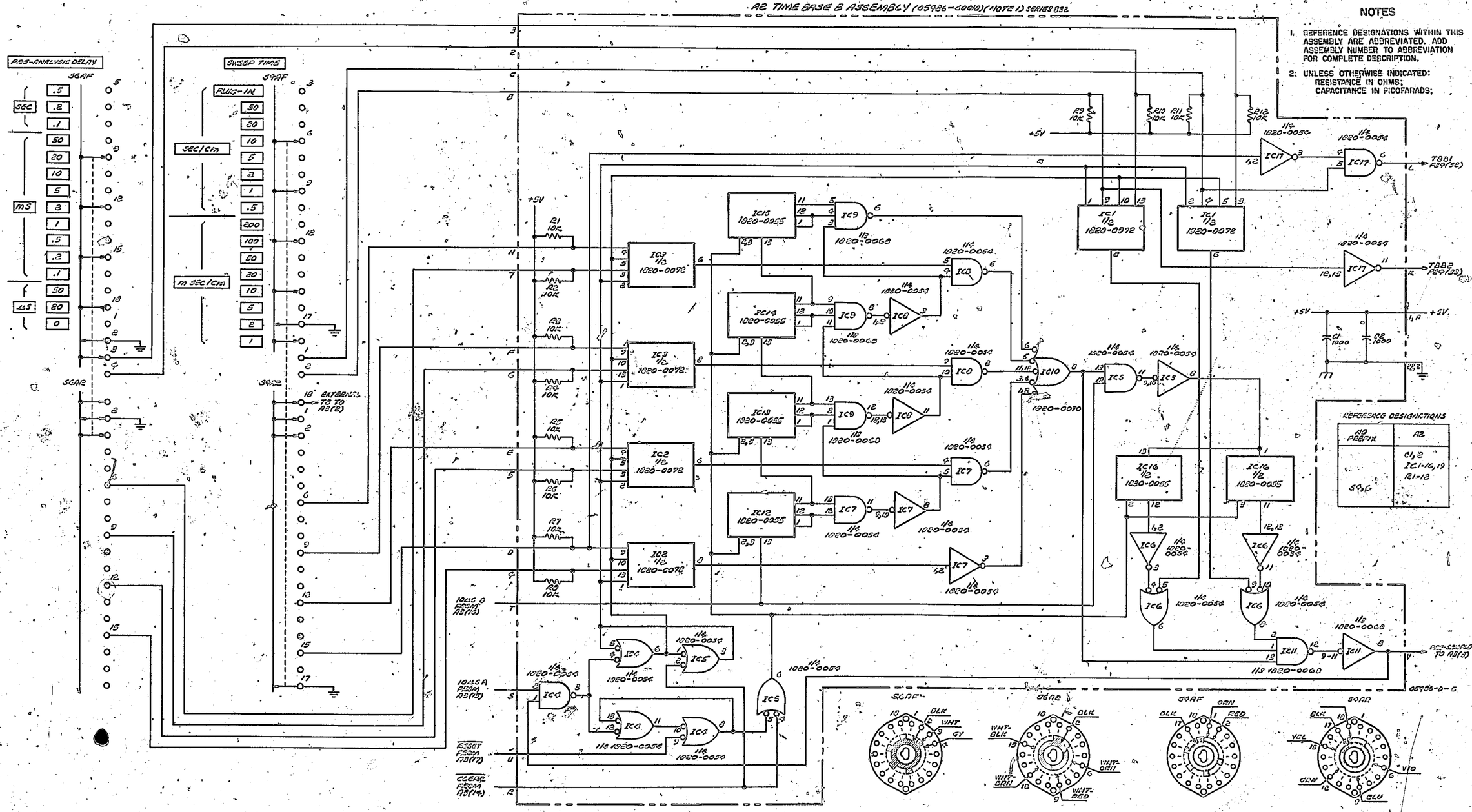


Figure 4-5
A2 Time Base B Series 832

A3 TIME BASE "A" (05486-60009)

DESCRIPTION

The 05486-60009 TIME BASE "A" board divides the 20 MHz Clock by 200 to produce pulses every 10 μsec (100 kHz), produces the first stage of decoding for up to 50 Timing Slots during the 10 μsec interval (second stage of decoding is on A4). The 05486-60009 also provides for external control of the Time Base.

FLIP/FLOP SEQUENCE

2	4	8	16	32	50	State	
1	1	1	1	1	1	R	Reset time base to start of sweep
0	0	0	0	0	0	0	
1	0	0	0	0	0	2	
0	1	0	0	0	0	4	
1	1	0	0	0	0	6	
0	0	1	0	0	0	8	
			etc.				
1	1	1	0	1	0	46	
0	0	0	1	1	0	48	
0	0	0	0	0	1	50	
1	0	0	0	0	1	52	
0	1	0	0	0	0	54	
			etc.				
1	1	1	0	1	1	96	
0	0	0	1	1	1	98	

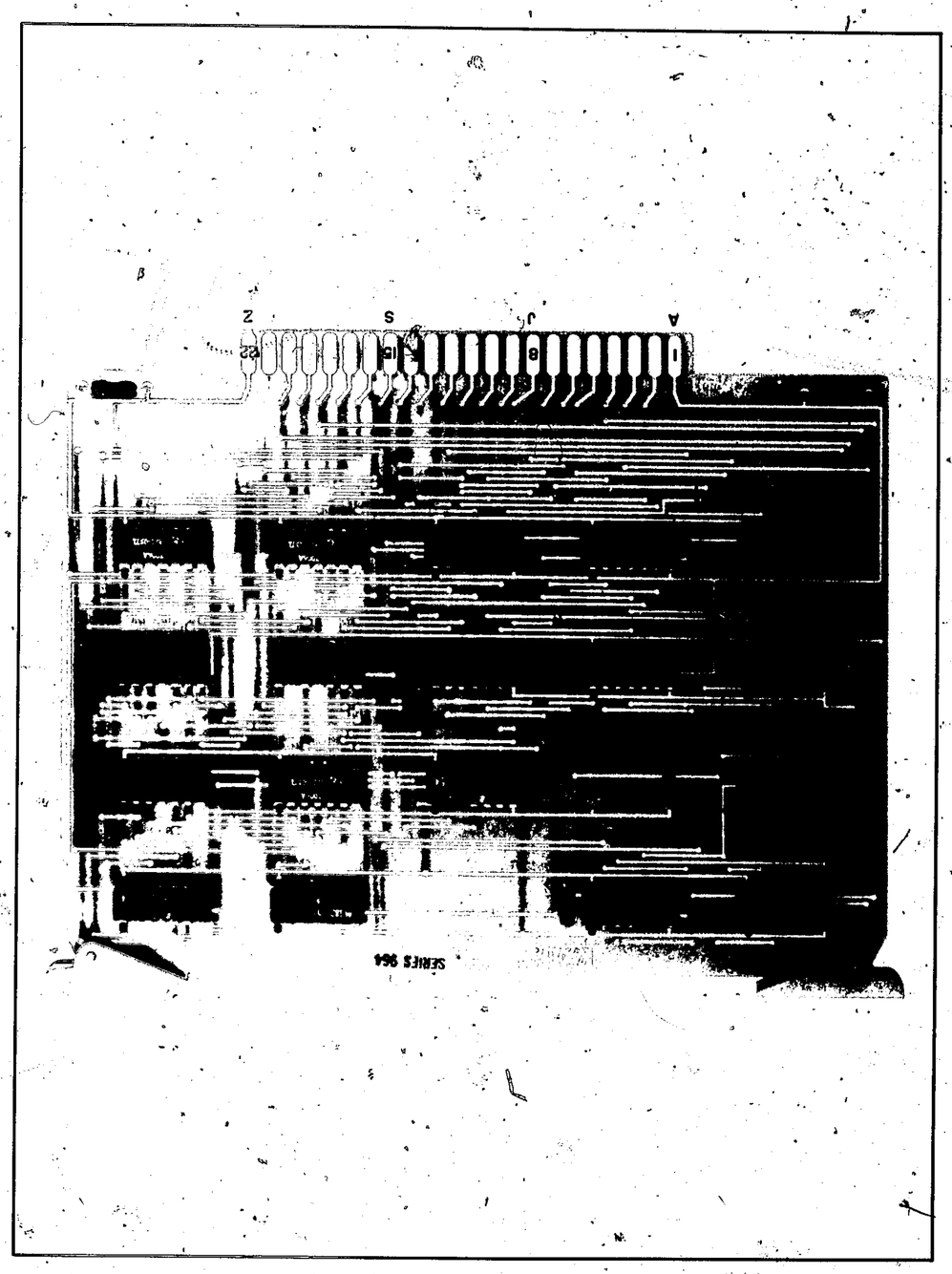
10 μs A (pin 15) gated out at state 98 and state R
10 μs B (pin 16) gated out at state 98 only
$\overline{\text{RESET}}$ (pin 17) low when FF6 is high (resets decade dividers on A2 after pre-analysis delay)
$\overline{\text{TB1}}$ through $\overline{\text{TB12}}$ code FF outputs

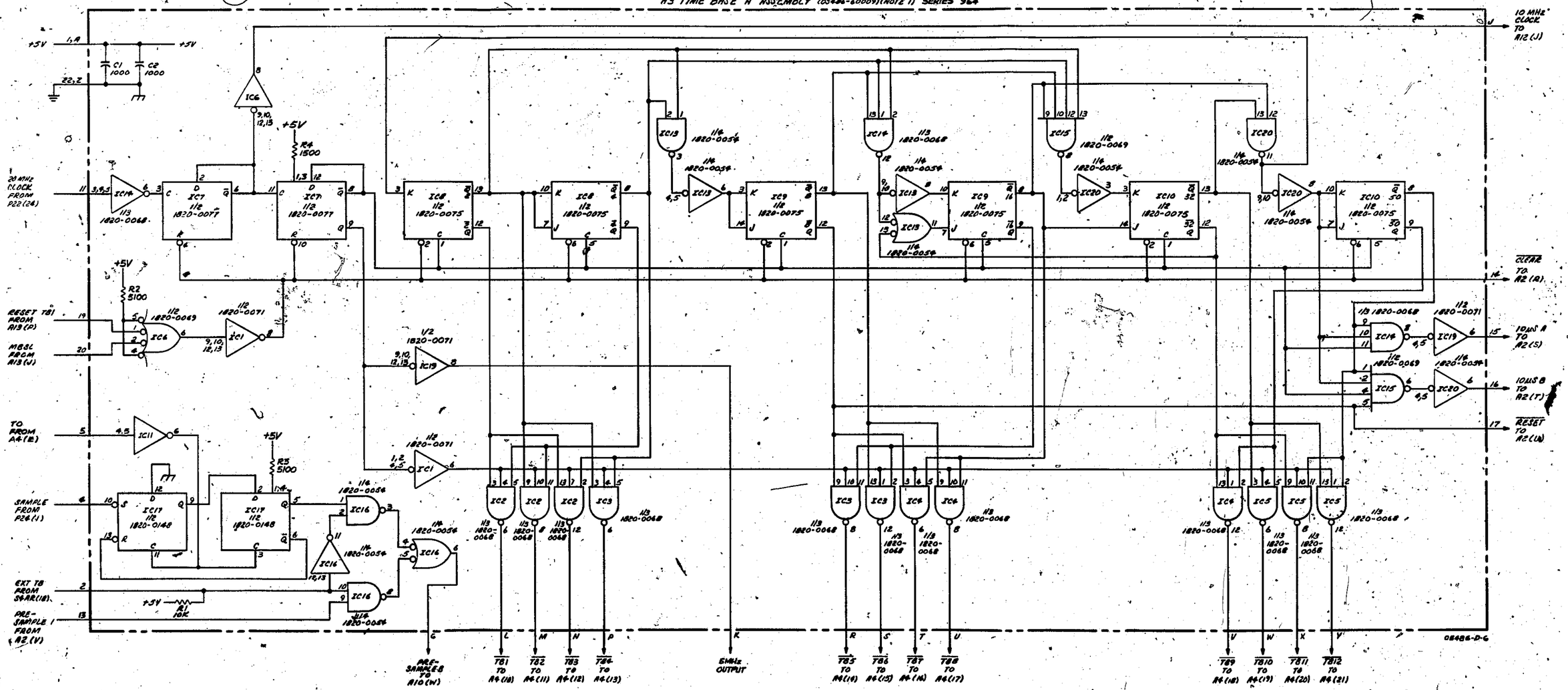
CHANGES FOR CURRENT BOARDS

Current Series: 864

Older Series: 852, 832

The current board may be used as a replacement for either older board.


SERIES 964



NOTES

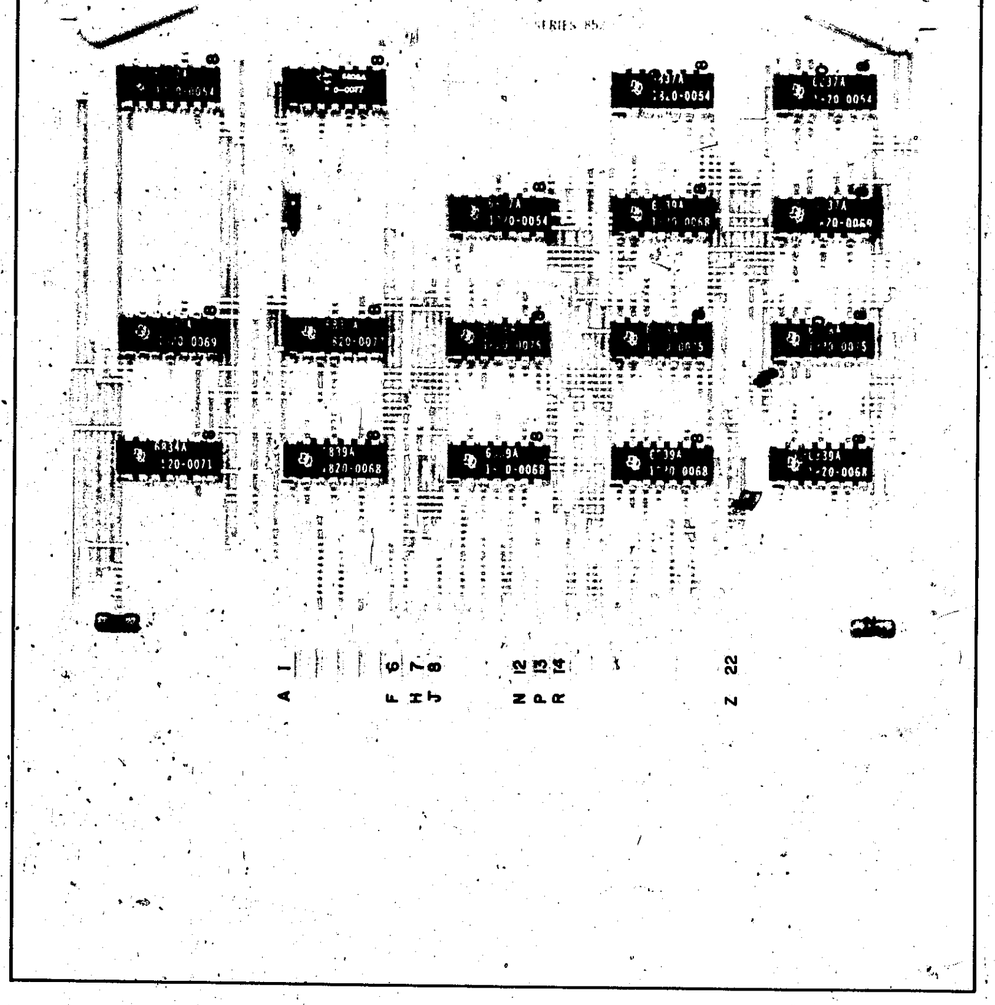
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS;

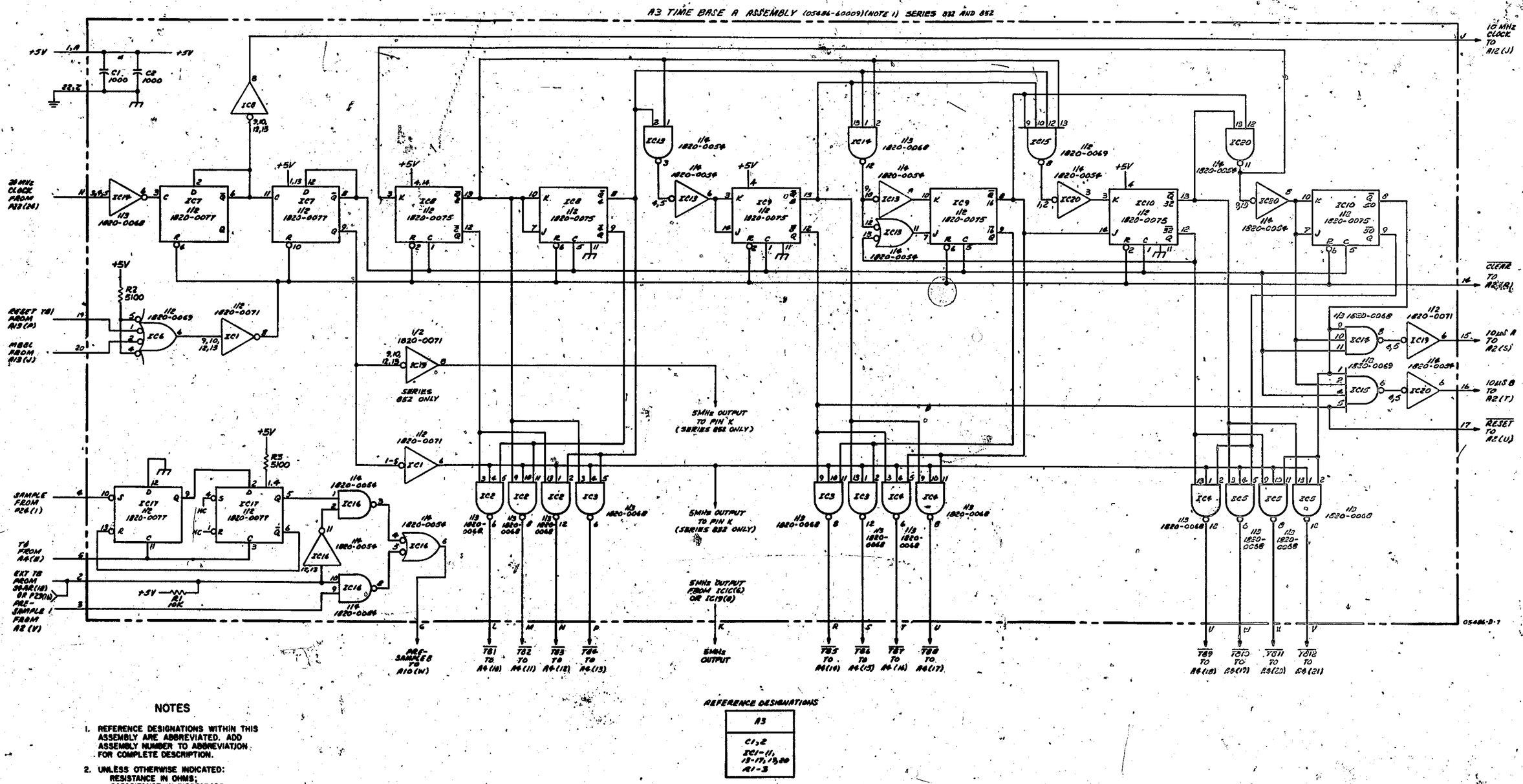
REFERENCE DESIGNATIONS

A3
C1,2 IC1-11, 13-17,19,20 R1-3

Figure 4-6
A3 Time Base A Series 964

See Figure 4-6 for Board description.





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;

REFERENCE DESIGNATIONS

A3
C1,2 IC1-11, 13-17, 19,20 A1-3

Figure 4-7
A3 Time Base A Series 852, 832

A4 TIME SLOT DECODER (05486-60036, 05486-60008)

DESCRIPTION

The Time Slot Decoder provides the second stage of decoding for the timing slots used during the 10 μsec basic timing cycle (the first stage of decoding is on A3).

The outputs decode $\overline{TB1}$ through $\overline{TB12}$, as shown in the table below. The bar indicates "L" signal state.

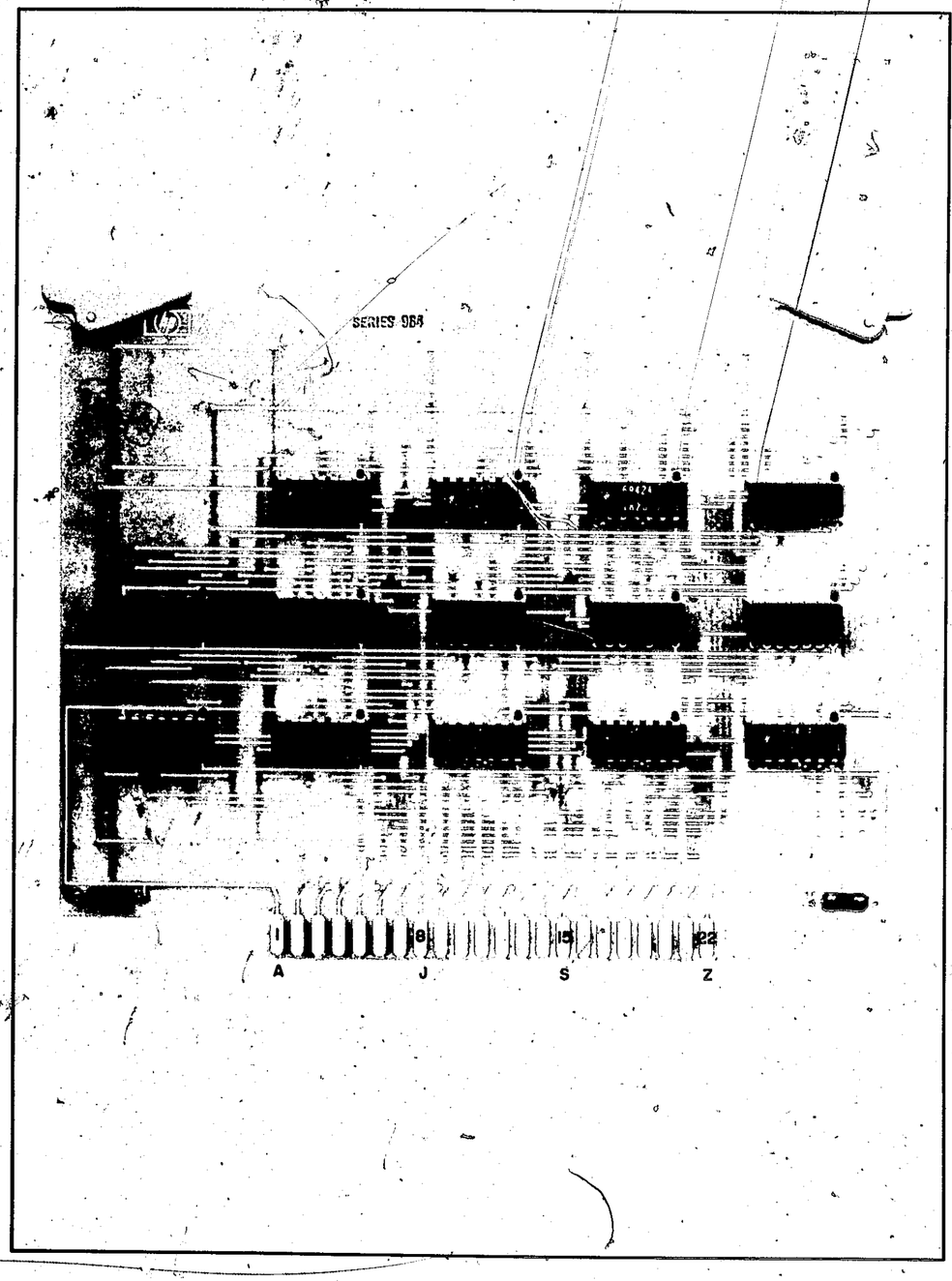
$\overline{TB1}$ =	$\overline{2.4}$	$\overline{TB5}$ =	$\overline{8.16}$	$\overline{TB9}$ =	$\overline{32.50}$
$\overline{TB2}$ =	$\overline{2.4}$	$\overline{TB6}$ =	$\overline{8.16}$	$\overline{TB10}$ =	$\overline{32.50}$
$\overline{TB3}$ =	$\overline{2.4}$	$\overline{TB7}$ =	$\overline{8.16}$	$\overline{TB11}$ =	$\overline{32.50}$
$\overline{TB4}$ =	$\overline{2.4}$	$\overline{TB8}$ =	$\overline{8.16}$	$\overline{TB12}$ =	$\overline{32.50}$

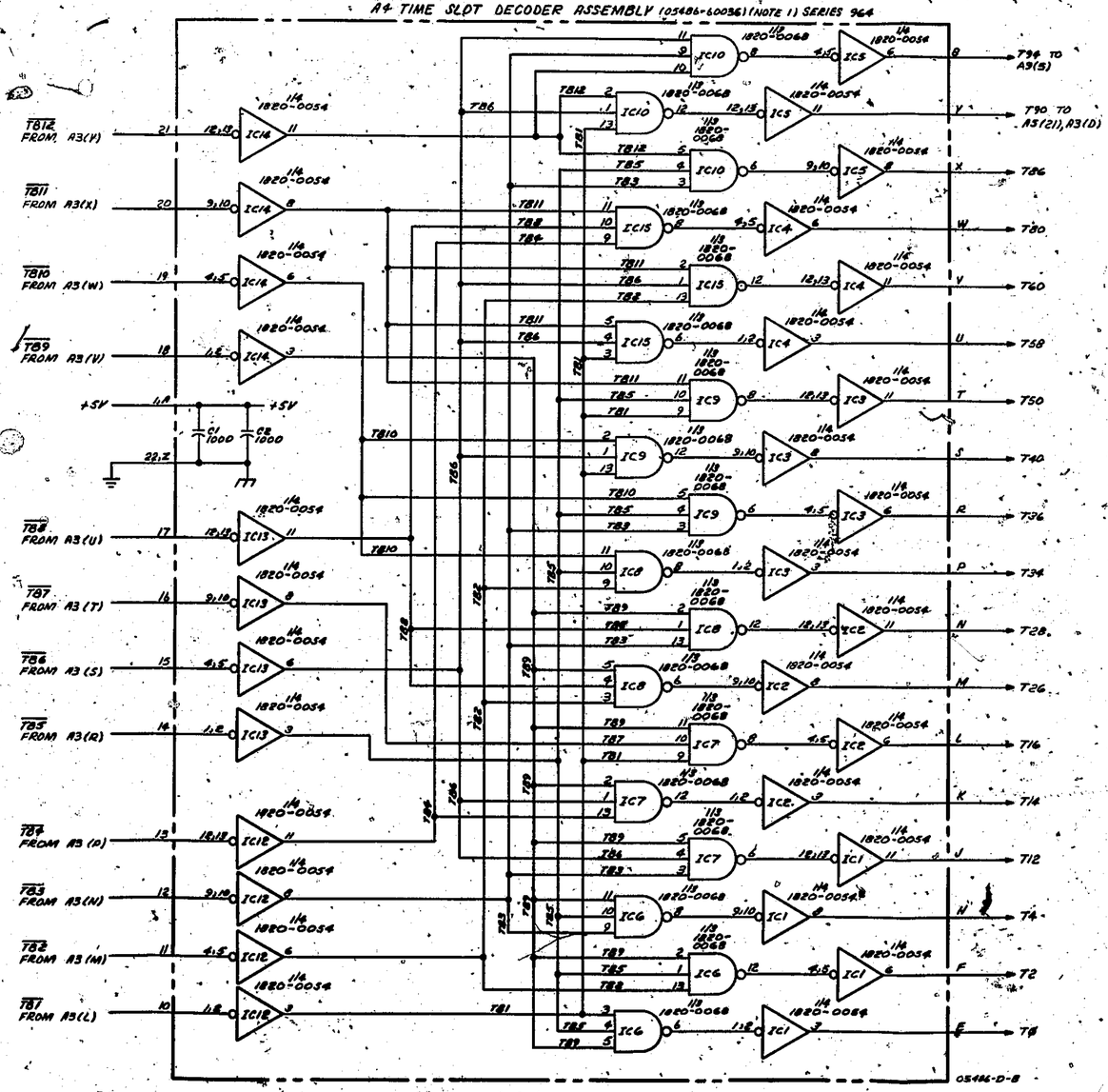
CHANGES FOR OLDER BOARDS

Current Board: 05486-60036

Older Board: 05486-60008

The current board is a direct replacement for the older board. The schematic for the older board is the same as for the current board, except the circuit for T94 was not etched on board (e.g., T94 did not exist).





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: CAPACITANCE IN PICOFARADS;

REFERENCE DESIGNATIONS

A4
C1, 2 IC1–10, 12–15

Figure 4-8
A4 Time Slot Decoder Series 964

A5 LIGHT DRIVER CONTROL BOARD (05486-60037, 05486-60003)

LOGIC AND DESCRIPTION

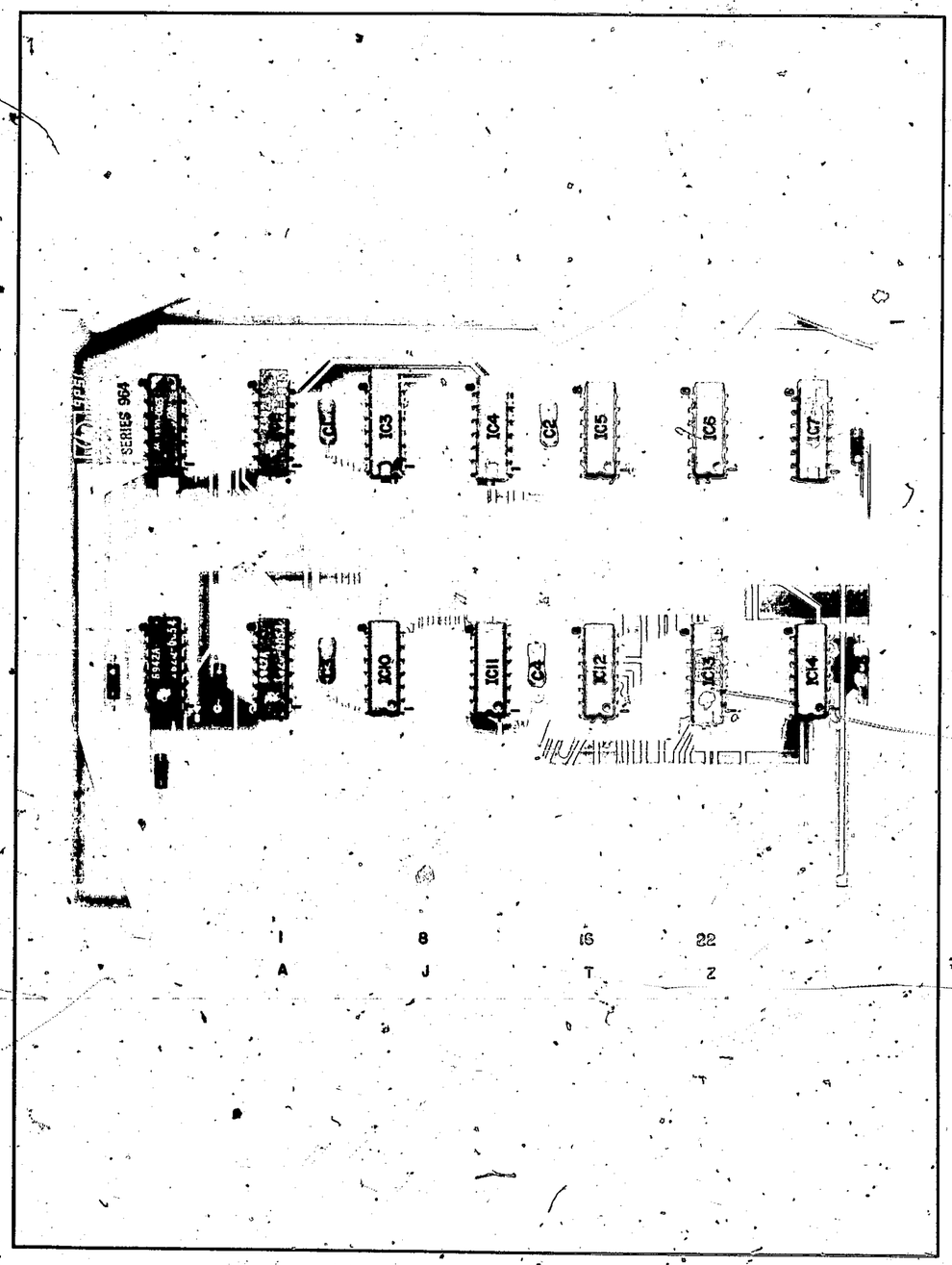
The function of the Light Driver Control Board is to combine the seven Internal Program States Average (AVG), Summation (SUM), Multichannel Scaling (MCS), Histogram Begin (HB), Histogram End (HE), Display (DISP), and Prepare (PREP), and the 17 Timing Slots (T0, T2, T4, T12, T14, T16, T26, T30, T34, T36, T40, T50, T58, T60, T80, T86, and T90) and several miscellaneous states Start Light On (LSTART), Processing Data as opposed to Displaying Data (P/D), Function Switch-Average (SWAVG), Advance Process Address Register Pulses (ADV Par 1), Histogram Switch-Amplitude (HAMP), Sensitivity Multiplier-Auto (AUTO), Function Switch-MCS (SWMCS), and Pulses to be counted during MCS (MCS PULSES) into pulses which Control Logic Operations in the 5486A/B Process Control, in the 5480A/B Memory/Display, * Start Generating Shift Pulses (START SHIFT) 5486A/B, Preset Shift Pulse Counter (PRESET SC) 5486A/B, Advance Process Address Register (ADVANCE PAR Z) 5480A/B, Increment Accumulator (ADV A) 5480A/B, Clear Shift Control Hold Register (CLEAR HOLD) 5486A/B, start Analog-to-Digital Converter Ramp (START ADC) 5485A, and set Sensitivity Multiplier Switch Position into Shift Control Hold Register (SET SCALE #) 5486A/B.

CHANGES FOR OLDER BOARDS

Current Board (5486B Only): 05486-60037

Older Board (5486A Only): 05486-60003

The current board is used in 5486B's only and is not a direct replacement for the 05486-60003, which is used only in the 5486A.



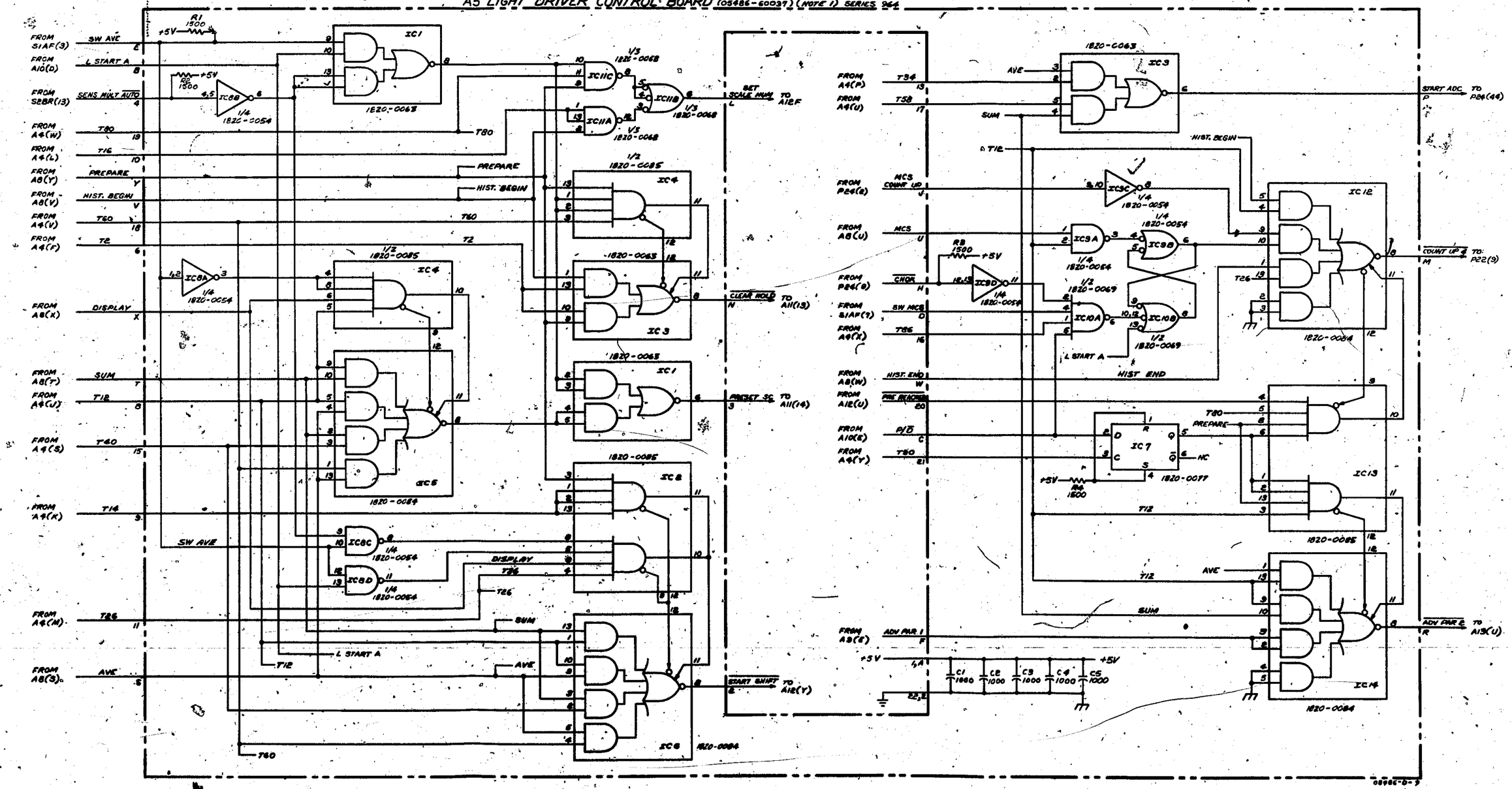
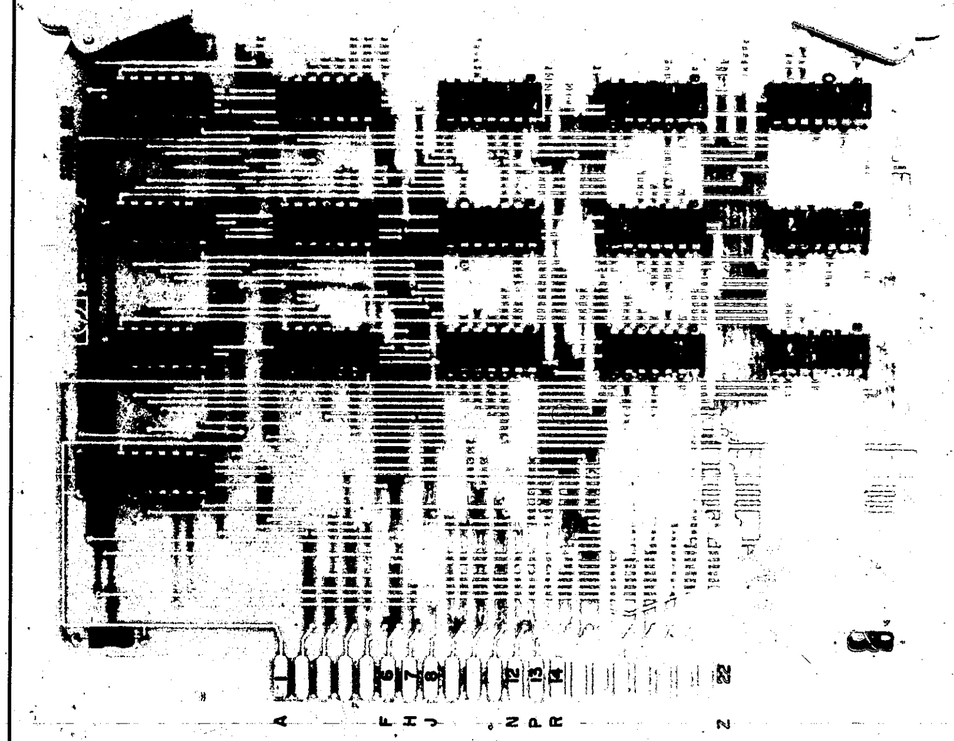


Figure 4-9
A5 Light Driver Control Series 964

See Figure 4-9 for Board description.



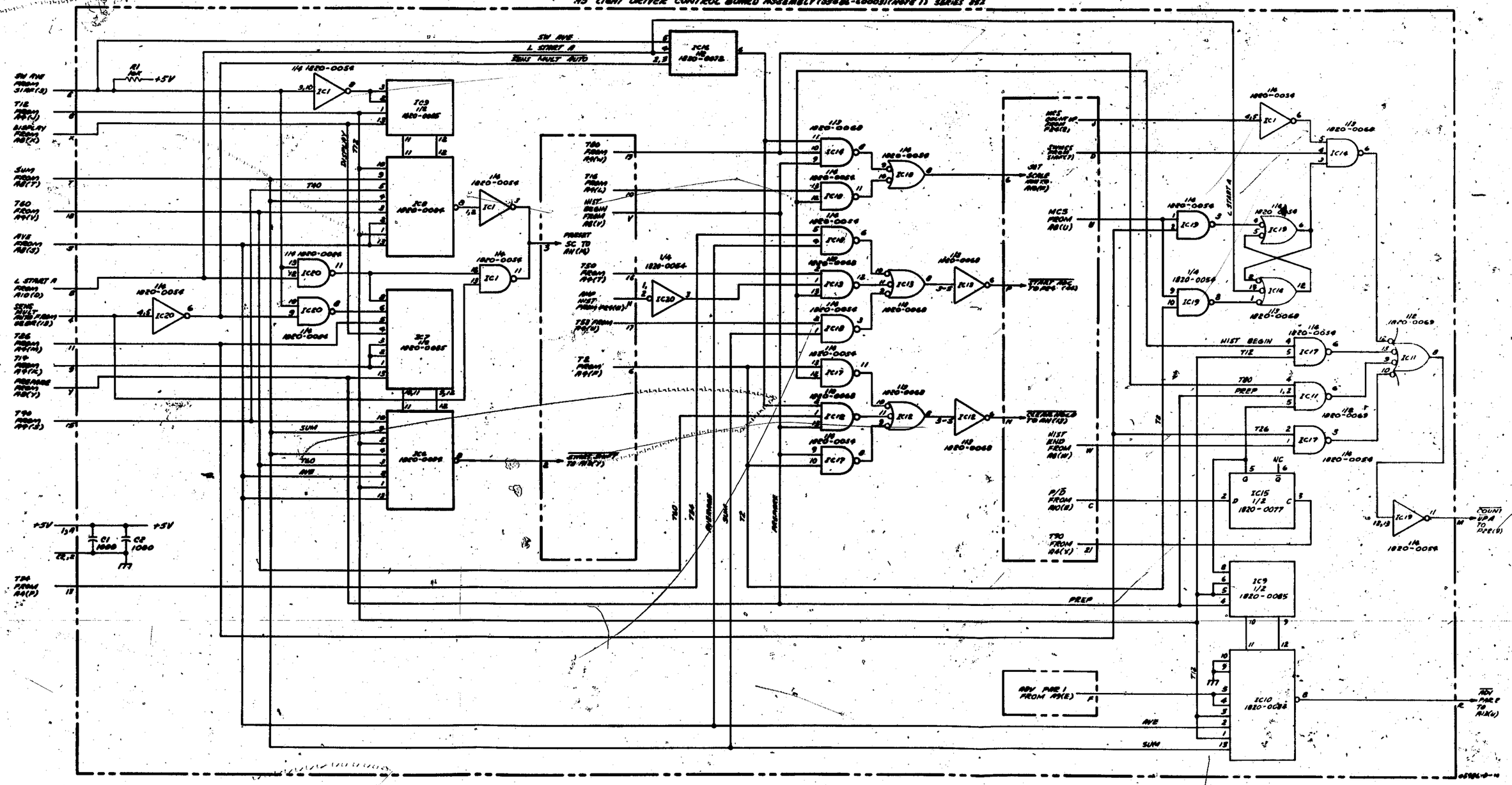


Figure 4-10
A5 Light Driver Control Series 852

See Figure 4-9 for A5 Board description.

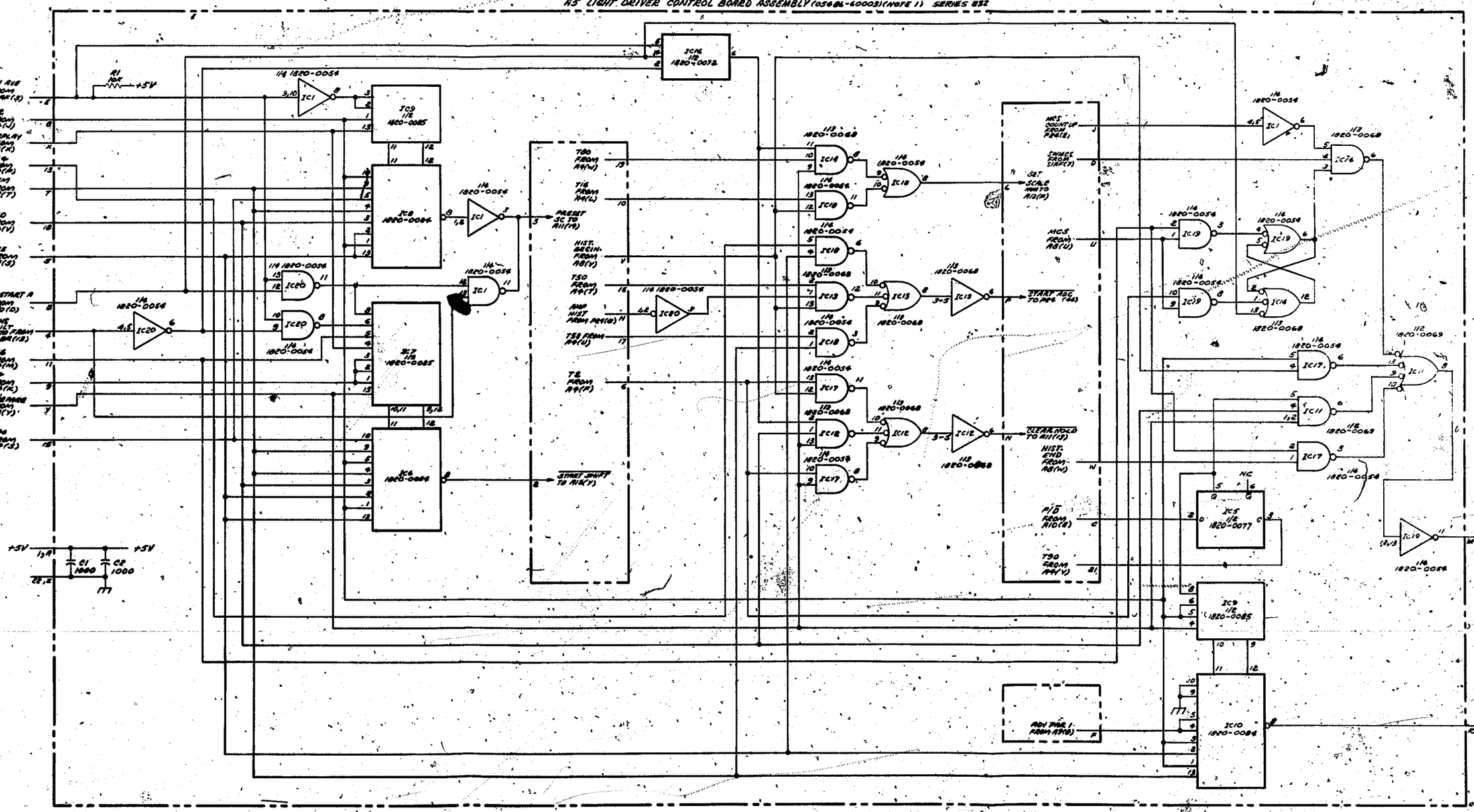


Figure 4-11
A5 Light Driver Control Series 832

A6 LOGIC MATRIX "C" (05486-60038).

LOGIC AND DESCRIPTION

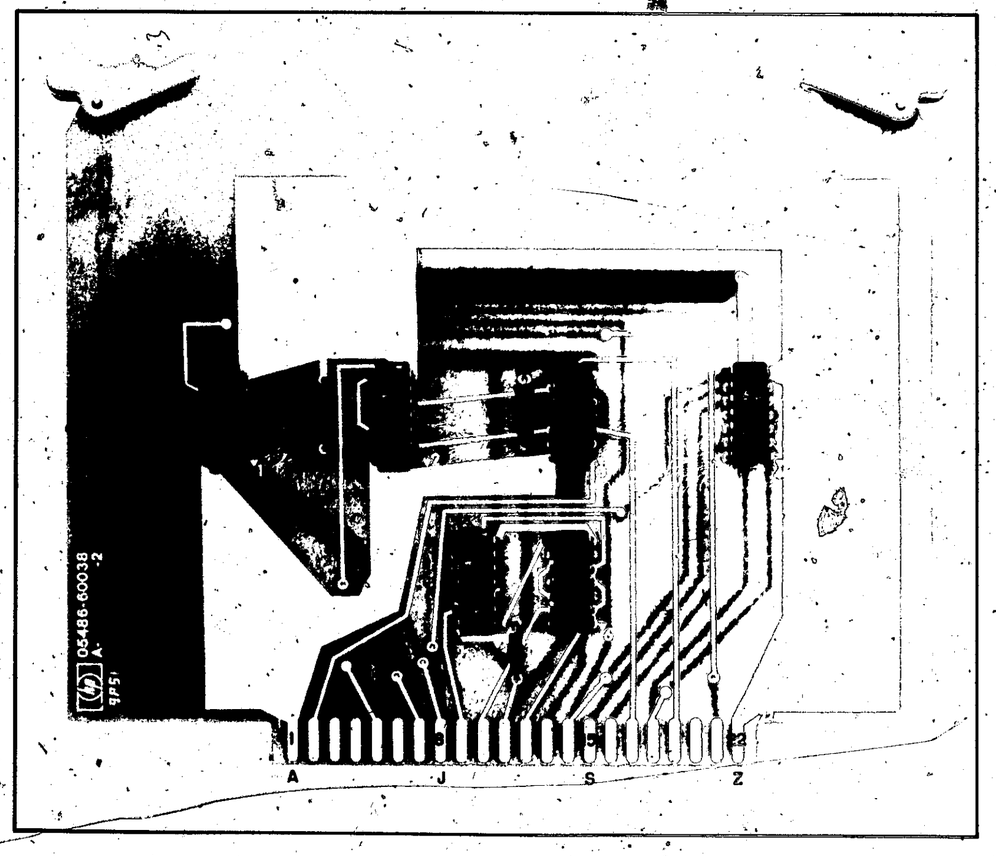
The function of LOGIC MATRIX "C" is to combine several Internal Program States Average (AVG), Summation (SUM), Histogram Begin (HB), and Prepare (PREP), and several Timing Slots (T0, T12, T34, T58, T80, and T90) and several miscellaneous States (Function Switch-Average (SWAVG), Function Switch-Summation (SWSUM), 5485A Analog-to-Digital Converter Finished (ADC FIN), and Process/Display (P/D) into pulses which control logic operations in the 5485A Two Channel Input (Start Amplitide Histogram Logic (START HAMP LOGIC), and Set Output Multiplexer (Set Out MPX) and in the 5486A/B Process Control (Set Sweep Number Switch Position into Shift Control Hold Register (SET SWEEP #), Inhibit Program State (INHIBIT), and Allow Program State (ALLOW).

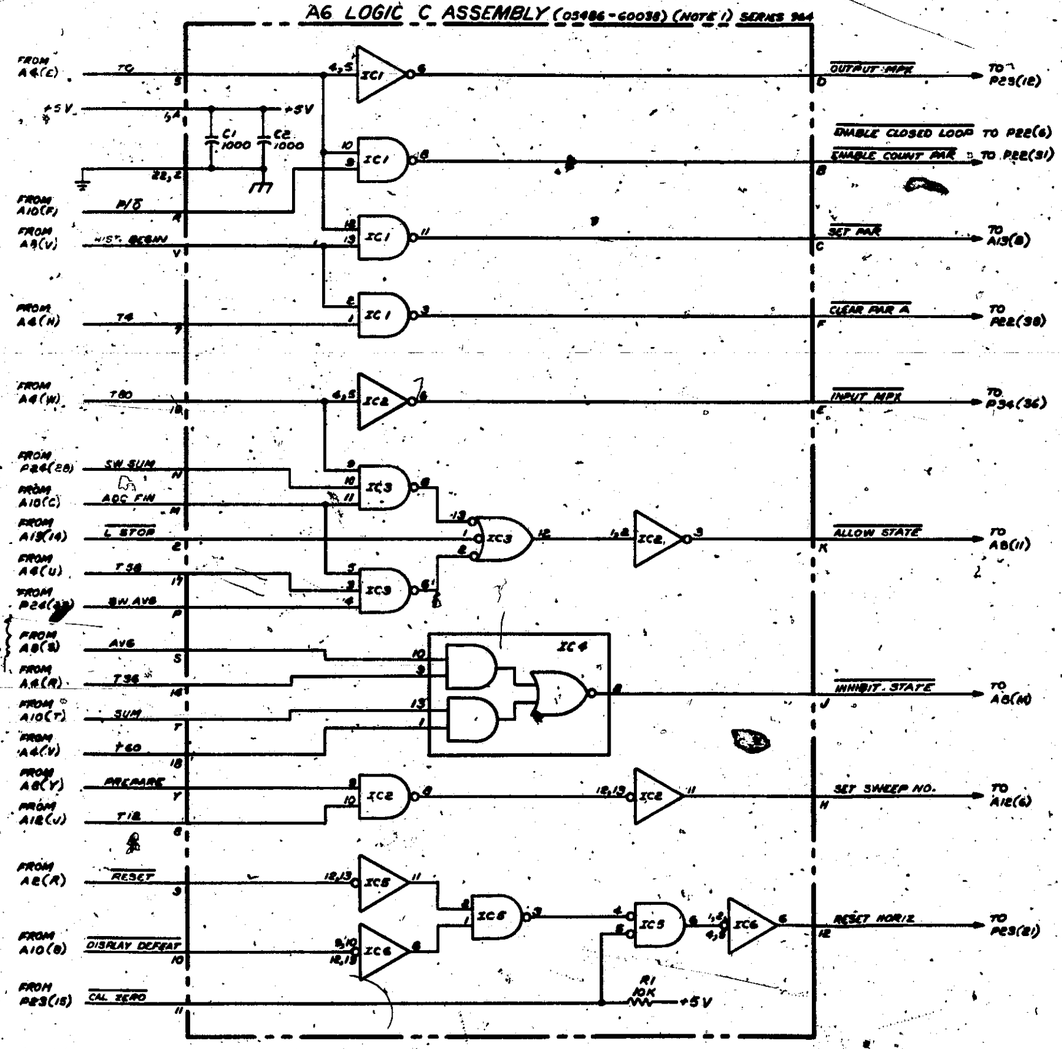
CHANGES FOR OLDER BOARDS

Current Board (5486B Only): 05486-60038

Older Boards (5486A Only): 05486-60014

The current board is used in 5486B's only and is not a direct replacement for the 05486-60014 used in the 5486A.





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;

REFERENCE DESIGNATIONS

A6
C1, 2 IC 1-6 R1

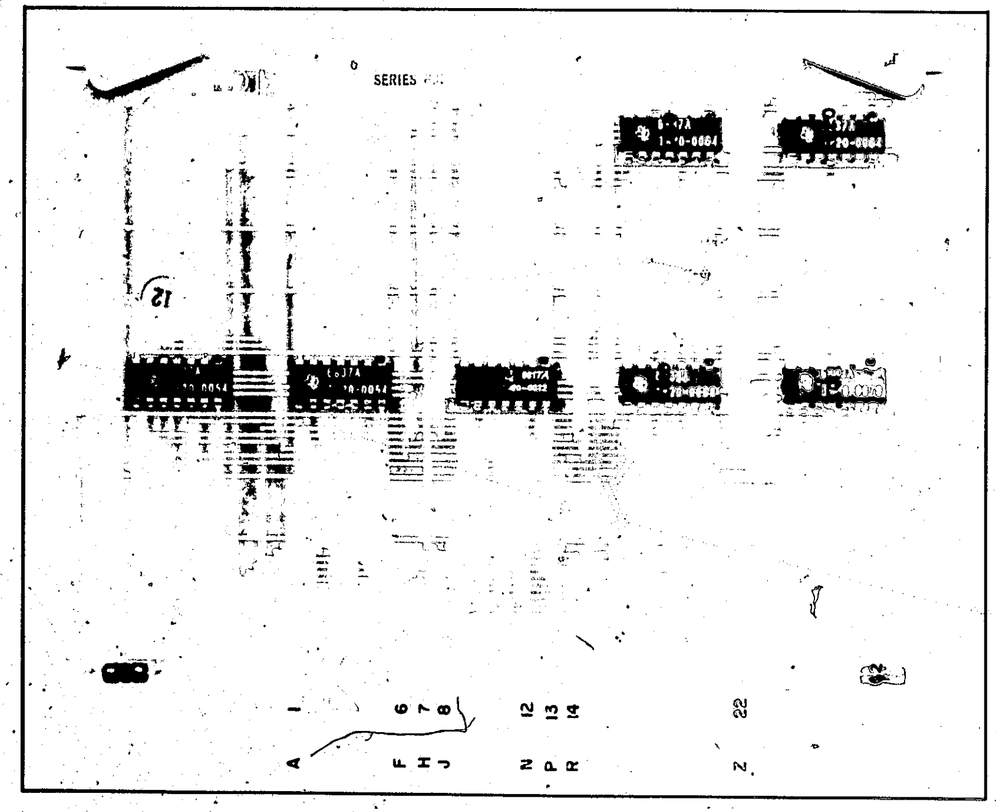
TABLE

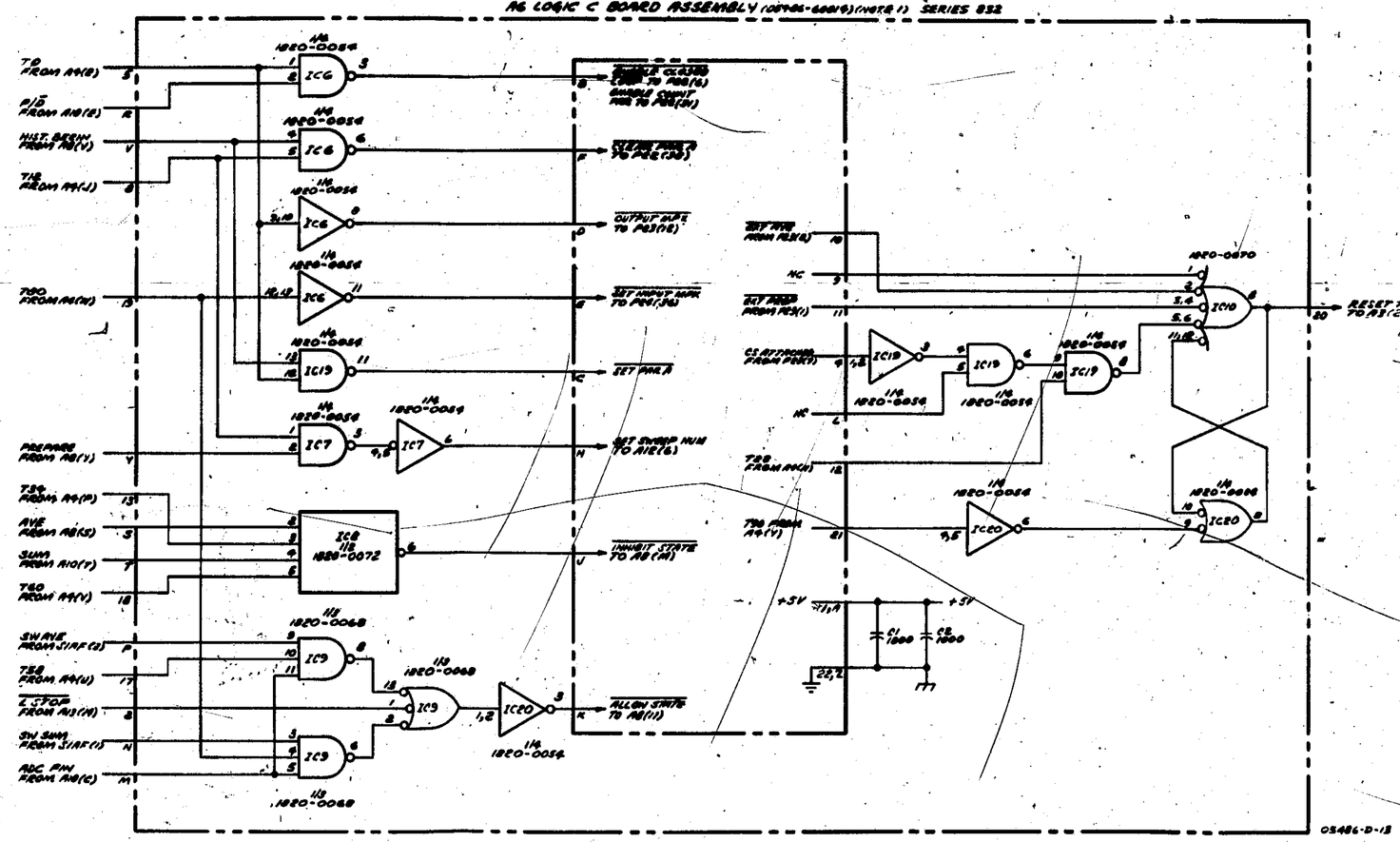
REFERENCE DESIGNATIONS	HP PART NUMBERS
IC 1, 2, 5	1820-0084
IC 3, 4	1820-0068
IC 4	1820-0063
IC 6	1820-0071

05486-D-12

Figure 4-12
A6 Logic C Series 964

See Figure 4-12 for Board description.





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: CAPACITANCE IN PICOFARADS;

Figure 4-13
A6 Logic C Series 832

A7 LOGIC MATRIX "A" (05486-60006)

LOGIC AND DESCRIPTION

The function of the 05486-60006 LOGIC MATRIX "A" BOARD is to combine:

1) The Seven Internal Program States: Average (AVG), Summation (SUM), Multichannel Scaling (MCS), Histogram Begin (HE), Histogram End (HE), Display (DISP), and Prepare (PREP).

2) The Seventeen Timing Slots (T0, T2, T4, T12, T14, T16, T26, T30, T34, T36, T40, T50, T58, T60, T80, T86, and T90).

3) Several miscellaneous states: Start Light on (LSTART) and FUNCTION Switch=AVERAGE (SWAVG) into pulses which control Logic Operations in the 5486A/B Process Control in the 5480A/B Memory/Display, and in the 5485A Two Channel Input.

The signals:

Clear Accumulator (Clear A) 5480A/B
Enable Accumulator to count (Enable count A) 5480A/B
Enable Accumulator to Shift Left (Enable SLA) 5480A/B
Reset Analog-to-Digital Converter Ramp (Reset ADC) 5485A
Read information from Memory into Accumulator (Read) 5480A/B
Write information into Memory from Accumulator (Write) 5480A/B
Transfer contents of accumulator Bit 23 to vertical DAC (Set MSB) 5480A/B
Transfer contents of accumulator bits 22 through 14 to vertical DAC (Set Vert) 5480A/B
Enable accumulator to shift right (Enable SRA) 5480A/B
Cycle memory, i.e., Read and then Write (Cycle) 5480A/B.

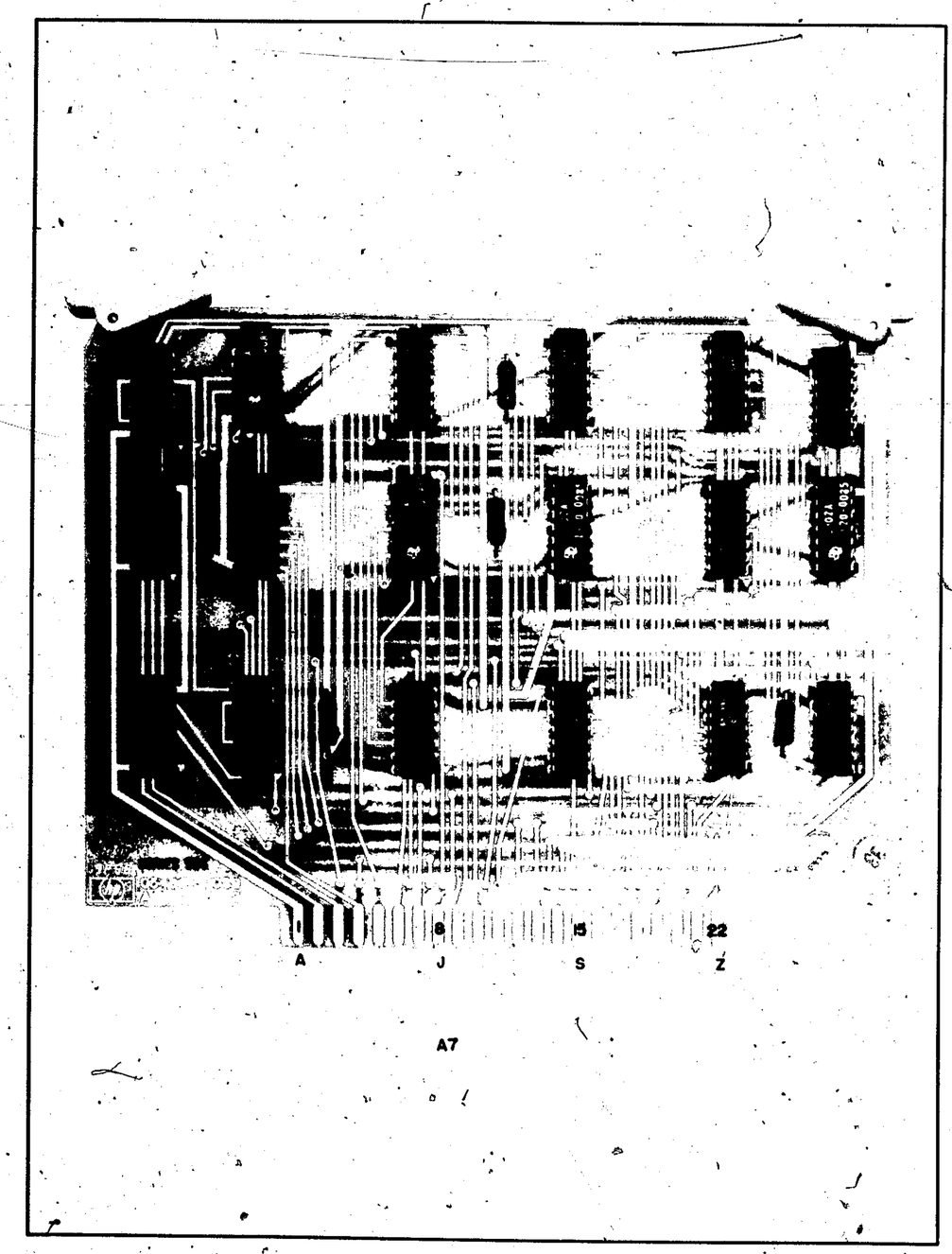
CHANGES FOR OLDER BOARDS

Current Board (5486B only): 05486-60039

Older Boards (5486A only): 05486-60006, Series 832 and 852

The current board is used in 5486B's only, and is not a direct replacement for the 05486-60006 boards used in the 5486A's.

The Series 852 05486-60006 board may be used as a direct replacement for the series 832 05486-60006 board.



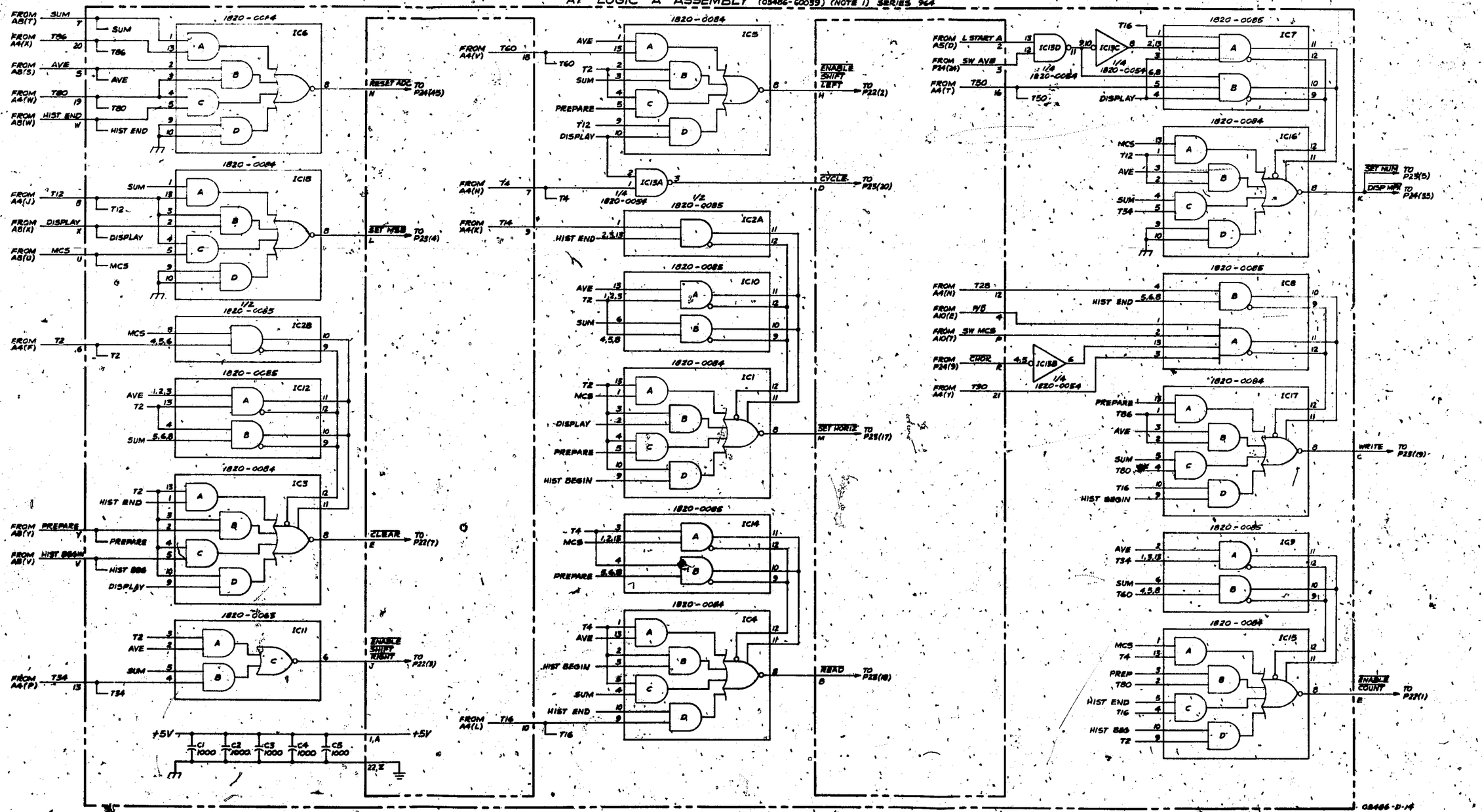
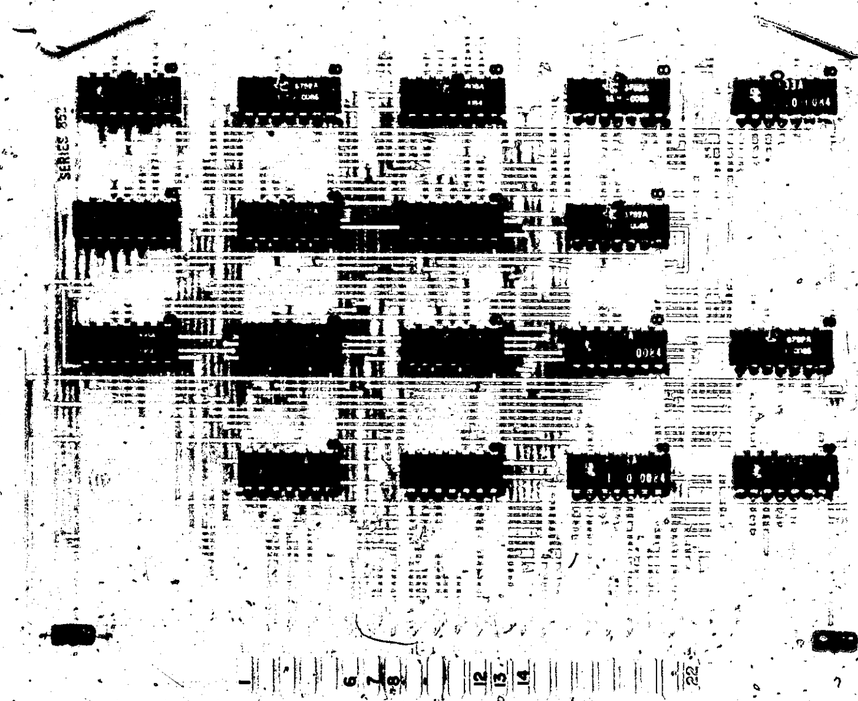
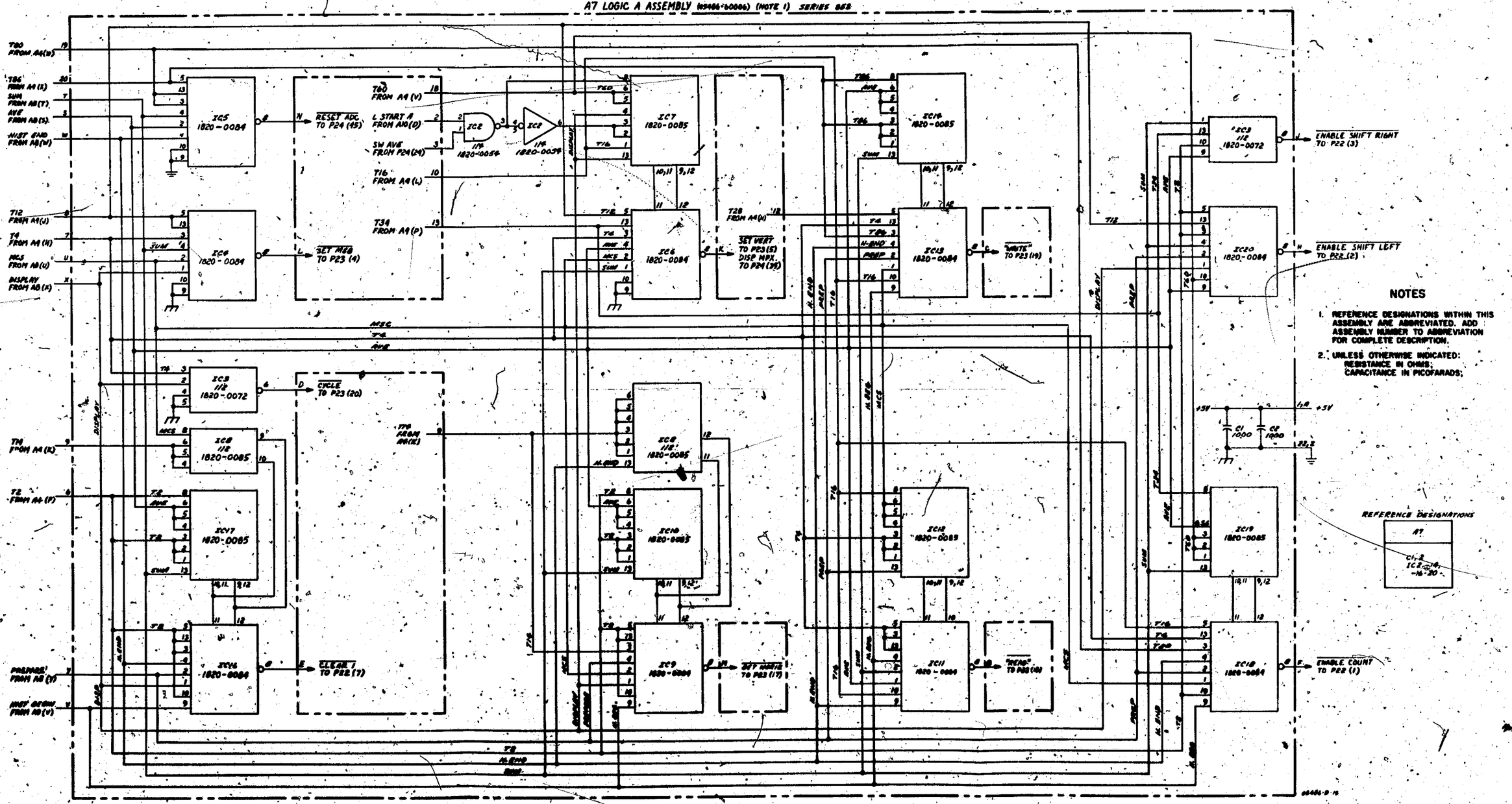


Figure 4-14
A7 Logic A Series 964

See Figure 4-14 for Board description.





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS;

Figure 4-15
A7 Logic A Series 852

See Figure 4-14 for A7 Board description.

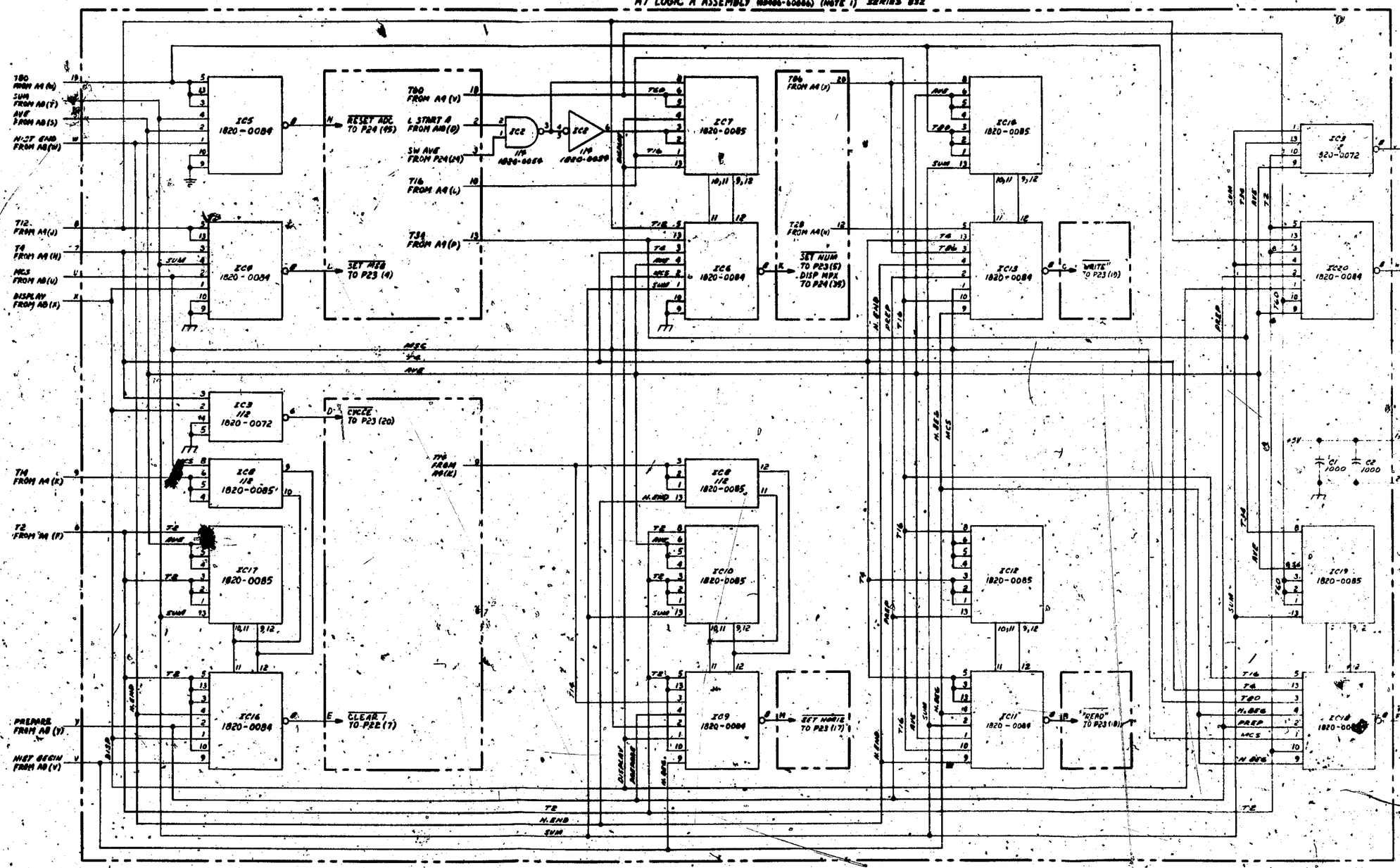


Figure 4-16
A7 Logic A Series 832

A8 PROGRAM SELECTOR "A" (05486-60005)

DESCRIPTION

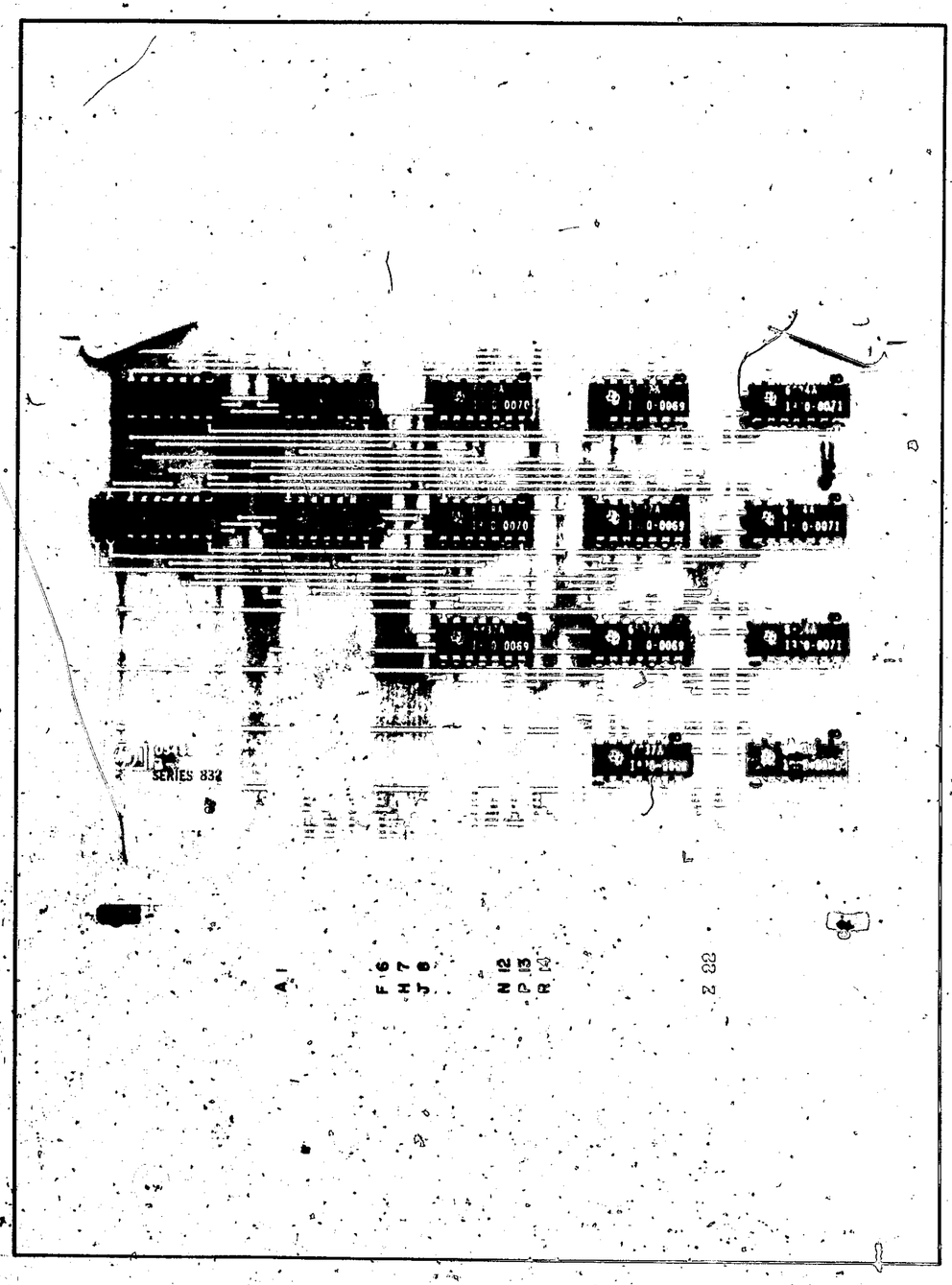
The function of the 05486-60005 Program Selector "A" is to provide the logic levels necessary to identify the Seven Internal Program States Average (AVG), Summation (SUM, Multichannel Scaling (MCS), Histogram Begin (HB), Histogram End (HE), Display (DISP), and Prepare (PREP). If an "INHIBIT" line has been low then no outputs are high. If an "ALLOW" lines has been low then one and only one of the outputs will be high. The output which is high corresponds to the input which was low last.

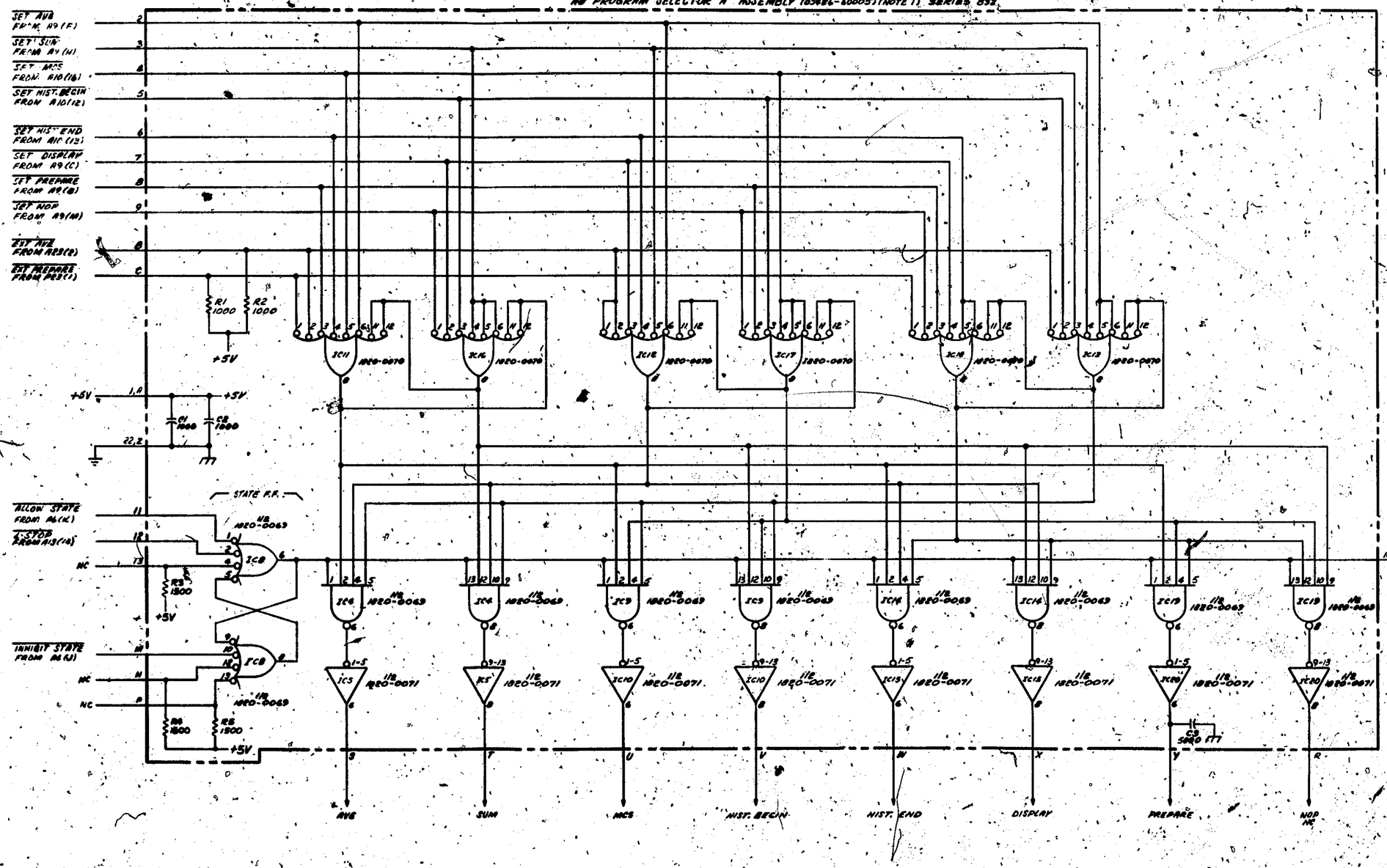
Program commands arriving at pins 2, 3, 4, 5, 6, 7, 8, 9, B, and C set flip/flops IC11-IC16, IC12-IC17, IC18-IC13.

Coding

Program	Q1(IC11-8)	Q2(IC12-8)	Q3(IC18-8)
AVE	1	1	0
SUM	0	1	0
MCS	1	0	0
HB	0	0	0
HE	1	1	1
DISP	0	1	1
PREP	1	0	1
NOP	0	0	1

The outputs of these flip/flops are decoded with gates so that one and only only program is on (high) at any given time.





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED; RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS.

REFERENCE DESIGNATIONS

Figure 4-17
A8 Program Selector A Series 832