HEWLETT PACKARD

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SYSTEM SERVICE MANUAL
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5480A/B
SERIAL PFX ALL SERIALS
05480-90015 (FICHE)
5 of 7

Figure 4-6. Test Points Multichannel Scaling (MCS) Program

NAME	LOC	5486 ORIGIN * INDIRECT
OPEN LOOP	A3A2(J)	
CLOSED LOOP	A3A2(8)	A3(B)*
COUNT	A3A2(9)	A7(F)*
SHIFT RIGHT	A3A2(10)	A7(J)*
SHIFT IN	A3A2(11)	
SHIFT LEFT	A3A2(12)	A7(H)*
$\overline{\text{SHIFT CLOCK}}$	A3A2(13)	AI2(P)
$\overline{\text{CLEAR}}$	A3A2(14)	A7(E)
$\overline{\text{COUNT UP}}$	A3A2(16)	A5(M)
$\overline{\text{COUNT DOWN}}$	A3A2(17)	
$\overline{\text{CI9SI8}}$	A3A7(19)	AI2(V)
$\overline{\text{PAR} \leftarrow \text{PAR}+1}$	A3A9(4)	AI3(T)
$\overline{\text{PAR} \leftarrow \text{PAR}-1}$	A3A9(5)	AI3(16)
$\overline{\text{PAR} \leftarrow \text{PAR}+2}$	A3A9(6)	
$\overline{\text{PAR} \leftarrow \text{PAR}+4}$	A3A9(7)	
SHIFT IN	A3A9(8)	
SHIFT RIGHT	A3A9(9)	
DAR ← PAR	A3A9(10)	
COUNT PAR	A3A9(11)	AG(B)
$\overline{\text{SHIFT}}$	A3A9(12)	
$\overline{\text{DAR} \leftarrow \text{DAR}+1}$	A3A9(P)	AI0(R)
$\overline{\text{CLEAR PAR}}$	A3A9(U)	AG(F)*
SYNC ON MCS	AG(U)	

NAME	LOC	5486 ORIGIN * INDIRECT
$\overline{\text{SET PAR}}$	A3A9(17)	AI3(E)
$\overline{\text{CLEAR DAR}}$	A3A9(18)	AI3(20)
$\overline{\text{SET DAR}}$	A3A10(V)	AI3(5)
DAR → HOLD	A3A9(19)	AI3(C)
PAR → HOLD	A3A9(20)	AI3(3)
ACCUM → HOLD	A3A9(21)	
$\overline{\text{READ}}$	A2AI3(11)	AI7(B)
$\overline{\text{WRITE}}$	A2AI3(8)	AI7(C)
$\overline{\text{CYCLE}}$	A2AI3(6)	AI7(D)
READ	A2AI3(2)	
STROBE	A2AI3(13)	
WRITE	A2AI3(5)	
$\overline{\text{INHIBIT}}$	A2AI3(4)	
$\overline{\text{SET MSB}}$	A2A10A(S)	AI7(L)
$\overline{\text{SET}}$ #	A2A10A(T)	
$\overline{\text{SET VERT}}$	A2A10A(U)	AI7(K)
$\overline{\text{SET HORIZ}}$	A2A9B(I)	AI7(M)

1. COUNT UP PULSES WILL APPEAR AT MCS INPUT RATE FROM 2.6µs OF ONE MCS PROGRAM TO 0.2µs OF THE NEXT MCS PROGRAM
2. IF 1000 PAR 1007
3. MCS SAWTOOTH (TRI, EVERY OTHER PROCESS) ON 5480A MODELS BELOW 928-00176
4. MCS TRIANGULAR ONLY ON 5480A MODELS BELOW 928-00176

02650-1

Figure 4-6. Test Points Multichannel Scaling (MCS) Program (Cont'd)

5486A/B Signals, MCS Program:

LOCATION	SIGNAL
A6(2)	Always high
A5(3)	Always low
A5(L)	Always low
A5(M)	5480A: May be pulses occurring from T26 of one MCS program to T2 of succeeding MCS program
A5(N)	Always high
A5(P)	Always high
A5(R)	Always high
A6(B)	Pulse at TØ if processing
A6(C)	Always high
A6(D)	Pulse at TØ
A6(E)	Pulse at T80
A6(F)	Always high
A6(H)	Always low
A6(J)	Always high
A6(K)	Always high
A6(20)	Always high
A7(5486B only)	
A7(B)	Pulse at T4
A7(C)	Pulse at T90
A7(D)	Always high
A7(E)	Pulse at T2
A7(F)	Pulse at T4
A7(H)	Always high
A7(J)	Always high
A7(K)	Pulse at T12
A7(L)	Pulse at T12
A7(M)	Pulse at T2
A7(N)	Always high
A7(5486A only)	
A7(B)	Pulse at T16
A7(C)	Pulse at T4
A7(D)	Always high
A7(E)	Pulse at T14
A7(F)	Pulse at T4
A7(H)	Always high
A7(J)	Always high
A7(K)	Pulse at T4
A7(L)	Pulse at T4
A7(M)	Pulse at T14
A7(N)	Always high

LOCATION	SIGNAL
A9(B)	Always high
A9(C)	Always high
A9(E)	Always low
A9(F)	Always high
A9(H)	Always high
A9(M)	5486B: Pulse at T94; 5486A: Pulse at T90
A9(U)	Always high
A9(V)	Always high
A9(W)	Always high
A9(X)	Pulse at T90
A9(Y)	Always high
A10(C)	Always high
A10(D)	Low; goes high at T40
A10(E)	High if PRESAMPLE high Will go low at T40 after PRESAMPLE goes low
A10(9)	Pulse at T98
A10(10)	Pulse at T98
A10(11)	Always low
A10(12)	Always high
A10(N)	Pulse at T98
A10(13)	Always high
A10(16)	Pulse at T98
A10(R)	Pulse at T12
A10(U)	Always high
A13(B)	Low is displaying
A13(C)	High if processing
A13(5)	High; pulse at T94 if displaying and address register is 1000 or greater.
A13(E)	High; pulse at T94 if address reg. is at 1000 or more.
A13(F)	Always high
A13(H)	Always high
A13(J)	Always high
A13(P)	High; pulse at T90 if address register is being reset from 1023 to Ø.
A13(16)	High; 5480A/5486A only: Pulse at T4 if SAWTOOTH/TRIANGLE is set to TRIANGLE. 5480A/5486A only: Pulse at T16 is processing and address is between 1000 and 1023 and SAWTOOTH/TRIANGLE is set to TRIANGLE.
A13(W)	Always high
A13(20)	High; pulse at T16 if: 1) Address reg. is between 1000 and 1023 and 2) 5480 is displaying and 3) PROCESS START is lighted.

Table 4-2. Wiring Lists

DESCRIPTION

The wiring lists in this table enable you to locate any signal in a 5480A/B system and follow its path throughout the system.

The table is divided into several parts, as listed below.

PART A is a signal dictionary, listing all signals in alphabetical order by name, and providing the following information about each signal:

1. What it does
2. What units of a 5480A/B system have this signal, e.g., what other sections of the list provide additional wiring information about the signal path.

PARTS B THROUGH J provide wiring lists for each section of the 5480A/B and for each plug-in. Each of these lists is independent of the other lists (except for cross-reference information in the "REMARKS" column) and provides the following information about each signal:

1. The source of the signal for the given unit or section; note that this is not necessarily the the original source for that signal, and you may be referred to another list to find the primary source.
2. All places in the given section or unit where the signal is connected (including, in some cases, board connector pins used as tie points).
3. Cross-reference information for signals that are in more than one list.

The wiring lists in this table can be used with the wiring diagrams that follow the table. The chart below provides cross-reference information for you.

Wiring list Part ___	and Wiring Diagram of Figure ___	Are for 5480A/B Section or unit listed below
B	4-7	Display Section (A1)
C	4-8	Memory Section (A2)
D	4-9	Main Frame Logic Section (A3)
E	4-10	Light Driver and Flip-Flop (A4) and Power Supply (A5) Sections
F	none	Connectors
G	4-11	5485A
H	4-12	5486A/B
I	4-13	5487A
J	4-14	5488A

ABBREVIATIONS

API = Analog Plug-In unit, which is a unit that plugs into the right-hand compartment of the 5480A/B. Current Analog Plug-In Units are: 5485A, 5487A, 5488A.

LD & FF = Light Driver and Flip-Flop, Section A4 of the 5480A/B

LPI = Logic Plug-In unit, which is a unit that plugs into the left-hand compartment of the 5480A/B. The 5486B unit should be used with the 5480A main frame, and the 5486A used with the 5480A main frame.

Table 4-2. Wiring Lists (Cont'd)

MEM = Memory section of 5480A/B
MFL = Main Frame Logic section of 5480A/B

CONNECTORS (REFERENCE DESIGNATIONS)

Connecting jacks (inter-connecting or interfacing) are numbered as follows:

P/J21	Power connection between 5480A/B and LPI
P/J22	Logic connection between 5480A/B and LPI
P/J23	Connections between LPI and 5480A/B rear-panel connectors
P/J24	Connections between LPI and API via 5480A/B (and P/J25)
P/J25	Connections between API and LPI via 5480A/B (and P/J24)
P/J26	Connections between API and 5480A/B rear-panel connectors, sections A2 and A3, and LPI
P/J27	Connections between API and 5480A rear-panel connectors
P/J28	Power connection between 5480A/B and API
P/J1	Connections between Memory (A2) and Main Frame Logic (A3) sections
P/J2	Connections between Memory section (A2) and 5480A/B rear-panel connectors
P/J3	Power connections to/from Memory Section

HOW TO USE THE WIRING LISTS

Suppose you want to know everything about the $\overline{\text{CYCLE}}$ signal.

1. Referring to the alphabetical listing in PART A, you will learn that:
   a. There are two $\overline{\text{CYCLE}}$ signals, one from an external source, and one from an internal source.
   b. The external signal source is listed only in the wiring list for 5480A/B Section 2, at line 38.
   c. The internal signal source is listed in 5480A/B Section 2, line 37, and 5486A/B, line 119.
2. Refer now to the 5480A/B Wiring List (Parts B through E)
   a. The LINE column is used only to provide a means for signal referencing
   b. Find LINE 37 of 5480A/B Memory Section A2 (Part C)
   c. SIGNAL NAME is listed as $\overline{\text{CYCLE}}$
   d. SIGNAL SOURCE is listed as P2(20), which translates to pin 20 of connector P2. This is the signal source for this section.
   e. The only place this signal is connected in the Memory Section is to board A13(6)
   f. Connectors P2/J2(20) rout this signal to the memory deck from J23(20), and we are referred to the 5486A/B wiring list, LINE 119.
   g. Find LINE 119 of the 5486A/B wiring list (Part H)
   h. The SIGNAL NAME is still listed as $\overline{\text{CYCLE}}$
   i. The SIGNAL SOURCE is listed as A7(D), which means that in the 5486A/B, this is the source.
   j. Moving across LINE 119, you will see that the only place this signal appears is at A7(D) and P23(20).

Table 4-2. Wiring Lists (Cont'd)

3. Summarizing what you learned about the $\overline{\text{CYCLE}}$ signal in Step 2,
   a. There are two $\overline{\text{CYCLE}}$ inputs to the 5480A/B Memory Section, one from an external source, and the other from the Logic Plug-in. The $\overline{\text{CYCLE}}$ signal causes the memory to perform a READ-WRITE cycle so memory contents are retained.
   b. The internal $\overline{\text{CYCLE}}$ signal originates at 5486A/B A7(D) and is routed through P/J23(20) and J2/A2P2(20) to A2A13(6) in the 5480A/B Memory Section. This signal is connected to no other points.

PART A – SIGNAL DICTIONARY

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
AA	Quarter Select Sw. - True in quarter 1, first half						52			52
AB	Quarter Select Sw. - True in quarter 2, first half						59			59
A+B/ALT							13			
A DATA SIGNAL							48			48
A DISP							69			69
A GAIN									70	
"A" INPUT SIGNAL							71			71
"A" NOISE SIGNAL							70			70
A OFF (A ON/OFF)							47		47	47
"A" POLARITY							9			9
"A" POSITION							75			75
"A" VERNIER							74			74
AC18	Accumulator Bit 18 Control			96				196		
AC Ø	Accumulator Bit 0		52	97						
AC 1	Accumulator Bit 1		53	98						
AC 2	Accumulator Bit 2		54	99						
AC 3	Accumulator Bit 3		55	100						
AC 4	Accumulator Bit 4		56	101						
AC 5	Accumulator Bit 5		57	102						
AC 6	Accumulator Bit 6		58	103						
AC 7	Accumulator Bit 7		59	104						
AC 8	Accumulator Bit 8		60	105						
AC 9	Accumulator Bit 9		61	106						
AC 1Ø	Accumulator Bit 10		62	107						
AC 11	Accumulator Bit 11		63	108						
AC 12	Accumulator Bit 12		64	109						
AC 13	Accumulator Bit 13		65	110						
AC 14	Accumulator Bit 14		66	111						
AC 15	Accumulator Bit 15		67	112						
AC 16	Accumulator Bit 16		68	113						
AC 17	Accumulator Bit 17		69	114						
AC 18	Accumulator Bit 18		70	115						
AC 19	Accumulator Bit 19		71	116						
AC 2Ø	Accumulator Bit 20		72	117						
AC 21	Accumulator Bit 21		73	118						
AC 22	Accumulator Bit 22		74	119						
AC 23	Accumulator Bit 23		75	120						

PART A (Cont'd) Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
$\overline{\text{AC Ø}}$	Accumulator Bit 0, True = 0			121						
$\overline{\text{AC 3}}$	Accumulator Bit 3, True = 0			122						
$\overline{\text{AC 4}}$	Accumulator Bit 4, True = 0			123						
$\overline{\text{AC 7}}$	Accumulator Bit 7, True = 0			124						
$\overline{\text{AC 8}}$	Accumulator Bit 8, True = 0			125						
$\overline{\text{AC 11}}$	Accumulator Bit 11, True = 0			126						
$\overline{\text{AC 12}}$	Accumulator Bit 12, True = 0			127						
$\overline{\text{AC 15}}$	Accumulator Bit 15, True = 0			128						
$\overline{\text{AC 16}}$	Accumulator Bit 16, True = 0			129						
$\overline{\text{AC 19}}$	Accumulator Bit 19, True = 0			130						
$\overline{\text{AC 2Ø}}$	Accumulator Bit 20 True = 0			131						
$\overline{\text{AC 23}}$	Accumulator Bit 23 True = 0			132						
AC TO HOLD	Grounded			165						
ADC FIN	Analog-to-Digital Converter finished True = 1							104		
$\overline{\text{ADC FIN}}$	Analog-to-Digital Converter finished True = 0						84	103	84	84
ADVANCE DAR+1	Advance display address by one			181				165		
ADVANCE PAR+4	Advance process address register by 4 (not used at present)			184						
ADVANCE PAR+4	Advance process address register by 4 (ext source)			216						
$\overline{\text{ADVANCE PAR 3}}$	Advance process address by 3							164		
ADVANCE PAR+2	Advance process address register by 2 (not used at present)			183						
ADVANCE PAR+2	Advance process address by 2 (from ext source)			217						
ADVANCE PAR 2	Advance process address register 2							101		
ADVANCE PAR+1	Advance process address register by 1			185				205		

PART A (Cont'd)

Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
ADVANCE PAR+1	Advance process address by one (from ext source)			186						
ADV PAR 1	Advance process address register 1							95		
$\overline{\text{ADVANCE PAR -1}}$	+5			187				206		
$\overline{\text{ADVANCE PAR -1}}$	+5			188						
$\overline{\text{ALLOW STATE}}$								115		
$\overline{\text{AR Ø}}$	Process address register or display address register bit 0		10	193			41		41	41
$\overline{\text{AR 1}}$	Process address register or display address register bit 1		11	194			42		42	42
$\overline{\text{AR 2}}$	Process address register or display address register bit 2		12	195						
$\overline{\text{AR 3}}$	Process address register or display address register bit 3		13	196						
$\overline{\text{AR 4}}$	Process address register or display address register bit 4		14	197						
$\overline{\text{AR 5}}$	Process address register or display address register bit 5		15	198						
$\overline{\text{AR 6}}$	Process address register or display address register bit 6		16	199						
$\overline{\text{AR 7}}$	Process address register or display address register bit 7		17	200						
$\overline{\text{AR 8}}$	Process address register or display address register bit 8		18	201						
$\overline{\text{AR 9}}$	Process address register or display address register bit 9		19	202						
AVE	Average mode							83		
"B"-DATA	Disp. Sw. Mem. "B" on data						55			55
"B" GAIN									72	
"B" INPUT SIGNAL	Disp. Sw. "B" Channel on input						73			73
BIT NO. 1										102
BIT NO. 2										103
BIT NO. 3										104
BIT NO. 4										105

PART A (Cont'd)

Table 4-2: Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
"B" NOISE SIGNAL	Display Sw. "B" Channel on noise						72			72
"B" ON/OFF									48	
"B" OFF	Display Sw "B" Channel on "Off"						54			54
"B" POLARITY	B Channel + or - Sw. Setting						10			
"B" POSITION	Pot Adjust						77		73	77
"B" VERNIER	Pot Adjust						76			76
BASELINE ADJ	Pot Adjust						20		20	20
BA	Switch Setting						51			51
BB	Switch Setting						58			58
CA	Switch Setting						50			50
CALIBRATOR	Internal 1V square wave signal (to CAL out jack	20								
CAL ZERO	Level from calibrate switch (GND level in zero position)		22							
CAL FULL	Level from calibrate switch (GND when switch in full)		21							
CAR Ø	Lines to horiz. hold reg. after MPX with DAR-to-PAR and EXT Commands		27							
CAR 1			28							
CAR 2			29							
CAR 3			30							
CB	Switch Setting						57			57
"C" GAIN									74	
CHAN "A"	Tells input amp to look at Channel A input						14			14
CHAN A	(Not used)							14		
CHANNEL COMMAND	Ext source to control what channels the ADR will be looking at						40		40	40
CHAN OK	Determines if front panel switches are set for correct channel to process data						61	137	61	61
CLAC 19 - SET AC 18	Clear accumulator bit 19, set accumulator bit 18			215				192		
$\overline{\text{CLEAR}}$	Reset for time base (TB_1, TB_2) MBBL							32		
$\overline{\text{CLEAR 1}}$	Clear accumulator			13						

PART A (Cont'd)

Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
$\overline{\text{CLEAR 1}}$	Clear accumulator when in display. Prepare, 4 begin, or 4 end.			12				120		
$\overline{\text{CLEAR 2}}$	Clear accumulator			34						
CLEAR ACCUM	From pushbutton switches (front panel) 0V when both pushed in				1					
CLEAR DAR A	Clear display address register (low when T16, PSD1, EN PAR to hold reg, start lights are high			154				207		
CLEAR DAR B	Clear display address register (A3A10-12) occurs same time as clear DAR A			167						
CLEAR HORIZ HOLD	Clear horizontal hold register		127							
CLEAR HOLD	Clear hold register containing shift information							99		
CLEAR PAR A	Clear process address register A (from logic plug-in)			153				109		
CLEAR PAR A	Clear process address register A (from external source)			214						
CLEAR PAR B	Clear process address register, occurs same time clear PAR A			166						
CLOCK 1	Clocks into buffer storage for horizontal DAC (first 4 bits)		31							
CLOCK 2	Clocks information into buffer storage of 4 DAC (bits 4-9)		32							
CLOSED LOOP	(Not used - closes loop in accumulator so information will not be lost during shifting)			33						
"C" ON/OFF CORRELATION COUNT	Control line to all accumulators to enable the accumulators to count.			26					49	9

PART A (Cont'd)

Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
COUNT DN A	Count down in accumulators (from EXT source)			24						
COUNT DN B	Count down in high speed accumulator			37						
COUNT DN C	Count down carry line from high speed accumulator board			39						
COUNT DN D	Count down carry line from second decade accumulator			41						
COUNT DN E	Count down carry from third decade counter			43						
COUNT DN ENABLE/GD DN 20 MHz PAR	Allows accumulator to count down (from logic plug-in)			22, 191			32	210	32	32
COUNT DN F	Count down carry from fourth decade of accumulator			45						
COUNT DN G	Count down carry from fifth decade of accumulator			47						
$\overline{\text{COUNT DN}}$ PAR A	Carry down from process address register			207						
COUNT DN PAR B	Carry line from process address register			211						
COUNT DN PAR C	Carry down from process address register			213				199 (A only)		
COUNT PAR	To enable process address register to count			159						
COUNT UP A	Enables first accumulator to count			20				100		
COUNT UP B	Enables count for high speed accumulator			36						
COUNT UP C	Carry from accumulator to next lower one to enable count			38						
COUNT UP D	Enables count in accumulator (carry line from higher decade)			40						

PART A (Cont'd) Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
COUNT UP E	Enable count in accumulator (carry from previous accumulator)			42						
COUNT UP F	Enable count in accumulator (carry line from previous stage)			44						
COUNT UP G	Enables count in accumulator (carry from previous stage)			46						
COUNT UP DAR A	To enable count up in display address register			203						
COUNT UP DAR B	Count up by one in display register			204						
COUNT UP ENABLE/GATED UP 20 MHz PAR/ GD UP 20 MHz DAR	Gate 20 MHz to PAR to count			16, 189			33	211	33	33
COUNT UP PAR B	Carry up line from process address register			210						
COUNT UP PAR C	Carry up line from process address register			212				10		
$\overline{\text{COUNT UP PAR A}}$	Carry up line from process address register			206						
"C" POSITION CS ATTACHED	(Not used)							75 107 (A only)		
CS ATTACHED	From EXT source - Not used						79		79	79
$\overline{\text{CYCLE}}$	To enable memory cycle (read-write)		37					119		
$\overline{\text{CYCLE}}$	From EXT source to control memory cycle time		38							
D1 DISP MULT D2 DISP MULT									11 12	
DA							49			49
DAR TO HOLD	Enables word in display address reg. to be held in hold reg.			164						
DAR TO PAR	Enables line to transfer display reg. contents into process reg.			162						

PART A (Cont'd) Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
DATA SIGNAL	– Signal from memory to output amp.						26		26	26
DB	– Switch Setting						56			56
DC BAL	– Pot Adjust						21		21	21
DC BAL A	– Pot Adjust						11			
DC BAL B	– Pot Adjust						12			
"D" GAIN									76	
DISPLAY	– Line from program selector board to enable 5480A/B to display a point							81		
DISPLAY DEFEAT	– Blanks CRT						62	162	62	62
DISPLAY LAMP DR.	– From transistor driver to light display light during display mode				16					
DISPLAY PBH	– Enables display rout.				21	21		151		
DISPLAY PBM	– From display sw. btn.				14	14				
DISP SW DATA									51	
DISP SW INPUT									53	
DISP SW NOISE									52	
"D" ON/OFF									50	
"D" POSITION									77	
EA	Switch Setting						53			53
EB	Switch Setting						60			60
EN CDN 20 MHz	(From EXT source) control line to enable 20 MHz clock - to count down lines			23						
ENABLE AC TO HOLD	Enable accumulator contents to the hold register			152						
ENABLE COUNT	Control line from EXT source to enable count in accumulators			4						
ENABLE COUNT	Enable count in accumulator for all functions (SUM - AUG - MCS H BEG, END, PREP)			3				125		
ENABLE COUNT DN 4	From EXT source to enable accumulator to count down			25						
ENABLE COUNT PAR	Enable process address register to count			142						
ENABLE COUNT UP A	Enables accumulators to count up			21			85		85	85

PART A (Cont'd) Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
ENABLE DAR TO HOLD	Enables display register contents to transfer to hold register			151				204		
ENABLE DAR TO PAR	Enables display register contents to transfer to process register			148						
ENABLE DAR TO PAR	From EXT source to enable display register contents to transfer to process register			149						
ENABLE EXT TB	Enable line to allow an external time base							42		
ENABLE OPEN LOOP	(Not used)			26						
ENABLE OPEN LOOP	From EXT source to accumulator control board			27						
ENABLE PAR TO HOLD	From EXT source to transfer contents of process register to hold register			192						
ENABLE PAR TO HOLD	Enable process register contents to transfer to hold register			15Ø				197		
ENABLE 20 MHz/ SW HIST	Enable 20 MHz clock for counting in histogram mode			18			43	150	43	43
ENCLOSED LOOP/ EN COUNT PAR				11, 143				108		
ENCUP 20 MHz	Enable count up (20 MHz clock) from EXT source			17						
ENSHIFT IN	(Not used)			9						
ENSHIFT IN	From EXT source			10						
ENSHIFT IN PAR	From EXT source to enable shifting in process address register			146						
ENSHIFT IN PAR	(Not used)			147						
ENSHIFT LEFT	Enables accumulators to shift left			5				124		
ENSHIFT LEFT	From EXT source			6						

PART A (Cont'd) Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
ENSHIFT RIGHT	Enables accumulators to shift right			7				123		
ENSHIFT RIGHT	From EXT source			8						
ENSHIFT RT PAR	From EXT source			144						
ENSHIFT RT PAR	(Not used)			145						
EXT AC Ø	EXT bit to accumulator			72						
EXT AC 1	(Input) EXT accumulator bit			73						
EXT AC 2	(Input) EXT accumulator bit			74						
EXT AC 3	(Input) EXT accumulator bit			75						
EXT AC 4	(Input) EXT accumulator bit			76						
EXT AC 5	(Input) EXT accumulator bit			77						
EXT AC 6	(Input) EXT accumulator bit			78						
EXT AC 7	(Input) EXT accumulator bit			79						
EXT AC 8	(Input) EXT accumulator bit			80						
EXT AC 9	(Input) EXT accumulator bit			81						
EXT AC 1Ø	(Input) EXT accumulator bit			82						
EXT AC 11	(Input) EXT accumulator bit			83						
EXT AC 12	(Input) EXT accumulator bit			84						
EXT AC 13	(Input) EXT accumulator bit			85						
EXT AC 14	(Input) EXT accumulator bit			86						
EXT AC 15	(Input) EXT accumulator bit			87						
EXT AC 16	(Input) EXT accumulator bit			88						
EXT AC 17	(Input) EXT accumulator bit			89						
EXT AC 18	(Input) EXT accumulator bit			90						
EXT AC 19	(Input) EXT accumulator bit			91						

PART A (Cont'd)

Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
EXT AC 2Ø	(Input) EXT accumulator bit			92						
EXT AC 21	(Input) EXT accumulator bit			93						
EXT AC 22	(Input) EXT accumulator bit			94						
EXT AC 23	(Input) EXT accumulator bit			95						
EXT ARØ	(Input) EXT address register bit			171						
EXT AR 1	(Input) EXT address register bit			172						
EXT AR 2	(Input) EXT address register bit			173						
EXT AR 3	(Input) EXT address register bit			174						
EXT AR 4	(Input) EXT address register bit			175						
EXT AR 5	(Input) EXT address register bit			176						
EXT AR 6	(Input) EXT address register bit			177						
EXT AR 7	(Input) EXT address register bit			178						
EXT AR 8	(Input) EXT address register bit			179						
EXT AR 9	(Input) EXT address register bit			180						
EXT SAMPLE	(Input) EXT sample command						94		94	94
+EXT TRIG LINE	Line to enable input buffer for positive trigger input							6		
$\overline{\text{EXT AVE}}$	(Input) EXT average command							105		
$\overline{\text{EXT PREP}}$	(Input) to control prepare line							106		
FREQ HISTOGRAM	From histogram switch						82		82	82
$\overline{\text{FREQ HIST}}$	Line to enable histogram program						86	159	86	86
GRD	Ground	12								
GRD	Ground		5							
GRD	Ground			2						

PART A (Cont'd)

Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
GRD	Ground				9	9				
GRD	Ground						4		4	4
GRD	Ground							4		
HIST BEGIN	Histogram begin program							88		
HIST END	Histogram end program							93		
HORIZ DAC	Horiz. DAC output		42				89		89	89
HORIZ DEFL		3								
HORIZ POS	Pot Adjust	17								
I1 INPUT MULT		3							13	
I2 INPUT MULT		17							14	
$\overline{\text{INHIBIT STATE}}$	Do not allow state							114		
$\overline{\text{INHIBIT TIME}}$	Part of mem. cycle to allow inhibit time		45							
INPUT A	Sig. input line to Channel "A"						7		7	7
INPUT B	Sig. input line to Channel "B"						8		8	8
INPUT C	Sig. input line to Channel "C"								9	
INPUT D	Sig. input line to Channel "D"								10	
INPUT AMPL. OUTPUT	Signal output line to sample and hold LRC						15		15	15
INTENSIFY	(Not used)	18								
INTENSITY MOD	(Not used)	16								
INT TRIGGER	Sw. Setting line - indicates when using internal trigger							7		
L START	Level - indicates when start lite is on				30	30		84 (A only)		
L START A	If lite start is on or EXT source wants to turn on start lite - L START A is high							85 (A only)		
L CONTINUE	(Not used)							161		
L DISPLAY	High level when lite display is on				19	19	46	139		146
$\overline{\text{L DISPLAY}}$	Low level when lite display is on							190		
L RECORD	High level when lite record is on				24	24	93	145	93	93
L STOP	High when lite "STOP" is on				20	20	83	153	83	83

PART A (Cont'd)

Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
$\overline{\text{L STOP}}$	Low level when lite "STOP" is on							116		
LINE SYNC	From transformer to provide 60 cycles for a line sync					33		212		
MA Ø	Memory address register bit 0		102							
MA 1	Memory address register bit 1		104							
MA 2	Memory address register bit 2		106							
MA 3	Memory address register bit 3		108							
MA 4	Memory address register bit 4		110							
MA 5	Memory address register bit 5		112							
MA 6	Memory address register bit 6		114							
MA 7	Memory address register bit 7		116							
MA 8	Memory address register bit 8		118							
MA 9	Memory address register bit 9		120							
$\overline{\text{MA Ø}}$	Memory address register bit 0 (compl. out)		103							
$\overline{\text{MA 1}}$	Memory address register bit 1 (compl. bit 1)		105							
$\overline{\text{MA 2}}$	Memory address register bit 2 (compl. out)		107							
$\overline{\text{MA 3}}$	Memory address register bit 3 (compl. out)		109							
$\overline{\text{MA 4}}$	Memory address register bit 4 (compl. out)		111							
$\overline{\text{MA 5}}$	Memory address register bit 5 (compl. out)		113							
$\overline{\text{MA 6}}$	Memory address register bit 6 (compl. out)		115							

PART A (Cont'd)

Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
$\overline{\text{MA 7}}$	Memory address register bit 7 (compl. out)		117							
$\overline{\text{MA 8}}$	Memory address register bit 8 (compl. out)		119							
$\overline{\text{MA 9}}$	Memory address register bit 9 (compl. out)		121							
$\overline{\text{MAAR Ø}}$	Memory switch setting (Looks)		131				66		66	66
$\overline{\text{MAAR 1}}$			133				63		63	63
MAIN SRQ	Main service request							193		
$\overline{\text{MBAR Ø}}$			130				65		65	65
$\overline{\text{MBAR 1}}$			132				64		64	64
MBSL	Main box slaved (EXT command)							39		
MBSSL	Main box sort of slaved (EXT)		50					201		
MCS	Level - indicates multi channel scale on							92		
MCS COUNT UP	Level - count up in multi channel scale						99	90	99	99
MCS INPUT	Signal input line for MCS mode						91		91	91
MOD HOLD	Horiz. hold register (EXT command)		51							
MM 1	Indicates if memory is being exercised		47							
MM 2	Indicates if memory is being exercised		48							
NEG EXT TRIGGER	Level - indicates pos. for neg. EXT trigger							5		
NEG SYNC OUT	Rear panel output for neg. trigger						98		98	98
NINE BITS	Any setting past 2 millisec/cm 16 9-bit ADC resolution - except EXT						35	180	35	35
NOISE SIGNAL	Output from sample-hold board to output amplifier to show noise on CRT						24		24	24

PART A (Cont'd)

Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
NON-PROCESS	Mode of operation where no processing takes place							142		
NORMAL	From Normal/ Preset Sw. /high in normal							147		
OPEN LOOP	Instruction during shifting in accumulator			32						
$\overline{\text{OUTPUT MPX}}$	To turn on output multiplier							11Ø		
OVERLAY	Overlap instruction						67			67
$\overline{\text{PAD FIN}}$	(Not used)						15		15	15
PAD OFF	Post analysis delay off						11		11	11
PAR TO HOLD	Contents of process address to hold register			163						
$\overline{\text{PAR Ø}}$	Process address register bit 0			205				(A only) 144		
PBH CONTINUE	(Not used)							94		
P/$\overline{\text{D}}$	Process and not display							208		
PEN LIFTER	Level - commands plotter pen to lift on retrace									
PLOT	Level to instruct plotter to plot						92		92	92
PLUG IN SYNC CONT	(Not used)							13		
POINT NO. 1										107
POS SYNC OUT	To rear panel - positive sync output pulse						97		97	97
POST ANAL DELAY	From switch - indicates pad is on or off							12		
POWER SENSE	(AC) from A5T1 transformer		76			36				
POWER SENSE	(AC) from A5T1 transformer		77			37				
PRADX1	Pre-analysis delay X1							19		
PRADX2	Pre-analysis delay X2							17		
PRADX5	Pre-analysis delay X5							18		

PART A (Cont'd)

Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
PRADX1Ø	Pre-analysis delay X10							2Ø		
PRADX1ØØ	Pre-analysis delay X100							21		
PRADX 1K	Pre-analysis delay X1K							22		
PREPARE	Level to indicate in prepare program							87		
PRESET REACHED	Level indicates when a preset number has been reached							148		
PRE SAMPLE A	Level occurring 10 μsec before sample pulse							35		
PRESET SHIFT CONT	Determined by sweep switch as to how far to shift in the accumulator							96		
PRESET TOTAL	High when counts match switch setting (for histogram mode)			139				149		
PRESET TOTAL 10^2	Switch setting of preset totalizer			133				74		
PRESET TOTAL 10^3	Switch setting - preset totalizer			134				75		
PRESET TOTAL 10^4	Switch setting - preset totalizer			135				76		
PRESET TOTAL 10^5	Switch setting - preset totalizer			136				77		
PRESET TOTAL 10^7	Switch setting - preset totalizer			138				79		
PROCESS	Enable line telling unit to process							141		
$\overline{\text{PROCESS INHIBIT}}$	Inhibits processing of data							163		
PRODUCT $\overline{\text{PSD1}}$	For prepare mode, determines a channel between 1000 and 1019			141				198		12
$\overline{\text{PSD2}}$	For prepare mode, determines a channel between 1020 and 1023			140				138		

PART A (Cont'd)

Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
RAMP FIN	ADC ramp is done						31		31	31
$\overline{\text{READ}}$	Part of memory timing - read portion		33					127		
$\overline{\text{READ}}$	From EXT source to induce memory to read		34							
$\overline{\text{READ TIME}}$	Stays down for that portion of memory cycle for reading		44							
RECORD LAMP DR	From transistor driver for record lite				17					
RECORD PBH	Level - high when record lite on				22	22		152		
RECORD PBM	Line from record pushbutton - low when pushed in				18	18		200		
+REF	Voltage reference for baseline offset in summation						22		22	22
-REF	Voltage reference for baseline offset in summation						23		23	23
$\overline{\text{RESET}}$	Reset to a flip/flop, for looking at pre-analysis/sweeptime switch settings							31		
$\overline{\text{RESET ADC}}$	Reset ADC at beginning of each sample						30	117	30	30
RESET LAMP DRIVE	From transistor driver for reset lamp driver				12					
RESET TB1	Reset timebase 1						90	38	90	90
RESET TB2	Reset timebase 2							40		
$\overline{\text{SAAR0}}$	EXT control of address register 0		125				39		39	39
$\overline{\text{SAAR1}}$	EXT control address register bit 1		123			36				
$\overline{\text{SAAR2}}$	EXT control of address register bit 2		128							
$\overline{\text{SAAR3}}$	EXT control of address register bit 3		129							

PART A (Cont'd)

Table 4-2. Wiring Lists (Cont'd).

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
SAMPLE							100	41	100	100
SAMPLE	Level - instructs to sample input signal							140		
SAMPLED SIGNAL	Input signal to output amplifier for viewing on CRT						25		25	25
SAMPLE INTERV, SAWTOOTH/ TRIANGLE	From switch rear panel for MCS mode (discontinued on newer units)							195 (A only)		11
$\overline{\text{SA 0}}$	Set accumulator 0 (from sense line)		78	48						
$\overline{\text{SA 1}}$	Set accumulator 1 (from sense line)		79	49						
$\overline{\text{SA 2}}$	Set accumulator 2 (from sense line)		80	50						
$\overline{\text{SA 3}}$	Set accumulator 3 (from sense line)		81	51						
$\overline{\text{SA 4}}$	Set accumulator 4 (from sense line)		82	52						
$\overline{\text{SA 5}}$	Set accumulator 5 (from sense line)		83	53						
$\overline{\text{SA 6}}$	Set accumulator 6 (from sense line)		84	54						
$\overline{\text{SA 7}}$	Set accumulator 7 (from sense line)		85	55						
$\overline{\text{SA 8}}$	Set accumulator 8 (from sense line)		86	56						
$\overline{\text{SA 9}}$	Set accumulator 9 (from sense line)		87	57						
$\overline{\text{SA 10}}$	Set accumulator 10 (from sense line)		88	58						
$\overline{\text{SA 11}}$	Set accumulator 11 (from sense line)		89	59						
$\overline{\text{SA 12}}$	Set accumulator 12 (from sense line)		90	60						
$\overline{\text{SA 13}}$	Set accumulator 13 (from sense line)		91	61						
$\overline{\text{SA 14}}$	Set accumulator 14 (from sense line)		92	62						
$\overline{\text{SA 15}}$	Set accumulator 15 (from sense line)		93	63						
$\overline{\text{SA 16}}$	Set accumulator 16 (from sense line)		94	64						
$\overline{\text{SA 17}}$	Set accumulator 17 (from sense line)		95	65						

PART A (Cont'd) Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE A1	A2	A3	A4	A5	5485A	5486A/B	5487A	5488A
SA 18	Set accumulator 18 (from sense line)		96	66						
SA 19	Set accumulator 19 (from sense line)		97	67						
SA 20	Set accumulator 20 (from sense line)		98	68						
SA 21	Set accumulator 21 (from sense line)		99	69						
SA 22	Set accumulator 22 (from sense line)		100	70						
SA 23	Set accumulator 23 (from sense line)		101	71						
SBAR Ø	EXT control of address register bit Ø		124				38		38	38
SBAR 1	EXT control of address register bit 1		122				37		37	37
SC 1	Shift control 1							167		
SC 2	Shift control 2							168		
SC 3	Shift control 3							169		
SC 4	Shift control 4							170		
SC 5	Shift control 5							171		
SC 6	Shift control 6							172		
SC 7	Shift control 7							173		
SC 9	Shift control 9							174		
SC 10	Shift control 10							175		
SC 11	Shift control 11							176		
SC 12	Shift control 12							177		
SC 13	Shift control 13							178		
SEEK	Control line for plotter/record mode						101		101	101
SEG	Segment						68			68
SENS MULT AUTO	Switch position (sens multiplier switch)							86		
SENS MULT 2^0	Switch setting (sens multiplier switch)							182		
SENS MULT 2^1	Switch setting (sens multiplier switch)							184		
SENS MULT 2^2	Switch setting (sens multiplier switch)							186		
SENS MULT 2^3	Switch setting (sens multiplier switch)							188		

PART A (Cont'd) Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE A1	A2	A3	A4	A5	5485A	5486A/B	5487A	5488A
SET AVG	Set average mode							128		
SET DAR	Set display address register		126							
SET DAR B	Set display address register B			158				203		
SET DAR C	Set display address register C			170						
SET DISPLAY	Set display mode		24							
SET DISP	Set display mode (Compl. out)							133		
SET DISP MULT									45	
SET - HIST BEGIN	Set histogram begin program							131		
SET - HIST END	Set histogram end program							132		
SET HORIZ			40							
SET HORIZ			41					122		
SET IN MPX	Set input multiplex for correct channel input						44	111	44	44
SET - L DISPLAY	Set lite display				23	23		157		
SET - L RECORD	Set lite record				25			158		
SET - L START	Set lite start				29	29		154		
SET MCS	Set multi-channel scale							130		
SET MSB	Set most significant bit (sign)		39					118		
SET - NOP	Set no operation mode							135		
SET PAR A	Set process address register A			157				112		
SET PAR B	Set process address register B			169						
SET - PREPARE	Set prepare mode							134		
SET SCALE NUMBER	Enable line to set scale number switch setting (sens multiplier)							98		
SET SUM	Set summation mode							129		
SET SWEEP NUM								113		
SET VERT	Set vertical point for display	1	25				45	121		45
SET VERT			26							
SEVEN BITS	Sweep time of 2 ms/cm is 7-bit information from ADC						34	179	34	34

PART A (Cont'd)

Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
$\overline{\text{SHIFT 1}}$				14				191		
$\overline{\text{SHIFT 1}}$				15						
SHIFT 2				35						
SHIFT IN PAR	Shift in process address register			161						
SHIFT IN				31						
SHIFT LEFT				29						
SHIFT PAR A	Shift process address register A			155						
SHIFT PAR A	Shift process address register A			156						
SHIFT PAR B	Shift process address register B			168						
SHIFT RIGHT				30						
SHIFT RT PAR				160						
SHIFT RT PAR A				182						
SHIFT RT PAR B				208						
SHIFT RT PAR C				209						
$\overline{\text{SRT PAR B}}$/ SHIFT RT PAR B	Shift right in process address register	19		208						
START										106
START ADC							27	73	27	27
START LAMP DR.					31					
START PBH	Level high when start on				28	28		143		
START PBM	Switch - start push-button low when pushed in				32	32				
$\overline{\text{START-SHIFT}}$								97		
START (TØ)	Start time Ø						17	166	17	17
STATE ENABLED								136		
STOP LAMP DR.					15					
STOP PBH	Stop pushbutton level - high when stop on				26	26		146		
$\overline{\text{STOP}}$ PBM/$\overline{\text{SET-L}}$ $\overline{\text{STOP}}$	Indicates pushbutton being held down				13, 27	13				
STOP T (T12)	Terminates sample inter.						18	59	18	18
$\overline{\text{STROBE TIME}}$	Part of memory cycle (part of read portion)		43							
SUB S/RQ	Sub service request (EXT cont)							194		
SUM	Summation mode							82		

PART A (Cont'd)

Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
SW/AVE	Switch average						16	80	16	16
SWEEP NUM 2^0	Switch setting 2^0							181		
SWEEP NUM 2^1	Switch setting 2^1							183		
SWEEP NUM 2^2	Switch setting 2^2							185		
SWEEP NUM 2^3	Switch setting 2^3							187		
SWEEP NUM 2^4	Switch setting 2^4							189		
SWEEP VOLTAGE	Horizontal DAC out through shaping network for NMR work						96		96	96
$\overline{\text{SW HIST}}$	Histogram mode switch		49	190				209		
SW MCS	Multichannel scale switch							91		
SW SUM	Summation switch							102		
SW TX1	Sweep time switch (X1)							25		
SW TX2	Sweep time switch (X2)							23		
SW TX5	Sweep time switch (X5)							24		
SW TX1Ø	Sweep time switch (X10)							26		
SW TX1ØØ	Sweep time switch (X100)							27		
SW TX1K	Sweep time switch (K1K)							28		
$\overline{\text{SYNC}}$	Sync pulse for system							16		
TØ	Time slot Ø							56		
T2	Time slot 2 (.2 μsec after TØ)							57		
T4	Time slot 4 (.4 μsec after TØ)							58		
T14	Time slot 14 (1.4 μsec after TØ)							60		
T16	Time slot 16 (1.6 μsec after TØ)							61		
T26	Time slot 26 (2.6 μsec after TØ)							62		
T28	Time slot 28 (2.8 μsec after TØ)							63		
T34	Time slot 34 (3.4 μsec after TØ)							64		
T36	Time slot 36 (3.6 μsec after TØ)							65		

PART A (Cont'd)

Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
T4Ø	Time slot 40 (4.0 μsec after TØ)							66		
T5Ø	Time slot 50 (5.0 μsec after TØ)							67		
T58	Time slot 58 (5.8 μsec after TØ)							68		
T6Ø	Time slot 60 (6.0 μsec after TØ)							69		
T8Ø	Time slot 80 (8.0 μsec after TØ)							70		
T86	Time slot 86 (8.6 μsec after TØ)							71		
T9Ø	Time slot 90 (9.0 μsec after TØ)							72		
TB 1	Time base 1							44		
TB 2	Time base 2							45		
TB 3	Time base 3							46		
TB 4	Time base 4							47		
TB 5	Time base 5							48		
TB 6	Time base 6							49		
TB 7	Time base 7							50		
TB 8	Time base 8							51		
TB 9	Time base 9							52		
TB 1Ø	Time base 10							53		
TB 11	Time base 11							54		
TB 12	Time base 12							55		
TB B1	Coder to determine if 5-, 7-, or 9-bit ADC information						28	33	28	28
TB B2	Coder to determine if 5-, 7-, or 9-bit ADC information						29	34	29	29
10 MHz CLOCK	Divide-by-2 output from 20 MHz main clock						80	43	80	80
10 MS A	10 μsec pulses occurring after reset (clear)							30		
10 MS B	10 μsec pulses (one pulse less than 10 μsec at beginning)							29		
TIME HISTOGRAM	Switch setting - histogram						81		81	81
$\overline{\text{TIME HIST}}$	Level - low when in time histogram						87	160	87	87
TOTAL, PRESET 10^6	Switch setting 10^6			137				78		

PART A (Cont'd)

Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
TRIGGER INPUT	Signal input for trigger							8		
TRIGGER LEVEL	Pot Adjust							9		
20 MHz	Main clock frequency		20	19				37		
VARIANCE OUTPUT	Back panel - only with variance option (5488)						88		88	88
VERTICAL DAC	Back panel output of vertical DAC		23				19		19	19
VERT DEFL		2								
VERT DEFLECTION							78		78	78
$\overline{\text{WRITE}}$	Part of memory cycle - write portion		35					126		
$\overline{\text{WRITE}}$	From EXT source - to control write portion of memory cycle		36							
$\overline{\text{WRITE TIME}}$	High for length of time in write portion of memory		46							
X5 MAG SW	On main frame - to expand CRT display to X5	13								
X5 MAG SW	Switch setting	14								
Z AXIS	Output rear panel - for unblanking of EXT CRT	21					95		95	95
Z AXIS CRT	For unblanking of internal CRT	15								
+200V		8				8				
+200V		8								
+50V		9				6				
+50V		9								
+35V			9			35				
+19.5V			6		10		5		5	5
+16V			8			34				
+12V			1							
+12V							1		1	1
+12V								1		
+12V						2				
+12V		4								
+5V			3							
+5V				1	4	4				
+5								3		
+5V		6								
+5V							3		3	3
+5V				1						
+5V REF										10
-7.5V			4			5				

PART A (Cont'd)

Table 4-2. Wiring Lists (Cont'd)

SIGNAL NAME	DESCRIPTION	5480A/B SECTION AND LINE					5485A	5486A/B	5487A	5488A
		A1	A2	A3	A4	A5				
-7.5V			4							
-12V		5								
-12V						3				
-12V							2		2	2
-12V								2		
-12V			2							
-19.5V			7			11	6		6	6
-50V		7								
-50V		7				7				
-2950V		10								
-3000V		11								

PARTS B THRU E — 5480A/B Table 4-2 (Cont'd)

This part of the table lists all connections in the 5480A/B Memory/Display (Main Frame) units. This part of the table is divided into sub-parts, corresponding with other documentation that divides the instrument into 5 major sections:

- A1 Display Section
- A2 Memory Section
- A3 Main Frame Logic Section
- A4 Switching Logic (Light Driver and Flip-flop) Section
- A5 Power Supply Section.

The main body of the list for each section applies directly to the 5480B units. Any changes for 5480A are listed at the end of the portion of the list where they apply.

The shaded portions of this list indicate signals that were present in the 5480A's with serial prefix 852- and below but are not in newer instruments.

Table 4-2. Wiring Lists (Cont'd)

PART B 5480A B A1 DISPLAY SECTION Wiring Diagram: Figure 4-7

LINE	SIGNAL NAME	SIGNAL SOURCE	DEFLECTION AMPLIFIER A1	CALIBRATOR A2	HIGH VOLTAGE REGULATOR A4	J37	REMARKS
1	SET NUM	J2(41)	11				From LPI Line 121
2	VERT DEFL	J26(49)	6				To J29 Vert Scope Output
3	HORIZ DEFL	J26(45)	4				
4	+12V	A5A1(2)	9	912			
5	-12V	A5A1(4)	20				
6	-5V	A5A1(8)	12				
7	-50V	A5A2(14)	5		907		
8	-200V	A5A2(6)	1		222		
9	-50V	A5A2(5)			229		
10	-2950V	A1A4			444		To A1V1(2) CRT Cathode
11	-3000V	A1A4			555		To A1V1(3) CRT Grid
12	GRD	Chassis	17,19	SCRW	000		
13	X5 MAG SW	A1S1	3				
14	X5 MAG SW	A1S1	2				
15	Z AXIS CRT	A1A1(8)	8		936		
16	INTENSITY MOD	J16(9)	13				
17	HORIZ POS	A1R4	7				
18	INTEN-SIFY	J26(31)	14				
19	$\overline{\text{SRTPARB}}$	A3A11(R)		991			Note: BH 6 From PAR
20	CALI-BRATOR	A1A2(992)		992			To A1J1 CAL Signal 1V
21	Z AXIS	A1A1(15)	15			41	To API Line 95 & J11 Rear
22	SET V HOLD	J2(4)	10				From MEM Line 26

Note: 3 Digit Numbers Denote Wire Color Using Standard Color Code

5480A: Serials Prefixed 852 - And Below Had Signal Indicated By Shading.

Table 4-2. Wiring Lists (Cont'd)

PART C 5480A/B A2 MEMORY SECTION Wiring Diagram: Figure 4-8

LINE	SIGNAL NAME	SIGNAL SOURCE	SENSE AMP A1	INHIBIT GATE A2	SENSE AMP A3	INHIBIT GATE A4	DECODER GATE A5	DECODER GATE A6	READ/WRITE GEN A7	READ/WRITE GEN A8	HORIZONTAL DAC A9	VERTICAL DAC A10	MEMORY VOLTAGE REG. A11	20 MHz CLOCK A12	MEMORY TIMER A13	MEMORY LOGIC A14	P2	P3	J15	J16	REMARKS
1	+12V	P3(5)										13, P	12					5			
2	-12V	P3(12)	A(4)							A(4,D)	A(4,D)	10, L	5					12			
3	+5V	P3(7, 14)	A(2)							A(6, F)	A(6, F)	15, S			10, L	14		7, 14			
4	-7.5V	P3(6, 13)	A(7)											1(3, 6)				6, 13			
5	GRD	P3(1, 8)	A(1, A)												15, S	15, S		1, 8			
6	-19.5V	A11(6, F)				A(11)				A(5, E)	A(5, E)	6, F						4			To API Line 5 & LD & FF Line 10
7	-19.5V	A11(14, R)	A(9)									14, R						11			To API Line 6 & P.S. Line 11
8	+1.6V	P3(10)										7, H						10			From Power Supply Line 34
9	+35V	P3(2)										3, C						2			From Power Supply Line 35
10	$\overline{\text{AR0}}$	P2(3)														J		3		$\overline{\text{h}}$	From MFL Line 193
11	$\overline{\text{AR1}}$	P2(4)														H		4		$\overline{\text{J}}$	From MFL Line 194
12	$\overline{\text{AR2}}$	P2(5)														4		5			From MFL Line 195
13	$\overline{\text{AR3}}$	P2(6)														3		6			From MFL Line 196
14	$\overline{\text{AR4}}$	P2(7)								B(H)								7			From MFL Line 197
15	$\overline{\text{AR5}}$	P2(8)								B(D)								8			From MFL Line 198
16	$\overline{\text{AR6}}$	P2(9)								A(Z)								9			From MFL Line 199
17	$\overline{\text{AR7}}$	P2(10)								A(W)								10			From MFL Line 200
18	$\overline{\text{AR8}}$	P2(11)								A(T)								11			From MFL Line 201
19	$\overline{\text{AR9}}$	P2(12)								A(P)								12			From MFL Line 202
20	20 MHZ CLOCK	A12(3)												2	1						Through P34 MFL Line 19
21	CAL FULL	P2(21)								A(8, J)	A(8, J)										From Scale Calsn S5
22	CAL ZERO	P2(46)									A(9, K)										From Scale Calsn S5
23	VERTICAL DAC	A10A(B)									A(B)										Through P33 To API Line 19
24	SET DISPLAY	A10A(10, L								A(10, L)	A(10, L)										
25	SET VERT.	P2(41)									A(17, U)							41			From LPI Line 121
26	SET VERT	P2(15)									A(16, T)							15	E		From Ext Source J15(E)
27	CAR0	A14(8)								B(W)						8					
28	CAR1	A14(7)								B(T)						7					
29	CAR2	A14(6)								B(P)						6					
30	CAR3	A14(5)								B(L)						5					

Table 4-2. Wiring Lists (Cont'd)

PART C 5480A/B (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	SENSE AMP A1	INHIBIT GATE A2	SENSE AMP A3	INHIBIT GATE A4	READ/WRITE GEN A7	READ/WRITE GEN A8	HORIZONTAL DAC A9	VERTICAL DAC A10	MEMORY VOLTAGE REG. A11	MEMORY TIMING A12	MEMORY LOGIC A13	P1	P2	J2S	J16	J16	REMARKS
31	CLOCK 1	A14(1)						B(1, A					1						
32	CLOCK 2	A14(2)						B(21, Y)					2						
33	$\overline{\text{READ}}$	P2(18)										11			18		18			From LPI Line 127
34	$\overline{\text{READ}}$	P2(42)										12			42				X	From Ext. Source J16(X)
35	$\overline{\text{WRITE}}$	P2(19)										8			19		19			From LPI Line 126
36	$\overline{\text{WRITE}}$	P2(44)										9			44				Y	From Ext Source J16(Y)
37	$\overline{\text{CYCLE}}$	P2(20)										6			20		20			From LPI Line 119
38	$\overline{\text{CYCLE}}$	P2(46)										7			46				C	From Ext. Source J16(C)
39	$\overline{\text{SET MEB}}$	P2(40)							A(8)						40		4			From LPI Line 118
40	$\overline{\text{SET HORIZ}}$	P2(42)											B		42			V	V	From Ext. Source J16(V).
41	$\overline{\text{SET HORIZ}}$	P2(17)											A		17		17			From LPI Line 122
42	HORIZ DAL	A9A(3)						A(B)												Thru P35 to J9 and J36(22)
43	$\overline{\text{STROBE TIME}}$	A13(3)	A(13)		A(13)							3								
44	$\overline{\text{READ TIME}}$	A13(2)					A(5)	A(5)				2								
45	$\overline{\text{INHIBIT TIME}}$	A13(4)		A(3)		A(3)						4								
46	$\overline{\text{WRITE TIME}}$	A13(5)					A(3)	A(3)				5								
47	MM1	A13(14)								11		14								
48	MM2	A13(13)								12		13								
49	$\overline{\text{SW HST}}$	P2 (13)											13		13		13			From LPI Line 209
50	MB88L	P2(36)											P		36		45			From LPI Line 201
51	MOD HOLD	P2(16)											D		16			W		From Ext Source J16(W)
52	AC0	P1(1)			A(5)									1						From MFL Line 87
53	AC1	P1(2)			A(6)									2						From MFL Line 98
54	AC2	P1(3)			A(11)									3						From MFL Line 99
55	AC3	P1(4)			A(12)									4						From MFL Line 100
56	AC4	P1(5)			A(15)									5						From MFL Line 101
57	AC5	P1(6)			A(16)									6						From MFL Line 102
58	AC6	P1(7)			A(17)									7						From MFL Line 103
59	AC7	P1(8)			A(18)									8						From MFL Line 104
60	AC8	P1(9)			A(19)									9						From MFL Line 105

Table 4-2. Wiring Lists (Cont'd)

PART C 5480A/B (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	SENSE AMP A1	INHIBIT GATE A3	SENSE AMP A5	INHIBIT GATE A6	MEMORY VOLTAGE REG. A11	P1	P2	REMARKS
61	AC9	P1(10)			A(20)			10		From MFL Line 106
62	AC10	P1(11)			A(21)			11		From MFL Line 107
63	AC11	P1(12)			A(23)			12		From MFL Line 108
64	AC12	P1(13)	A(5)					13		From MFL Line 109
65	AC13	P1(14)	A(6)					14		From MFL Line 110
66	AC14	P1(15)	A(11)					15		From MFL Line 111
67	AC15	P1(16)	A(12)					16		From MFL Line 112
68	AC16	P1(17)	A(15)					17		From MFL Line 113
69	AC17	P1(18)	A(16)					18		From MFL Line 114
70	AC18	P1(19)	A(17)					19		From MFL Line 115
71	AC19	P1(20)	A(18)					20		From MFL Line 116
72	AC20	P1(21)	A(19)					21		From MFL Line 117
73	AC21	P1(22)	A(20)					22		From MFL Line 118
74	AC22	P1(23)	A(21)					23		From MFL Line 119
75	AC23	P1(24)	A(22)					24		From MFL Line 120
76	POWER SENSE	P3(3)					3		3	From A5T1
77	POWER SENSE	P3(9)					B		9	From A5T1
78	$\overline{\text{SA0}}$	P1(26)			A(5)			26		To MFL Line 48
79	$\overline{\text{SA1}}$	P1(27)			A(6)			27		To MFL Line 49
80	$\overline{\text{SA2}}$	P1(28)			A(11)			28		To MFL Line 50
81	$\overline{\text{SA3}}$	P1(29)			A(12)			29		To MFL Line 51
82	$\overline{\text{SA4}}$	P1(30)			A(15)			30		To MFL Line 52
83	$\overline{\text{SA5}}$	P1(31)			A(16)			31		To MFL Line 53
84	$\overline{\text{SA6}}$	P1(32)			A(17)			32		To MFL Line 54
85	$\overline{\text{SA7}}$	P1(33)			A(18)			33		To MFL Line 55
86	$\overline{\text{SA8}}$	P1(34)			A(19)			34		To MFL Line 56
87	$\overline{\text{SA9}}$	P1(35)			A(20)			35		To MFL Line 57
88	$\overline{\text{SA10}}$	P1(36)			A(21)			36		To MFL Line 58
89	$\overline{\text{SA11}}$	P1(37)			A(22)			37		To MFL Line 59
90	$\overline{\text{SA12}}$	P1(38)	A(5)					38		To MFL Line 60

Table 4-2. Wiring Lists (Cont'd)

PART C 5480A/B (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	SENSE AMP A1	DECODER GATE A5	DECODER GATE A6	READ/WRITE GEN A7	READ/WRITE GEN A8	HORIZONTAL DAC A9	P1	REMARKS
91	$\overline{SA13}$	P1(39)	A(6)						39	To MFL Line 61
92	$\overline{SA14}$	P1(40)	A(11)						40	To MFL Line 62
93	$\overline{SA15}$	P1(41)	A(12)						41	To MFL Line 63
94	$\overline{SA16}$	P1(42)	A(15)						42	To MFL Line 64
95	$\overline{SA17}$	P1(43)	A(16)						43	To MFL Line 65
96	$\overline{SA18}$	P1(44)	A(17)						44	To MFL Line 66
97	$\overline{SA19}$	P1(45)	A(18)						45	To MFL Line 67
98	$\overline{SA20}$	P1(46)	A(19)						46	To MFL Line 68
99	$\overline{SA21}$	P1(47)	A(20)						47	To MFL Line 69
100	$\overline{SA22}$	P1(48)	A(21)						48	To MFL Line 70
101	$\overline{SA23}$	P1(49)	A(22)						49	To MFL Line 71
102	MA0	A9B(19)			A(5)		B(19)			
103	$\overline{MA0}$	A9B(18)			A(6)		B(18)			
104	MA1	A9B(16)			A(7)		B(16)			
105	$\overline{MA1}$	A9B(15)			A(3)		B(15)			
106	MA2	A9B(13)			A(9)		B(13)			
107	$\overline{MA2}$	A9B(12)			A(10)		B(12)			
108	MA3	A9B(10)				A(21)	B(10)			
109	$\overline{MA3}$	A9B(9)				A(19)	B(9)			
110	MA4	A9B(7)				A(20)	B(7)			
111	$\overline{MA4}$	A9B(6)				A(22)	B(6)			
112	MA5	A9B(4)			A(5)		B(4)			
113	$\overline{MA5}$	A9B(3)			A(8)		B(3)			
114	MA6	A9A(22)			A(7)		A(22)			
115	$\overline{MA6}$	A9A(21)			A(3)		A(21)			
116	MA7	A9A(19)			A(9)		A(19)			
117	$\overline{MA7}$	A9A(18)			A(10)		A(18)			
118	MA8	A9A(16)				A(20)	A(16)			
119	$\overline{MA8}$	A9A(15)				A(22)	A(15)			
120	MA9	A9A(13)				A(21)	A(13)			

Table 4-2. Wiring Lists (Cont'd)

PART C 5480A/B (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	READ/WRITE GEN A8	HORIZONTAL DAC A9	VERTICAL DAC A10	MEMORY LOGIC A14	P2	J15	J16	J20	J21	REMARKS
121	$\overline{MA5}$	A9A(12)	A(10)	A(12)								
122	$\overline{SBAR1}$	P2(30)				10	30		E		22	From EXT J16(E) To API Line 37
123	$\overline{SAAR1}$	P2(31)				9	31		F		43	From EXT J16(f) To API Line 36
124	$\overline{SBAR0}$	P2(29)				11	29		J		42	From EXT J16(d) To API Line 38
125	$\overline{SAAR0}$	P2(28)				12	28		E		21	From EXT J16(E) To API Line 39
126	SETDAR	P2(30)				C	39	U	U			From EXT Source J16(U)
127	CLEAR HORIZ HOLD	A14(R)		B(8)		R						
128	$\overline{SAAR2}$	P2(32)				F	32		U			From EXT Source J16(G)
129	$\overline{SAAR3}$	P2(33)				E	33		V			From EXT Source
130	$\overline{MBAP0}$	P2(35)				M	35			15		From API Line 65
131	$\overline{MBAP0}$	P2(34)				N	34			16		From API Line 66
132	$\overline{MBAP1}$	P2(36)				K	36			41		From API Line 64
133	$\overline{MAAR1}$	P2(37)				L	37			40		From API Line 63
134	RESET HORIZ	P2(22)		A (9, K)								From LPI Line 214
	5480A: MAKE THE CHANGES LISTED BELOW											
	(ALL SERIALS)											
122	CAL ZERO	P2(46)		A (9, K)	A (9, K)							From Scale CALSW 85
134	DELETE THIS LINE											
	SERIALS 852- AND BELOW											
	YOUR INSTRUMENT HAS ADDITIONAL SIGNAL LINES											
	INDICATED BY SHADING IN TABLE											

Table 4-2. Wiring Lists (Cont'd)

PART D 5480A/B A3 MAIN FRAME LOGIC SECTION Wiring Diagram: Figure 4-9

LINE	SIGNAL NAME	SIGNAL SOURCE	PRIORITY DETECTOR A1	ACCUMULATOR CONTROL A2	BCD ADDER ACCUMULATOR A3	ACCUMULATOR A4	ACCUMULATOR A5	ACCUMULATOR A6	ACCUMULATOR A7	ACCUMULATOR A8	ADDRESS REGISTER A9	ADDRESS REGISTER A10	ADDRESS REGISTER A11	ADDRESS REGISTER CONTROL A12	J1	J2	J15	J16	J17,18	J25	J26	A4A1A	REMARKS
1	+5V	A5A1(6)	1,A			19,W	19,W	19,W															
2	GRD	Chassis	22,Z												30, 50								
3	ENABLE COUNT	J22(1)		2																1			From LPI Line 125
4	ENABLE COUNT	J16(6)		B														C			35		From Ext Source
5	ENSHIFT LEFT	J22(2)		3																2			From LPI Line 124
6	ENSHIFT LEFT	J16(A)		C														A					From Ext Source
7	ENSHIFT RIGHT	J22(3)		4																3			From LPI Line 122
8	ENSHIFT RIGHT	J16(B)		D														B			36		From Ext Source
9	ENSHIFT IN	J22(4)		5																4			Not Used
10	ENSHIFT IN	J16(D)		E													D	D					From Ext Source
11	ENCLOSED LOOP	J22(6)		7																6			From LPI Line 108
12	CLEAR 1	J22(17)		15													F	F		7			From LPI Line 120
13	CLEAR 1	A4A1A		S																		15	
14	SHIFT 1	J22(8)		F																8			From LPI Line 191
15	SHIFT 1	J16(E)		R													E	H			32		From Ext Source
16	COUNTUP ENABLE	J22(10)		20																10			From LPI Line 211
17	ENCOUNT SOURCE	J16(P)		X													P						From Ext Source J16(P)
18	ENABLE 20MHZ	J22(12)		U																13			From LPI Line 190
19	20MHZ Clock	J34		T						2										24			From PCB Line 20 to LPI Line 27
20	COUNT UP A	J22(9)		18																9			From LPI Line 109
21	ENABLE COUNT UP A	J26(33) J16(J)		V														J			33		From Ext or API Line 85
22	COUNT DN ENABLE	J22(13)		21																12			From LPI Line 210
23	ENCOUNT SOURCE	J16(N)		Y													N						From Ext Source J16(N)
24	COUNT DN A	J22(11)		19																11			Not Used
25	ENABLE COUNT DN	J16(K)		W														K			34		From Ext Source
26	ENABLE OPEN LOOP	J22(5)		6																5			Not Used
27	ENABLE OPEN LOOP	J16(E)		F														E		4			From Ext Source
28	COUNT	A2A2(9)																					
29	SHIFT LEFT	A2A2(15)																					
30	SHIFT RIGHT	A2A2(10)																					

Table 4-2. Wiring Lists (Cont'd)

PART D 5480A/B (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	PRIORITY DETECTOR A1	ACCUMULATOR CONTROL A2	BCD ADDER ACCUMULATOR A3	ACCUMULATOR A4	ACCUMULATOR A5	ACCUMULATOR A6	ACCUMULATOR A7	ACCUMULATOR A8	ADDRESS REGISTER A9	ADDRESS REGISTER A10	ADDRESS REGISTER A11	ADDRESS REGISTER CONTROL A12	J1	J2	J15	J16	J17,18	J25	J26	A4A1A	REMARKS
31	SHIFT IN	A3A2(11)		11																			
32	OPEN LOOP	A3A3(J)		J	8					8													To A3 & A8 Only
33	CLOSED LOOP	A3A3(8)		8	J					J													To A3 & A8 Only
34	CLEAR 2	A3A2(14)		14																			
35	SHIFT 2	A3A2(13)		13																			
36	COUNT UP B	A3A3(16)		16	T																		
37	COUNT DN B	A3A3(17)		17	U																		
38	COUNT UP C	A3A3(16)			16	T																	
39	COUNT DN C	A3A3(17)			17	U																	
40	COUNT UP D	A3A4(16)				16	T																
41	COUNT DN D	A3A4(17)				17	U																
42	COUNT UP E	A3A5(16)					16	T															
43	COUNT DN E	A3A5(17)					17	U															
44	COUNT UP F	A3A6(16)						16	T														
45	COUNT DN F	A3A6(17)						17	U														
46	COUNT UP G	A3A7(16)							16	T													
47	COUNT DN G	A3A7(17)							17	U													
48	$\overline{BA0}$	J1(26)		2										26									From Memory Line 78
49	$\overline{BA1}$	J1(27)		B										27									From Memory Line 79
50	$\overline{BA2}$	J1(28)		3										28									From Memory Line 80
51	$\overline{BA3}$	J1(29)		C										29									From Memory Line 81
52	$\overline{BA4}$	J1(30)		2										30									From Memory Line 82
53	$\overline{BA5}$	J1 (31)		B										31									From Memory Line 83
54	$\overline{BA6}$	J1(32)		3										32									From Memory Line 84
55	$\overline{BA7}$	J1(33)		C										33									From Memory Line 85
56	$\overline{BA8}$	J1(34)				2								34									From Memory Line 86
57	$\overline{BA9}$	J1(35)				B								35									From Memory Line 87
58	$\overline{BA10}$	J1(36)				3								36									From Memory Line 88
59	$\overline{BA11}$	J1(37)				C								37									From Memory Line 89
60	$\overline{BA12}$	J1(38)					2							38									From Memdry Line 90

Table 4-2. Wiring Lists (Cont'd)

PART D 5480A/B (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	PRESET DETECTOR A1	ACCUMULATOR CONTROL A2	HIGH-SPEED ACCUMULATOR A3	ACCUMULATOR A4	ACCUMULATOR A5	ACCUMULATOR A6	ACCUMULATOR A7	ACCUMULATOR A8	ADDRESS REGISTER A9	ADDRESS REGISTER A10	ADDRESS REGISTER A11	ADDRESS REGISTER CONTROL A12	J1	J2	J15	J16	J17, 18	J23	J30	A4A1A	REMARKS
61	$\overline{SA13}$	J1(39)					B								39								From Memory Line 91
62	$\overline{SA14}$	J1(40)					3								40								From Memory Line 92
63	$\overline{SA15}$	J1(41)					C								41								From Memory Line 93
64	$\overline{SA16}$	J1(42)						2							42								From Memory Line 94
65	$\overline{SA17}$	J1(43)						B							43								From Memory Line 95
66	$\overline{SA18}$	J1(44)						3							44								From Memory Line 96
67	$\overline{SA19}$	J1(45)						C							45								From Memory Line 97
68	$\overline{SA20}$	J1(46)						2							46								From Memory Line 98
69	$\overline{SA21}$	J1(47)						B							47								From Memory Line 99
70	$\overline{SA22}$	J1(48)						3							48								From Memory Line 100
71	$\overline{SA23}$	J1(49)						C							49								From Memory Line 101
72	$\overline{EXTAC0}$	J17 J18 (A)			7														A				From External Source
73	$\overline{EXTAC1}$	J17 J18 (E)			6														E				
74	$\overline{EXTAC2}$	J17 J18 (K)			5														K				
75	$\overline{EXTAC3}$	J17 J18 (P)			4														P				
76	$\overline{EXTAC4}$	J17 J18 (U)				7													U				
77	$\overline{EXTAC5}$	J17 J18 (Y)				6													Y				
78	$\overline{EXTAC6}$	J17 J18 (d)				5													d				
79	$\overline{EXTAC7}$	J17 J18 (h)				4													h				
80	$\overline{EXTAC8}$	J17 J18 (k)					7												k				
81	$\overline{EXTAC9}$	J17 J18 (l)					6												l				
82	$\overline{EXTAC10}$	J17 J18 (n)					5												n				
83	$\overline{EXTAC11}$	J17 J18 (BB)					4												BB				
84	$\overline{EXTAC12}$	J17 J18 (C)						7											C				
85	$\overline{EXTAC13}$	J17 J18 (H)						6											H				
86	$\overline{EXTAC14}$	J17 J18 (M)						5											M				
87	$\overline{EXTAC15}$	J17 J18 (S)						4											S				
88	$\overline{EXTAC16}$	J17 J18 (W)							7										W				
89	$\overline{EXTAC17}$	J17 J18 (Z)							6										Z				
90	$\overline{EXTAC18}$	J17 J18 (g)							5										g				

Model 5480A/B

Table 4-2. Wiring Lists (Cont'd)

PART D 5480A/B (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	PRESET DETECTOR A1	ACCUMULATOR CONTROL A2	HIGH-SPEED ACCUMULATOR A3	ACCUMULATOR A4	ACCUMULATOR A5	ACCUMULATOR A6	ACCUMULATOR A7	ACCUMULATOR A8	ADDRESS REGISTER A9	ADDRESS REGISTER A10	ADDRESS REGISTER A11	ADDRESS REGISTER CONTROL A12	J1	J2	J15	J16	J17, 18	J23	J30	A4A1A	REMARKS
91	$\overline{EXTAC19}$	J17 J18 (E)								4									E				From External Source
92	$\overline{EXTAC20}$	J17 J18 (F)							7										F				
93	$\overline{EXTAC21}$	J17 J18 (V)							6										V				
94	$\overline{EXTAC22}$	J17 J18 (E)							5				1						E				
95	$\overline{EXTAC23}$	J17 J18 (DD)							4										DD				From External Source
96	SHIFT CONT AC14	A3A7(8)						8												22			To LPI Line 196
97	AC0	A3A3(20)		20						W				1					B				To Ext Source & Mem Line 52
98	AC1	A3A3(X)		X						V				2					F				To Mem Line 53
99	AC2	A3A3(21)	21	21							6			3					L				To Mem Line 54
100	AC3	A3A3(Y)	20	Y						7	7			4					R				To Mem Line 55
101	AC4	A3A4(20)	19		20						F			5					V				To Mem Line 56
102	AC5	A3A4(X)	18		X						H			6					Z				To Mem Line 57
103	AC6	A3A4(21)	17		21							6		7					d				To Mem Line 58
104	AC7	A3A4(Y)	16		Y							7		8					j				To Mem Line 59
105	AC8	A3A5(20)	15			20						F		9					p				To Mem Line 60
106	AC9	A3A5(X)	14			X						H		10					u				To Mem Line 61
107	AC10	A3A5(21)	13			21								11					y				To Mem Line 62
108	AC11	A3A5(Y)	12			Y								12					CC				To Mem Line 63
109	AC12	A3A6(20)	Y				20							13					D				To Mem Line 64
110	AC13	A3A6(X)	X				X							14					J				To Mem Line 65
111	AC14	A3A6(21)	W				21							15					N				To Mem Line 66
112	AC15	A3A6(Y)	V				Y							16					T				To Mem Line 67
113	A616	A3A7(20)	U					20						17					X				To Mem Line 68
114	AC17	A3A7(X)	T					X						18					b				To Mem Line 69
115	AC18	A3A7(21)	S					21						19					f				To Mem Line 70
116	AC19	A3A7(Y)	R					Y						20					m				To Mem Line 71
117	AC20	A3A8(20)	P						20					21					s				To Mem Line 72
118	AC21	A3A8(X)	N						X					22					w				To Mem Line 73
119	AC22	A3A8(21)	M						21					23					AA				To Mem Line 74
120	AC23	A3A8(Y)	L						Y					24					EE				To Ext Source & Mem Line 75

Table 4-2. Wiring Lists (Cont'd)

PART D 5480A/B (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	PRESET DETECTOR A1	ACCUMULATOR CONTROL A2	HIGH-SPEED ACCUMULATOR A3	ACCUMULATOR A4	ACCUMULATOR A5	ACCUMULATOR A6	ACCUMULATOR A7	ACCUMULATOR A8	ADDRESS REGISTER A9	ADDRESS REGISTER A10	ADDRESS REGISTER A11	ADDRESS REGISTER CONTROL A12	J1	J2	J15	J16	J17, 18	J22	J26	A4A1A	REMARKS
121	$\overline{AC0}$	A3A3(V)			V					18													
122	$\overline{AC3}$	A2A3(15)			15	S																	
123	$\overline{AC4}$	A3A4(V)			18	V																	
124	$\overline{AC7}$	A3A4(15)				15	S																
125	$\overline{AC8}$	A3A5(V)				18	V																
126	$\overline{AC11}$	A3A5(15)					15	S															
127	$\overline{AC12}$	A3A6(V)					18	V															
128	$\overline{AC15}$	A3A6(15)						15	S														
129	$\overline{AC16}$	A3A7(V)						18	V														
130	$\overline{AC19}$	A3A7(15)							15	S													
131	$\overline{AC20}$	A3A8(V)							18	V													
132	$\overline{AC23}$	A3A8(15)			S					15													
133	PRESET TOTAL 10^0	J22(15)	11																15				From LPI Line 74
134	PRESET TOTAL 10^1	J22(16)	10																16				From LPI Line 75
135	PRESET TOTAL 10^2	J22(17)	9																17				From LPI Line 76
136	PRESET TOTAL 10^3	J22(18)	8																18				From LPI Line 77
137	PRESET TOTAL 10^4	J22(19)	7																19				From LPI Line 78
138	PRESET TOTAL 10^5	J22(20)	6																20				From LPI Line 79
139	PRESET TOTAL	A3A1(F)	F																21				From LPI Line 149
140	$\overline{PSD2}$	A3A1(K)	K																46				To LPI Line 138
141	$\overline{PSD1}$	A3A1(J)	J																45				To LPI Line 198
142	ENABLE COUNT PAR	J16(M) J26(9)										E				M				9			From Ext Source
143	ENABLE COUNT PAR	J22(31)										5							31				From LPI Line 108
144	ENSHIFT RT PAR	J16(L) J26(11)										F				L				11			From Ext Source
145	ENSHIFT RT PAR	J22(29)										6							29				Not Used
146	ENSHIFT IN PAR	J15(Y) J26(10)										E			G					10			From Ext Source J16(L)
147	ENSHIFT IN PAR	J22(30)										7							30				Not Used
148	ENABLE DAR TO PAR	J22(28)										9							28				Not Used
149	ENABLE DAR TO PAR	J16(S)										10				S							From Ext Source
150	ENABLE PAR TO HOLD	J22(41)										16							41				From LPI Line 197

Table 4-2. Wiring Lists (Cont'd)

PART D 5480A/B (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	PRESET DETECTOR A1	ACCUMULATOR CONTROL A2	HIGH-SPEED ACCUMULATOR A3	ACCUMULATOR A4	ACCUMULATOR A5	ACCUMULATOR A6	ACCUMULATOR A7	ACCUMULATOR A8	ADDRESS REGISTER A9	ADDRESS REGISTER A10	ADDRESS REGISTER A11	ADDRESS REGISTER CONTROL A12	J1	J2	J15	J16	J17, 18	J22	J26	A4A1A	REMARKS
151	ENABLE DAR TO HOLD	J22(40)												18						40			From LPI Line 204
152	ENABLE PAR TO HOLD	J22(42)												20						42			Not Used
153	CLEAR PAR A	J22(36)												11						38			From LPI Line 109
154	CLEAR DAR A	J22(38)												13						26			From LPI Line 207
155	SHIFT PAR A	J26(6)												R							6		Not Used
156	SHIFT PAR A	J16(N)												14				W					From Ext Source
157	SET PARA	J22(39)												15						39			From LPI Line 112
158	SET DAR B	J22(48)												4						48			From LPI Line 203
159	COUNT PAR	A3A12(M)									11	11	11	M									
160	SHIFT RT PAR	A3A12(K)									9	9	9	K									
161	SHIFT IN PAR	A3A12(J)									8	8	8	J									
162	DAR TO DAR	A3A12(L)									10	10	10	L									
163	PAR TO HOLD	A3A12(X)									20	20	20	X									
164	DAR TO HOLD	A3A12(W)									19	19	19	W									
165	AC TO HOLD	A3A12(Y)									21	21	21	Y									
166	CLEAR PAR B	A3A12(U)									U	U	U	U									
167	CLEAR DAR B	A3A12(V)										V	V	V									
168	SHIFT PAR B	A3A12(N)									12	12	12	N									
169	SET PAR B	A3A12(17)									17	17	17	17									
170	SET DAR C	A3A12(18)									18	18	18										
[illegible]	[illegible]	[illegible]									M						M				5		From Ext Source J16(M)
[illegible]	[illegible]	[illegible]									N						S				4		From Ext Source J16(S)
[illegible]	[illegible]	[illegible]										R					W				5		From Ext Source J16(W)
[illegible]	[illegible]	[illegible]										C					E				3		From Ext Source J16(E)
[illegible]	[illegible]	[illegible]										D					D				1		From Ext Source J16(D)
[illegible]	[illegible]	[illegible]										E					E				30		From Ext Source J16(E)
[illegible]	[illegible]	[illegible]											B				F				29		From Ext Source J16(F)
[illegible]	[illegible]	[illegible]											C				V				28		From Ext Source J16(V)
[illegible]	[illegible]	[illegible]											D				E				27		From Ext Source J16(E)
[illegible]	[illegible]	[illegible]											E				ED				26		From Ext Source J16(ED)

Table 4-2. Wiring Lists (Cont'd)

PART D 5480A/B (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	PRESET DETECTOR A1	ACCUMULATOR CONTROL A2	HIGH-SPEED ACCUMULATOR A3	ACCUMULATOR A4	ACCUMULATOR A5	ACCUMULATOR A6	ACCUMULATOR A7	ACCUMULATOR A8	ADDRESS REGISTER A9	ADDRESS REGISTER A10	ADDRESS REGISTER A11	ADDRESS REGISTER CONTROL A12	J1	J2	J15	J16	J17, 18	J22	J26	A4A1A	REMARKS
181	ADVANCE DAR+1	J22(27)									P									27			From LPI Line 165
182	SHIFT RT PAR A	A3A10(R)									14	R											
183	ADVANCE PAR+2	J22(33)									6									33			Not Used
184	ADVANCE PAR+4	J22(34)									7									34			Not Used
185	ADVANCE PAR+1	J22(32)									4									32			From LPI Line 205
186	ADVANCE PART+1	J16(P) J26(7)									D							P			7		From Ext Source
187	ADVANCE PAR-1	J22(35)									5									35			From LPI Line 206
188	ADVANCE PAR-1	J26(8)									E							R			8		From Ext Source
189	GATED UP 20MHZ PAR	J26(17)									3									36	17		To LPI Line 211 From API Line 33
190	$\overline{SW\ HBT}$	J22(47)									B									47			From LPI Line 209
191	GATED DN 20MHZ PAR	J26(42)									C									37	42		To LPI Line 210 From API Line 32
192	ENABLE PAR TO HOLD	J15(AA) J16(AA)												T			AA	AA					From Ext (See Line 150)
193	$\overline{AR0}$	A3A9(Y)									Y					3		$\overline{h}$			14		To Mem Line 10 To API Line 41
194	$\overline{AR1}$	A3A9(X)									X					4		$\overline{J}$			30		To Mem Line 11 To API Line 42
195	$\overline{AR2}$	A3A10(2)	B									2				5							To Memory Line 12
196	$\overline{AR3}$	A3A10(3)	C									3				6							To Memory Line 13
197	$\overline{AR4}$	A3A10(4)	D									4				7							To Memory Line 14
198	$\overline{AR5}$	A3A10(5)	E									5				8							To Memory Line 15
199	$\overline{AR6}$	A3A11(2)	2										2			9							To Memory Line 16
200	$\overline{AR7}$	A3A11(3)	3										3			10							To Memory Line 17
201	$\overline{AR8}$	A3A11(4)	4										4			11							To Memory Line 18
202	$\overline{AR9}$	A3A11(5)	5										5			12		Z					To Memory Line 19 & Ext Source
203	COUNT UP DAR A	A3A9(13)									13	P											
204	COUNT UP DAR B	A3A10(13)										13	P										
205	$\overline{PAR0}$	A3A9(K)									K							$\overline{Z}$			13		To Ext Source
206	COUNT UP $\overline{PAR\ A}$	A3A9(15)									15	S											
207	$\overline{COUNT\ DN}$ $\overline{PAR\ A}$	A3A9(16)									16	T											
208	SHIFT RT PAR B	A3A11(R)										14	R										
209	SHIFT RT PAR C	J16(b)											14					$\overline{b}$			12		From Ext Source
210	COUNT UP PAR B	A3A10(15)										15	S										
211	COUNT DN PAR B	A3A10(16)										16	T										
212	COUNT UP PAR C	A3A11(15)											15							43			To LPI Line 10
213	COUNT DN PAR C	A3A11(16)											16							44			To LPI Line 199
214	CLEAR DN PAR A	J15(T) J16(T)												12			T	T					From Ext See Line 153
215	CLAC 19 SETAC 18	J22(14)							19											14			From LPI Line 192
216	ADVANCE PAR+4	J16(W)									H							$\overline{W}$					From Ext Source
217	ADVANCE PAR+2	J16([illegible])									F							$\overline{X}$					From Ext Source

5480A: Serials Prefixed 8[illegible]2- and below your instrument has additional signals indicated by shaded areas in table

Table 4-2. Wiring Lists (Cont'd)

LINE	SIGNAL NAME	SIGNAL SOURCE	LIGHT DRIVER AND 48 V REG. A1	LOW VOLTAGE REG. A1	HIGH VOLTAGE REG. A5	J3	J21	J28	J23	J24	J16	REMARKS
			A4 LIGHT DRIVER AND FLIP-FLOP			A5 POWER SUPPLY						
	PART E 5480A/B A4 SWITCHING LOGIC SECTION (LIGHT DRIVER AND FLIP-FLOP) A5 POWER SUPPLY SECTION Wiring Diagram: Figure 4-10											
1	CLEAR ACCUM.	A3A2(5)	A(15) B(9)								EE	Also From Clear Display Push Buttons
2	+12V	A5A1(2)		2		5	4	4				To All Sections
3	-12V	A5A1(14)		4		12	12	12				To All Sections
4	+5V	A5A1(8)	B(22)	8		7, 14	2	2, 10				To Main Frame Logic Line 1
5	-7.5V	A5A1(15)		15		6, 13						To Memory Line 4
6	+50V	A5A2(5)			5							To Display Section Line 9
7	-50V	A5A2(14)			14							To Display Section Line 7
8	+200V	A5A2(6)			6							To Display Section Line 8
9	GRD	Chassis	B(1)	1	1	1, 8	1, 9 8, 16	1, 9 8, 16				To All Sections
10	+19.5	J3(10)	A(2)			10		6				From Memory Voltage Reg.
11	-19.5	J3(11)	A(1)			11		14				From Memory Voltage Reg.
12	RESET LAMP DR	A4A1A(3)	A(3)									To Reset Lamp DS2
13	STOP PBM	A4S2(2)	A(10) B(4)								BB	Tied to Line 27, Set L Stop
14	DISPLAY PBM	A4S4(2)	A(14)								CC	
15	STOP LAMP DR.	A4A1B(13)	B(13)									To Stop Lamp A4DS2
16	DISPLAY LAMP DR.	A4A1B(18)	B18)									To Display Lamp A4DS4
17	RECORD LAMP DR.	A4A1B(20)	B(20)									To Record Lamp A4DS5
18	RECORD PBM	A4S5(2)	A(16)					47			DD	To LPI Line 200
19	L DISPLAY	A4A1B(19)	B(19)					38				To LPI Line 139
20	L STOP	A4A1B(14)	B(14)					40				To LPI Line 153
21	DISPLAY PBH	A4A1A(21)	A(21)					33				To LPI Line 151
22	RECORD PBH	A4A1A(22)	A(22)					34				To LPI Line 152
23	SET-L DISPLAY	J23(28)	B(8)					28				From LPI Line 157
24	L RECORD	A4A1B(21)	B(21)					39				To LPI Line 145 & API Line 93
25	SET-L RECORD	J23(29)	B(10)					29				From LPI Line 158
26	STOP PBH	A4A1A(19)	A(19)					35				To LPI Line 146
27	SET-L STOP	J23(30)	B(4)					30				From LPI (156 See Line 13
28	START PBH	A4A1A(18)	A(18)					31				To LPI Line 143
29	SET-L START	J23(26)	B(2)					26				From LPI Line 154
30	L START	A4A1B(15)	B(15)					36				To LPI Line 84

Table 4-2. Wiring Lists (Cont'd)

LINE	SIGNAL NAME	SIGNAL SOURCE	LIGHT DRIVER AND 48 V REG. A1	LOW VOLTAGE REG. A1	HIGH VOLTAGE REG. A5	J3	J21	J28	J23	J24	J16	REMARKS
			A4 LIGHT DRIVER AND FLIP-FLOP			A5 POWER SUPPLY						
	PART E 5480A/B (CONT'D)											
31	START LAMP DR.	A4A1B(12)	B(12)									To Start Lamp A4DS1
32	START PBM	A4S1(3)	A(8)					41		E		From Ext Source
33	LINE SYNC	AST1					3					To LPI Line 212
34	+16V					10						To Memory Line 6
35	+35V					2						To Memory Line 9
36	POWER SENSE	AST1				3						To Memory Line 76
37	POWER SENSE	AST1				9						To Memory Line 77
38	CLEAR 1	A4A1A(15)	A(15)									To Memory Line 13

Table 4-2. Wiring Lists (Cont'd)

PART F — 5480A/B INPUT/OUTPUT CONNECTORS

Wiring Diagram: none

1. MATING CONNECTORS

Reference Designator	Instrument Connector Type (HP Part No.)	Mating Connector Type (HP Part No.)
J4-11, 13, 14, 19, 29-35	BNC Female	Standard BNC male
J15-18	Body: Winchester MRAC 50S6 (1251-1921) Pin, female, 2-wire: Winchester 100-1016S (1251-1911) Pin, female, 1-wire: Winchester 100-1022S (1251-1909) Mtg. screws (set): Winchester J602 (1251-1911)	Body: Winchester MRAC 50P8 (1251-1918) Pin, male: Winchester 100-1022P (1251-1908) Hood: Winchester 45-50H33/ES69 (1251-1922) Shell: Winchester XMRE 50-1000 (1251-1924) Mating Cable: (05495-60038)
J20	Connector: Power, 3-pin male (1251-0148)	Power cord (8120-0078)
J36	Connector: female, ribbon, 14-contact, Amphenol or Cinch type 57-40140 (1251-0143)	Connector: male, ribbon, 14-contact, Amphenol or Cinch type 57-30140 (1251-0142)
A1J1	Connector: banana, female (1251-0463)	Connector: banana, male

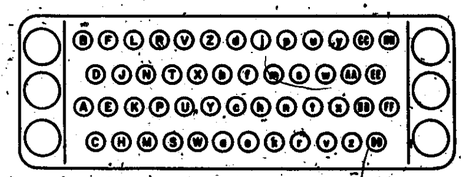
2. CONNECTOR WIRING

Connector	Signal Name	Signal Description	Connection
J4	SAMPLE INPUT	Frequency: < 20 kHz. Pulses, L = 0V or more negative, H = +2V or more positive	J27(15) API line 94
J5	SAMPLE OUTPUT	Sample pulses, 1000 pulses per sweep. L = +0.4V or more negative, H = +2.5V or more positive	J23(23) LPI line 166
J6	NOISE OUTPUT	Train of voltage pulses whose amplitude equals difference between INPUT and AVERAGE. Amplitude is proportional to CRT display of NOISE (0.5V per cm of deflection). Can be gated with Z-AXIS OUTPUT	J27(25) API line 24

Table 4-2. Wiring Lists (Cont'd)

PART F (Cont'd)

Connector	Signal Name	Signal Description	Connection
J7	NEG SYNCH OUTPUT	Negative pulse at start of each sweep (before PRE-ANALYSIS DELAY). Level: -12V; Width: >0.5 usec	J27(14) API line 98
J8	POS SYNCH OUTPUT	Positive pulse at start of each sweep (before PRE-ANALYSIS DELAY). Level: +12V; Width: >0.5 usec	J27(39) API line 97
J9	HORIZ DAC OUTPUT	Sweep ramp. 0V to +10V; 0.2% linearity	J26(45) Display line 3
J10	VERT DAC OUTPUT	-4V to +4V, proportional to CRT display)1.0V per cm deflection); 0.2% linearity	J33 (BNC) Memory line 23
J11	Z AXIS OUTPUT	+5V blanking pulses (can be used to gate NOISE OUTPUT)	A1A1(15) Display line 21
J12	EXTERNAL DATA INPUT		
J12(1-12)	Not used		J27(1-12)
J12(13-24)	Not used		J27(26-37)
J13	POINT PLOTTER SEEK	Positive pulse tells Point Plotter to seek a null. Level: +10V; Width: >50 usec	J27(44) API line 101
J14	POINT PLOTTER PLOT	Positive pulse from Point Plotter indicates plot is complete. Level: >+2V; Width: 200 nsec	J27(45) API line 92
J15-J18	SYSTEM LOGIC INTERCONNECTION		



J15-J18 NOTES:

H = +2.5V or more positive voltage level
L = +0.4V or more negative voltage level
N = negative pulse, 200 nsec wide (H to L to H)
P = positive pulse, 200 nsec wide (L to H to L)

A = voltage step from L to H (positive step)
B = voltage step from H to L (negative step)
LE = trigger (clock) on leading edge of pulse
TE = trigger (clock) on trailing edge of pulse

J15 and J17 are only on 5480A's with serials prefixed 852- and below.

Table 4-2. Wiring Lists (Cont'd)

PART F (Cont'd)

Connector	Signal Name	Signal Description*	Connection
J15 SYSTEM LOGIC INTERCONNECTION A			
J15(A)	Not used		
J15(B)	Not used		
J15(C)	CYCLE	N, LE	J2(45) Mem line 38
J15(D)	EN SHIFT IN	N, LE	A3A2(E) MFL line 10
J15(E)	SET VERT	L=TRUE	J2(15) Mem line 26
J15(F)	$\overline{\text{CLEAR 1}}$	L=TRUE	A3A2(S) MFL line 13
J15(H)	$\overline{\text{SHIFT 1}}$	N, LE	A3A2(R) MFL line 15
J15(J)	Not used		
J15(K)	Not used		
J15(L)	Not used		
J15(M)	EXT AR 0	L=TRUE	A3A9(M) MFL line 171
J15(N)	SHIFT PAR A	N, LE	A3A12(14) MFL line 156
J15(P)	EN C UP 20 MHz	L=TRUE	A3A2(X) MFL line 17
J15(R)	EN C DN 20 MHz	L=TRUE	A3A2(Y) MFL line 23
J15(S)	EXT AR 1	L=TRUE	A3A9(N) MFL line 172
J15(T)	CLEAR PAR A	N, LE	A3A12(12) MFL line 214
J15(U)	SET DAR	L=TRUE	J2(39) Mem line 126
J15(V)	$\overline{\text{SET HORIZ}}$	N, LE	J2(42) Mem line 40
J15(W)	EXT AR 2	L=TRUE	A3A10(B) MFL line 173
J15(X)	$\overline{\text{READ}}$	N, LE	P2(43) Mem line 34
J15(Y)	$\overline{\text{WRITE}}$	N, LE	P2(44) Mem line 36
J15(Z)	Not used		
J15(a)	EXT AR 3	L=TRUE	A3A10(C) MFL line 174
J15(b)	EN SHIFT IN PAR	L=TRUE	A3A12(H) MFL line 146
J15(c)	$\overline{\text{EXT PREP}}$	N, LE	J23(1) LPI line 106
J15(d)	$\overline{\text{EXT AVE}}$	N, LE	J23(2) LPI line 105
J15(e)	EXT AR 4	L=TRUE	A3A10(D) MFL line 175
J15(f)	Not used		
J15(h)	$\overline{\text{SET L DISPLAY}}$	Output, N, LE	J23(3) LPI line 157
J15(j)	START ADC	Output, L=TRUE	J23(6) LPI line 73

*See J15-J18 Notes.

Table 4-2. Wiring Lists (Cont'd)

PART F (Cont'd)

Connector	Signal Name	Signal Description	Connection
J15(k)	EXT AR 5	L=TRUE	A3A10(E) MFL line 176
J15(m)	Not used		
J15(n)	CS ATTACHED	L=TRUE	J23(7), J27(19) LPI line 107 API line 79
J15(p)	L STOP	Output, L=TRUE	J23(8) LPI line 153
J15(r)	EXT AR 6	L=TRUE	A3A11(B) MFL line 177
J15(s)	Not used		
J15(t)	Not used		
J15(u)	Not used		
J15(v)	EXT AR 7	L=TRUE	A3A11(C) MFL line 178
J15(w)	Not used		
J15(x)	Not used		
J15(y)	Not used		
J15(z)	EXT AR 8	L=TRUE	A3A11(D) MFL line 179
J15(AA)	ENABLE PAR TO HOLD	L=TRUE	A3A12(T) MFL line 192
J15(BB)	Not used		
J15(CC)	Not used		
J15(DD)	EXT AR 9	L=TRUE	A3A11(E) MFL line 180
J15(EE)	Not used		
J15(FF)	GRD		
J15(HH)	GRD		
J16 SYSTEM LOGIC INTERCONNECTION B			
J16(A)	EN SHIFT LEFT	N, LE	A3A2(C) MFL line 6
J16(B)	EN SHIFT RIGHT	N, LE	A3A2(D) MFL line 8
J16(C)	ENABLE COUNT	N, LE	A3A2(B) MFL line 4
J16(D)	Same as J15(B)		
J16(E)	EN OPEN LOOP	N, LE	A3A2(F) MFL line 27
J16(F)	Same as J15(F)		
J16(H)	Same as J15(H)		
J16(J)	EN C UP A	N, TE	A3A2(V) MFL line 21
J16(K)	EN C DN A	N, TE	A3A2(W) MFL line 25
J16(L)	EN SHIFT RT PAR	N, LE	A3A12(F) MFL line 144
J16(M)	EN COUNT PAR	N, LE	A3A12(E) MFL line 142
J16(N)	Same as J15(N)		
J16(P)	ADVANCE PAR +1	N, TE	A3A9(D) MFL line 186
J16(R)	ADVANCE PAR -1	N, TE	A3A9(E) MFL line 188
J16(S)	EN DAR TO PAR	N, LE	A3A12(10) MFL line 148

Table 4-2. Wiring Lists (Cont'd)

PART F (Cont'd)

Connector	Signal Name	Signal Description	Connection
J16(T)	Same as J15(T)		
J16(U)	Same as J15(U)		
J16(W)	Same as J15(V)		
J16(W)	MOD HOLD	N, TE	J2(16) Mem line 51
J16(X)	Same as J15(X)		
J16(Y)	Same as J15(Y)		
J16(Z)	$\overline{\text{AR 9}}$	Output; L=TRUE	A3A11(5) MFL line 202
J16(a)	$\overline{\text{PAR 0}}$	Output; L=TRUE	A3A9(K) MFL line 205
J16(b)	SHIFT RT PAR C	L=TRUE	A3A11(14) MFL line 209
J16(c)	$\overline{\text{SAAR 0}}$	L=TRUE	J2(28) Mem line 125
J16(d)	$\overline{\text{SBAR 0}}$	L=TRUE	J2(29) Mem line 124
J16(e)	$\overline{\text{SBAR 1}}$	L=TRUE	J2(30) Mem line 122
J16(f)	$\overline{\text{SAAR 1}}$	L=TRUE	J2(31) Mem line 123
J16(h)	$\overline{\text{AR 0}}$	Output; L=TRUE	A3A9(Y) MFL line 193
J16(j)	$\overline{\text{AR 1}}$	Output; L=TRUE	A3A9(X) MFL line 194
J16(k)	MAIN SRQ	L=TRUE	J23(43) LPI line 193
J16(m)	SUB SRQ	L=TRUE	J23(44) LPI line 194
J16(n)	MBSL	Output; L=TRUE	J23(46) LPI line 39
J16(p)	$\overline{\text{OUTPUT MPX}}$	Output; L=TRUE	J23(12) LPI line 110
J16(r)	$\overline{\text{L DISPLAY}}$	Output; L=TRUE	J23(11) LPI line 190
J16(s)	CHANNEL COMMAND	L=TRUE	J27(18) API line 40
J16(t)	+5 volts	Output	
J16(u)	$\overline{\text{SAAR 2}}$	L=TRUE	J2(32) Mem line 128
J16(v)	$\overline{\text{SAAR 3}}$	L=TRUE	J2(33) Mem line 129
J16(w)	ADVANCE PAR +4	L=TRUE	A3A9(H) MFL line 216
J16(x)	ADVANCE PAR +2	L=TRUE	A3A9(F) MFL line 217
J16(y)	INTENSITY MOD	L=TRUE	A1A1(13) Disp line 16
J16(z)	START PBM	L=TRUE	A4A1A(8) LD & FF line 32
J16(AA)	Same as J15(AA)		
J16(BB)	STOP PBM	L=TRUE	A4A1A(8) LE & FF line 13
J16(CC)	DISPLAY PBM	L=TRUE	A4A1A(14) LD & FF line 14
J16(DD)	RECORD PBM	L=TRUE	A4A1A(16) LD & FF line 18

Table 4-2. Wiring Lists (Cont'd)

PART F (Cont'd)

Connector	Signal Name	Signal Description	Connection
J16(EE)	CLEAR DISPLAY	L=TRUE	A4A1A(15), A4A1B(9) LD & FF line 1

J17, J18 SYSTEM INTERCONNECTION C1, C2. These connectors are wired in parallel. Signal appears at indicated pin of either connector.

A	$\overline{\text{EXT AC 0}}$	L=TRUE	A3A3(7) MFL line 72
B	AC 0	Output, H=TRUE	A3A3(20) MFL line 97
C	$\overline{\text{EXT AC 12}}$	L=TRUE	A3A6(7) MFL line 84
D	AC 12	Output, H=TRUE	A3A6(20) MFL line 109
E	$\overline{\text{EXT AC 1}}$	L=TRUE	A3A3(6) MFL line 73
F	AC 0	Output, H=TRUE	A3A3(X) MFL line 98
H	$\overline{\text{EXT AC 13}}$	L=TRUE	A3A6(6) MFL line 85
J	AC 13	Output, H=TRUE	A3A6(X) MFL line 110
K	$\overline{\text{EXT AC 2}}$	L=TRUE	A3A3(5) MFL line 74
L	AC 2	Output, H=TRUE	A3A3(21) MFL line 99
M	$\overline{\text{EXT AC 14}}$	L=TRUE	A3A6(5) MFL line 86
N	AC 14	Output, H=TRUE	A3A6(21) MFL line 111
P	$\overline{\text{EXT AC 3}}$	L=TRUE	A3A3(4) MFL line 75
R	AC 3	Output, H=TRUE	A3A3(Y) MFL line 100
S	$\overline{\text{EXT AC 15}}$	L=TRUE	A3A6(4) MFL line 87
T	AC 15	Output, H=TRUE	A3A6(Y) MFL line 112
U	$\overline{\text{EXT AC 4}}$	L=TRUE	A3A4(7) MFL line 76
V	AC 4	Output, H=TRUE	A3A4(20) MFL line 101
W	$\overline{\text{EXT AC 16}}$	L=TRUE	A3A7(7) MFL line 88
X	AC 16	Output, H=TRUE	A3A7(20) MFL line 113
Y	$\overline{\text{EXT AC 5}}$	L=TRUE	A3A4(6) MFL line 77
Z	AC 5	Output, H=TRUE	A3A4(X) MFL line 102
a	$\overline{\text{EXT AC 17}}$	L=TRUE	A3A7(6) MFL line 89
b	AC 17	Output, H=TRUE	A3A7(X) MFL line 114

Table 4-2. Wiring Lists (Cont'd)

PART F (Cont'd)

Connector	Signal Name	Signal Description	Connection
c	$\overline{\text{EXT AC 6}}$	L=TRUE	A3A4(5) MFL line 78
d	AC 6	Output, H=TRUE	A3A4(21) MFL line 103
e	$\overline{\text{EXT AC 18}}$	L=TRUE	A3A7(5) MFL line 90
f	AC 18	Output, H=TRUE	A3A7(21) MFL line 115
h	$\overline{\text{EXT AC 7}}$	L=TRUE	A3A4(4) MFL line 79
j	AC 7	Output, H=TRUE	A3A4(Y) MFL line 104
k	$\overline{\text{EXT AC 19}}$	L=TRUE	A3A7(4) MFL line 91
m	AC 19	Output, H=TRUE	A3A7(Y) MFL line 116
n	$\overline{\text{EXT AC 8}}$	L=TRUE	A3A5(7) MFL line 80
p	AC 8	Output, H=TRUE	A3A5(20) MFL line 105
r	$\overline{\text{EXT AC 20}}$	L=TRUE	A3A8(7) MFL line 92
s	AC 20	Output, L=TRUE	A3A8(20) MFL line 117
t	$\overline{\text{EXT AC 9}}$	L=TRUE	A3A5(6) MFL line 81
u	AC 9	Output, H=TRUE	A3A5(X) MFL line 106
v	$\overline{\text{EXT AC 21}}$	L=TRUE	A3A8(6) MFL line 92
w	AC 21	Output, H=TRUE	A3A8(X) MFL line 118
x	$\overline{\text{EXT AC 10}}$	L=TRUE	A3A5(5) MFL line 82
y	AC 10	Output, H=TRUE	A3A5(21) MFL line 107
z	$\overline{\text{EXT AC 22}}$	L=TRUE	A3A8(5) MFL line 93
AA	AC 22	Output, H=TRUE	A3A8(21) MFL line 119
BB	$\overline{\text{EXT AC 11}}$	L=TRUE	A3A5(4) MFL line 83
CC	AC 11	Output, H=TRUE	A3A5(Y) MFL line 108
DD	$\overline{\text{EXT AC 23}}$	L=TRUE	A3A8(4) MFL line 94
EE	AC 23	Output, H=TRUE	A3A8(Y) MFL line 120
FF	GRD		
HH	GRD		
J19	SWEEP VOLTAGE OUTPUT	Sweep ramp, 0V to +1V (0V to any value 10V obtainable by changing internal resistor)	J27(33) API line 96

Table 4-2. Wiring Lists (Cont'd)

PART F (Cont'd)

Connector	Signal Name	Signal Description	Connection
J29	AC POWER	AC power input 115 or 230V	
J29	VERTICAL SCOPE OUTPUT	-5V to +5V, proportional to CRT display. API POSITION control determines dc offset of this signal.	J26(49) API line 78
J30	PEN LIFT CONTROL	Output, +5V = Pen UP; 0V = Pen DOWN (5480A only, see J36(4) for 5480B.)	J23(24) LPI line 208
J31	MCS INPUT	Signal input for MCS FUNCTION. Pulses; amplitude between 2V and 20V; max rep rate 1 MHz; min width 500 nsec; pulse pair resolution 500 nsec; input impedance 3K ohms minimum	J27(49) API line 91
J32	VARIANCE OUTPUT	Square of noise signal. Available only when variance option installed in API (5485A Option 01)	J27(46) API line 88
A1J1	CALIBRATOR	Square wave, 1V P-P. Frequency depends on LPI SWEEP TIME setting.	Display line 20

PART G — 5485A TWO CHANNEL INPUT (API) Table 4-2 (Cont'd)

Wiring Diagram: Figure 4-11

This part of the table lists all connections in the 5485A Two Channel Input (Analog Plug-in) unit.

Note:

Shading at line 79 indicates that the C.S. Attached signal was an input from 5480A rear-panel connector J15 (serials prefixed 852- and below). The 5485A wiring was not changed when the 5480A rear panel was changed (by deleting J15 and J17).

Table 4-2. Wiring Lists (Cont'd)

PART G 5485A (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	INPUT AMPLIFIER A1	SAMPLE AND HOLD A3	ADC A3	SWITCHING LOGIC A A5 OUTPUT AMPLIFIER	SWITCHING LOGIC B A6	INTERFACE A7	P25	P26	P27	P28	J22	J23	J24	REMARKS
1	+12V	P28(4)	9, K								4					From Main Frame
2	-12V	P28(12)	20, X								12					
3	+5V	P28(2, 10)	12, N								2, 10					Also on Pin A1 (14) thru 100
4	GRD	P28(1, 9, 8, 16)	17, U 19, W			17, U					1, 9, 8, 16					From Main Frame
5	+19.5V	P28(6)					11, M				6					From Memory Regulator
6	-19.5V	P28(14)		8							14					
7	INPUT A	A8P1	J1													From J1 thru A8
8	INPUT B	A8P1	J2													From J2 thru A8
9	"A" POLARITY	S3	5													
10	"B" POLARITY	S10	10													
11	DC BAL A	R3	16													
12	DC BAL B	R5	13													
13	A+B/ALT	S7	4													
14	CHAN "A"	A4(10)	6		10											
15	INPUT AMPL OUTPUT	A1(1)	1	1												
16	SWAVE	P25(2)		18				2							27	From LPI Line 80
17	START (T0)	P25(15)		5				15							40	From LPI Line 166
18	STOPT (T12)	P25(44)		6											19	From LPI Line 59
19	VERTICAL DAC	P26(47)		11					47							From Mem Line 23 thru J33
20	BASELINE ADJ	R6		13												
21	DC BAL A+B	R4		10												
22	+REF	A2(7)		7												To R4 & R6
23	-REF	A2(8)		8												To R6 A+B Balance
24	NOISE SIGNAL	A2(22)		22	22	3				25						To Rear Panel J6
25	SAMPLED SIGNAL	A2(6)		6		2										
26	DATA SIGNAL	A2(14)		f4		1										
27	START ADC	P25(19)			13		13	19						6	34	From LPI Line 73
28	TBB1	P25(7)			2			7							32	From LPI Line 33
29	TBB2	P25(9)			9			8							33	From LPI Line 34
30	RESET ADC	P25(20)			14			20							35	From LPI Line 117

Table 4-2. Wiring Lists (Cont'd)

PART G 5485A (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	INPUT AMPLIFIER A1	SAMPLE AND HOLD A2	ADC A3	SWITCHING LOGIC A A4	OUTPUT AMPLIFIER A5	SWITCHING LOGIC B A6	INTERFACE A7	P25	P26	P27	P28	J15	J31	J32	J33	J34	REMARKS
31	RAMP FIN	A3(16)			16		16												
32	COUNT DN ENABLE	A3(21)			21		21			42							37, 12			MFL 191 LPI 210
33	COUNT UP ENABLE	A3(18)			18		R			17							36, 10			To MFL Line 189
34	7 BITS	A3(1)			1		10		35										10	To LPI Line 179
35	9 BITS	A3(6)			6		11		36										11	To LPI Line 180
36	$\overline{SAAR1}$	P27(43)			S						43									From Memory Line 123
37	$\overline{SBAR1}$	P27(22)			R						22									From Memory Line 122
38	$\overline{SBAR0}$	P27(42)			15						42									From Memory Line 124
39	$\overline{SAAR0}$	P27(21)			14						21									From Memory Line 125
40	CHANNEL COMMAND	P27(18)			T						18									From EXT Source
41	$\overline{AR0}$	P26(14)			E					14										From MFL Line 193
42	$\overline{AST}$	P26(39)			F					39										From MFL Line 194
43	HISTO-GRAM	P25(37)			U		4		37											From EXT Data J12(24)
44	SET MIN MPY	P25(11)			M				11										36	From LPI Line 117
45	SET VERT	P25(10)			L				10										35	From LPI Line 121
46	L DISPLAY	P25(5)			J		5												30	From LPI Line 139
47	A OFF	S1AF (1-1, 2)			13															From "A" Display SW
48	"A" DATA SIGNAL	S1AF (5-1, 2)																		
49	DA	S2CF(2)			5															From "A" Mem Select
50	CA	S2CF(1)			6															
51	BA	S2BF(2)			7															
52	AA	S2AF(1)			8															
53	EA	S2DF(7)			22															From "A" Mem Select (O'lap)
54	"B" OFF	S4AF (1-1/2)			11															From "B" Display SW
55	"B" DATA SIGNAL	S4AF (5-1, 2)			16															
56	DB	S5CF(2)			1															From "B" Mem Select
57	CB	S5CF(1)			2															
58	BB	S5BF(2)			3															
59	AB	S5AF(1)			4															
60	EB	S5DF(7)			Z															From "B" Mem Select (O'lap)

Table 4-2. Wiring Lists (Cont'd)

PART G 5485A (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	INPUT AMPLIFIER A1	SAMPLE AND HOLD A2	ADC A3	SWITCHING LOGIC A A4	OUTPUT AMPLIFIER A5	SWITCHING LOGIC B A6	INTERFACE A7	P25	P26	P27	P28	J15	J31	J32	J33	J34	REMARKS
61	CHAN OK	A4(H)			H					34								9	To LPI Line 137
62	DISPLAY DEFEAT	A4(21)			21					12								37	To LPI Line 162
63	$\overline{MAAR1}$	A4(A)			A						40									To Memory Line 133
64	$\overline{MBAR1}$	A4(B)			B						41									To Memory Line 132
65	$\overline{MBAR0}$	A4(C)			C					1	15									To Memory Line 130
66	$\overline{MAAR0}$	A4(D)			D						16									To Memory Line 131
67	OVERLAY	A4(16)			16	16														
68	SEG	A4(17)			17	6														
69	A DISP	A4(P)			P	13														
70	"A" NOISE SIGNAL	S1AF (7-1/2)				A														From "A" Display SW
71	"A" INPUT SIGNAL	S1AF (3-1/2)				B														
72	"B" NOISE SIGNAL	S4AF (7-1/2)				D														From "B" Display SW
73	"B" INPUT SIGNAL	S4AF (3-1/2)				E												6		
74	"A" VERNIER	A8R309				H														
75	"A" POSITION	R1				L														
76	"B" VERNIER	A8R309				J														
77	"B" POSITION	R2				M														
78	VERT DEFLECTION	A5(18)			18					49										To Disp Sect. & Vert Scope Out
79	C.S. ATTACHED	P27(19)		15.S	14						19							7		From Exit Source
80	10 MHZ CLOCK	P25(41),				V		41											16	From LPI Line 43
81	TIME HISTOGRAM	S8				3														
82	FREQ HISTOGRAM	S8				1														
83	L STOP	P25(40)				6		40											15	From LPI Line 153
84	ADC FIN	A6(22)				22		30											9	To LPI Line 103
85	ENABLE COUNT UP A	A6(15)				15			33											To MFL Line 21
86	$\overline{FREQ\ HIST}$	A6(S)				S		17											42	To LPI Line 159
87	$\overline{TIME\ HIST}$	A6(T)				T		18											43	To LPI Line 160
88	VARIANCE OUTPUT	A6(Y)				Y			46											To J32 (Rear) Variance Out
89	HORIZ DAC	P26(44)					10		44, 45											From Mem Line 42 to Rear Panel J9
90	RESET TBI	P25(14)					2	14											39	From LPI Line 38