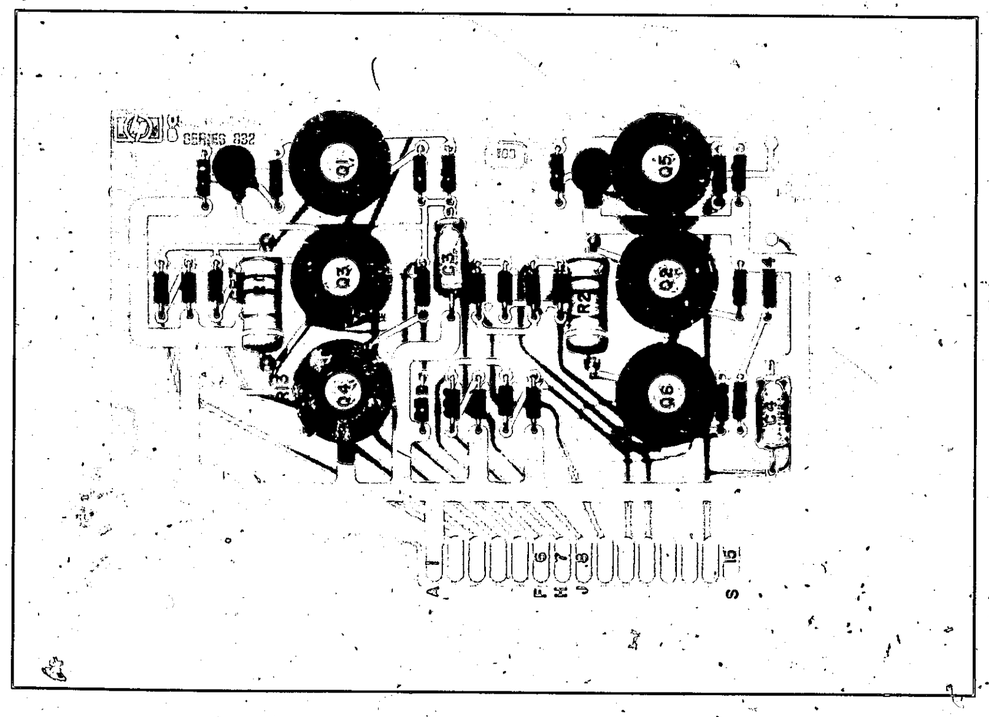
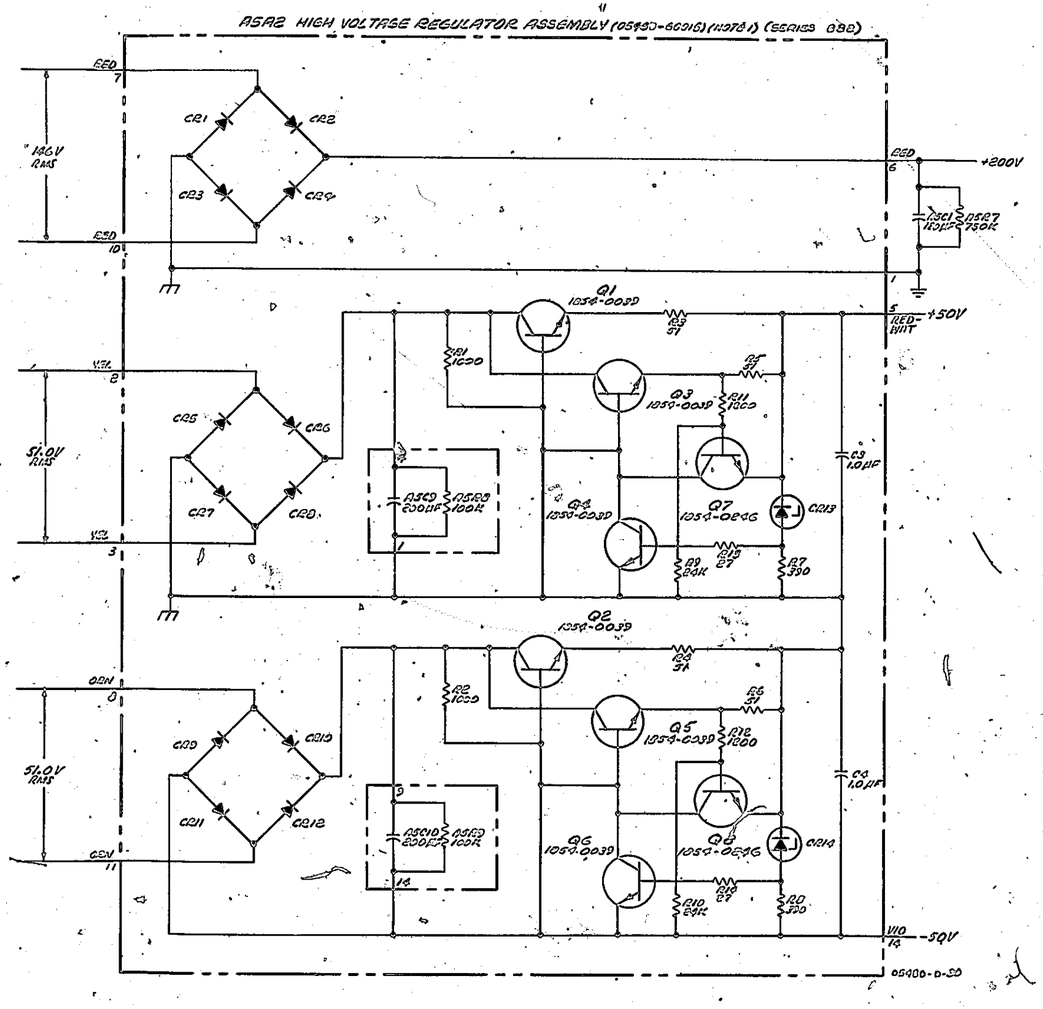
HEWLETT PACKARD

SIGNAL ANALYZER 5480AB WITH 5485A 5486AB,5487A,5488A PLUG-INS
SERVICE VOL. II III & IV SERIAL PFX ALL SERIALS
PART NO. 05480-90013 (MANUAL) 05480-90016 (FICHE)
APRIL 1971 4 of 8

See Figure 2-40 for board description.





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;

REFERENCE DESIGNATIONS

A5	A5A2
C1,2,10	C3,4, CR1-14, Q1-8 R1-12
R7-9	

Figure 2-41
A5A2 High Voltage Regulator Series 332

SECTION III

ANALOG PLUG-IN UNITS (5485A, 5487A, 5488A)

The Plug-In Units described in this manual section are operated in the 5480A/B right-hand plug-in compartment. The plug-in units are similar, the major differences being in the front-end signal processing circuits for four-channel-vs-two-channel operation or correlation-vs-variance operation.

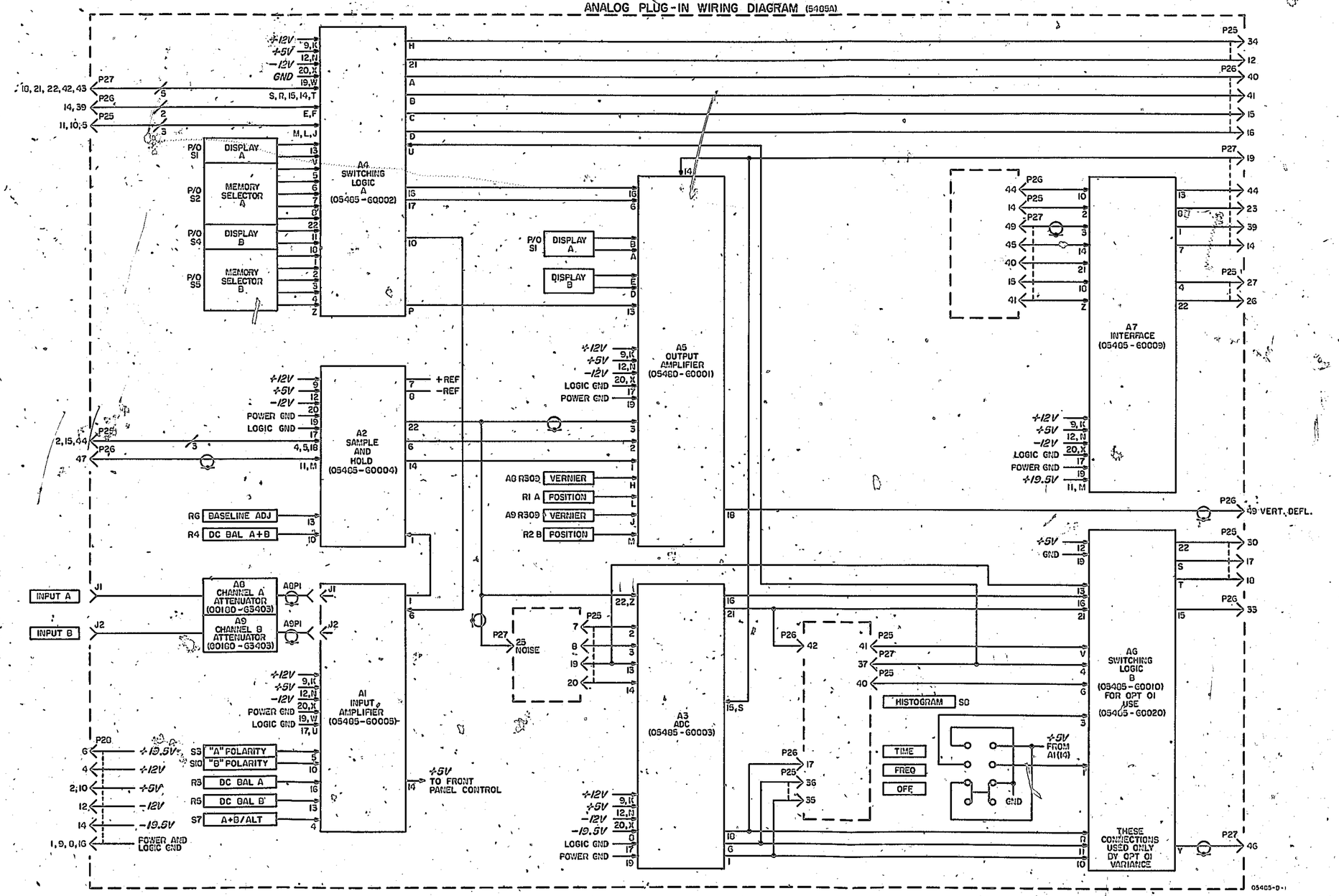


Figure 3-1
5405A Wiring Diagram

S1, 2, 4, 5 DISPLAY AND MEMORY SELECTOR SWITCHES

Truth Table for 5485A Memory Selector Switches

H = +5 L = 0

		AA	BA	CA	DA	EA
QUARTER	1	L	H	L	H	H
	2	L	H	H	L	H
	3	H	L	L	H	H
	4	H	L	H	L	H
HALF	1, 2	L	H	H	H	H
	3, 4	H	L	H	H	H
FULL		H	H	H	H	H
OVERLAP		H	H	H	H	L

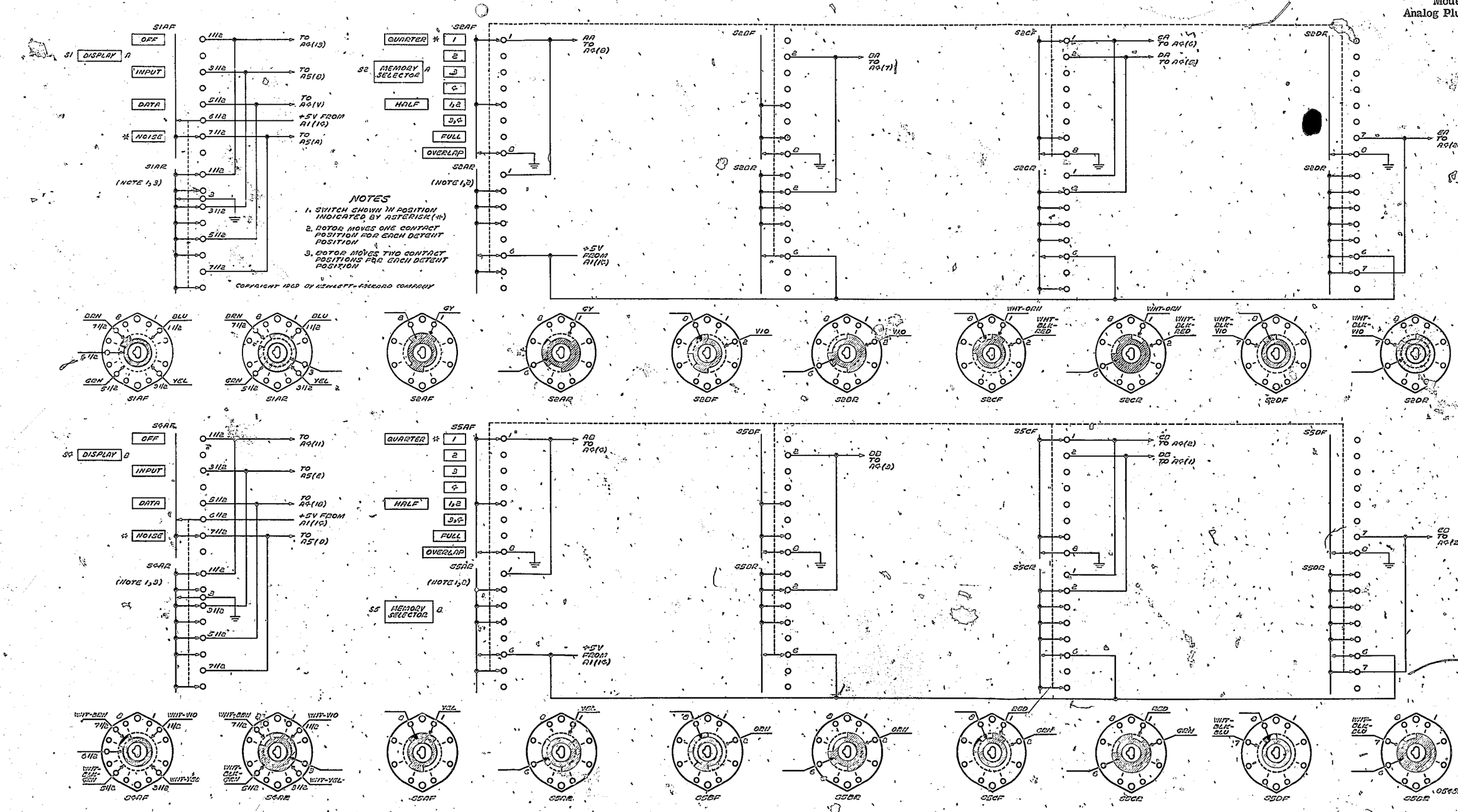


Figure 3-2
S1, 2, 4, 5, Display and Memory Selector Switches

A1 INPUT AMPLIFIER BOARD (05485-60005)

LOGIC AND DESCRIPTION

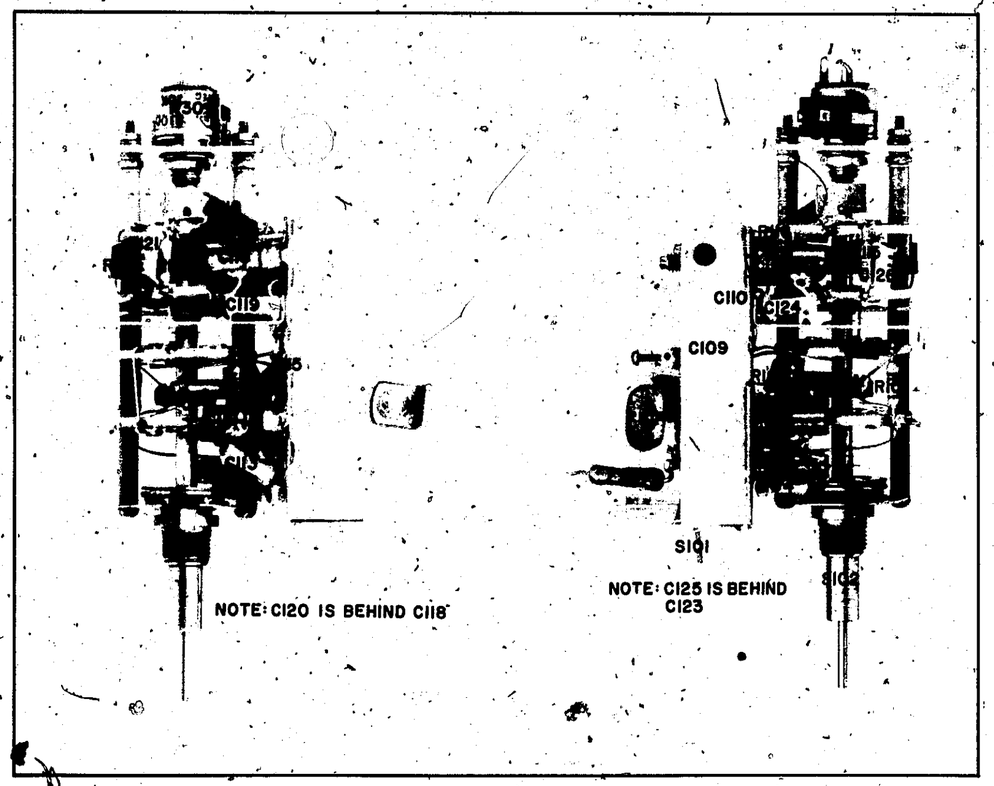
The 05485-60005 Board contains two Fet Input Operational Amplifiers with + and - Polarity outputs and an Analog Multiplexer. The Amplifier outputs can be mixed in the Multiplexer to give ± A, ± B, A+B, B-A, as controlled by the Front Panel Polarity Switches and the A+B, Alternate Switch.

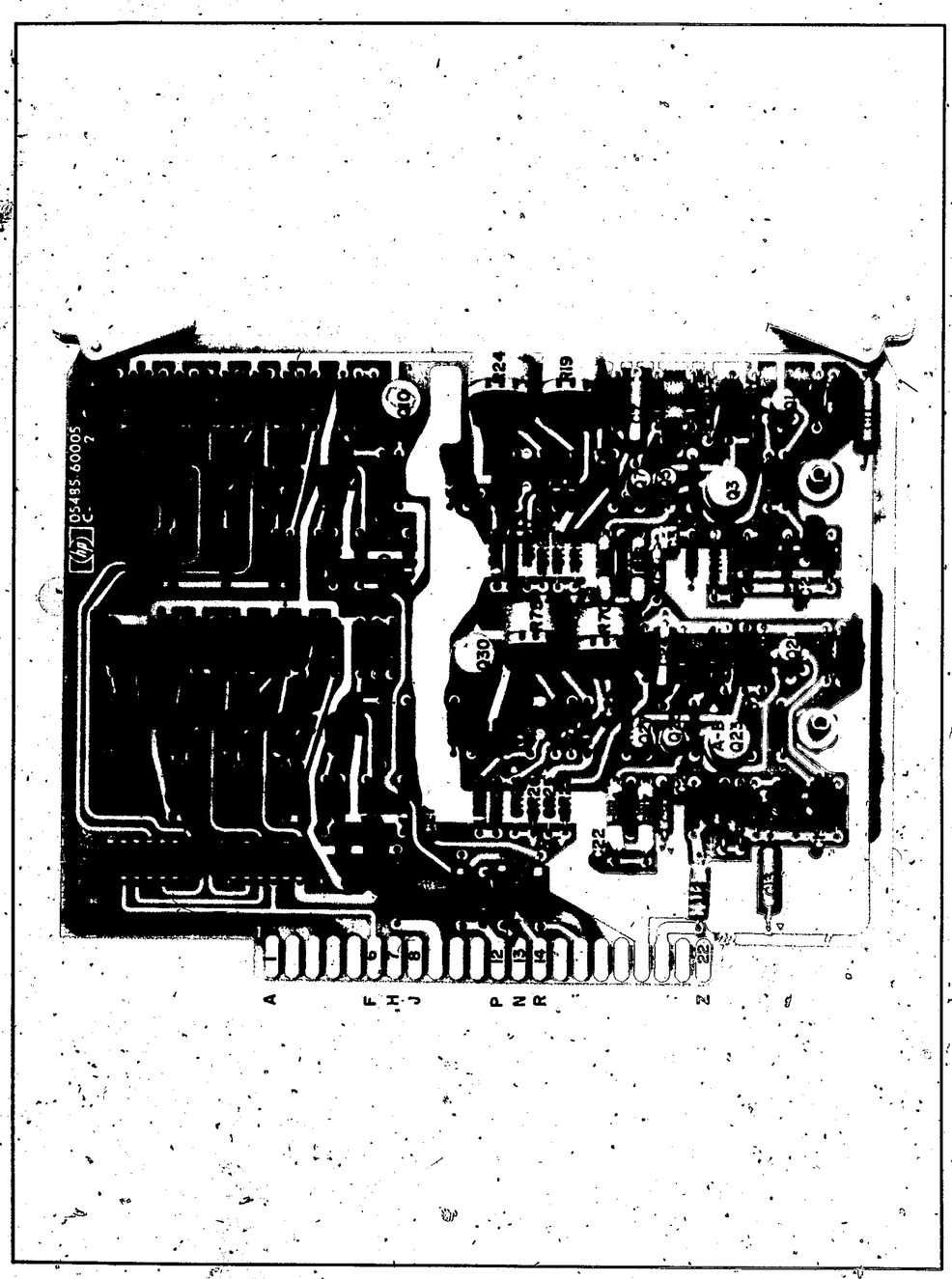
CHANGES FOR OLDER BOARDS

Current Series: 852

Older Series: 832 (see Figure 3-4)

The newer series board is a direct replacement for the older series board.





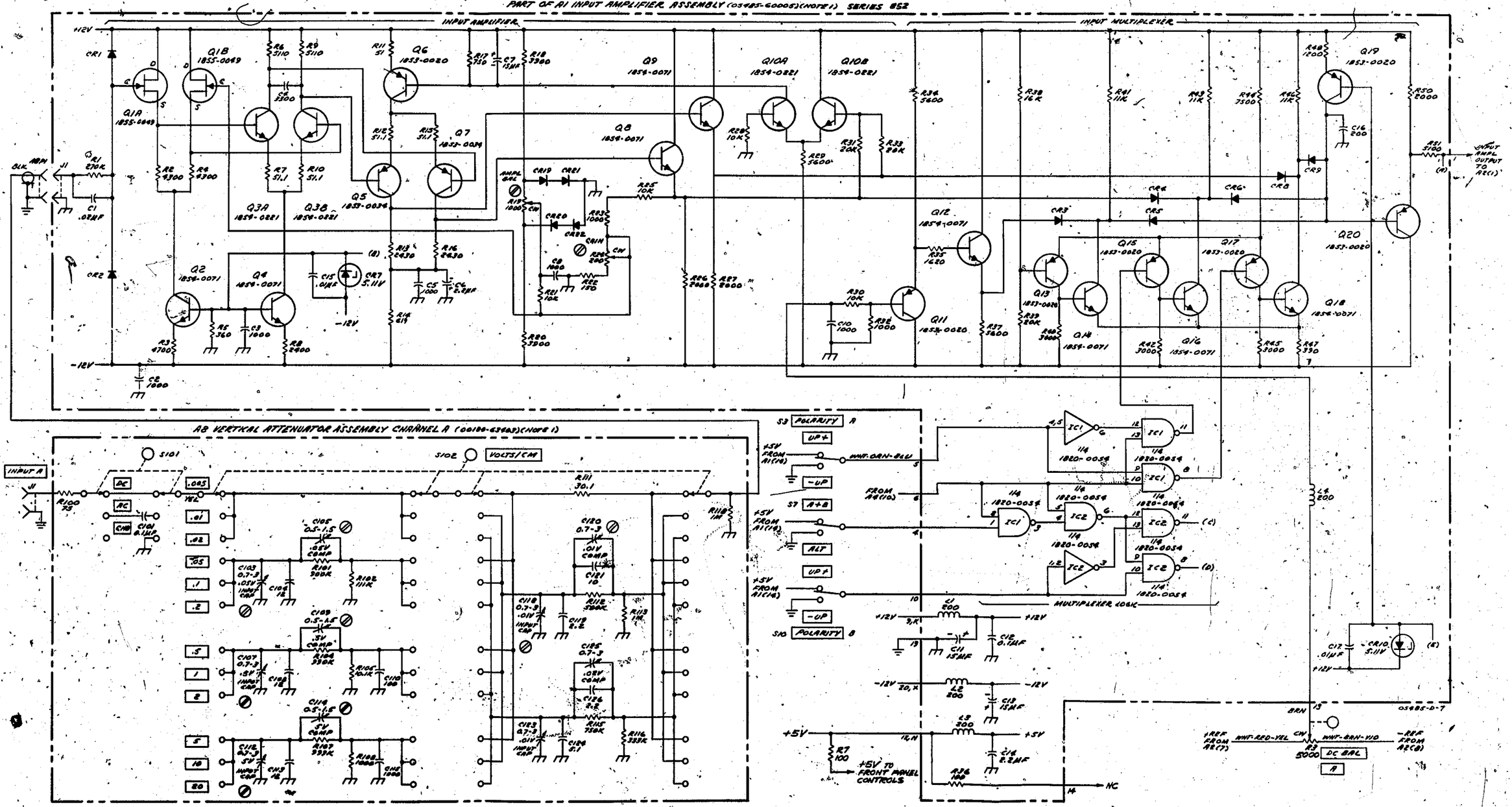
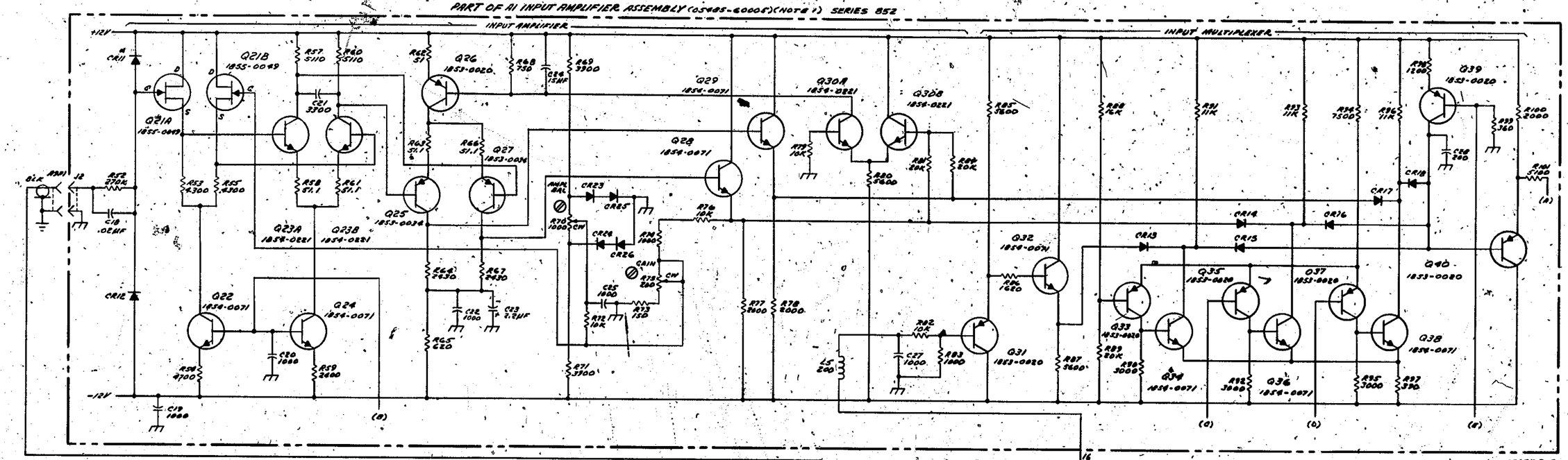


Figure 3-3
A1, 8, 9 Input Amplifier and Vertical Attenuator
Series 852 (Sheet 1 of 2)

See Sheet 1 of this Figure for A1 Board description, Component Locator and Switch description.



NO PREFIX	A1	A8, A9
	C1-28	C101-126
	CR1-26	
	IC1, 2	
J1, 2	J1, 2	
	L1-5	
	Q1-60	
		RDM, RDM1
R3, 5	R1-101	R100-118
S1, 7, 10		S101, 102

DELETED: C9, 26, R49, 56

NOT ASSIGNED: C102, 104, 111, 116, 117, 122, R103, 108, 109, 110, 114, 119

Figure 3-3
A1, 8, 9 Input Amplifier and Vertical Attenuator
Series 852 (Sheet 2 of 2)

See Figure 3-3, Sheet 1 for A1 Board description.

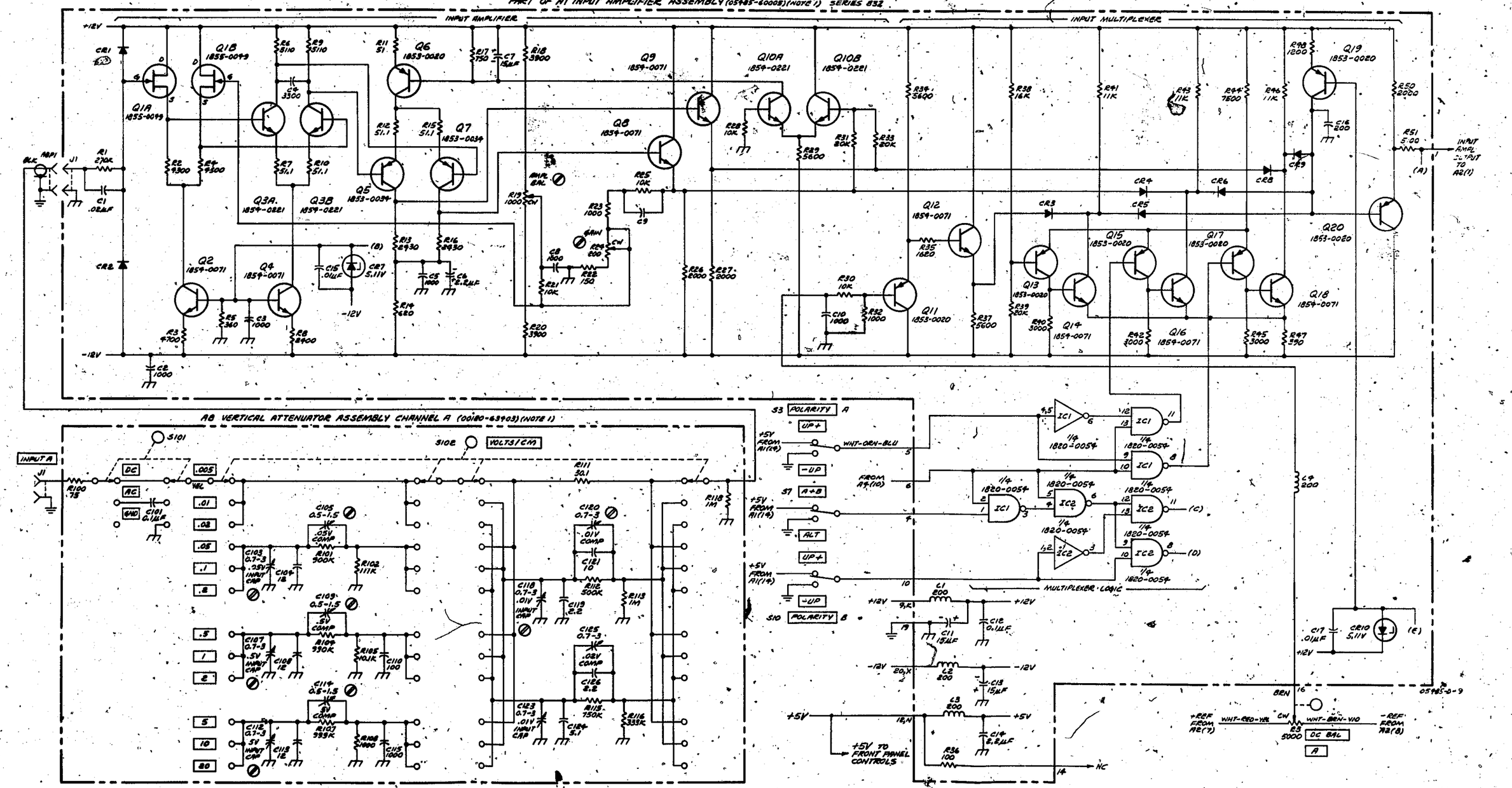


Figure 3-4
A1, 8, 9, Input Amplifier and Vertical Attenuator Series 832 (Sheet 1 of 2)

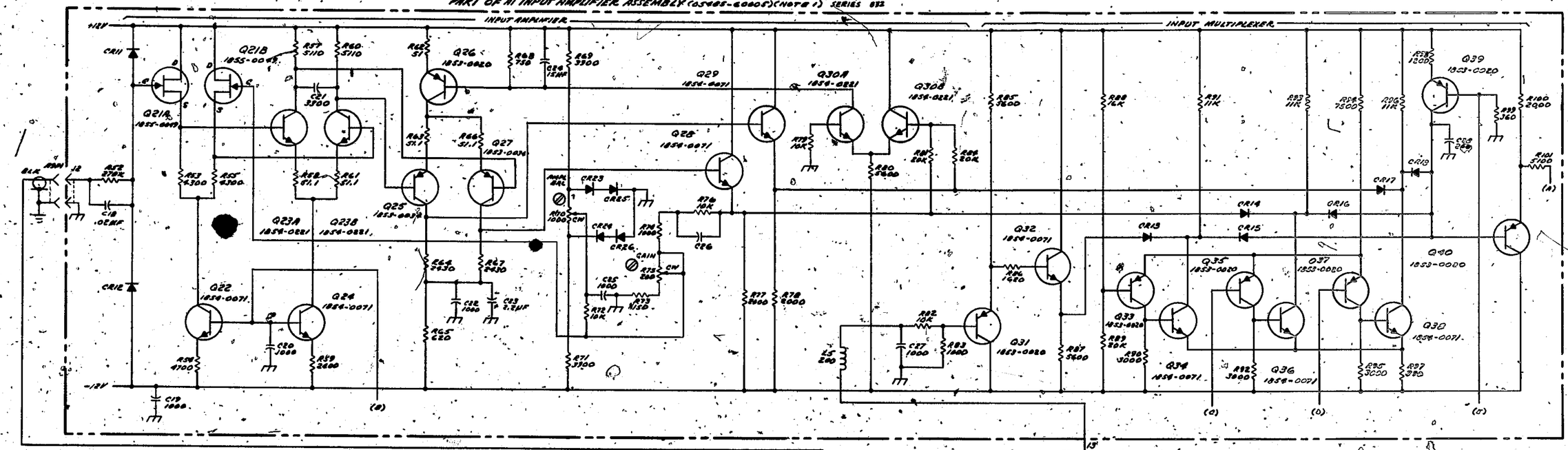


Figure 3-4
A1, 8, 9 Input Amplifier and Vertical Attenuator
Series 832 (Sheet 2 of 2)

A2 SAMPLE AND HOLD BOARD (05485-60004)

LOGIC AND DESCRIPTION

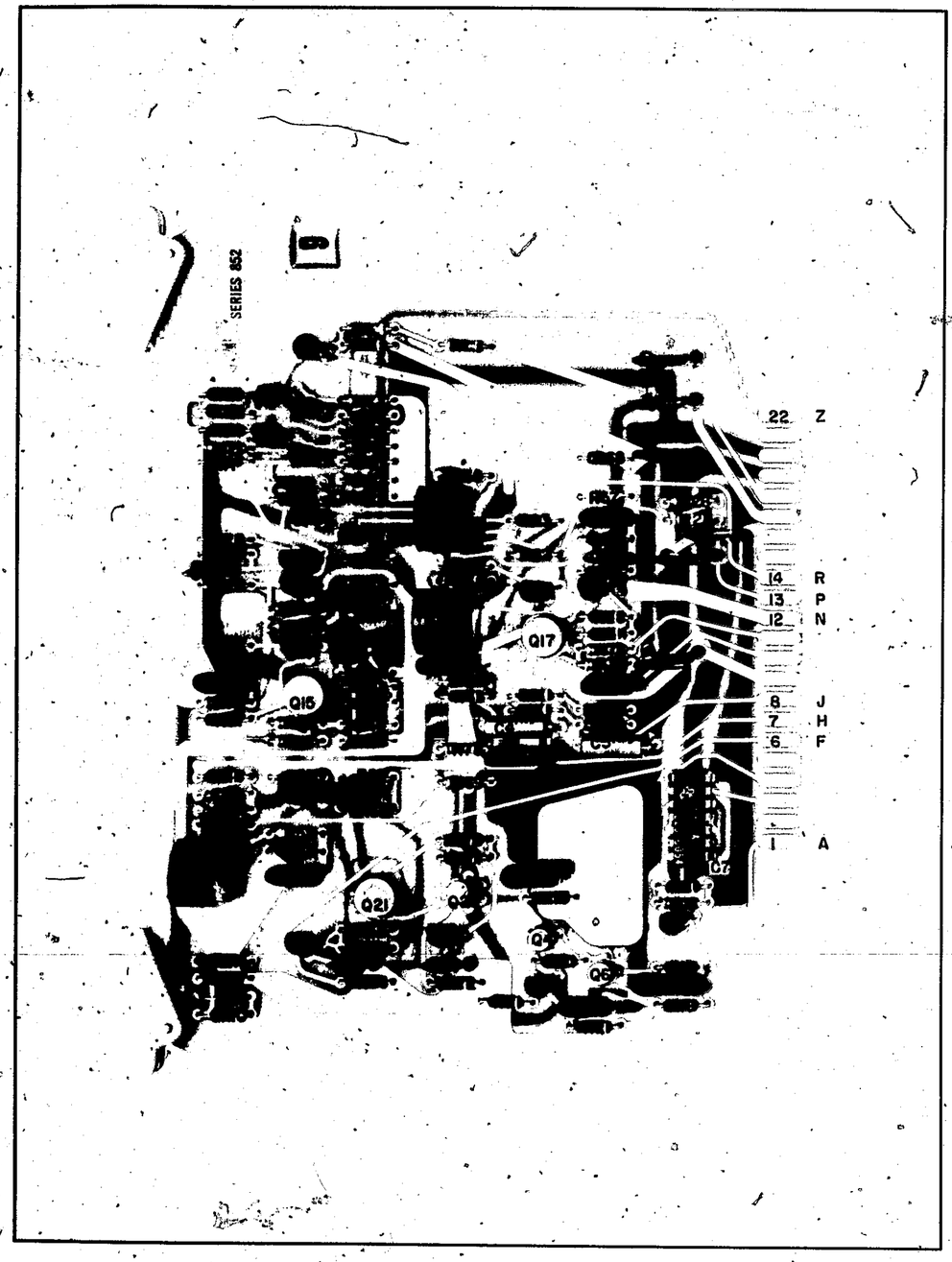
The 05485-60004 Board contains the Sample and Hold Circuitry and Differential Amplifier. The Sample and Hold Circuit contains a Fet Switch (1.2 μsec Sample Time); its output is buffered with a Fet Operational Amplifier. The Positive input, Negative input, and output of the Differential Amplifier are routed off the Board to the output Amplifier to be displayed as the input, data, and noise respectively. The Positive input comes from the Sample and Hold Circuit; the Negative input comes from a Buffer Amplifier, driven by the Vertical DAC. The Noise output serves as the input to the Ramp Generator Board (this is the Signal which is Quantized in the ADC).

CHANGES FOR OLDER BOARDS

Current Series: 852

Older Series: 832

The current board may be used as a direct replacement for the older board. The only difference between these two boards is that C25 was 0.1 μF on Series 832, and is 2.2 μF on Series 852.



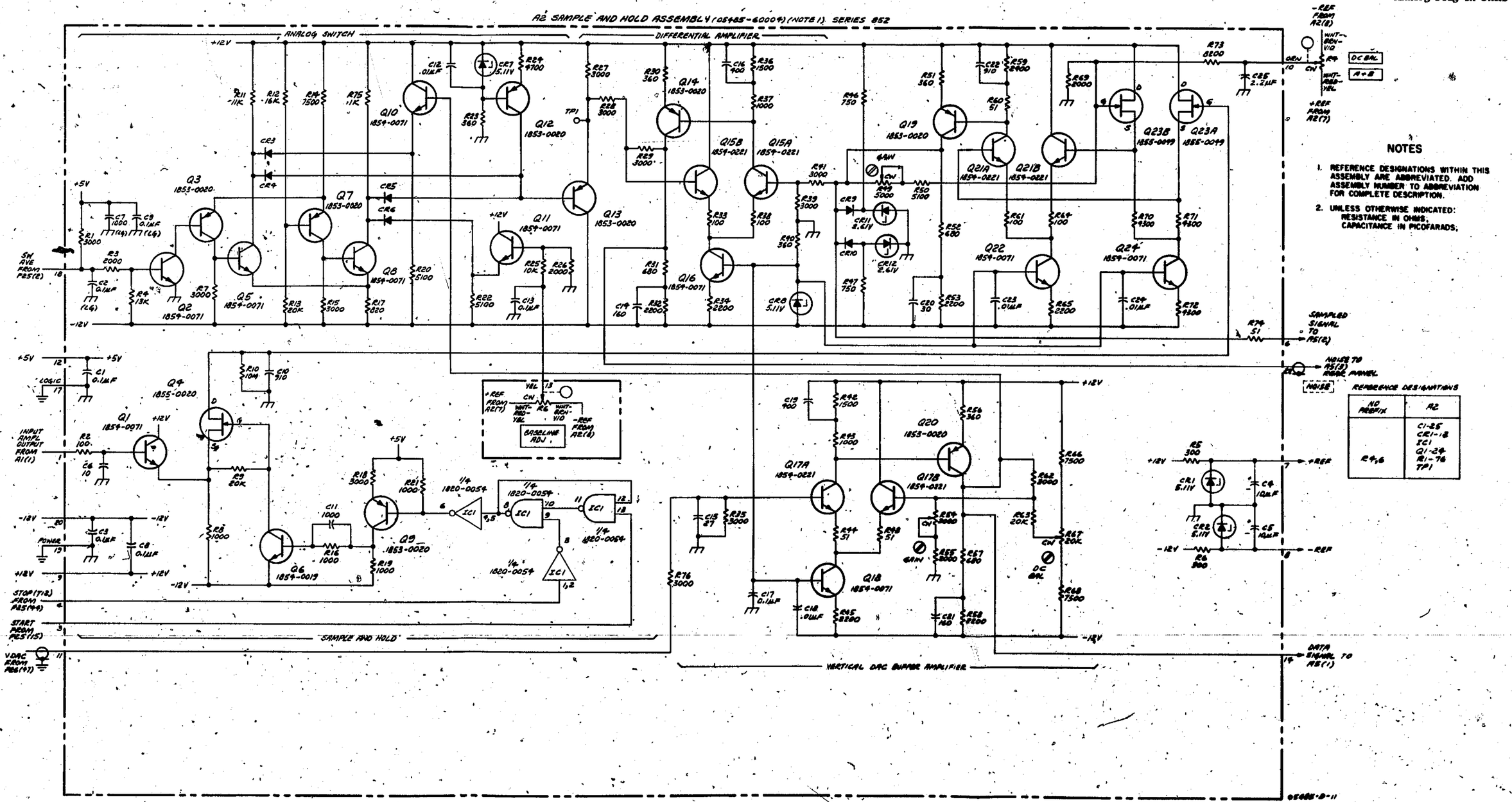


Figure 3-5
A2 Sample and Hold Series 852, 832

A3 ADC BOARD (05485-60003)

LOGIC AND DESCRIPTION

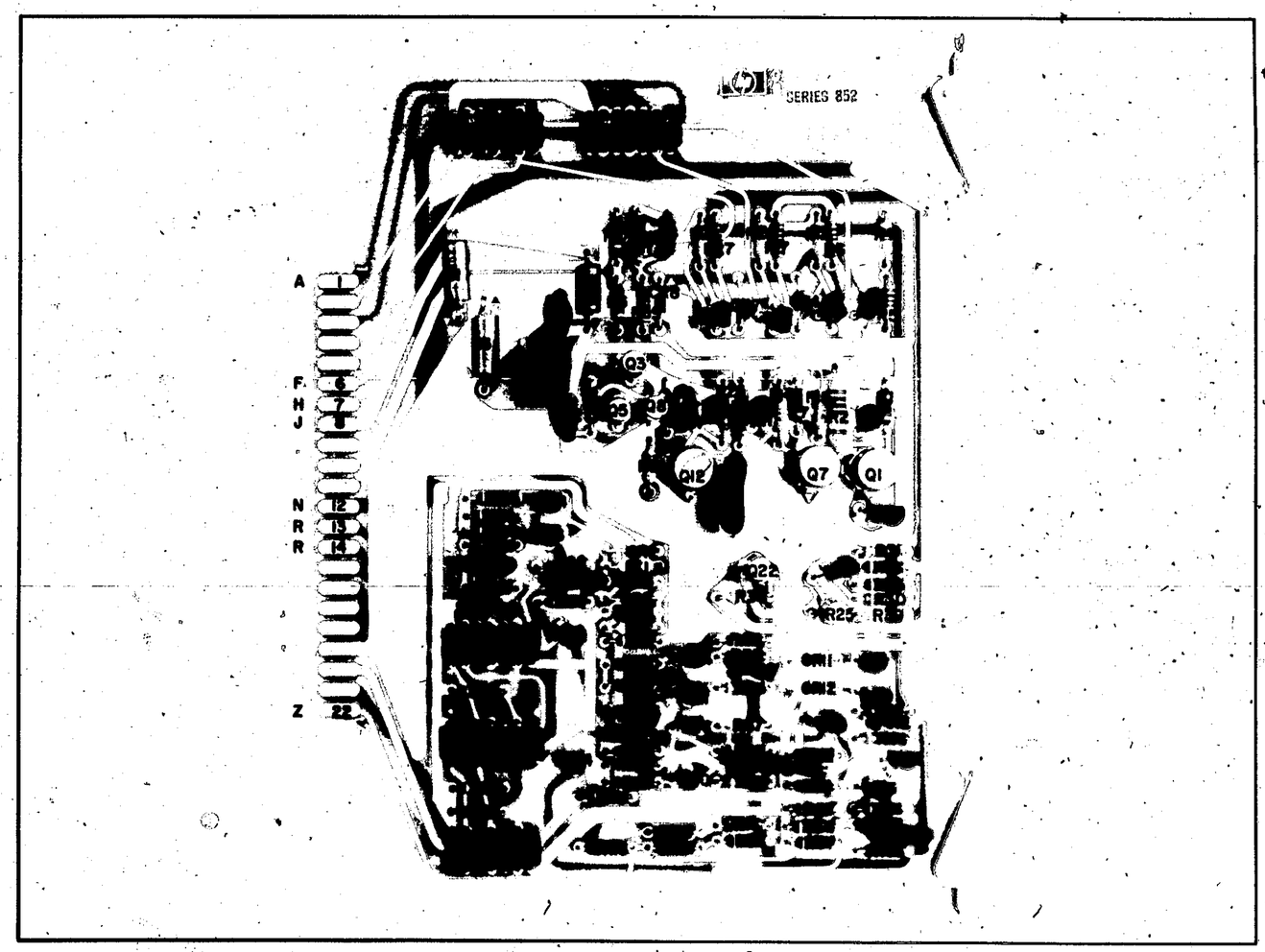
The 05485-60003 Board converts a Bipolar Voltage Amplitude into a count-up or count-down timing pulse whose length is proportional to the Input Amplitude. The Amplitude to time conversion is done by using a Precision Ramp (+5 V to -5 V) whose slope is selectable to give 5, 7, or 9 Bit ADC Resolution. The Ramp is formed by withdrawing a constant current from the Ramp Capacitor through one of these current sinks. The timing pulses are formed by Logic Gating on the outputs of two comparators -- one looking at the Ramp and the signal, and the other looking at the Ramp and Ground.

CHANGES FOR OLDER BOARDS

- Current Board Series: 920

  Older Board Series: 852, 832

  1. The Current board is a direct replacement for either older series board.
  2. C3 on the Series 852 board was a 22 μF, 15 V capacitor. On the Series 920 board, this capacitor is 22 μF, 35 V. Component locator and schematic are same for Series 852 and 920 boards.
  3. Schematic for Series 832 boards is in Figure 3-7.



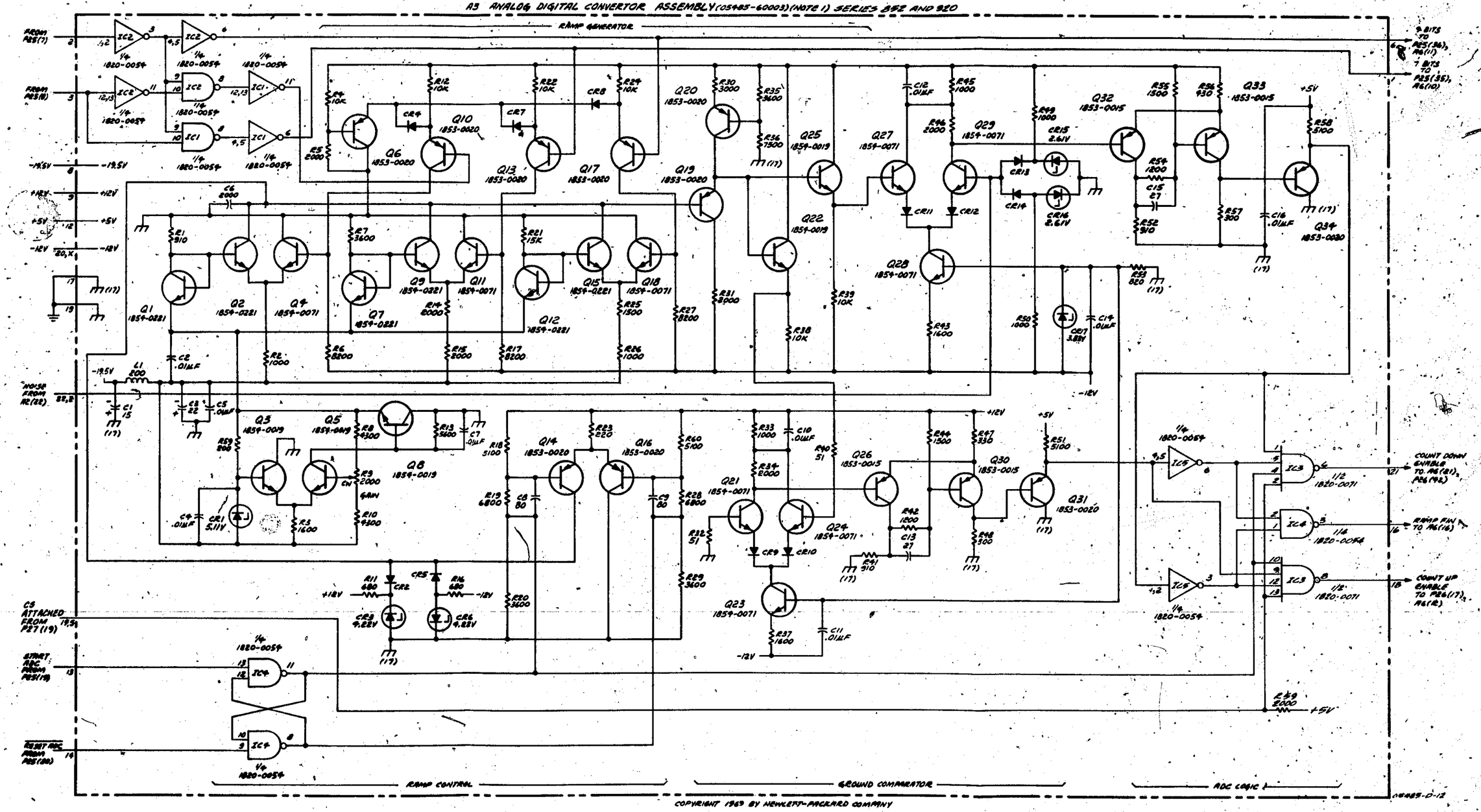


Figure 3-6
A3 ADC Assembly Series 852, 920

See Figure 3-6 for A3 Board description.

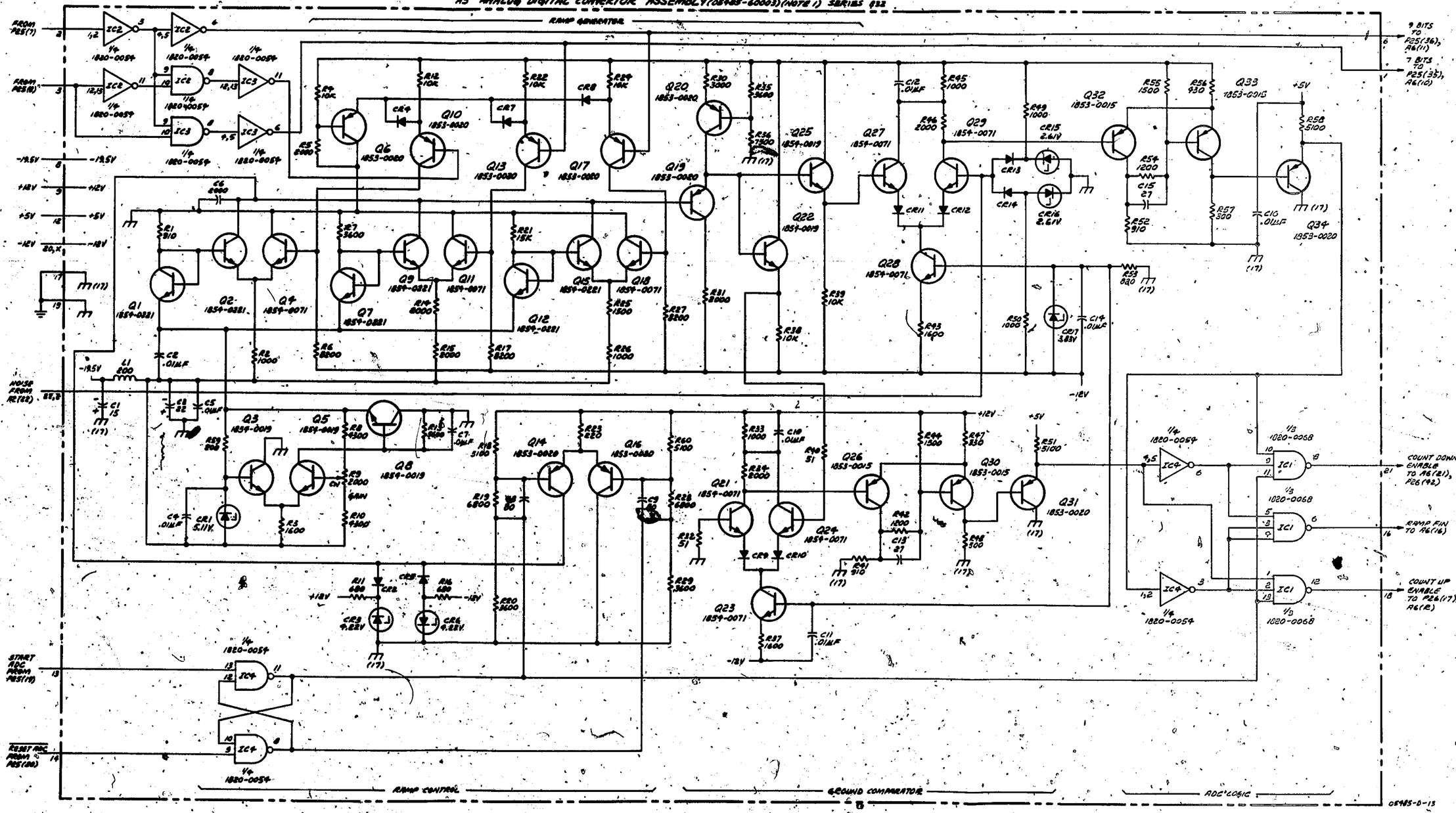


Figure 3-7
A3 ADC Assembly Series 832

A4 SWITCHING LOGIC (05485-60002)

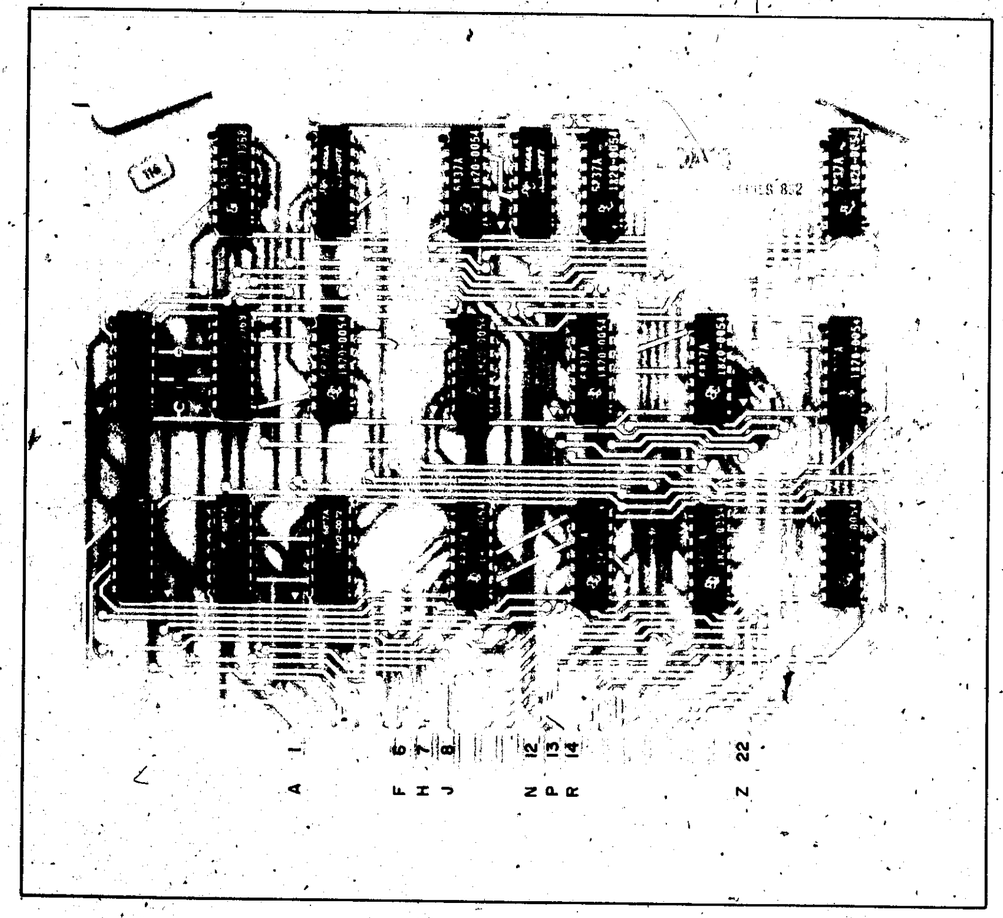
LOGIC AND DESCRIPTION

The 05485-60002 Board decades the Memory Selector Switches on the front panel and the least two significant bits of the Address Register in the 5486A to drive the input and Display Multiplexers on the 05485-60005 and 05485-60001 Boards respectively. Additional output signals like "Display Defeat" and "Channel OK" are sent to the 5486A to alter programs for special case front panel switch settings.

CHANGES FOR OLDER BOARDS

Current Series: 832

Older Series: None



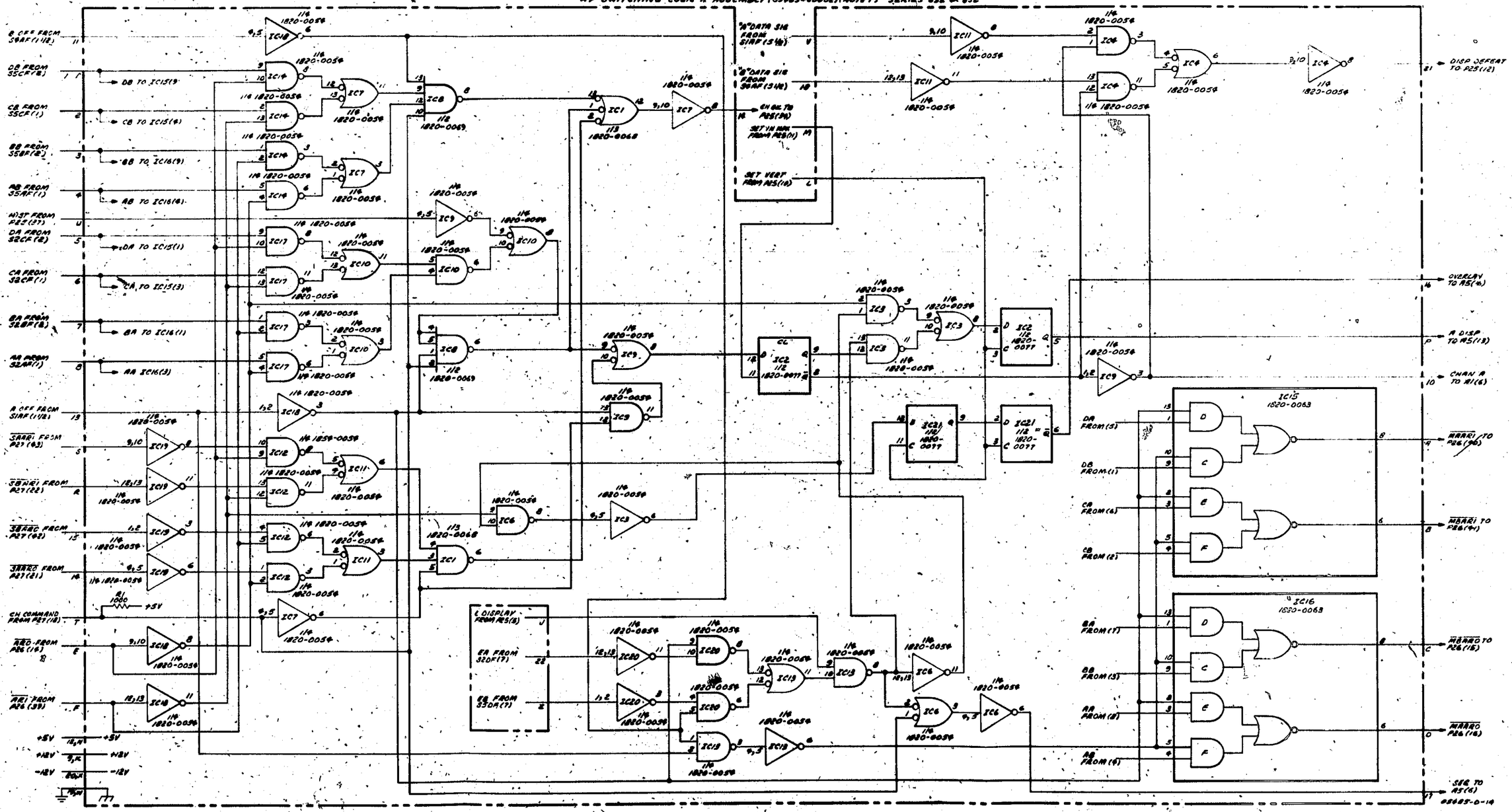


Figure 3-8
A4 Switching Logic A Series 832

A5 OUTPUT AMPLIFIER BOARD (05485-60001)

LOGIC AND DESCRIPTION

The 05485-60001 board is made up of two multiplexing circuits and three amplifiers. The first multiplexer chooses between the input, data, or noise signals. The output of this multiplexer drives both the A and B Channel Amplifiers. These amplifiers have Gain and dc position adjustable from the front panel.

The second multiplexer chooses between the A Amplifier and the B Amplifier, and sends this to the third amplifier or output buffer amplifier. This third amplifier has provision for shifting the output level by one volt, so that four waveforms can be displayed simultaneously on the CRT.

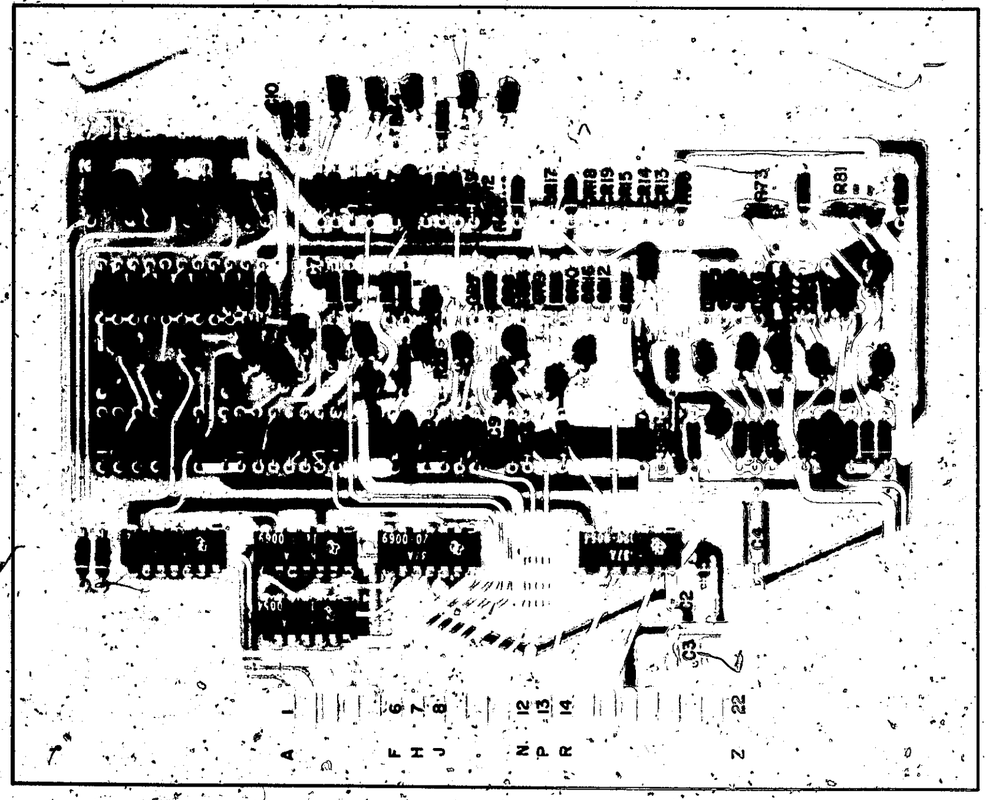
CHANGES FOR OLDER BOARDS

Current Series: 964

This is the board shown in the schematic. Component Locator same as shown in photo.

Older Series: 852, 832

Series 852 is identical to Series 964, except R80 and 5100 ohms. Series 832 is identical to Series 852, except R34 was 10K ohms, and R27 and R42 were 1300 ohms.



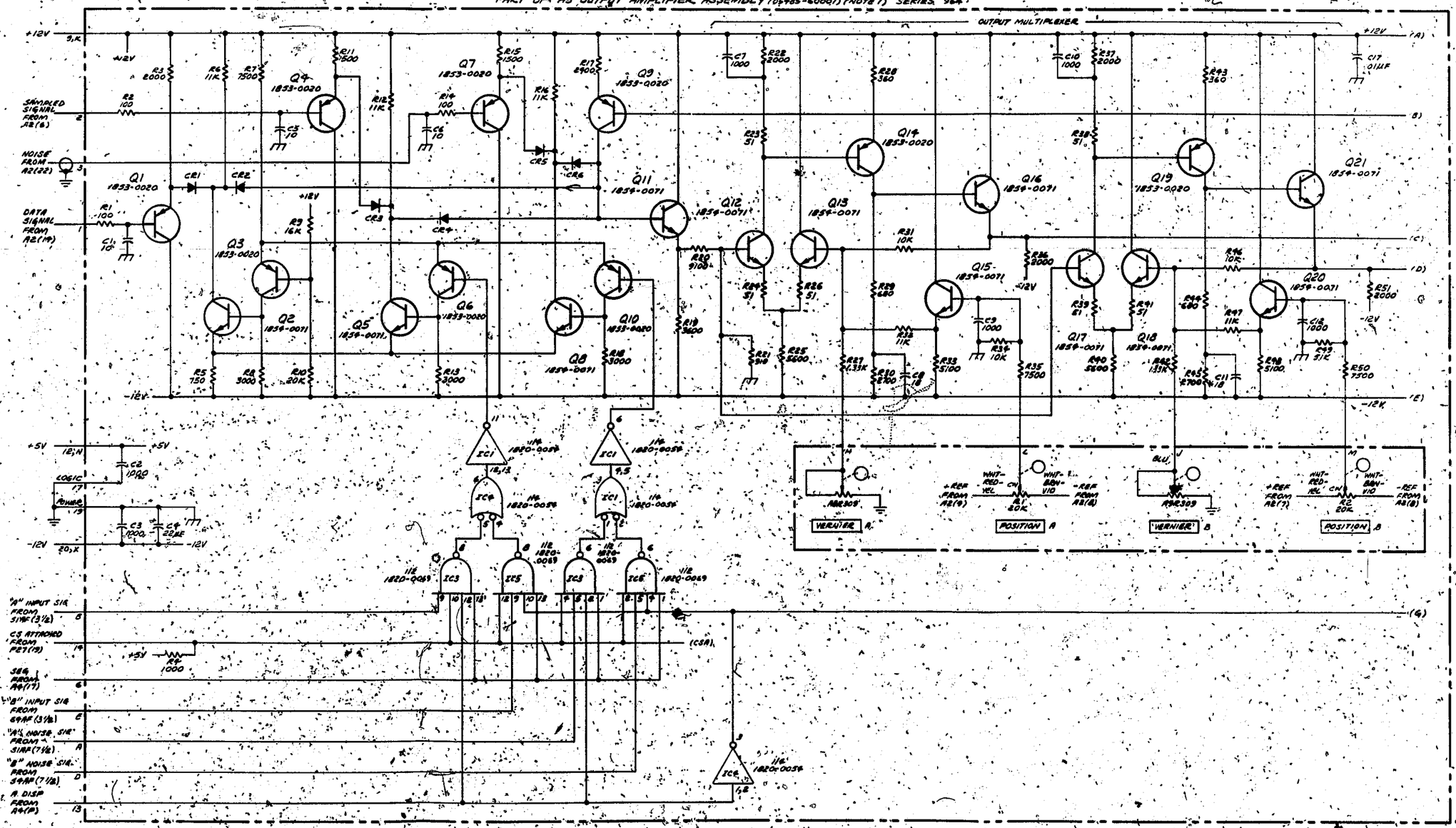
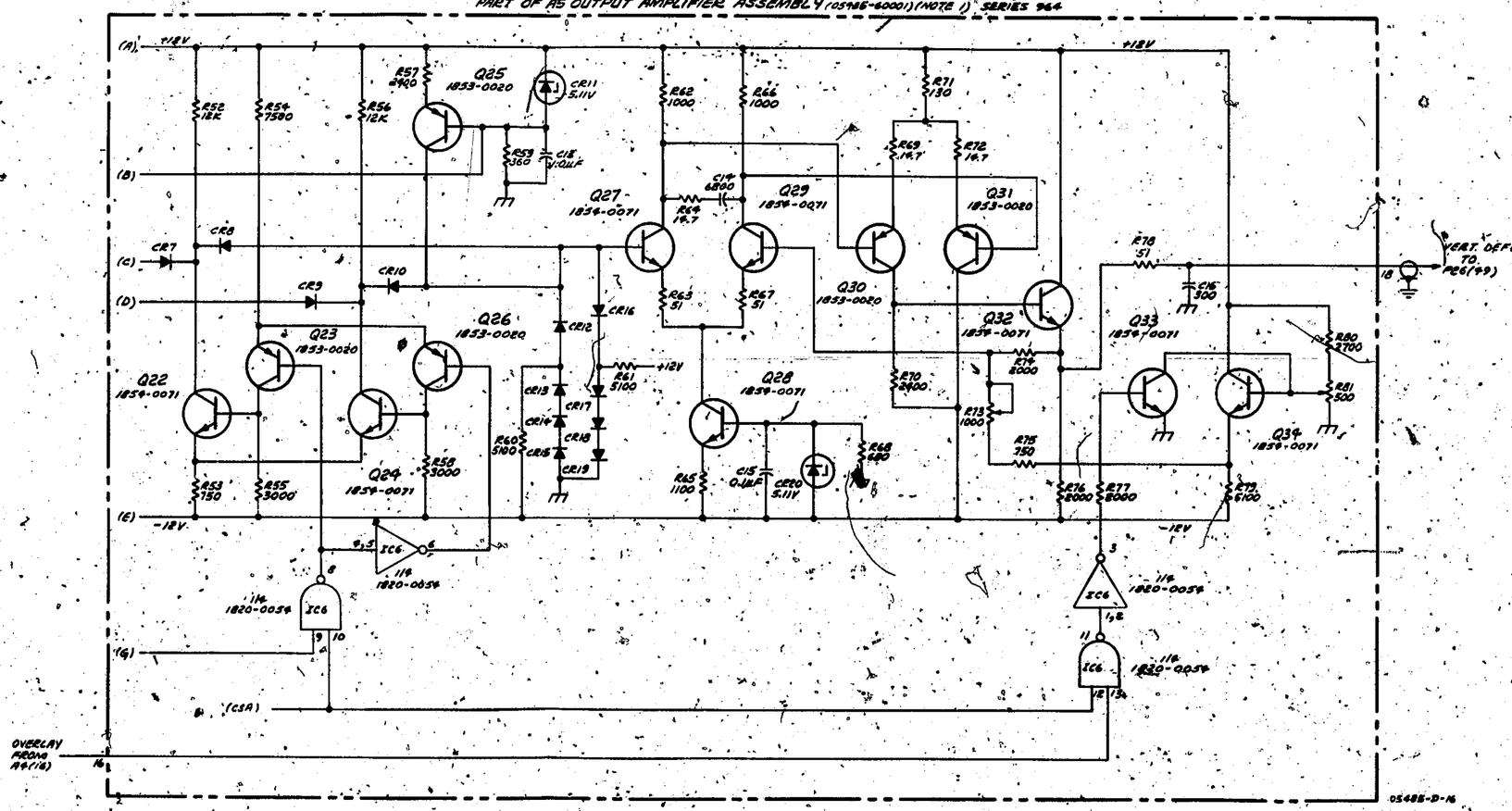


Figure 3-9
A5 Output Amplifier Series 964, 852, 832
(Sheet 1 of 2)

See Sheet 1 of this Figure for A5 Board description and Component Locator.



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS.

REFERENCE DESIGNATIONS

NO PREFIX	A5	A8	A9
-A1,2	C1-17 CR1-20 IC1,3-6 Q1-34 R1-81	R309	R309

NOT ASSIGNED: 1CC

Figure 3-9
A5 Output Amplifier Series 964, 852, 832
(Sheet 2 of 2)

A6 (STANDARD) SWITCHING LOGIC B (05485-60010)

DESCRIPTION

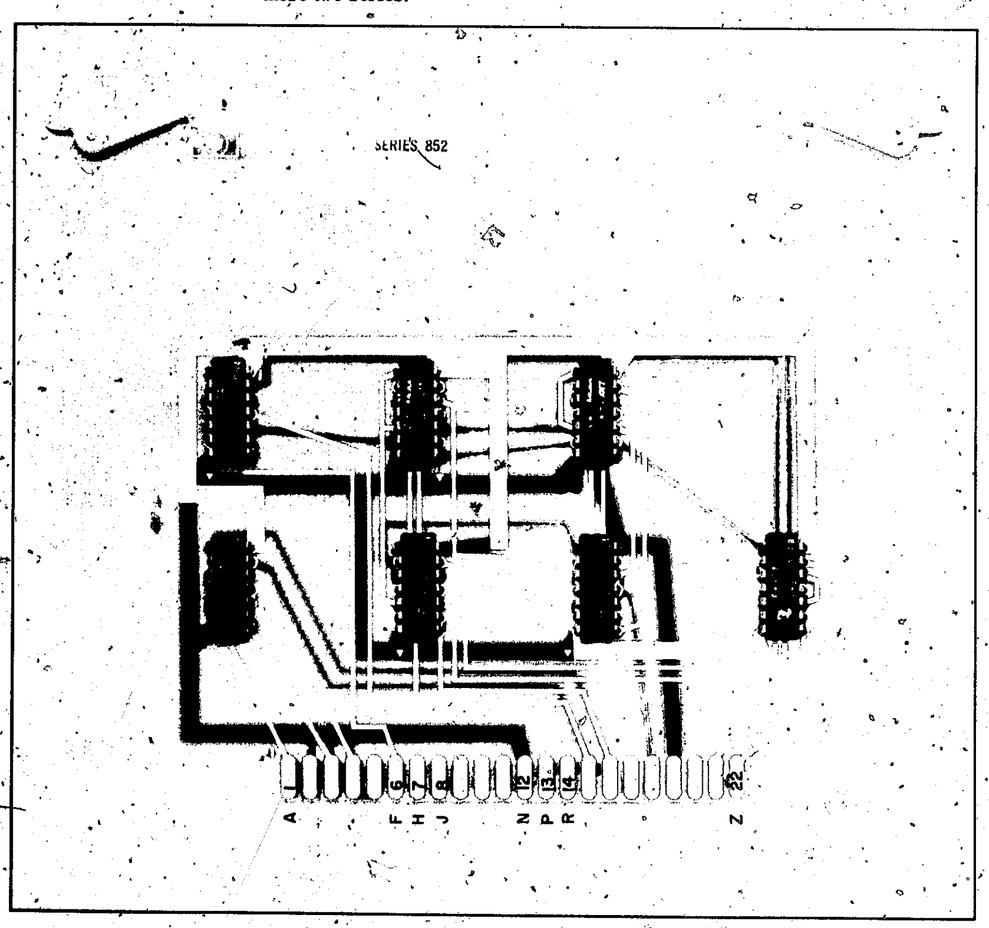
This board decades the Histogram Switch and provides additional timing pulses associated with ADC.. The timing is done synchronously, dividing down from a 10 MHz clock.

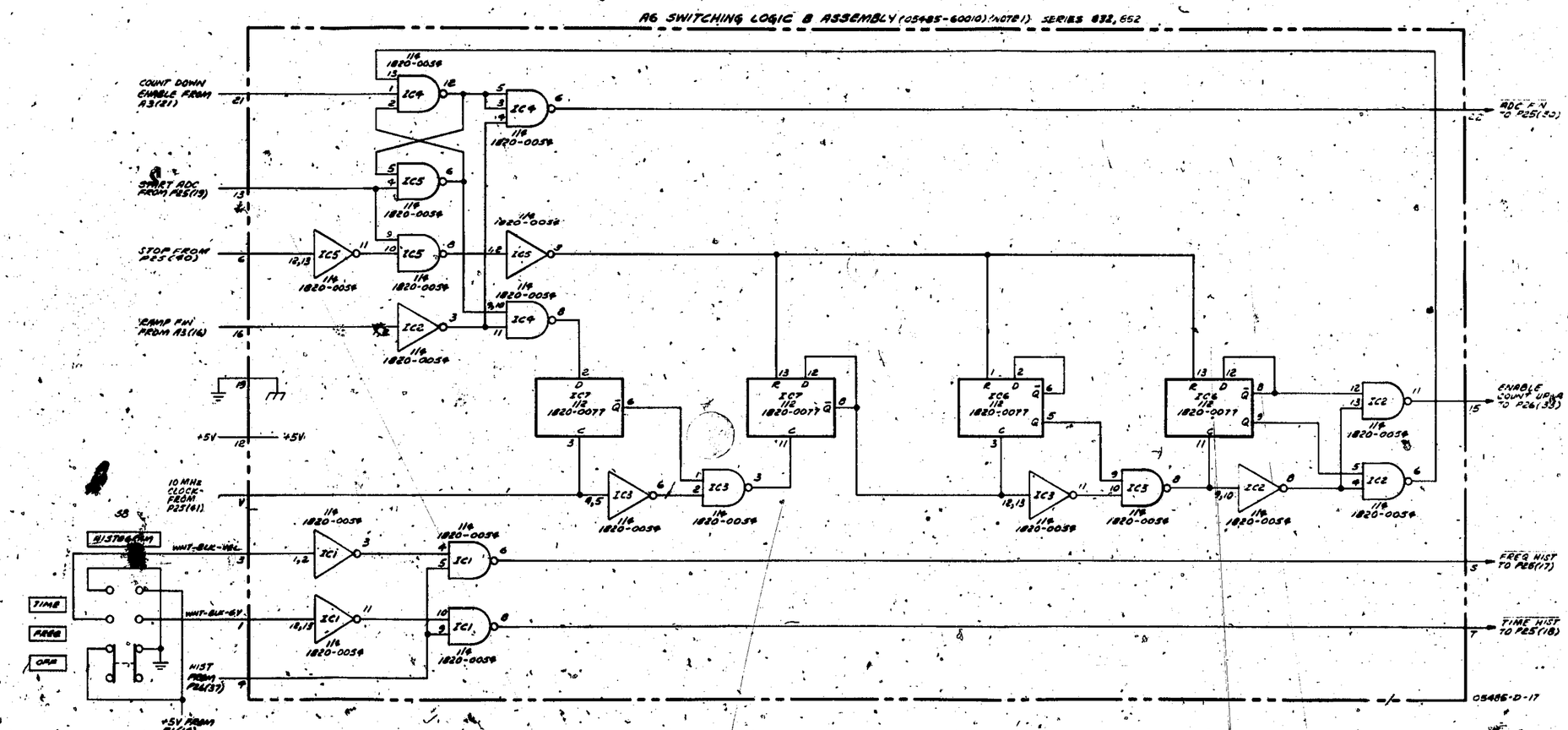
CHANGES FOR OLDER BOARDS

Current Board Series: 852

Older Board Series: 832

The current series may be used as a direct replacement for the older series boards. There is no difference between these two series.





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS;

REFERENCE DESIGNATIONS

W PREFIX	A6
S8	IC1-7

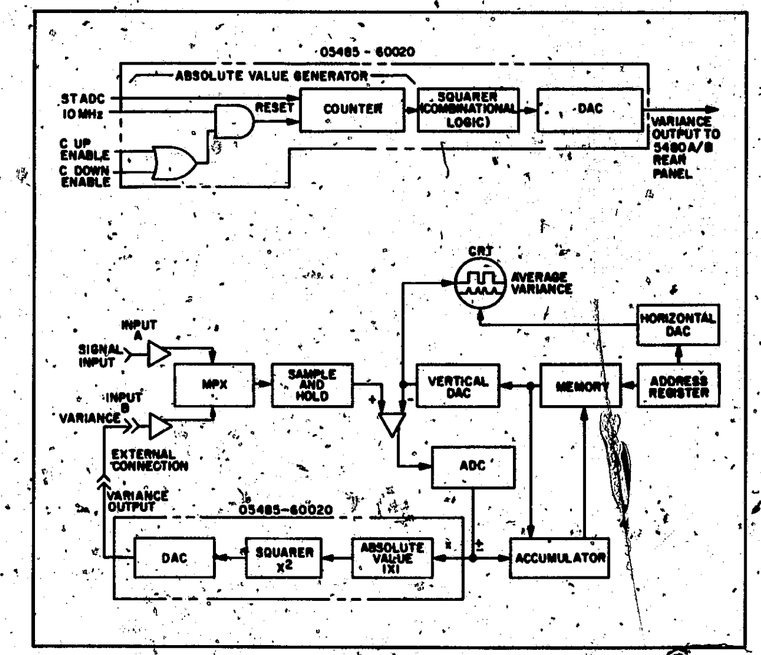
Figure 3-10
A6 Switching Logic B (Standard) Series 852, 832

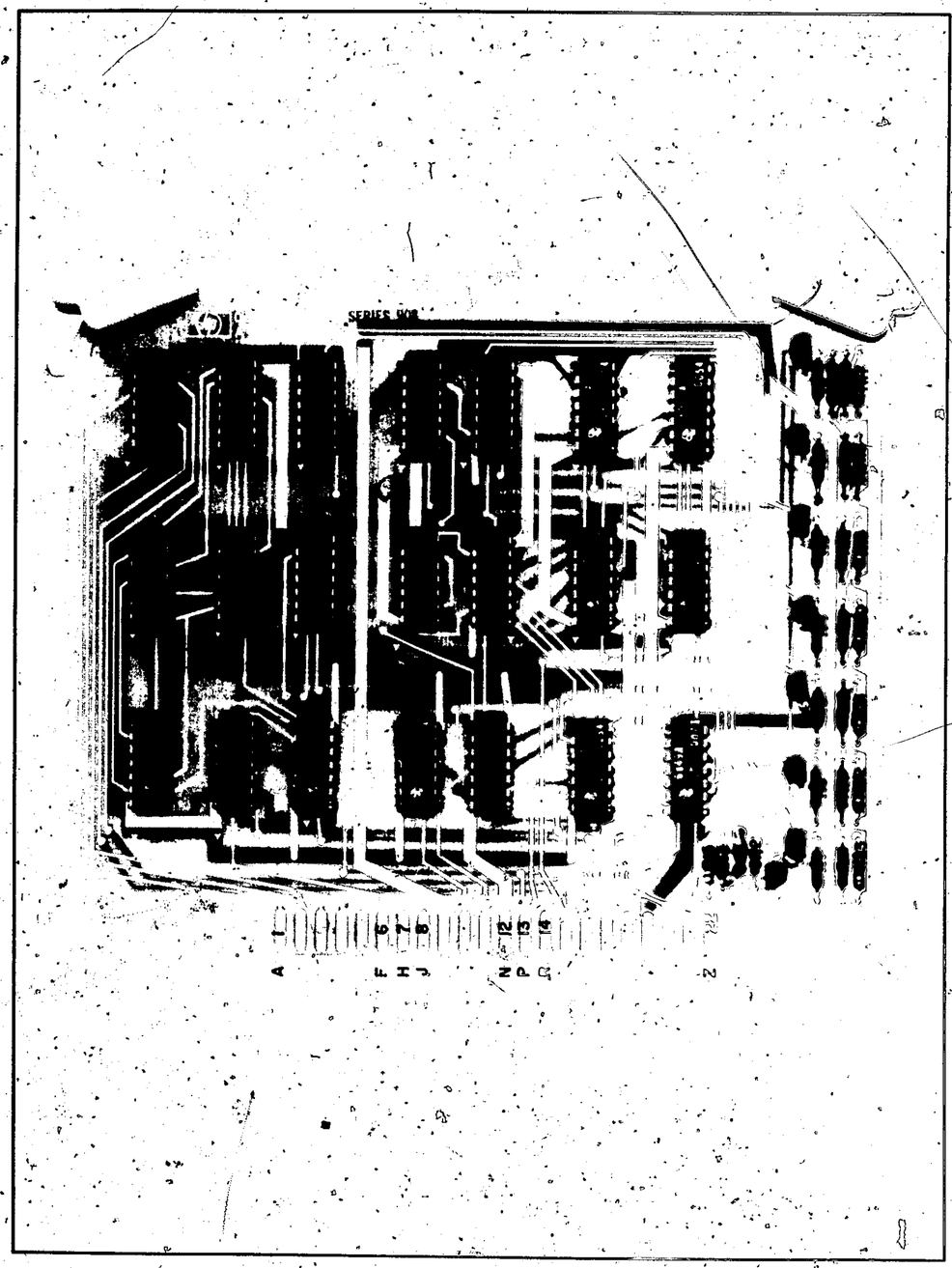
A6 (OPTIONS 01) SWITCHING LOGIC B (05485-60020)

The variance is defined as the average of the square of the deviation from the mean. The variance signal is formed in much the same way as the average signal is. The average signal is formed by splitting the incoming signal into equal time increments and forming the average over successive sweeps of each one of these time increments; each time increment is represented by a dot in the Signal Analyzer display. The variance is formed by comparing each successive input for each of the time increments against the stored average value for the same point, and squaring the difference between them. By time-locking the variance signal to the average signal, points in the variance signal are easily used to identify points in the average waveform where there is additional activity at the input, other than random noise.

The variance is formed by gating a 10 MHz clock signal into the counter in the Absolute Value Generator, using the Count-Up Enable or Count-Down Enable signal from the ADC as the gate control. When the Signal Analyzer is averaging, as it must be doing, to use the Variance Option, the ADC digitizes the difference between the analog input signal and the anlog value of the average, which is stored in memory. Thus, the counter in the Absolute Value Generator contains a count which is proportional to the magnitude of the difference signal, but which is without any sign (polarity) information. The output of the Absolute Value Generator is squared, digitally, then converted into an analog signal, using an 8-bit Digital-to-Analog Converter (DAC). The DAC output is the signal that appears at the 5480A/B rear-panel VARIANCE OUTPUT connector. The Variance Output signal contains noise, and must be averaged to yield meaningful results.

If the Signal Analyzer is operating in the SUMMATION FUNCTION, the Variance Output signal is not the variance of the input signal, it is, instead, the square of the input signal. This property is useful in verifying that the variance is operating properly. If a triangular wave is put into one input while the 5480A/B is summing (instead of averaging), the Variance Output Signal, averaged on another channel, should be a repetitive paraboloid of twice the input signal frequency. Peaks of the paraboloid will be of uniform amplitude only if BASELINE ADJUST has been adjusted to be at the center of the triangular input waveform.





A6 SWITCHING LOGIC B ASSEMBLY (05485-60020) (NOTE 1) OPTION 01 SERIES 908

NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS;

REFERENCE DESIGNATIONS

A6 OPTION 01
C1
CR1,2
IC1-21
Q1-8
R1-23

START RAMP FROM A25(19)
7 BITS FROM A3(1)
9 BITS FROM A3(6)
10 MHz FROM A25(61)
↑ UP ENABLE FROM A3(18)
↓ DOWN ENABLE FROM A3(21)
STOP FROM A25(60)
RAMP FIN FROM A3(16)
MIST FROM A26(37)
SH FREQ FROM SB
SH TIME FROM SB

VARIANCE OUTPUT TO A22(46)
ENABLE COUNT UP TO A26(39)
ROC FIN TO A25(20)
N FREQ TO A25(17)
N TIME TO A25(18)

05485-0-16

Figure 3-11
A6 Switching Logic B (Option 01) Series 908