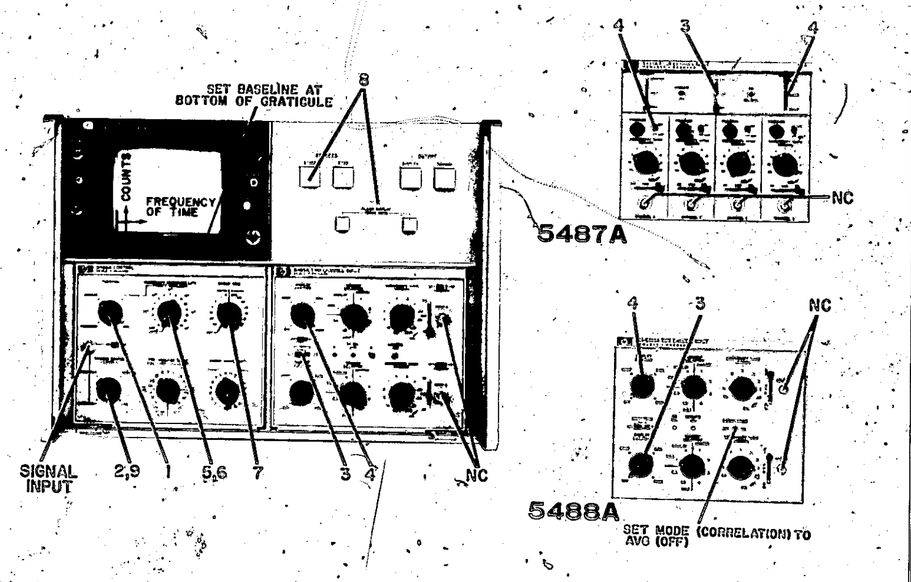
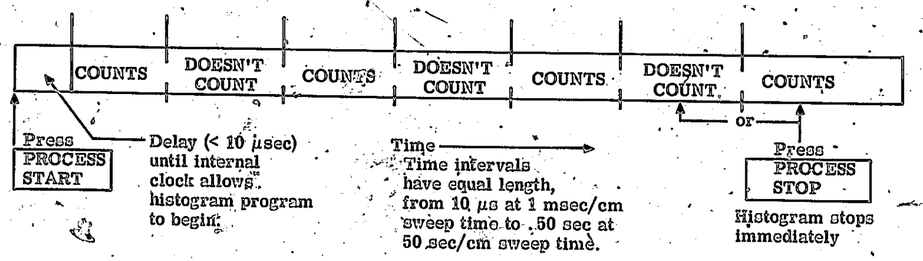
Figure 1-13. Histograms



DESCRIPTION: Analyzer displays a probability-versus-frequency (or time interval) plot. Number of incoming pulses during a set gate time determines memory location into which a count is placed. After several gate times, a distribution results.

In FREQ or TIME HISTOGRAMS, the 5480A/B accumulates histogram counts during alternate time periods, as shown in the two examples below.

FREQ HISTOGRAMS



Number of counts received at SYNC connector determines address which is incremented.

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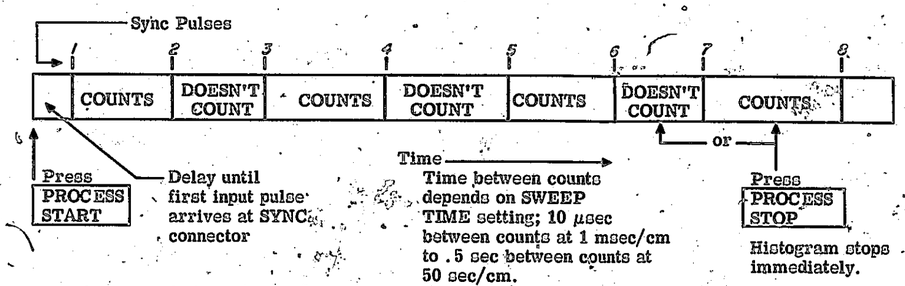
Figure 1-13. Histograms (Cont'd)

DESCRIPTION (Cont'd):

TIME HISTOGRAMS



Number of counts accumulated between two SYNC pulses determines which address is incremented.

Perform SETUP and TURN-ON procedure described in Figure 1-8.

CONTROL SETTINGS

1. FUNCTION to HISTOGRAM
2. TRIGGER SOURCE to either EXTERNAL position.
3. HISTOGRAM to: FREQ for input signals between 1 kHz and 1 MHz TIME for input signals below 1 kHz.
4. One Channel to DISPLAY DATA
5. MEMORY SELECTOR:

   5465A or 5468A: Use CHANNEL A MEMORY SELECTOR to select one QUARTER, the HALF or FULL memory for processing. NOTE: If A DISPLAY is OFF, use B MEMORY SELECTOR as above.

   5467A processes in FULL memory only, MEMORY switch has no effect in HISTOGRAM.
6. SENSITIVITY MULTIPLIER to 15.
7. PRESET TOTALIZER to OFF, or to number of events to be accumulated.
8. SWEEP TIME to 2 msec/cm.
9. Press both CLEAR DISPLAY buttons, then PROCESS START.
10. Adjust TRIGGER LEVEL, if necessary, to enable triggering.

CRT DISPLAY

SWEEP TIME may be adjusted for best display.

Horizontal baseline calibration is as follows:

For TIME HISTOGRAMS, read calibration directly from SWEEP TIME setting. Max Time Interval is 10 times SWEEP TIME, or overflow will occur, causing erroneous reading.

Figure 1-13. Histograms (Cont'd)

CRT DISPLAY (Cont'd)

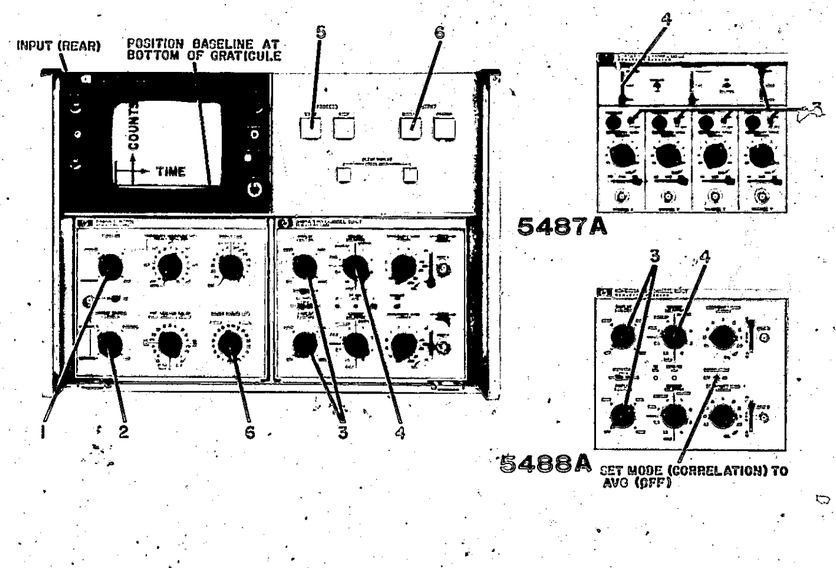
For FREQ HISTOGRAMS, convert SWEEP TIME to frequency/cm, using chart below:

SWEEP TIME SETTING	DISPLAY CALIBRATION	MAX INPUT FREQUENCY	USABLE HORIZ RANGE
1 msec/cm	10 MHz/cm	1 MHz	0.1 cm
2 msec/cm	5 MHz/cm	1 MHz	0.2 cm
5 msec/cm	2 MHz/cm	1 MHz	0.5 cm
10 msec/cm	1 MHz/cm	1 MHz	1.0 cm
20 msec/cm	500 kHz/cm	1 MHz	2.0 cm
50 msec/cm	200 kHz/cm	1 MHz	5.0 cm
100 msec/cm	100 kHz/cm	1 MHz*	10.0 cm
200 msec/cm	50 kHz/cm	500 kHz*	10.0 cm
5 sec/cm	20 kHz/cm	200 kHz*	10.0 cm
1 sec/cm	10 kHz/cm	100 kHz*	10.0 cm
2 sec/cm	5 kHz/cm	50 kHz*	10.0 cm
5 sec/cm	2 kHz/cm	20 kHz*	10.0 cm
10 sec/cm	1 kHz/cm**	10 kHz*	10.0 cm

* Maximum frequency that can be displayed, without overflow
** For frequencies below 1 kHz, use TIME HISTOGRAM mode.

Overflow occurs when the process address register in the 5480A/B accumulates more than 1024 counts during either FREQ or TIME HISTOGRAM processing. When more than 1024 counts have been accumulated, the process address register automatically returns to address 0000 and continues counting; at the end of processing, address x (which really should be 1024 + x) is incremented (causing an error in the display). Overflow problem is eliminated by proper setting of SWEEP TIME control.

Figure 1-14. MCS (Multichannel Scaling)



DESCRIPTION: Analyzer displays a plot of frequency-versus-time. Analyzer sweeps through its memory, remaining at each location for a set gate time. Number of counts placed in each location is determined by number of input pulses during gate time for that location.

Perform SETUP and TURN-ON procedure described in Figure 1-8.

CONTROL SETTINGS

1. FUNCTION to MCS
2. TRIGGER SOURCE as desired.
3. DISPLAY to DATA (Channel A), all other channels OFF
4. 5480B System: MEMORY SELECTOR as desired
   If system contains 5487A, refer to Figure 1-6 for memory allocations.

   5480A System: MEMORY SELECTOR A to FULL.
   If system contains 5487A, set A ON/OFF to ON, all others to OFF.

Figure 1-14. MCS (Multichannel Scaling) (Cont'd)

CONTROL SETTINGS (Cont'd)

5. Press PROCESS START button.
6. After desired processing interval, press OUTPUT DISPLAY button. 5480B/5486B only: if desired, set SWEEP NUMBER to number of sweeps desired (2^N), and PRESET/NORMAL to PRESET. 5480B system will perform preset number of MCS processing sweeps and stop automatically, displaying result on CRT.

   NOTE: (5480A only) If PROCESS STOP is pressed, memory contents of point being processed are lost (cleared); and this point will appear as "0" on display.

CRT DISPLAY

During MCS processing, CRT display is only a dot moving across screen at rate determined by SWEEP TIME control. When OUTPUT DISPLAY is pressed, processing continues until end of sweep, then display appears.

Display represents number of counts received at each horizontal position as memory is stepped through all 1000 points. There are no "holes" in processing when 5480B/5486B MEMORY SELECTOR switch is set to process in QUARTER or HALF of MEMORY; the memory sections addressed are addressed for a longer period than they would be during FULL memory processing, each memory point accumulating the total number of counts as would have been placed in all the points it is replacing.

If MCS display is not satisfactory, try a different SWEEP TIME setting. Be sure to clear display after changing SWEEP TIME.

Vertical display is not calibrated, however number of counts in any one channel can be calculated using the information presented below, when OUTPUT DISPLAY button is lighted.

SENSITIVITY MULTIPLIER SETTING	MCS CALIBRATION (COUNTS/CM ON VERTICAL AXIS)
15	31
14	61
13	122
12	244
11	488
10	976
9	1,953
8	3,906
7	7,813
6	15,625
5	31,250
4	62,500
3	125,000
2	250,000
1	500,000
0	1,000,000

Horizontal display is calibrated by SWEEP TIME. Either the HORIZ DAC or SWEEP VOLTAGE output (available at rear-panel connectors) may be used to control MCS input source, to relate input signal frequency to horizontal channel being scaled, instead of the more usual time variation.

THEORY

SECTION II

PRINCIPLES OF OPERATION

2-1. INTRODUCTION.

2-2. General.

2-3. The 5480A/B Signal Analyzer is an oscilloscope using computer-type hardware and digital signal processing techniques to improve the signal to noise ratio of repetitive signals up to 60 dB. A knowledge of computer and oscilloscope circuits and techniques is helpful (but not required) for servicing this system. This manual provides general information required for servicing the system. More detailed explanations of operating principles for parts of the system are given in other volumes of the system service manual.

2-4. Display

2-5. The Display Section of the Memory/Display unit uses the high voltage power supply for the HP Model 1200 A/AR Oscilloscope. Note that the CRT is covered by a warranty separate from the rest of the instrument. This warranty and a warranty claim form are given in the operating manual and in Volume II of the service manual. The Display Section vertical and horizontal amplifiers are designed for this signal analyzer. INTENSITY, FOCUS, HORIZONTAL POSITION and (horizontal) MAGNIFIER controls are located in the vicinity of the CRT. The vertical POSITION and SENSITIVITY controls are located on the analog plug-in unit, which mounts in the lower right-hand corner of the Memory/Display unit. Refer to Section I of this manual for a description of all controls.

2-6. Data Processing Circuits

2-7. All data processing in the Signal Analyzer is done by a special-purpose computer circuit, using one or more of seven hard-wired (built-in) programs.

2-8. Data processing circuits are described in Tables 2-1 through 2-9.

2-9. Data processing and display programs are described in Tables 2-10 through 2-18.

2-10. Data processing and display functions are described in Tables 2-19 through 2-24.

Table 2-1. Major Circuit Sections

A1: DISPLAY SECTION

Location:

Upper left front corner of 5480A/B Memory/Display unit.

Function:

This section contains the CRT and its power supply and amplifier circuits. Normal inputs are the Vertical and Horizontal DAC outputs from the Memory Section (A2). Horizontal input is an analog voltage corresponding to the number in the Horizontal (Address) Hold Register. Vertical input is an analog voltage corresponding to Accumulator (memory) contents at that address (after any display scaling operations have been performed, see Table 2-9). Vertical inputs may also be sampled input or difference between sampled input and Vertical DAC output.

A2: MEMORY SECTION

Location:

On swing-out deck at upper right side of 5480A/B.

Function:

This section contains a 1024 word x 24 bits-per-word magnetic core memory stack, and its associated power supply, timing, and driving (read, write, sense, and inhibit) circuits, and the Vertical and Horizontal DACs (digital-to-analog converters) that convert the Accumulator and AR output (digital) to analog for the display section.

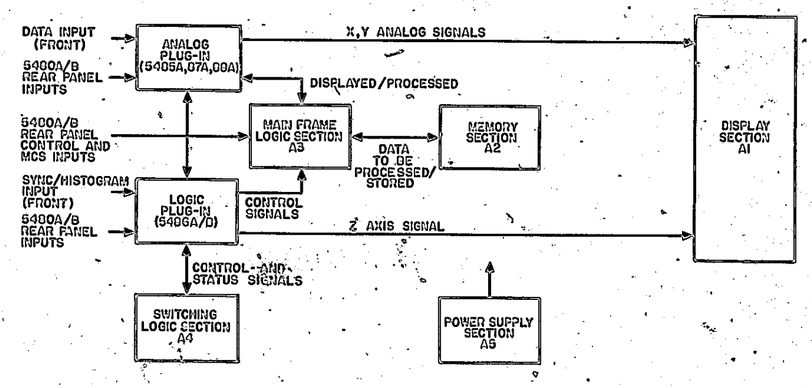


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Table 2-1. Major Circuit Sections (Cont'd)

A3: MAIN FRAME LOGIC SECTION

Location:

Lower left rear corner of 5480A/B Memory/Display unit.

Function:

This section contains the Address Register and Accumulator (register) circuits, and their control circuits and preset detector. There are two address registers (display, which is incremented at the rate of 100,000 points/sec--except for processing time points per second, and Process, which is incremented at a rate determined by the SWEEP TIME switch in the Logic plug-in), and a multiplex circuit which selects which address register output will be outputted to the Horizontal (Address) Hold Register. The Horizontal Hold Register drives the Read/Write Generators and the Decoder Gates in the Memory Section to address a given memory location of 24 cores. The Accumulator can manipulate data and serves as input/output buffer for Memory contents, working through the Sense Amplifiers and Inhibit Generators in the Memory Section.

A4: SWITCHING LOGIC SECTION

Location:

Upper right front corner of 5480A/B Memory/Display unit.

Function:

This section contains only one circuit assembly, the Light Driver and two four-output "flip-flop" circuits. One flip-flop circuit provides an output indicating which PROCESS or OUTPUT switch was pressed and released last. Another similar flip-flop controls the lights in these buttons. The RESET light driver is on this board. If the Memory section ±19.5V supplies fail, or if there is a momentary interruption of ac power, the RESET lamp will light; Memory contents are protected, but there is no processing until you can turn the lamp off (see Section IV of this Manual). (This is accomplished by turning power switch of the 5480A/B off and then on again.)

A5: POWER SUPPLY SECTION

Location:

Lower right rear corner of 5480A/B Memory/Display unit.

Function:

This section is the main power supply for the 5480A/B Signal Analyzer system, including plug-ins. All power supplies except the temperature-compensated ±19.5V supply (in the Memory Section) and the CRT High-voltage supply (in the Display Section) are located here.

API: ANALOG PLUG-IN

Location:

Lower right front corner of 5480A/B Memory/Display unit.

Function:

The analog plug-in accepts analog input signals and converts them to digital form for processing and storage in the Memory/Display unit. Additional functions include control of vertical display source, position, and size; control of signal routing to one or more quarters of memory; and interfacing between Signal Analyzer circuits and Memory/Display unit rear-panel connectors.

Table 2-1. Major Circuit Sections (Cont'd)

LPI: LOGIC PLUG-IN

Location:

Lower left front corner of 5480A/B Memory/Display unit.

Function:

This plug-in contains the time base circuits for the Display and Process sweeps, it accepts and/or generates the signals necessary to trigger processing, provides program control for the Signal Analyzer system, keeps track of sweep number, and provides scaling of the vertical display.

Table 2-2. Display Section (A1)

The Display Section provides the normal visual output for the Signal Analyzer.

The Display Section contains the calibrator circuit, which produces a 1V p-p square wave output for checking vertical calibration. The CALIBRATOR frequency is controlled by the SWEEP TIME switch through the Process Address Register. The CALIBRATOR output is available only when the PROCESS START button is lighted; under any other condition the output will be either 0V or +1V, depending on calibrator output level when processing was stopped. Because the CALIBRATOR frequency changes as the SWEEP TIME switch setting is changed, the number of cycles displayed on the 5480A/B CRT is the same, regardless of setting; if the CALIBRATOR is connected through an AC coupled input, it will become differentiated as sweep time is decreased.

Inputs to this section are the outputs of the Vertical and Horizontal Digital-to-Analog converters, located in the Memory Section (see Table 2-3). The signal path between these sections is through the Analog plug-in (see Table 2-1).

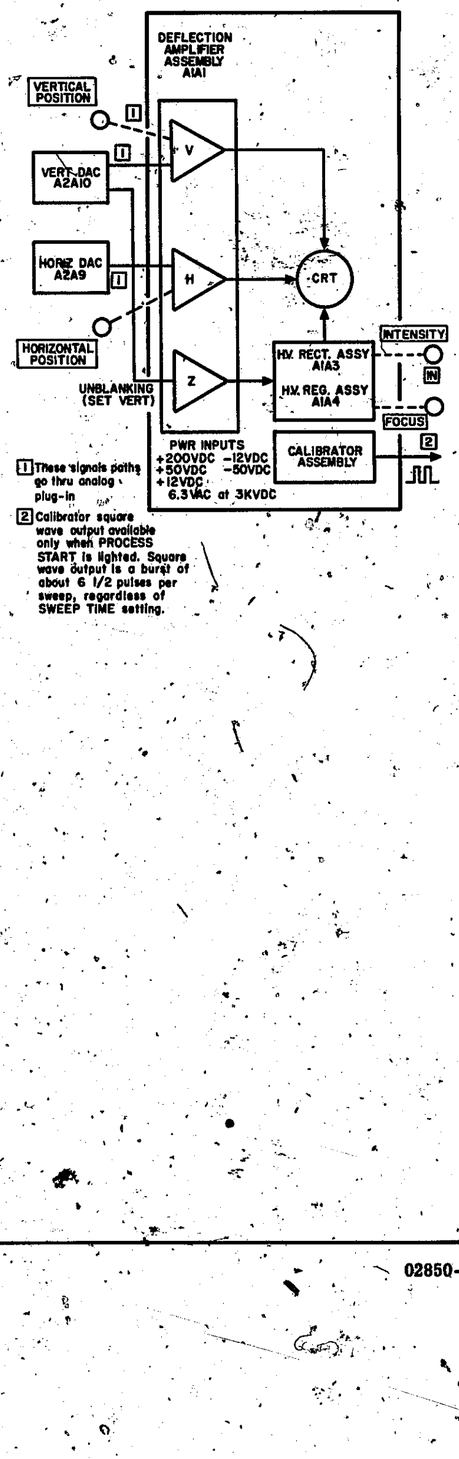


Table 2-3. Memory and Main Frame Logic Sections (A2, A3)

The Memory Section (A2) and Main Frame Logic Section (A3) are interdependent.

All data inputs to, or outputs from, the magnetic core Memory stack in the Memory Section are through the Accumulator register in the Main Frame Logic Section.

The Memory Section contains the magnetic core Memory stack and its associated read/write, decoder gate, sense amplifier, inhibit generator, memory sectioning, timing, temperature-compensated power supply, and digital-to-analog converter (DAC) circuits.

The Main Frame Logic Section contains general purpose registers for input/output operations with the Memory section, and for data processing. These registers are the Accumulator, the Process Address Register, and the Display Address Register and control boards for these registers.

Descriptions of each major circuit are given in the following figures. Refer also to the figures in this section that describe the operating programs.

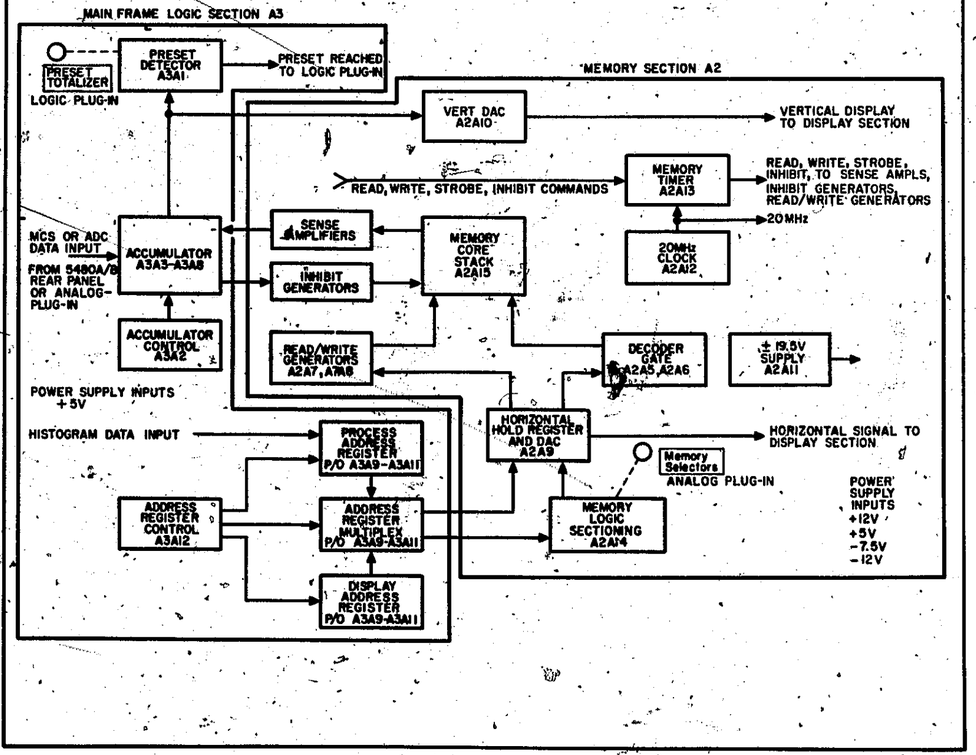
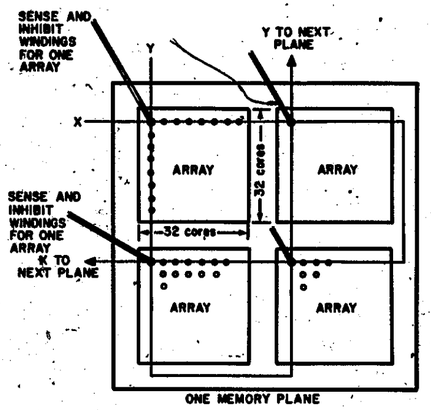


Table 2-4. Memory Core Stack (A2A15)

The Memory Core Stack contains 24576 ferrite cores arranged as shown below to enable storage of 1024 24-bit words.

Except for the cover plates and a board on which connections with other circuits are made, the Memory Core Stack consists of three boards. Each board has two planes (top and bottom) on which the cores are mounted. On each plane, the ferrite cores are arranged in four 32 x 32 core arrays. Each array represents one bit in a word. There are 24 arrays.



Four wires are threaded through the center of every memory core. These are:

X address line: runs through 32 cores in each array. There are 32 "X" address lines.

Y address line: runs through 32 cores in each array. There are 32 "Y" address lines.

Note that in each array there is only one core at which a given X address line and Y address line intersect. The 24 cores in memory (one in each array) where a given X and Y address lines intersect are the ones in which the addressed word is written or read.

Sense line: runs through all cores in one array. There are 24 sense lines.

Inhibit line: runs through all cores in one array. There are 24 inhibit lines.

Table 2-5. Read, Write, Sense, Inhibit

DATA STORAGE

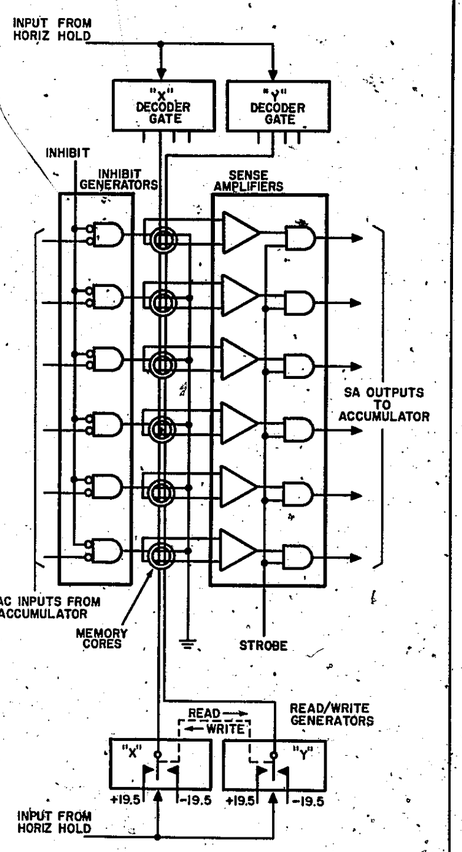
In the Signal Analyzer, all data are converted to binary digital form and processed and stored in that form. The ferrite cores in the Memory Core Stack are made of a material which can be magnetized in a clockwise or counterclockwise direction, corresponding to a "1" or a "0" in binary notation. The direction of core magnetization is changed by changing the direction of the (addressing) current through the core. Since the mass of each core is small, little magnetizing force is required to switch between binary states. The core maintains its magnetized state indefinitely after the magnetizing current ends, so pulses can be used to change states. The main difference between "reading" and "writing" is the direction of currents on the address lines.

SENSE AMPLIFIERS

There is one sense amplifier for each of the 24 core arrays in the Signal Analyzer Memory Core Stack; the assumption is made that since only one core in each array is addressed at any one time, any activity in that array must be associated with the addressed core.

Each Sense Amplifier is a differential amplifier that provides an output during the READ TIME, if any core in its array changes state. A "read" current writes "0" in all cores of the addressed location in the Memory Core Stack. Any core that had previously been magnetized in the "1" direction changes state, producing an output current pulse that is sensed by the Sense Amplifier for that core's array. Any core that had previously been magnetized in the "0" direction remains at "0," producing no output.

Because the output pulse produced by a core changing state is very small, a STROBE signal is used to "turn on" the Sense Amplifiers only during the time when a pulse can be expected to appear (this occurs at the middle of the READ TIME pulse).



INHIBIT GENERATORS

There is one Inhibit Generator for each of the 24 core arrays in the Signal Analyzer Memory Core Stack; the assumption is made that since only one core in each array is addressed at any one time, any writing that would occur in that array must take place at the addressed core.

A "write" current writes "1" in all cores of the addressed location in the Memory Core Stack. To get a meaningful word (one that is not necessarily all "1's") stored in memory, the bits that are to remain "0" are inhibited. If any core is to store a "0," the Inhibit Generator for the array containing that core is turned on, causing a current equal to -1/2 the "write" current to pass through all cores in the array. In the addressed core, this current "bucks" the "write" current, reducing its net effect by .1/2; there is insufficient flux change to cause the ferrite core to change to the "1" magnetization state, so at the end of the WRITE TIME, the core is left magnetized in the "0" state. The INHIBIT signal enables inhibiting only during the WRITE TIME.

Table 2-5. Read, Write, Sense, Inhibit (Cont'd)

DECODER GATES

Each Decoder Gate Assembly contains eight decoder gate circuits. One Decoder Gate Assembly decodes part of the "X" address from the Horizontal Hold Assembly. The other Decoder Gate Assembly decodes part of the "Y" address from the Horizontal Hold Assembly. Other decoding takes place at the Read/Write Generators for "X" and "Y" addresses.

The Decoder Gate Assemblies provide current paths to ground for the "read" or "write" currents from the Read/Write Generators.

READ/WRITE GENERATORS

Each Read/Write Generator contains four decoding gate circuits. One Read/Write Generator is for the "X" address lines, the other for the "Y" address lines. The Read/Write Generators connect one line from each Decoder Gate Assembly to the +19.5-volt supply (to "write") or to the -19.5-volt supply (to "read").

ADDRESS DECODING

The Memory Core Stack contains 1024 (2^{10}) addressable locations.

By arranging the ferrite cores in 32 x 32 ($2^5 \times 2^5$) core arrays, we need supply only 32 "X" addresses and 32 "Y" addresses.

All addresses are 10-bit binary numbers. Each Decoder Assembly decodes three bits of the address; and each Read/Write Generator decodes two address bits.

Each Decoder Gate controls four current paths from the associated Read/Write Generator. Each Decoding Gate in the Read/Write Generator controls one of these four current paths.

When decoding is correctly completed, only one of the 32 possible "X" Read/Write Generator-thru-Memory Core Stack-thru-Decoder Gate current paths is completed, and only one of 32 similar "Y" paths is completed. Thus only one of the 1024 total possible "X" and "Y" combinations has both current paths completed, causing a "read" or a "write" current to pass through the correct group of 24 cores.

TEMPERATURE-COMPENSATED ±19.5-VOLT POWER SUPPLIES

The amount of current required to cause ferrite cores in the Memory Core Stack to change states depends on Memory Core Stack temperature. As temperature decreases, it becomes more difficult to cause the ferrite cores to change states, so the supply must provide increased current. Conversely, as temperature increases, and it becomes easier to cause the cores to change states, it becomes more difficult to inhibit writing of a "1." The temperature-compensated ±19.5-volt supplies in the memory section have the required voltage-vs-temperature coefficient for proper Memory Core Stack operation over the specified Signal Analyzer operating temperature range.

Table 2-6. Memory Sectioning

GENERAL

Memory sectioning enables addressing only certain groups (quarters) or memory addresses during processing or display modes of operation. Which memory quarters are enabled depends on

a. FUNCTION switch setting

b. MEMORY SELECTOR setting

c. Which Analog Plug-in is installed

d. Which front-panel pushbutton is lighted.

The circuitry shown in the accompanying block diagram determines which memory quarters are enabled.

DESCRIPTION

Inputs

MEMORY SELECTOR is either or both of the 5485A MEMORY SELECTOR switches.

DISPLAY is either or both of the 5485A DISPLAY switches.

FUNCTION is the 5486A/B FUNCTION switch, when set to SUMMATION or AVERAGE.

20 MHz and Gate (Direction) Control Signals increment the Process Address Register at a rate determined by the 5486A/B SWEEP TIME switch, and/or increment the Display Address Register at a fixed 100 kHz rate. The Address Registers are multiplexed, and the output from either one is used (see Figure 2-8).

Circuits

ADDRESS REGISTER is a 10-bit register, incremented serially, that keeps track of memory location being processed or displayed. Memory sectioning is determined by AR bits 0 and 1, the last two Address Register (AR) bits, which are located on A3A9 in the 5480A/B Main Frame Logic Section.

5485A SWITCHING LOGIC A compares settings of both MEMORY SELECTOR switches and states of AR bits 0 and 1. The four output signals to the Memory Logic Assembly (A2A14) are coded to represent the settings of the two switches, and whether or not either DISPLAY switch is set to OFF. The CHANNEL OK ($\overline{\text{CHOK}}$) indicates that the Address Register Multiplexer (AR MPX) output, as indicated by AR bits 0 and 1, is in a quarter chosen by the MEMORY SELECTOR switches.

$\overline{\text{MAAR0}}$ A2A14(N)	$\overline{\text{MBAR0}}$ A2A14(M)	$\overline{\text{MAAR1}}$ A2A14(L)	$\overline{\text{MBAR1}}$ A2A14(K)	MEMORY QUARTERS ENABLED (By Channel A and/or Channel B MEMORY SELECTOR switches)
H	H	H	H	NONE (A DISPLAY and B DISPLAY both OFF)
H	H	H	L	NOT USED
H	H	L	H	NOT USED
H	H	L	L	NOT USED
H	L	H	H	NOT USED
H	L	H	L	1
H	L	L	H	2
H	L	L	L	1, 2
L	H	H	H	NOT USED
L	H	H	L	3
L	H	L	H	4
L	H	L	L	3, 4
L	L	H	H	NOT USED
L	L	H	L	1, 3
L	L	L	H	2, 4
L	L	L	L	1, 2, 3, 4 (Either switch set to FULL or OVERLAP, or one switch set to HALF 1, 2 and other switch set to HALF 3, 4)

Table 2-6. Memory Sectioning (Cont'd)

5486A/B PROGRAM SELECTOR B uses the $\overline{\text{CHOK}}$ signal to enable processing (Summation or Average), Display, or Prepare program (see Figure 2-10) when FUNCTION is set to SUMMATION or AVERAGE. If $\overline{\text{CHOK}}$ indicates AR MPX output is not for selected memory quarter, there will be no operation.

5486A/B PROGRAM SELECTOR A determines which program will be done during any 10 usec period. (See Table 2-10.)

5486A/B LOGIC A converts the program selection information into control signals that determine whether (and when) a READ, WRITE, or CYCLE (READ-then-WRITE) will be performed at the addressed memory location. This assembly also provides the SET HORIZ signal, which controls gating of AR MPX contents into Horizontal (Address) Hold Register.

MEMORY TIMER makes sure the $\overline{\text{READ TIME}}$ and $\overline{\text{STROBE TIME}}$, $\overline{\text{WRITE TIME}}$ and $\overline{\text{INHIBIT TIME}}$ signals required for proper memory core operation occur when they should (see Table 2-5).

READ/WRITE GENERATOR (see Table 2-5) decodes some address bits and $\overline{\text{READ TIME}}$ or $\overline{\text{WRITE TIME}}$ signals to enable data transfer from or to memory.

MEMORY LOGIC compares AR bits 0 and 1 against signals representing MEMORY SELECTOR switch settings, and modifies the AR bits as required so only bits corresponding to selected memory quarters will be transmitted to Horizontal (Address) Hold Register. In addition, this assembly uses the SET HORIZ signal from 5486A/B LOGIC A to form CLOCK 2. When the FUNCTION switch is set to SUMMATION or AVERAGE, and the 5480A/B is operating independently, CLOCK 2 occurs only when there is a $\overline{\text{CHOK}}$ signal.

HORIZONTAL D.A.C. (INCLUDING HORIZONTAL HOLD REGISTER) inputs are 8 unmodified AR MPX bits, and two bits that can be modified as described in this figure to correspond to selected memory quarters only. When FUNCTION switch is set to SUMMATION or AVERAGE, Horizontal Hold Register contents can be changed only when AR MPX output bits 0 and 1 indicate address is for a selected memory quarter.

DECODER GATE decodes part of Horizontal Hold Register output, including modified AR bits 0 and 1 and provides a sink for Read or Write addressing currents as described in Figure 2-5.

Operation Example

FUNCTION switch set to SUMMATION or AVERAGE

Channel A MEMORY SELECTOR switch set to QUARTER 1

Channel B DISPLAY switch set to OFF

ADDRESS REGISTER OUTPUTS*				HORIZ HOLD OUTPUTS*			Memory Location Addressed	CHOK State
Address	AR2	AR1	AR0	MA2	MA1	MA0		
0000	0	0	0	1	1	1	0000	L
0001	0	0	1	1	1	1	0000	H
0002	0	1	0	1	1	1	0000	H
0003	0	1	1	1	1	1	0000	H
0004	1	0	0	0	1	1	0004	L
0005	1	0	1	0	1	1	0004	H
				etc.				

* 1 = signal names without "bar" (AR0, AR1, etc.) are "H"
signal names with "bar" ($\overline{\text{AR0}}$, $\overline{\text{AR1}}$, etc.) are "L"
0 = opposite of "1"

Table 2-6. Memory Sectioning (Cont'd)

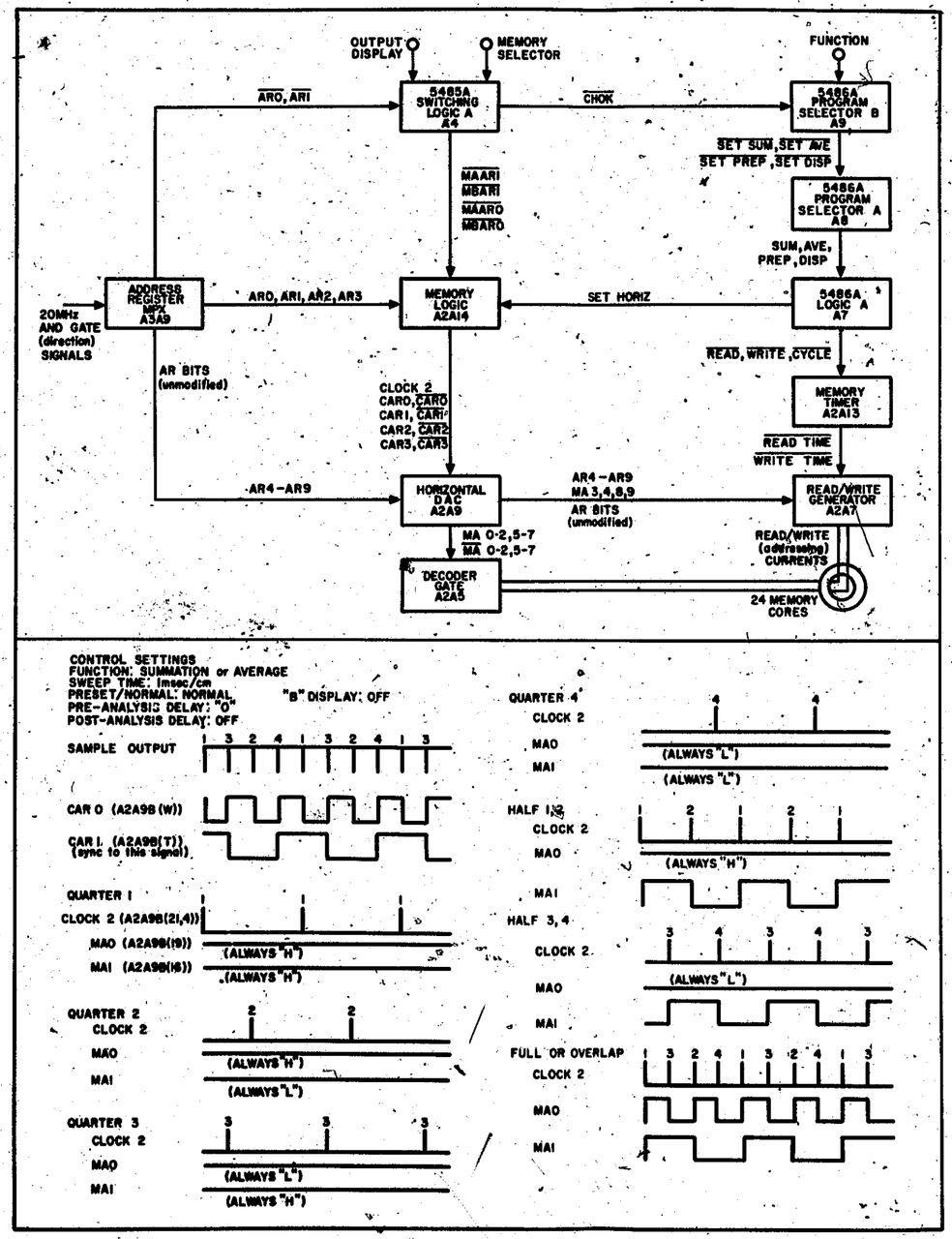


Table 2-7. Registers

GENERAL

The Signal Analyzer contains the following registers to process data and keep track of programs. The Process Address Register, Display Address Register, and Accumulator are part of the Main Frame Logic Section (5480A/B Section 3); the Horizontal Hold Register, and the Horizontal and Vertical Digital-to-Analog Converters are part of the Memory Section (5480A/B Section 2); the Shift Hold Register is located in the 5486A/B Plug-in.

PROCESS ADDRESS REGISTER (PAR)

This register keeps track of the processing address for the AVERAGE, SUMMATION and MCS functions. It is advanced one count each time processing begins, so it always contains the address of the next point to be processed. PAR rate depends on SWEEP TIME switch setting. PAR handles 10 bits. In HISTOGRAM, this register counts input frequency or time base for gated TIME INTERVAL.

DISPLAY ADDRESS REGISTER (DAR)

This register keeps track of the display address for the display routine. This register is incremented one count each time the display for an address ends, so it contains the address of the point being displayed. DAR rate is fixed at 1 millisecond per centimeter. DAR handles 10 bits.

HORIZONTAL HOLD REGISTER

This register always contains the address of the word being processed or displayed, and is the register that actually addresses the memory stack and provides the drive for the horizontal digital-to-analog converter in the display section. Input to this register is gated from either the PAR or DAR. Horizontal Hold Register handles 10 bits.

ACCUMULATOR

The Accumulator is the data processing register and the input/output register for the memory stack. It can be controlled to produce open loop shifts (shifts) or closed loop shifts (rotations) in either direction (see Table 2-10). A left shift causes multiplication, a right shift causes division. The multiplier or divisor is always 2^n, where n is the number of shifts performed by the accumulator. Data is counted into the accumulator at bit 0. Data transfer between the accumulator and the memory stack is bit-for-bit parallel entry. The accumulator can handle 24 bits.

DIGITAL-TO-ANALOG CONVERTERS

The Vertical DAC and Horizontal DAC include flip-flop registers for storing the digital information that is to be converted to analog information for the Display Section. The digital-to-analog converters each can handle 10 bits of information (vertical DAC input is the 10 most-significant Accumulator bits).

SHIFT HOLD REGISTER

This sixth register in the 5480A/B System is located in the 5486A/B Control Plug-in; its function is to keep track of accumulator shifts. While the Signal Analyzer is processing signals, it keeps track of the number of sweeps that have occurred, to provide proper data weighting. When the OUTPUT DISPLAY button is lighted, it provides the proper number of accumulator shifts, as determined by the SENSITIVITY MULTIPLIER for proper scaling of the display.

Table 2-8. Address Registers

The address registers are located on board assemblies A3A9 through A3A11 in the 5480A/B Main Frame logic section.

GENERAL

Separate registers are used to keep track of the memory location being processed and the memory location being displayed. The outputs of the process and display address registers are multiplexed together and sent to the memory decoding circuit (see Table 2-6). By multiplexing we mean that only one address register output is used at any given time. The address contained in either register is not lost when the interlace display control selects the other register during a display or process routine. Generally, the instrument is displaying faster than it is processing as can be seen by the slower rate of the processing sweep in the CRT display.

DISPLAY ADDRESS REGISTER

The display address register (DAR) is a series of simple D-type flip-flops in cascade, counting up in a binary sequence. Except when a data point is being processed, the display address register is clocked every ten microseconds, its count increasing by one each time, until it is reset. This is explained in further detail in the display program, Table 2-13.

PROCESS ADDRESS REGISTER (PAR)

The PAR is much more sophisticated than the DAR, and resembles the accumulator in its action and appearance. Except for bits 0 and 1, the process address register is almost an exact duplicate of the accumulator as far as the regular bits are concerned. Bits 0 and 1 of the PAR are set up to count by +2 and +4 as well as by +1 and -1. Normally, in the 5480A/B, we only count up or down plus-or-minus one count in bits 0 of the process address register. The input to the process address register is 20 MHz clock pulses, gated through a pulse synchronizing circuit to improve pulse resolution and eliminate partial pulses. A similar circuit appears on the accumulator control board. The output from bit 1 is sent through a pulse stretching one-shot multivibrator so the pulse will reliably propagate into the succeeding bits. Each address register assembly A3A9, A3A10, or A3A11 contains both the display address register and the process address register and the multiplexing circuit for two or four bits. Bits 0 and 1 are on A3A9, bits 2 through 5 are on A3A10, and bits 6 through 9 are on A3A11.

ADDRESS REGISTER CONTROL ASSEMBLY

The address register control assembly contains two flip-flop type circuits and several buffer circuits that are used to enable operations on the address registers and data transfer between the address registers and the horizontal hold register, which is in the memory section.

Par Mode Flip-Flop

The process address mode flip-flop or PAR mode flip-flop has four outputs and 8 inputs. Four of the inputs are from sources inside the 5480A/B system and four inputs are from external sources. The flip-flop outputs are all H = true, the inputs are L = true.

The PAR mode flip-flop command outputs do the following things:

COUNT PAR is used during HISTOGRAMS enabling the Process Address Register to count the output from the Analog-to-Digital converter or the 5480A/B time base. The greater number of counts, the higher address number the PAR will reach before counting stops (indicating higher FREQUENCY or longer TIME interval). When PAR counting has stopped (in HISTOGRAM), the memory contents at that address are read into the Accumulator, incremented by one count, and this new value written back into memory at the same address (see Table 2-22). Count PAR is also used for enabling the PAR to be incremented during the AVERAGE, SUMMATION, MCS, and PREPARE programs.

SHIFT RIGHT PAR is a command that is not normally used in the 5480. It enables certain mathematical operations (division) using the process address register. All mathematical operations now use the Accumulator register.

SHIFT IN PAR is not normally used in the 5480A/B. This command enables data to be shifted in parallel into the process address register.

(Cont'd on next page)

Table 2-8. Address Registers (Cont'd)

MPX Control Flip-Flop

The Multiplex control Flip-flop has three outputs and up to 6 inputs. The MPX FF output commands do the following things:

PAR TO HOLD enables the Process Address Register contents to be shifted to the Horizontal Hold Register. Thus the PAR contents may be converted to a memory address and provide the horizontal display location.

DAR TO HOLD enables the Display Address Register contents to be shifted to the Horizontal Hold Register, in which case the DAR contents become the memory address and provide the horizontal display location.

ACCUM TO HOLD is not used in the 5480A/B. It would cause accumulator bits 0-9 to be transferred to the Horizontal Hold Register.

Table 2-9. Accumulator

DESCRIPTION

The accumulator is a 24-bit register that performs the mathematical operations required by the 5480A/B. It has data inputs from both the memory stack and from the analog plug-in, and control inputs from the logic plug-in and from the rear panel. Processing consists of the arithmetical functions of addition, subtraction, multiplication, and division. All inputs to, and outputs from, the memory stack are through the accumulator register.

INPUTS AND OUTPUTS

Information can be put into the accumulator in any of three ways: transferring it in from memory (parallel entry); shifting it in (serially); or counting it in. Output information from the accumulator is always parallel, whether back into the memory core stack or to the vertical digital-to-analog converter. The Digital-to-Analog converter uses only the 10 most significant accumulator bits, bits 14 through 23.

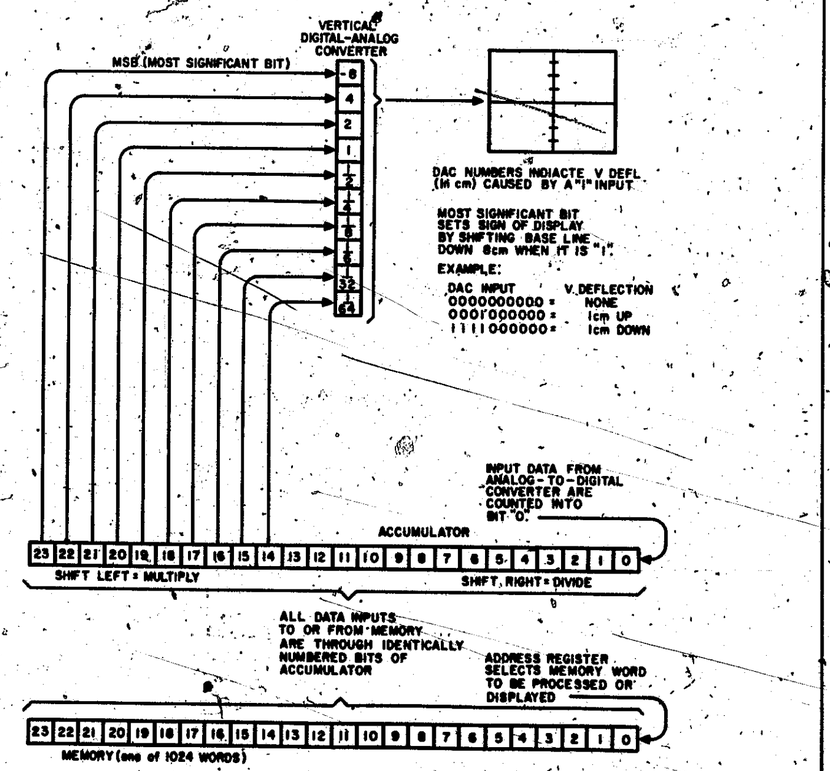


Table 2-9. Accumulator (Cont'd)

MATHEMATICAL OPERATIONS

Negative Numbers

In the 5480A/B all numbers are processed and stored in "two's complement" form. In this form, the most significant bit (bit 23) is used as a sign bit, and the remaining bits represent the magnitude in two's complement form. Using only bits 14 through 23 (the only ones that affect the 5480A/B display), the examples below show the differences between a positive and negative number in the 5480A/B accumulator, memory, A-D and D-A converters; the numbers used represent those required for 1 cm vertical deflection on 5480A/B CRT.

INPUTS	"+1 cm"	"-1 cm"
Two's comp representation	0001000000	1111000000

To find the magnitude of the negative number:

1) change all 1's to 0, all 0's to 1: 0000111111

2) add 1 to this number:

```
  0000111111
+           1
------------
  0001000000
```

3) put a minus sign in front of the answer, and convert the answer from binary to cm of deflection -0001000000 = -1 cm

To find the accumulator contents for a negative number:

EXAMPLE find accumulator contents that will give -3 cm deflection

1) write the binary representation that will give a positive deflection of the given amount: 0011000000

2) change all 1's to 0, all 0's to 1: 1100111111

3) add 1 to this number:

```
  1100111111
+           1
------------
  1101000000
```

Addition And Subtraction

Normal rules for binary addition and subtraction apply.

ADDITION:

```
  1100101000
+ 1011100011
------------
 11000001011
```

= 1000001011 (the 1 carrier at left in addition is "lost")

```
  0100100000   (+4-1/2 cm deflection) (Sign bit = "0")
+ 0100100000   (+4-1/2 cm deflection) (Sign bit = "0")
------------
  1001000000   (-7 cm deflection) (sign bit = "0") (note the "foldover" effect, two
               positive numbers added together producing a negative number.
               This can happen in SUMMATION when SENSITIVITY MULTIPLIER
               switch is not set to AUTO.
```

SUBTRACTION:

```
  1100101000
- 1011100011
------------
```

can't be done in this form (convert - number to two's complement from and add)

```
  1100101000
+ 0100011101
------------
 10001000101
```

= 0001000101 (the 1 carried at left in addition is "lost")

Table 2-9. Accumulator (Cont'd)

Multiplication And Division

Normal rules for binary multiplication and division apply. All multiplication is by powers of 2, and is accomplished by shifting data left or right in the accumulator the required number of places.

```
  1100101000
  1100101000
  1100101000
+ 1100101000
------------
 1100101000000
```

= 1100101000 shifted left two places (multiplied by 2^2)

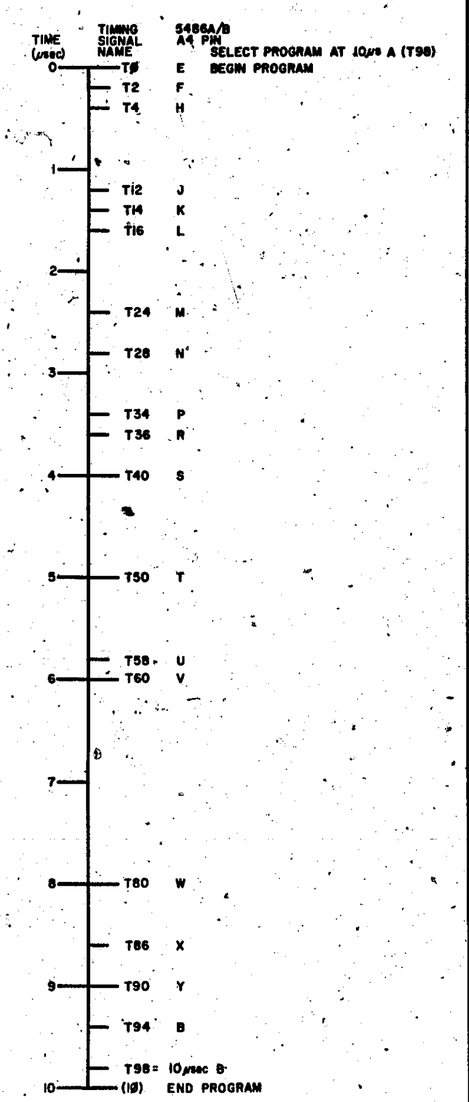
Table 2-10. Programs

GENERAL

Eight hard-wired programs are available for data acquisition, data processing, and data output. These programs are built into the System hardware and cannot be changed. Only certain program combinations are used with each FUNCTION switch setting, as described in Figures 2-19 through 2-22. Program selection is done by 5486A/B Program Selector A8. The programs are summarized below and described in detail in Figures 2-11 through 2-18.

Outputs are all "H" = "true"

Program	5486A/B A8 pin
NOP	R
PREPARE	Y
DISPLAY	X
SUMMATION	T
AVERAGE	S
HIST. BEGIN	V
HIST. END	W
MCS	U



NOP (No Operation)

A general-usage program, which can be used with other programs or by itself. Since the 5486A/B A8 NOP output (pin R) is not connected, we actually do a "psuedo-NOP" program when there is no other program selected. NOP occurs for the last microsecond of any of the processing programs (SUM, AVE, HIST. BEG., HIST. END, MCS), and continuously when the PROCESS STOP pushbutton is lighted.

Prepare

A general-usage program, used with other 5480A/B programs. Keeps track of SWEEP NUMBER, determines "k" for Averaging program (see Figure 2-20), and determines scaling factor based on SENSITIVITY MULTIPLIER setting when OUTPUT DISPLAY or OUTPUT RECORD button is pressed. Active only when address register is in last address of selected memory quarter (this program may be executed up to four times per sweep).

Memory Quarter	Last Address
1	1020
3	1021
2	1022
4	1023

Table 2-10. PROGRAMS (Cont'd)

Display

A general-usage program, which can be used with other 5480A/B programs. Enables all points selected by MEMORY SELECTOR switches to be shown when PROCESS START is lighted (when Display Interlace is set to In), or when OUTPUT DISPLAY or OUTPUT RECORD is lighted.

Summation

Used only when FUNCTION switch is set to SUMMATION. Enables SUMMATION averaging of analog signals at 5485A inputs. (See Figures 2-14 and 2-20.)

Average

Used only when FUNCTION switch is set to AVERAGE. Enables 5480A/B to keep a running average of analog signals at 5485A inputs. (See Figures 2-15 and 2-20.)

Histogram Begin

Histogram End

Used only when FUNCTION switch is set to HISTOGRAM. Enable 5480A/B to measure frequency or period of pulsed signal connected to 5486A/B input connector. (See Figures 2-16, 2-17, 2-21.)

Mcs

Used only when FUNCTION switch is set to MCS. Enables 5480A/B to accumulate counts in each of 1000 separate channels.

BASIC TIMING CYCLE

All of the above programs use timing signal generated as part of the basic timing cycle. The timing cycle is 10 microseconds long. Timing signals are named T0 through T98. Each signal name indicates how many tenths of a microsecond after T0 the signal occurs; T2 occurs 0.2 usec after T0, etc. The timing signals are generated by 5486A/B cards A2-A4. Each of these signals is a "H" (+5V) = "true" pulse, 100 nsec wide. As you read the timing descriptions for the 5480A/B programs (Figures 2-11 through 2-18), note that although the timing signals are used in ascending numerical order, the signals used are not necessarily from the same 10 usec period. A Program may use the T2 signal from the first 10 usec period, but it won't necessarily use T4 until one or more additional periods have passed.

The 5480A/B cannot change from one program to another until it completes the program it is using.

Table 2-11. No-Operation Program

GENERAL

The No Operation (NOP) Program output is "H" during the conditions shown in the diagram below. The output signal (available at 5486A/B A8(R)) is not used in the 5480A/B system (this output is not connected), so any reference to the NOP program really refers to the "Psuedo-NOP" Program.

PSUEDO-NOP PROGRAM

When the NOP program is selected (eg. no other program was selected), the 5480A/B stops all processing and display functions. The PROCESS STOP pushbutton does not necessarily light (the signal that lights the light is used to enable the NOP program, not vice-versa); when PROCESS STOP is lighted, the NOP output (only) from 5486A/B A8 should be "H".

The NOP program occurs at T94* of any processing or display program, and lasts until a new program is begun.

Normally, the last PROCESS or OUTPUT control pushbutton pressed, then released, eventually gains programming control of the 5480A/B System. The delay circuit built into A4A1 at one input to the PROCESS STOP gate acts, simulates this condition when ac power is first turned on, causing the Switching Logic circuit to act as if PROCESS STOP were the last button pressed. The PROCESS TOP button lights, and the NOP program is executed continuously until one of the other control pushbuttons is pressed.

*For 5486A: T94 was T90, T36 was T34

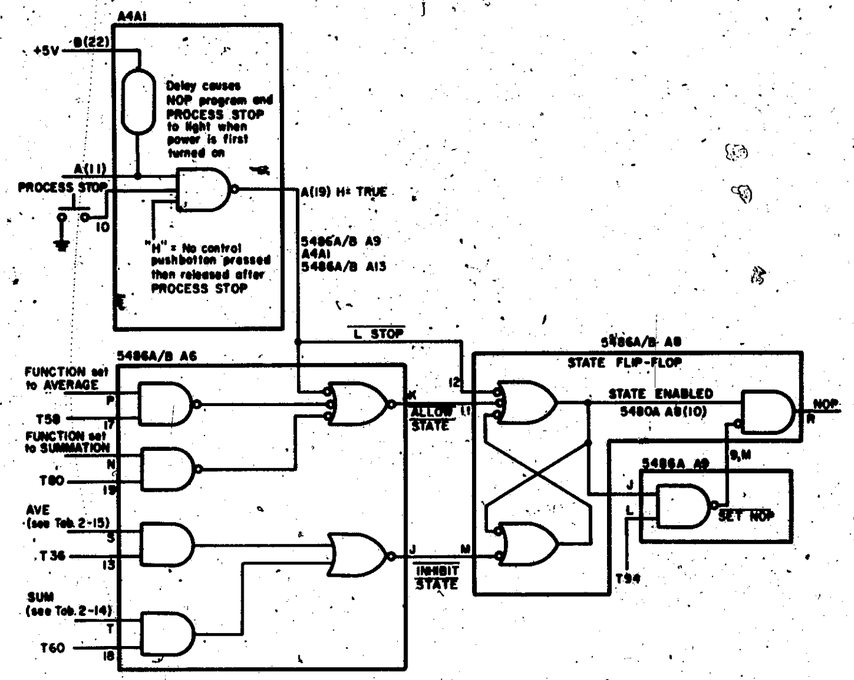


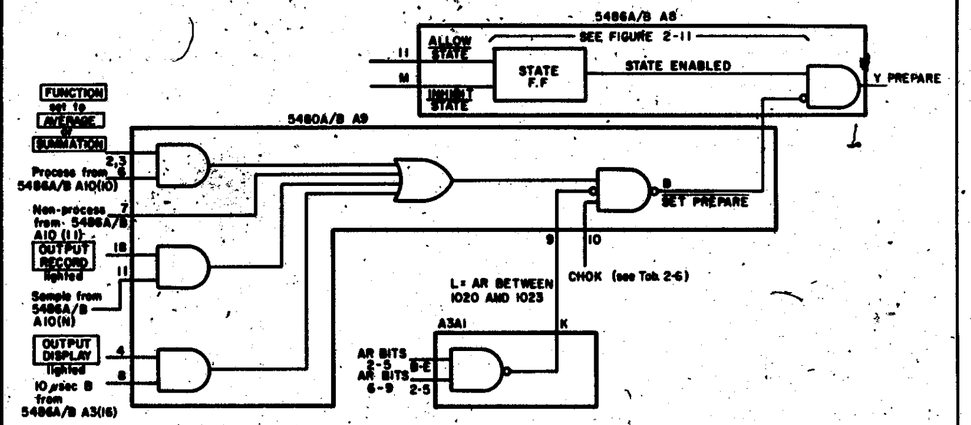
Table 2-12. Prepare Program

GENERAL

The Prepare Program is a general-purpose "housekeeping" program used with other processing or display programs. It keeps track of the following 5480A/B System information.

1) "k" for the Averaging algorithm (see Figures 2-15 and 2-21), 2) scaling factor, based on SENSITIVITY MULTIPLIER setting.

The Prepare Program is enabled by the conditions shown in the diagram below.



TIMING

Timing Signal	Boards	Event
T0	A3A1 5486A/B A9 5486A/B A8	Prepare Program begins
T2	5486A/B A7 A3A2-A3A8	Accumulator is cleared
	5486A/B A5, A11	Shift Control Register is cleared
	5486A/B A7, A3A2-A3A8	Accumulator left shift is enabled, but not executed
	5486A/B A13 A3A9-A3A12	Address Register contents are transferred to Horizontal Hold Register
T4	5486A/B A7, A3A2-A3A8	Contents of addressed memory location are transferred to Accumulator
T12	5486A/B A13, A3A9-A3A12	If PROCESS START is lighted, Process Address Register contents are increased by "1"
	5486A/B A12 A3A9-A3A12 5486A/B A11	Display Address Register contents are increased by "1" (19-sweep number setting on 5486A/B) is set into Shift Control Register

(Cont'd on next page)

Table 2-12. Prepare Program (Cont'd)

Timing Signal	Boards	Event
T14	5486A/B A6 A3A2-A3A8 5486A/B A11	Accumulator (closed loop) left shift begins. Shifting continues until Shift Control Register contents are counted down to zero, one shift at a time, for a total of 24 shifts. There is no net shift, since Accumulator contents are same as when shifting began.
T60	5486A/B A5, A11	If SENSITIVITY MULTIPLIER is not set to AUTO and PROCESS START is not lighted, and FUNCTION is not set to AVERAGE Shift Hold Register is cleared
T80	5486A/B A5, A11	If SENSITIVITY MULTIPLIER is not set to AUTO and PROCESS START is not lighted, and FUNCTION is not set to AVERAGE SENSITIVITY MULTIPLIER (scale number) setting is set into Shift Hold Register
	5486A/B A5 A3A2-A3A8	If PROCESS START is lighted and PRESET REACHED Accumulator contents are increased one count, so contents of memory addresses 1020 through 1023 are number of times each quarter has been processed.
T86	5486A/B A7 A3A3-A3A8 A2A1-A2A8	Accumulator contents are transferred into memory. Note that there is no display as part of the Prepare Program, so these memory contents do not appear on the CRT.
	T90 5486A/B A9	Select next program to be done
T98		End Program

(End)

Table 2-13. Display Program

GENERAL

This program enables memory contents to be read out for presentation on the 5480A/B CRT or external unit. The normal Display Program causes the Display Address Register to be incremented at a 100 kHz rate. A program modification (when OUTPUT RECORD is pressed) causes the Display Address Register to be incremented at a rate determined by the SWEEP TIME control, enabling a slow presentation for a point plotter or X-Y recorder.

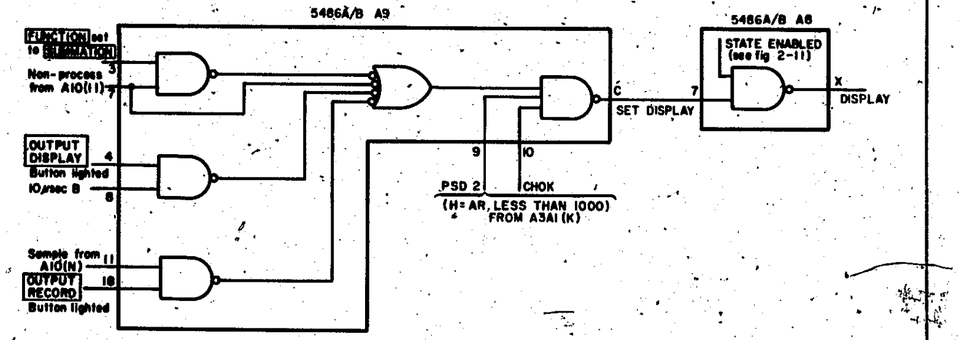
The Display Program is enabled by the conditions shown in the figure below.

As part of the Average of Summation programs, memory contents for each selected point are displayed before the point is processed. Except for the fastest sweep times, the trace will flicker or appear as a slowly moving dot. By interlacing the Display Program and the Processing (Summation or Average) Program, a flicker-free display of data can be provided.

Processed points are not displayed as part of the Histogram Begin or Histogram End Programs, so the Display Program must be interlaced to enable viewing these points during processing. Note: there is no display in 1 msec/cm HISTOGRAMs, as there is no time to interlace.

As part of the MCS program, memory contents for each selected point are displayed before new MCS counts are added. Ordinarily the display will be a dot (or trace), whose speed is determined by SWEEP TIME setting. Because we have only one Accumulator, and don't want to take time from processing for display, it is unlikely that there will be any apparent vertical deflection in the trace while the system is processing in MCS; no Accumulator shifts are performed, and data must be in the 15th Accumulator bit position (bit 14) before it can cause the trace to deflect even 1/64 cm vertically ($2^{15} = 32,768$).

TIMING



Timing Boards	Boards	Event
T0	5486A/B A8 A4A1 5486A/B A9 5486A/B A10	Display Program Starts
T2	5486A/B A7 A3A2-A3A8	Accumulator is cleared
	5486A/B A10 5486A/B A13 A3A12-A3A9- A3A11 A2A14, A2A9	Display Address Register number is transferred to Horizontal Hold Register
	5486A/B A7 A2A10	If PROCESS START is lighted, and FUNCTION SWITCH is set to AVERAGE, Accumulator contents (all '0') are transferred to Vertical DAC.

(Cont'd next page)

Table 2-13. Display Program (Cont'd)

Timing Signal	Boards	Event
T4	5486A/B A7 A2A13 A2A7, A2A8	$\overline{\text{CYCLE}}$ causes contents of addressed memory location to be read from memory into Accumulator, then written back into memory at the same location (using the Accumulator as source). Data is now in the Accumulator for current use (Display) and in memory for future use (Display or Processing).
T12	5486A/B A7 A3A2	Accumulator left shift is enabled, but not performed at this time.
	5486A/B A10 A3A12, A3A9-11	Display Address Register is incremented to next address
	5486A/B A7 A2A10	Accumulator bit 23 is set into Vertical DAC
	5486A/B A7 5486A/B A11	If SENSITIVITY MULTIPLIER is set to AUTO and FUNCTION is not set to AVERAGE Mod 24 counter is preset to cause correct number of accumulator shifts, as determined by SWEEP TIME setting.
T16	5486A/B A7 A2A10	If FUNCTION is set to AVERAGE Accumulator contents are transferred into Vertical Digital-to-Analog Converter. The Average Program (Figure 2-15) shifts data to most significant accumulator bits before storing it in memory. When this data is retrieved from memory, it is already in the proper accumulator bit positions for display (if SENSITIVITY MULTIPLIER is set to AUTO).
	5486A/B A13 A3A12, A3A9-11	If Display Interlace is set to In and PROCESS START is lighted and AR MPX output is between 1020 and 1023 Display Address Register is cleared.
T26	5486A/B A5 5486A/B A12 5486A/B A11 A3A2-A3A8	If SENSITIVITY MULTIPLIER is not set to AUTO or FUNCTION is not set to AVERAGE Accumulator left shift begins. Each shift causes the Mod 24 counter to count up one count. Shifting continues until the Mod 24 counter contents equal contents of Shift Hold Register.
T34	5486A/B A13 A3A12, A3A9, 11	If AR MPX output is between 1020 and 1023 and OUTPUT DISPLAY OR OUTPUT RECORD is lighted Display Address Register is set to address 1023.

(Cont'd on next page)

Table 2-13. Display Program (Cont'd)

Timing Signal	Boards	Event
T60	5486A/B A7 A2A10	If FUNCTION is not set to AVERAGE Accumulator contents are transferred into Vertical Digital-to-Analog Converter.

OUTPUT RECORD

This program is the same as the Display Program is nearly all respects, except that different enabling circuits are used to determine when the program will be performed.

When the OUTPUT RECORD button is pressed

	A4A1 5486A/B A13	The Display Address Register is cleared, and remains cleared as long as the button is held in.

As soon as the OUTPUT RECORD button is released, the PEN LIFT signal goes to 0V; this signal may be used to lower the pen of a point plotter or chart recorder.

As long as the OUTPUT RECORD button is lighted, the Servo Enable/Disable signal can enable a point plotter servo (5480B and 5480A with serial prefix 928 and above, only).

At T90 of a NOP or Display Program	A4A1 5486A/B A9	The gating circuits that allow the occurrence of the Display Program to be controlled by the SWEEP TIME switch are enabled.
T0	5486A/B A9 5486A/B A10 5486A/B A3 5486A/B A2	The SWEEP TIME and PRE-ANALYSIS DELAY switches determine the occurrence of timing signals that are required to start the Display Program. (Normally, the Display Program is started by a 100 kHz signal directly from the time base, without the additional gating.)

The Display Program from here through T90 is the same as for the normal Display Program

Shortly (3-5 usec) after T60, the CRT Z-axis is unblanked (for 3 to 5 usec) and the SEEK pulse (> 50 μsec wide) is outputted to the plotter. If a point plotter is used, it provides a PLOT input to the 5480A/B when the plot of each point has been completed; this signal enables plotting of the next point (5486A/B SWEEP TIME must be set to EXT.).

The Display Address Register is incremented as in the normal Display Program, and at the end of the time determined by SWEEP TIME and PRE-ANALYSIS DELAY switch settings, the program occurs again at the new address.

T90	5486A/B A9 5486A/B A8	If Display Address Register is between 1020 and 1023 The 5480A/B does one Prepare Program (OUTPUT RECORD button remains lighted).
At T90 of the Prepare Program	5486A/B A9 5486A/B A8	The PROCESS STOP button is lighted (OUTPUT RECORD button light turns off), and the 5480A/B does NOP Programs until one of the unlighted buttons is pressed, to make it do something else.

(End)

Table 2-14. Summation Program

GENERAL

This program is started (set) only when:

PROCESS START is lighted

and

FUNCTION is set to SUMMATION

and

Process Address Register output is for a selected memory quarter

This program causes the Signal Analyzer to add the digitized input signal to previous inputs (stored in memory), and store the new value in memory. The SENSITIVITY MULTIPLIER and SWEEP NUMBER switches control display size during processing, as follows:

1. If SENSITIVITY MULTIPLIER is not set to AUTO, the Signal Averager display will grow with each sweep. In time, it will grow "off-screen", and appear to fold over and the top and bottom of the display as Accumulator contents appear to be incremented from their most positive value to their most negative value (see Figure 2-9).
2. If SENSITIVITY MULTIPLIER is set to AUTO, the Signal Averager will automatically scale the growing display to keep it "on-screen". After completion of every 2^Nth sweep (until N is equal to the SWEEP NUMBER setting), the display size is cut in half (by having the Accumulator perform one less shift before displaying the data). If PRESET/NORMAL is set to PRESET, the display will be calibrated in accordance with the SENSITIVITY setting when processing stops; if PRESET/NORMAL is set to NORMAL, the display will continue growing, as if SENSITIVITY MULTIPLIER were not set to AUTO.

TIMING

Timing Signal	Boards	Events
T0	5486A/B A9 5486A/B A8 5485A A4 A3A1	Summation Program begins
	5486A/B A6 A3A2-A3A8	Closed loop is enabled, thus an Accumulator shift is, effectively, a rotation.
	5486A/B A6 5486A/B A12	Output MPX is set
T2	5486A/B A7 A3A2-A3A8	Accumulator is cleared
	5486A/B A7 A3A2-A3A8	Accumulator left shift is enabled, but not performed at this time
	5486A/B A7 5486A/B A13 A3A12, A3A9-A3A11 A2A14, A2A9	Process Address Register contents are transferred to Horizontal Hold Register
T4	5486A/B A7 A2A13 A2A7, 8	Contents of addressed memory location are read into accumulator. Memory contents at this address after this operation are all "0"
T12	5486A/B A5 5486A/B A11 5485A A3 5486A/B A2	Mod 24 counter is preset to cause correct number of accumulator shifts, as determined by SWEEP TIME setting

(Cont'd on next page)

Table 2-14. Summation Program (Cont'd)

Timing Signal	Boards	Events
T12 (cont)	5486A/B A5 5486A/B A12 A3A2-A3A8 5486A/B A11	Accumulator left shift begins. Each shift causes the Mod 24 counter to count up one count. Shifting continues until contents of the Mod 24 counter equal contents of Shift Hold register.
	5486A/B A10 A3A12, A3A9-A3A11	Display Address Register is incremented to next address
	5486A/B A13 5486A/B A5 A3A12, A3A9-A3A11	Process Address Register is incremented one count.
	5486A/B A7 A2A10	Most significant Vertical DAC input but is transferred from accumulator.
T16	5486A/B A13 A3A12, A3A9-A3A11	If PROCESS START is lighted and Display Interlace is set to In and Display Address Register output is between 1020 and 1023 Display Address Register is cleared
		If PROCESS START is lighted Process Address Register contents are transferred to Horizontal Hold Register
		If OUTPUT DISPLAY is lighted Display Address Register contents are transferred to Horizontal Hold Register
T34	5486A/B A7 A2A10	Accumulator contents are transferred to Vertical DAC
	5486A/B A13 A3A12, A3A9-A3A11	If AR MPX output is between 1020 and 1023, and A Summation Program was done last Process Address Register is set to 1023
		If AR MPX output is between 1020 and 1023 and A Display Program was done last Display Address Register is set to 1023
	5486A/B A7 A3A2-A3A8	Accumulator right shift is enabled, but not performed at this time

(Cont'd on next page)

Table 2-14. Summation Program (Cont'd)

Timing Signal	Boards	Events
T40	5486A/B A5 5486A/B A11 5485A A3 5486A/B A2	Mod 24 counter is preset (to same number as T12) to cause correct number of accumulator shifts. In this case, the correct number of shifts results in data being stored in the same bits as when this program started. The left shift was provided to enable proper scaling of data in the CRT presentation (data was presented when accumulator contents were transferred into Vertical DAC). The right shift puts these same data bits back into their correct places for processing (adding digitized input data).
	5486A/B A5 A3A2-A3A8	Accumulator shift starts. Each shift causes the Mod 24 counter to count down one count. Shifting continues until the Mod 24 counter contents are equal to contents of Shift Hold Register.
T58	5486A/B A5 5485A A3 5485A A6 A3A2-A3A8	START ADC begins digitizing process, to convert analog input signal to digital for processing and storage. For a discussion of the digitizing process, see Figure 2-20.
T60	5486A/B A7 A3A2-A3A8	ENABLE COUNT causes the Accumulator to count a 20 MHz signal. The number of counts added into the Accumulator when the ADC is finished is proportional to input voltage at that time.
	5486A/B A6 5486A/B A8	INHIBIT STATE turns off the (Summation) program in progress. The digitizing process may require more than the time allowed in one 10 usec program period. If this is the case, the program is inhibited until the appropriate timing signal of the next period. The greater the input voltage, the longer time the digitizing process will take; digitizing small input signals may be accomplished within the time allowed in one program.
T80	5486A/B A6 5486A/B A10 5485A A6	If Analog-to-Digital Conversion (digitizing) process is finished ALLOW STATE enables summation program to continue. If digitizing process is not finished, program is inhibited until T80 of next 10 usec period, when this check is made again. No other program can be performed during this time, because the 5480A will not have finished the (Summation) program it is working on.
	5486A/B A6 5485A A4	Input multiplexer is set to enable next data to be summed to come from the correct channel, as selected by MEMORY SELECTOR switches.
T86	5486A/B A7 5485A A3	Analog-to-Digital Converter is reset
	5486A/B A7 A2A13, A2A7, 8	Contents of Accumulator are written into memory location addressed at T2 of this program

(Cont'd on next page)

Table 2-14. Summation Program (Cont'd)

Timing Signal	Boards	Events
T90	5486A/B A13 5486A/B A3	If Process Address Register output is 0000 Time Base is reset.
T94**	5486A/B A9 5486A/B A8	No Operation Program is set. This provides a "back-up" program, in case none of the other possible programs (Summation, Display, Prepare) is set.
T98*	5486A/B A9 5486A/B A8	Summation Program is set.
	5486A/B A5	Process Address Register is advanced one count if channel is not OK. This keeps the 5480A/B from wasting time at a channel that wasn't selected.
	5486A/B A10 5486A/B A3	Presample and 10 usec A are combined to form START, PROCESS, and SAMPLE signals for next summation program.

*T98 = 10 μsec B
**For 5486A Plug-ins: T94 was T90.

(End)

Table 2-15. Average Program

GENERAL

This program causes the Signal Analyzer to compare the current signal value against the previous (averaged) signal value stored in memory, form a new average value, and store the new value in memory. This program is similar to the Summation Program described in Figure 2-15. In the Average Program, the difference between the input signal and the stored signal is digitized and added to the old signal (digitally).

Some other comparisons between the Average and Summation Programs are:

1. In the Average Program, processed data are shifted right before processing, then are shifted left to the most significant accumulator bit positions before being stored. In the Summation Program, stored data are shifted left before being displayed, then are shifted back to the right for processing and storage, and are stored in the least significant memory bit positions.

2. There is no comparison between memory contents and input signal in the Summation Program.

The Average Program is started (set) only when:

PROCESS START is lighted

and

FUNCTION is set to AVERAGE

and

Process Address Register output is for a selected memory quarter

TIMING

Timing Signal	Boards	Events
T0	5486A/B A9 5486A/B A8 5486A/B A4 A3A1	Average Program begins
	5486A/B A6	Closed loop is enabled, thus an Accumulator shift is, effectively, a rotation
	5486A/B A6 5486A/B A12	Output MPX is set
T2	5486A/B A7 A3A2-A3A8	Accumulator is cleared
	5486A/B A7 A3A2-A3A8	Accumulator right shift is enabled, but not performed at this time
	5486A/B A7 5486A/B A13 A3A12 A3A9-A3A11 A2A14, A2A9	Process Address Register contents are transferred to Horizontal (Address) Hold Register
T4	5486A/B A7 A2A13 A2A7, 8	Contents of addressed memory location are read into accumulator. Memory contents at this address after this operation are all "0"
T12	5486A/B A5 5486A/B A11 5485A A3 5486A/B A2	Mod 24 counter is preset to cause correct number of accumulator shifts, as determined by SWEEP TIME setting

(Cont'd on next page)

Table 2-15. Average Program (Cont'd)

Timing Signal	Boards	Events
T12 (cont)	5486A/B A7 A2A10	Accumulator contents are transferred to Vertical DAC
		One analog output from the DAC is connected as an input to a difference amplifier on 5485A A2. The difference amplifier will compare the input signal against this signal, digitize the difference between them, and thus form a new average in the accumulator.
	5486A/B A5 5486A/B A12 A3A2-A3A8 5486A/B A11	Accumulator right shift begins. Each shift causes the Mod 24 counter to count up one count. Shifting continues until the Mod 24 counter contents equal Shift Hold Register contents. Because each shift is a closed-loop shift, data in the accumulator are not lost, but are rotated to other bit positions. An identical number of closed-loop left shifts would restore the data to their original positions.
	5486A/B A10 A3A12 A3A9-A3A11	Display Address Register is incremented to next address
	5486A/B A13 5486A/B A5 A3A12 A3A9-A3A11	Process Address Register is incremented one count
T16	5486A/B A13 A3A12 A3A9-A3A11	If PROCESS START is lighted and Display Interlace is set to In and Display Address Register output is between 1020 and 1023 Display Address Register is cleared
T34	5486A/B A6 5486A/B A8	INHIBIT STATE turns off the (Average) Program in progress. The digitizing process may require more than the time allowed in one 10 μsec period. If this happens, the program is inhibited until the appropriate timing signal of the next 10 μsec period. The greater the difference between the input signal and the averaged signal in the accumulator, the longer time the digitizing process will take; digitizing small differences may be accomplished within the time allowed in one program. No other program can be performed while the program in progress is being inhibited
	5486A/B A7 A3A2-A3A8	ENABLE COUNT causes the Accumulator to count a 20 MHz signal. The number of counts in the Accumulator when the ADC is finished is proportional to the difference between the input voltage and the value in memory at that time.
	5486A/B A13 A3A12 A3A9-A3A11	If AR MPX output is between 1020 and 1023 and An Average Program was done last Process Address Register is set to 1023

(Cont'd on next page)

Table 2-15. Average Program (Cont'd)

Timing Signal	Boards	Events
T34 (cont)		If
		AR MPX output is between 1020 and 1023
		and
		A Display Program was done last
		Display Address Register is set to 1023
	5486A/B A5 5485A A3 5485A A6 A3A2-A3A8	Start ADC begins digitizing process to convert difference between analog input signal and the averaged signal to digital for processing and storage
T58	5486A/B A6 5486A/B A10 5485A A6	If
		Analog-to-Digital Conversion (digitizing) process is finished
		ALLOW STATE enables Average Program to continue
		If digitizing process is not finished, program is inhibited until T80 of next 10 μsec period, when this check is made again. No other program can be performed during this time, because the 5480A/B will not have finished the (Average) program it is working on.
T60	5486A/B A5 5486A/B A11 5486A/B A3 5486A/B A2	Mod 24 counter is preset (to same number as at T12) to cause correct number of accumulator shifts. In this case, the correct number of shifts results in data being stored in the same memory bits as when this program started. The right shift was provided to provide proper scaling of data for averaging. The left shift enables data to be presented at full value on CRT screen (data are presented when accumulator contents are transferred to Vertical DAC).
	5486A/B A7 A3A2-A3A8	Accumulator left shift restores data bits to their original positions for correct scaling in display. The shift is enabled and performed at this time.
T80	5486A/B A7 5485A A3	Analog-to-Digital Converter is reset
	5486A/B A6 5485A A4	Input multiplexer is set to enable next data to be averaged to come from the correct input channel, as selected by MEMORY SELECTOR switches
T86	5486A/B A7 A2A13 A2A7, 8	Accumulator contents are written into memory location addressed at T2 of this program
T90	5486A/B A13 5486A/B A3	If
		Process Address Register output is 0000
		Time Base is reset
T94*	5486A/B A9 5486A/B A8	No operation Program is set. This provides a "back-up" program, in case none of the other possible programs (Average, Display, Prepare) is set.

*For 5486A Plug-ins: T94 was T90.

(End)

Table 2-16. Histogram Begin Program

GENERAL

This program uses memory locations 1020 through 1023 to keep track of the number of Histograms performed. One of these addresses is incremented each time the Histogram Begin program is performed. Ordinarily, this information is not used, but the 5480A/B system can be modified to compare this number against the PRESET TOTALIZER setting and stop histogramming after a selected number of histogram programs have been performed.

The Histogram Program, after incrementing one of the above memory locations, clears the Process Address Register; because the register is already enabled to count, it begins counting either the input signal pulses or time base pulses until T12 of the Histogram End Program.

There is no display as part of this program.

TIMING

Timing Signal	Boards	Events
T0	5486A/B A10 5486A/B A8	Histogram Begin program starts
	5486A/B A6 A3A12 A3A9-11	Process Address Register is set to 1020, 1021, 1022, or 1023 and enabled to count
T2	5486A/B A7 A2A14 A2A9	Process Address Register contents are transferred to Horizontal (Address) Hold Register; addressing last memory location
	5486A/B A7 A3A2-A3A8	Accumulator is cleared
	5486A/B A5 5486A/B A11	Shift Control (Switch Hold) Register is cleared
T4	5486A/B A7 A2A13 A2A7, 8	Memory contents are read into accumulator
T12	5486A/B A5 5486A/B A6 A3A2-A3A8	Accumulator contents are increased by one count
	5486A/B A6 A3A12 A3A9-A3A11 A3A10	Process Address Register is cleared Par count enable begins
T16	5486A/B A7 A2A13 A2A7, 8	Accumulator contents are written into memory
	5486A/B A5 5486A/B A12 5486A/B A11	Scale number is set from sensitivity multiplier into shift hold register, to provide proper display scaling
T94	5486A/B A9 5486A/B A8	No operation program is set

The next processing program will be Histogram End.

Table 2-17. Histogram End Program

GENERAL

The number of counts received between T12 of the Histogram Begin Program and T12 of the Histogram End Program determines the memory location to be addressed by the Histogram End Program. This program reads contents of the addressed memory location into the accumulator, increments the accumulator contents by one count, and returns the new value to the same memory location. If the accumulator contents equal the number selected by the PRESET TOTALIZER switch, the 5480A/B will automatically switch to the OUTPUT DISPLAY mode, and histogramming will be stopped.

There is no display as part of this program.

TIMING

Timing Signal	Boards	Events
T0	5486A/B A10 5486A/B A8	Histogram End Program begins
T2	5486A/B A7 A3A2-A3A8	Accumulator is cleared
T12	A3A10	PAR COUNT ENABLE ends
T14	5486A/B A7	Process Address Register contents (number of counts, proportional to time or frequency) are transferred to Horizontal Hold Register, addressing one memory location.
T16	5486A/B A7 A2A13 A2A7, 8	Contents of addressed memory location are read into Accumulator
T26	5486A/B A5 5486A/B A6 A3A2-A3A8	Accumulator counts are increased by one count
T30	5486A/B A7 A2A13 A2A7, 8	Accumulator contents are written into memory at addressed location
T80*	5486A/B A7 5485A A3	Analog-to-Digital Converter is reset. This signal was necessary when the possibility of doing Amplitude Histograms was being considered. However, no instruments were produced with this capability, so the signal is not needed.
T90	5486A/B A9 5486A/B A8	If The contents of the addressed memory channel equal the number set by the PRESET TOTALIZER Or The OUTPUT DISPLAY button was pressed The output light is automatically lighted and the display program will be set at T98. Otherwise
	5486A/B A10 5486A/B A8	The Histogram Begin Program will be the next processing program performed again

*Only available in 5486A Plug-ins.

Table 2-18. Multichannel Scaling (MCS) Program

GENERAL

The Multichannel Scaling Program enables the system to display the relative frequency of up to 100 points. At each selected memory location (point), the accumulator counts input pulses for approximately 1/100 of the sweep time per centimeter (2 μsec is lost because of other processing requirements in the MCS program). The number of counts received by the accumulator is equal to the average input frequency times the period the MCS gate is open.

There is a display as part of this program. However, because there is no time in the MCS program to allow the accumulator left and right shifts required for display scaling, the vertical display scale during processing is 2^{21} counts/cm (2^{15} counts are required to produce 1/64 cm deflection); effectively, the SENSITIVITY MULTIPLIER setting is restricted to "0" during MCS processing. Therefore, the display during processing can normally be considered to be just a dot moving across the baseline at the rate selected by the SWEEP TIME control.

TIMING (5480B/5486B ONLY)

The MCS program starts at address 0000 because a Prepare Program is performed when the PROCESS START button is pressed, resetting the Process Address Register to 0000.

Timing Signal	Boards	Events
T0	5486B A10 5486B A8	The MCS Program is set
T2	5486B A7 A3A2-A3A8	Accumulator is cleared
	5486B A7 A2A14 A2A9	Process Address Register contents are transferred to Horizontal Hold Register, addressing location to be processed
T4	5486B A7 A3A2-A3A8	The Accumulator is enabled to count
	5486B A7 A2A13 A2A7, 8	Contents of memory location addressed at T2 of this MCS program are read into the Accumulator
T12	5486B A7 A2A10	Accumulator contents are transferred to Vertical DAC. Note that there was no Accumulator shift before this transfer
	5486B A5	MCS gate is enabled, and counts are added to Accumulator contents until MCS gate closes
T34	5486B A10	Process Address Register contents are increased by one count to next address
T86	5486B A5	If 5480B is processing (not displaying) and FUNCTION switch is set to MCS and Channel addressed at T2 is in a quarter selected by MEMORY SELECT switch, MCS gate closes, ending counting by Accumulator Otherwise, counting continues

(Cont'd on next page)

Table 2-18. Multichannel Scaling (MCS) Program (Cont'd)

Timing Signal	Boards	Events
T90	5486B A7 A2A13 A2A7, 8	If 5480B is processing and FUNCTION switch is set to MCS and Channel addressed at T2 is in a quarter selected by MEMORY SELECT switch, Accumulator contents are written into memory location addressed at T2 of this program Otherwise, counting continues
	5486B A9	If 5480B is processing and FUNCTION switch is set to MCS and Channel addressed at T2 is in a quarter selected by MEMORY SELECT switch and STOP PBH line is active (because PROCESS STOP button was pressed or PRESET SWEEP NUMBER was reached) and PRESAMPLE pulse occurs, Processing stops and PROCESS STOP switch button lights Otherwise, counting continues
T94	5486B A9 5486B A8	No Operation Program is set. This program resets all other programs in the 5486B, and provides a "backup" program in case no other program (Prepare, MCS) is set

The program described above enables MCS processing in selectable memory quarters, halves, or full memory. Processing address is "tested" at T86 and T90; if address after test is not one for a channel in a selected memory quarter, the 5480B continues counting in the MCS program, with the Process Address Register being incremented every 1/100 of the rate of the SWEEP TIME setting until it is in a selected memory quarter. When the PAR reaches a selected memory quarter, all accumulated contents are transferred to that memory location.

TIMING (5480A/5486A ONLY)

The MCS program is made to start at address 0000, because a Prepare Program is performed when the PROCESS START button is pressed, resetting the Process Address Register to 0000.

Timing Signal	Boards	Events
T0	5486A A10	The MCS Program is started
	5486A A8 5486A A7 5486A A5	As the Program begins, the MCS gate is open, and counts are being added to the Accumulator
T2	5486A A5	MCS gate is closed; no more counts are accumulated.
T4	5486A A7	Accumulator contents are transferred to Vertical DAC. CRT is unblanked (see GENERAL, above)
	5486A A7 A2A13 A2A7, 8	Accumulator contents are written into memory

(Cont'd on next page)

Table 2-18. Multichannel Scaling (MCS) Program (Cont'd)

Timing Signal	Boards	Events
T4 (cont)	5486A A13	Process Address Register contents are increased by one count to next address. (If Triangle sweep is used, Process Address Register contents are decreased by one count when dot is moving from right to left.)
	5486A A7 A3A2-A3A8	The Accumulator is enabled to count
T14	5486A A7 A2A14 A2A9	Process Address Register contents are transferred to Horizontal Hold Register, addressing next location to be processed
	5486A A7 A3A2-A3A8	Accumulator is cleared
T16	5486A A7 A2A13 A2A7, 8	Memory contents of newly addressed memory location are read into Accumulator
T26	5486A A5	MCS gate is enabled, and counts are added to Accumulator contents until T2 of next MCS Program.
T90	5486A A9 5486A A8	No Operation Program is set. This provides a "back-up" program, in case none of the other possible programs (MCS, Prepare) are set Occurrence of next program is determined by SWEEP TIME setting.

(End)

Table 2-19. Readout of Memory Contents

The relative values of data stored in memory during the Summation or Average Program determines how much vertical deflection there is for each address, and therefore how big the waveform in the display will be. The value of these contents is determined by the processing program (whether Average or Summation) and the SENSITIVITY switch setting while data was being inputted. In Average, data are shifted to the most significant accumulator bit positions to provide the largest possible display. In Summation, data are counted in at the least significant accumulator bit position and are not shifted before storage. More accumulator shifts are required to be able to see Summation-stored data than for Average-stored data. It is possible to retrieve the voltage value for any point in memory by applying one of the following formulas:

If data was stored in Average:

Display calibration = SENSITIVITY $\div 2^{SM}$

where SENSITIVITY = VOLTS/CM setting of input attenuator during processing

SM = SENSITIVITY MULTIPLIER setting and VERNIER is set to CAL

If data were stored in SUMMATION, the number of counts accumulated depends on:

SWEEP TIME and SENSITIVITY switch settings

Number of times the point was processed

Input signal value each time point was processed

If PRESET/NORMAL is set to PRESET, processing will automatically stop after each point has been processed 2^N times, and display can be calibrated as follows:

Display calibration = SENSITIVITY X $2^{(24-N-R-SM)}$ In V/CM,

where N is the PRESET SWEEP NUMBER (2^N is the number of sweeps performed). Read "N" from the SWEEP NUMBER switch setting.

R is the ADC resolution, and depends on SWEEP TIME switch setting. Use the table below to determine "R".

SWEEP TIME	R (resolution, in bits)
1 msec/cm	5
2 msec/cm	7
Any other setting	9

SM is the SENSITIVITY MULTIPLIER setting

If SM = AUTO, Display Calibration = SENSITIVITY, because the 5480A/B automatically solves the equation above.

In Histogram and MCS processing, the absolute value at each point is meaningful, in addition to the relative scaling of all points in the display. In this case, knowing the number of points each centimeter of deflection represents is useful knowledge.

(Cont'd on next page)

Table 2-19. Readout of Memory Contents (Cont'd)

The vertical display can be calibrated in terms of memory contents as described below. Memory contents are displayed without processing when OUTPUT DISPLAY button is lighted. The SENSITIVITY MULTIPLIER controls the number of left shifts the accumulator performs before data from memory is set into the Vertical DAC for display; the same number of right shifts is performed to restore data to the proper bit memory bit positions after display.

Although the Vertical DAC gives 1/64 cm resolution, the table below must be used to relate memory contents to vertical deflection from a "cleared memory" baseline. With OUTPUT DISPLAY button lighted, set other controls to display the quarter(s) desired.

SENSITIVITY MULTIPLIER SETTING (N)	Memory contents-to-Vertical Deflection (Counts/cm)
0	1,000,000
1	500,000
2	250,000
3	125,000
4	62,500
5	31,250
6	15,625
7	7,813
8	3,906
9	1,953
10	976
11	488
12	244
13	122
14	61
15	31*

*When SENSITIVITY MULTIPLIER is set to 15, data that was stored in bit 23 is shifted (rotated) to bit 14, and can cause 1/64 cm deflection in the display (if bit 23 was a "1").

(End)

Table 2-20. Summation and Average Functions

GENERAL

The block diagram in this figure shows how similar these functions are. Programs that can be performed during processing are:

Process (Summation or Average)

Display (if Display Interlace is set to In)

No Operation (at every address not selected by MEMORY SELECTOR switches)

Prepare

EQUATIONS

The SUMMATION FUNCTION solves the equation

$$S_n = S_{n-1} + I_n$$

The AVERAGE FUNCTION solves the equation

$$A_n = A_{n-1} + \frac{I_n - A_{n-1}}{2^k}$$

Where

S_n and A_n represent memory contents after processing

S_{n-1} and A_{n-1} represent memory contents before processing

I_n represents current value of input signal

2^k is a weighting factor based on number of process sweeps performed; the value of 2^k is always equal to or greater than the number of sweeps performed, but less than twice that number

Number of Process Sweeps Performed	Weighting Factor (2^k)
1	1
2	2
3 or 4	4
5 thru 8	8
9 thru 16	16
17 thru 32	32
etc.	

The slight error that is caused because the weighting factor is not exactly correct for the number of sweeps is almost overcome in the averaging process.

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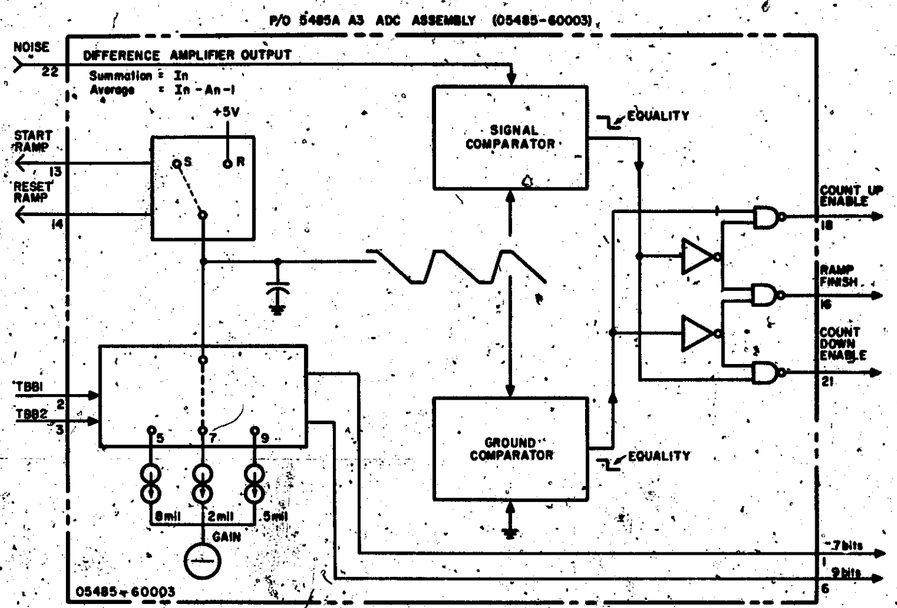
Table 2-20. Summation and Average Functions (Cont'd)



SWITCH TRUTH TABLE

TBBI	TBB2	7bits	9bits
1	0	0	1
1	1	0	1
0	1	1	0
0	0	0	0

PROCESSING

Analog-to-Digital Conversion

The Analog-to-Digital Converter digitizes the difference amplifier output. This signal is available at the rear panel NOISE output, and can be displayed on the 5480A/B CRT by switching the DISPLAY switch for the channel being processed to NOISE. The difference amplifier output is:

I_n in the Summation equation

$I_n - A_{n-1}$ in the Average equation.

Analog-to-Digital Conversion uses a voltage-to-time conversion to control a gate that allows the Accumulator to count 20 MHz from the 5480A/B time base. The time base for digitizing is a voltage ramp that starts at some positive value, and runs down toward some negative value until the digitizing is completed. The time required for digitizing depends on difference amplifier output, negative values require more time than positive values. If the difference amplifier output is more positive than ground, the ramp will equal this voltage before it equals ground, and the Accumulator will be enabled to count up; when the ramp voltage reaches ground, counting will end and the RAMP FINISH signal will be "true". If the difference amplifier output is more negative than ground, the ramp will cross the positive signal region and reach ground before the signal comparator is fired, and the Accumulator will be made to count down from whatever number it contains; counting continues until the ramp voltage equals the signal voltage and the signal comparator fires, ending the digitizing process and making the RAMP FINISH go true.

Resolution

The digitizing process converts voltage to time to gate a 20 MHz signal into the Accumulator. The smallest time interval we can resolve is the period of the 20 MHz signal (0.05 μsec). At 1 msec/cm, because we have 100 points to address, we can spend no longer than 10 μsec at each point or we are warding trouble; therefore, we cannot do an Interlace Display, and every addressed point must be processed. Examination of the timing descriptions for the Summation and Average Programs will show that digitizing must take place in 2.2 μsec (Summation) or 2.4 μsec (Average), because we cannot extend the program into another time frame. During these digitizing times, the maximum number of counts we can place into the Accumulator is 44 or 48; however, these numbers don't fit conveniently into our binary math system, so the ADC ramp slope is selected to allow 32 counts maximum (5-bit resolution). At 2 msec/cm, we can use two 10 μsec time frames for processing without getting into trouble, so a slower ADC ramp can be used, giving us 7 bits of resolution (more counts can be accumulated into the Accumulator to represent the same voltage). At 5 msec/cm and slower sweep speeds, even more time is available, and we use a third (and slowest) ADC ramp, which gives 9-bit resolution.

When accumulator data is shifted (whether manually or automatically) to place the most significant bit in Accumulator bit position 23, you can see (by looking at the diagram in Figure 2-9) that the least significant data bit will cause 1/2 cm of vertical deflection. Thus, in some cases, it is possible to process a dc input signal (including grounded input) and have the CRT display "noise", if the digitizing time is very close to some multiple of 0.05 μsec. In the Average mode, this "noise" is averaged out. In Summation, the BASELINE adjust can be used to offset the dc base line far enough to compensate for this "noise" and provide a smooth 0V baseline when all signals have the same polarity. This resolution can be converted back through the SENSITIVITY switch setting and expressed in terms of voltage; for example, at 50 mV/cm, 1/2 cm resolution corresponds to 25 mV in the 1 msec/cm SWEEP TIME.

EXAMPLES

Example 1

Assume that at one point the input signal has the following levels (in mV):

89, 57, 178, 110, 115, 100, 42, 0, 423, 167, 23, 111, -4, 50, 150, 100

Assume the following control settings

FUNCTION to AVERAGE — SWEEP NUMBER to 4

SWEEP TIME TO 1 msec/cm — SENSITIVITY to 50 mV/cm (0.05 V/cm)

Memory has been cleared, and PROCESS STOP is lighted

Sweep Number (Actual)	Input Data (I_n)	Old Average (Mem contents) (A_{n-1})	Diff Amp Output ($I_n - A_{n-1}$)	ADC Output (min. resolution is 25)	Weighting Factor (2^k)	Correction (Actual)	New Average (A_n)
1	89	0	89	75	1	75	75
2	57	75	-18	0	2	0	75
3	178	75	105	100	4	25	100
4	110	100	10	0	4	0	100
5	115	100	15	0	8	0	100
6	100	100	0	0	8	0	100
7	42	100	-58	-50	8	-6	94
8	0	94	-94	-75	8	-8	86
9	423	86	337	325	16	20	106
10	167	106	61	50	16	3	109
11	23	109	-86	-75	16	-4	105
12	111	105	6	0	16	0	105
13	-4	105	-109	-100	16	-5	100
14	50	100	-50	-50	16	-3	97
15	150	97	53	50	16	3	100
16	100	100	0	0	16	0	100

Example 2

Assume that the input signal is 200 mV high, and is present for only one sweep, and then is removed, while processing continues

Assume the following control settings

FUNCTION to AVERAGE — SWEEP NUMBER to

SWEEP TIME to 1 msec/cm — SENSITIVITY to 50 mV/cm

Sweep Number (actual)	Input Data (I_n)	Old Average (Mem contents) (A_{n-1})	Diff Amp Output ($I_n - A_{n-1}$)	ADC Output (min. resolution is 25)	Weighting Factor (2^k)	Correction (Actual)	New Average (A_n)
1	200	0	200	200	1	200	200
2	0	200	-200	-200	2	-100	100
3	0	100	-100	-100	4	-25	75
4	0	75	-75	-75	4	-18	57
5	0	57	-57	-50	8	-6	51
6	0	51	-51	-50	8	-6	45
7	0	45	-45	-25	8	-3	42
8	0	42	-42	-25	8	-3	39
9	0	39	-39	-25	8	-3	36
10	0	36	-36	-25	8	-3	33
11	0	33	-33	-25	8	-3	30
12	0	30	-30	-25	8	-3	27

(Cont'd on next page)

Table 2-20. Summation and Average Functions (Cont'd)

Sweep Number (Actual)	Input Data (I_n)	Old Average (Mem contents) (A_{n-1})	Diff Amp Output ($I_n - A_{n-1}$)	ADC Output (min. resolution is 25	Weighting Factor (2^k)	Correction (Actual)	New Average (A_n)
13	0	27	-27	-25	8	-3	24
14	0	24	-24	0	8	0	24
15	0	24	-24	0	8	0	24
16	0	24	-24	0	8	0	24

The above example was for a system without noise. For proper interpolation, the RMS value of noise must be greater than or equal to one-half the quantization levels; e.g. 1/4 cm (12.5 mV) in the case of 5-bit resolution, 1/16 cm in the case of 7-bit resolution, and 1/64 cm in the case of 9-bit resolution.

Data Storage

The Average Program causes the Accumulator to shift data so the most significant data bit is in bit position 23 before being written into memory. This causes the Accumulator to always appear to be "full", with additional sweeps increasing resolution by adding bits to the right of bits already in the Accumulator. (Remember, in the Average Program, the Accumulator shifts data to the right, adds in new data, shifts data back to the left, and then this data is stored in memory.)

The Summation Program causes the Accumulator to shift data so the most significant data bit is in bit position 23 before being displayed. In the Summation Program, the Accumulator shifts data to the left, displays it, shifts data back to the right, adds in new data, and this data is stored in Memory.

DATA STORAGE

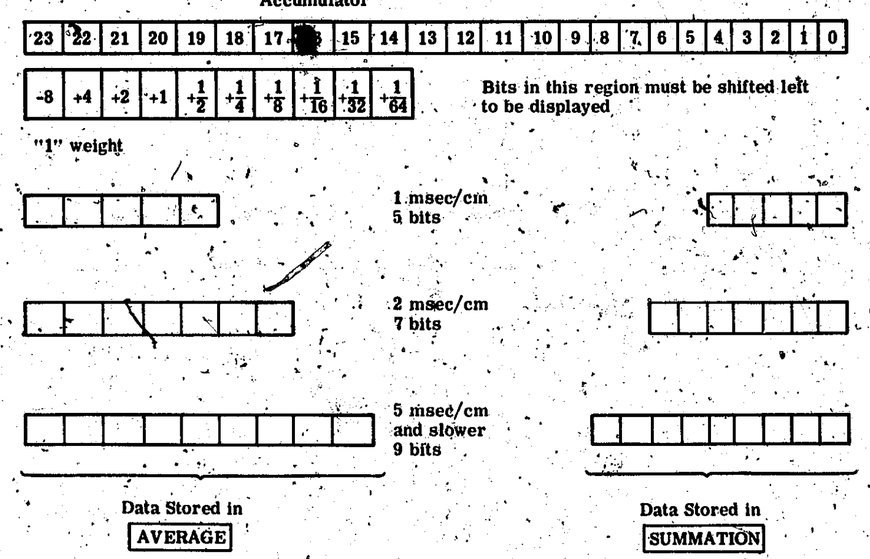


Table 2-20. Summation and Average Functions (Cont'd)

These differences between the Summation and Average programs can be shown by the following demonstration:

Set controls as listed below:

- the 5480A/B to a slow SWEEP TIME (0.5 sec/cm or slower)
- SENSITIVITY MULTIPLIER to AUTO
- FUNCTION to AVERAGE
- SWEEP NUMBER to "0"
- PRESET/NORMAL to PRESET
- Channel A DISPLAY to DATA
- Channel B DISPLAY to OFF
- Channel A SENSITIVITY and VERNIER for convenient display of CALIBRATOR 1V P-P signal.

Connect CALIBRATOR to Channel A INPUT, DC coupled

Press both CLEAR DISPLAY, then PROCESS START

After about 10 seconds, when the processing address has reached the middle of the CRT, switch FUNCTION to SUMMATION. The signal processed in AVERAGE will "disappear", but the signal being processed in SUMMATION will be just as big as the one in AVERAGE was.

At the end of one process sweep, the 5480A/B will switch to the Display mode, and the OUTPUT DISPLAY light will come on.

Remember, the left half of the display represents AVERAGE processing, and the right half represents SUMMATION processing.

In SUMMATION and AUTO and OUTPUT DISPLAY, you will see only the square waves processed in SUMMATION.

In AVERAGE and AUTO and OUTPUT DISPLAY, you will see only the square waves processed in AVERAGE.

In each case, the Accumulator performs the number of closed loop shifts required for proper scaling of data processed in that function (SUMMATION or AVERAGE). Thus, data processed in the other function (AVERAGE or SUMMATION) is not properly scaled to appear on the CRT. This can be proven by switching the SENSITIVITY MULTIPLIER from AUTO to 15 and observing the CRT display. In position "0", regardless of FUNCTION, no Accumulator shifts are performed, so the AVERAGE data (which is already properly positioned) is displayed, while SUMMATION data is not in position to be displayed. As the SENSITIVITY MULTIPLIER number is increased, the Accumulator performs the number of shifts indicated, and finally the SUMMATION data is in Accumulator bits that can be displayed, while AVERAGE data has been rotated so its most significant (sigh) bit can cause only 1/64 cm of deflection.

PROGRAMMING

Process, NOP, Prepare

The Process Address Register starts at address 0000. If this is within one of the selected memory quarters, a Process (Summation or Average) Program will be performed. If this address is not within a selected memory quarter, a NOP Program will be performed. The Process Address Register is then stepped to the next address (0001), and the above process is repeated. When the Process Address Register reaches an address between 1000 and 1007 (on later models, between 1000 and 1019), it is instructed to go to Process Address Register address 1020; the instruction is derived from decoding the address, not from memory contents. If address 1020 is within a selected memory quarter, the 5480A/B will do a Prepare Program, storing in this location the number of times this quarter has been processed. If Address 1020 is not within a selected memory quarter, the 5480A/B

Table 2-20. Summation and Average Functions (Cont'd)

does a NOP Program, and steps the Process Address Register to address 1021, and again checks on whether to do a Prepare or a NOP Program. If the contents of an address between 1020 and 1023 indicate that a PRESET number of process sweeps has been performed, the 5480A/B automatically switches to the Display mode, and processing is ended.

Display, NOP, Prepare

If the 5480A/B is in a Processing mode (PROCESS START lighted), and the Display Interlace is switched In, the Display Program can display contents of any selected memory quarter, except when a point is being processed. The Display Program is never activated in the 1 msec/cm SWEEP TIME setting. In the Processing mode, the Display Address is reset when it gets to address 1000.

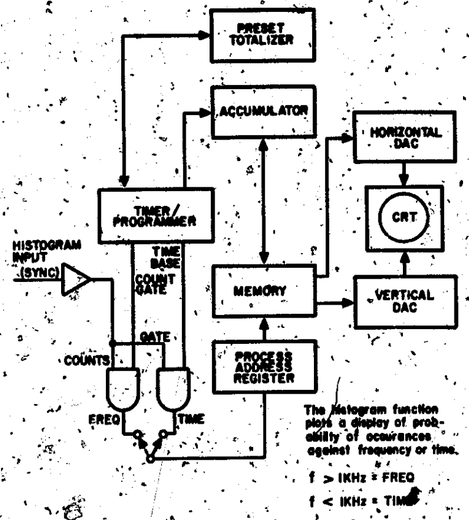
If the 5480A/B is in a Display Mode (OUTPUT DISPLAY lighted), the Display Program will cause all selected memory data points to be displayed. The NOP Program will be performed at all points not selected. When the Display Address Register reaches an address between 1000 and 1007 (1000 and 1019 on later models), it is jumped to the Prepare addresses (1020 to 1023) for proper scaling of the display, according to the SENSITIVITY MULTIPLIER setting.

(End)

Table 2-21. Histogram Function

GENERAL

Histogramming is a sorting process that classifies input signals by some characteristic (frequency, time interval (period),, amplitude). In the 5480A, we can perform frequency or time interval histograms. When the 5480A is set to perform histograms, each memory location represents some frequency or time interval. Each time a histogram is performed, the 5480A measures the frequency or time interval of the input signal and adds one count to the contents of the corresponding memory location.



PROGRAMMING

Every Histogram process required two programs, Histogram Begin and Histogram End, so it takes at least 20 usec to process one point. The signal analysis is performed by having the Process Address Register count

1. the Input signal frequency for a period determined by the SWEEP TIME switch (to make a FREQ HISTOGRAM)
2. the time base frequency, controlled by SWEEP TIME switch, for a period determined by input signal period (for a TIME HISTOGRAM).

In FREQ HISTOGRAMs, the SWEEP TIME switch determines the time between Histogram Begin and Histogram End programs.

In TIME HISTOGRAMs, the input signal determines the time between Histogram Begin and Histogram End programs.

The Display Program can be interlaced during all Histogram processing exeept 1 msec/cm FREQ HISTOGRAMs.

The NOP and Prepare Programs are not used for Histogram functions.

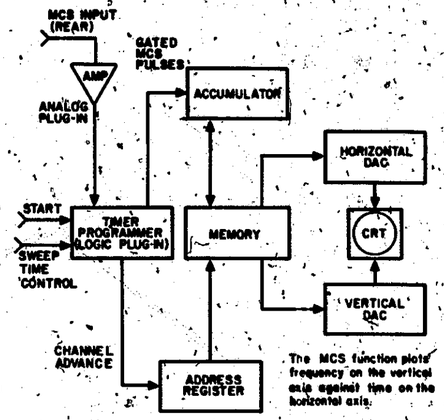
DATA STORAGE

Counts are accumulated in the least significant Accumulator bit position. The Histogram Programs do not shift data in the Accumulator. Data can be scaled for by using the SENSITIVITY MULTIPLIER when Display Interlace is set to In.

Table 2-22. Multichannel Scaling Function

GENERAL

The Multichannel Scaling Function enables the Accumulator to accumulate counts directly from an external input. The only processing that occurs is addition of counts to those already in the accumulator. The number of counts accumulated at each address is independent of signal amplitude.



PROGRAMMING

5480B/5486B Only

Every Multichannel Scaling Process begins with a Prepare Program to set the Process Address Register to address 0000. During MCS processing, a memory location is addressed, its contents read into the Accumulator, and the Accumulator allowed to count for a certain gate time (controlled by the SWEEP TIME switch). The memory address is stored in the Horizontal Hold Register, and the Process Address Register is incremented during the time the Accumulator is counting the input signal. At the end of the gate time, the Accumulator contents are written into the memory at the address in the Horizontal Hold Register, and the program ends. The next MCS program transfers the new number in the Process Address Register to the Horizontal Hold Register, and repeats the program at the newly addressed location.

The Display Program cannot be used during MCS processing, all available time is used for the Processing (MCS), Prepare, and NOP Programs.

5480A/5486A Only

This program is entirely different from the program described above for the 5480B/5486B system.

The Multichannel Scaling process begins with a prepare program that sets the Process Address Register to address 0000. MCS processing begins with the Accumulator counting the MCS input pulses. The SWEEP TIME switch determines when the MCS gate will close and the Accumulator contents be written into Memory, contents of the next address read out, and the MCS gate opened again.

This program does not permit memory sectioning, it requires full 5480A/B memory.

DATA STORAGE

MCS input signals are counted into the accumulator, and then written into memory without shifting. No data shifting is performed during MCS functions.