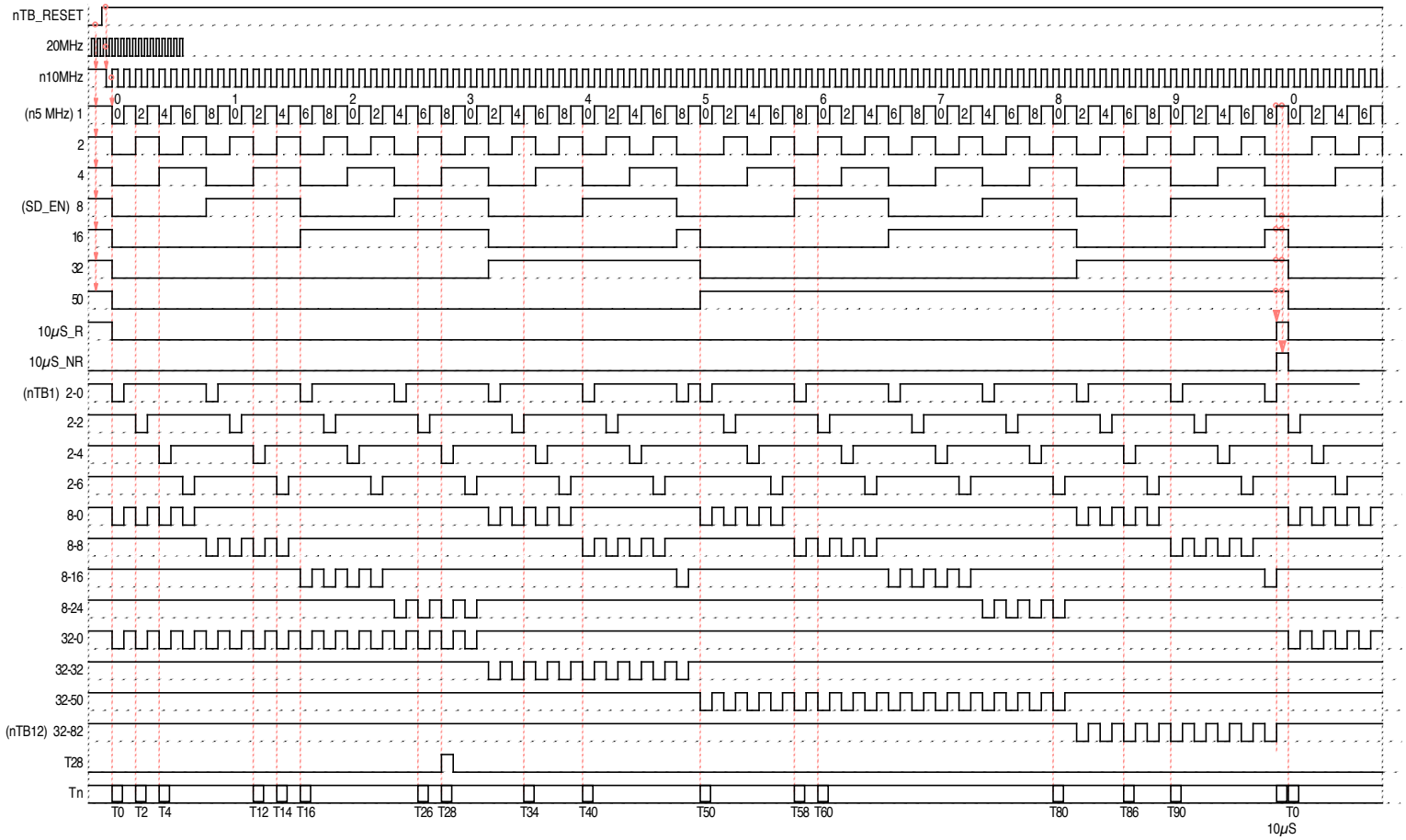
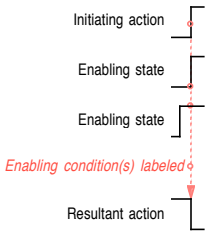


Logic Transition Key

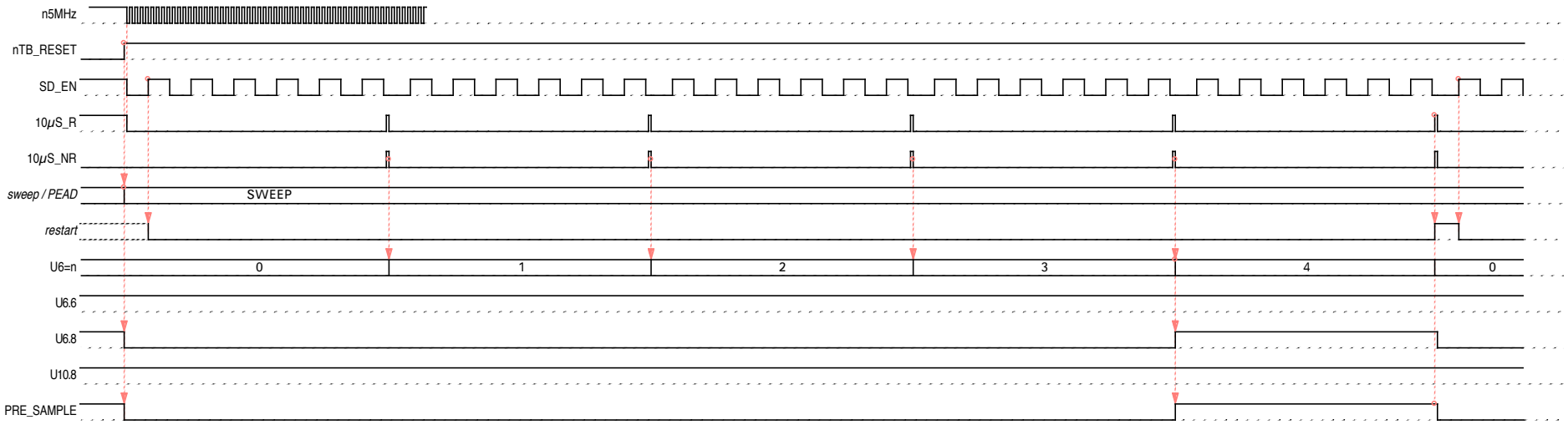


Trigger Slot Timing

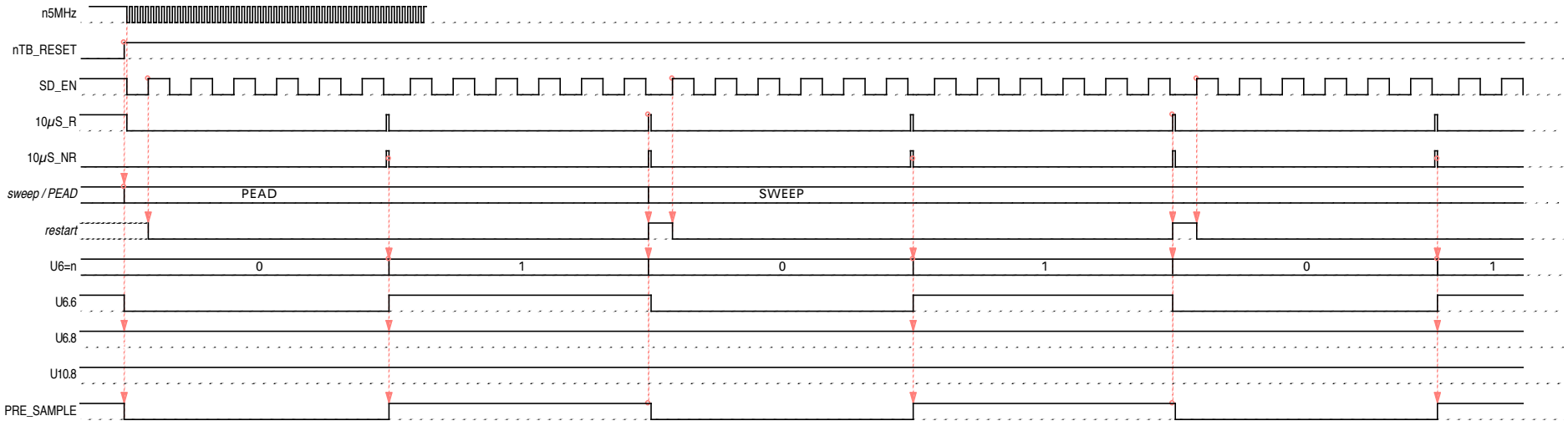
- The diagram presents one 10μS process cycle starting from the release of reset (RESET_TB).

1. The master clock is a 20 MHz crystal oscillator [A2A12].
2. The 20 MHz is divided by a 2-stage binary ripple counter to 5 MHz [86A3U7].
3. The 5 MHz clocks a 6-stage synchronous counter configured for modulus 50 [86A3U8::10]. The final output of this counter is 100 KHz.
4. The 6 stages of the synchronous counter are decoded into 3 groups of 1-of-4 [86A3,nTB1::12].
5. The 3 * 1-of-4 signals are additionally gated by the 5MHz, and fed to a set of 3-input AND gates where each AND gate decodes 1 of 100 distinct time slots. (The 5MHz is the 1-bit of a 7-stage counter clocked at a 10 MHz step rate). [86U4,Tn]

- The timing counters thus define a 10μS / 100KHz processing cycle. The time slots within this cycle trigger various actions during the cycle. Only even-numbered time slots are used as triggers, with the exception of the 10μS triggers at 99.
- Resetting the timing counter sets the synchronous section to all-1s. This is an 'initial' state unique from the states of the normal clocked cycle. The 10μS_R & 10μS_NR signals are distinguished in that R will assert during this initial state (after Reset) while NR does not.



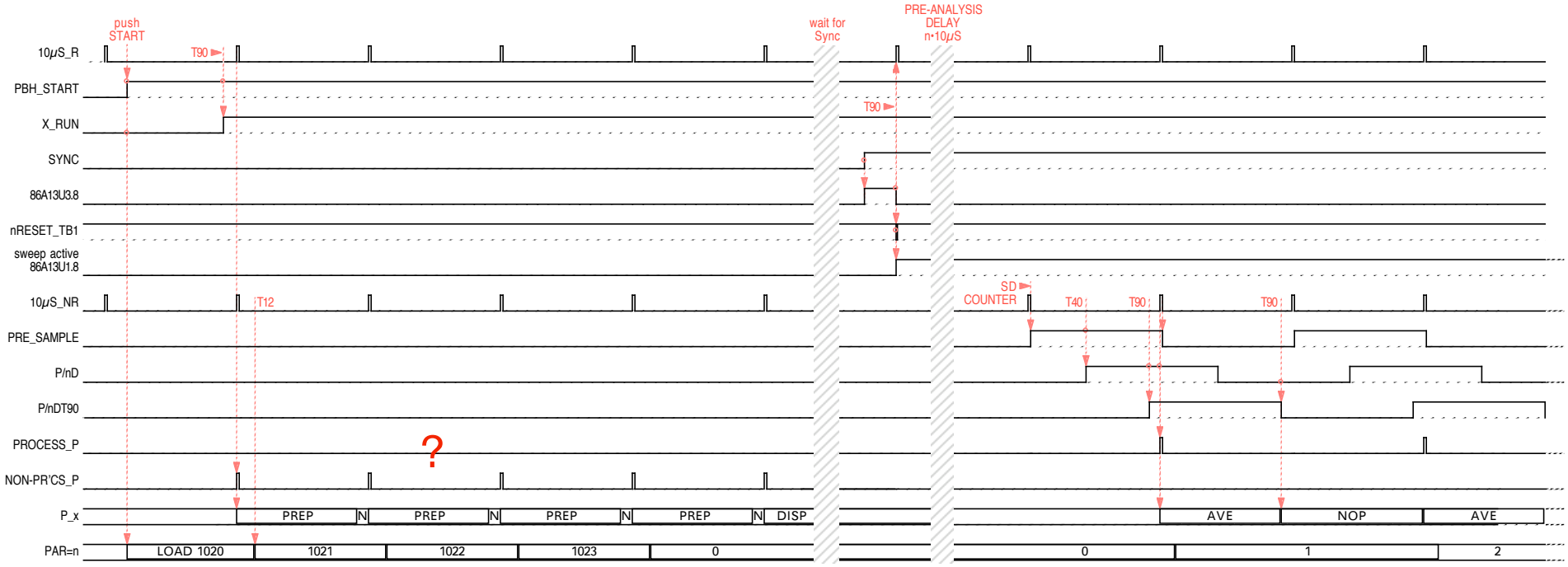
SCENARIO:
PRE-ANALYSIS DELAY = 0μS
SWEEP TIME = 5mS/cm (SAMPLE DELAY = 50μS)



SCENARIO:
PRE-ANALYSIS DELAY = 20μS
SWEEP TIME = 2mS/cm (SAMPLE DELAY = 20μS)

HP 5480A DSA

Section: Sample-Delay Counter Timing Graph
Page: T2 Rendition: 2022 Sep 5



SCENARIO:
FUNCTION = AVE
SWEEP TIME = 2mS (SAMPLE DELAY = 2μS)

HP 5480A DSA

Section: Execution TIming Graph
Page: T3 Rendition: 2022 Sep 5

PRESET SWEEP COUNT LIMIT DETECTION

• An experiment is an analysis of input signals, performed over some number of sweeps. An experiment begins with the clearing of memory and pressing of the START button. Subsequent sync events initiate a sweep. The experiment may be stopped and restarted by pressing of the STOP/START buttons. Completion of the experiment may be arbitrarily determined upon the pressing of the STOP button or by specifying a preset number of sweeps.

• During execution, the number of sweeps performed is tracked by storing a count of sweeps in high addresses of memory (1020:1023). This sweep count is set to 0 when memory was cleared to begin the experiment.

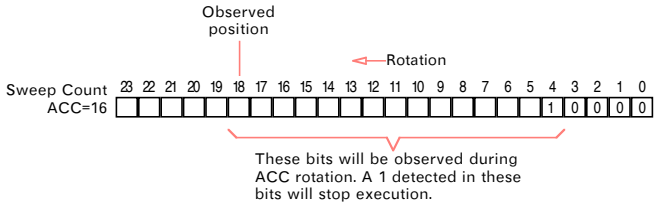
• Prior to a sweep a PREP state micro-cycle is performed. The PREP state is invoked after a pressing of the START button (by starting PAR at 1020), and at the end of a sweep by noting when PAR >=1020.

• During the PREP state, the sweep count is read from memory into ACC, checked against the preset limit, incremented, and written back to memory.

• To check for the preset limit, ACC is rotated left a full 24-bit cycle. As the bits of the sweep count are rotated up, ACC bit 18 is observed during a portion of the shifting to detect a 1 bit. The observed portion is from the start of shifting to 19-SWEEP_NUMBER. These are the bits equal to or greater than the preset limit.

Scenario: SWEEP_NUMBER = 4

The value encoded by the SWEEP_NUMBER switch is 19-4=15. This value is loaded into the SFH for comparison to the SFC. When the SFC reaches this value, observation of bit 18 is disabled, as any 1 bits in the count which might be subsequently detected are less than the preset limit.



PREP STATE TRIGGER SEQUENCE

• The P_PREP state is entered for processing cycles when 1020<=PAR<=1023.

• The Shifter Counter (SFC) is a modulo-24 up-counter.

• SF_START triggers 5 flip-flops:

• SFC Clock Enable:	Set 1. Set 0 when SFC cycles to 0. [U20.11, U20.8, U13.9, U12.8]
• ACC Shift Enable:	Set 1. Set 0 when nPREP and H=C. ACC will be shifted left as SFC is incremented.
• Preset-Limit-Bit Detection Active:	Set 1. Set 0 when Sweep Count setting reached. Observe AC bit 18.
• Preset-Limit-Bit Detected:	Set 0. Set 1 when 1 observed in AC bit 18.
• SWPCNT_STOP:	Set 0. Set 1 to Stop Running, go to Display.

• The setting o the ACC Shift Enale FF initiates shifting left/up of the Accumulator. In the PREP state this shifting is consistent with the SFC cycle, thus – the ACC loop being closed – the Accumulator will make a net full rotation.

• As the bits in ACC move up, if bit 18 becomes non-zero, or SFC reaches 19, U20.6 is set to 1. This also sets SWPCNT_STOP to indicate execution termination due to the sweep count having been reached.

• The Sweep Num switch encodes 19-Limit. If SFC reaches this coded value – as loaded into the Shifter Hold register (SFH) – detection of the ACC bit is disabled by the clearing of U17.6.

• SFC transitions may start at T15 or T16 due to the indeterminate relation of the 5MHz clock for SFC [86A12U13.5] vs TSC.