HEWLETT hp PACKARD

SIGNAL ANALYZER SYSTEM VOL. I
SYSTEM SERVICE MANUAL
PART NO. 05480-90012 (MANUAL)
APRIL 1971

5480A/B
SERIAL PFX ALL SERIALS
05480-90015 (FICHE)
6 of 7

Table 4-2. Wiring Lists (Cont'd)

PART G 5405A (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	INPUT AMPLIFIER A1	SAMPLE AND HOLD	ADC A3	SWITCHING LOGIC A4 OUTPUT AMPLIFIER A5	SWITCHING LOGIC B A6	INTERFACE A7	P25	P26	P27	P28	J22	J23	J24	REMARKS
91	MCS INPUT	P27(49)					3	14		49						From Rear J91 MCS In
92	PLOT	P27(45)					14			45						From Rear J92 Plot
93	LRECORD	P27(40)					21			40				30		From DOF. F. Line 24
94	EXT SAMPLE	P27(15)					10			15						From Rear J4 (Sample In)
95	Z AXIS	P27(41)					Z			41						From Display Line 21
96	SWEEP VOLTAGE	A7(0)					0			23						To Rear J19 Sweep V. Output
97	POS SYNC OUT	A7(1)					1			39						To Rear J8
98	NEG SYNC OUT	A7(7)					7			14						To Rear J7
99	MCS COUNT UP	A7(4)					4	27							2	To LPI Line 90
100	SAMPLE	A7(22)					22	-26							1	To LPI Line 41
101	SEEK	A7(13)					13			44						To Rear Panel J13
5460A Serials Prefixed 052- and below																
79	C.S. ATTACHED	P27(19)			15, S		14			19						From EXT Source J15(u)
Wiring in 5405A not changed																

PART H — 5486A/B Table 4-2 (Cont'd)

This part of the table is divided into two sub-parts. Sub-part H1 lists signal connections for the 5486B; sub-part H2 lists signal connections for the 5486A.

The signal list for the 5486B was derived from the list for the 5486A. Signals that are the same for both the A and B models have the same line reference number. Note, however, that there is not necessarily a line-for-line correspondence between the two lists; in some cases, a signal that appears in the 5486B only may be listed where a signal that was only in the 5486A was "deleted". All signals referenced from other lists (other portions of this table) keep the same reference for A and B models. Blank spaces in the B list occur because of signals that were in the A model only, with no replacement signal in the B model.

Table 4-2. Wiring Lists (Cont'd)

PART H1 5486B CONTROL (LOGIC PLUG IN) Wiring Diagram: Figure 4-12

LINE	SIGNAL NAME	SIGNAL SOURCE	SYNC & DELAY A1	TIME BASE "B" A2	TIME BASE "A" A3	TIME SLOT DECODER A4	LIGHT DRIVER CONTROL A5	LOGIC MATRIX "C" A6	LOGIC MATRIX "A" A7	PROGRAM SELECTOR "B" A8	PROGRAM SELECTOR "A" A9	LOGIC MATRIX "B" A10	SHIFT CONTROL LOGIC "B" A11	SHIFT CONTROL LOGIC "A" A12	LOGIC MATRIX "D" A13	P21	P22	P23	P24	J25		REMARKS
1	+12V	P21(4)	2, B													4						To R1
2	-12V	P21(12)	3, C													12						To R1
3	+5	P21(2)	1, A													2						From M. F. Power Supply
4	GRD	P21(1, 9, 0, 10)	22, 2													1, 9 0, 10						
5	NEG EXT TRIGGER	S5AF(4)	18						D													
6	+EXTRIG LINE	S5AF(6) S5AF(2)	19, 20																			
7	INT. TRIGGER	S5AF(0)	17																			
8	TRIGGER INPUT	S5	4																			From J1 thru S10 & S5
9	TRIGGER LEVEL	R1	5																			
10	COUNT UP PAR C	P22(43)	6											12		43						From MFL Line 212
11	PAD OFF	S7	13																			
12	POST ANAL DELAY	R2	8																			
13	PLUG-IN SYNC CONT	P24(14)	14																14	30		Not Used
14	CHAN A	P24(13)	16																13	30		Not Used
15	$\overline{\text{PADEN}}$	A1(15)	15											13								
16	$\overline{\text{SYNC}}$	A1(21)	21								S			14								
17	PRADX2	S2AF(6)	2																			
18	PRADX5	S2AF(3)	3																			
19	PRADX1	S2AR(15)	4																			
20	PRADX10	S2AR(12)	5																			
21	PRADX100	S2AR(9)	6																			
22	PRADX1K	S2AR(6)	7																			
23	SWTX2	S4AF(2)	B																			
24	SWTX5	S4AF(1)	C																			
25	SWTX1	S4AR(15)	D																			
26	SWTX10	S4AR(12)	E																			
27	SWTX100	S4AR(9)	F																			
28	SWTX1K	S4AR(6)	H																			
29	10mD	A3(16)	T	16					6													
30	10m A	A3(15)	U	16							16											

Table 4-2. Wiring Lists (Cont'd)

PART H1 5486B (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	SYNC & DELAY A1	TIME BASE "B" A2	TIME BASE "A" A3	TIME SLOT DECODER A4	LIGHT DRIVER CONTROL A5	LOGIC MATRIX "C" A6	LOGIC MATRIX "A" A7	PROGRAM SELECTOR "A" A9	PROGRAM SELECTOR "B" A8	LOGIC MATRIX "B" A10	SHIFT CONTROL LOGIC "B" A11	SHIFT CONTROL LOGIC "A" A12	LOGIC MATRIX "D" A13	P21	P22	P23	P24	J25		REMARKS
31	RESET	A3(17)	U	17																		
32	CLEAR	A3(14)	R	14			9															
33	TDD1	A2(L)	L																32	7		To API Line 20
34	TDD2	A2(K)	K																33	8		To API Line 20
35	PRE-SAMPLE A	A2(V)	V	8																		
36	PRE-SAMPLE B	A3(0)		6						K	W											
37	20 MHZ CLOCK	P22(24)		11													24					From MFL Line 19
38	RESET TB 1	A13(P)		10							20			P					30	14		To API Line 90
39	MESL	A13(J)		20										J			46					To Ext Source J16(f)
40	RESET TB2	A6(20)					20															
41	SAMPLE	P24(1)		4															1	26		From MPI Line 109
42	ENABLE EXT TB	S4AR(10)		2															16	31	6	From J15 (HH) J16(HH) Rear
43	10 MHZ CLOCK	A3(J)		J									J						16	41		To API Line 90
44	TB1	A3(L)		L	10																	
45	TB2	A3(M)		M	11																	
46	TB3	A3(N)		N	12																	
47	TB4	A3(P)		P	13																	
48	TB5	A3(R)		R	14																	
49	TB6	A3(S)		S	15																	
50	TB7	A3(T)		T	16																	
51	TB8	A3(U)		U	17																	
52	TB9	A3(V)		V	18																	
53	TB10	A3(W)		W	19																	
54	TB11	A3(X)		X	20																	
55	TB12	A3(Y)		Y	21																	
56	T0	A4(R)			R	5	5	5														
57	T2	A4(F)			F	6	6	6														
58	T4	A4(H)				7	7	7														
59	T12	A4(J)			J	0	0	0			H								10	44		To API Line 10
60	T14	A4(K)			R	0		0														

Table 4-2. Wiring Lists (Cont'd)

PART H1 5400B (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	SYNC & DELAY A1	TIME BASE "B" A2	TIME BASE "A" A3	TIME SLOT DECODER A4	LIGHT DRIVER CONTROL A5	LOGIC MATRIX "C" A6	LOGIC MATRIX "A" A7	PROGRAM SELECTOR "A" A8	PROGRAM SELECTOR "B" A9	LOGIC MATRIX "B" A10	SHIFT CONTROL LOGIC "B" A11	SHIFT CONTROL LOGIC "A" A12	LOGIC MATRIX "D" A13	P21	P22	P23	P24	J25			REMARKS
61	T16	A4(L)			L	10		10						10									
62	T26	A4(M)			M	11		11															
63	T26	A4(N)			N	12		12															
64	T34	A4(P)			P	13	13	13						4									
65	T36	A4(R)			R	14	14	14															
66	T40	A4(S)			S	15	15	15				14											
67	T	A4(T)			T		16	16															
68	T50	A4(U)			U	17	17	17															
69	T60	A4(V)			V	18	18	18															
70	T80	A4(W)			W	19	19	19															
71	T86	A4(X)			X	16		20															
72	T90	A4(Y)			Y	21	21	21		L													
73	START ADC	A5(P)				P											6	44	19				API Line 27 EXT Source
74	PRESET TOTAL 10^0	S3AF(1)			2										15								To MFL Line 133
75	PRESET TOTAL 10^1	S3AF(2)			3										16								To MFL Line 134
76	PRESET TOTAL 10^2	S3AF(3)			4										17								To MFL Line 135
77	PRESET TOTAL 10^3	S3AF(4)			5										18								To MFL Line 136
78	PRESET TOTAL 10^4	S3AF(5)			6										19								To MFL Line 137
79	PRESET TOTAL 10^5	S3AF(6)			7										20								To MFL Line 138
80	SWAVE	S1AF(3)				E	P	3		2								27					To API Line 16
81	DISPLAY	A9(20, X)				X	X	X	20, X														
82	SUM	A9(16, T)				T	T	T	16, T														
83	AVE	A9(15, S)				S	S	S	65, S														
84																							
85	LSTARTA	A10(D)				B		2		D				11			30			5			
86	GENS MULT AUTO	S2BD(13)				4																	
87	EPREPARE	A9(21, Y)				Y	Y	Y	21, Y	R		3	15										
88	HIST BEGIN	A9(16, V)				V	V	V	16, V		18												
89																							
90	MCS COUNT UP	P24(2)				J												2	27				From API Line 99

Table 4-2. Wiring Lists (Cont'd)

PART H1 5400B (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	SYNC & DELAY A1	TIME BASE "B" A2	TIME BASE "A" A3	TIME SLOT DECODER A4	LIGHT DRIVER CONTROL A5	LOGIC MATRIX "C" A6	LOGIC MATRIX "A" A7	PROGRAM SELECTOR "A" A8	PROGRAM SELECTOR "B" A9	LOGIC MATRIX "B" A10	SHIFT CONTROL LOGIC "B" A11	SHIFT CONTROL LOGIC "A" A12	LOGIC MATRIX "D" A13	P21	P22	P23	P24	J25			REMARKS
01	SWMCS	S1AF(7)				D		F		D				L				26	1				
02	MCS	A9(U)				U	U	U	17, U					15									
03	HIST END	A9(10, W)				W	W	W	10, W	N	10												
04	P/$\overline{D}$	A10(E)				C	R	4		12	E												
05	ADVPAR1	A9(E)				F				E													
06	PRESET SHIFT CONT	A5(3)				3						14											
07	START-SHIFT	A5(2)				2									T, Y							Note:	Reset Preset Reached(A12(T1))
08	SET SCALE NUMBER	A5(L)				L									T								
09	CLEAR HOLD	A5(N)				N					13												
100	COUNT UP A	A5(M)				M											9						To MFL Line 20
101	ADVANCE PAR 2	A5(R)				R								U									
102	SWSUM	S1AF(1)					N			3								20	3				Not Used
103	ADCFIN	P24(5)									B								5	30			From API Line 94
104	ADCFIN						M				C												
105	EXTAVE	P23(2)						B									2						
106	EXTPREP	P23(1)						C									1						
107																							
108	ENCLLP & ENCT PAR	A6(B)					B									6, 31				1			To MFL Lines 11,143
109	CLEAR-PAR A	A6(F)					F									38							To MFL Line 153
110	OUTPUT-MPX	A6(D)					D						M				12						To EXT Source J16(2)
111	SET IN MPX	A6(E)					E											36					To API Line 44
112	SET PAR A	A6(C)					C							B		30							To MFL Line 157
113	SET SWEEP NUM	A6(H)					H						6										
114	INHIBIT-STATE						J		M														
115	ALLOW-STATE						K		11														
116	LSTOP	A13(14)					2		12		F	6		14				34	0				Not Used
117	RESET ADC	A7(N)						N										45	20				To API Line 30
118	SETMSB	A7(L)						L									4						To Memory Line 30
119	CYCLE	A7(D)						D									20						To Memory Line 37
120	CLEAR 1	A7(E)						E								7							To MFL Line 12

Table 4-2. Wiring Lists (Cont'd)

PART H1 5400B (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	SYNC & DELAY A1	TIME BASE "B" A2	TIME BASE "A" A3	TIME SLOT DECODER A4	LIGHT DRIVER CONTROL A5	LOGIC MATRIX "C" A6	LOGIC MATRIX "A" A7	PROGRAM SELECTOR "A" A8	PROGRAM SELECTOR "B" A9	LOGIC MATRIX "B" A10	SHIFT CONTROL LOGIC "B" A11	SHIFT CONTROL LOGIC "A" A12	LOGIC MATRIX "D" A13	P21	P22	P23	P24	J25			REMARKS
121	SET VERT	A7(E)						K										5	35	10			API Line 45 Mem Line 25
122	SET HORIZ	A7(D)						M										17					To Mem Line 40
123	ENSHIFT RIGHT	A7(J)						J										3					To MFL Line 7
124	ENSHIFT LEFT	A7(H)						H										2					To MFL Line 5
125	ENABLE COUNT	A7(F)						F										1					To MFL Line 3
126	WRITE	A7(C)						C											10				To Memory Line 35
127	READ	A7(B)						B											18				To Memory Line 33
128	SETAVE	A9(E)							2	F													
129	SETSUM	A9(H)							3	H													
130	SETMCS	A10(10)							4		16												
131	SETHIS BEGIN	A10(12)							5		12												
132	SETHIST END	A10(13)							6		13												
133	SETDUP	A9(C)							7	C													
134	SET-PREPARE	A9(B)							0	B													
135	SETNOP	A9(M)							0	M													
136	STATE ENABLED	A9(10)							10	J	K												
137	CHAN OK	P24(9)				H		R		10	V								9	34			From API Line 61
138	FSD2	P22(40)								9	J						40						From MFL Line 140
139	LDSPLAY	P23(33)								3			K	9				30	30	5			From LD&FF Line 10, to API Line 46
140	SAMPLE	A10(N)								11	N												
141	PROCESS	A10(10)								C	10												
142	NON PROCESS	A10(11)								D	11												
143	START PBH	P23(31)								20			K					31					From LD&FF Line 20
144																							
145	LRECORD	P23(30)								10	P			10				30					From LD&FF Line 23
146	STOP PBH	P23(35)								19								35					From LD&FF Line 26
147	NORMAL	60AF								S			S										
148	PRESET REACHED	A12(U)				20				T			U										From MFL Line 139
149	PRESET TOTAL	P22(21)								P							21						
150	GWHST & FR20MHZ	61AF(5)								13				0					12	37			To MFL Line 10 and API Line 43

Table 4-2. Wiring Lists (Cont'd)

PART H1 5400 (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	SYNC & DELAY A1	TIME BASE "B" A2	TIME BASE "A" A3	TIME SLOT DECODER A4	LIGHT DRIVER CONTROL A5	LOGIC MATRIX "C" A6	LOGIC MATRIX "A" A7	PROGRAM SELECTOR "A" A8	PROGRAM SELECTOR "B" A9	LOGIC MATRIX "B" A10	SHIFT CONTROL LOGIC "B" A11	SHIFT CONTROL LOGIC "A" A12	LOGIC MATRIX "D" A13	P21	P22	P23	P24	J25			REMARKS
151	DISPLAY PBH	P23(33)									16							33					From LD&FF Line 21
152	RECORD PBH	P23(34)									17							34					From LD&FF Line 22
153	L STOP	P23(40)									15				Y			0, 40	15	40			From LD&FF Line 30 to J1S(P)
154	SET-L START	A9(S)									K							26					To LD&FF Line 20
155																							
156	SET-L STOP	A9(W)									W							30					To LD&FF Line 27
157	SET-L DISPLAY	A9(U)									U							3, 20					To LD&FF Line 23, and J1S(U)
158	SET-L RECORD	P23(20)									V							20					To LD&FF Line 25
159	FREQ-HIST.	P24(42)										4							42	17			From API Line 66
160	TIME-HIST	P24(43)										6							43	18			From API Line 67
161																							
162	DISPLAY DEFEAT	P24(37)					10					8							37	12			From API Line 62
163	PROCESS INHIBIT	A13(N)										M			N								
164	ADVANCE PARS	A10(U)										U			17								
165	ADVANCE DAR + 1	A10(R)										R				27							To MFL Line 104
166	START	A10(0)										9							40	15			To API Line 17
167	SC1	A12(9)											J	0									
168	SC2	A12(0)											K	9									
169	SC3	A12(10)											L	10									
170	SC4	A12(11)											M	11									
171	SC5	A12(12)											N	12									
172	SC6	A11(P)											P	13									
173	SC7	A11(R)											R	14									
174	SC8	A11(T)											T	16									
175	SC10	A11(U)											U	17									
176	SC11	A12(10)											V	18									
177	SC12	A12(19)											W	19									
170	SC13	A11(X)											X	20									
170	7 BITS	P24(10)										15							10	35			From API Line 34
169	9 BITS	P24(11)										16							11	36			From API Line 35

Table 4-2. Wiring Lists (Cont'd)

PART H1 5486B (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	SYNC & DELAY A1	TIME BASE "B" A2	TIME BASE "A" A3	TIME SLOT DECODER A4	LIGHT DRIVER CONTROL A5	LOGIC MATRIX "C" A6	LOGIC MATRIX "A" A7	PROGRAM SELECTOR "A" A8	PROGRAM SELECTOR "B" A9	LOGIC MATRIX "B" A10	SHIFT CONTROL LOGIC "B" A11	SHIFT CONTROL LOGIC "A" A12	LOGIC MATRIX "D" A13	P21	P22	P23	P24	J25			REMARKS
181	SWEEP NUM 2^0	S0AF(17)												2									
182	SENS MULT 2^0	S2AF(14)												B									
183	SWEEP NUM 2^1	S0AF(16)												3									
184	SENS MULT 2^1	S2AF(15)												C									
185	SWEEP NUM 2^2	S0AR(18)												4									
186	SENS MULT 2^2	S2AR(12)												D									
187	SWEEP NUM 2^3	S0BF(10)												5									
188	SENS MULT 2^3	S2BF(15)												E									
189	SWEEP NUM 2^3	S0BR(20)												7									
190	$\overline{\text{L DISPLAY}}$	A12(L)												L				11					To EXT source J16($\overline{r}$)
191	$\overline{\text{SHIFT 1}}$	A12(P)												P			8						To MFL Line 14
192	CLAC10 SETAC 10	A12(W)												W			14						To MFL Line 215
193	MAIN SRQ	P23(43)													7			43					From EXT source J16($\overline{k}$)
194	SUB SRQ	P23(44)													8			44					From EXT source J16($\overline{m}$)
195																							
196	AC10	P22(22)												X			22						From MFL Line 96
197	ENABLE PAR TO HOLD	P22(41)													3		41						From MFL Line 150
198	$\overline{\text{PSD1}}$	P22(45)													D		45						From MFL Line 141
199																							
200	RECORD PBM	P23(47)													V			47					From LD&FF Line 10
201	MBSSL	A13(11)													H			46					To memory Line 50
202	NOT ASSIGNED																						NOT ASSIGNED
203	SET DAR B	A13(5)													5		48						To MFL Line 150
204	ENABLE DAR TO HOLD	A13(C)													C		40						To MFL Line 151
205	ADVANCE PAR + 1	A13(T)													T		32						To MFL Line 105
206	ADVANCE PAR - 1	A13(10)													10		35						To MFL Line 107
207	CLEAR DAR A	A13(20)													20		20						To MFL Line 154
208	PEN LIFTER	A13(W)													W			24					To rear J30 (pen lift control)
209	$\overline{\text{SW HIST}}$	A13(F)													F		47	13					To MFL Line 100 To MCM Line 40
210	GO DN 20 MHz DAR CONEN	P22(37)															37, 12						From MFL Line 101 to MFL Line 22

Table 4-2. Wiring Lists (Cont'd)

PART H1 5486B (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	SYNC & DELAY A1	TIME BASE "B" A2	TIME BASE "A" A3	TIME SLOT DECODER A4	LIGHT DRIVER CONTROL A5	LOGIC MATRIX "C" A6	LOGIC MATRIX "A" A7	PROGRAM SELECTOR "A" A8	PROGRAM SELECTOR "B" A9	LOGIC MATRIX "B" A10	SHIFT CONTROL LOGIC "B" A11	SHIFT CONTROL LOGIC "A" A12	LOGIC MATRIX "D" A13	P21	P22	P23	P24	J25			REMARKS
211	GD UP 20 MHz DAR	P22(30)															36, 10						From MFL line 109 to MFL line 16
212	LINE SYNC	P21(3)														3							From pwr supply to S5AF(3-12)
213	$\overline{\text{CAL}}$ ZERO	P23(15)						11										15					
214	RESET HORIZ	A6(12)						12										21					
215	T04	A4(B)				B					5				K								
216	SAMP OUT	A10(L)										L						23					To rear panel J5
217	INH SHFT 1	A11(Y)											Y	H									
218	PEN LIFT RETURN	A13(21)													21			22					

Table 4-2. Wiring Lists (Cont'd)

PART H2 5486A CONTROL (LOGIC PLUG-IN) Wiring Diagram: Figure 4-12

LINE	SIGNAL NAME	SIGNAL SOURCE	SYNC & DELAY A1	TIME BASE "B" A2	TIME BASE "A" A3	PROGRAM SELECTOR "B" A9	LOGIC MATRIX "B" A10	LOGIC MATRIX "B" A19	P21	P22	P24	J25	REMARKS
1	+12V	P21(4)	2, B					4					To R1
2	-12V	P21(12)	3, C					12					To R1
3	+5	P21(2)	1, A	10 c		T		2					From MF power supply
4	GRD	P21 (1, 9 8, 16)	22, 2					1, 9 8, 16					
5	NEG EXT TRIGGER	S5AF(4)	10										
6	+ EXT RIG LINE	S5AF(6) S5AF(2)	19, 20										
7	INT TRIGGER	S5AF(8)	17										
8	TRIGGER INPUT	S5	4										From J1 thru S10 & S5
9	TRIGGER LEVEL	R1	5										
10	COUNT UP PAR C	P22(43)	6					12		43			From MFL Line 242
11	PAD OFF	S7	13										
12	POST ANAL DELAY	R2	8										
13	PLUG-IN SYNC CONT	P23(14)	14								14	30	Not Used
14	CHAN A	P23(13)	16								13	30	Not Used
15	PAD FIN	A1(15)	15					3					
16	SYNC	A1(21)	21			S		M					
17	PRADX2	S6AF(4)	2										
18	PRADX5	S6AF(3)	3										
19	PRADX1	S6AR(15)	4										
20	PRADX10	S6AR(12)	5										
21	PRADX100	S6AR(9)	6										
22	PRADX1K	S6AR(6)	7										
23	SWTX2	S4AF(2)	B										
24	SWTX5	S4AF(1)	C										
25	SWTX1	S4AR(15)	D										
26	SWTX10	S4AR(12)	E										
27	SWTX100	S4AR(9)	F										
28	SWTX1K	S4AR(6)	H										
29	10μsB	A3(12)	T	16		0							
30	10μsA	A3(15)	S	15		15							

Table 4-2. Wiring Lists (Cont'd)

PART H2 5490A (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	TIME BASE "B" A2	TIME BASE "A" A3	TIME SLOT DECODER A4	LIGHT DRIVER CONTROL A5	LOGIC MATRIX "C" A6	LOGIC MATRIX "A" A7	LOGIC MATRIX "B" A10	SHIFT CONTROL LOGIC "A" A12	LOGIC MATRIX "D" A13	P20	P23	P24	J25	REMARKS
31	RESET	A3(17)	U	17												
32	CLEAR	A3(14)	R	14												
33	TBB1	A2(L)	L										32	7		To API Line 20
34	TBB2	A2(K)	K										33	0		To API Line 20
35	PRE-SAMPLE A	A2(V)	V	3												
36	PRE-SAMPLE B	A3(0)	0						W							
37	20MHZ CLOCK	P22(24)	11									24				From MFL Line 10
38	RESET TB 1	A13(P)	10						20		P			39	14	To API Line 90
39	MESL	A13(J)	20								J		40			To EXT Source J16(H)
40	RESET TB 2	A6(20)	21			20										
41	SAMPLE	P24(1)	4											1	26	From API Line 100
42	ENABLE EXT TB	S4AR(10)	2										16	31	6	From J15(HH) J16(HH) rear
43	10MHZ CLOCK	A3(J)	J							J				16	41	To API Line 90
44	TB1	A3(L)	L	10												
45	TB2	A3(M)	M	11												
46	TB3	A3(N)	N	12												
47	TB4	A3(P)	P	13												
48	TB5	A3(R)	R	14												
49	TB6	A3(S)	S	15												
50	TB7	A3(T)	T	16												
51	TB8	A3(U)	U	17												
52	TB9	A3(V)	V	18												
53	TB10	A3(W)	W	19												
54	TB11	A3(X)	X	20												
55	TB12	A3(Y)	Y	21												
56	T0	A4(E)	5	E	5	5	5									
57	T2	A4(F)		F	6	6	6									
58	T4	A4(H)		H	7	7	7				S					
59	T12	A4(J)		J	0	0	0	1	H					19	44	To API Line 10
60	T14	A4(K)		K	9		9									

Table 4-2. Wiring Lists (Cont'd)

PART H2 5486A (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	TIME BASE 'A' A3	TIME SLOT DECODER A4	LIGHT DRIVER CONTROL A5	LOGIC MATRIX "C" A6	LOGIC MATRIX "A" A7	PROGRAM SELECTOR "A" A8	PROGRAM SELECTOR "B" A9	LOGIC MATRIX "B" A10	SHIFT CONTROL LOGIC "B" A11	LOGIC MATRIX "A" A12	LOGIC MATRIX "D" A13	P22	P23	P24	J25		REMARKS
61	T16	A4(L)	L	10		10						18							
62	T26	A4(M)	M	11		11													
63	T28	A4(N)	N	12		12													
64	T34	A4(P)	P	13	13	13						4							
65	T36	A4(R)	R	14	14	14													
66	T40	A4(S)	S	15	15	15			14										
67	T50	A4(T)	T	16	16	16													
68	T58	A4(U)	U	17	17	17													
69	T60	A4(V)	V	18	18	18													
70	T80	A4(W)	W	19	19	19													
71	T86	A4(X)	K	20		20													
72	T90	A4(Y)	Y	21	21	21	L					K							
73	START ADC	A5(P)		P										6	44	192			API Line 27 Ext Source
74	PRESET TOTAL 10^2	S3AF(1)	2											15					To MFL Line 133
75	PRESET TOTAL 10^3	S3AF(2)	3											16					To MFL Line 134
76	PRESET TOTAL 10^4	S3AF(3)	4											17					To MFL Line 135
77	PRESET TOTAL 10^5	S3AF(4)	5											18					To MFL Line 136
78	PRESET TOTAL 10^6	S3AF(5)	6											19					To MFL Line 137
79	PRESET TOTAL 10^7	S3AF(6)	7											20					To MFL Line 138
80	SWAVE	S1AF(3)		E	P	3		2							27				To API Line 16
81	DISPLAY	A8(20, X)		X	X	X	20, X												
82	SUM	A8(16, T)		T	T	T	16, T												
83	AVE	A8(15, S)		S	S	S	15, S												
84	L START	P23(36)							2					36					From LD&FF Line 30
85	LSTART A	A10(D)		B		2			D			11							
86	SENS MULT AUTO	S2BR(13)		4															
87	PREPARE	A8(21, Y)		Y	Y	Y	21, Y	R		S	15								
88	RST BEGIN	A8(18, V)		V	V	V	18, V		18										
89	AMP - RST	P24(41)		H					5						41	16			
90	MCS COUNT UP	P24(2)		J											2	27			From API Line 99

Table 4-2. Wiring Lists (Cont'd)

PART H2 5486A (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	LIGHT DRIVER CONTROL A5	LOGIC MATRIX "C" A6	LOGIC MATRIX "A" A7	PROGRAM SELECTOR "A" A8	PROGRAM SELECTOR "B" A9	LOGIC MATRIX "B" A10	SHIFT CONTROL LOGIC "B" A11	LOGIC MATRIX "A" A12	LOGIC MATRIX "D" A13	P22	P23	P24	J25		REMARKS
91	SWMCS	S1AF(7)	D				7			L							
92	MCS	A8(U)	U	U	U	17, U				15							
93	HIST END	A8(19, W)	W	W	W	19, W	N	19									
94	P/D	A10(E)	C	R			12	E		2							
95	ADV PAR1	A9(E)	F				E										
96	PRESET SHIFT CONT	A5(3)	3					14									
97	START-SHIFT	A5(2)	2						T, Y								Note: Reset Preset reached [A12(T1)]
98	SET SCALE NUMBER	A5(L)	L						F								
99	CLEAR-HOLD	A5(N)	N					13									
100	COUNT UP A	A5(M)	M										9				To MFL Line 20
101	ADVANCE PAR 2	A5(R)	R							U							
102	SWSUM	S1AF(1)		N		3								28	3		Not used
103	ADCFIN	P24(5)					B							5	30		From API Line 84
104	ADCFIN	A10(C)	M				C										
105	EXT AVE	P23(2)	10		B								2				
106	EXT PREP	P23(1)	11		C								1				
107	CS ATTACHED	P23(7)	4										7				From J1500
108	ENCLLP& ENCT PAR	A6(B)	B									8, 31					To MFL Lines 11, 143
109	CLEAR-PAR A	A6(F)	F														To MFL Line 153
110	OUTPUT-MPX	A6(D)	D						M				12				To Ext Source J16(P)
111	SET IN MPX	A6(E)	E											36			To API Line 44
112	SET PAR A	A13(E) A6(C)	C							E		39					To MFL Line 157
113	SET SWEEP SUM	A6(H)	H						6								
114	INHIBIT-STATE		J		M												
115	ALLOW-STATE		K		11												
116	STOP	A13(14)	2		12		F			14				34	9		Not used
117	RESET ADC	A7(N)		N										45	20		To API Line 30
118	SET MEB	A7(L)		L									4				To memory Line 39
119	CYCLE	A7(D)		D									20				To memory Line 37
120	CLEAR 1	A7(E)		E								7					To MFL Line 12

Table 4-2. Wiring Lists (Cont'd)

PART H2 5486A (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	TIME BASE "A" A3	LOGIC MATRIX "A" A7	PROGRAM SELECTOR "A" A8	PROGRAM SELECTOR "B" A8	LOGIC MATRIX "B" A10	SHIFT CONTROL LOGIC "A" A13	LOGIC MATRIX "D" A13	P23	P23	P24	J25	REMARKS
121	SET VERT	A7(K)		K							5	35	10	API Line 45 Mem Line 25
122	$\overline{\text{SET HORIZ}}$	A7(M)		M							17			To Mem Line 40
123	ENSHIFT RIGHT	A7(J)		J						3				To MFL Line 7
124	ENSHIFT LEFT	A7(H)		H						2				To MFL Line 5
125	ENABLE COUNT	A7(F)		F						1				To MFL Line 3
126	$\overline{\text{WRITE}}$	A7(C)		C							19			To Memory Line 35
127	$\overline{\text{READ}}$	A7(B)		B							18			To Memory Line 33
128	$\overline{\text{SET AVE}}$	A9(F)			2	F								
129	$\overline{\text{SET SUM}}$	A9(H)			3	H								
130	$\overline{\text{SET MCS}}$	A10(16)			4		16							
131	$\overline{\text{SET-HIST BEGIN}}$	A10(12)			5		12							
132	$\overline{\text{SET-HIST END}}$	A10(13)			6		13							
133	$\overline{\text{SET DISP}}$	A9(C)			7	C								
134	$\overline{\text{SET-PREPARE}}$	A9(B)			8	B								
135	$\overline{\text{SET NOP}}$	A9(M)			9	M								
136	STATE ENABLED	A8(10)			10	J	K							
137	CHAN OK	P24(9)			10						9	34		From API Line 61
138	$\overline{\text{PSD 2}}$	P22(46)	B		9					46				From MFL Line 140
139	L DISPLAY	P23(33)	E		4			K	9		38	30	5	From LD&FF Line 19, to API Line 46
140	SAMPLE	A10(N)			11	N								
141	PROCESS	A10(10)			6	10								
142	NON PROCESS	A10(11)			7	11								
143	START PBH	P23(31)			20				X		31			From LD&FF Line 38
144	PBH CONTINUE	P23(32)			21						32			
145	L RECORD	P23(39)			18	P			19		39			From LD&FF Line 24
146	STOP PBH	P23(35)			19						35			From LD&FF Line 26
147	NORMAL	S9AF			S									
148	PRESET REACHED	A12(V)			T			V						
149	PRESET TOTAL	P22(21)			P					21				From MFL Line 139
150	SW HIST & EN 20MHZ	S1AF(5)			13				6			12	37	To MFL Line 18 and API Line 42

Table 4-2. Wiring Lists (Cont'd)

PART H2 5486A (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	PROGRAM SELECTOR "B" A9	LOGIC MATRIX "B" A10	SHIFT CONTROL LOGIC "B" A11	SHIFT CONTROL LOGIC "C" A13	LOGIC MATRIX "D" A13	P22	P23	P24	J25	REMARKS
151	DISPLAY PBH	P23(33)	16						33			From LD&FF Line 21
152	RECORD PBH	P23(34)	17						34			From LD&FF Line 22
153	L STOP	P23(40)	15			Y			8, 40	15	40	From LD&FF Line 20 to J16(P
154	$\overline{\text{SET-L START}}$	A9(X)	X						26			To LD&FF Line 29
155	$\overline{\text{SET- L CONTINUE}}$	A9(Y)	Y						27			
156	$\overline{\text{SET-L STOP}}$	A9(W)	W						30			To LD&FF Line 27
157	$\overline{\text{SET-L DISPLAY}}$	A9(U)	U						3, 28			To LD&FF Line 23, and J15(U)
158	$\overline{\text{SET-L RECORD}}$	P23(29)	V						29			To LD&FF Line 25
159	$\overline{\text{FREQ-HIST}}$	P24(42)		4						42	17	From API Line 86
160	$\overline{\text{TIME-HIST}}$	P24(43)		6						43	18	From API Line 87
161	L CONTINUE	P23(37)		3					37			Not used
162	DISPLAY DEFEAT	P24(37)		8						37	12	From API Line 62
163	PROCESS INHIBIT	A13(N)		M		N						
164	$\overline{\text{ADVANCE DAR 3}}$	A10(U)		U		17						
165	ADVANCE DAR + 1	A10(R)		R				27				To MFL Line 181
166	START	A10(9)		9					23	40	15	To API Line 17 & rear panel J5
167	$\overline{\text{SC1}}$	A12(8)			J	8						
168	$\overline{\text{SC2}}$	A12(9)			K	9						
169	$\overline{\text{SC3}}$	A12(10)			L	10						
170	$\overline{\text{SC4}}$	A12(11)			M	11						
171	$\overline{\text{SC5}}$	A12(12)			N	12						
172	$\overline{\text{SC6}}$	A11(P)			P	13						
173	$\overline{\text{SC7}}$	A11(R)			R	14						
174	$\overline{\text{SC9}}$	A11(T)			T	16						
175	SC10	A11(U)			U	17						
176	SC11	A12(18)			V	18						
177	SC12	A12(19)			W	19						
178	$\overline{\text{SC13}}$	A11(X)			X	20						
179	7 BITS	P24(10)	15							10	35	From API Line 34
180	9 BITS	P24(11)	16							11	36	From API Line 35

Table 4-2. Wiring Lists (Cont'd)

PART H2 5486A (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	BDEX CONTROL LOGIC "A" A13 LOGIC MATRIX "B" A13	P22	P23	REMARKS
181	SWEEP NUM 2^0	S8AF(17)	2			
182	SENS MULT 2^0	S2AF(14)	B			
183	SWEEP NUM 2^1	S8AF(16)	3			
184	SENS MULT 2^1	S2AF(15)	C			
185	SWEEP NUM 2^2	S8AR(18)	4			
186	SENS MULT 2^2	S2AR(12)	D			
187	SWEEP NUM 2^3	S8BF(18)	5			
188	SENS MULT 2^3	S2BF(15)	E			
189	SWEEP NUM 2^4	S8BR(20)	7			
190	$\overline{\text{L DISPLAY}}$	A12(L)	L		11	To Ext Source J16(F)
191	$\overline{\text{SHIFT 1}}$	A12(P)	P	8		To MFL Line 14
192	CLAC19 SETAC18	A12(W)	W	14		To MFL Line 215
193	MAIN SRQ	P23(43)	7		43	From Ext Source J16(E)
194	SUB SRQ	P23(44)	8		44	From Ext Source J16(m)
195	SAWTOOTH/ TRIANGLE	P23(9)	10		9	From Rear 86
196	AC19	P22(22)	X	22		From MFL Line 96
197	ENABLE PAR TO HOLD	P22(41)	3	41		From MFL Line 150
198	$\overline{\text{PSDI}}$	P22(45)	D	45		From MFL Line 141
199	COUNT ON PAR C	P22(44)	R	44		From MFL Line 199
200	RECORD PBM	P23(47)	V		47	From LD&FF Line 18
201	MBSSL	A13(11)	H		45	To Memory Line 50
202	Not Assigned					Not Assigned
203	SET DAR B	A13(5)	5	48		To MFL Line 158
204	ENABLE DAR TO HOLD	A13(C)	C	40		To MFL Line 151
205	ADVANCE PAR + 1	A13(T)	T	32		To MFL Line 185
206	ADVANCE PAR - 1	A13(16)	16	35		To MFL Line 187
207	CLEAR DAR A	A13(20)	20	26		To MFL Line 154
208	PEN LIFTER	A13(W)	W		24	To Rear BNC J30 (pen lift contro)
209	$\overline{\text{SW}}$ HBT	A13(F)	F	47	13	To MFL Line 199 To Mem Line 49
210	GD DN 20 MHz DAR CONEN	P22(37)		37, 12		From MFL Line 191 to MFL Line 12

Table 4-2. Wiring Lists (Cont'd)

PART H2 5486A (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	P21	P22	REMARKS
211	GD UP 20 MHz RAR	P22(36)		36, 10	From MFL Line 189 to MFL Line 16
212	LINE SYNC	P21(3)	3		From pwr supply to S5AF(3-42)

PART I — 5487A FOUR CHANNEL INPUT (ANALOG PLUG-IN)

Table 4-2 (Cont'd)

Wiring Diagram: Figure 4-13

This part of the table lists all connections in the 5487A FOUR CHANNEL INPUT (Analog Plug-In) unit.

This list is based on the list for the 5485A (Part C of this table). All signals that are common to both units, and referenced from other lists, have the same line reference number in both lists. Note, however, that there is not necessarily a line-for-line correspondence between the two lists; in some cases, a signal that appears only in the 5487A may be listed where a different signal in the 5485A was listed, because the 5485A signal is not in the 5487A; this explanation also applies to blank spaces in the table, a signal was deleted with no other signal to replace it.

Table 4-2. Wiring Lists (Cont'd)

PART I 5487A (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	A1 FOUR-CHANNEL INPUT AMPLIFIER	A2 SAMPLE AND HOLD	A3 ADC	A4 SWITCHING LOGIC	A5 OUTPUT AMPLIFIER	A6 SWITCHING LOGIC	A7 INTERFACE	P25	P26	P27	P28	J23	J24	REMARKS
1	+12V	P28(4)	9, K										4			From Main Frame
2	-12V	P28(12)	20, X										12			From Main Frame
3	+5V	P28(2, 10)	6F	12, N									2, 10			Also on Pin A1 (14) thru 100
4	GRD	P28(1, 9, 8, 16)	5, E	17, U 19, W			19W	19W					1, 9, 8, 16			From Main Frame
5	+19.5V	P28(6)							11				6			From Memory Regulator
6	-19.5 V	P28(14)			8, J								14			From Memory Regulator
7	INPUT A	A8	11, M													From J1 thru A8
8	INPUT B	A9	14, R													From J2 thru A9
9	INPUT C	A10	17, U													
10	INPUT D	A11	22, Z													
11	D1 DISP MULT	A4(13)			13	V										
12	D2 DISP MULT	A4(14)			14	T										
13	I1 INPUT MULT	A4(15)	8		15											
14	I2 INPUT MULT	A4(16)	7		16											
15	INPUT AMPLOUT	A1(1)	1	1												
16	SWAVE	P25(2)		18						2					27	From LPI Line 80
17	START (T0)	P25(15)		3						15					40	From LPI Line 106
18	STOP (T12)	P25(44)		4, D						44					19	From LPI Line 59
19	VERTICAL DAC	P26(47)		11, M							47					From Mem Line 23 thru 233
20	BASELINE ADJ	R1		13												
21	DCBAL	R2		10, L												
22	+REF	A2(7, H)		7, N												To R4 & R6
23	-REF	A2(8, J)		8, J												To R6 A&B Balance
24	NOISE SIGNAL	A2(22, Z)		22	22, Z	B						25				To Rear Panel J6
25	SAMPLED SIGNAL	A2(6)		6		A										
26	DATA SIGNAL	A2(14)		14		C										
27	START ADC	P25(19)			13, P		13			19				6	44	From LPI Line 73
28	TBR1	P25(7)			2, B					7					32	From LPI Line 33
29	TBR2	P25(8)			3, C					8					33	From LPI Line 34
30	RESET ADC	P25(20)			14					20					45	From LPI Line 117

Table 4-2. Wiring Lists (Cont'd)

PART I 5487A (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	A3 ADC	A4 SWITCHING LOGIC	A5 OUTPUT AMPLIFIER	A6 SWITCHING LOGIC	P25	P26	P27	J12	J24	REMARKS
31	RAMP FIN	A3(16)	16		16							
32	COUNT DN ENABLE	A3(21)	21		21		42	42		13, 12		MFL 191 LPI 210
33	COUNT UP ENABLE	A3(18)	18		R		17					To MFL Line 189
34	7 BITS	A3(1, A)	1, A		10	35					10	To LPI Line 179
35	9 BITS	A3(6, F)	6, F		11	36					11	To LPI Line 180
36	$\overline{SAAR1}$	P27(43)		S				43				From Memory Line 123
37	$\overline{SBAR1}$	P27(22)		V				22				From Mem Line 122
38	$\overline{SBAR0}$	P27(42)		Y				42				From Mem Line 124
39	$\overline{SAAR0}$	P27(21)		Z				21				From Mem Line 125
40	CHANNEL COMMAND	P27(18)		F				18	$\overline{5}$			From EXT Source
41	$\overline{AR0}$	P26(14)		1			14					From MFL Line 193
42	$\overline{AR1}$	P26(39)		2			39					From MFL Line 194
43	HISTO-GRAM	P25(37)			4	37						From EXT Data J12(24)
44	SET IN MPX	P25(11)		22		11					36	From LPI Line 111
45	SET DISP MULT	P25(10)		21		10					35	From LPI Line 121
46												
47	"A" ON/OFF	S4		3								
48	"B" ON/OFF	S5		4								
49	"C" ON/OFF	S6		5								
50	"D" ON/OFF	S7		6								
51	DISP SW DATA	S3AF(9)		A								
52	DISP SW NOISE	S3AF(10)			E							
53	DISP SW INPUT	S3AF(11)			D							
54												
55												
56												
57												
58												
59												
60												

Table 4-2. Wiring Lists (Cont'd)

PART I 5487A (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	A4 SWITCHING LOGIC	A5 OUTPUT AMPLIFIER	A6 SWITCHING LOGIC	A7 INTERFACE	P25	P26	P27	J15	J16	J23	J24	REMARKS
61	CHAN OK	A4(11)	11			34							9	To LPI Line 137
62	DISPLAY DEFEAT	A4(B)	B			12							37	To LPI Line 162
63	$\overline{MAAR1}$	GND				40			WIRED TO GND					To Memory Line 133
64	$\overline{MBAR1}$	GND				41			WIRED TO GND					To Memory Line 132
65	$\overline{MBAR0}$	GND					15							
66	$\overline{MAAR0}$	GND					16							
67														
68														
69														
70	"A" GAIN	A8R10		J										
71	"A" POSITION	R4		L										
72	"B" GAIN	A9R10		R										
73	"B" POSITION	R5		S										
74	"C" GAIN	A10R10		2										
75	"C" POSITION	R6		1										
76	"D" GAIN	A11R10		M										
77	"D" POSITION	R7		P										
78	VERT DE-FLECTION	A5(21)		21			49							To Disp Sect & Vert Scope Out
79	C.S. AT-TACHED	P27(19)		Z				19				7		From EXT Source
80	10 MHZ CLOCK	P25(41)			V	41							16	From LPI Line 43
81	TIME HIS-TOGRAM	S2		3										
82	FREQ HIS-TOGRAM	S2		1										
83	L STOP	P25(40)		6		40							15	From LPI Line 153
84	$\overline{ADC\ FIN}$	A6(22)		22		30							5	To LPI Line 103
85	ENABLE COUNT UP A	A6(15)		15			33							To MFL Line 21
86	$\overline{FREQ\ HIST}$	A6(8)		S		17							42	To LPI Line 159
87	$\overline{TIME\ HIST}$	A6(T)		T		18							43	To LPI Line 160
88	VARIANCE OUTPUT	A6(Y)		Y				46						To J32(Rear) Variance Out
89	HORIZ DAC	P26(44)			10		44							From Mem Line 42 to Rear Panel J9
90	RESET TB1	P25(14)			2	14							39	From LPI Line 38

Table 4-2. Wiring Lists (Cont'd)

PART I 5487A (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	A7 INTERFACE	P28	P27	J28	J24	REMARKS
91	MCS INPUT	P27(49)	3		49			From Rear J31 MCS In
92	PLOT	P27(45)	14		45			From Rear J14 Plot
93	L RECORD	P27(40)	21, Y		40	39		From L. DR Line 24
94	EXT. SAMPLE	P27(15)	18		15			From Rear J4(Sample In)
95	Z AXIS	P27(41)	Z		41			From Display Line 21
96	SWEEP VOLTAGE	A7(8)	8		23			To Rear J19 Sweep V Output
97	POS SYNC OUT	A7(1)	1		39			To Rear J8
98	NEG SYNC OUT	A7(7)	7		14			To Rear J7
99	MCS COUNT UP	A7(4)	4	27		2		To LPI Line 90
100	SAMPLE	A7(23)	22	26		1		To LPI Line 41
101	SEEK	A7(13)	13		44			To Rear Panel J13

PART J — 5488A AVERAGE/CORRELATION INPUT (ANALOG PLUG-IN) Table 4-2 (Cont'd)

Wiring Diagram: Figure 4-14

This part of the table lists all connections in the 5487A AVERAGE/CORRELATION INPUT (Analog Plug-In) unit.

This list is based on the list for the 5485A (Part C of this table). All signals that are common to both units, and referenced from other lists, have the same line reference number in both lists. Note, however, that there is not necessarily a line-for-line correspondence between the two lists; in some cases, a signal that appears in the 5488A may be listed where a different signal was listed for the 5485A, because the 5485A signal is not in the 5488A; this explanation also applies to blank spaces in the table, a signal was deleted with no other signal to replace it.

In most cases, this list also applies directly to the H01-5485A.

Table 4-2. Wiring Lists (Cont'd)

PART J 5488A (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	A1 INPUT AMPLIFIER	A2 FAST ADC	A3 COOR. COEF. GEN.	A4 RAMP-HOLD-DIFF. AMPL.	A5 ADC	A6 SWITCHING LOGIC A	A7 OUTPUT AMPLIFIERS	A8 SWITCHING LOGIC B	A9 INTERFACE	P25	P26	P27	P28	J13	J22	J24	REMARKS
1	-12V	P28(4)	9,K											4					From Main Frame
2	-12V	P28(12)	20,X							20,X				12					From Main Frame
3	-5V	P28(2, 10)	12,N											2, 10					Also on Pin A1(14) Thru 100N
4	GRD	(1, 9 P28 8, 16)	17, U 19, W	2, 14 17, 21	19, W	17, U 19, W	17, U 19, W	19, W	17, U 19, W	17, U 19, W	19, W			7, 9 8, 16					From Main Frame
5	+19.5V	P28(6)												6					From Main Frame
6	-19.5V	P28(14)				8								14					From J1 Thru A9
7	INPUT A	A10	14,R																From J2 Thru A9
8	INPUT B	A11	18,V																
9	CORRE-LATION	S7	5,E		2,B														
10	-5VREF	A1(15,S)	15,S																To S1, 2, 4, 5, 7, 8
11	SAMPLE INTERVAL	A1 (1,A)	1,A	7															From MFL Line 193
12	PRODUCT	A3(18)		18	8,J														From MFL Line 194
13																			From Ext Data J12(24)
14	CHAN "A"	16(10)	5,F				10											36	From LPI Line 111
15	INPUT AMPL OUTPUT	A1 (22Z)	22,Z	22	1													36	From LPI Line 121
16	SWAVE	P25(2)			18,V					2								30	From LPI Line 139
17	START (T0)	P25(15)	3,B		3,C					15									From "A" Display SW
18	STOP (T12)	P25(44)			4,D					44									From "A" Display SW
19	VERTICAL DAC	P26(47)			11,M		1				47								From "A" Mem Select
20	BASELINE ADJ	R1			15,S														From "A" Mem Select
21	DC BAL	R2			7,H														From "A" Mem Select
22	-REF	A4(10, L)													To Front Panel Controls				From "A" Mem Select
23	-REF	A4(5, E)													To Front Panel Controls				To R8A+B Balance
24	NOISE SIGNAL	A4(22, Z)			22, Z	22	9				35								From "B" Display SW
25	SAMPLED SIGNAL	A4(6, F)			6, F		2												To Rear Panel J8
26	DATA SIGNAL																		From "B" Mem Select
27	START ADC	P25, (19)				13		13		19						6	44		From "B" Mem Select
28	TBB1	P25(7)				9				7							33		From "B" Mem Select
29	TBB2	P25(8)				10				8							33		From "B" Mem Select
30	RESET ADC	P25(20)				14				20							45		From LPI Line 34
																			From LPI Line 117

Table 4-2. Wiring Lists (Cont'd)

PART J 5488A (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	A1 INPUT AMPLIFIER	A2 FAST ADC	A3 COOR. COEF. GEN.	A4 RAMP-HOLD-DIFF. AMPL.	A5 ADC	A6 SWITCHING LOGIC A	A7 OUTPUT AMPLIFIERS	A8 SWITCHING LOGIC B	A9 INTERFACE	P25	P26	P27	P28	J16	J22	J23	J24	REMARKS
31	RAMP PIN	A5(16)					16			16										
32	COUNT DN ENABLE	A5(21)					21			21			42					37, 12			MFL 191 LPI 210
33	COUNT UP ENABLE	A5(18)					18			R			17					36, 10			To MFL Line 189
34	7 BITS	A5(1)					1			10		35								10	To LPI Line 179
35	9 BITS	A5(6)					6			11		36								11	To LPI Line 180
36	SAARI	P27(43)						S					43								From Mem Line 123
37	SBARI	P27(22)						R					22								From Mem Line 122
38	SBAR0	P27(42)						15					42								From Mem Line 124
39	SAAR0	P27(21)						14					21								From Mem Line 125
40	CHANNEL COMMAND	P27(18)						T					18			E					From Ext Source
41	AR0	P26(14)						E					14								From MFL Line 193
42	AR1	P26(39)						F					39								From MFL Line 194
43	HISTO-GRAM	P25(37)						U		4		37									From Ext Data J12(24)
44	SET IN MPX	P25(11)						M				11								36	From LPI Line 111
45	SET VERT	P25(10)						L				10								36	From LPI Line 121
46	L DISPLAY	P25(5)						J				5								30	From LPI Line 139
47	A OFF	S1AF($1\frac{1}{2}$)						13													From "A" Display SW
48	A DATA SIGNAL	S1AF($5\frac{1}{2}$)						V													From "A" Display SW
49	DA	S2CF(3)						5													From "A" Mem Select
50	CA	S2CF(1)						6													From "A" Mem Select
51	BA	S2BF(3)						7													From "A" Mem Select
52	AA	S2AF(1)						8													From "A" Mem Select
53	EA	S2DF(7)						22													From "A" Mem Select (O'Lap)
54	"B" OFF	S4AF($1\frac{1}{2}$)						20													From "B" Display SW
55	"B" DATA SIGNAL	S4AF($5\frac{1}{2}$)						18													From "B" Display SW
56	DB	S5CF(3)						1													From "B" Mem Select
57	CB	S5CF(1)						2													From "B" Mem Select
58	BB	S5BF(3)						3													From "B" Mem Select
59	AB	S5AF(1)						4													From "B" Mem Select
60	EB	S5DF(7)						21													From "B" Mem Select (O'Lap)

Table 4-2. Wiring Lists (Cont'd)

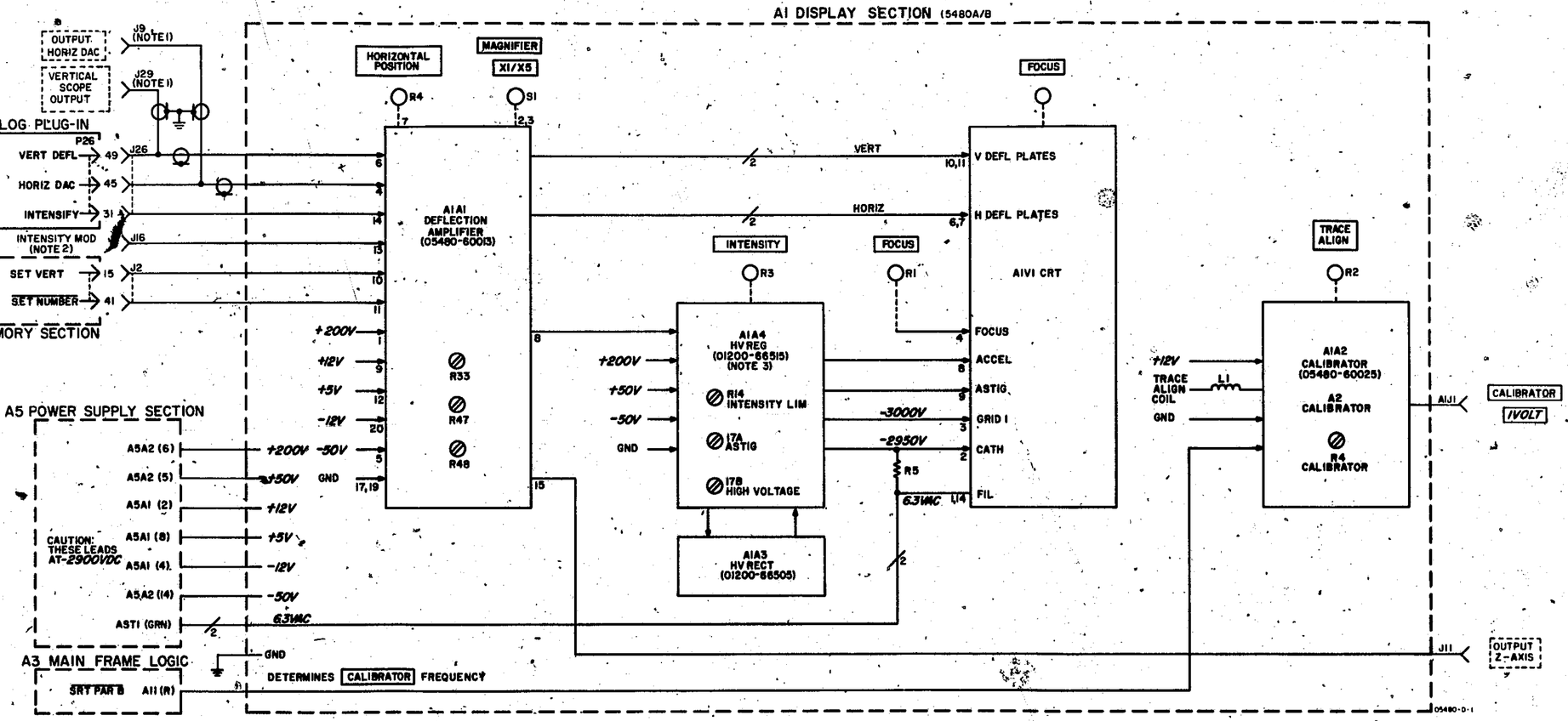
PART J 5488A (CONT'D)

LINE	SIGNAL NAME	SIGNAL SOURCE	A1 INPUT AMPLIFIER	A2 FAST ADC	A3 COOR. GEN. COEF. GEN.	A4 SAMP-HOLD DIFF. AMPL.	A5 ADC	A6 SWITCHING LOGIC A	A7 OUTPUT AMPLIFIER	A8 SWITCHING LOGIC B	A9 INTERFACE	P25	P26	P27	P28	J15	J16	J22	J23	J24	REMARKS
61	CHAN OK	A6(H)					H				34									9	To LPI Line 137
62	DISP DEFEAT	A6(21)					21				12	B								37	To LPI Line 162
63	$\overline{MAARI}$	A6(A)					A					40									To Memory Line 133
64	$\overline{MBARI}$	A6(B)					B					41									To Memory Line 132
65	$\overline{MBARO}$	A6(C)					C					15									To Memory Line 130
66	$\overline{MAARO}$	A6(D)					D					16									To Memory Line 131
67	OVERLAY	A6(16)					16	16													
68	SEG	A6(17)					17	8													
69	A DISP	A6(P)					P	13													
70	"A" NOISE SIGNAL	S1AF(7 1/2)						A													From "A" Display SW
71	"A" INPUT SIGNAL	S1AF(3 1/2)						B													From "A" Display SW
72	"B" NOISE SIGNAL	S4AF(7 1/2)						D													From "B" Display SW
73	"B" INPUT SIGNAL	S4AF(3 1/2)						E													From "B" Display SW
74	"A" VERNIER	A10R10						H													
75	"A" POSITION	R5						L													
76	"B" VERNIER	A11R10						J													
77	"B" POSITION	R6						M													
78	VERT DEFL	A7(18)						18					49								To Disp Sect & Vert Scope Out
79	C.S. ATTACHED	P27(19)				15,S		14						19			H			7	From Ext Source
80	10 MHZ CLOCK	P25(41)							V		41									16	From LPI Line 43
81	TIME HISTOGRAM	80							3												
82	FREQ HISTOGRAM	80							1												
83	L STOP	P25(40)							6		40									15	From LPI Line 153
84	ADC PIN	A8(22)							22		30									5	To LPI Line 103
85	ENABLE COUNTER A	A8(15)							15			33				J					To MFL Line 31
86	TRIG SET	A8(S)							S		17									43	To LPI Line 150
87	TRIG RST	A8(T)							T		18									43	To LPI Line 160
88	VARIANCE OUTPUT	A8(Y)							Y				46								To J22 (Rear) Variance Out
89	HORIZ DAC	P26(44)								10		44									From HPIB Line 43 to Rear Panel J8
90	RESET TRI	P25(14)								2	14									20	From LPI Line 36

Table 4-2. Wiring Lists (Cont'd)

PART J 5488A (CONT'D)

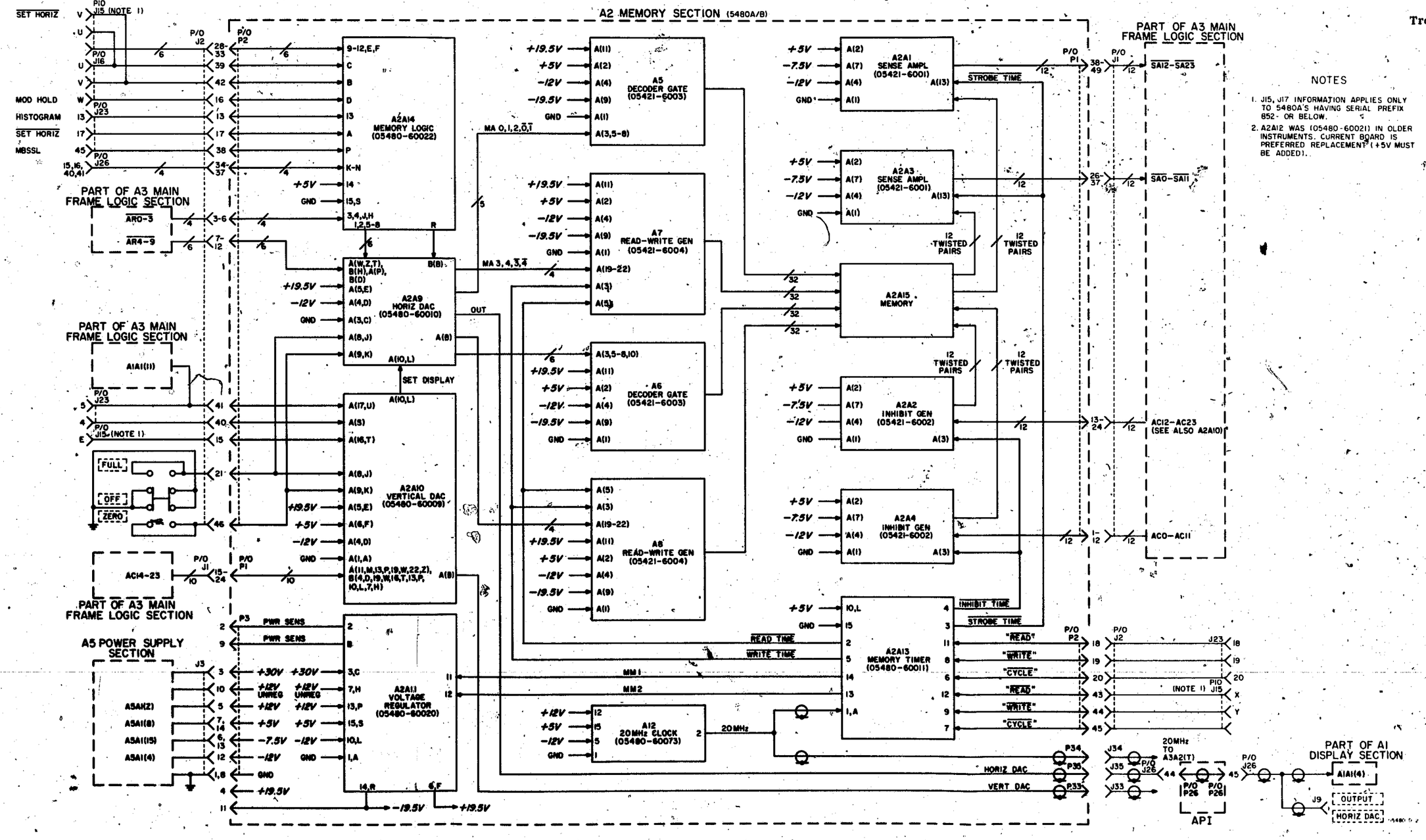
LINE	SIGNAL NAME	SIGNAL SOURCE	A1 INPUT AMPLIFIER	A2 FAST ADC	A3 COOR. GEN. COEF. GEN.	A4 SAMP-HOLD DIFF. AMPL.	A5 ADC	A6 SWITCHING LOGIC A	A7 OUTPUT AMPLIFIER	A8 SWITCHING LOGIC B	A9 INTERFACE	P25	P26	P27	P28	J22	J23	J24	REMARKS
91	MCS INPUT	P27(49)									3			49					From Rear J31 MCS In
92	PLOT	P27(45)									14			45					From Rear J14 Plot
93	L RECORD	P27(40)									21			40			39		From L. DR Line 24
94	EXT SAMPLE	P27(15)									18			15					From Rear J4(Sample In)
95	Z AXIS	P27(41)									Z			41					From Display Line 21
96	SWEEP VOLTAGE	A9(8)									8			23					To Rear J16 Sweep V. Output
97	POS SYNC OUT	A9(1)									1			39					To Rear J8
98	NEG SYNC OUT	A9(7)									7			14					To Rear J7
99	MCS COUNT UP	A9(4)									4	27						2	To LPI Line 90
100	SAMPLE	A9(23)									22	26						1	To LPI Line 41
101	SEEK	A9(13)									13			44					To Rear Panel J13
102	BIT NO. 1	A2(4, D)		4, D		2, 4													
103	BIT NO. 2	A2(15, S)		15, S		1, 3													
104	BIT NO. 3	A2(16, T)		16, T		5, 16													
105	BIT NO. 4	A2(13, P)		13, P		6, 13													
106	START	A1(6, J)																	Not Used
107	POINT NO. 1	A1(4, D)																	Not Used



NOTES

1. J9 AND J29 CAN BE USED AS INPUTS TO DISPLAY SECTION WHEN PLUG-INS ARE REMOVED.
2. CAN BE USED AS INTENSITY MODULATION INPUT AT ANY TIME.
3. A1A4 WAS (01200-66506) IN OLDER INSTRUMENTS, THE CURRENT BOARD IS A DIRECT REPLACEMENT FOR THE OLDER ONE.

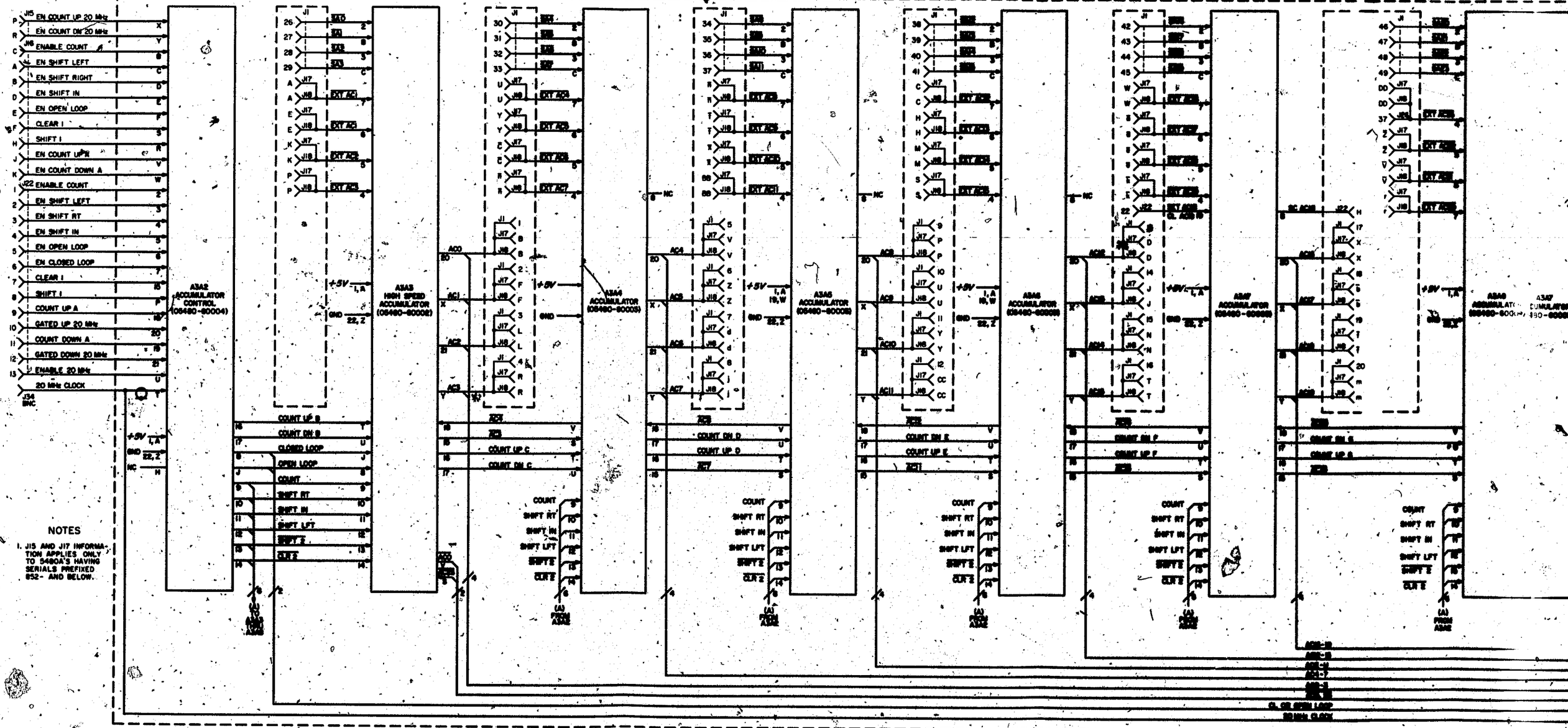
Figure 4-7
5480A/B (Display Section A1)
Wiring List: Table 4-2, Part B



NOTES

1. J15, J17 INFORMATION APPLIES ONLY TO 5480A'S HAVING SERIAL PREFIX 852- OR BELOW.
2. A2A12 WAS (05480-60021) IN OLDER INSTRUMENTS. CURRENT BOARD IS PREFERRED REPLACEMENT (+5V MUST BE ADDED).

Figure 4-8
5480A/B (Memory Section A2)
Wiring List: Table 4-2, Part C



NOTES

1. J15 AND J17 INFORMATION APPLIES ONLY TO 5480A'S HAVING SERIALS PREFIXED 852- AND BELOW.

02850-1

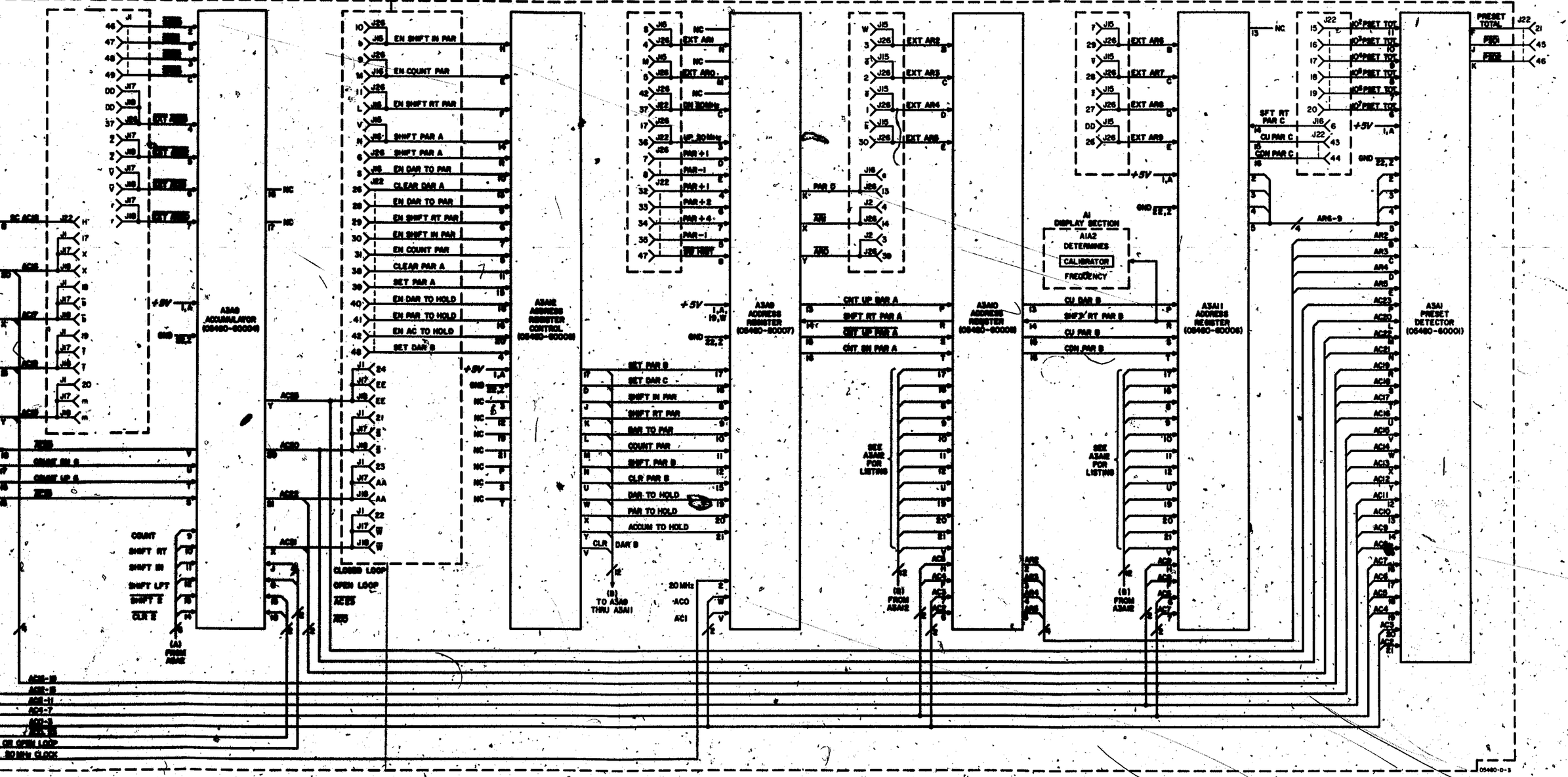
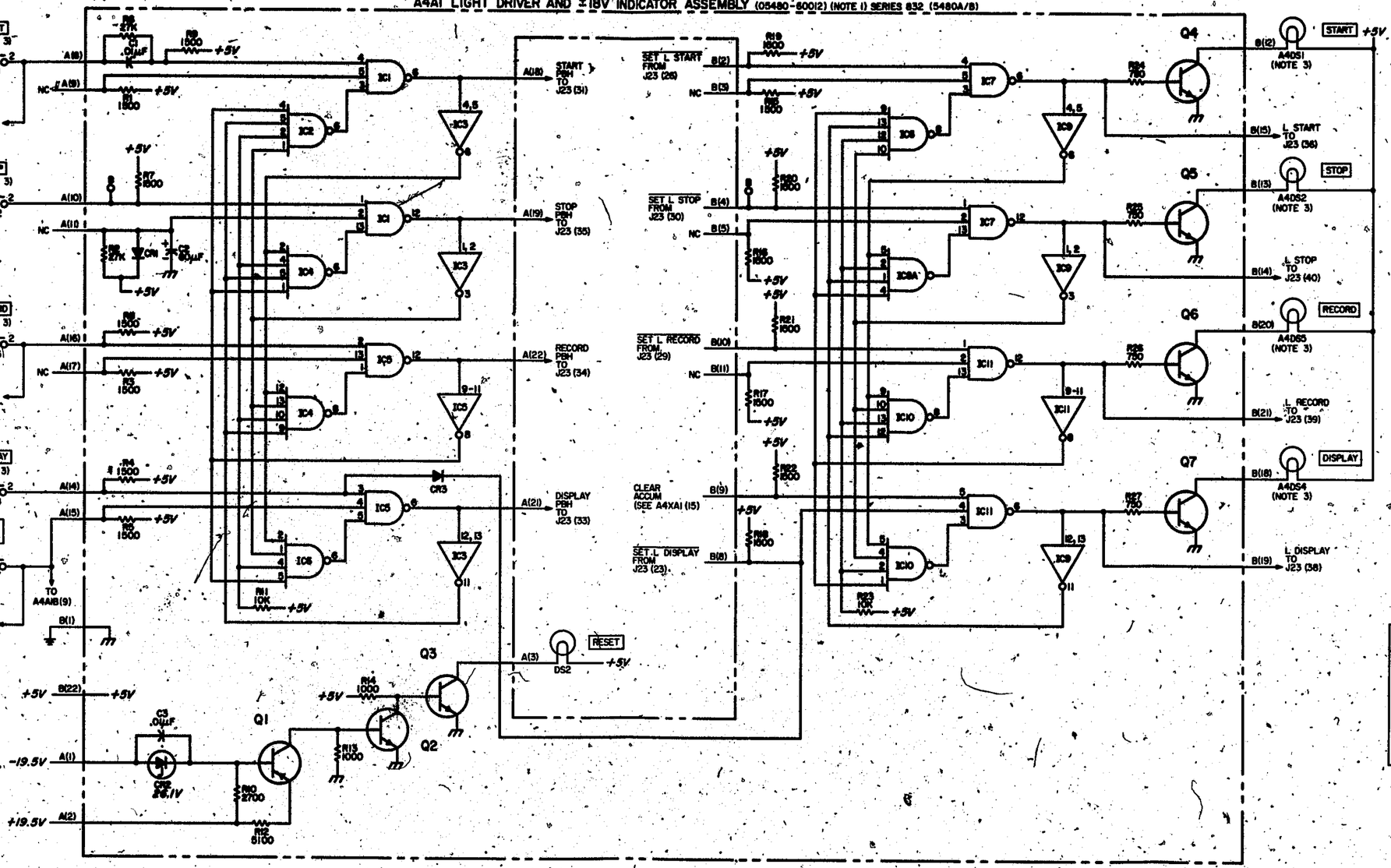


Figure 4-9
5480A/B (Main Frame Logic A3)
Wiring List: Table 4-2, Part D

Main Frame Logic Section (A3) is located at the lower left-hand rear corner of the 5480A/B. Board assemblies are numbered, in order, from the rear to the front of the instrument; there is a vacant (spare) board location between A1 and A3.

Figure 4-9
5480A/B (MAIN FRAME LOGIC A3)
Wiring List: Table 4-2, Part D

A4AI LIGHT DRIVER AND ±18V INDICATOR ASSEMBLY (05480-60012) (NOTE 1) SERIES 832 (5480A/B)



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
3. START | STOP | DISPLAY | RECORD
   SWITCH CONNECTIONS
   2,4: NORMALLY OPEN
   1,3: NORMALLY CLOSED
   CENTER CONNECTIONS: LAMP

REFERENCE DESIGNATIONS

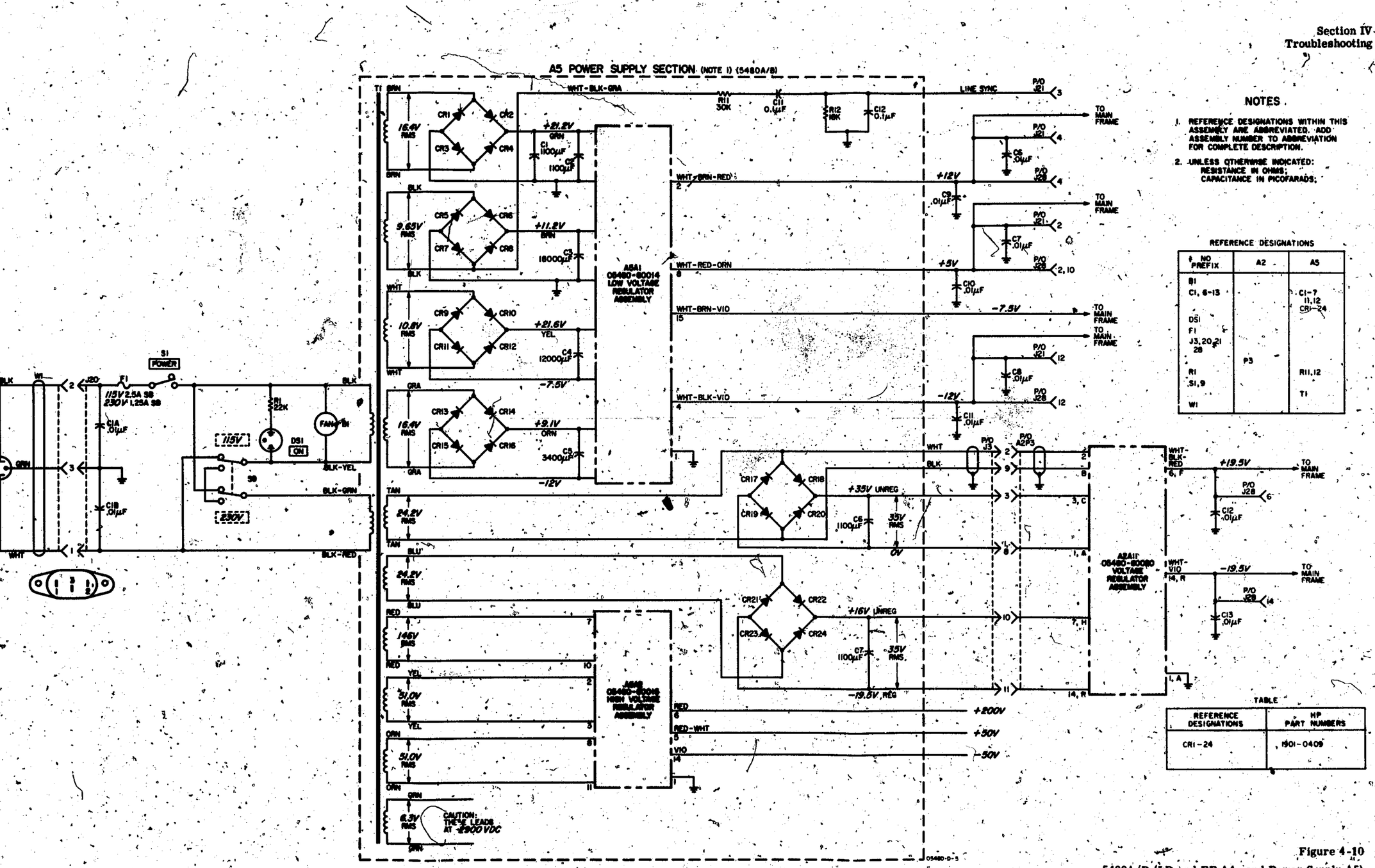
NO PREFIX	A4	A4AI
DS2	DS1,2,4,5	C1-3 CR1-3 IC1-11 Q1-7 R1-27-
	S1,2,4-7	

TABLE

REFERENCE DESIGNATIONS	HP PART NUMBER
CR 1,2	1901 - 0040
" 3	1902 - 3268
IC 1,9,7,11	1820 - 0088
2,4,6,8,10	" - 0089
3,5	" - 0054
Q1	1853 - 0020
2-7	1854 - 0246
	2N3643

05480-8-4

02850-1



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS;

REFERENCE DESIGNATIONS

NO PREFIX	A2	A5
B1		
C1, 6-13		C1-7, 11, 12
DS1		CR1-24
F1		
J3, 20, 21, 28	P3	
R1		R11, 12
S1, 9		
T1		
W1		

TABLE

REFERENCE DESIGNATIONS	HP PART NUMBERS
CR1-24	1901-0409

Figure 4-10
5480A/B (LD and FF A4, and Power Supply A5)
Wiring List: Table 4-2, Part E

NOTES:

1. A4 (A4A1) is located immediately behind the 5480A/B front-panel section on which the illuminated pushbuttons are mounted. For access to this section, remove top cover, and swing memory section deck out of the way.

2. A5 (Power Supply Section) is located at lower right-hand rear corner of 5480A/B unit. For access to boards in this section, remove top cover and swing memory section deck out of the way. For access to board sockets, remove bottom cover.

Figure 4-10

5480A/B (LD and FF A4, and POWER SUPPLY A5)

Wiring List: Table 4-2, Part E

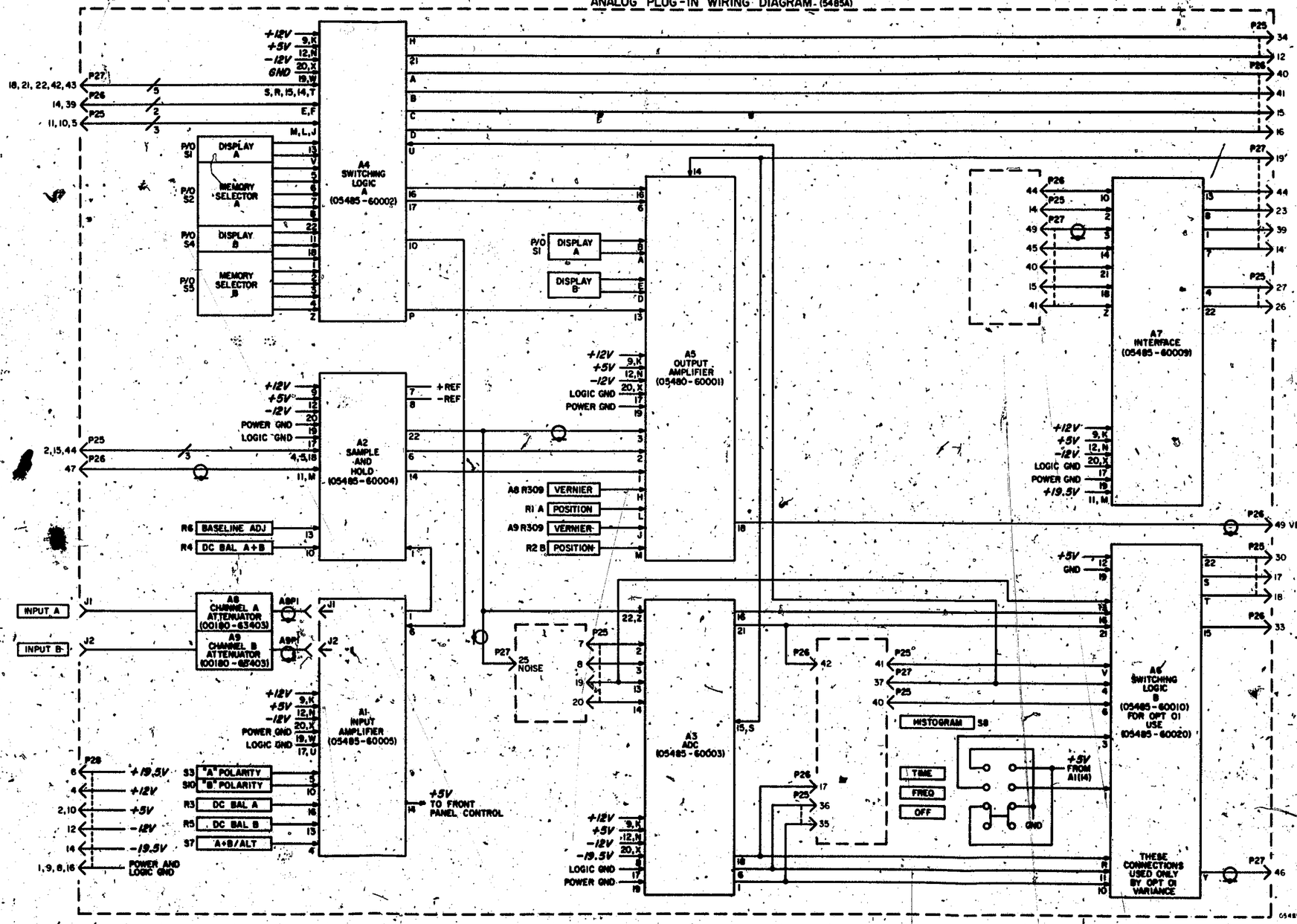


Figure 4-11
5485A
Wiring List: Table 4-2, Part G