A9 PROGRAM SELECTOR "B" (95486-60040, 05486-60004)

LOGIC AND DESCRIPTION

The function of Program Selector "B" is to control which one of the four front panel push button lights is lit, and to select four of the seven internal program states (Average, Summation, Display, and Prepare).

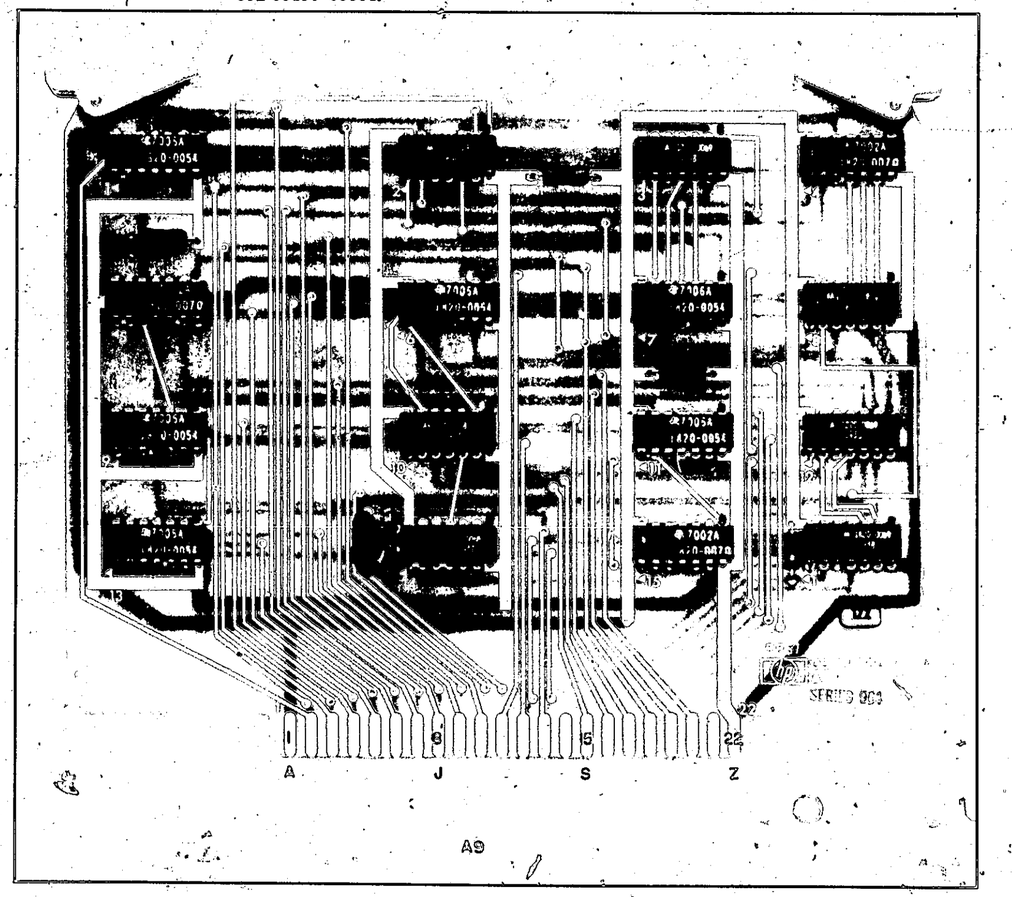
CHANGES FOR OLDER BOARDS

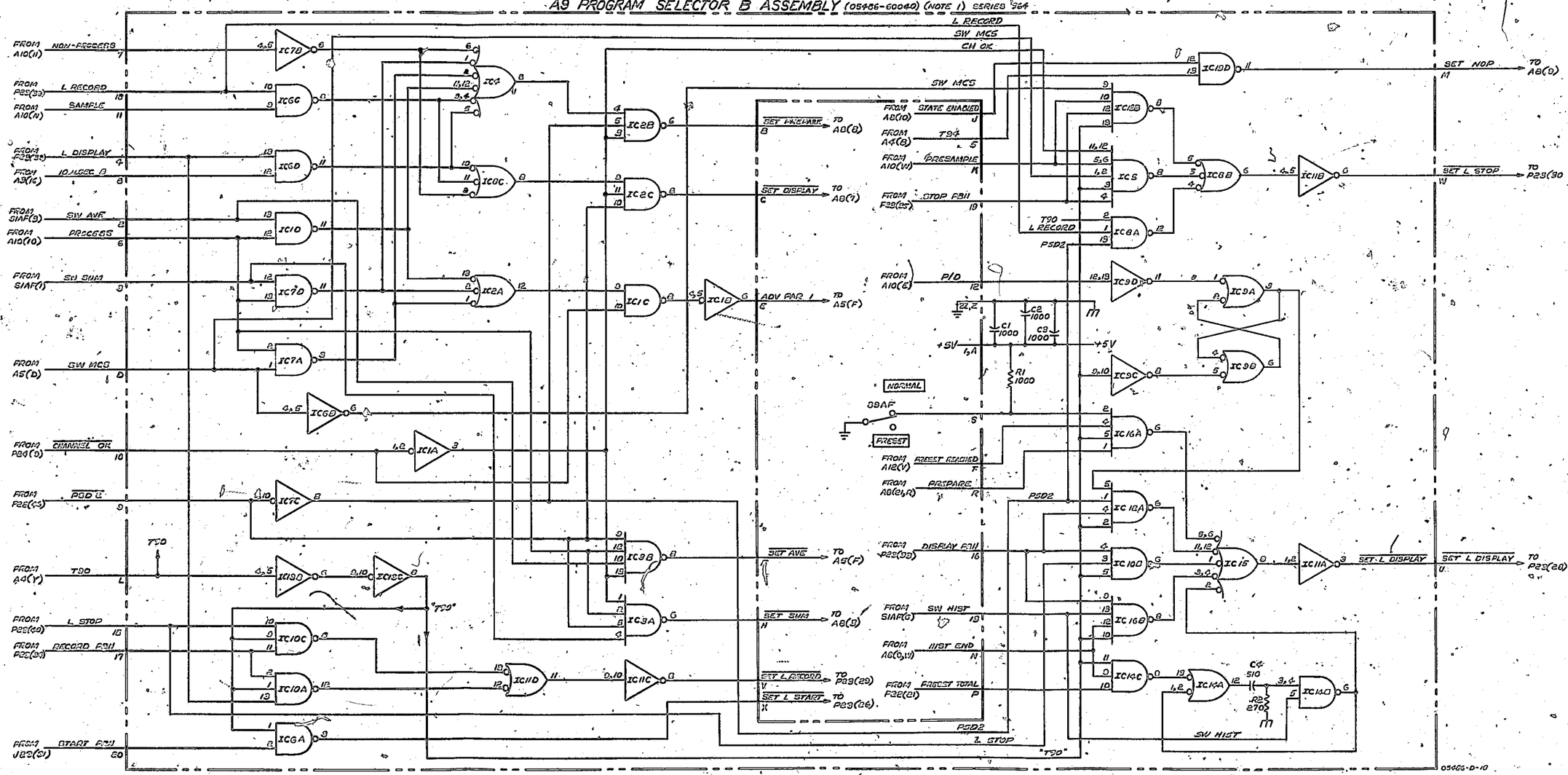
Current board (5486B only): 05486-60040

Older boards (5486A only): 05486-60004, Series 832 and 852

The current board, used in 5486B's only, is not a direct replacement for the 05486-60004 board used in the 5486A's.

The Series 852 05486-60004 is a direct replacement for the Series 832 05486-60004.





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;

REFERENCE DESIGNATIONS

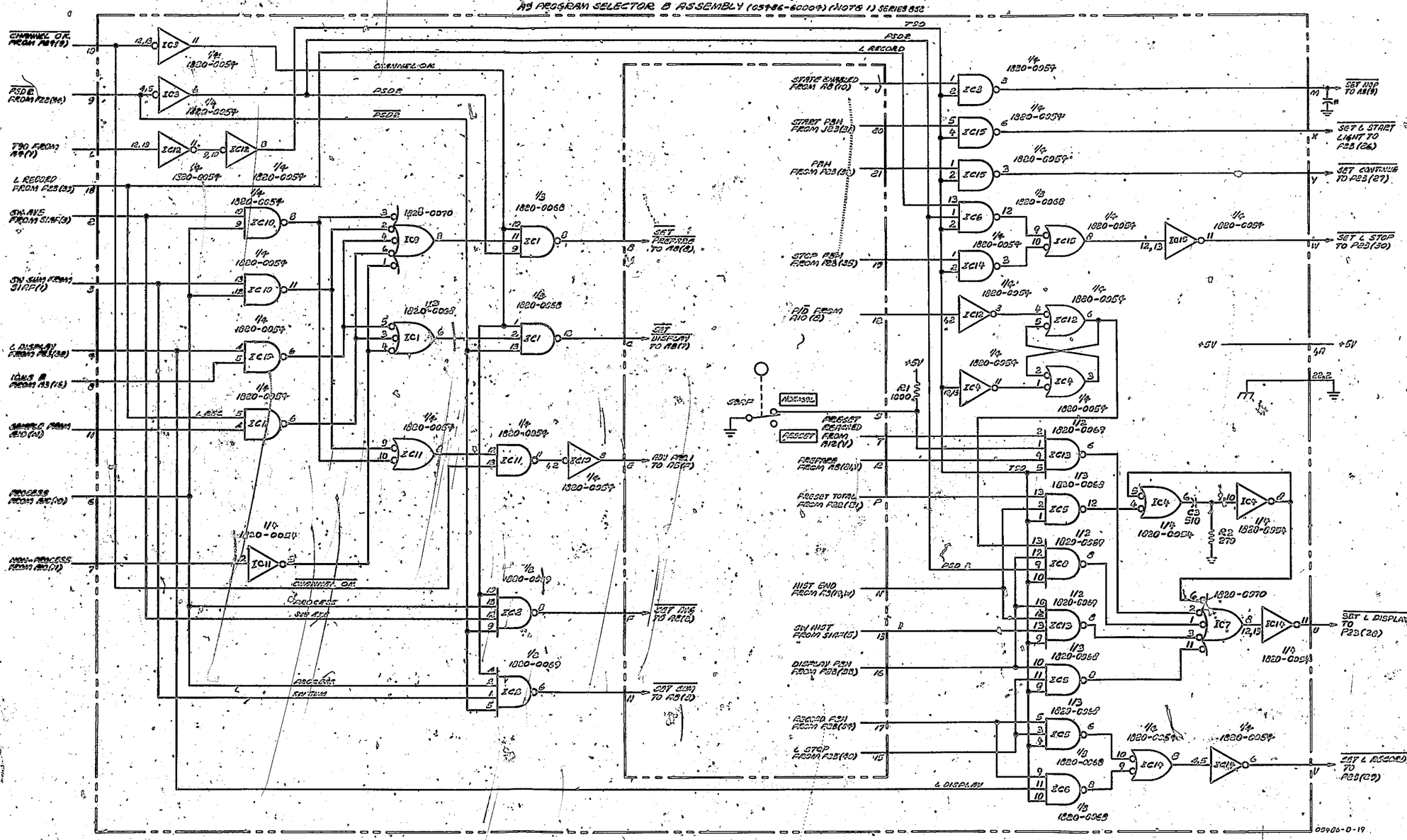
NO PREFIX	A9
	C1-4 IC1-16 R1,2
S9	

TABLE

REFERENCE DESIGNATIONS	HP PART NUMBERS
IC 1, 6, 7, 9, 11, 13	1820-0054
IC 2, 8, 10, 14	1820-0066
IC 3, 12, 16	1820-0069
IC 4, 5, 15	1820-0070

Figure 4-18
A9 Program Selector B Series 964

See Figure 4-18 for A9 Board description.



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS.
3. BOARD MAY BE STAMPED "SERIES 852"
4. ASTERISK (*) INDICATED COMPONENT MAY BE OMITTED

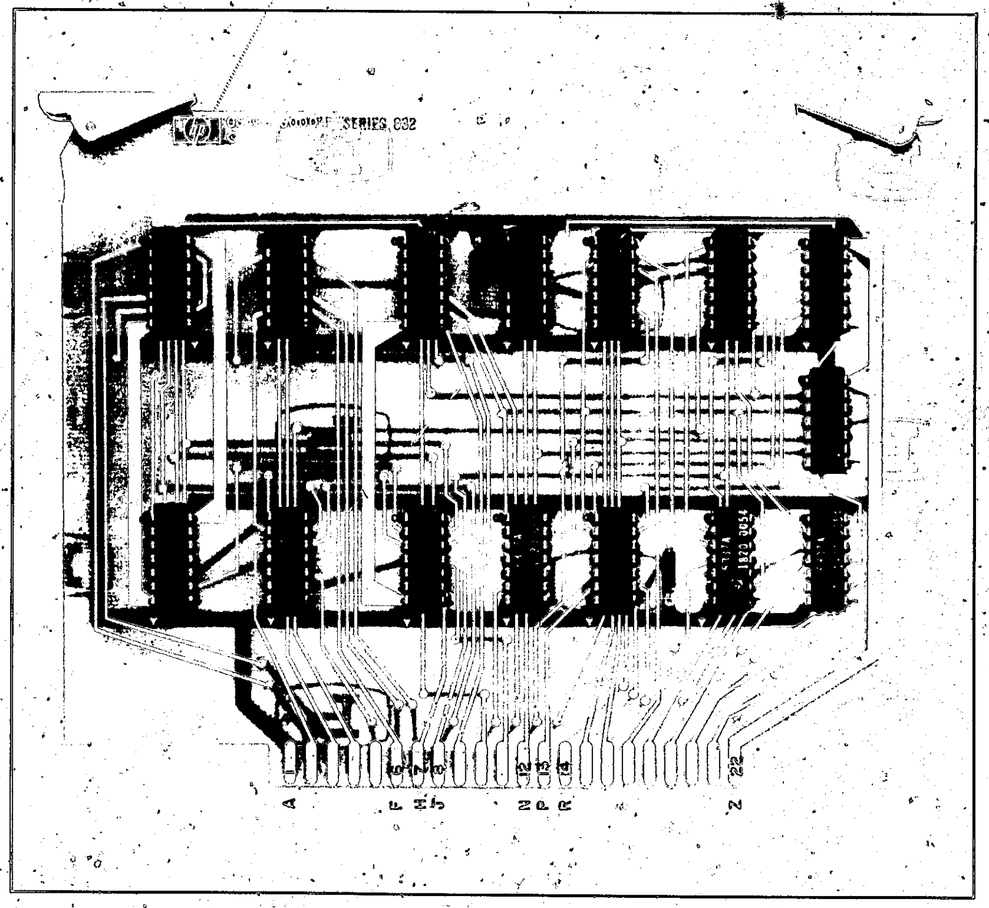
REFERENCE DESIGNATIONS

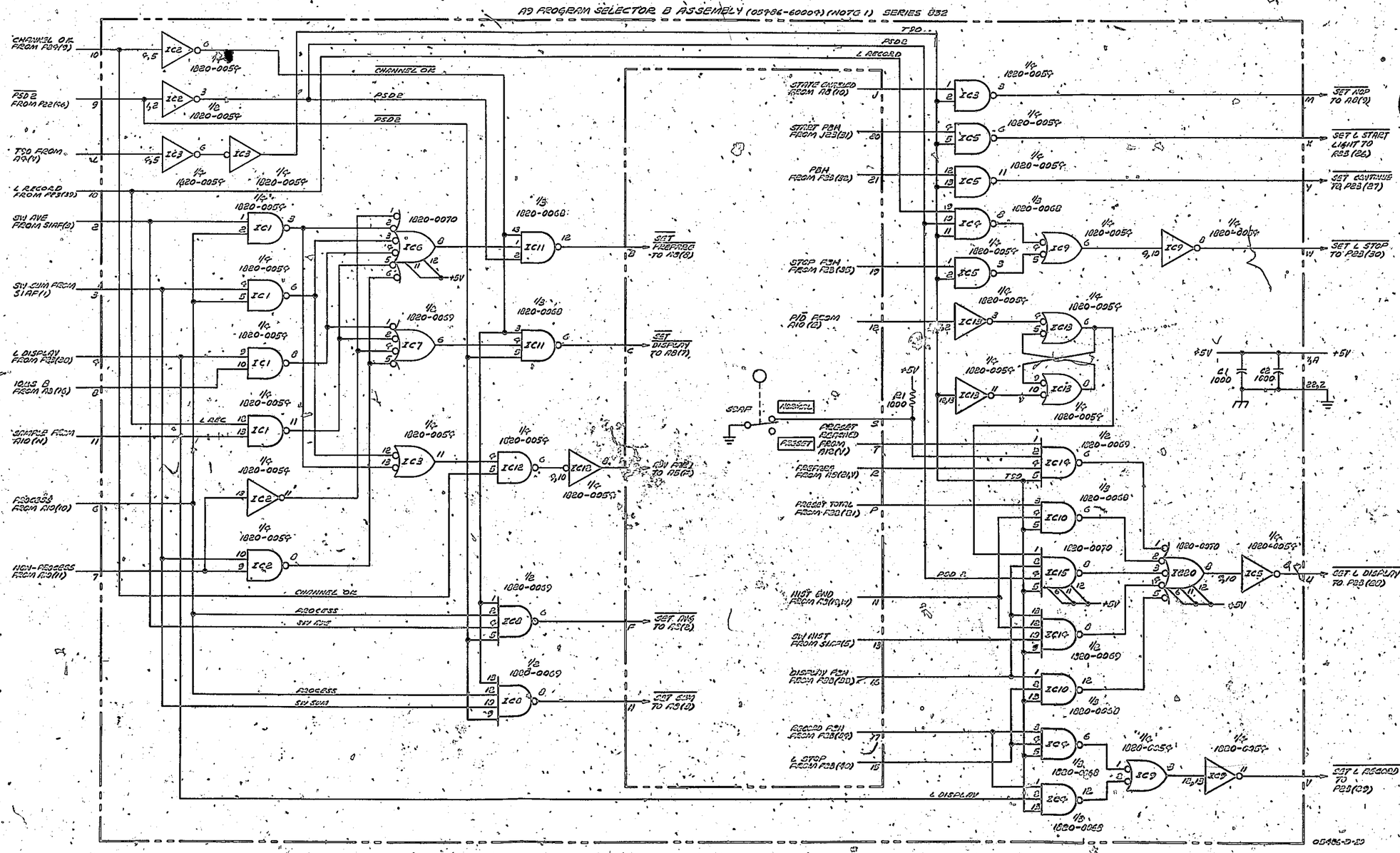
NO PREFIX	A9
59	C1-3 IC1-15 R1, 2

CIVE OMITTED

Figure 4-19
A9 Program Selector B Series 852

See Figure 4-18 for Board description.





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS;
3. S0 SHOWN IN 0
4. S0 ROTOR MOVES ONE CONTACT POSITION FOR EACH DETENT POSITION.

REFERENCE DESIGNATIONS

NO PREFIX	A9
S9	S1,2 IC1-15,20 R1

Figure 4-20
A9 Program Selector B Series 632

A10 LOGIC MATRIX "B" (05486-60041, 05486-60007)

DESCRIPTION

The function of the LOGIC MATRIX "B" BOARD is to provide the pulses Set Histogram Begin (Set HB), Set Histogram End (Set HE), (Sample), (Process), (Non-Process), and Set Multichannel Scaling (Set MCS), which control the internal 10 μsec programs of the 5486A/B. It also contains a flip/flop whose output (P/D) indicates whether the next 10 μsec program will process new data (P/D=High) or display stored data (P/D=Low). The 05486-60007 also contains circuitry for gating sync pulses to the process address register while accumulating frequency histograms and for gating sample pulses, whose rate is controlled by the Sweep Time switch, to the process address register while accumulating time-interval Histograms. This board also advances the Display Address Register (ADV DAR) once every 10 μsec except during the output mode when it is advanced at a rate controlled by the Time Base switch.

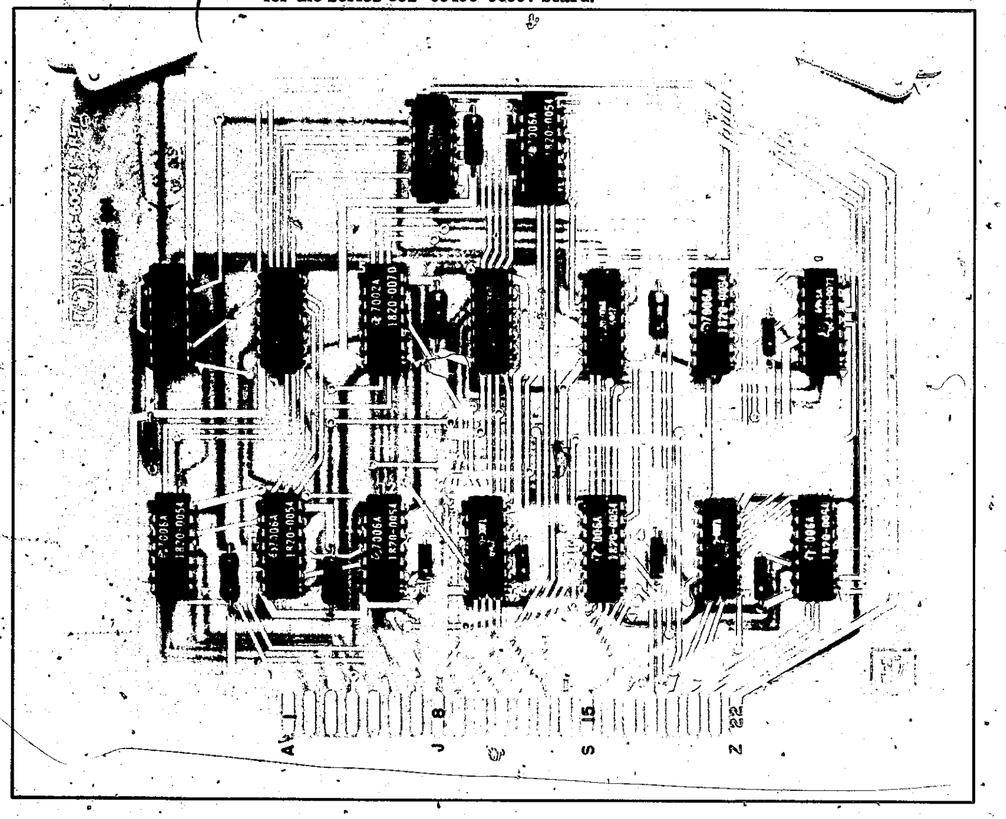
CHANGES FOR OLDER BOARDS

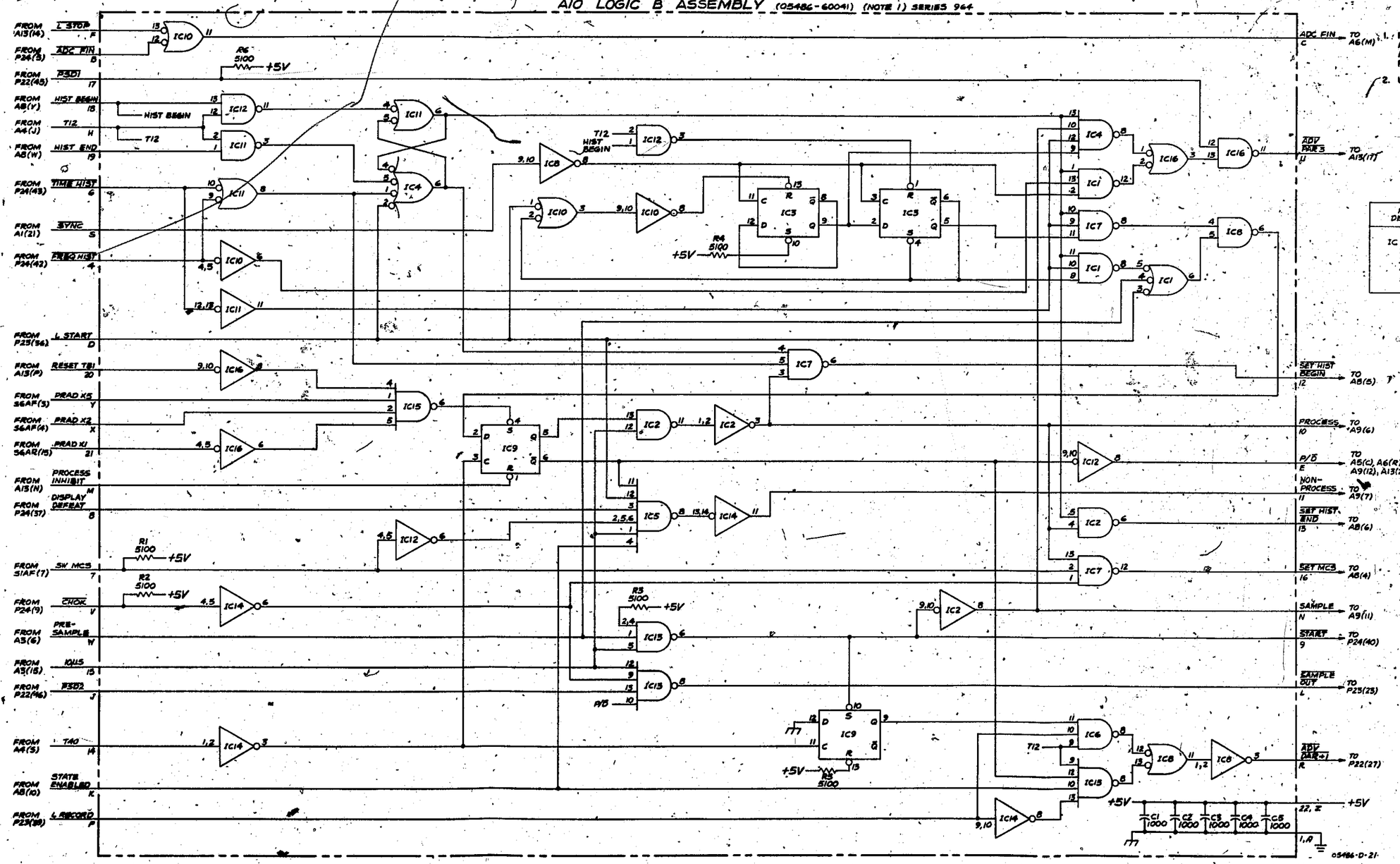
Current Board (5486B only): 05486-60041

Older Boards (5486A only): 05486-60007, Series 832 and 852

The current board, used only in 5486B's, is not a direct replacement for the 05486-60007, used in the 5486A.

The Series 852 05486-60007 board is a direct replacement for the Series 832 05486-60007 board.





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS;

TABLE

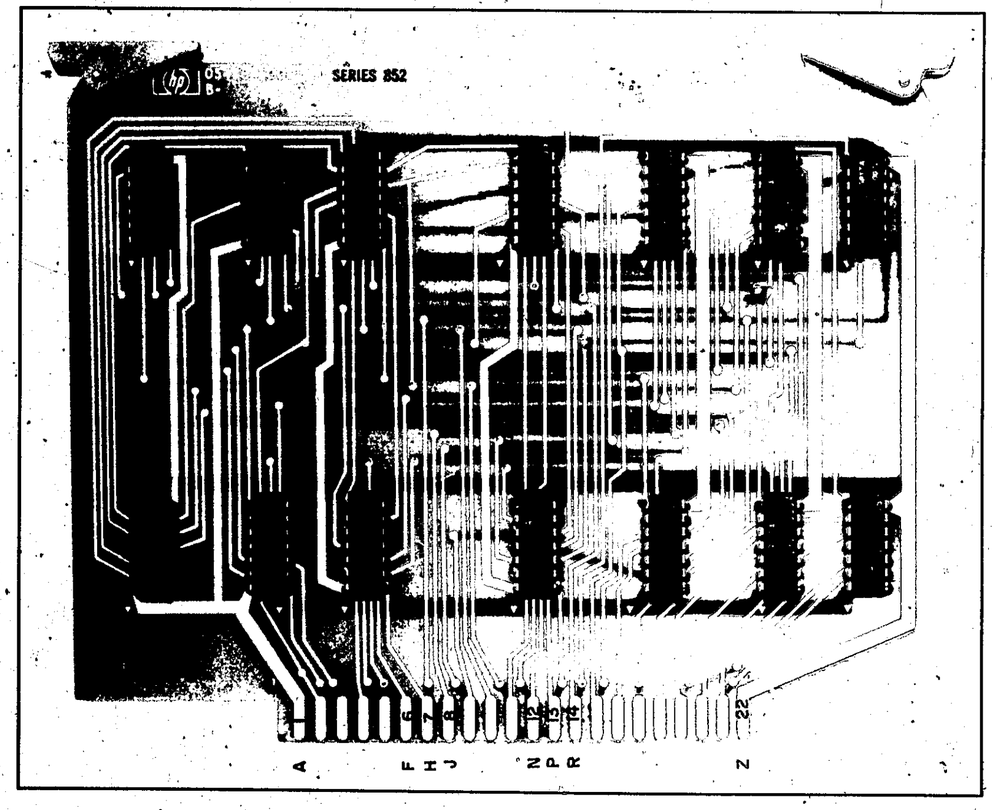
REFERENCE DESIGNATIONS	PART NUMBERS
IC 1, 6, 7	1820 - 0068
2, 8, 10-12, 14, 16	1820 - 0054
3, 9	1820 - 0077
4, 13, 15	1820 - 0069
5	1820 - 0070

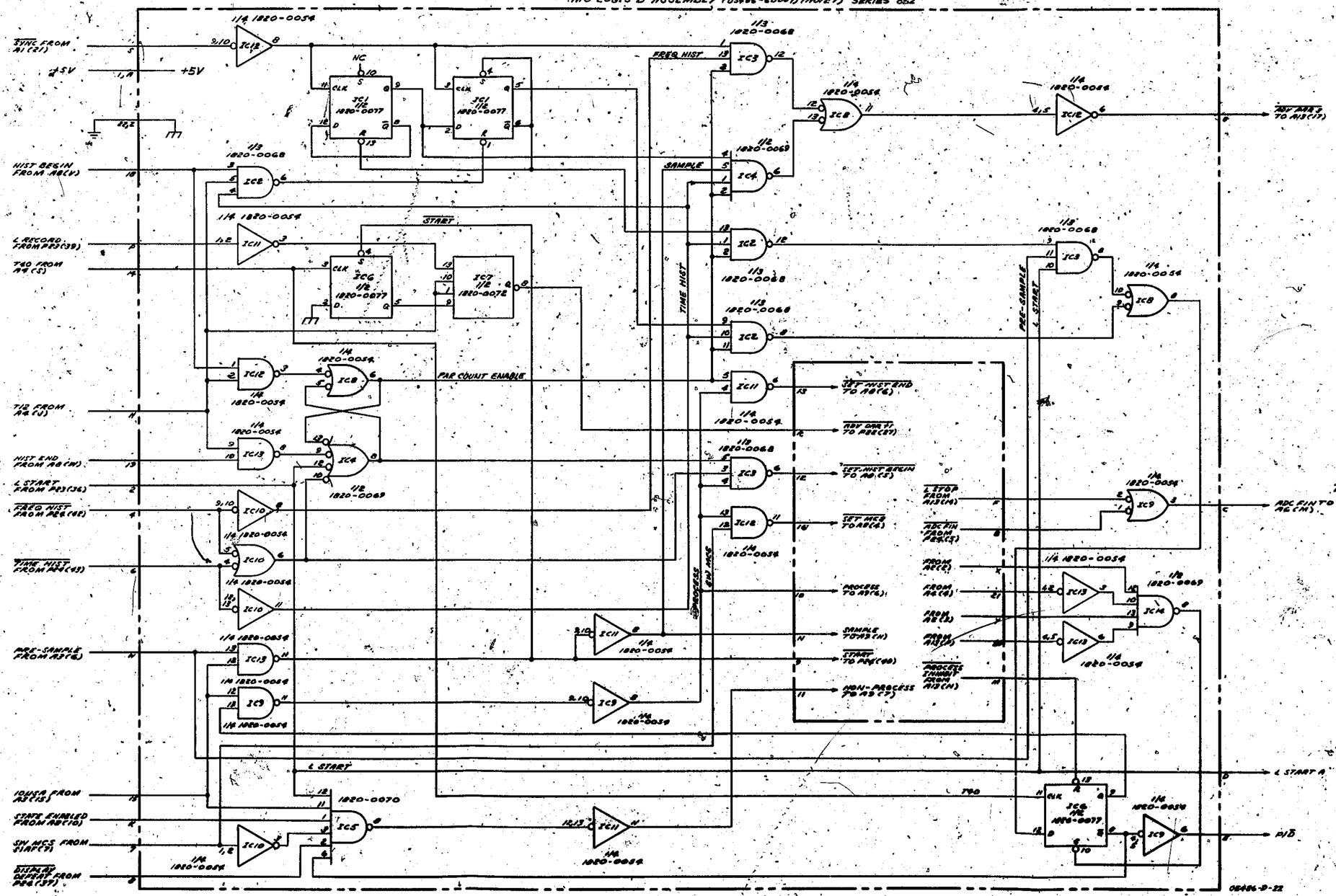
REFERENCE- DESIGNATIONS

A10
C1-5 IC1-16 R1-5

Figure 4-21
A10 Logic B Series 964

See Figure 4-21 for Board description.





NOTES

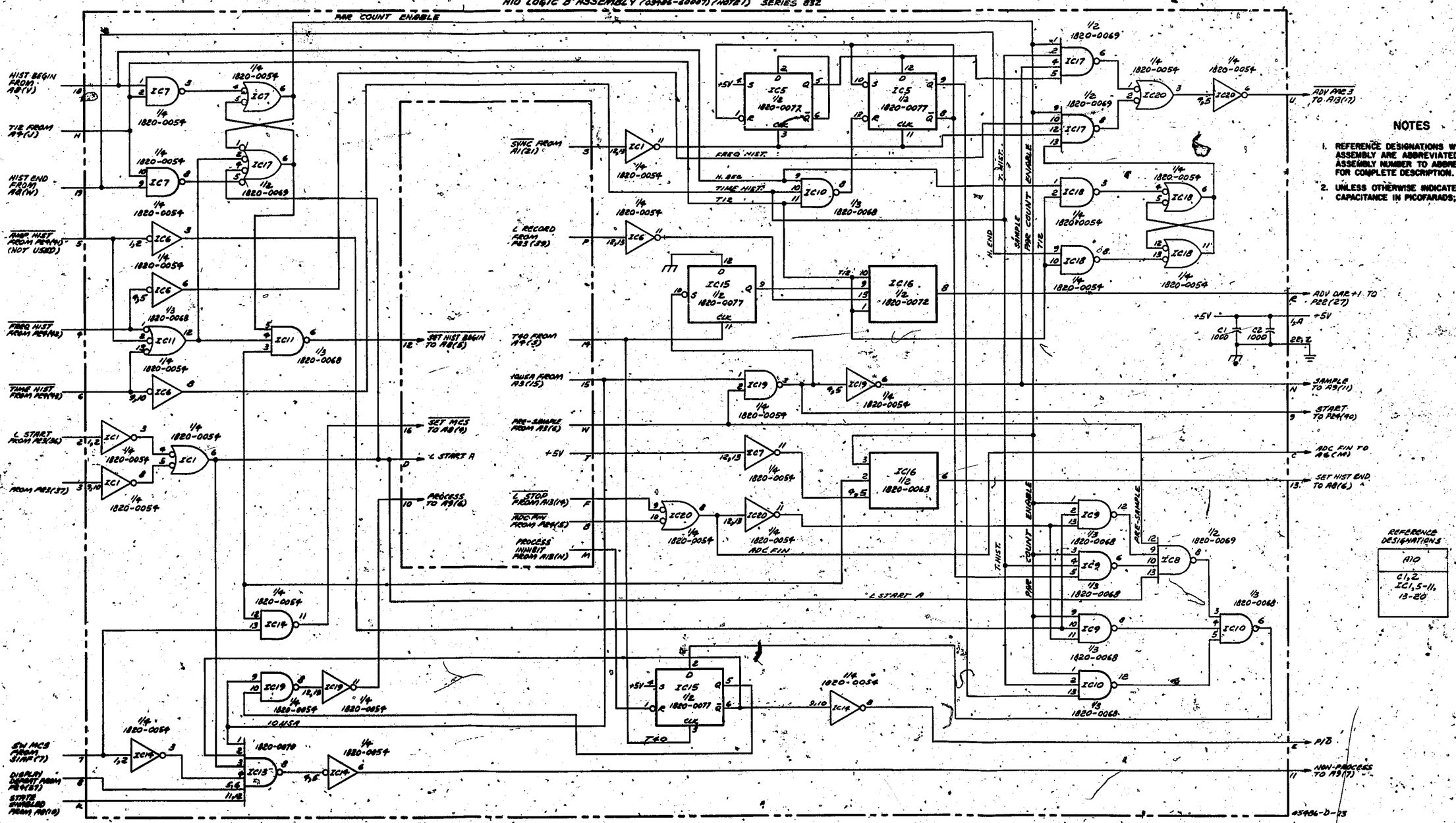
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: CAPACITANCE IN PICOFARADS;

REFERENCE DESIGNATIONS

A10
IC1-14

Figure 4-22
A10 Logic B Series 852

See Figure 4-21 for A10 Board description.



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: CAPACITANCE IN PICOFARADS;

REFERENCE DESIGNATIONS
A10
C1, 2 IC1, 5-11, 13-20

Figure 4-23
A10 Logic B Series 832

A11 SHIFT CONTROL LOGIC "B" (05486-60042, 05486-60002)

DESCRIPTION

The function of the Shift Control Logic "B" is to generate the correct number of Shift Pulses to be sent to the Accumulator during shift operations. This board contains a Counting Register which can count 0-23, and a Storage Register which contains the desired number of Shift Pulses. When the contents of the Counting Register equals the contents of the Storage Register a pulse is sent to A12 which indicates the desired number of Shift Pulses have been generated.

1. SW=AVERAGE

a. Prepare program (accumulator holds number of sweeps)

1) Strobe sweep number switch into hold register on A11 board actually (19-SN) T12.

2) Assume 5-bit information (with 7-bit information, counter is set "+2", with 9-bit information, counter is set "+4").

Start MOD 24 counter, start accumulator shift T14.
When counter=hold, then SC7 goes low.
When SC7 goes low, it sets RS2 (RS2 was reset at T_0 by MPX).
Monitor AC18. When a "1" is detected, RS4 will be set (RS4 was reset by start shift command).
When RS2 and RS4 are both set, a 0 to 1 transition occurs on SC12, which clock contents of MOD 24 counter into hold register.
Also, RS4 will be set after 19 pulses counted into MOD 24 counter, by SC13 going low. This is to insure that a clock pulse will be sent to hold register, even if accumulator contains all zeros.

Operation of RS1 in PREPARE

RS1 controls shift pulses on SHIFT 1 line reset with start shift command (T14). No reset occurs. However only 24 input pulses arrive on SC11 line to be gated out.

b. AVERAGE program

From PREPARE, HOLD register contains proper number of shifts.
START shift at T12. (Accumulator shifts and MOD 24 counter counts.
Reset RS1 with start shift
Compare MOD 24 counter with HOLD register. When equal, SC6 goes low, setting RS1 and inhibiting shift pulses to accumulator.

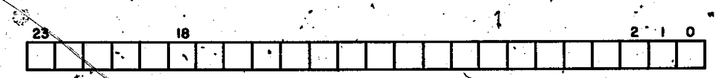
2. SW=SUMMATION

a. Prepare program initiated as in SW=AVE. If in AUTO the SUMMATION program will use the number that was inserted into HOLD register. However, if AUTO, then contents of sensitivity multiply into HOLD register via SET SCALE # Line (A5) at 780. PREPARE. Now, when in SUMMATION program, accumulator will be shifted the # of time directed by MULTIPLIER.

3. SW=HISTOGRAM

a. In HB, set SCALE #. During histogram program shift as indicated by HOLD.

Operation of RS5 - controls MOD 24 counter
Set will START SHIFT, enabling clock pulses to counter and remaining 8 pulses enabled by SC10.



SWEEP 1

Assume all zeros in acc.

Say SWITCH=2

HOLD = 19 - SWITCH = 17

Then SC7 goes low on 17th pulse, setting RS2
AC18 will always equal zero
SC13 goes low on 19th pulse, setting RS4
Now a clock pulse arrives on SC12, setting contents of counter into HOLD, or 19 HOLD

This number (19) represents number of shifts required in SUMMATION and AVERAGE program.

SWEEP 2

Now LSB=1

Say SWITCH=2

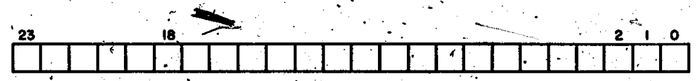
HOLD = 17

SC7 goes low on 17th pulse, setting RS2
After 18 pulses, a "1" will be in AC18, thus setting RS4
Now a clock pulse arrives on SC12, setting contents of counter into HOLD, or 18 HOLD

(SC12 goes low on 19th pulse, but RS4 has already been set, so it is ignored)

This number (18) represents # of shifts required in SUM and AVE.

SWEEP 3



Now Bit 1 = 1

SWITCH = 2

HOLD = 7

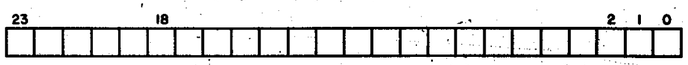
SC7 goes low on 17th pulse, setting RS2
After 17 pulses, a "1" will be in AC18, thus setting RS4
Clock pulse arrives on SC12, setting C (Counter) HOLD, or 17 HOLD

This number (17) represents # of shifts required in SUM and AVE

Figure 4-23
A10 LOGIC B SERIES 832

(See Page 4-45)

SWEEP 4



Same as above case (Sweep #3), as Bit 1 = 1, and state of bit 0 is immaterial.

Consider Preset reached line (RS3) - only applicable in prepare program

Reset with START SHIFT (T12)

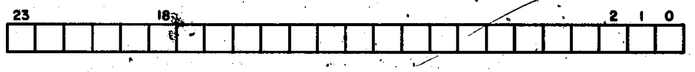
Set if RS2 = RS4 (same as RS2 reset and RS7 set)

But RS2 is reset with START SHIFT (T12)

And RS4 is set when a "1" is detected at AC18

In order to set P. R: , RS4 must be set before RS2 is

SWEEP 5



Now Bit 2 = 1

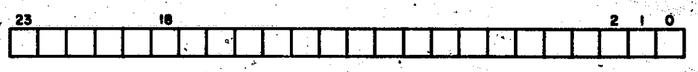
SWITCH = 2

HOLD = 17

After 16 pulses, a "1" will occur on AC18, this setting RS4
SC7 goes low on 17th pulse, setting RS2
RS4 set before RS2, therefore set P. R.

(On another board (A9), if PRESET/NORMAL is at PRESET, then set LDISPLAY at T90 and PREPARE.)

At same time set 18 CL19 goes low, effectively shifting position of "1" one bit to right. End result is accumulator containing the following



Set 18 CL19 stays low until RS2 is set. (RS2 is set when COUNTER=HOLD)

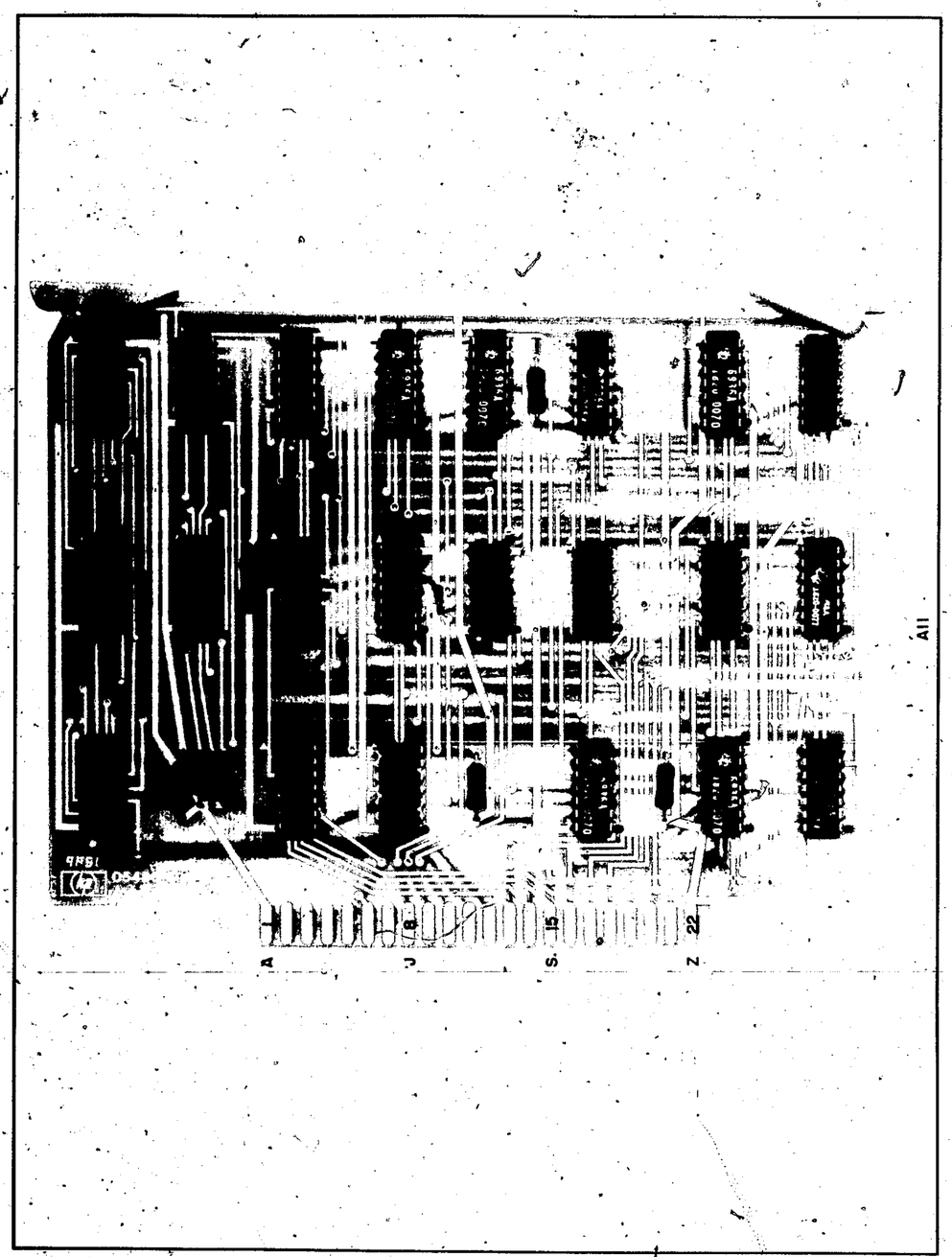
e.g.: Consider situation where we have a "1" in Bit 10 (Sweep number switch originally 10)

Now operator sets switch to 2

In next prepare program, RS2 will be set on 17th pulse; RS4 will set on 9th pulse

S18C19 will be low for 17-8=9 pulses

Position of "1" moves a place to right



A11 SHIFT CONTROL ASSEMBLY (05486-60048) (NOTE 1) SERIES 964

NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;

REFERENCE DESIGNATIONS

A11
C1 - 5 IC1 - 28 R1 - 3

TABLE

REFERENCE DESIGNATIONS	HP PART NUMBERS
IC 1, 3, 6, 18, 22	1820-0054
2	1820-0068
4, 5, 7, 9, 20, 21	1820-0070
8	1820-0069
10 - 12, 16, 17	1820-0077
13 - 15	1820-0072
19	1820-0071

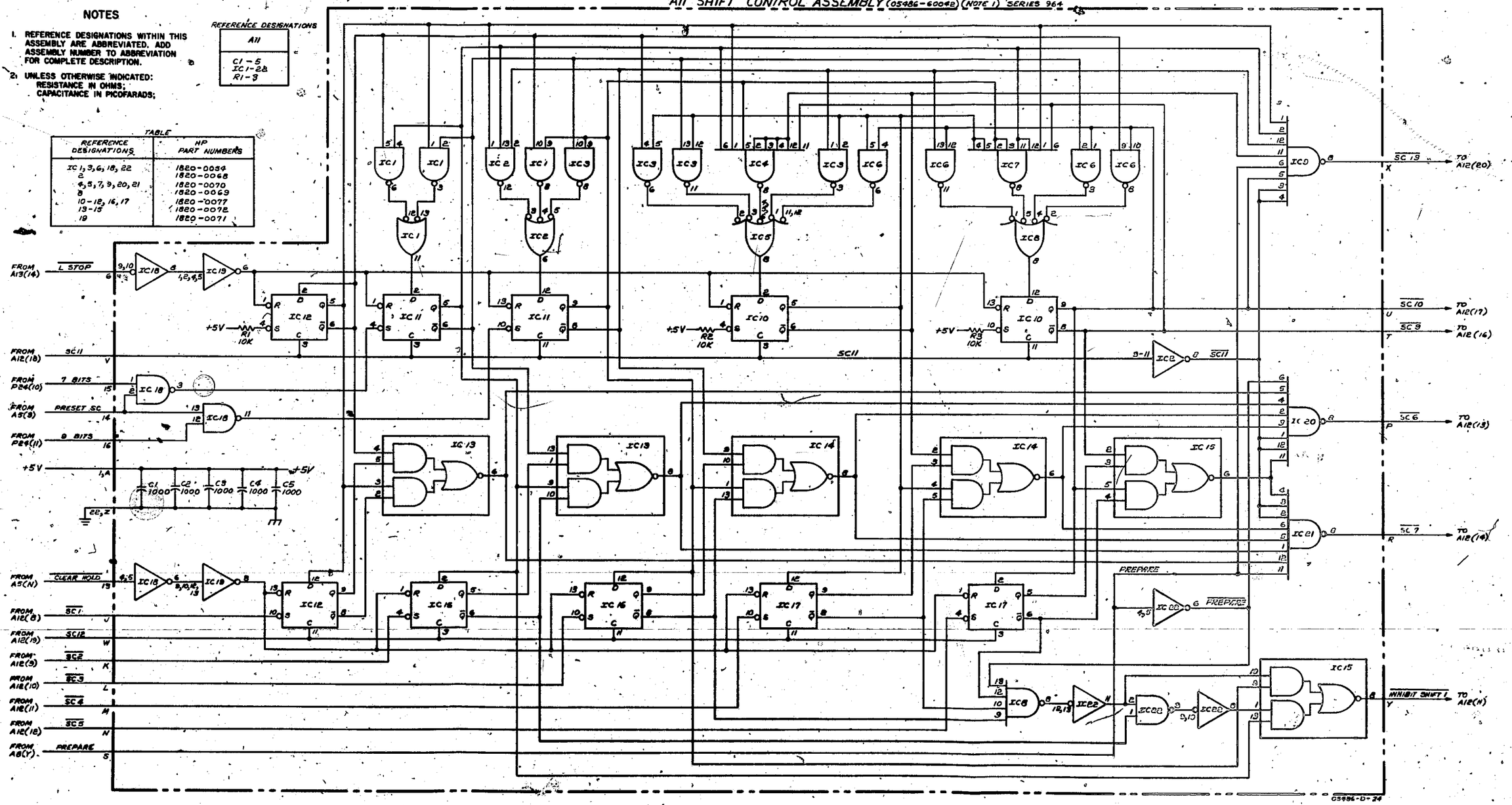
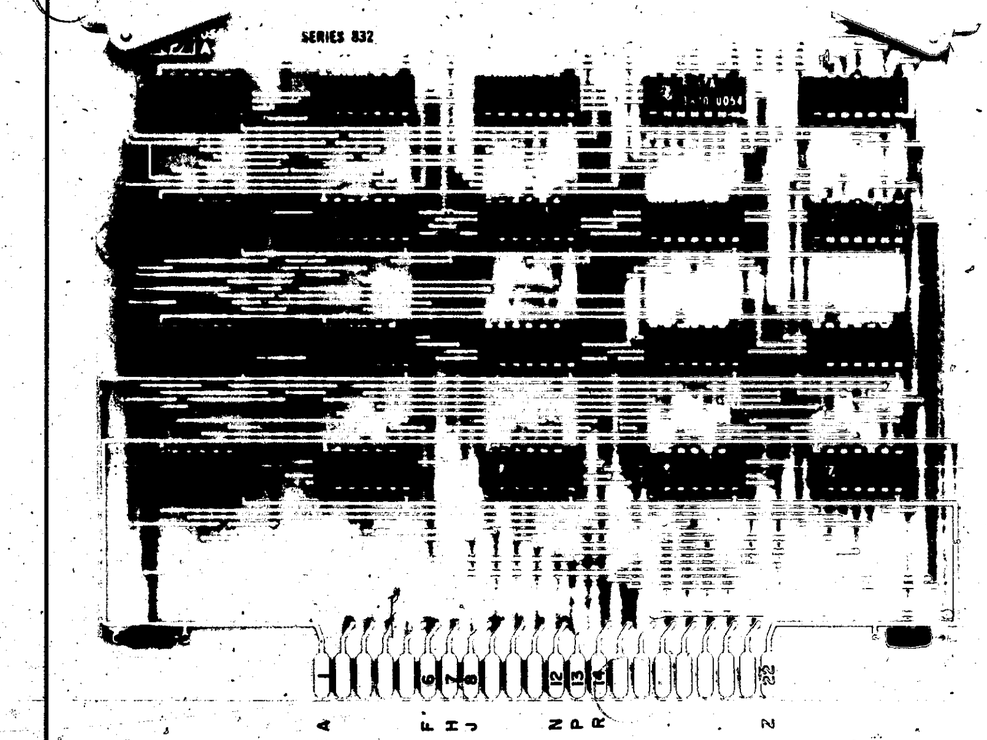
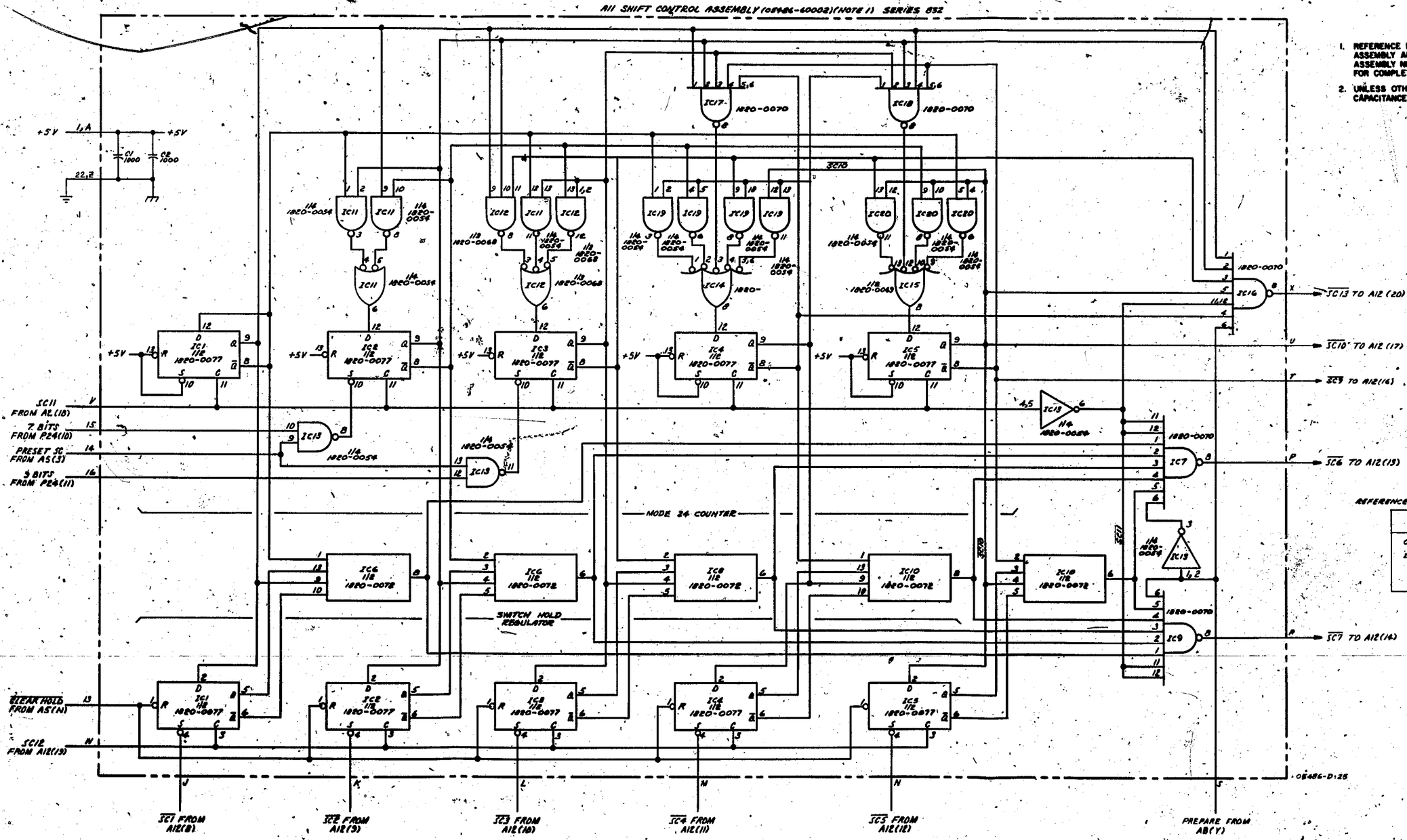


Figure 4-24
A11 Shift Control B Series 964

See Figure 4-24 for Board description.





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: CAPACITANCE IN PICOFARADS;

REFERENCE DESIGNATIONS

A11
C1, 2
IC1-20

Figure 4-25
A11 Shift Control B Series 832

A12 SHIFT CONTROL LOGIC "A" (05486-60043, 05486-60001)

LOGIC AND DESCRIPTION

The function of Shift Control Logic "A" is to control the operation of A11. It gates the contents of the Sweep Number Swithc and the Sensitivity Multiplier Switch into the A11 Storage Register. It sends 10 MHz Clock Pulses to the A11 Counting Register except during the Prepare Program when it sends 5 MHz Clock Pulses. It contains a Flip/Flop which indicates when a Preset Number of sweeps have occurred.

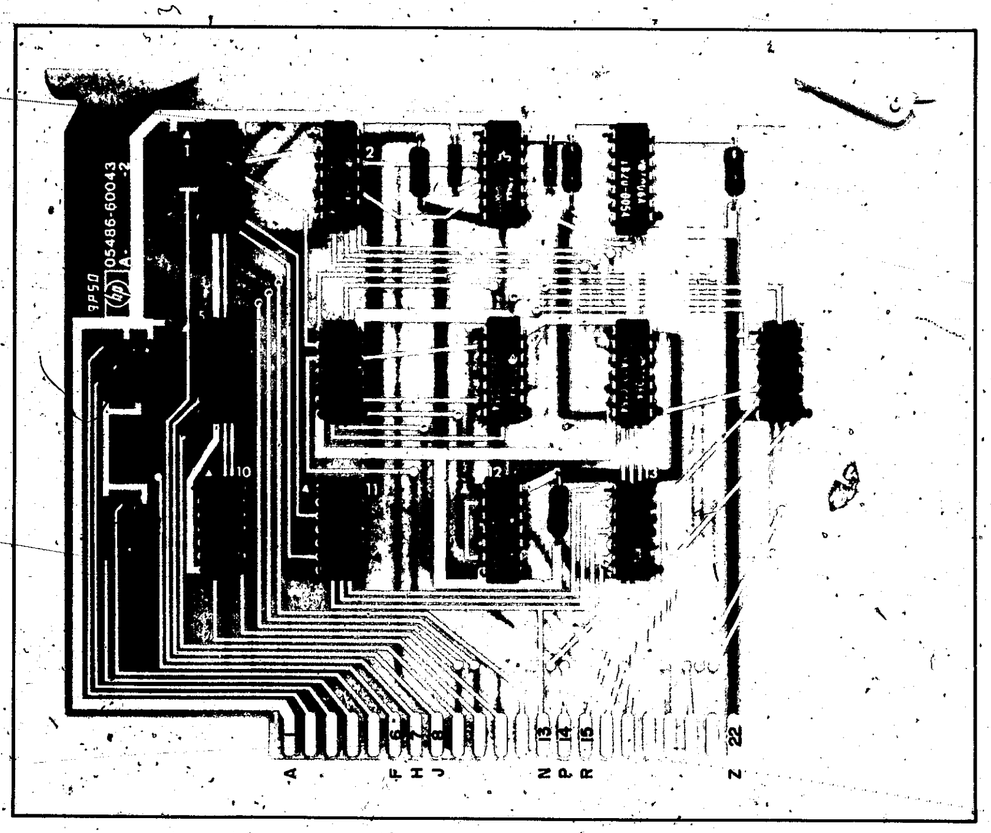
CHANGES FOR OLDER BOARDS

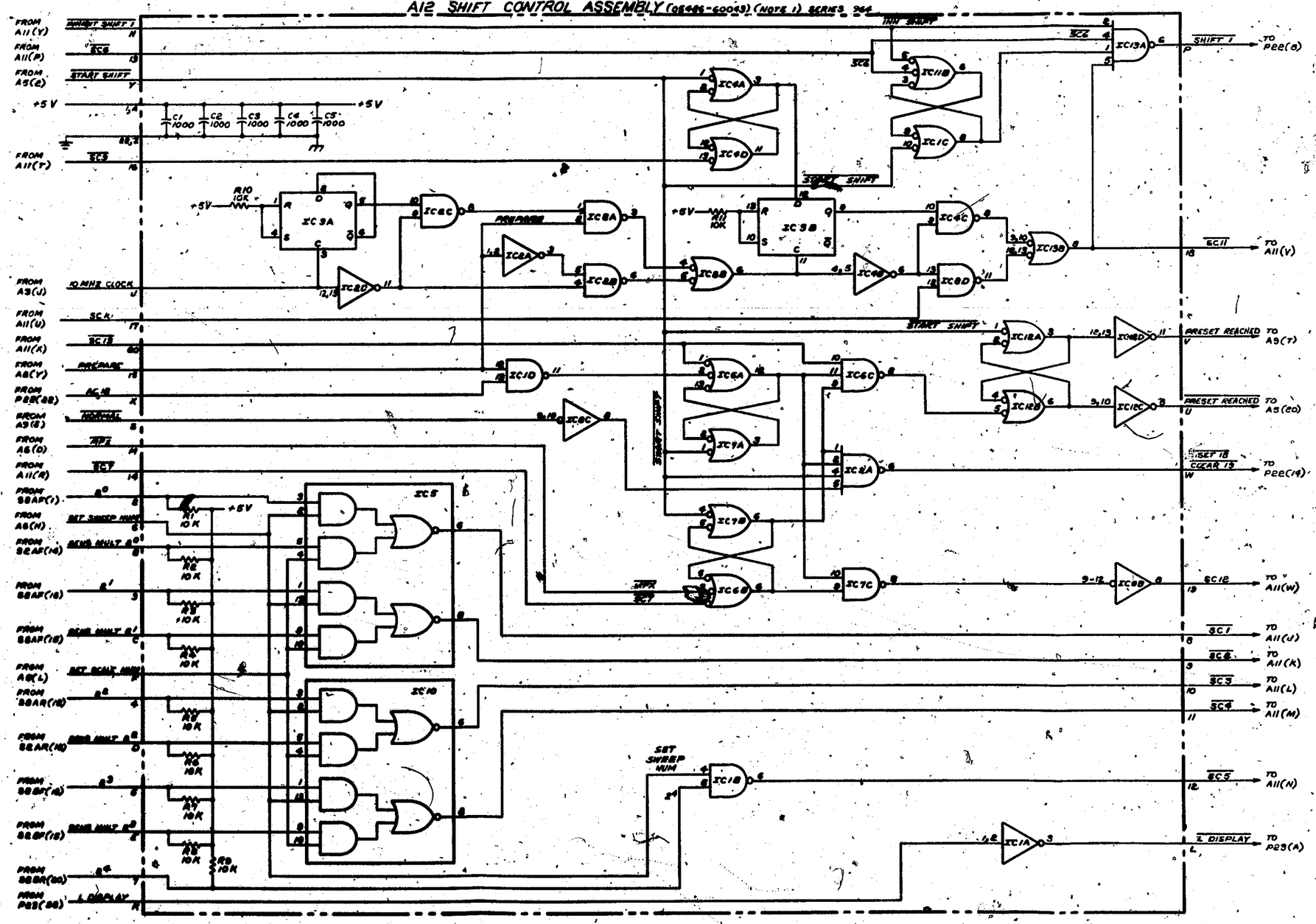
Current Board (5486B only): 05486-60043

NOTE: SWEEP NUMBER switch connections are same as for 5486A SWEEP NUMBER switch shown with older board.

Older Board (5486A only): 05486-60001

The current board, used in 5486B's only, is not a direct replacement for the 05486-60001, used in 5486A's.





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS;

REFERENCE DESIGNATIONS

A12
C1 - 5 IC1 - 19 R1 - 11

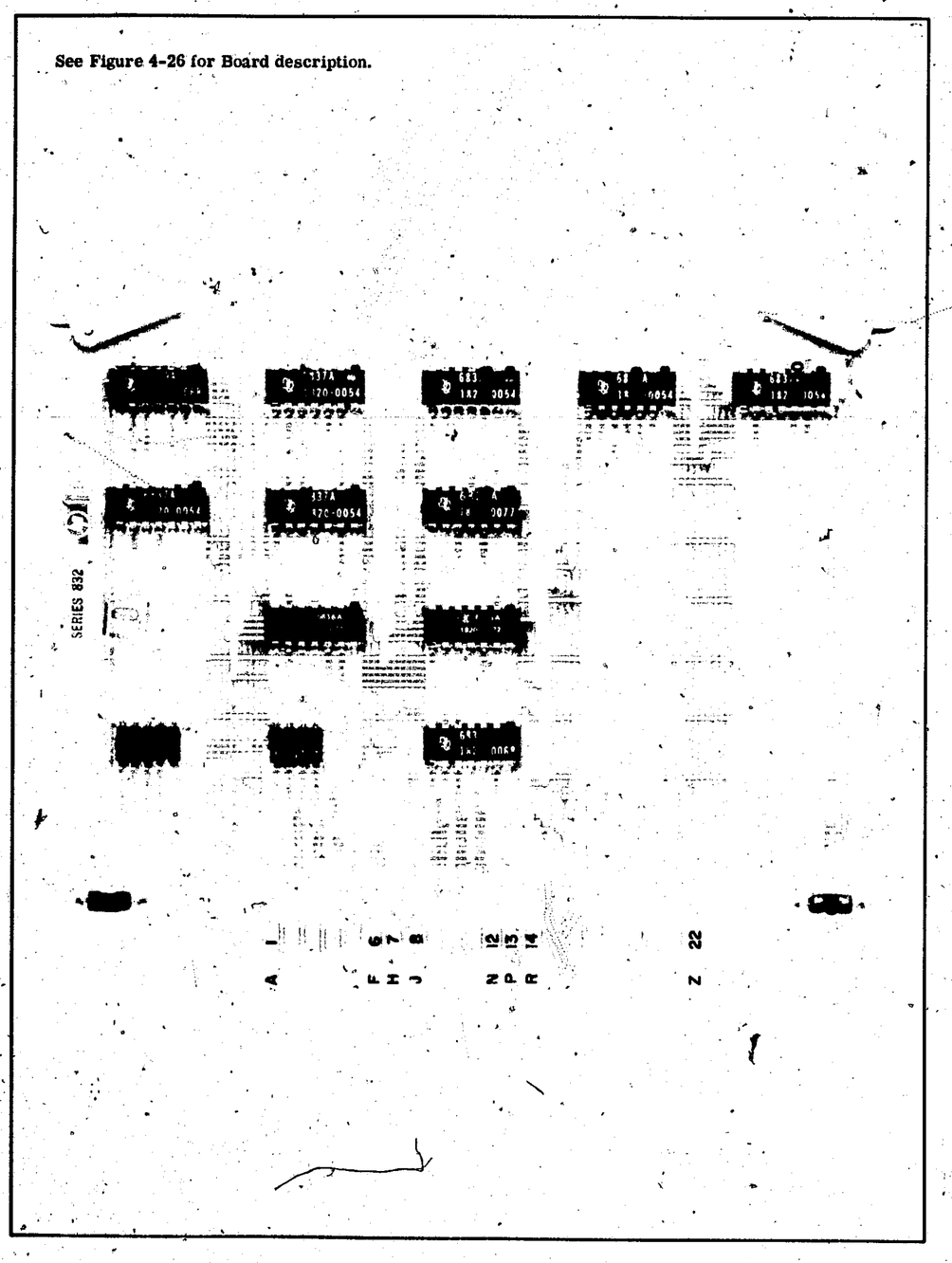
TABLE

REFERENCE DESIGNATIONS	HP PART NUMBERS
IC 1,2,4,7,8,12	1820-0054
6,11	1820-0068
9,13	1820-0071
5,10	1820-0063
3	1820-0077

05486-D-36

Figure 4-26
A12 Shift Control A Series 964

See Figure 4-26 for Board description.



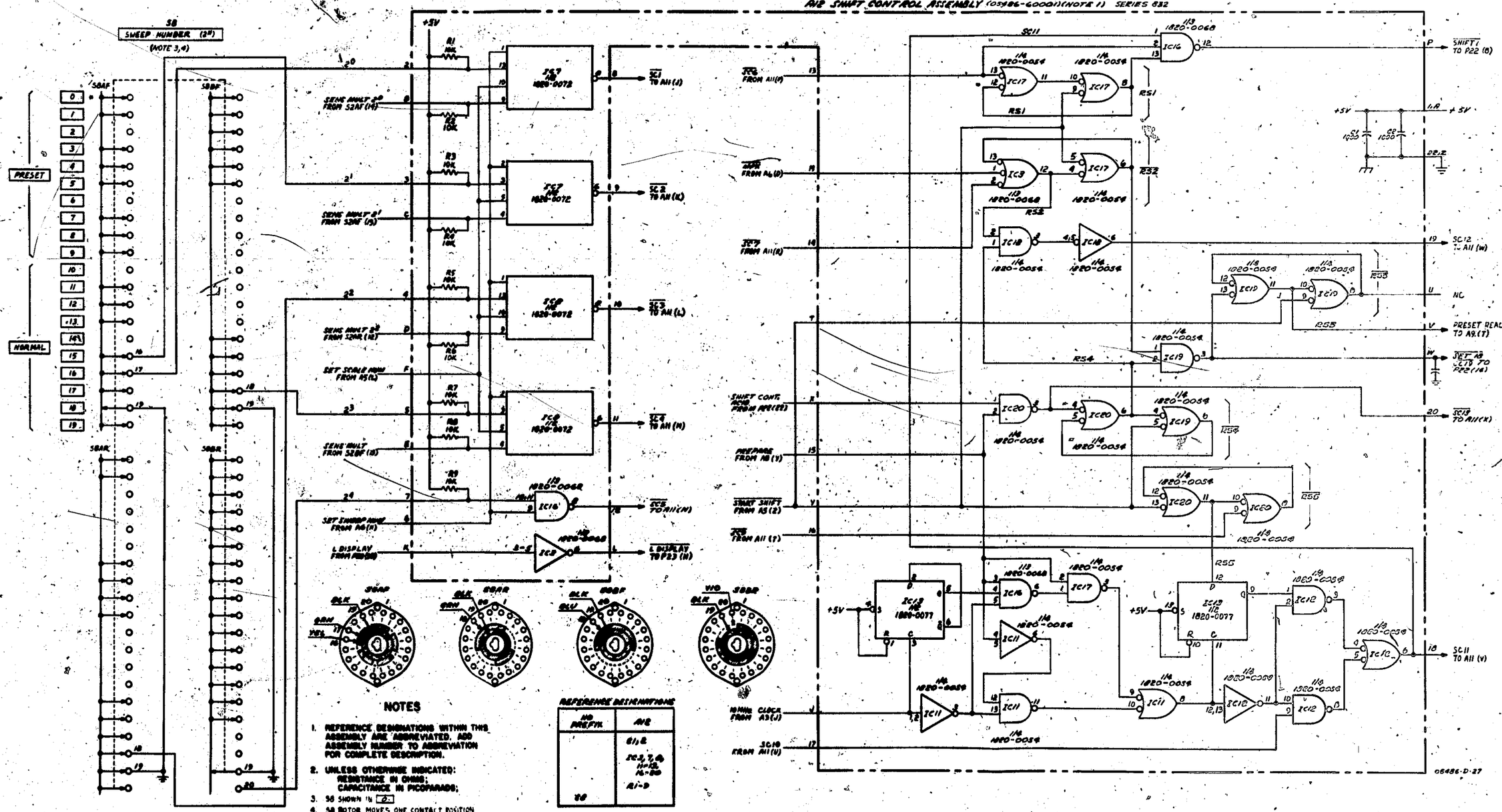


Figure 4-27
A12 Shift Control A Series 832

A13 LOGIC MATRIX "D" (05486-60044, 05486-60015)

DESCRIPTION

The function of LOGIC MATRIX "D" is to provide the following commands at the proper time, Clear Display Address Register (Clear DAR), set Process Address Register to 1111111100 (SET PAR), set Display Address Register to 1111111100 (Set DAR), (Reset Time Base), increment process address register (PAR PAR + 1), Decrement Process Address Register (PAR PAR - 1), lift X-Y Plotter Pen (Pen Lifter), and two commands used with the I/O Coupler - 5480A/B Slaved (MBSL), and 5480A/B Semi-slaved (MBSSL).

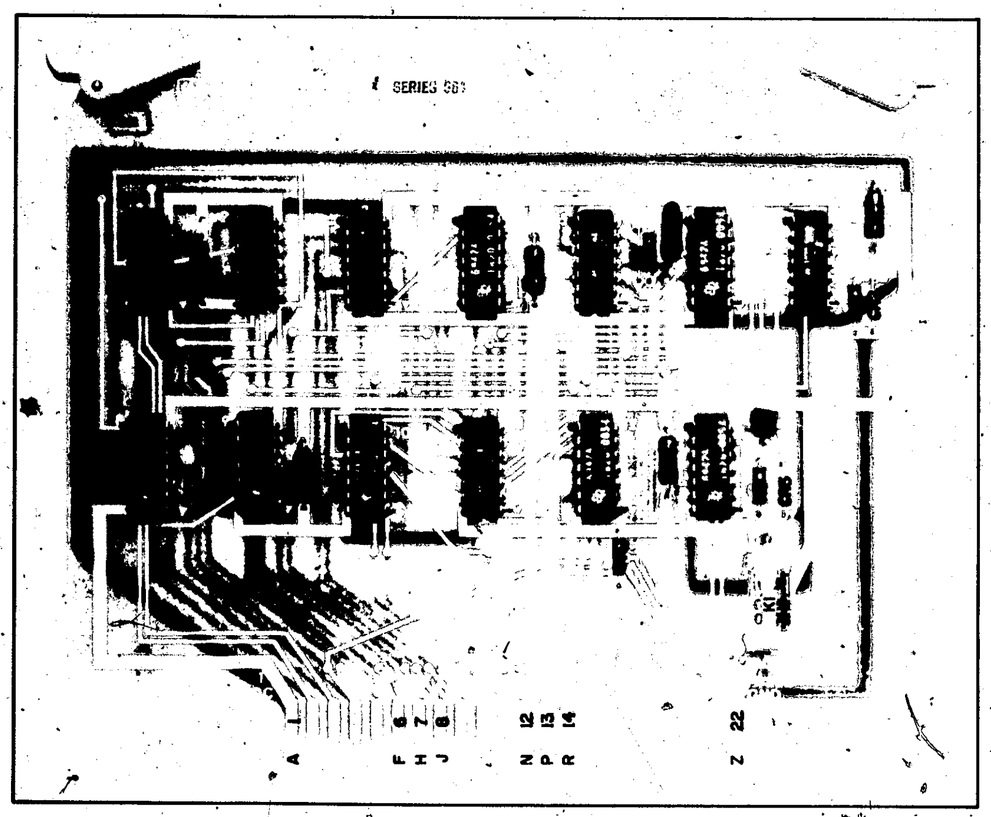
CHANGES FOR OLDER BOARDS

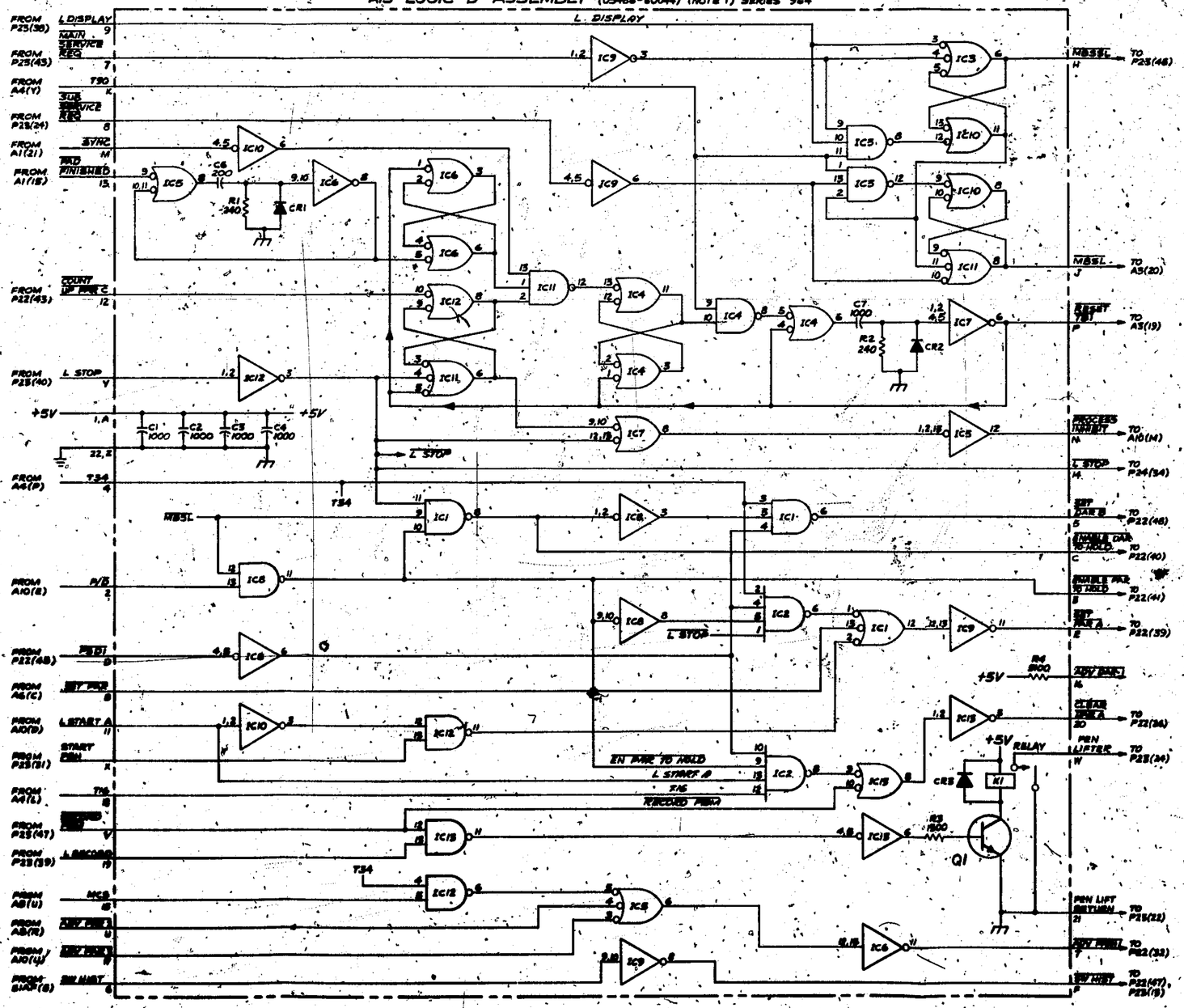
Current Board (5486B only): 05486-60044

Older Boards (5486A only): 05486-60015, Series 832 and 852

The current board, used in 5486B's only, is not a direct replacement for the 05486-60015 boards used in 5486A's.

The Series 852 05486-60015 board can be used as a replacement for the Series 832 05486-60015 board.





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS;

REFERENCE DESIGNATIONS

A13
C1 - 4, 6, 7 CR1 - 3 IC1 - 15 K1 Q1 R1 - 4

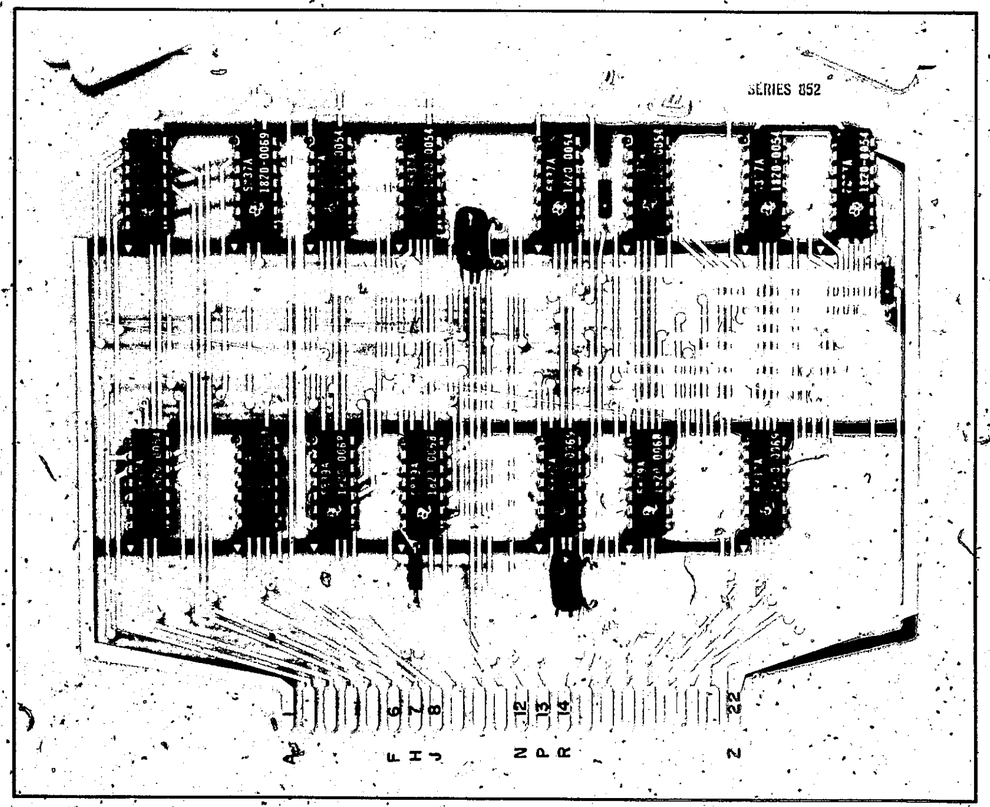
TABLE

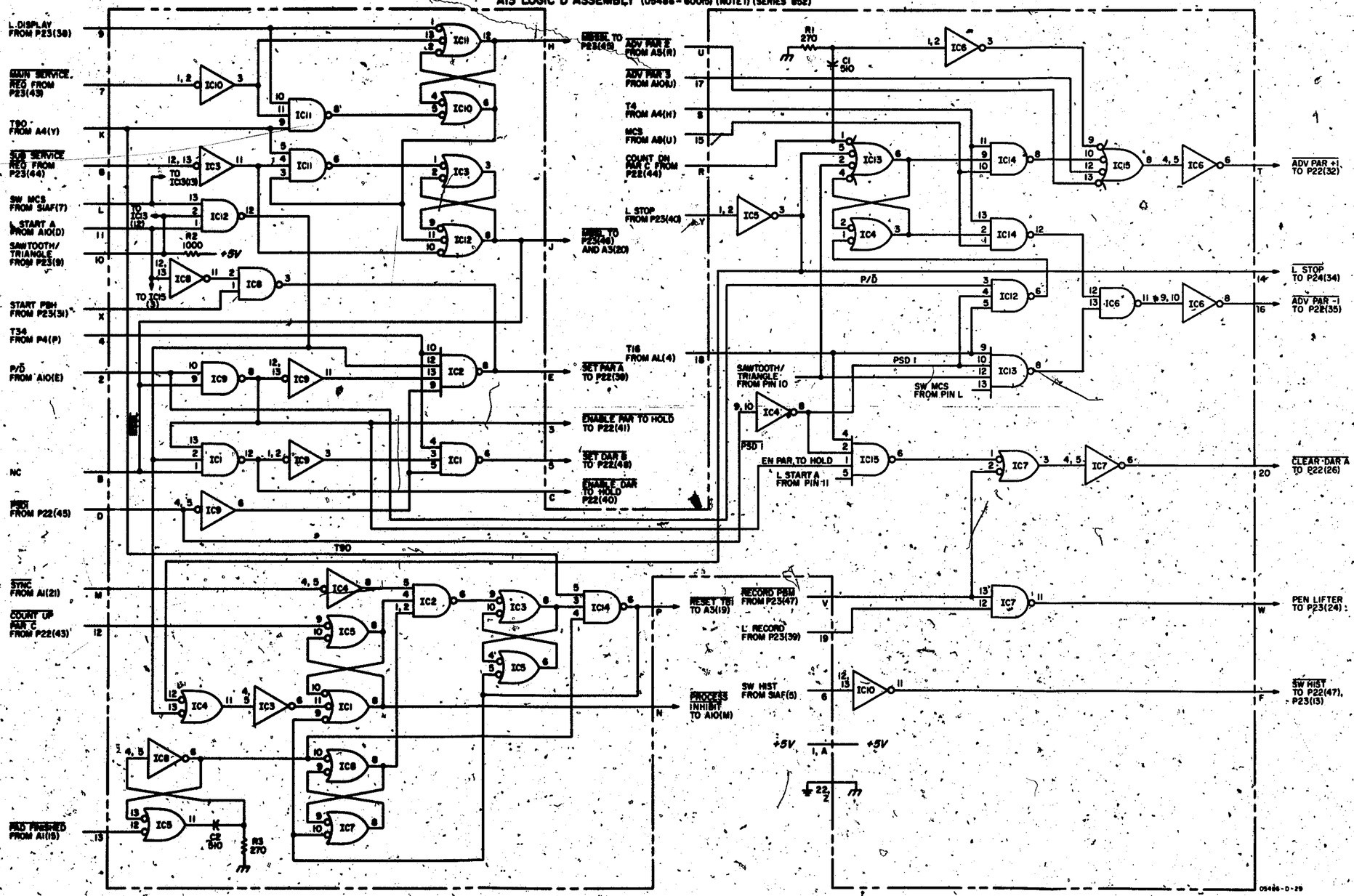
REFERENCE DESIGNATIONS	PART NUMBERS
CR1 - 3	1901 - 0040
IC1, 5, 6, 11	1820 - 0068
2	1820 - 0069
4, 6, 8, 9, 10, 12, 13	1820 - 0054
7	1820 - 0071
Q1	1854 - 0071

05486-B-28

Figure 4-28
A13 Logic D Series 964

See Figure 4-28 for Board description.





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS.

REFERENCE DESIGNATIONS

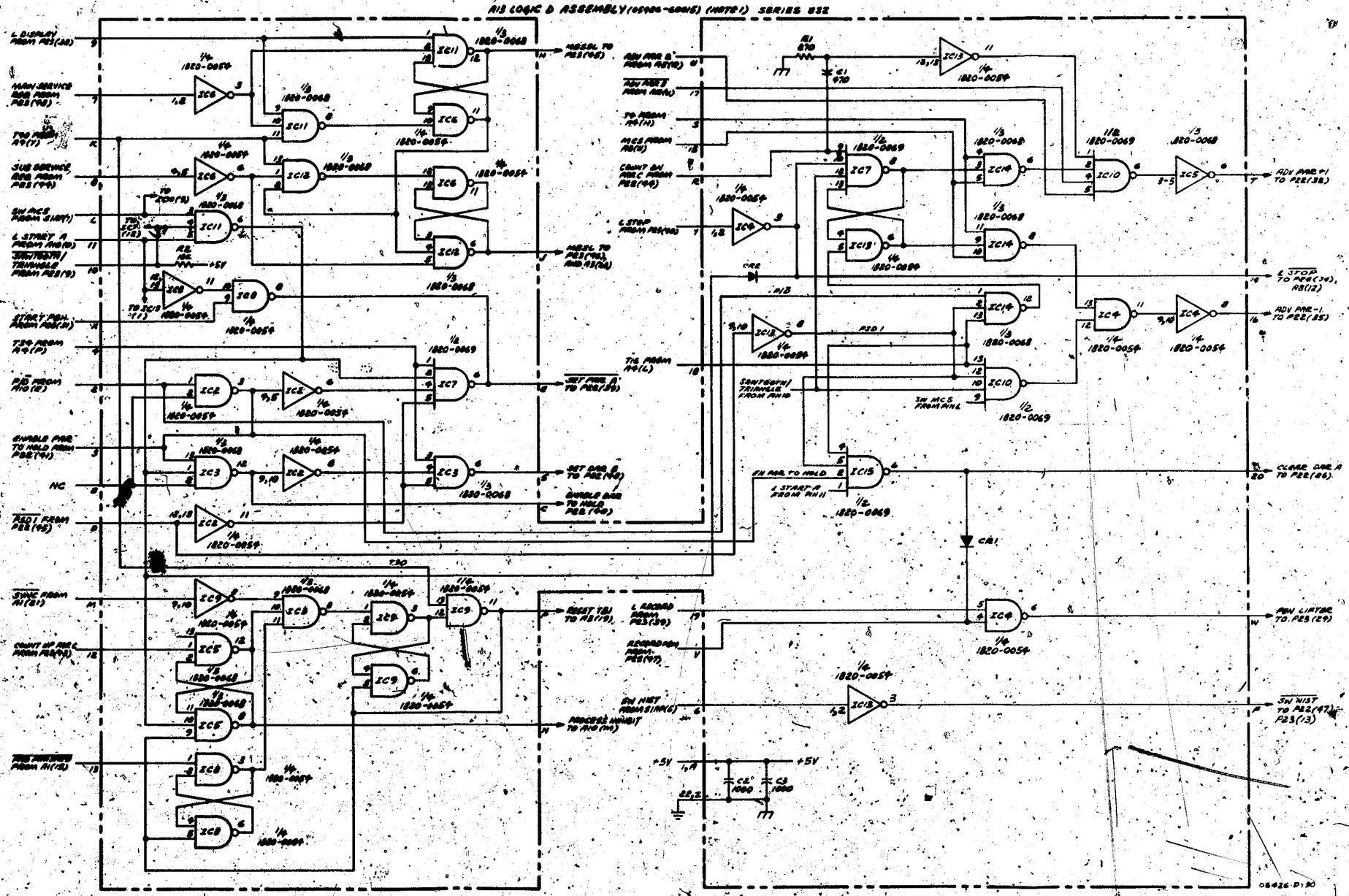
A13
C1, 2
IC1-15
R1-3

TABLE

REFERENCE DESIGNATIONS	HP PART NUMBERS
IC1, 11, 12	1820-0068
IC2, 13, 15	1820-0069
IC3-10	1820-0054

Figure 4-29
A13 Logic D Series 852

See Figure 4-28 for A13 Board description.



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;

REFERENCE DESIGNATIONS

A13 #
C1-3 CR1,2 IC2-15 R1,2

Figure 4-30
A13 Logic D Series 832

END