Practical Submission Sheet

Term: 2020-1
Lecture Date: October 16, 2020.
Course Code: PHY249
Registration Number: 11912610
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Submission Date: October 16, 2020
Practical Number: 8
Section: G2903
Roll No: 03

Aim

To create XOR and NOT gates using NAND logic.

Concepts Learnt

Key Observations & Insights

Application Areas

Report

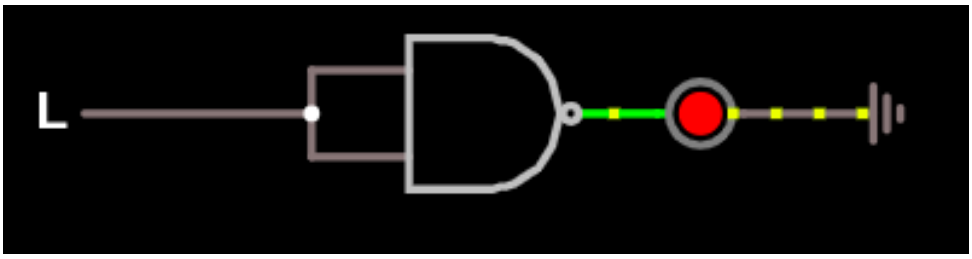

Figure 1: NAND combination for constructing the NOT (inverter) gate.

Input	Output
0	1
1	0

Table 1: Truth table for the NAND combination. It can be seen that it behaves identically to a NOT gate.

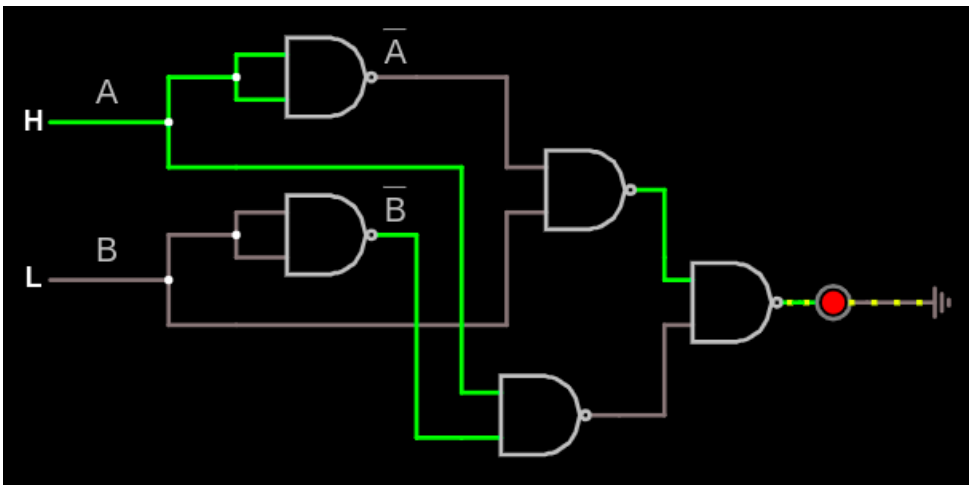

Figure 2: NAND logic for the XOR gate.

Input A	Input B	Output
0	0	0
0	0	1
0	1	1
0	1	0

Table 2: Truth table for the logic system in Figure 2

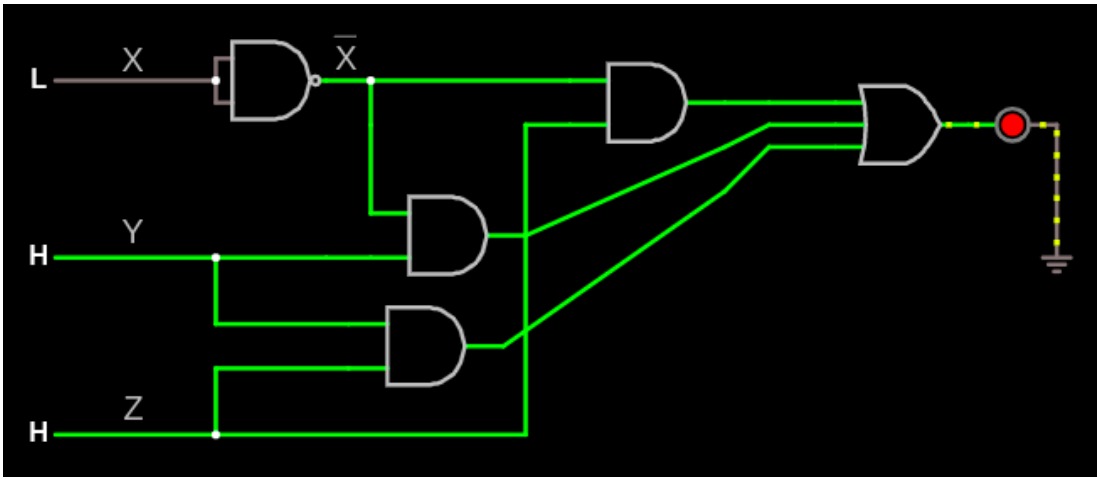

Figure 3: $f = \overline{X}.Y + \overline{X}.Z + Y.Z$