Practical Submission Sheet

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Course Code: PHY249
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Aim

To create a logic circuit based on given boolean expressions

(i) $z = [A \cdot (\overline{B} + C) + D] \cdot \bar{B} + C \cdot D$

(ii) $f = x + \overline{x}.\overline{(y + z)} + \overline{y}.(\overline{x} + \overline{z})$

(iii) $f = \overline{(\overline{y} + \overline{z})} + y.\overline{z} + \overline{(x.y)}$

Concepts Learnt

Realization of boolean expressions using logic gate combinations.

Key Observations & Insights

Boolean expressions for certain circuits were realized using logic gates, particular using AOI gates. Such complicated circuits can sometimes be avoided by simplifying the expression using either boolean algebra or using K-maps.

Application Areas

Often in electronics one may have to deal with complicated networks, a finger-exercise for dealing with such circuits is beneficial.

Report

For expression (i), an AOI gate combination was simulated as depicted in the figure below.

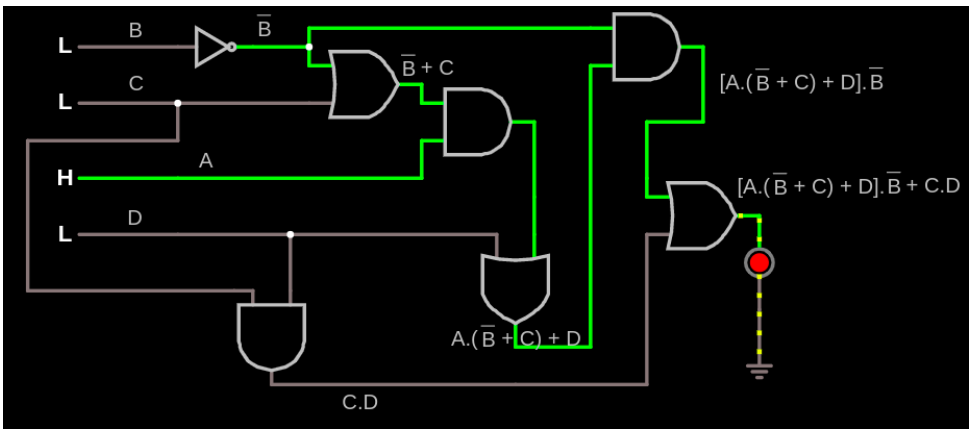

Figure 1: Logic gate combination for the boolean expression (i)

The truth table for the boolean function z is then

Input A	Input B	Input C	Input D	Output (z)
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Table 1: Truth table for the logic corresponding to the boolean expression $z = [A \cdot (\overline{B} + C) + D] \cdot \bar{B} + C \cdot D$.

Expression (ii) can be realised using the following circuit

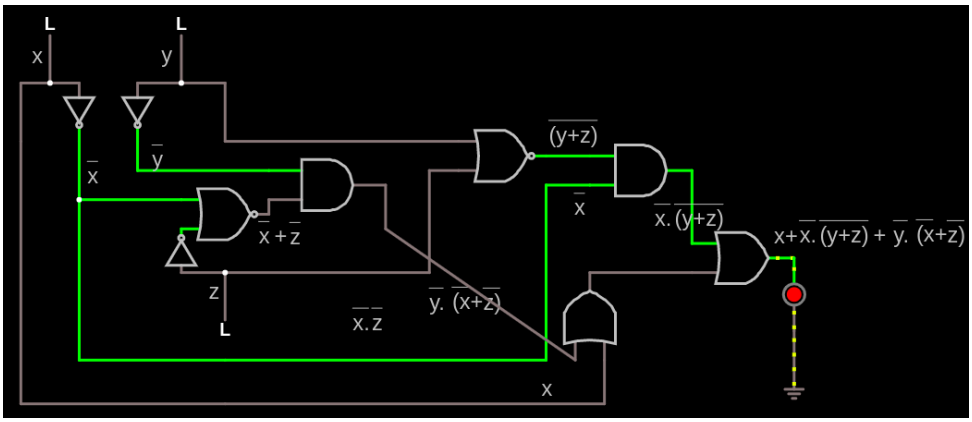

Figure 2: AOI logic circuit corresponding to the expression $f = x + \overline{x}.\overline{(y+z)} + \overline{y}.(\overline{x} + \overline{z})$

The truth table for this logic system is slightly surprisingly

Input x	Input y	Input x	Output (f)
0	0	0	1
0	0	1	1
0	1	0	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Table 2: Truth table for the logic system $f = x + \overline{x}.\overline{(y+z)} + \overline{y}.(\overline{x} + \overline{z})$.

and it can be verified mathematically by reducing the boolean expression, resulting in $f = 1$ for all cases.
For the third and final expression, the boolean logic was realised using the 3 input circuit shown in Figure 3.

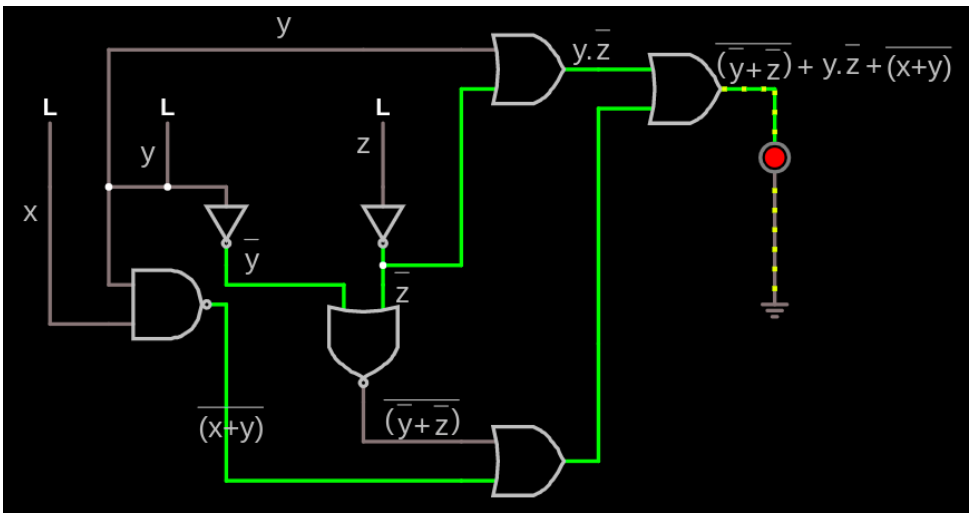

Figure 3: Circuit diagram for the logic system $f = \overline{(\overline{y} + \overline{z})} + y.\overline{z} + \overline{(x.y)}$

Again this expression, when reduced, leads to $f = 1$ and thus all output entries in the truth table are 1, as in table 3.

Input x	Input y	Input x	Output (f)
0	0	0	1
0	0	1	1
0	1	0	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Table 3: Truth table for the logic system $f = \overline{(\overline{y} + \overline{z})} + y.\overline{z} + \overline{(x.y)}$.