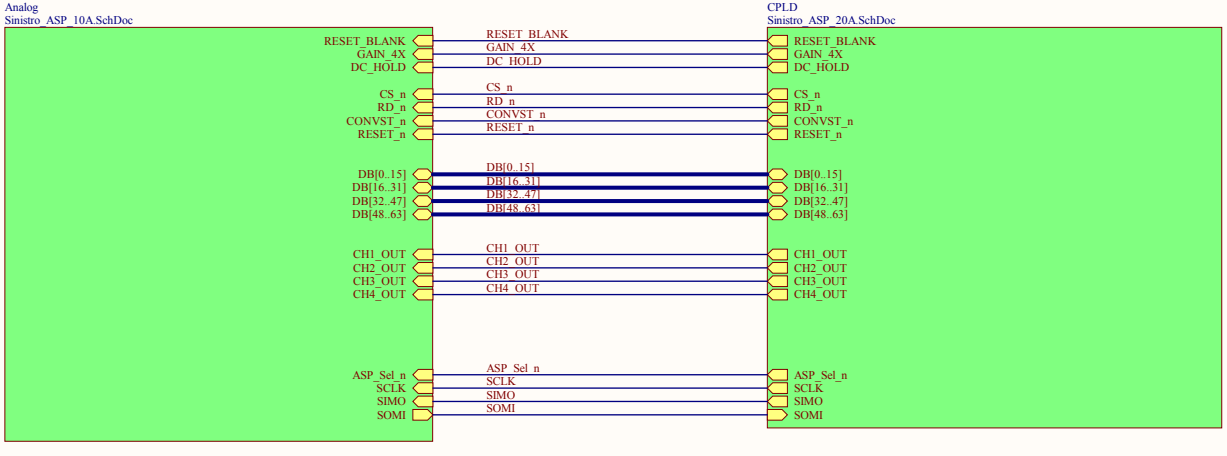
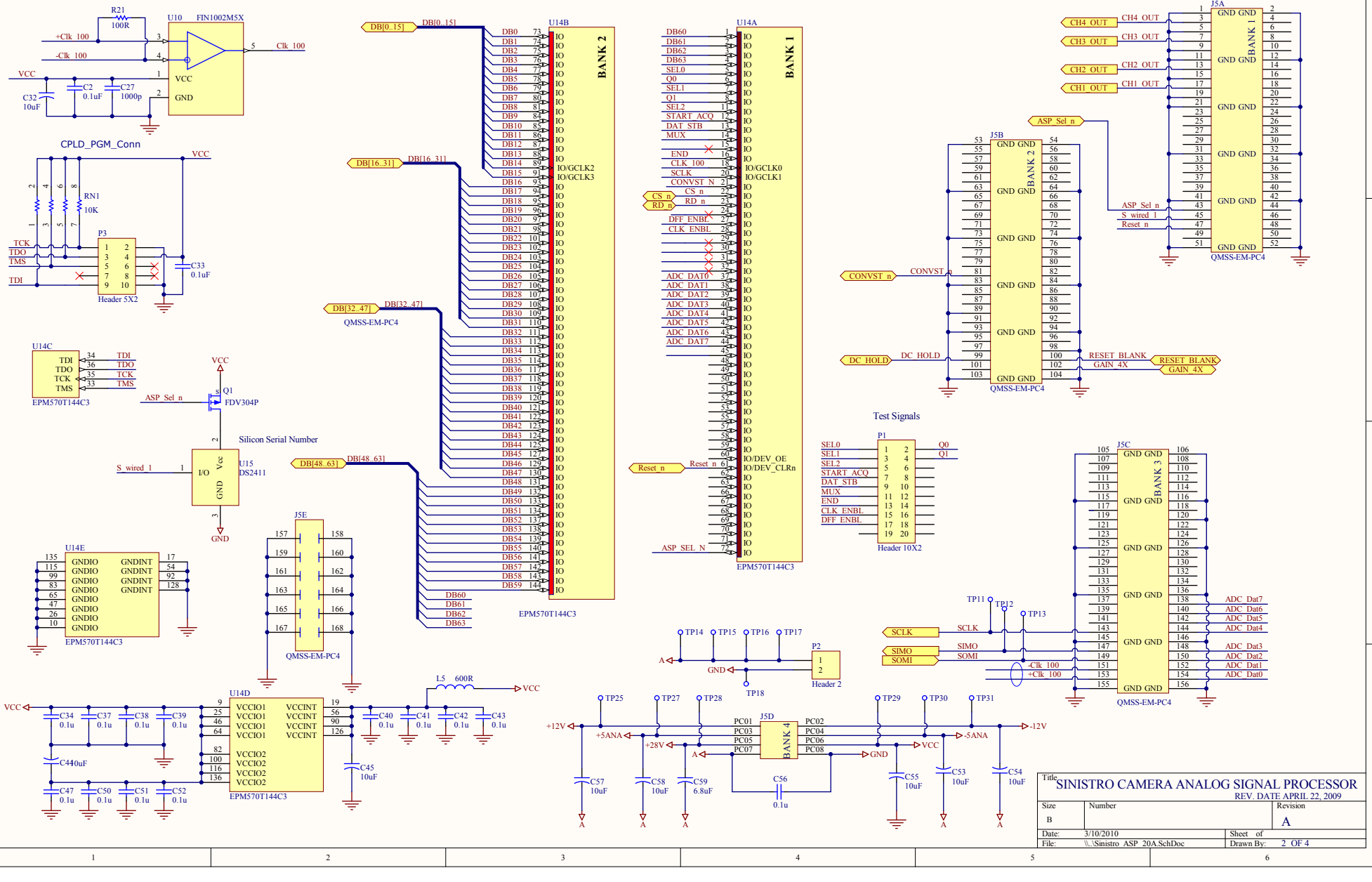
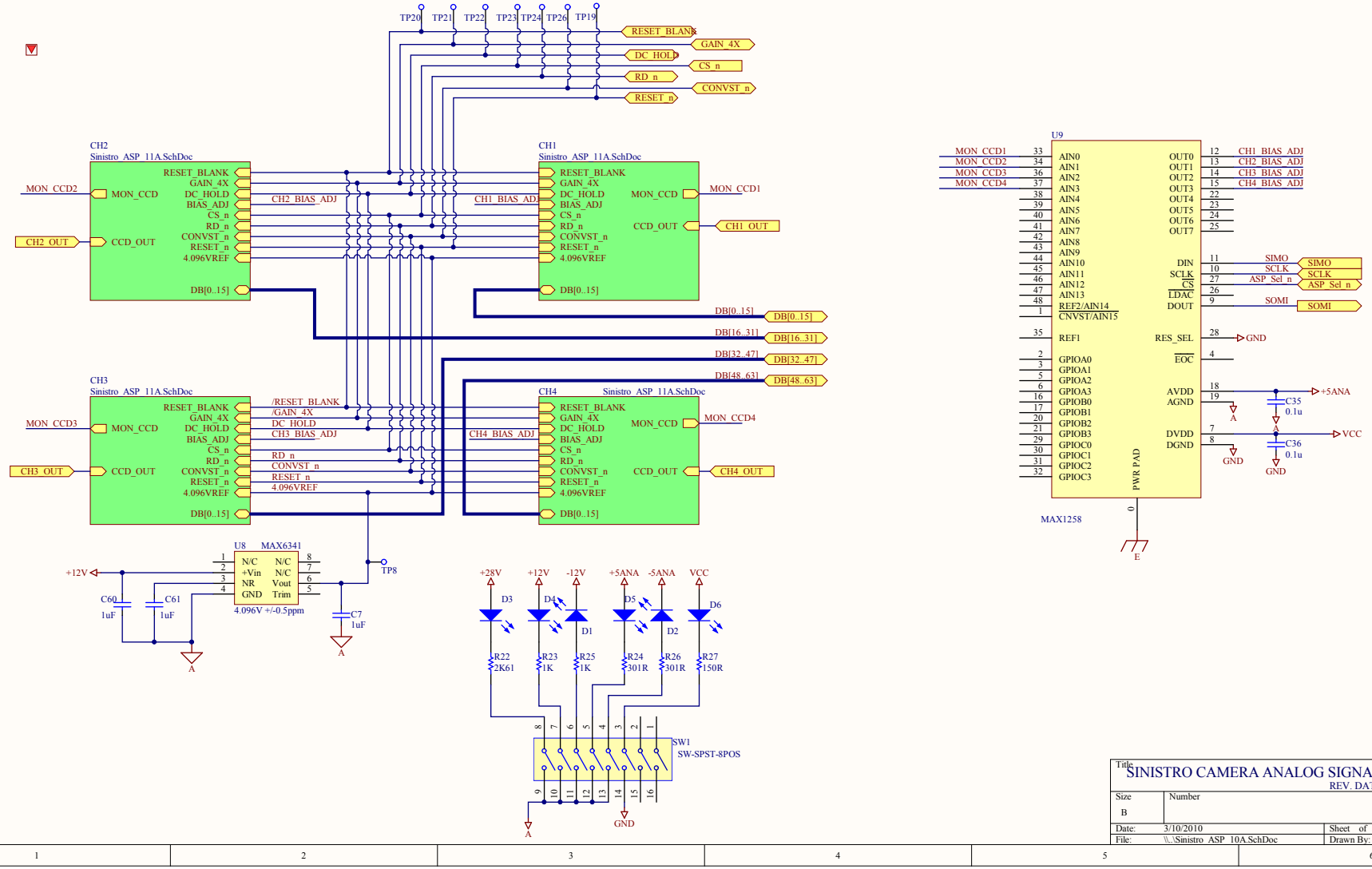
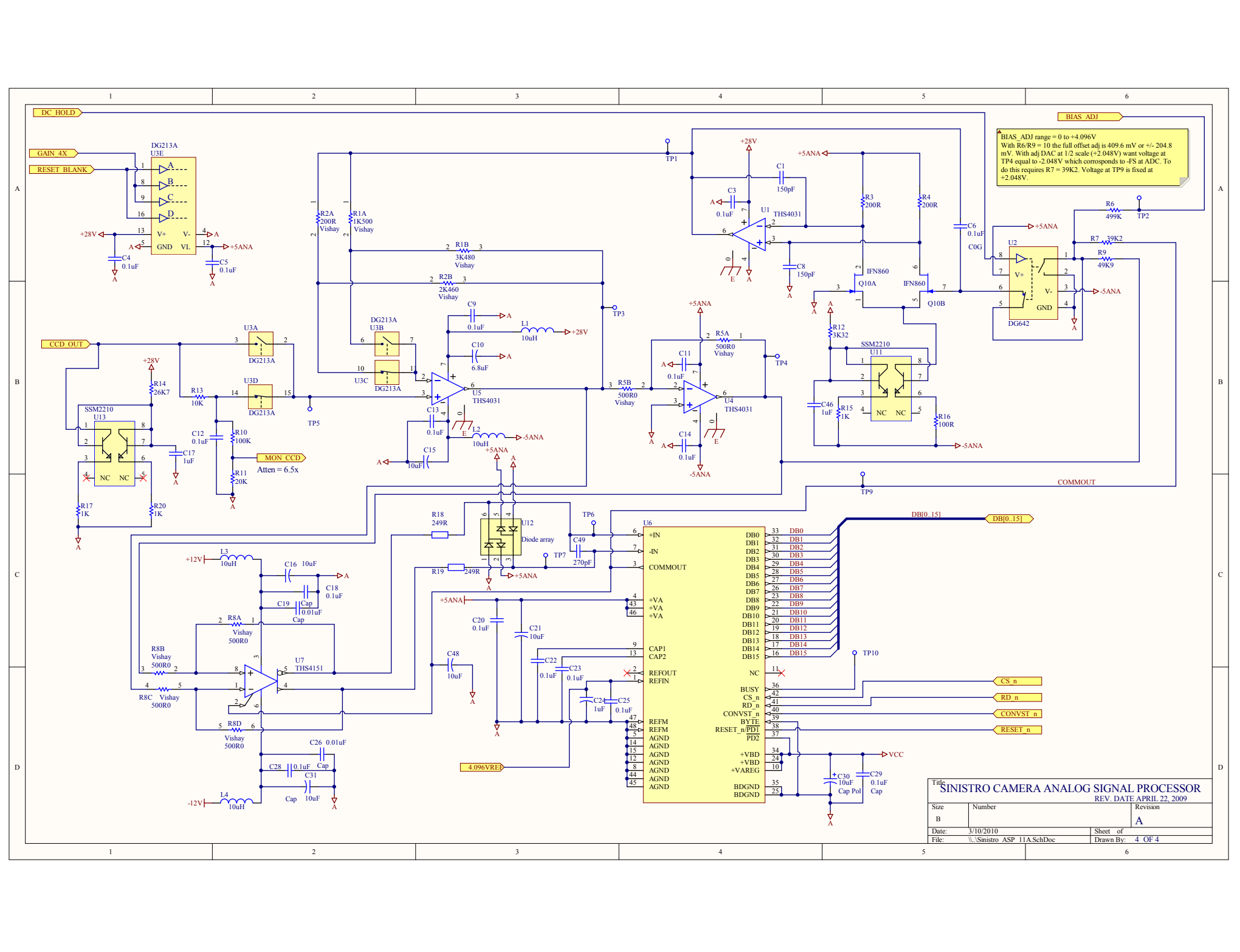


Title	SINISTRO CAMERA ANALOG SIGNAL PROCESSOR REV. DATE APRIL 22, 2009		
Size B	Number		Revision A
Date:	3/10/2010	Sheet of	
File:	\\..\Sinistro_ASP_00A.SchDoc	Drawn By:	1 OF 4


R21
100R
U10
FIN1002M5X
+Clk_100
-Clk_100
Clk_100
VCC
GND
C32
10uF
C2
0.1uF
C27
1000p
CPLD_PGM_Conn
RN1
10K
P3
Header 5X2
TCK
TDO
TMS
TDI
C33
0.1uF
U14C
EPM570T144C3
ASP_Sel_n
Q1
FDV304P
Silicon Serial Number
S_wired_1
U15
DS2411
I/O
Vcc
GND
U14E
GNDIO
GNDINT
J5E
QMSS-EM-PC4
U14D
VCCIO1
VCCIO2
VCCINT
L5 600R
C34
C37
C38
C39
C40
C41
C42
C43
C44
40uF
C45
10uF
C47
C50
C51
C52
U14B
BANK 2
DB[0..15]
DB[16..31]
DB[32..47]
DB[48..63]
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
DB10
DB11
DB12
DB13
DB14
DB15
DB16
DB17
DB18
DB19
DB20
DB21
DB22
DB23
DB24
DB25
DB26
DB27
DB28
DB29
DB30
DB31
DB32
DB33
DB34
DB35
DB36
DB37
DB38
DB39
DB40
DB41
DB42
DB43
DB44
DB45
DB46
DB47
DB48
DB49
DB50
DB51
DB52
DB53
DB54
DB55
DB56
DB57
DB58
DB59
DB60
DB61
DB62
DB63
IO/GCLK2
IO/GCLK3
U14A
BANK 1
DB60
DB61
DB62
DB63
SEL0
Q0
SEL1
Q1
SEL2
START_ACQ
DAT_STB
MUX
END
CLK_100
SCLK
CONVST_N
CS_n
RD_n
DFF_ENBL
CLK_ENBL
ADC_DAT0
ADC_DAT1
ADC_DAT2
ADC_DAT3
ADC_DAT4
ADC_DAT5
ADC_DAT6
ADC_DAT7
Reset_n
ASP_SEL_N
IO/GCLK0
IO/GCLK1
IO/DEV_OE
IO/DEV_CLRn
EPM570T144C3
Test Signals
P1
Header 10X2
SEL0
SEL1
SEL2
START_ACQ
DAT_STB
MUX
END
CLK_ENBL
DFF_ENBL
Q0
Q1
J5A
CH4_OUT
CH3_OUT
CH2_OUT
CH1_OUT
GND GND
BANK 1
QMSS-EM-PC4
J5B
BANK 2
ASP_Sel_n
S_wired_1
Reset_n
CONVST_n
DC_HOLD
RESET_BLANK
GAIN_4X
J5C
BANK 3
ADC_Dat7
ADC_Dat6
ADC_Dat5
ADC_Dat4
ADC_Dat3
ADC_Dat2
ADC_Dat1
ADC_Dat0
TP11
TP12
TP13
SCLK
SIMO
SOMI
-Clk_100
+Clk_100
TP14
TP15
TP16
TP17
TP18
P2
Header 2
J5D
BANK 4
PC01
PC02
PC03
PC04
PC05
PC06
PC07
PC08
TP25
TP27
TP28
TP29
TP30
TP31
+12V
+5ANA
+28V
-5ANA
-12V
C57
10uF
C58
10uF
C59
6.8uF
C56
0.1uF
C55
10uF
C53
10uF
C54
10uF
Title
SINISTRO CAMERA ANALOG SIGNAL PROCESSOR
REV. DATE APRIL 22, 2009
Size
B
Number
Revision
A
Date:
3/10/2010
Sheet of
File:
\\..\Sinistro_ASP_20A.SchDoc
Drawn By:
2_OF 4



Title	SINISTRO CAMERA ANALOG SIGNAL PROCESSOR REV. DATE APRIL 22, 2009	
Size: B	Number:	Revision: A
Date: 3/10/2010		Sheet of: 3 OF 4
File: \\..\Sinistro_ASP_10A.SchDoc		Drawn By:


DC_HOLD
GAIN_4X
RESET_BLANK
BIAS_ADJ
BIAS_ADJ range = 0 to +4.096V
With R6/R9 = 10 the full offset adj is 409.6 mV or +/- 204.8 mV. With adj DAC at 1/2 scale (+2.048V) want voltage at TP4 equal to -2.048V which corresponds to -FS at ADC. To do this requires R7 = 39K2. Voltage at TP9 is fixed at +2.048V.
CCD_OUT
MON_CCD
Atten = 6.5x
COMMOUT
DB[0..15]
CS_n
RD_n
CONVST_n
RESET_n
4.096VREF
VCC
DG213A
THS4031
THS4151
SSM2210
DG642
IFN860
Diode array
SINISTRO CAMERA ANALOG SIGNAL PROCESSOR
REV. DATE APRIL 22, 2009
Size B
Number
Revision A
Date: 3/10/2010
Sheet of
File: \\..\Sinistro_ASP_11A.SchDoc
Drawn By:
4 OF 4