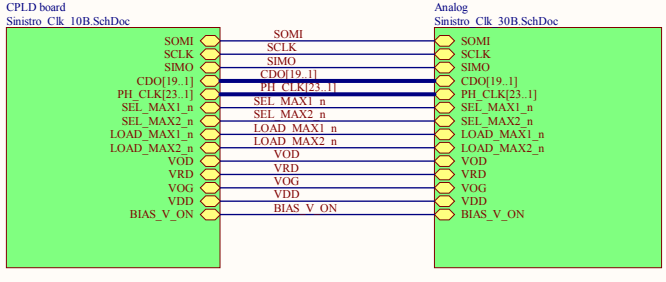

Title	SINISTRO CAMERA CLOCK DRIVER REV. DATE MARCH 9, 2010		
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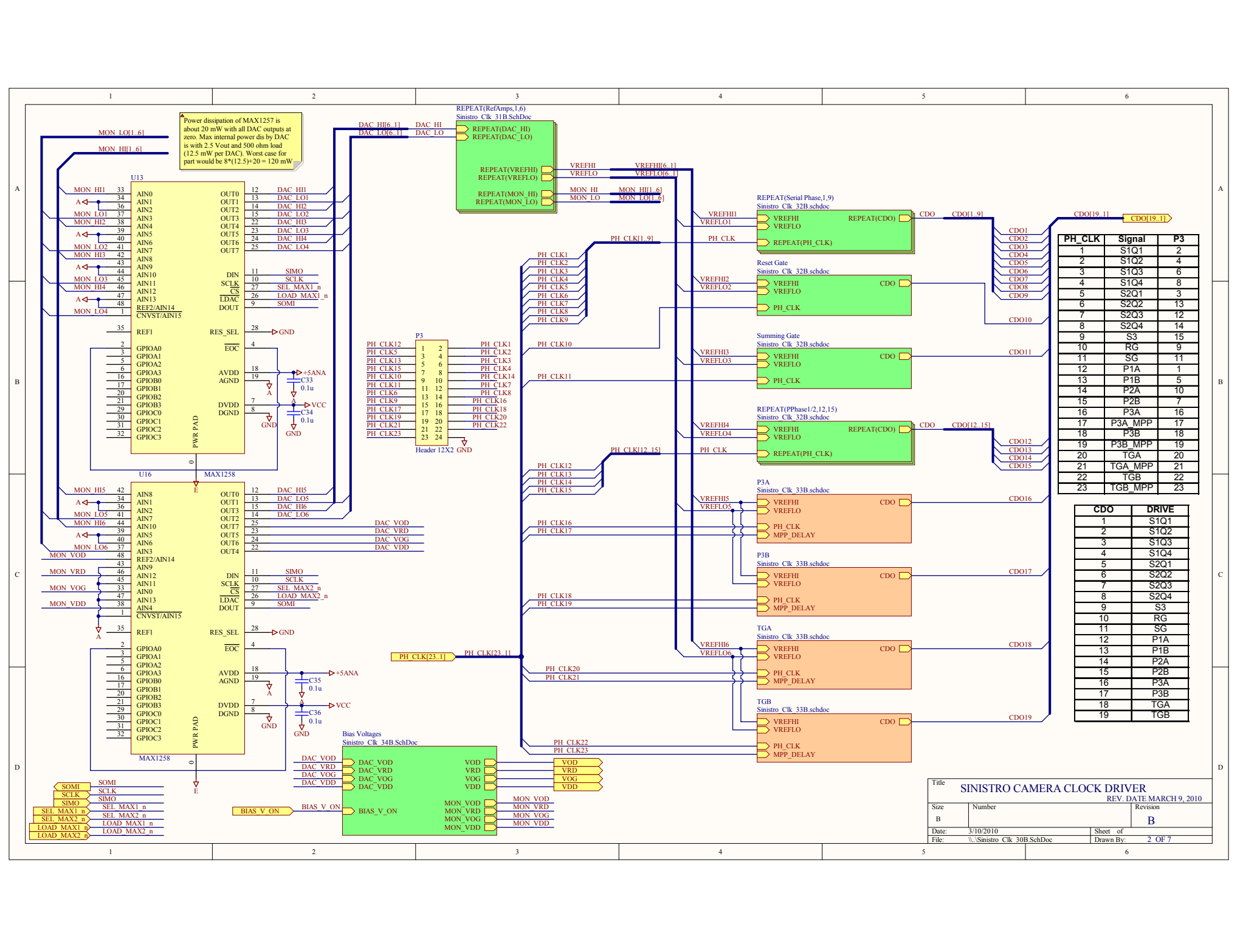
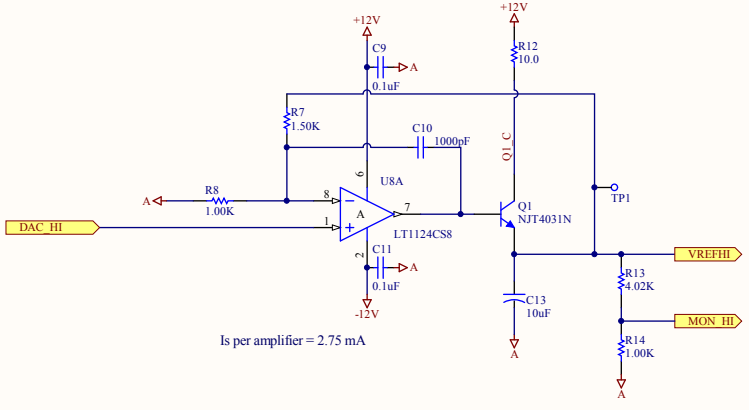


PH_CLK	Signal	P3
1	S1Q1	2
2	S1Q2	4
3	S1Q3	6
4	S1Q4	8
5	S2Q1	3
6	S2Q2	13
7	S2Q3	12
8	S2Q4	14
9	S3	15
10	RG	9
11	SG	11
12	P1A	1
13	P1B	5
14	P2A	10
15	P2B	7
16	P3A	16
17	P3A_MPP	17
18	P3B	18
19	P3B_MPP	19
20	TGA	20
21	TGA_MPP	21
22	TGB	22
23	TGB_MPP	23

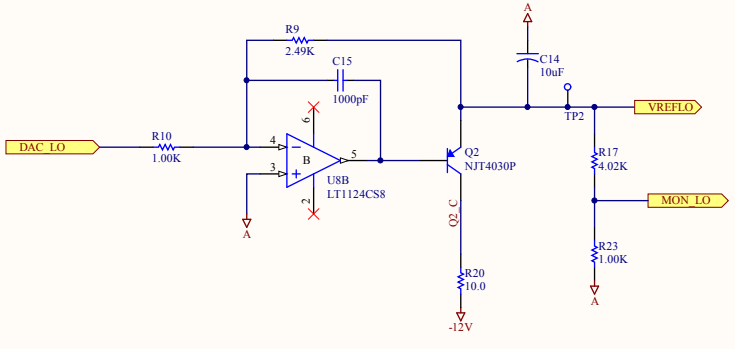
CDO	DRIVE
1	S1Q1
2	S1Q2
3	S1Q3
4	S1Q4
5	S2Q1
6	S2Q2
7	S2Q3
8	S2Q4
9	S3
10	RG
11	SG
12	P1A
13	P1B
14	P2A
15	P2B
16	P3A
17	P3B
18	TGA
19	TGB



Is per amplifier = 2.75 mA

Max quiescent pwr for U8 = 132 mW

Max q pwr for Q1 or Q2 (+6V/-6V out) = 21.6 mW



Power Dissipation (worst case)

	U8	Q1 or Q2 quiescent (Vout = +/- 6V)	Q1 or Q2 Load* (Vout = +/- 6V)	Total W (U8 + Q1 +Q2)
VREFHI/LO 1	132mW	21.6mW	319 mW	814 mW
VREFHI/LO 2	"	"	neg	175 mW
VREFHI/LO 3	"	"	neg	175 mW
VREFHI/LO 4	"	"	406 mW	988 mW
VREFHI/LO 5	"	"	288 mW	752 mW
VREFHI/LO 6	"	"	9.2 mW	194 mW
				2.92 W

*1 MHz pixel rate/all quadrants clocked

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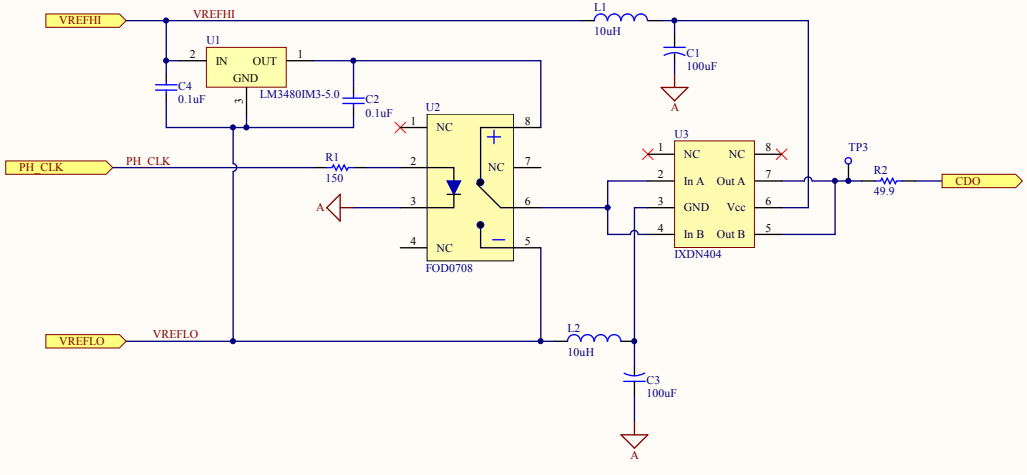
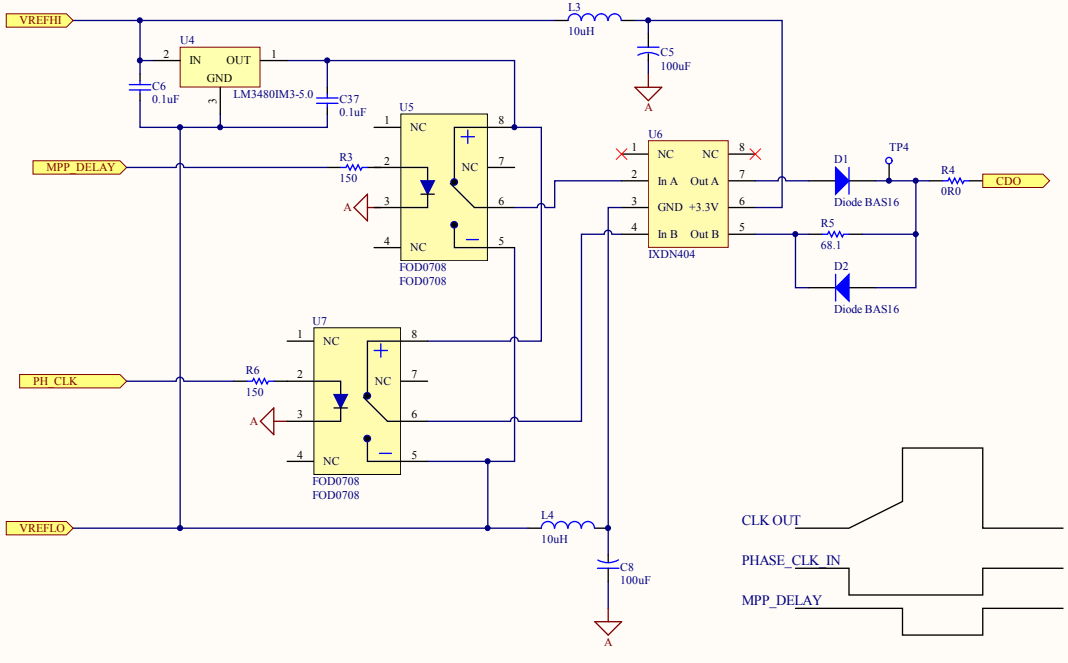


Title	SINISTRO CAMERA CLOCK DRIVER REV. DATE MARCH 9, 2010	
Size: B	Number:	Revision: B
Date: 3/10/2010		Sheet of: 4 OF 7
File: \\..\Sinistro Clk 32B.SchDoc		Drawn By:



Title	SINISTRO CAMERA CLOCK DRIVER REV. DATE MARCH 9, 2010	
Size: B	Number	Revision: B
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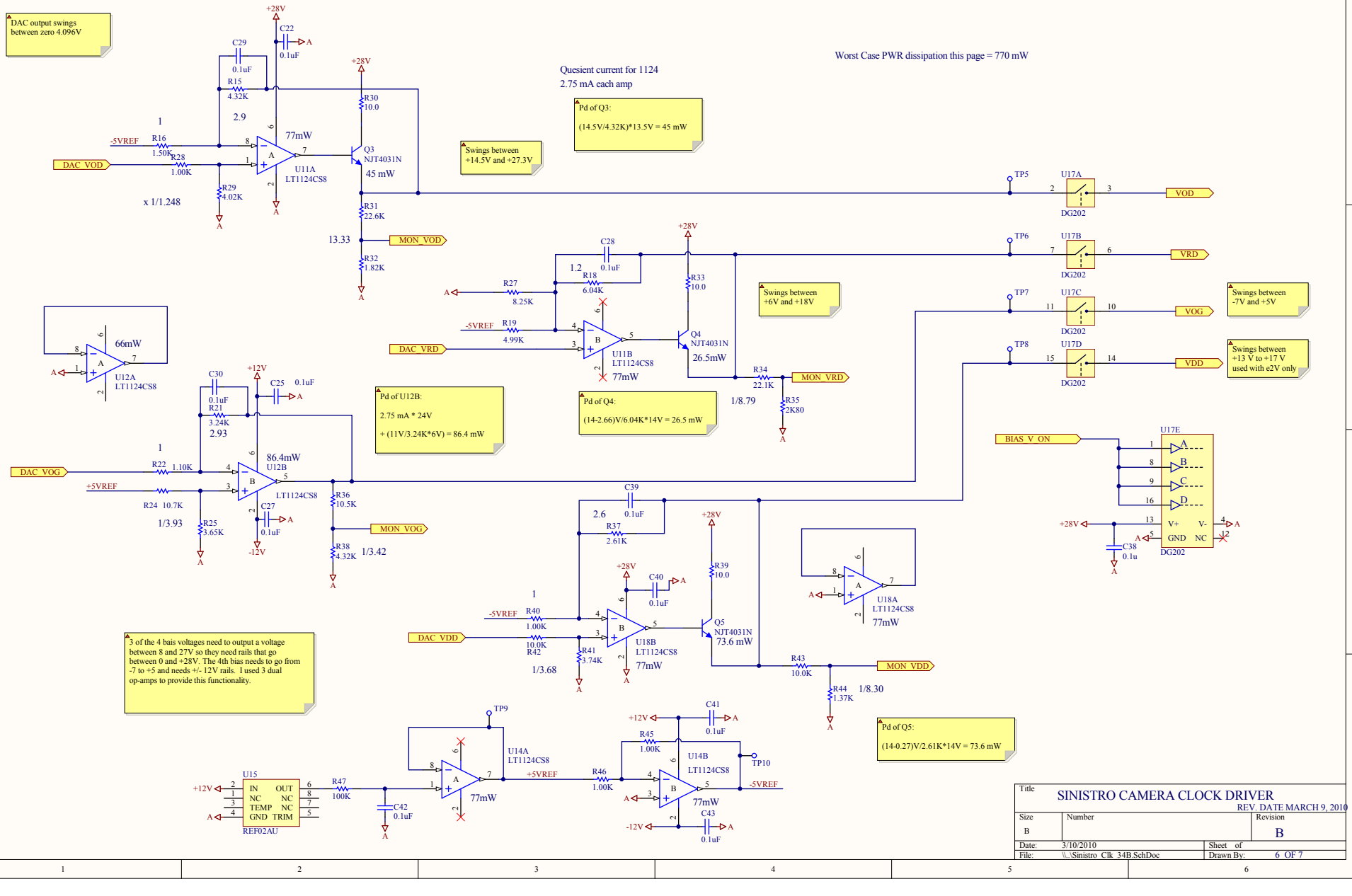
File: \\..\Sinistro_Clk_33B.SchDoc		Drawn By: 5_OF 7


DAC output swings between zero 4.096V
Worst Case PWR dissipation this page = 770 mW
Quesient current for 1124
2.75 mA each amp
Pd of Q3:
(14.5V/4.32K)*13.5V = 45 mW
Swings between +14.5V and +27.3V
Swings between +6V and +18V
Swings between -7V and +5V
Swings between +13 V to +17 V used with e2V only
Pd of U12B:
2.75 mA * 24V
+ (11V/3.24K*6V) = 86.4 mW
Pd of Q4:
(14-2.66)V/6.04K*14V = 26.5 mW
Pd of Q5:
(14-0.27)V/2.61K*14V = 73.6 mW
3 of the 4 bais voltages need to output a voltage between 8 and 27V so they need rails that go between 0 and +28V. The 4th bias needs to go from -7 to +5 and needs +/- 12V rails. I used 3 dual op-amps to provide this functionality.
+28V
+12V
-12V
-5VREF
+5VREF
DAC_VOD
DAC_VRD
DAC_VOG
DAC_VDD
BIAS_V_ON
MON_VOD
MON_VRD
MON_VOG
MON_VDD
VOD
VRD
VOG
VDD
U11A LT1124CS8
U11B LT1124CS8
U12A LT1124CS8
U12B LT1124CS8
U14A LT1124CS8
U14B LT1124CS8
U18A LT1124CS8
U18B LT1124CS8
U15 REF02AU
U17A DG202
U17B DG202
U17C DG202
U17D DG202
U17E DG202
Q3 NJT4031N
Q4 NJT4031N
Q5 NJT4031N
77mW
45 mW
66mW
86.4mW
26.5mW
73.6 mW
x 1/1.248
1/3.93
1/3.42
1/3.68
1/8.30
1/8.79
Title
SINISTRO CAMERA CLOCK DRIVER
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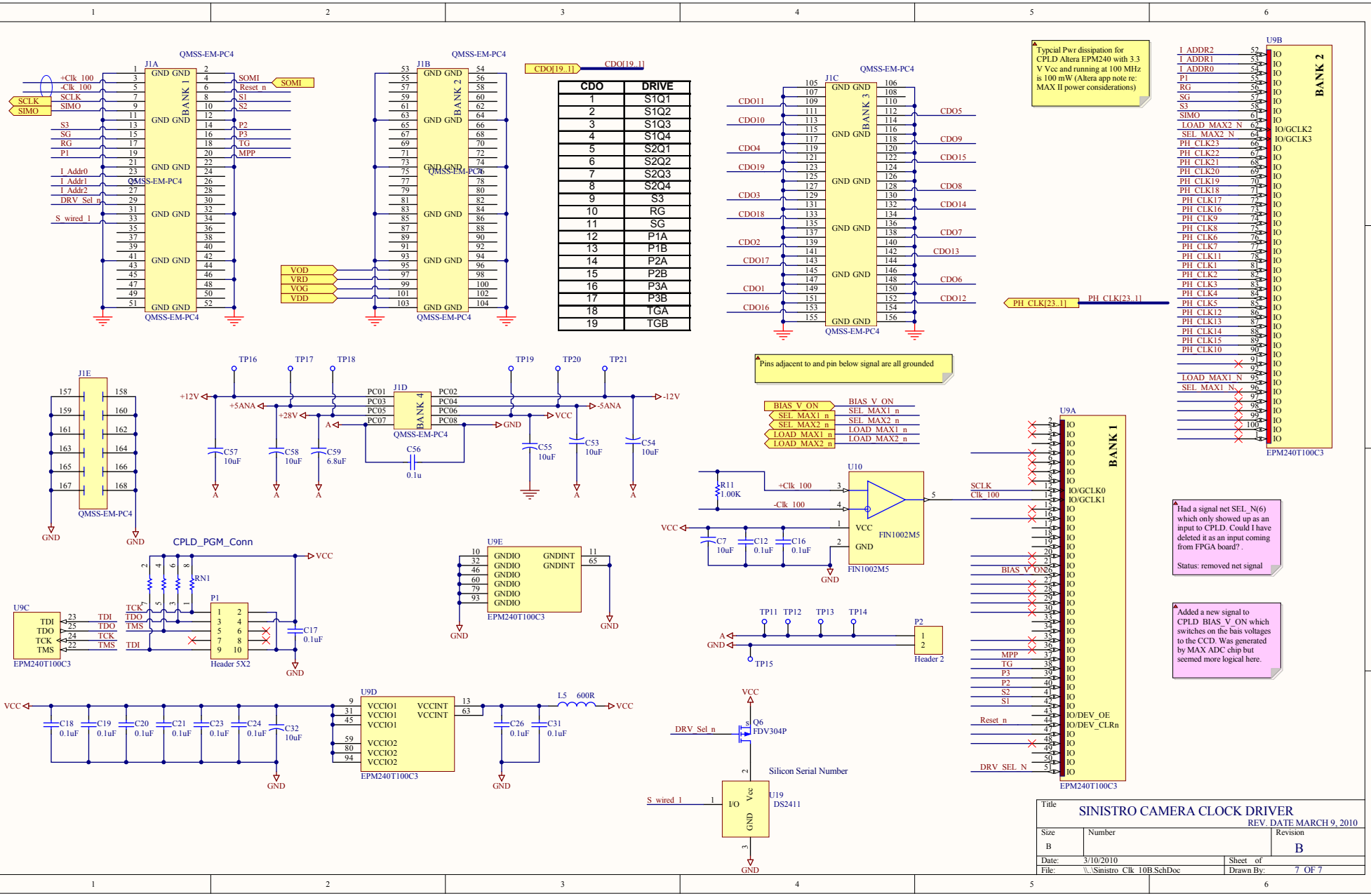
J1A
QMSS-EM-PC4
BANK 1
+Clk_100
-Clk_100
SCLK
SIMO
S3
SG
RG
P1
I_Addr0
I_Addr1
I_Addr2
DRV_Sel_n
S_wired_1
SOMI
Reset_n
S1
S2
P2
P3
TG
MPP
GND
J1B
BANK 2
VOD
VRD
VOG
VDD
CDO[19..1]
CDO
DRIVE
1 S1Q1
2 S1Q2
3 S1Q3
4 S1Q4
5 S2Q1
6 S2Q2
7 S2Q3
8 S2Q4
9 S3
10 RG
11 SG
12 P1A
13 P1B
14 P2A
15 P2B
16 P3A
17 P3B
18 TGA
19 TGB
J1C
BANK 3
CDO11
CDO10
CDO4
CDO19
CDO3
CDO18
CDO2
CDO17
CDO1
CDO16
CDO5
CDO9
CDO15
CDO8
CDO14
CDO7
CDO13
CDO6
CDO12
Typcial Pwr dissipation for CPLD Altera EPM240 with 3.3 V Vcc and running at 100 MHz is 100 mW (Altera app note re: MAX II power considerations)
U9B
BANK 2
I_ADDR2
I_ADDR1
I_ADDR0
P1
RG
SG
S3
SIMO
LOAD_MAX2_N
SEL_MAX2_N
PH_CLK23
PH_CLK22
PH_CLK21
PH_CLK20
PH_CLK19
PH_CLK18
PH_CLK17
PH_CLK16
PH_CLK9
PH_CLK8
PH_CLK6
PH_CLK7
PH_CLK11
PH_CLK1
PH_CLK2
PH_CLK3
PH_CLK4
PH_CLK5
PH_CLK12
PH_CLK13
PH_CLK14
PH_CLK15
PH_CLK10
LOAD_MAX1_N
SEL_MAX1_N
IO/GCLK2
IO/GCLK3
EPM240T100C3
PH_CLK[23..1]
J1E
TP16
TP17
TP18
TP19
TP20
TP21
+12V
+5ANA
+28V
-5ANA
-12V
VCC
GND
BANK 4
PC01
PC03
PC05
PC07
PC02
PC04
PC06
PC08
C56
0.1u
C57
10uF
C58
10uF
C59
6.8uF
C55
10uF
C53
10uF
C54
10uF
Pins adjacent to and pin below signal are all grounded
BIAS_V_ON
SEL_MAX1_n
SEL_MAX2_n
LOAD_MAX1_n
LOAD_MAX2_n
U10
FIN1002M5
R11
1.00K
+Clk_100
-Clk_100
C7
10uF
C12
0.1uF
C16
0.1uF
U9A
BANK 1
IO/GCLK0
IO/GCLK1
IO/DEV_OE
IO/DEV_CLRn
SCLK
Clk_100
BIAS_V_ON
MPP
TG
P3
P2
S2
S1
Reset_n
DRV_SEL_N
Had a signal net SEL_N(6) which only showed up as an input to CPLD. Could I have deleted it as an input coming from FPGA board? .
Status: removed net signal
Added a new signal to CPLD BIAS_V_ON which switches on the bais voltages to the CCD. Was generated by MAX ADC chip but seemed more logical here.
CPLD_PGM_Conn
U9C
TDI
TDO
TCK
TMS
RN1
P1
Header 5X2
C17
0.1uF
U9E
GNDIO
GNDINT
EPM240T100C3
TP11
TP12
TP13
TP14
TP15
P2
Header 2
U9D
VCCIO1
VCCINT
VCCIO2
C18
C19
C20
C21
C23
C24
C32
10uF
C26
C31
L5
600R
Q6
FDV304P
DRV_Sel_n
Silicon Serial Number
U19
DS2411
S_wired_1
I/O
Vcc
Title
SINISTRO CAMERA CLOCK DRIVER
REV. DATE MARCH 9, 2010
Size
B
Number
Revision
B
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