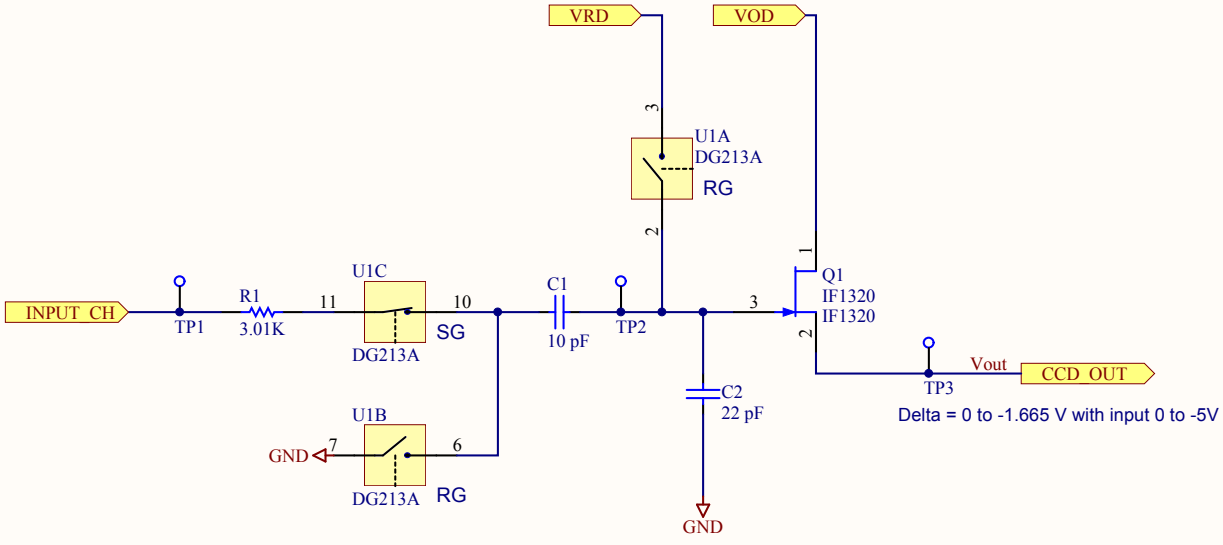

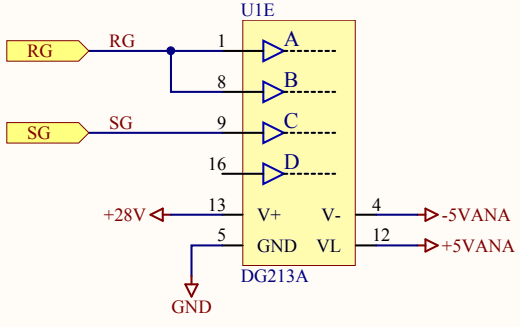

When RG is HIGH Q1 gate is charged to VRD and votlage across C1 is VRD

U1C is NC but since SG is normally high, U1 is open unless SG is pulsed LOW.

Input waveform needs to run from zero to -5V.

After Reset is finished all the switches are open.

During the SG pulse, U1C is closed which briefly samples the input voltage and the charge injected through C1 and C2 causes the summing node to jump to a new voltage. Time constant R1*C1 sets the rise time of the voltage step seen at the gate of Q1. (set initially at 100 ns).

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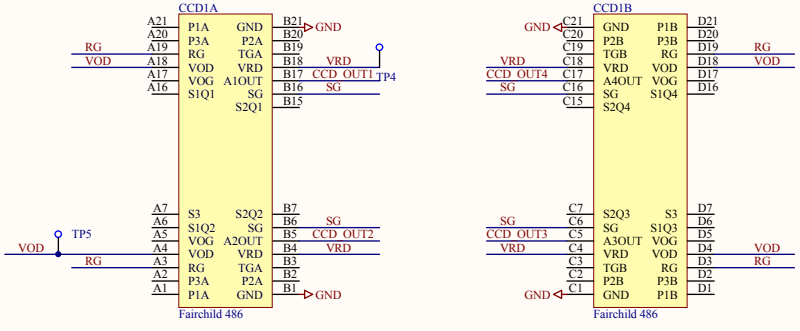
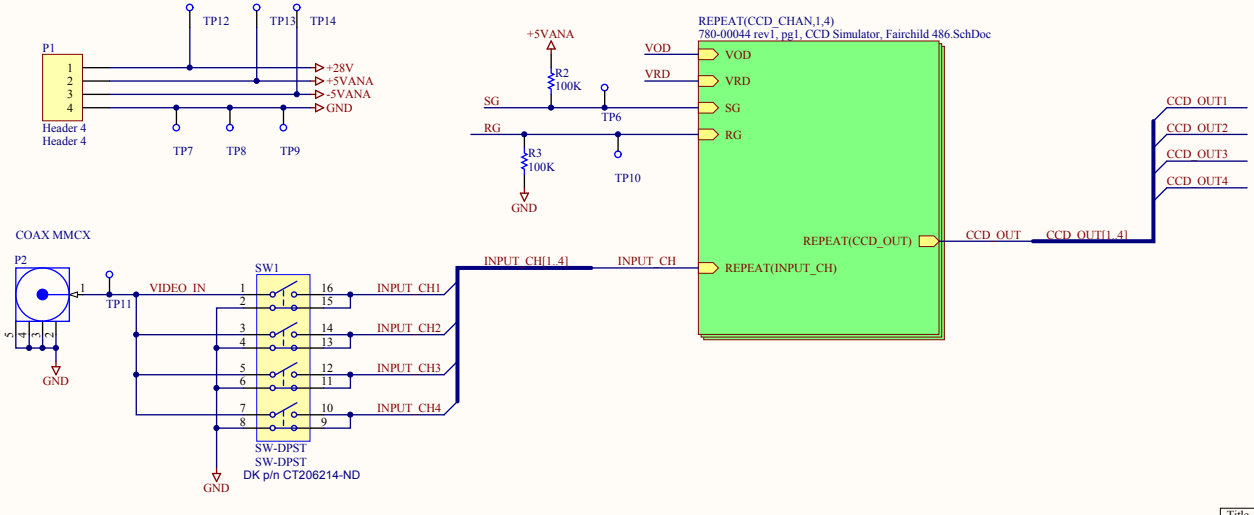
Use press-fit pins Keystone 1996-2 (0.020 pin)
3/9/2012 100 pcs @ Mouser, 700 pcs @Future





Title	SCH, CCD SIMULATOR, FAIRCHILD 486	
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