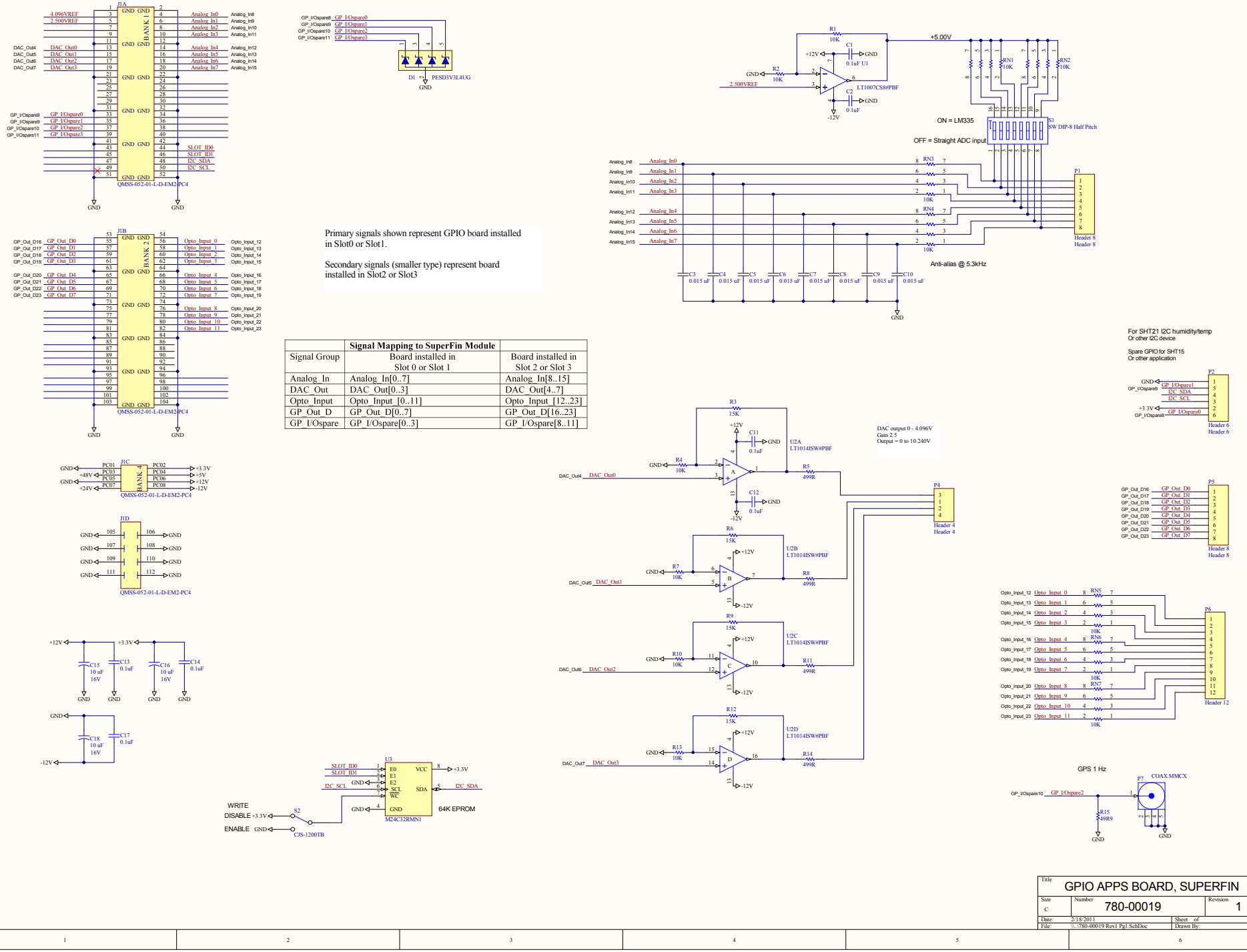

Primary signals shown represent GPIO board installed in Slot0 or Slot1.
Secondary signals (smaller type) represent board installed in Slot2 or Slot3
Signal Mapping to SuperFin Module
Signal Group | Board installed in Slot 0 or Slot 1 | Board installed in Slot 2 or Slot 3
Analog_In | Analog_In[0..7] | Analog_In[8..15]
DAC_Out | DAC_Out[0..3] | DAC_Out[4..7]
Opto_Input | Opto_Input_[0..11] | Opto_Input_[12..23]
GP_Out_D | GP_Out_D[0..7] | GP_Out_D[16..23]
GP_I/Ospare | GP_I/Ospare[0..3] | GP_I/Ospare[8..11]
ON = LM335
OFF = Straight ADC input
Anti-alias @ 5.3kHz
DAC output 0 - 4.096V
Gain 2.5
Output = 0 to 10.240V
For SHT21 I2C humidity/temp
Or other I2C device
Spare GPIO for SHT15
Or other application
GPS 1 Hz
WRITE DISABLE
ENABLE
64K EPROM
GPIO APPS BOARD, SUPERFIN
780-00019
Revision 1
2/18/2011
\...\780-00019 Rev1 Pg1.SchDoc

NOTES (UNLESS OTHERWISE SPECIFIED):

GENERAL

1) PCB IS 6-LAYER, .062" THICK.
2) CONSTRUCTION IS SOLDER-MASK-OVER-BARE-COPPER (SMOBC).
3) ACCEPTABILITY SHALL BE BASED ON IPC-A-600, CLASS 2.
4) THE FOLLOWING GERBER RS274X PHOTO TOOL FILES SHALL BE USED TO DEFINE ALL CIRCUIT FEATURES:

*.GTL – TOP LAYER GERBER DATA
*.G1 – MID LAYER 1 GERBER DATA

*.GP1 – INTERNAL PLANE LAYER 1 GERBER DATA
*.GP2 – INTERNAL PLANE LAYER 2 GERBER DATA
*.GP3– INTERNAL PLANE LAYER 3 GERBER DATA

*.GBL – BOTTOM LAYER GERBER DATA
*.GTO – TOP OVERLAY GERBER DATA
*.GTS – TOP SOLDER MASK GERBER DATA
*.GTP – TOP-SIDE SOLDER PASTE MASK
*GBO BOTTOM OVERLAY GERBER DATA
*.GBS – BOTTOM SOLDER MASK GERBER DATA
*.GBP – BOTTOM-SIDE SOLDER PASTE MASK

5) THE PHOTO TOOL SHALL NOT BE COMPENSATED WITHOUT PRIOR ENGINEERING APPROVAL.
PCB DESIGNER: RICH LOBDILL PH (805) 880-1621 FAX (805) 961-1792.

FABRICATION TOLERANCES

6) END PRODUCT CONDUCTOR WIDTHS AND PAD DIAMETERS SHALL NOT VARY MORE THAN 0.002" FROM THE 1:1 DIMENSIONS OF THE MASTER ARTWORK.
7) THE CONDUCTIVE PATTERN SHALL BE POSITIONED SO THAT THE LOCATION OF ANY PAD OR LAND SHALL BE WITHIN 0.005" DIAMETER TO THE TRUE POSITION OF THE HOLE IT CIRCUMSCRIBES.
8) ALL DRILL HOLE SIZES AND TOLERANCES APPLY AFTER PLATING.
9) THE MINIMUM ANNULAR RING SHALL BE 0.005".
10) BOW AND TWIST SHALL NOT EXCEED 0.010" PER INCH.
11) FOR PCB ROUTING DIMENSIONS: .XXX = +/-.005" .XX = +/-.020"

MATERIAL

12) BASE MATERIAL IS FR4 EPOXY FIBERGLASS
13) SEE STACK-UP LEGEND FOR COPPER CLADDING CALL OUTS

PLATING

14) ALL HOLES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH A MINIMUM OF 0.001" COPPER.
15) AFTER SOLDERMASK, ALL EXPOSED HOLES AND CONDUCTIVE SURFACES SHALL BE COATED WITH A GOLD IMMERSION PLATING TO PRESERVE SOLDERABILITY.

COATINGS

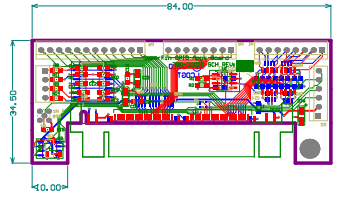
16) THE SOLDERMASK SHALL BE BLACK LIQUID PHOTO-IMAGEABLE PER IPC-SM-840, TYPE-B, CLASS 2.
17) THE SOLDERMASK REGISTRATION ALLOWANCE IS 0.003". THERE SHALL BE NO SOLDERMASK ON ANY SOLDER PAD OR LAND.

MARKING

18) THE LEGEND SHALL BE SCREEN-PRINTED USING PERMANENT YELLOW EPOXY INK.
19) THE SCREEN PRINTING REGISTRATION ALLOWANCE IS 0.007". THERE SHALL BE NO INK ON ANY SOLDER PAD OR LAND.
20) THE VENDOR CODE AND UL FLAMMABILITY RATING MAY BE ETCHED IN THE FOIL OR MARKED IN PERMANENT EPOXY INK (VENDOR'S OPTION).

ELECTRICAL TESTING

21) ALL BOARDS SHALL BE ELECTRICALLY TESTED TO THE SUPPLIED IPC-D-356A NET LIST FOR CONTINUITY, OPENS AND SHORTS.



175-00016_Rev1, SuperFin GPIO Apps Brd
LAS CUMBRES OBSERVATORY 11/18/2010

*.GTO – MID LAYER 1 GERBER DATA

Layer Stack Up Detail for: 175-00016_rev1 SuperFin GPIO Apps Board.PcbDoc

Layer Name	COPPER THICKNESS
Top Layer (*.GTL)	1/2 oz
Mid-Layer 1 (*.G1)	1 OZ
Internal Plane 1 (*.GP1)	1 OZ
Internal Plane 2 (GP2)	1 OZ
Internal Plane 3 (GP3) (GP3)	1 OZ
Bottom Layer (GBL)	1/2 oz

PRIMARY PCB SPECIFICATIONS

(REFER TO COMPLETE SPEC LISTING AT LEFT FOR FURTHER DETAILS)

NUMBER OF LAYERS	–	6
FINISHED THICKNESS	–	.062"
BASE MATERIAL	–	FR4
PLATING TYPE	–	GOLD IMMERSION
SOLDER MASK COLOR	–	BLACK

Las Cumbres Observatory
Global Telescope Network
Las Cumbres Observatory, Inc.
6740 Cortona Dr.
Goleta, CA 93117
www.lcogt.net

DATE	DESIGNED	DRAWN	SCALE
11/18/2010	Rich Lobdill	Rich Lobdill	1 : 1

CHECKED/DATE
APPROVED/DATE

TITLE: 175-00016, SuperFin GPIO Apps Board

SIZE	DOC NO.	REV	SHEET
C	– GPT	1	1 OF X

LCO p/n	Quantity	Designator
120-00002	7	C1, C2, C11, C12, C13, C14, C17
120-00043	8	C3, C4, C5, C6, C7 C8, C9, C10
120-00001	3	C15, C16, C18
140-00011	1	D1
125-00059	1	J1
125-00047	2	P1, P5
125-00033	1	P2
125-00037	1	P4
125-00055	1	P6
125-00054	1	P7
181-01002	6	R1, R2, R4, R7, R10, R13
181-01502	4	R3, R6, R9, R12
181-04990	4	R5, R8, R11, R14
181-049R9	1	R15
180-00043	7	RN1, RN2, RN3, RN4, RN5, RN6, RN
185-00011	1	S1
185-00010	1	S2
150-00067	1	U1
150-00077	1	U2
150-00076	1	U3