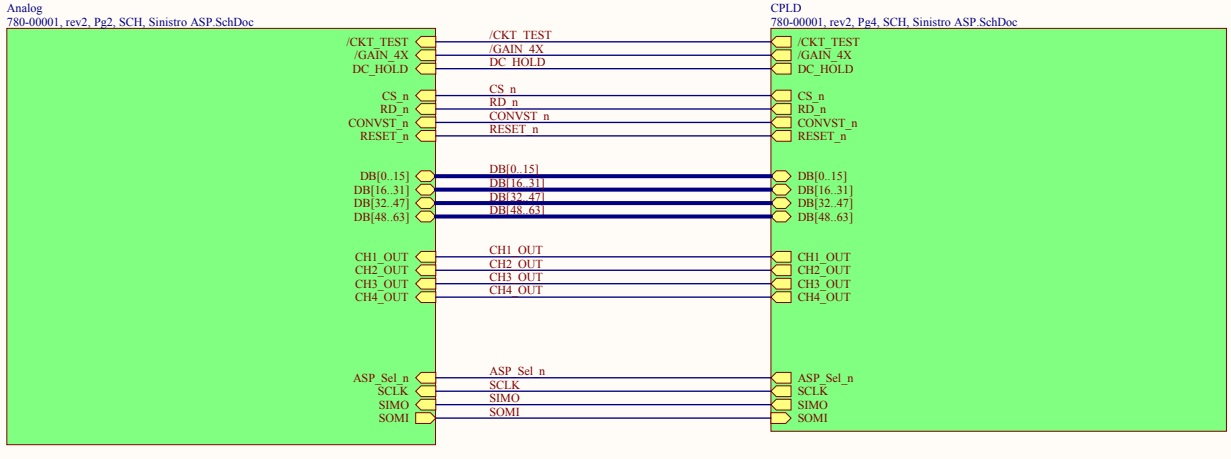

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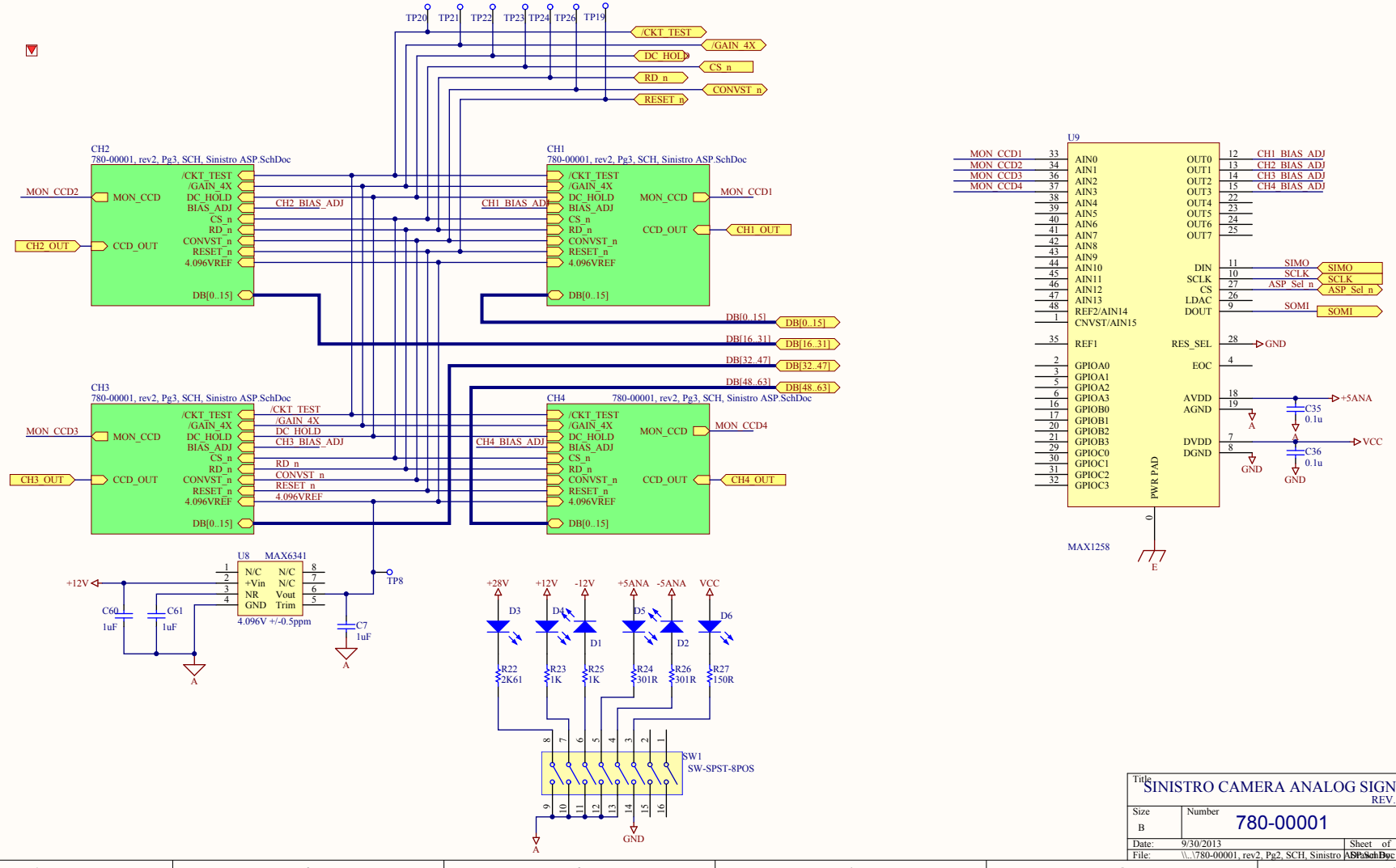

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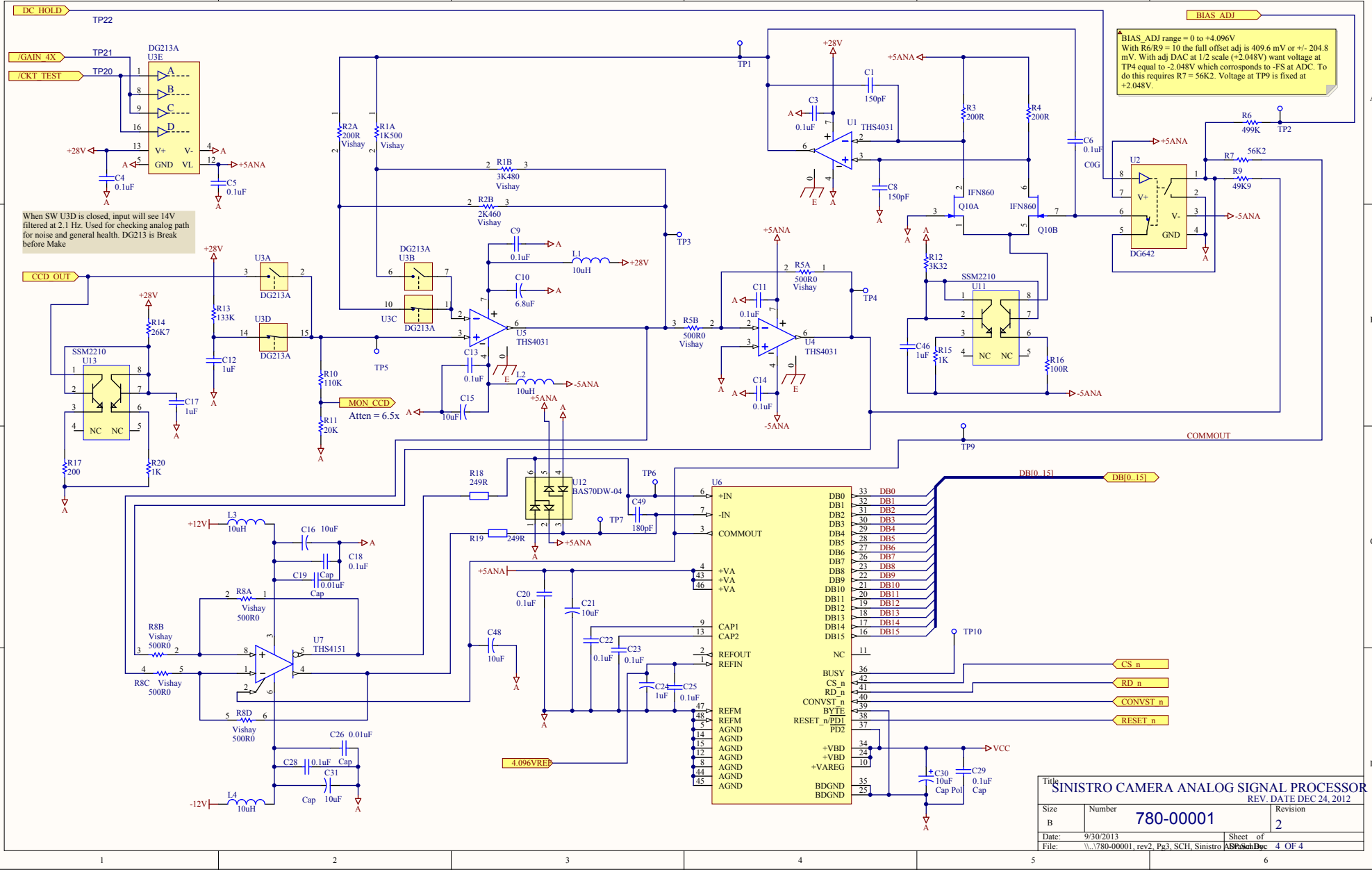
DC_HOLD
TP22
/GAIN_4X
TP21
/CKT_TEST
TP20
DG213A
U3E
+28V
+5ANA
C4 0.1uF
C5 0.1uF
When SW U3D is closed, input will see 14V filtered at 2.1 Hz. Used for checking analog path for noise and general health. DG213 is Break before Make
CCD_OUT
U3A
U3B
U3C
U3D
DG213A
R13 133K
R14 26K7
R10 110K
R11 20K
C12 1uF
C17 1uF
SSM2210
U13
NC NC
R17 200
R20 1K
MON_CCD
Atten = 6.5x
R2A 200R Vishay
R1A 1K500 Vishay
R1B 3K480 Vishay
R2B 2K460 Vishay
TP5
TP3
C9 0.1uF
C10 6.8uF
L1 10uH
C13 0.1uF
C15 10uF
L2 10uH
-5ANA
U5 THS4031
R5B 500R0 Vishay
R5A 500R0 Vishay
U4 THS4031
C11 0.1uF
C14 0.1uF
TP4
TP1
C1 150pF
C3 0.1uF
C8 150pF
U1 THS4031
R3 200R
R4 200R
IFN860
Q10A
Q10B
C6 0.1uF C0G
BIAS_ADJ
BIAS_ADJ range = 0 to +4.096V
With R6/R9 = 10 the full offset adj is 409.6 mV or +/- 204.8 mV. With adj DAC at 1/2 scale (+2.048V) want voltage at TP4 equal to -2.048V which corresponds to -FS at ADC. To do this requires R7 = 56K2. Voltage at TP9 is fixed at +2.048V.
R6 499K
TP2
R7 56K2
R9 49K9
U2
DG642
V+
V-
GND
R12 3K32
SSM2210
U11
C46 1uF
R15 1K
R16 100R
TP9
COMMOUT
R18 249R
R19 249R
U12 BAS70DW-04
TP6
TP7
C49 180pF
U6
+IN
-IN
COMMOUT
+VA
CAP1
CAP2
REFOUT
REFIN
REFM
AGND
+VBD
+VAREG
BDGND
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
DB10
DB11
DB12
DB13
DB14
DB15
NC
BUSY
CS_n
RD_n
CONVST_n
BYTE
RESET_n/PD1
PD2
DB[0..15]
TP10
CS_n
RD_n
CONVST_n
RESET_n
4.096VREF
VCC
C20 0.1uF
C21 10uF
C22 0.1uF
C23 0.1uF
C24 1uF
C25 0.1uF
C48 10uF
C30 10uF Cap Pol
C29 0.1uF Cap
L3 10uH
L4 10uH
C16 10uF
C18 0.1uF
C19 0.01uF Cap
C26 0.01uF
C28 0.1uF Cap
C31 Cap 10uF
R8A Vishay 500R0
R8B Vishay 500R0
R8C Vishay 500R0
R8D Vishay 500R0
U7 THS4151
+12V
-12V
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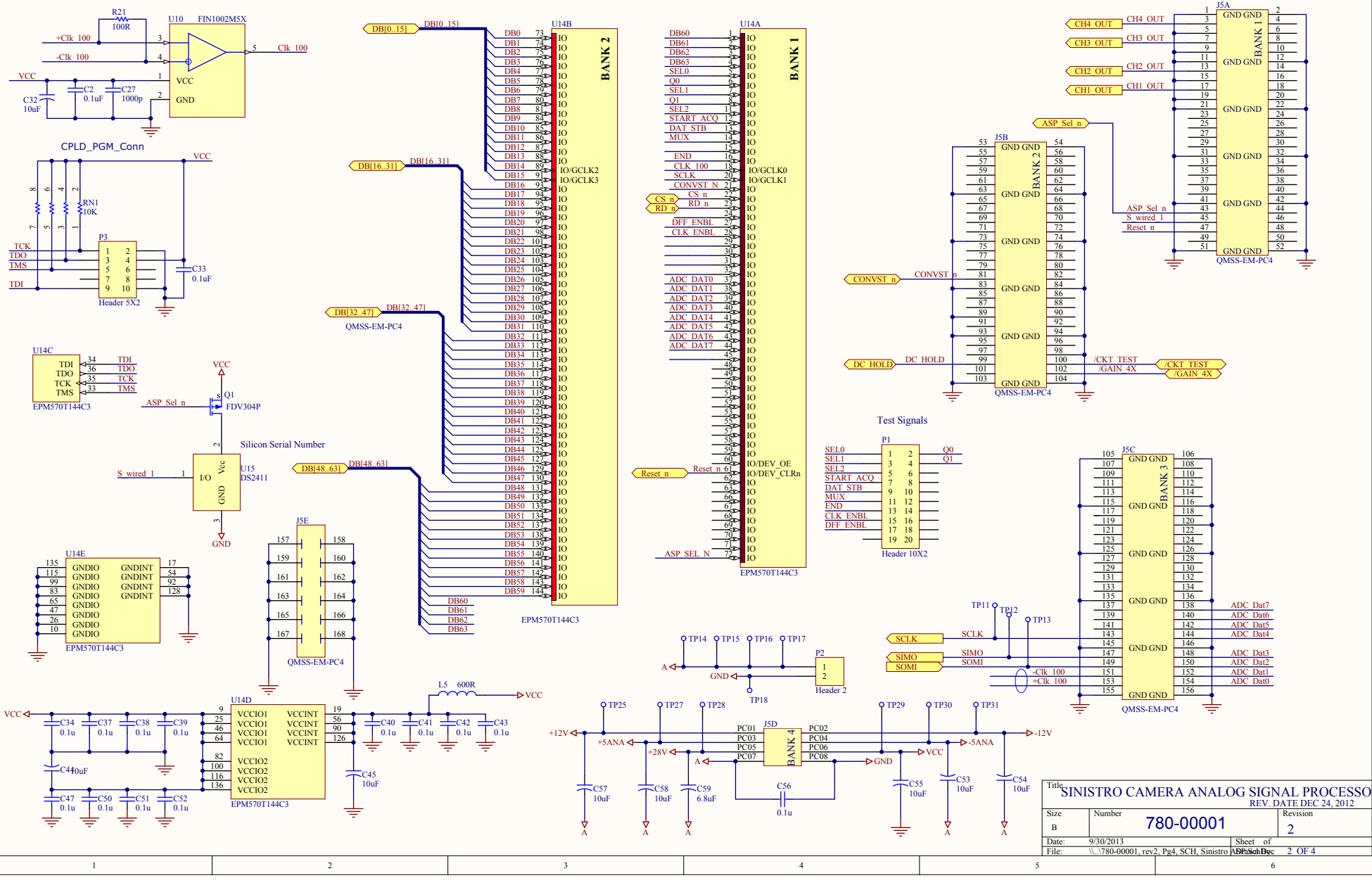
U10 FIN1002M5X
R21 100R
+Clk_100
-Clk_100
Clk_100
VCC
GND
C32 10uF
C2 0.1uF
C27 1000p
CPLD_PGM_Conn
RN1 10K
P3
Header 5X2
TCK
TDO
TMS
TDI
C33 0.1uF
U14C
EPM570T144C3
ASP_Sel_n
Q1
FDV304P
Silicon Serial Number
S_wired_1
U15 DS2411
U14E
U14D
VCCIO1
VCCINT
VCCIO2
L5 600R
C34 0.1u
C37 0.1u
C38 0.1u
C39 0.1u
C40 0.1u
C41 0.1u
C42 0.1u
C43 0.1u
C44 10uF
C45 10uF
C47 0.1u
C50 0.1u
C51 0.1u
C52 0.1u
DB[0..15]
DB[16..31]
DB[32..47]
DB[48..63]
U14B
BANK 2
IO/GCLK2
IO/GCLK3
QMSS-EM-PC4
J5E
U14A
BANK 1
IO/GCLK0
IO/GCLK1
CS_n
RD_n
DFF_ENBL
CLK_ENBL
ADC_DAT0
ADC_DAT1
ADC_DAT2
ADC_DAT3
ADC_DAT4
ADC_DAT5
ADC_DAT6
ADC_DAT7
Reset_n
IO/DEV_OE
IO/DEV_CLRn
ASP_SEL_N
J5A
BANK 1
CH4_OUT
CH3_OUT
CH2_OUT
CH1_OUT
ASP_Sel_n
S_wired_1
Reset_n
J5B
BANK 2
CONVST_n
DC_HOLD
/CKT_TEST
/GAIN_4X
Test Signals
P1
Header 10X2
SEL0
SEL1
SEL2
START_ACQ
DAT_STB
MUX
END
CLK_ENBL
DFF_ENBL
Q0
Q1
J5C
BANK 3
ADC_Dat7
ADC_Dat6
ADC_Dat5
ADC_Dat4
ADC_Dat3
ADC_Dat2
ADC_Dat1
ADC_Dat0
SCLK
SIMO
SOMI
-Clk_100
+Clk_100
TP11
TP12
TP13
TP14
TP15
TP16
TP17
TP18
P2
Header 2
J5D
BANK 4
PC01
PC02
PC03
PC04
PC05
PC06
PC07
PC08
+12V
-12V
+5ANA
-5ANA
+28V
TP25
TP27
TP28
TP29
TP30
TP31
C53 10uF
C54 10uF
C55 10uF
C56 0.1u
C57 10uF
C58 10uF
C59 6.8uF
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