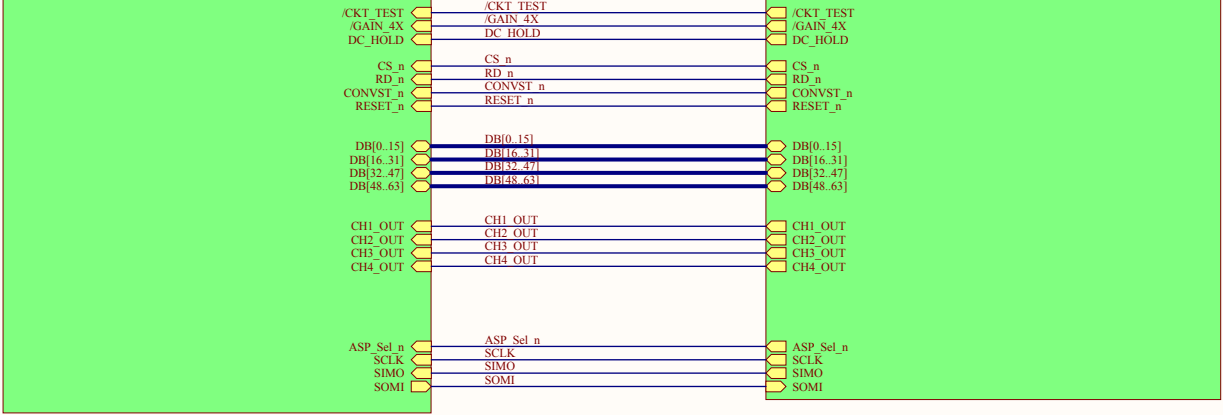
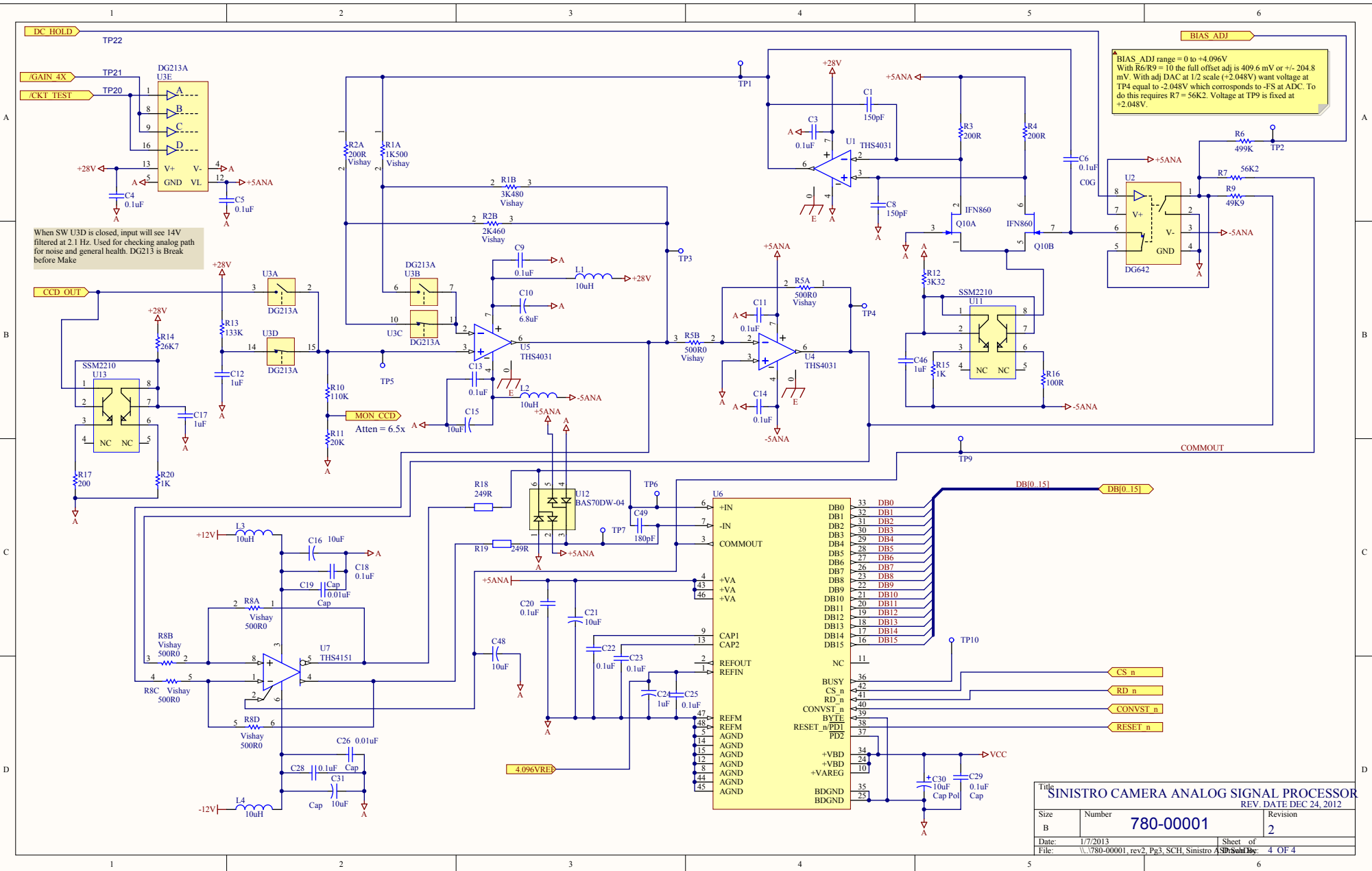


Analog
780-00001_rev2_Pg2_SCH_Sinistro ASP.SchDoc



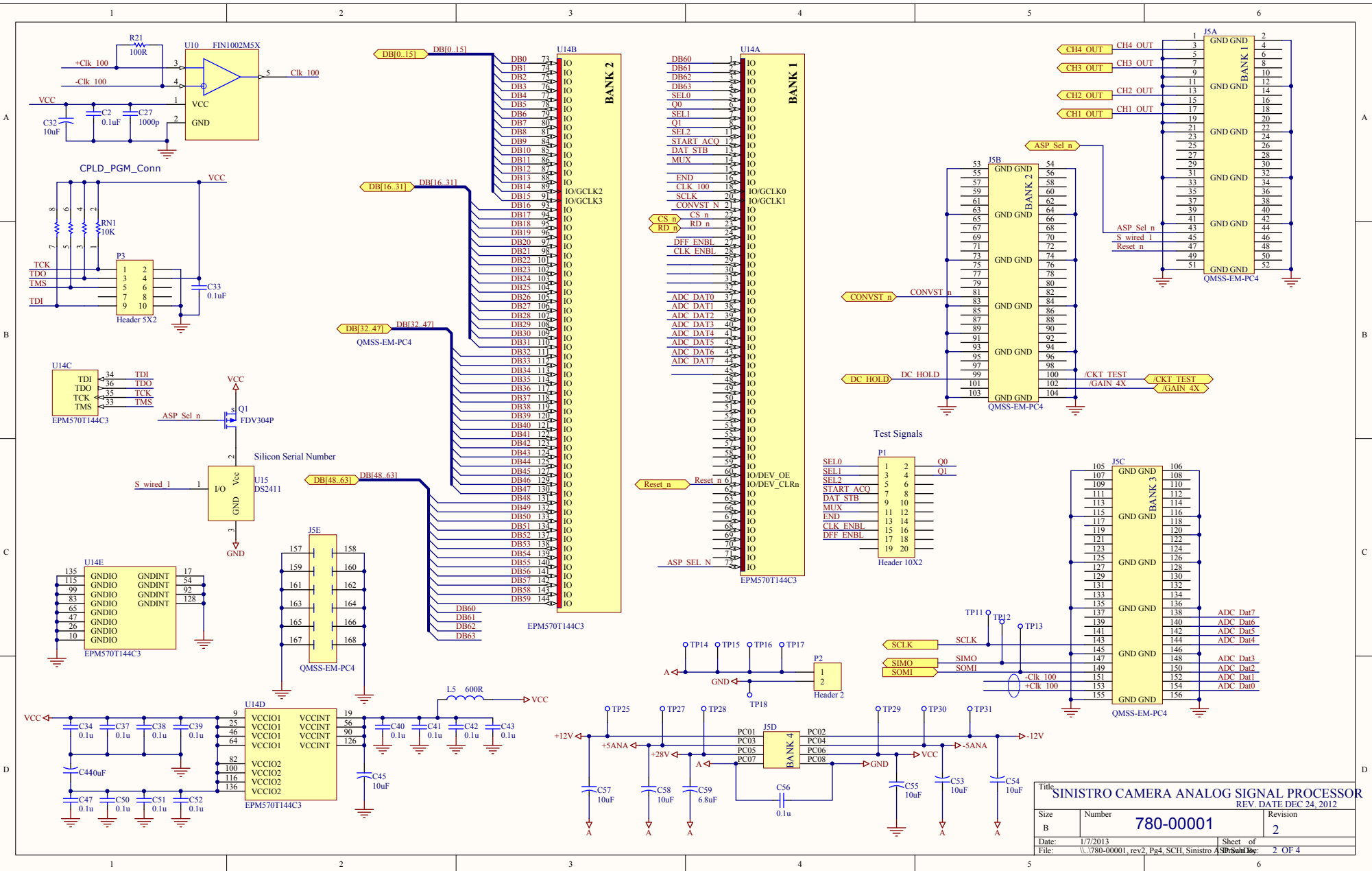
CPLD
780-00001_rev2_Pg4_SCH_Sinistro ASP.SchDoc



When SW U3D is closed, input will see 14V filtered at 2.1 Hz. Used for checking analog path for noise and general health. DG213 is Break before Make

BIAS_ADJ range = 0 to +4.096V
With R6/R9 = 10 the full offset adj is 409.6 mV or +/- 204.8 mV. With adj DAC at 1/2 scale (+2.048V) want voltage at TP4 equal to -2.048V which corresponds to -FS at ADC. To do this requires R7 = 56K2. Voltage at TP9 is fixed at +2.048V.

Title			
SINISTRO CAMERA ANALOG SIGNAL PROCESSOR			
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