This page represents the core of the Blackfin. It includes the USB to serial converter for access to the U-Boot and uCLinux console (terminal) on the Blackfin. The JTAG header is for programming the flash. Pin 3 needs to be cut off since the JTAG programming cable is keyed. The Ethernet connector has an integrated transformer inside. High frequency PCB layout techniques need to be utilized between the Ethernet connector and the Blackfin CoreModule.

All signals in and out of the board (GPIO) are 0V - 3.3V. The only exception are the I2C lines, which are 5V compliant (i.e. no level shifting is necessary to communicate on the I2C bus).

Note on PCB Layout:

Ethernet carries signals up to 100MHz. High frequency PCB layout techniques apply. RX and TX lines are differential, so differential microstrip lines should be laid out with a differential impedance of 100 ohms.

Pay attention to the amount of bus capacitance present on the I2C line. See the I2C specification for the maximum amount of bus capacitance allowed. Adjust the two pull-up resistors according to the bus capacitance.

The SP0503BAHT introduces 30pF of capacitance to each line. If the capacitance is too high, and all I2C communications is kept local on the board (output header is omitted), then this diode can be removed.

Note:

The Blackfin input ports are VERY sensitive to ESD. Your input and output headers to the Blackfin should be well protected with TVS diodes.

Parts we have used before (datasheets included in datasheets folder):
SP0503BAHT (3 channel, Digikey PN F2715CT-ND)
CDNBS08-SRDA3.3-4 (4 channel, Digikey PN CDNBS08-SRDA3.3-4CT-ND)

U2
CP2102

C1 1uF
C2 10uF
C3 0.1uF
C4 0.1uF
C5 1uF
C6 0.1uF
C7 0.1uF
C8 1uF
C9 0.1uF
C10 0.1uF

R1 10.0K
R2 10.0K
R5 100K
R6 4.75K

D2
SP0503BAHT

U3
CM-BF537E

P2
Header 10X2

P6
Header 7X2
JTAG Header

J3
Wurth Elektronik 7498011002

S1
B3U-1000P

S2
SD03H0SB

SW1
CJS-1200TB

Schematic for PLD program
FPGA_U1_Auto_revC.SchDoc

Stepper Motor Driver IC
Stepper_Motor_Drive_revC.SchDoc

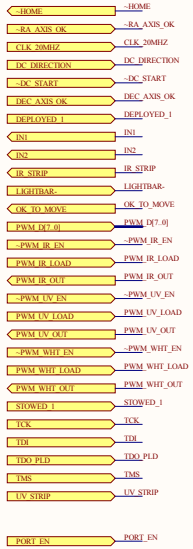
Bootmodes can be found on page 16 of the ADSP-BF537 datasheet. The default for our needs is all 3 switches open.

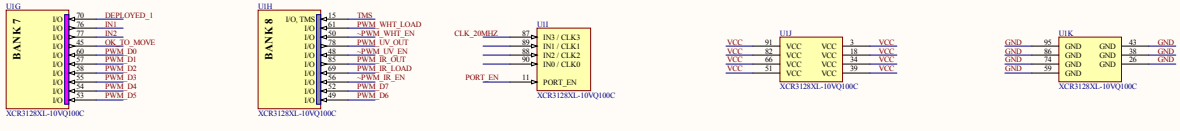
Note:

The JTAG programming cable is keyed, so pin 3 on the header needs to be cut off.

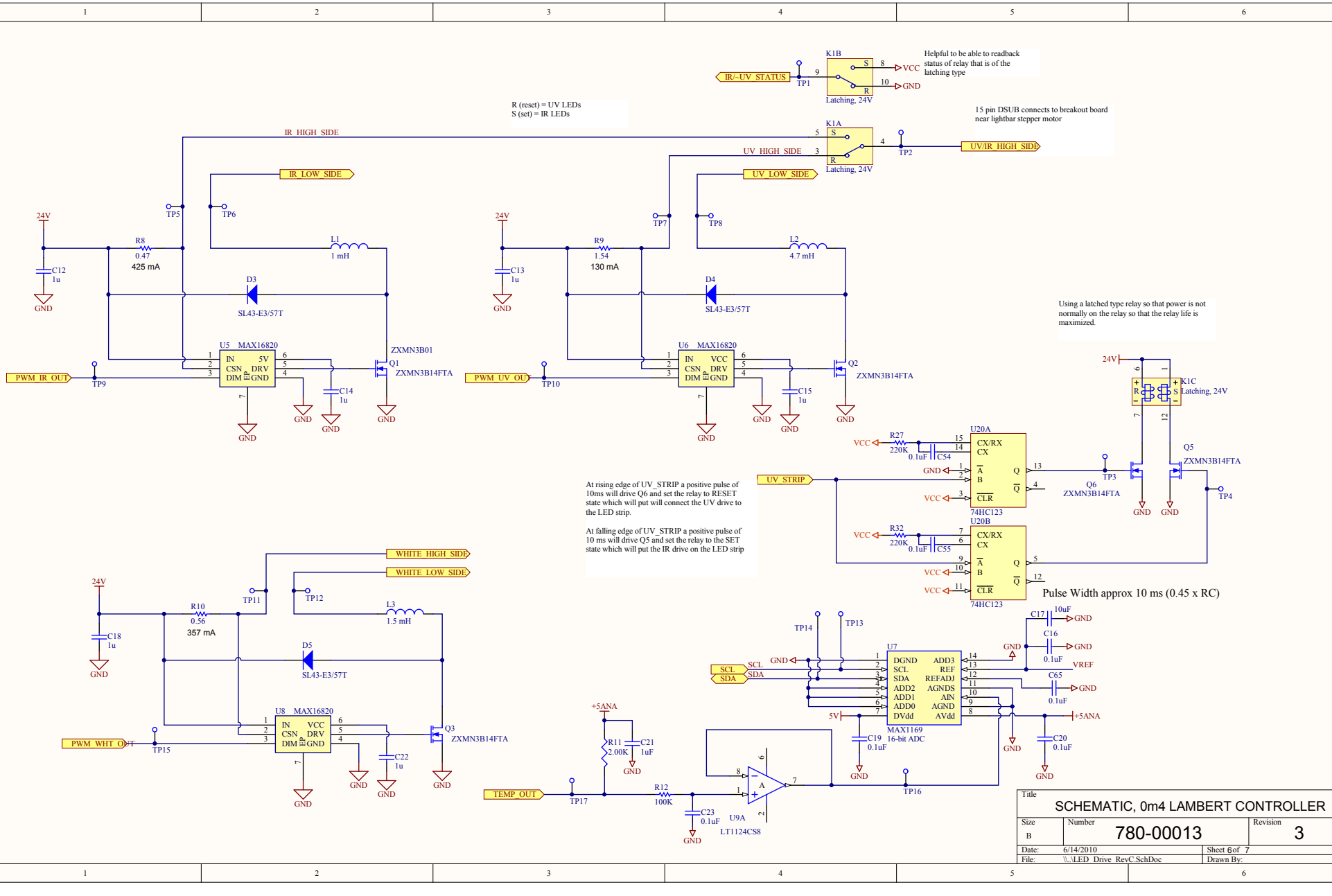
Up to PRGM BF, Down for PMD

Title	SCHEMATIC, 0m4 LAMBERT CONTROLLER		
Size	Number		Revision
Tabloid	780-00013		3
Date:	6/14/2010	Sheet 2 of 7	
File:	\\...\Blackfin_revC.SchDoc	Drawn By:	





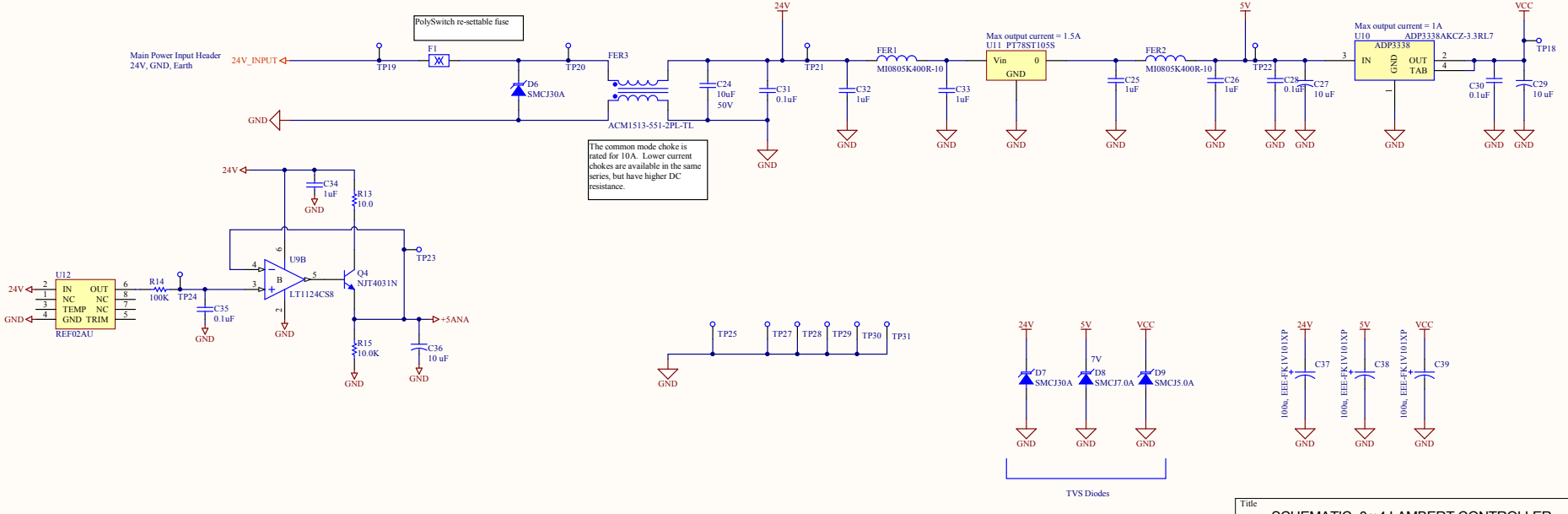
Title	SCHEMATIC, 0m4 LAMBERT CONTROLLER		
Size A2	Number 780-00013		Revision 3
Date: 6/14/2010		Sheet 4 of 7	
File: ..\..\FPGA_U1_Auto_revC.SchDoc		Drawn By:	


IR/~UV_STATUS
TP1
K1B
Latching, 24V
VCC
GND
Helpful to be able to readback status of relay that is of the latching type
R (reset) = UV LEDs
S (set) = IR LEDs
15 pin DSUB connects to breakout board near lightbar stepper motor
K1A
Latching, 24V
IR_HIGH_SIDE
UV_HIGH_SIDE
UV/IR_HIGH_SIDE
TP2
IR_LOW_SIDE
UV_LOW_SIDE
24V
TP5
TP6
TP7
TP8
R8
0.47
425 mA
L1
1 mH
C12
1u
D3
SL43-E3/57T
R9
1.54
130 mA
L2
4.7 mH
C13
1u
D4
SL43-E3/57T
U5 MAX16820
U6 MAX16820
ZXMN3B01
ZXMN3B14FTA
Q1
Q2
PWM_IR_OUT
PWM_UV_OUT
TP9
TP10
C14
1u
C15
1u
Using a latched type relay so that power is not normally on the relay so that the relay life is maximized.
K1C
Latching, 24V
Q5
Q6
TP3
TP4
U20A
U20B
74HC123
R27
220K
R32
220K
0.1uF
C54
C55
UV_STRIP
At rising edge of UV_STRIP a positive pulse of 10ms will drive Q6 and set the relay to RESET state which will put will connect the UV drive to the LED strip.
At falling edge of UV_STRIP a positive pulse of 10 ms will drive Q5 and set the relay to the SET state which will put the IR drive on the LED strip
Pulse Width approx 10 ms (0.45 x RC)
WHITE_HIGH_SIDE
WHITE_LOW_SIDE
TP11
TP12
R10
0.56
357 mA
L3
1.5 mH
C18
1u
D5
SL43-E3/57T
U8 MAX16820
Q3
ZXMN3B14FTA
PWM_WHT_OUT
TP15
C22
1u
TP13
TP14
U7
MAX1169
16-bit ADC
SCL
SDA
5V
C17
10uF
C16
0.1uF
C65
0.1uF
C19
0.1uF
C20
0.1uF
VREF
+5ANA
TEMP_OUT
TP16
TP17
R11
2.00K
C21
1uF
R12
100K
C23
0.1uF
U9A
LT1124CS8
Title
SCHEMATIC, 0m4 LAMBERT CONTROLLER
Size
B
Number
780-00013
Revision
3
Date:
6/14/2010
Sheet 6of 7
File:
\\..\LED Drive RevC.SchDoc
Drawn By:

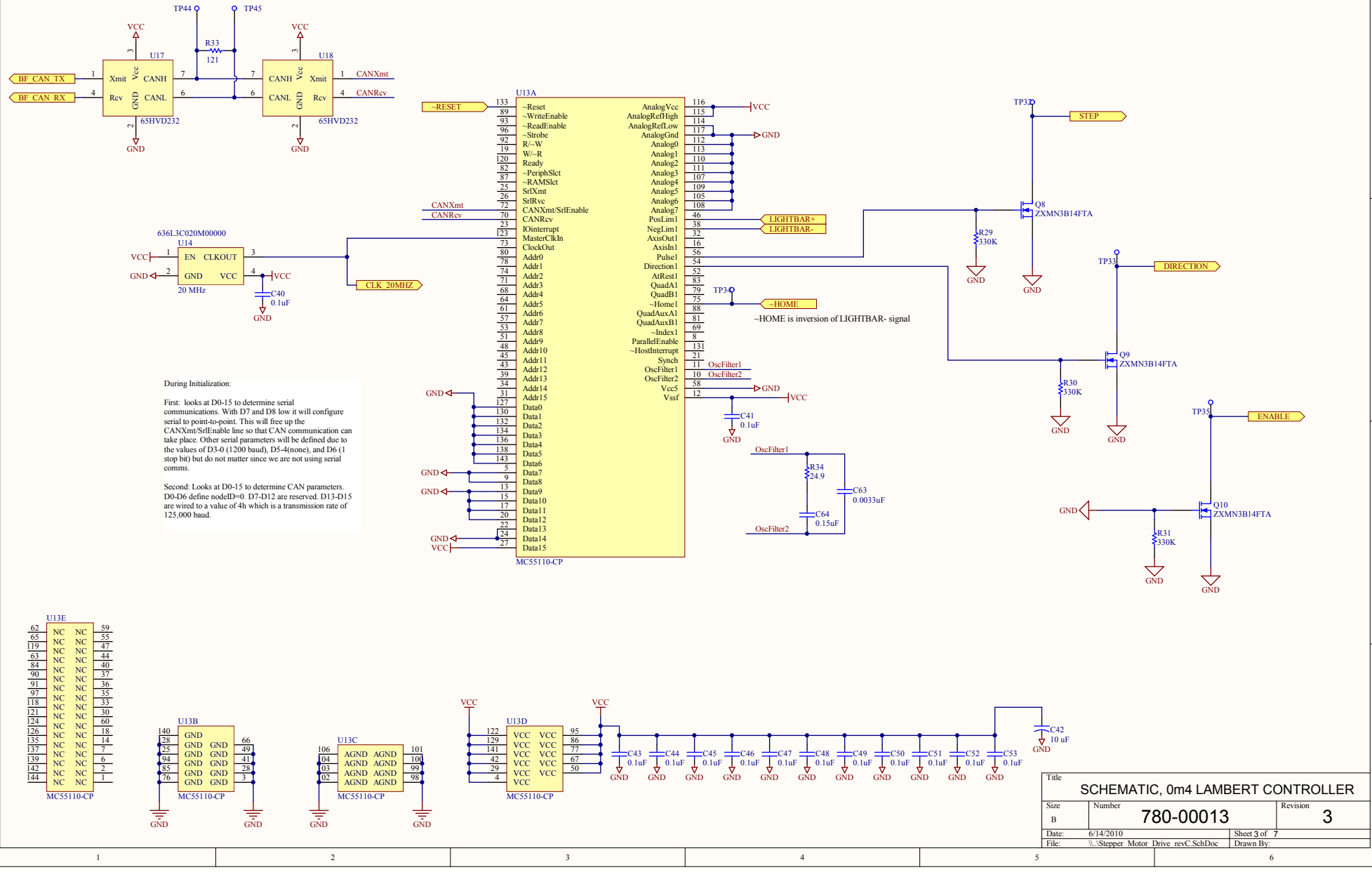
This page is the main power input stage. It takes 24Vdc in and converts it to 5V and 3.3V. Filtering and transient protection is also on this page.

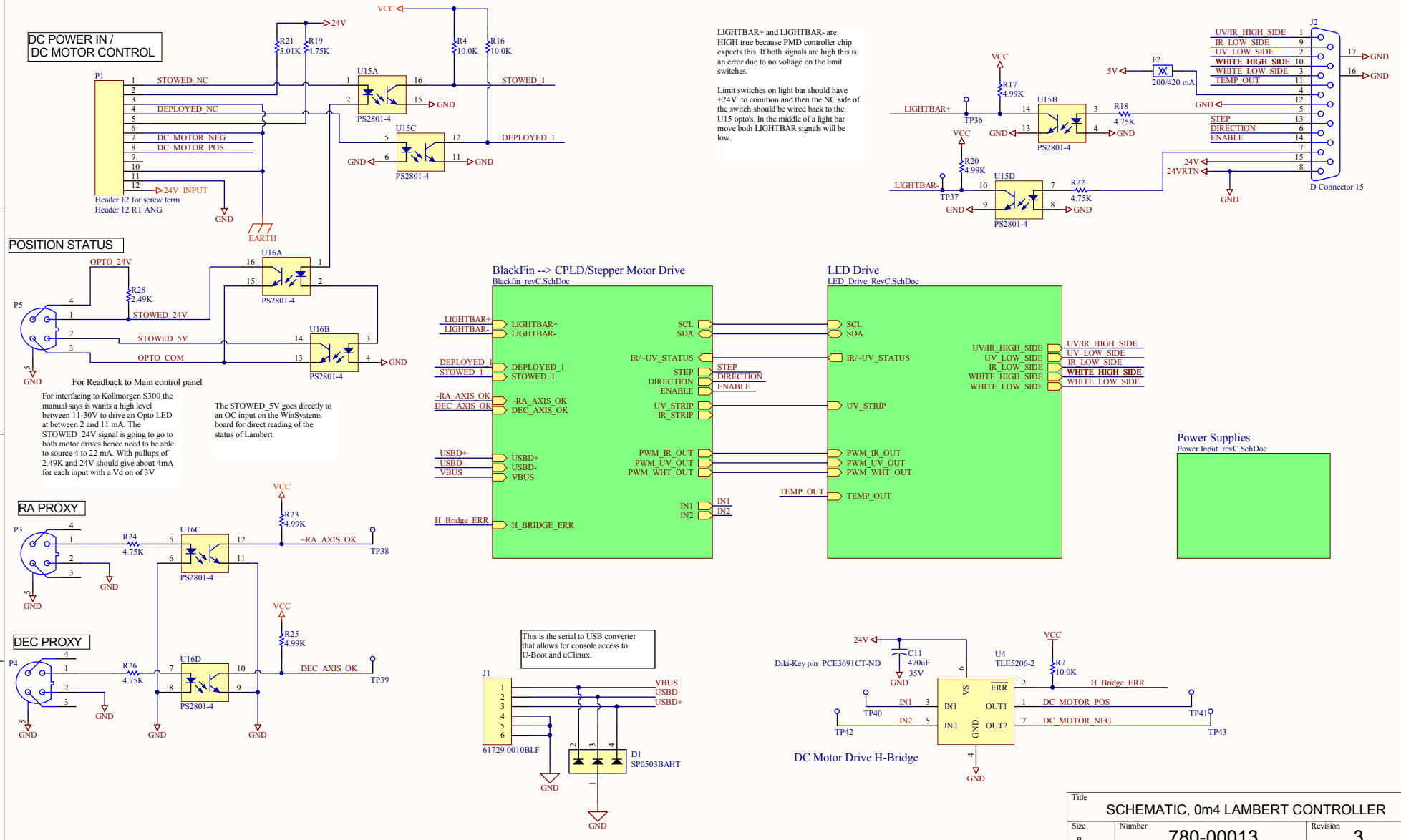
The PT78ST105S is a switching buck converter. It outputs 5V with a maximum output current of 1.5A.

The ADP3338 is a 3.3V linear regulator with a maximum output current of 1A.



Title	SCHEMATIC, 0m4 LAMBERT CONTROLLER
Size	Tabloid
Number	780-00013
Revision	3
Date:	6/14/2010
Sheet 5 of 7	
File:	\\...\Power Input_revC.SchDoc
Drawn By:	


TP44
TP45
VCC
U17
U18
R33
121
BF_CAN_TX
BF_CAN_RX
Xmit
Rcv
CANH
CANL
Vcc
GND
65HVD232
CANXmt
CANRcv
U13A
~RESET
~Reset
~WriteEnable
~ReadEnable
~Strobe
R/~W
W/~R
Ready
~PeriphSlct
~RAMSlct
SrlXmt
SrlRvc
CANXmt/SrlEnable
CANRcv
IOinterrupt
MasterClkIn
ClockOut
Addr0
Addr1
Addr2
Addr3
Addr4
Addr5
Addr6
Addr7
Addr8
Addr9
Addr10
Addr11
Addr12
Addr13
Addr14
Addr15
Data0
Data1
Data2
Data3
Data4
Data5
Data6
Data7
Data8
Data9
Data10
Data11
Data12
Data13
Data14
Data15
AnalogVcc
AnalogRefHigh
AnalogRefLow
AnalogGnd
Analog0
Analog1
Analog2
Analog3
Analog4
Analog5
Analog6
Analog7
PosLim1
NegLim1
AxisOut1
AxisIn1
Pulse1
Direction1
AtRest1
QuadA1
QuadB1
~Home1
QuadAuxA1
QuadAuxB1
~Index1
ParallelEnable
~HostInterrupt
Synch
OscFilter1
OscFilter2
Vcc5
Vssf
MC55110-CP
LIGHTBAR+
LIGHTBAR-
~HOME
~HOME is inversion of LIGHTBAR- signal
636L3C020M00000
U14
EN
CLKOUT
20 MHz
CLK_20MHZ
C40
0.1uF
C41
0.1uF
During Initialization:
First: looks at D0-15 to determine serial communications. With D7 and D8 low it will configure serial to point-to-point. This will free up the CANXmt/SrlEnable line so that CAN communication can take place. Other serial parameters will be defined due to the values of D3-0 (1200 baud), D5-4(none), and D6 (1 stop bit) but do not matter since we are not using serial comms.
Second: Looks at D0-15 to determine CAN parameters. D0-D6 define nodeID=0. D7-D12 are reserved. D13-D15 are wired to a value of 4h which is a transmission rate of 125,000 baud.
TP32
STEP
Q8
ZXMN3B14FTA
R29
330K
TP33
DIRECTION
Q9
ZXMN3B14FTA
R30
330K
TP35
ENABLE
Q10
ZXMN3B14FTA
R31
330K
OscFilter1
R34
24.9
C63
0.0033uF
C64
0.15uF
OscFilter2
U13E
U13B
U13C
U13D
NC
C43
C44
C45
C46
C47
C48
C49
C50
C51
C52
C53
0.1uF
C42
10 uF
Title
SCHEMATIC, 0m4 LAMBERT CONTROLLER
Size
B
Number
780-00013
Revision
3
Date:
6/14/2010
Sheet 3 of 7
File:
\\..\Stepper Motor Drive revC.SchDoc
Drawn By:



Title	SCHEMATIC, 0m4 LAMBERT CONTROLLER	
Size: B	Number: 780-00013	Revision: 3
Date: 6/14/2010		Sheet 1of 7
File: \\..\Top Level IO revC.SchDoc		Drawn By: