

Comment	Description	Designator	Footprint	Lib Ref	Quantity
	D-Type Flip-Flop				
	with Asynchronous				
FDC	Clear	U1, U8, U11		FDC	3
	Clock Divider by 8				
	with 50% Duty				
CDIV8DC50	Cycle Output	U2		CDIV8DC50	1
	Clock Divider by				
CDIV256	256	U3		CDIV256	1
		114 1140 1140 1104			
IN IN /	la contan	U4, U13, U16, U21,		IN 13 /	
INV	Inverter	U22, U24, U26, U28		INV	8
	Cascadable				
	Bid irectional Binary				
	Counter with Cloc				
	Enable and				
	Asynchronous				
CB8CLEDB	Clear, Bus Version	U5 U9 U12		CB8CLEDB	3
	8-Bit D-Type Flip-	00, 00, 0.1			
FD8B	Flop, Bus Version	U6, U7, U10		FD8B	3
	z-ыг p-туре гір-				
	Flop with				
	Asynchronous				
	Clear, Single Pin				
FD2CS	Version	U14		FD2CS	1
	2-Input AND Gate,	U15, U17, U18, u20,			
AND2S	Single Pin Version	U29, U31		AND2S	6
	2-Input OR Gate,				
OR2S	Single Pin Version	U19		OR2S	1
	iransparent Data				
	Latch with				
	Asynchronous				
LDC	Clear	U23, U25, U27		LDC	3
XOR2S	2-Input Exclusive-C	U30		XOR2S	1