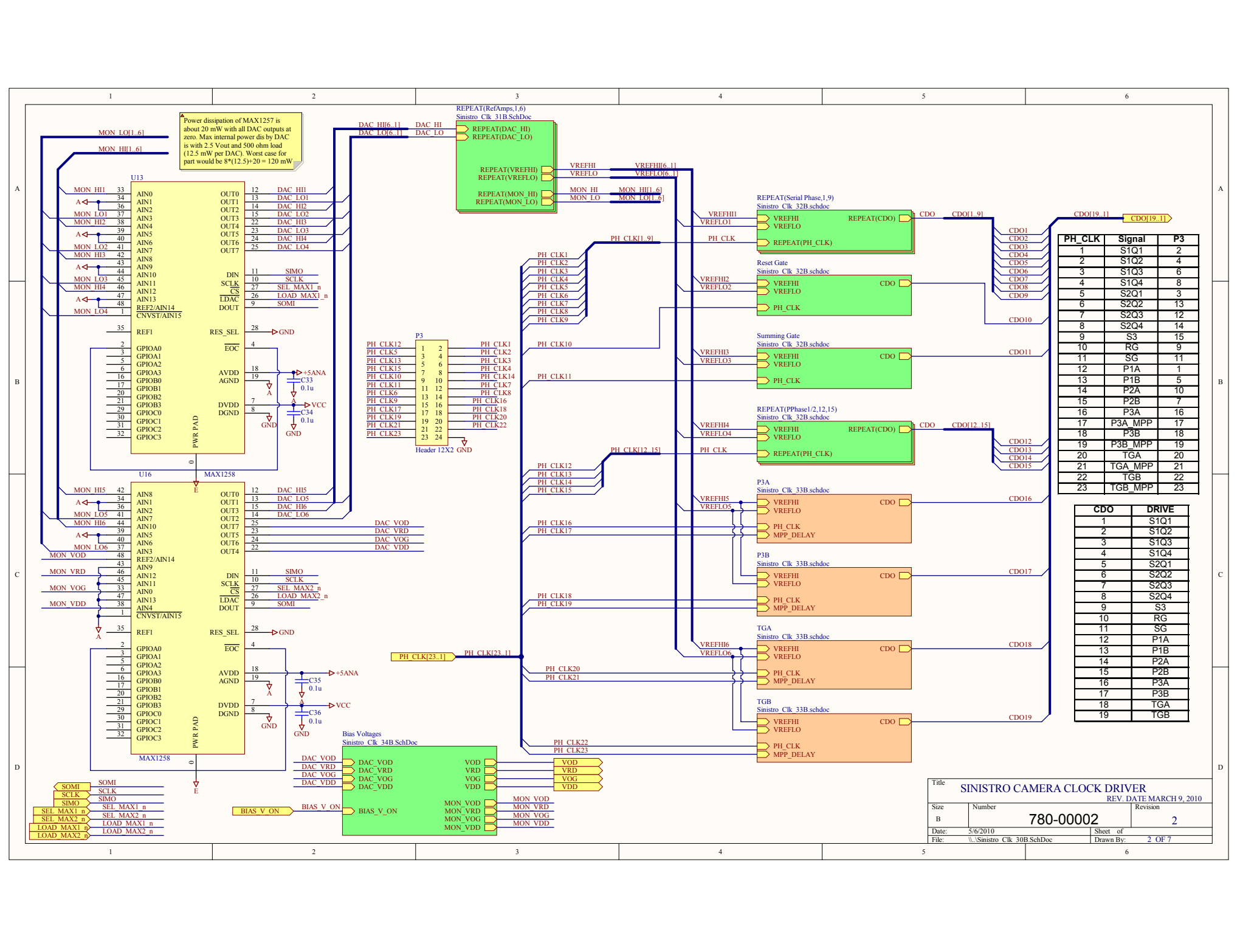

PH_CLK	Signal	P3
1	S1Q1	2
2	S1Q2	4
3	S1Q3	6
4	S1Q4	8
5	S2Q1	3
6	S2Q2	13
7	S2Q3	12
8	S2Q4	14
9	S3	15
10	RG	9
11	SG	11
12	P1A	1
13	P1B	5
14	P2A	10
15	P2B	7
16	P3A	16
17	P3A_MPP	17
18	P3B	18
19	P3B_MPP	19
20	TGA	20
21	TGA_MPP	21
22	TGB	22
23	TGB_MPP	23

CDO	DRIVE
1	S1Q1
2	S1Q2
3	S1Q3
4	S1Q4
5	S2Q1
6	S2Q2
7	S2Q3
8	S2Q4
9	S3
10	RG
11	SG
12	P1A
13	P1B
14	P2A
15	P2B
16	P3A
17	P3B
18	TGA
19	TGB

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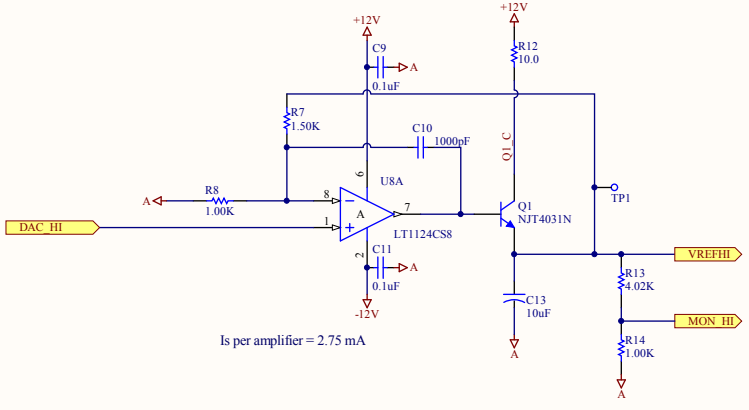
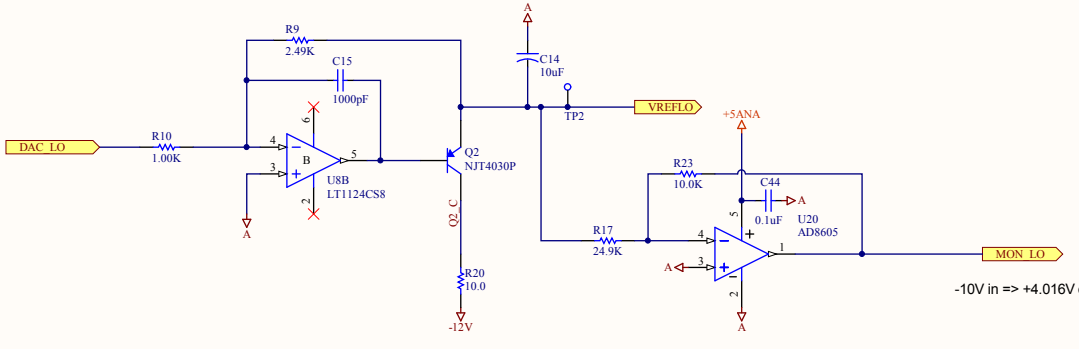


Is per amplifier = 2.75 mA

Max quiescent pwr for U8 = 132 mW

Max q pwr for Q1 or Q2 (+6V/-6V out) = 21.6 mW



-10V in => +4.016V out

Power Dissipation (worst case)

	U8	Q1 or Q2 quiescent (Vout = +/- 6V)	Q1 or Q2 Load* (Vout = +/- 6V)	Total W (U8 + Q1 +Q2)
VREFHI/LO 1	132mW	21.6mW	319 mW	814 mW
VREFHI/LO 2	"	"	neg	175 mW
VREFHI/LO 3	"	"	neg	175 mW
VREFHI/LO 4	"	"	406 mW	988 mW
VREFHI/LO 5	"	"	288 mW	752 mW
VREFHI/LO 6	"	"	9.2 mW	194 mW
				2.92 W

*1 MHz pixel rate/all quadrants clocked

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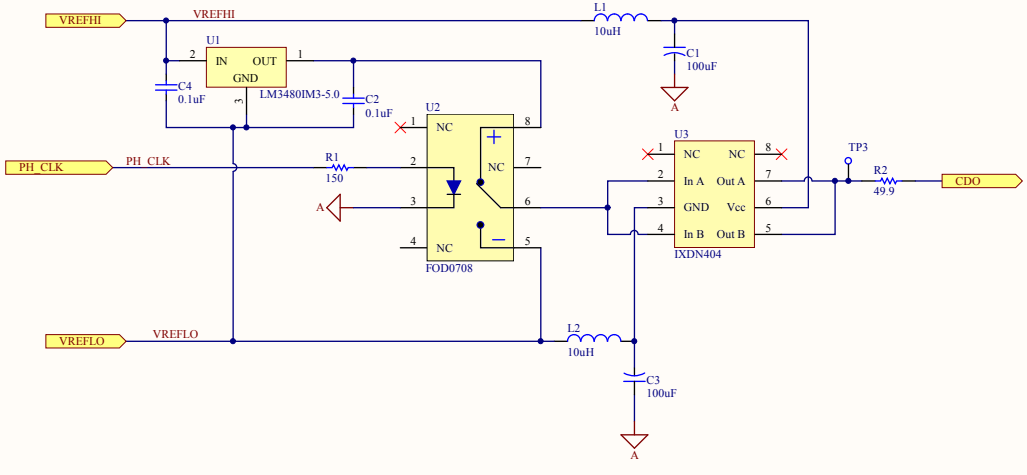

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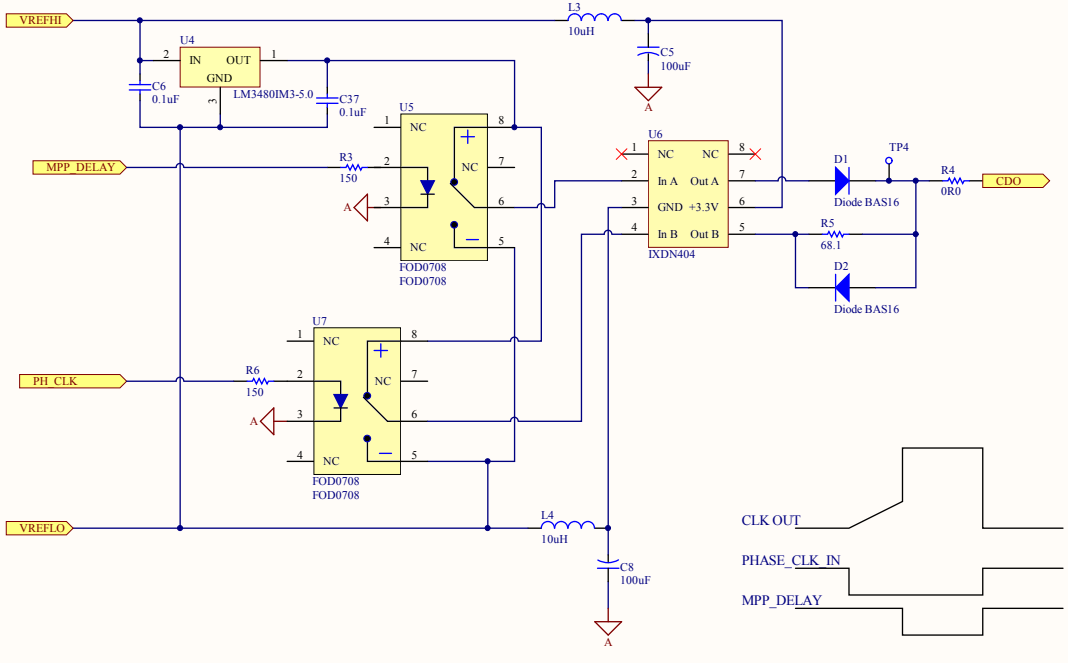

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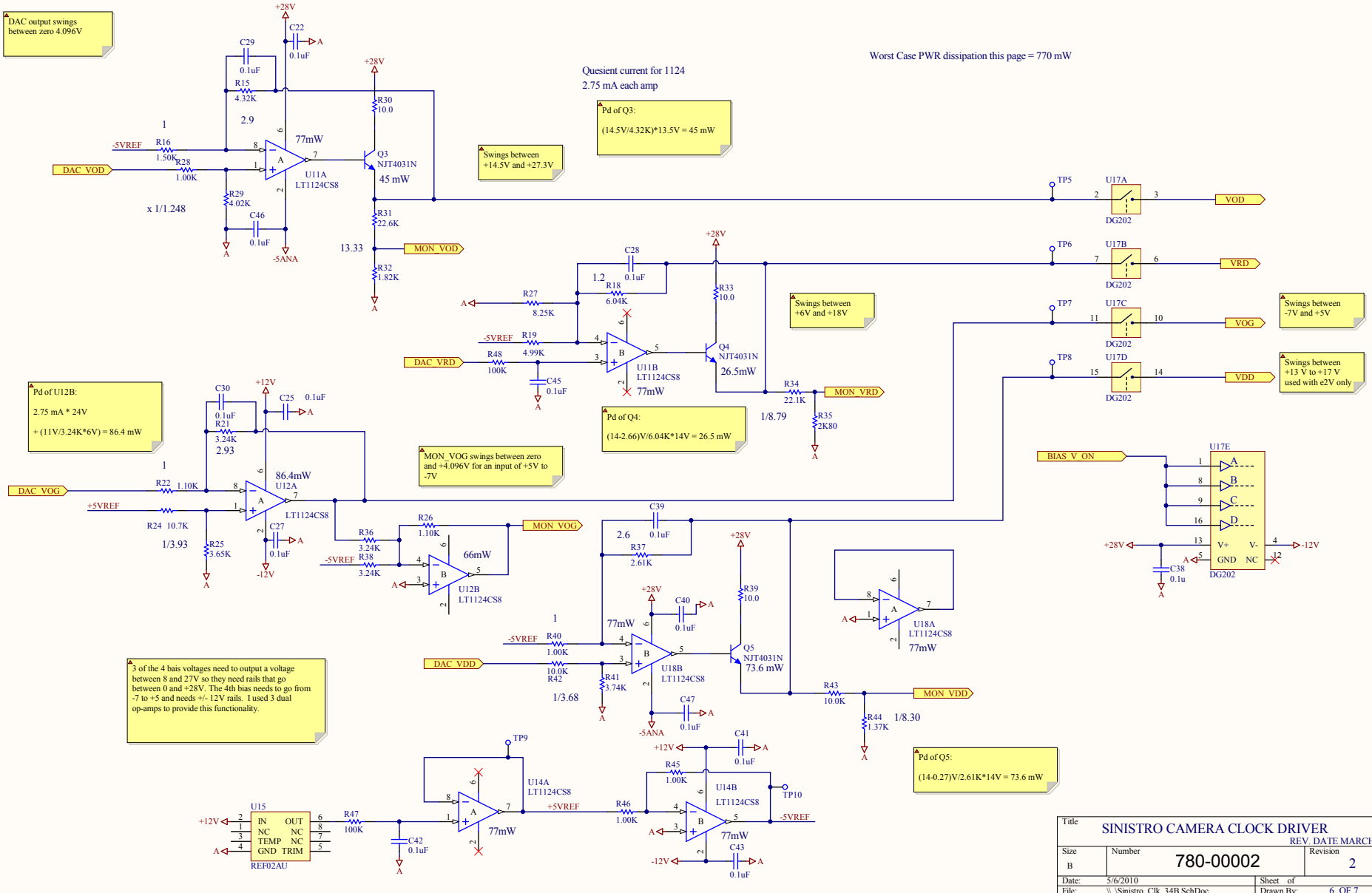
DAC output swings between zero 4.096V
Worst Case PWR dissipation this page = 770 mW
Quesient current for 1124
2.75 mA each amp
Pd of Q3:
(14.5V/4.32K)*13.5V = 45 mW
Swings between +14.5V and +27.3V
Swings between +6V and +18V
Swings between -7V and +5V
Swings between +13 V to +17 V used with e2V only
Pd of U12B:
2.75 mA * 24V
+ (11V/3.24K*6V) = 86.4 mW
MON_VOG swings between zero and +4.096V for an input of +5V to -7V
Pd of Q4:
(14-2.66)V/6.04K*14V = 26.5 mW
Pd of Q5:
(14-0.27)V/2.61K*14V = 73.6 mW
3 of the 4 bais voltages need to output a voltage between 8 and 27V so they need rails that go between 0 and +28V. The 4th bias needs to go from -7 to +5 and needs +/- 12V rails. I used 3 dual op-amps to provide this functionality.
+28V
+12V
-5VREF
+5VREF
-5ANA
-12V
DAC_VOD
DAC_VRD
DAC_VOG
DAC_VDD
MON_VOD
MON_VRD
MON_VOG
MON_VDD
BIAS_V_ON
VOD
VRD
VOG
VDD
x 1/1.248
1/3.93
1/3.68
1/8.30
1/8.79
77mW
45 mW
86.4mW
66mW
26.5mW
73.6 mW
U11A LT1124CS8
U11B LT1124CS8
U12A LT1124CS8
U12B LT1124CS8
U14A LT1124CS8
U14B LT1124CS8
U18A LT1124CS8
U18B LT1124CS8
Q3 NJT4031N
Q4 NJT4031N
Q5 NJT4031N
U15 REF02AU
U17A DG202
U17B DG202
U17C DG202
U17D DG202
U17E DG202
TP5
TP6
TP7
TP8
TP9
TP10
Title
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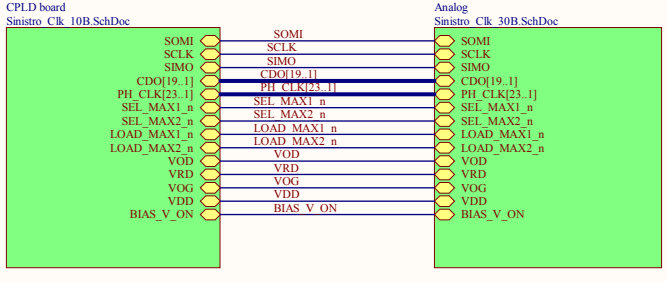

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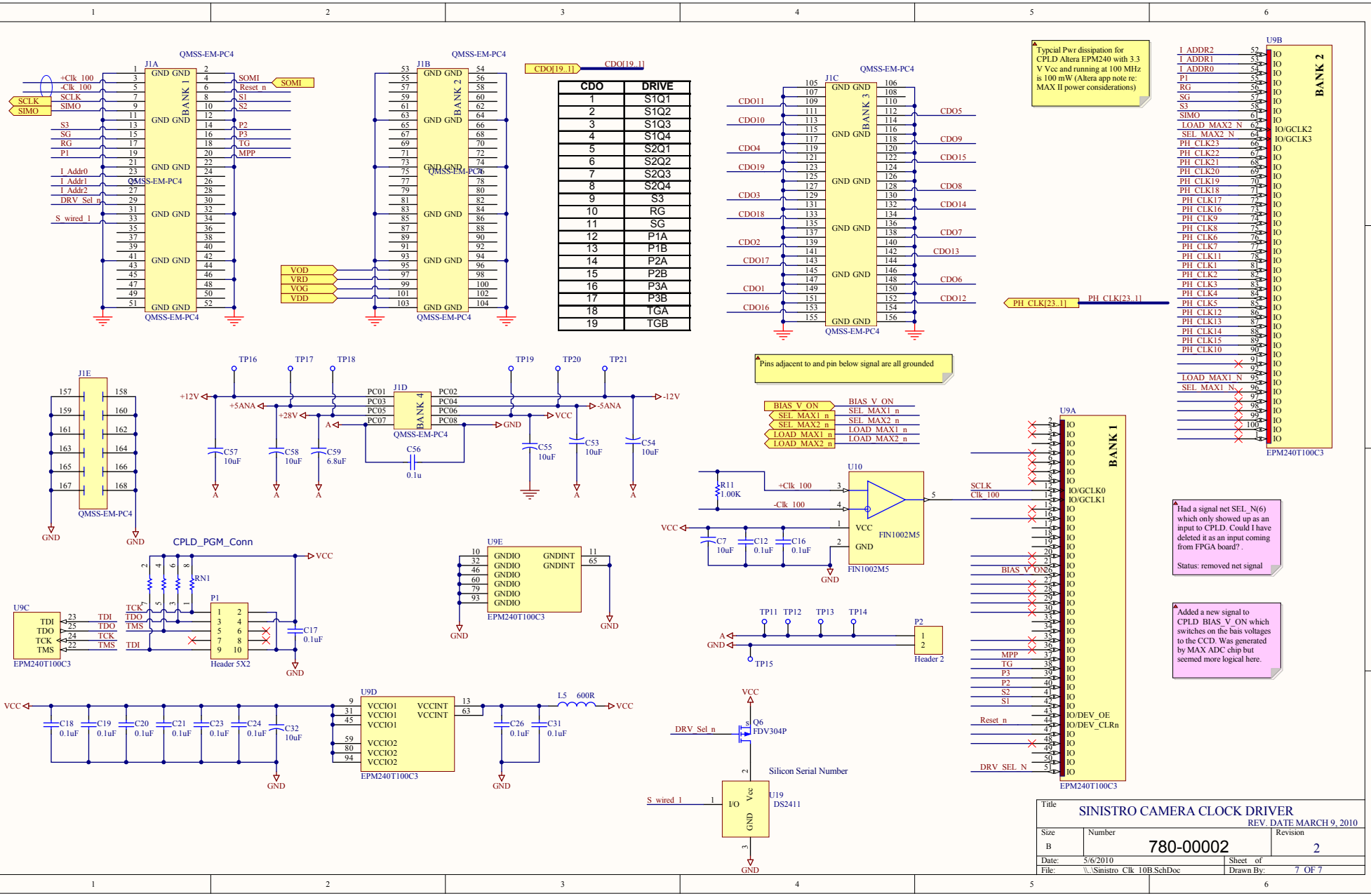

CDO	DRIVE
1	S1Q1
2	S1Q2
3	S1Q3
4	S1Q4
5	S2Q1
6	S2Q2
7	S2Q3
8	S2Q4
9	S3
10	RG
11	SG
12	P1A
13	P1B
14	P2A
15	P2B
16	P3A
17	P3B
18	TGA
19	TGB

Title	SINISTRO CAMERA CLOCK DRIVER
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