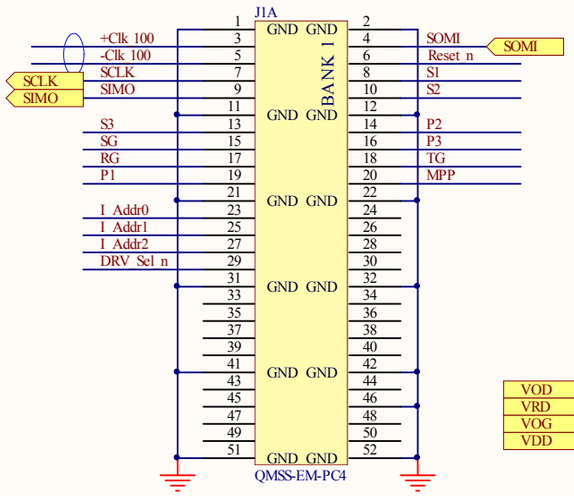
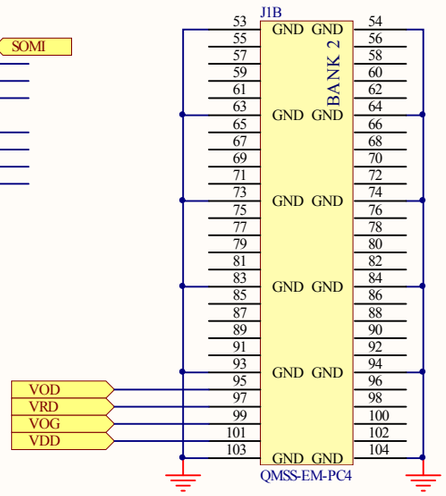
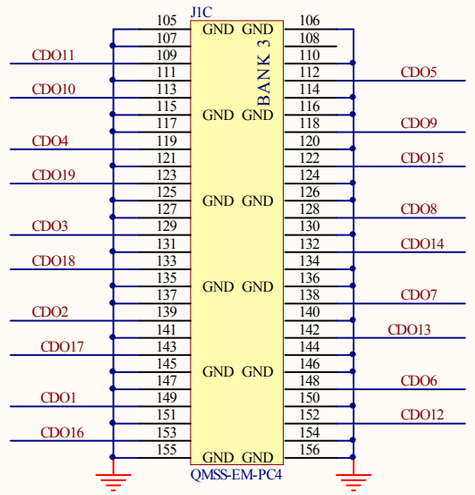


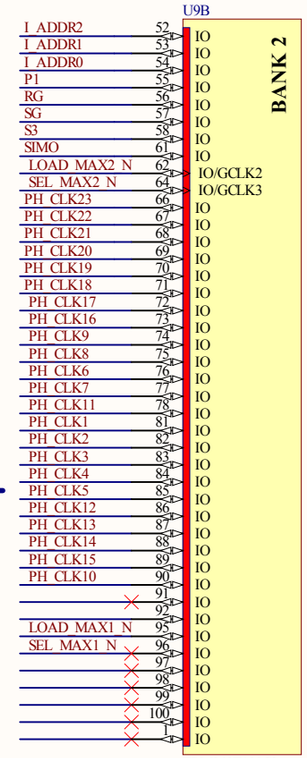




CDO[19..1] CDO[19..1]

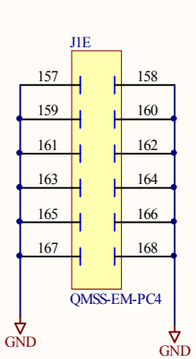
| CDO | DRIVE |
|---|---|
| 1 | S1Q1 |
| 2 | S1Q2 |
| 3 | S1Q3 |
| 4 | S1Q4 |
| 5 | S2Q1 |
| 6 | S2Q2 |
| 7 | S2Q3 |
| 8 | S2Q4 |
| 9 | S3 |
| 10 | RG |
| 11 | SG |
| 12 | P1A |
| 13 | P1B |
| 14 | P2A |
| 15 | P2B |
| 16 | P3A |
| 17 | P3B |
| 18 | TGA |
| 19 | TGB |

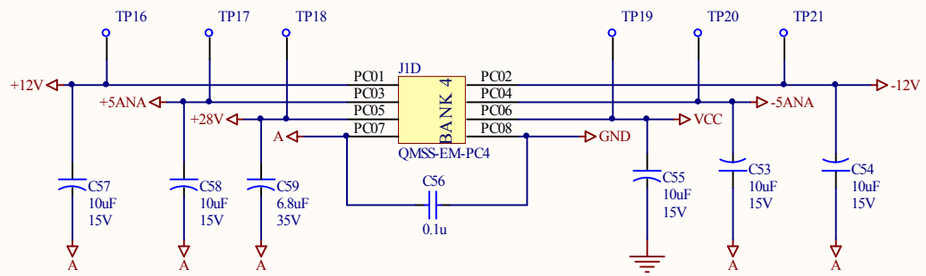



Typcial Pwr dissipation for CPLD Altera EPM240 with 3.3 V Vcc and running at 100 MHz is 100 mW (Altera app note re: MAX II power considerations)



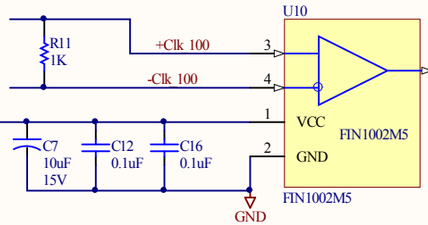

PH_CLK[23..1] PH_CLK[23..1]

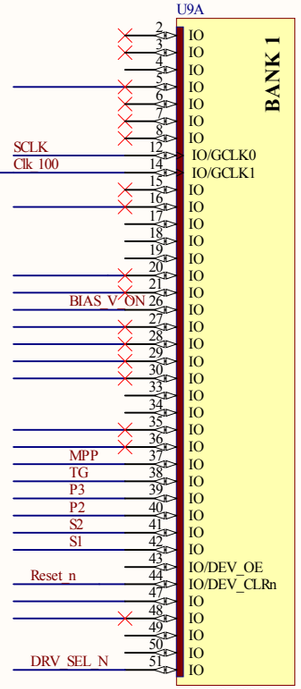



Pins adjacent to and pin below signal are all grounded

BIAS_V_ON
SEL_MAX1_n
SEL_MAX2_n
LOAD_MAX1_n
LOAD_MAX2_n

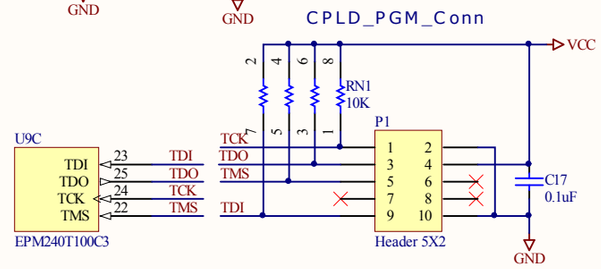


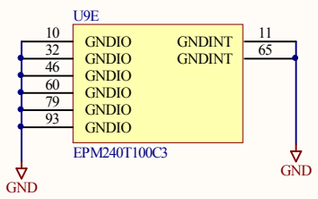



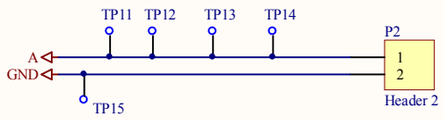

Had a signal net SEL_N(6) which only showed up as an input to CPLD. Could I have deleted it as an input coming from FPGA board? .

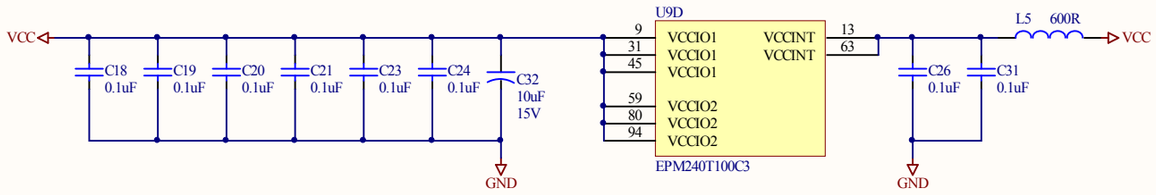
Status: removed net signal

Added a new signal to CPLD BIAS_V_ON which switches on the bais voltages to the CCD. Was generated by MAX ADC chip but seemed more logical here.




| | | | |
|---|---|---|---|
| Title | SINISTRO CAMERA CLOCK DRIVER | | |
| | REV. DATE APRIL 27, 2009 | | |
| Size: B | Number: | Revision: A-1 | |
| Date: 5/11/2009 | | Sheet of: 7 OF 7 | |
| File: \\..\Sinistro_Clk_10A.SchDoc | | Drawn By: | |

Power dissipation of MAX1257 is about 20 mW with all DAC outputs at zero. Max internal power dis by DAC is with 2.5 Vout and 500 ohm load (12.5 mW per DAC). Worst case for part would be 8*(12.5)+20 = 120 mW

MON_LO[1..6]
MON_HI[1..6]

U13
MAX1257
PWR PAD
AIN0 AIN1 AIN2 AIN3 AIN4 AIN5 AIN6 AIN7 AIN8 AIN9 AIN10 AIN11 AIN12 AIN13 REF2/AIN14 CNVST/AIN15 REF1
GPIOA0 GPIOA1 GPIOA2 GPIOA3 GPIOB0 GPIOB1 GPIOB2 GPIOB3 GPIOC0 GPIOC1 GPIOC2 GPIOC3
OUT0 OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 OUT7
DIN SCLK CS LDAC DOUT
RES_SEL EOC AVDD AGND DVDD DGND
DAC_HI1 DAC_LO1 DAC_HI2 DAC_LO2 DAC_HI3 DAC_LO3 DAC_HI4 DAC_LO4
SIMO SCLK SEL_MAX1_n LOAD_MAX1_n SOMI
GND +5ANA C33 0.1u VCC C34 0.1u

U16
MAX1258
DAC_HI5 DAC_LO5 DAC_HI6 DAC_LO6 DAC_VOD DAC_VRD DAC_VOG DAC_VDD
SIMO SCLK SEL_MAX2_n LOAD_MAX2_n SOMI
C35 0.1u C36 0.1u

SOMI SCLK SIMO SEL_MAX1_n SEL_MAX2_n LOAD_MAX1_n LOAD_MAX2_n

BIAS_V_ON

Bias Voltages
Sinistro_Clk_34A.SchDoc
DAC_VOD DAC_VRD DAC_VOG DAC_VDD BIAS_V_ON
VOD VRD VOG VDD MON_VOD MON_VRD MON_VOG MON_VDD

DAC_HI[6..1]
DAC_LO[6..1]
DAC_HI
DAC_LO

REPEAT(RefAmps,1,6)
Sinistro_Clk_31A.schdoc
REPEAT(DAC_HI) REPEAT(DAC_LO) REPEAT(VREFHI) REPEAT(VREFLO) REPEAT(MON_HI) REPEAT(MON_LO)
VREFHI VREFLO MON_HI MON_LO
VREFHI[6..1] VREFLO[6..1] MON_HI[1..6] MON_LO[1..6]

P3
Header 12X2
PH_CLK12 PH_CLK5 PH_CLK13 PH_CLK15 PH_CLK10 PH_CLK11 PH_CLK6 PH_CLK9 PH_CLK17 PH_CLK19 PH_CLK21 PH_CLK23
PH_CLK1 PH_CLK2 PH_CLK3 PH_CLK4 PH_CLK14 PH_CLK7 PH_CLK8 PH_CLK16 PH_CLK18 PH_CLK20 PH_CLK22
GND

PH_CLK[1..9]
PH_CLK1 PH_CLK2 PH_CLK3 PH_CLK4 PH_CLK5 PH_CLK6 PH_CLK7 PH_CLK8 PH_CLK9
PH_CLK10
PH_CLK11
PH_CLK[12..15]
PH_CLK12 PH_CLK13 PH_CLK14 PH_CLK15
PH_CLK16 PH_CLK17
PH_CLK18 PH_CLK19
PH_CLK[23..1]
PH_CLK20 PH_CLK21
PH_CLK22 PH_CLK23

REPEAT(Serial Phase,1,9)
Sinistro_Clk_32A.schdoc
VREFHI1 VREFLO1 PH_CLK REPEAT(CDO) REPEAT(PH_CLK) CDO CDO[1..9]

Reset Gate
Sinistro_Clk_32A.schdoc
VREFHI2 VREFLO2 VREFHI VREFLO PH_CLK CDO CDO10

Summing Gate
Sinistro_Clk_32A.schdoc
VREFHI3 VREFLO3 VREFHI VREFLO PH_CLK CDO CDO11

REPEAT(PPhase1/2,12,15)
Sinistro_Clk_32A.schdoc
VREFHI4 VREFLO4 VREFHI VREFLO PH_CLK REPEAT(CDO) REPEAT(PH_CLK) CDO CDO[12..15]

P3A
Sinistro_Clk_33A.schdoc
VREFHI5 VREFLO5 VREFHI VREFLO PH_CLK MPP_DELAY CDO CDO16

P3B
Sinistro_Clk_33A.schdoc
VREFHI VREFLO PH_CLK MPP_DELAY CDO CDO17

TGA
Sinistro_Clk_33A.schdoc
VREFHI6 VREFLO6 VREFHI VREFLO PH_CLK MPP_DELAY CDO CDO18

TGB
Sinistro_Clk_33A.schdoc
VREFHI VREFLO PH_CLK MPP_DELAY CDO CDO19

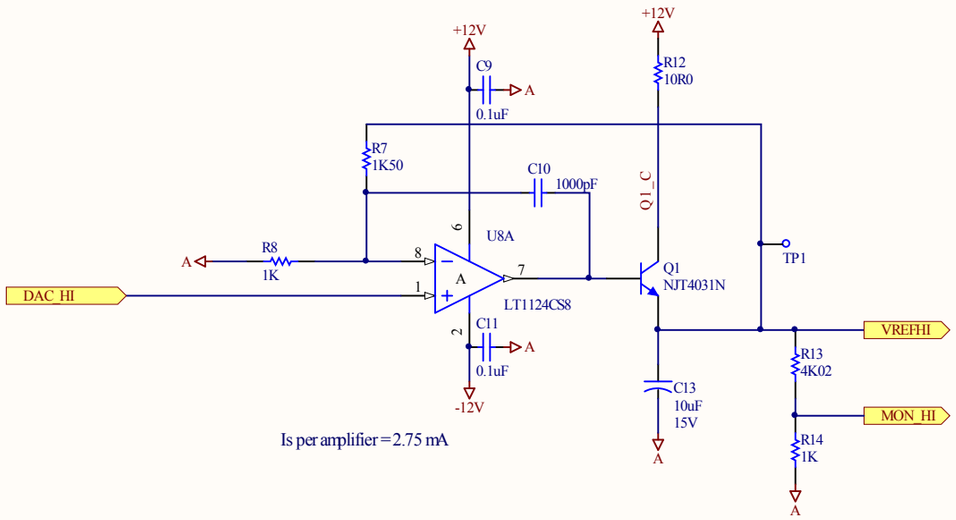
CDO[19..1]
CDO1 CDO2 CDO3 CDO4 CDO5 CDO6 CDO7 CDO8 CDO9 CDO10 CDO11 CDO12 CDO13 CDO14 CDO15 CDO16 CDO17 CDO18 CDO19

| PH_CLK | Signal | P3 |
|---|---|---|
| 1 | S1Q1 | 2 |
| 2 | S1Q2 | 4 |
| 3 | S1Q3 | 6 |
| 4 | S1Q4 | 8 |
| 5 | S2Q1 | 3 |
| 6 | S2Q2 | 13 |
| 7 | S2Q3 | 12 |
| 8 | S2Q4 | 14 |
| 9 | S3 | 15 |
| 10 | RG | 9 |
| 11 | SG | 11 |
| 12 | P1A | 1 |
| 13 | P1B | 5 |
| 14 | P2A | 10 |
| 15 | P2B | 7 |
| 16 | P3A | 16 |
| 17 | P3A_MPP | 17 |
| 18 | P3B | 18 |
| 19 | P3B_MPP | 19 |
| 20 | TGA | 20 |
| 21 | TGA_MPP | 21 |
| 22 | TGB | 22 |
| 23 | TGB_MPP | 23 |

| CDO | DRIVE |
|---|---|
| 1 | S1Q1 |
| 2 | S1Q2 |
| 3 | S1Q3 |
| 4 | S1Q4 |
| 5 | S2Q1 |
| 6 | S2Q2 |
| 7 | S2Q3 |
| 8 | S2Q4 |
| 9 | S3 |
| 10 | RG |
| 11 | SG |
| 12 | P1A |
| 13 | P1B |
| 14 | P2A |
| 15 | P2B |
| 16 | P3A |
| 17 | P3B |
| 18 | TGA |
| 19 | TGB |

Title: SINISTRO CAMERA CLOCK DRIVER
REV. DATE APRIL 27, 2009

| Size | Number | Revision |
|---|---|---|
| B | | A-1 |
| Date: 5/11/2009 | | Sheet of |
| File: \\..\Sinistro_Clk_30A.SchDoc | | Drawn By: 2 OF 7 |




Is per amplifier = 2.75 mA

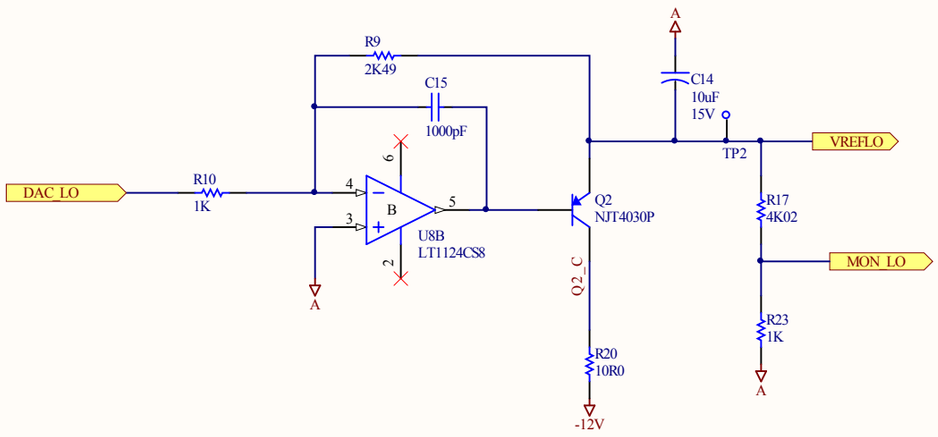
Max quiescent pwr for U8 = 132 mW

Max q pwr for Q1 or Q2 (+6V/-6V out) = 21.6 mW

## Power Dissipation (worst case)

| | U8 | Q1 or Q2 quiescent (Vout = +/- 6V) | Q1 or Q2 Load* (Vout = +/- 6V) | Total W (U8 + Q1 +Q2) |
|---|---|---|---|---|
| VREFHI/LO 1 | 132mW | 21.6mW | 319 mW | 814 mW |
| VREFHI/LO 2 | " | " | neg | 175 mW |
| VREFHI/LO 3 | " | " | neg | 175 mW |
| VREFHI/LO 4 | " | " | 406 mW | 988 mW |
| VREFHI/LO 5 | " | " | 288 mW | 752 mW |
| VREFHI/LO 6 | " | " | 9.2 mW | 194 mW |
| | | | | 2.92 W |

*1 MHz pixel rate/all quadrants clocked

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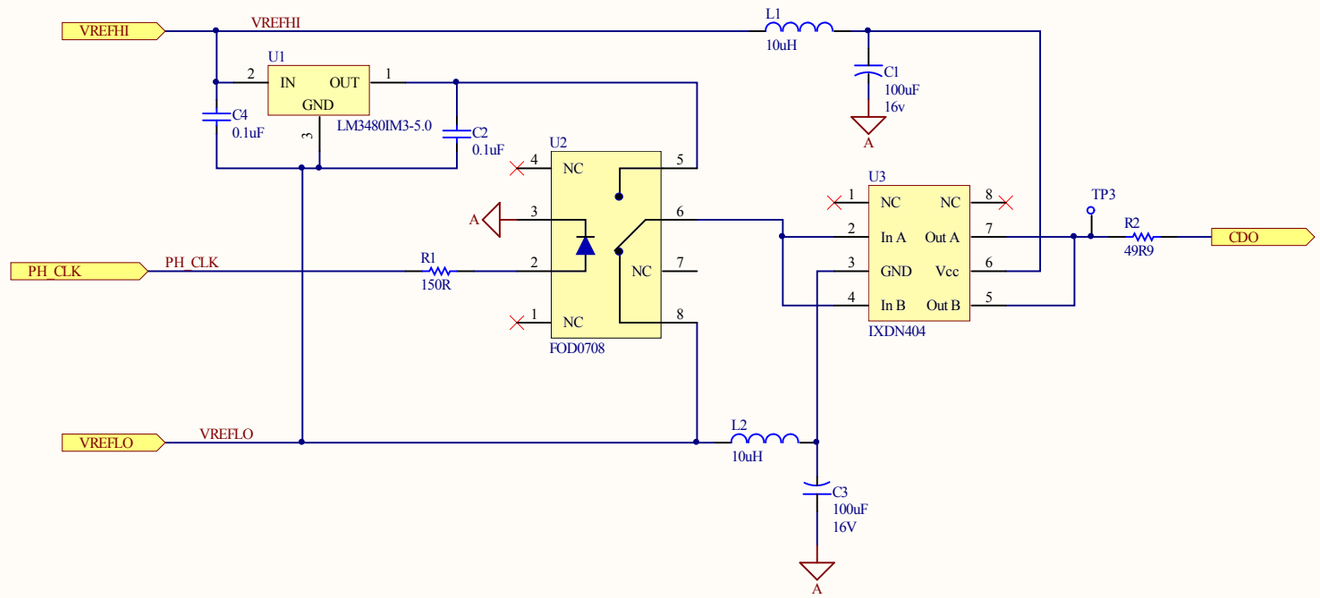
|---|---|---|
| Title | SINISTRO CAMERA CLOCK DRIVER<br>REV. DATE APRIL 22, 2009 | |
| Size: B | Number: | Revision: A |
| Date: 5/11/2009 | Sheet of | |
| File: \\..\Sinistro_Clk_31A.SchDoc | Drawn By: | 3 OF 7 |

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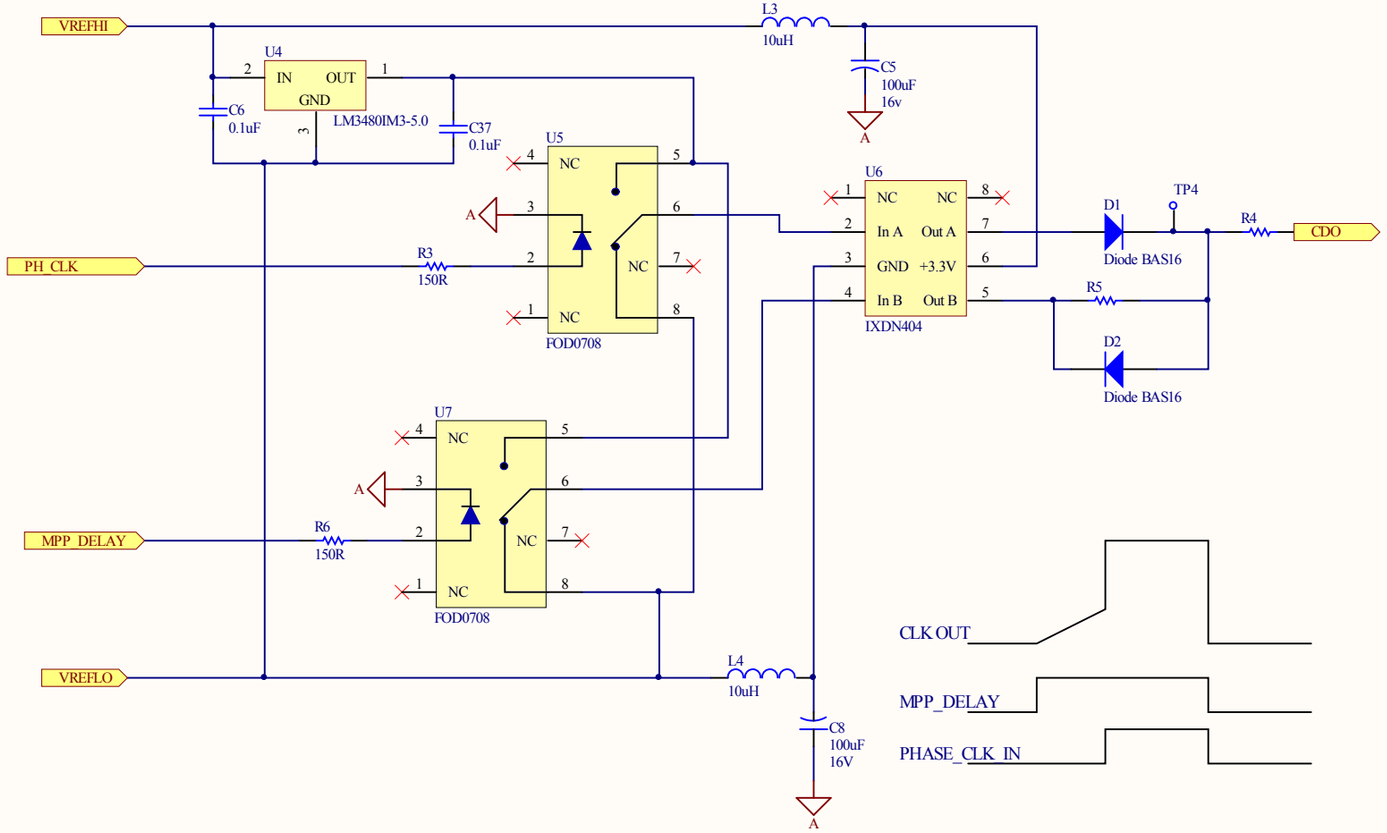
|---|---|---|---|
| Title | SINISTRO CAMERA CLOCK DRIVER | | |
| | REV. DATE APRIL 22, 2009 | | |
| Size: B | Number: | Revision: A | |
| Date: 5/11/2009 | | Sheet of: 4 OF 7 | |
| File: \\..\Sinistro_Clk_32A.SchDoc | | Drawn By: | |




| | | |
|---|---|---|
| Title | SINISTRO CAMERA CLOCK DRIVER<br>REV. DATE APRIL 22, 2009 | |
| Size: B | Number: | Revision: A |
| Date: 5/11/2009 | Sheet of | |
| File: \\..\Sinistro_Clk_33A.SchDoc | Drawn By: | 5 OF 7 |

DAC output swings between zero 4.096V

Worst Case PWR dissipation this page = 770 mW

Quesient current for 1124
2.75 mA each amp

Pd of Q3:

(14.5V/4.32K)*13.5V = 45 mW

Swings between +14.5V and +27.3V

+28V
C22 0.1uF
C29 0.1uF
R15 4K32
2.9
1
-5VREF
R16 1K50
DAC_VOD
R28 1K
x1/1.248
R29 4K02
U11A LT1124CS8
77mW
Q3 NJT4031N
45 mW
R30 10R0
R31 22K6
13.33
MON_VOD
R32 1K82

TP5 U17A DG202 2 3 VOD
TP6 U17B DG202 7 6 VRD
TP7 U17C DG202 11 10 VOG
TP8 U17D DG202 15 14 VDD

Swings between +6V and +18V

Swings between -7V and +5V

Swings between +13 V to +17 V used with e2V only

+28V
C28 0.1uF
1.2
R18 6K04
R27 8K25
-5VREF
R19 4K99
DAC_VRD
U11B LT1124CS8
77mW
R33 10R0
Q4 NJT4031N
26.5mW
R34 22K1
1/8.79
R35 2K80
MON_VRD

Pd of Q4:

(14-2.66)V/6.04K*14V = 26.5 mW

U12A LT1124CS8
66mW

+12V
C30 0.1uF
R21 3K24
2.93
C25 0.1uF
1
DAC_VOG
R22 1K10
+5VREF
R24 10K7
1/3.93
R25 3K65
U12B LT1124CS8
86.4mW
C27 0.1uF
-12V
R36 10K5
R38 4K32
1/3.42
MON_VOG

Pd of U12B:

2.75 mA * 24V

+ (11V/3.24K*6V) = 86.4 mW

BIAS_V_ON
U17E DG202
1 8 9 16 A B C D
13 V+
5 GND
4 V- 12 NC
+28V
C38 0.1u

C39 0.1uF
2.6
R37 2K61
+28V
C40 0.1uF
1
-5VREF
R40 1K
DAC_VDD
10K R42
R41 3K74
1/3.68
U18B LT1124CS8
77mW
R39 10R0
Q5 NJT4031N
73.6 mW
R43 10K
MON_VDD
R44 1K37
1/8.30

U18A LT1124CS8
77mW

Pd of Q5:

(14-0.27)V/2.61K*14V = 73.6 mW

3 of the 4 bais voltages need to output a voltage between 8 and 27V so they need rails that go between 0 and +28V. The 4th bias needs to go from -7 to +5 and needs +/- 12V rails. I used 3 dual op-amps to provide this functionality.

TP9
U14A LT1124CS8
77mW
+5VREF
R46 1K
TP10
-5VREF
+12V
C41 0.1uF
R45 1K
U14B LT1124CS8
77mW
-12V
C43 0.1uF

U15 REF02AU
IN OUT NC NC TEMP NC GND TRIM
+12V
R47 100K
C42 1uf

| Title | SINISTRO CAMERA CLOCK DRIVER | |
|---|---|---|
| | REV. DATE APRIL 22, 2009 | |
| Size: B | Number: | Revision: A |
| Date: 5/11/2009 | | Sheet of: 6 OF 7 |
| File: \\..\Sinistro_Clk_34A.SchDoc | | Drawn By: |