Lab Week3, 20 points Name: _____

Due: Wednesday, September 16th, 5:20pm

The purpose of this lab is to familiarize you with the DE10-Lite board, and how a Quartus based project interfaces to the board.

A separate answer sheet is included in the lab archive. **Please submit only the answer sheet for this lab.** All files reference are in the ECEN2350_Lab3.zip file.

Part 1. (4 points) The purpose of Part 1 is to familiarize you with the details of your DE10-Lite board. Open the user's manual for the DE10-Lite board. Using this manual, answer the following questions from Section 3.3 of the manual:

a) What logic level (logic 0 or logic 1) will be seen at the FPGA input pins when a pushbutton is pressed and held?

_____Answer sheet_____

b) What logic level will be seen at the FPGA input pins when a slide switch is pushed toward the center of the board?

_____Answer sheet_____

c) What logic level turns on the LEDRs?

_____Answer sheet_____

c) What logic level turns on the segments of the 7-segment displays?

_____Answer sheet_____

Part 2. (2 points) Open the Lab3.qsf file in a text editor, being careful to not modify this file. Answer the following questions:

a) How many total FPGA pins are used to connect to the 6 7-segment displays?

_____Answer sheet_____

b) What input/output voltage is used for all the signals defined in the .qsf file?

_____Answer sheet_____

The inputs and outputs in your top level Verilog file are the signals that Quartus will connect to the MAX10 FPGA pins. The top level module input and output names must exactly match the names used in the .qsf file. A top level input or output signal that does not have a corresponding entry in the .qsf file will be assigned to a random FPGA pin by the Quartus software. Random pin assignments will guarantee that your design will not operate correctly on the DE10-Lite board.

Part 3. (6 points) Open your text editor and create a new file called Start.v

a) The inputs to the Verilog module will be a, b, c, and d.

b) The output from this module will be x.

c) The truth table that defines output x is

a	**b**	**c**	**d**	**x**
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

d) Complete your Start.v file by coding the sum of products equation to match the truth table.

Hint 1: Refer to Appendix A in the text for Verilog syntax.

Hint 2: You must use the Verilog keyword `assign` at the beginning of each equation.

Hint 3: If you want to create intermediate values, you must declare these signals using the keyword `wire`. For this assignment, intermediate values are not required, but you are free to use them if it is helpful.

e) Open tb_Start.v in a text editor. On line 21, **replace the words Simulation complete with your name**, and save the file.

f) Simulate your Start.v file using the tb_Start.v testbench. Correct any mistakes in your Start.v file so that the simulation completes without errors. **Attach a screenshot of the simulation result when you submit this lab.**

Part 4. (6 points) Open the Lab3 Quartus project using the files in Lab3.zip. Add Lab3.v as a source to your Quartus project.

a) Paste the equations you created in Part3 into Lab3.v.

b) Change the values a, b, c, and d to SW[3], SW[2], SW[1], and SW[0]. This change will connect the 4 switches on the DE10-Lite board so that these switches values will now be used as inputs to your design.

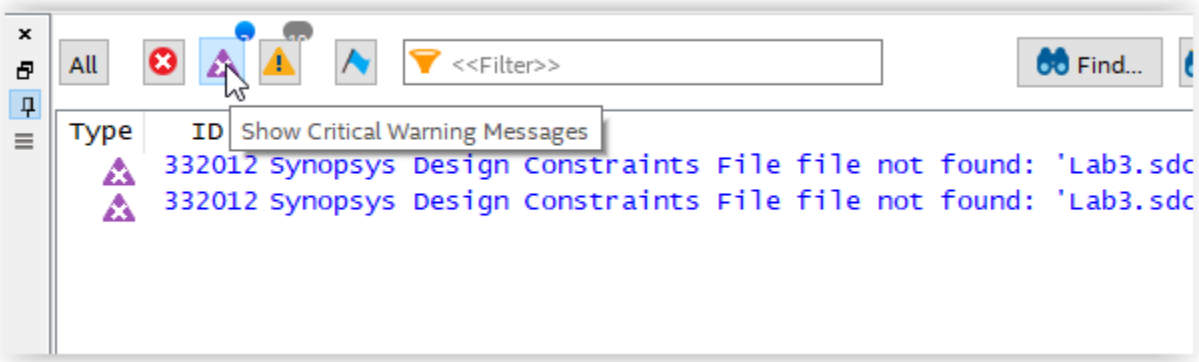
c) Change the value x to LEDR[0]. This will connect the output of your design to the LED on your board.

d) Compile your design in Quartus.

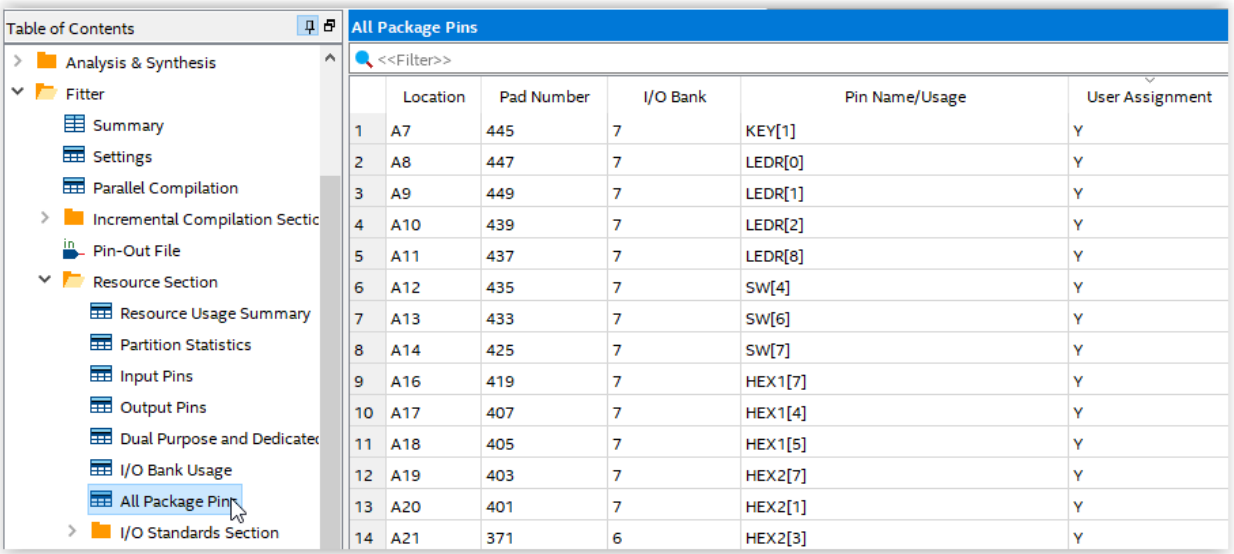
e) When your design has compiled with 0 errors, verify that your design has the correct pinout.

i) Click the purple triangle toward the bottom right of the Quartus screen. Any messages that show up when you click the purple triangle are called critical warnings. It is a good idea to always look at critical warnings after compiling a project. You can return to viewing all messages and warnings by clicking the All button.

You should not see any messages stating that unassigned pins exist.



ii) In the Table of Contents, go to Fitter > Resource Section > All Package Pins as shown below. Click on the User Assignment Heading to sort the results so that you see values in the User Assignment column. Verify that the first 70 rows show a Y in the User Assignment column. This indicates that all pins received location assignments from the project .qsf file.



	Location	Pad Number	I/O Bank	Pin Name/Usage	User Assignment
1	A7	445	7	KEY[1]	Y
2	A8	447	7	LEDR[0]	Y
3	A9	449	7	LEDR[1]	Y
4	A10	439	7	LEDR[2]	Y
5	A11	437	7	LEDR[8]	Y
6	A12	435	7	SW[4]	Y
7	A13	433	7	SW[6]	Y
8	A14	425	7	SW[7]	Y
9	A16	419	7	HEX1[7]	Y
10	A17	407	7	HEX1[4]	Y
11	A18	405	7	HEX1[5]	Y
12	A19	403	7	HEX2[7]	Y
13	A20	401	7	HEX2[1]	Y
14	A21	371	6	HEX2[3]	Y

e) Download the design to your DE10-Lite board. Using the switches defined in Lab3.v, does your design work correctly?

_____Answer sheet_____