

ECEN2350 Digital Logic - Lab1

Fall, 2020

Due Monday August 31st (beginning of class) 20 Points

Name: Case Chrisbacher _____

[Question 1 – 1 pt]

What type of computer are you using (Windows, Apple, Linux)? _____ Apple _____

[Question 2 - 1 pt]

Were you able to successfully install Verilog (Yes / No)? _____ Yes _____

If no, briefly explain the problems you are having:

[Question 3 – 1 pt]

Were you able to successfully install GTKWave (Yes / No)? _____ Yes _____

If no, briefly explain the problems you are having:

[Question 4 - 1 pt]

Were you able to successfully compile and simulate the my_and design (Yes / No)? _____ Yes _____

If no, briefly explain the problems you are having:

[Question 5 - 1 pt]

Which text editor will you use in ECEN2350 this semester? _____ Visual Studio Code _____

[Question 6 - 3 pts]

The first line of a testbench is ``timescale 10 ns / 1 ns`

#10 will result in how much simulation time delay? _____ 400 ns _____

Hint: If you aren't sure, simulate it.

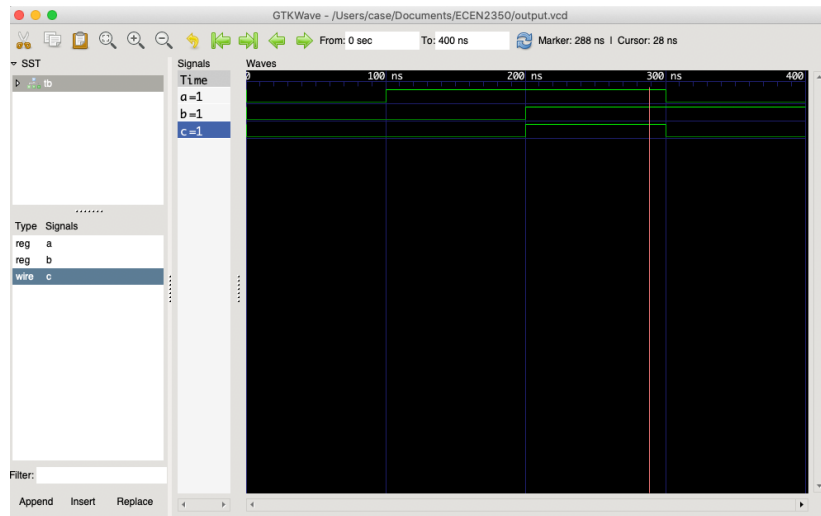
[Question 7 - 4 pts]

What are the two primary functions provided by iVerilog?

_____ VerilogCompiler _____ and _____ VerilogSimulator _____

[Question 8 - 4 pts]

Paste your screenshots to your GTKWave my_and simulation here.



```
EXPLORER  my_and.v  tb.v
OPEN EDITORS
my_and.v
tb.v
ECEN2350
a.out
Digital Logic Textbook...
my_and.v
output.txt
output.vcd
tb.v

1: `timescale 1 ns / 100 ps
2: module tb();
3:   reg a, b;
4:   wire c;
5:   my_and u1 (.in1(a), .in2(b), .out(c));
6:   initial
7:   begin
8:     $dumpfile("output.vcd");
9:     $dumpvars;
10:    $display("Starting simulation");
11:    a = 0;
12:    b = 0;
13:    #10 a = 1;
14:    #10 b = 1;
15:    #10 a = 0;
16:    #10 $display("Simulation ended.");
17:    $display("Case Christopher");
18:    $finish;
19:  end
20:  initial
21:  begin
22:    $monitor($time, "a = %b, b = %b, c = %b", a, b, c);
23:  end
endmodule

PROBLEMS  OUTPUT  TERMINAL  DEBUG CONSOLE
Case: MacBook-Pro-0: ECEN2350 case5 iverilog tb.v my_and.v
Case: MacBook-Pro-0: ECEN2350 case5 vvp a.out > out.txt
Case: MacBook-Pro-0: ECEN2350 case5 vvp a.out
VDP info: dumpfile output.vcd opened for output.
Starting simulation
a = 0, b = 0, c = 0
10a = 1, b = 0, c = 0
10a = 1, b = 1, c = 1
10a = 0, b = 1, c = 0
10a = 0, b = 0, c = 0
Simulation ended.
Case Christopher
Case: MacBook-Pro-0: ECEN2350 case5 [
```