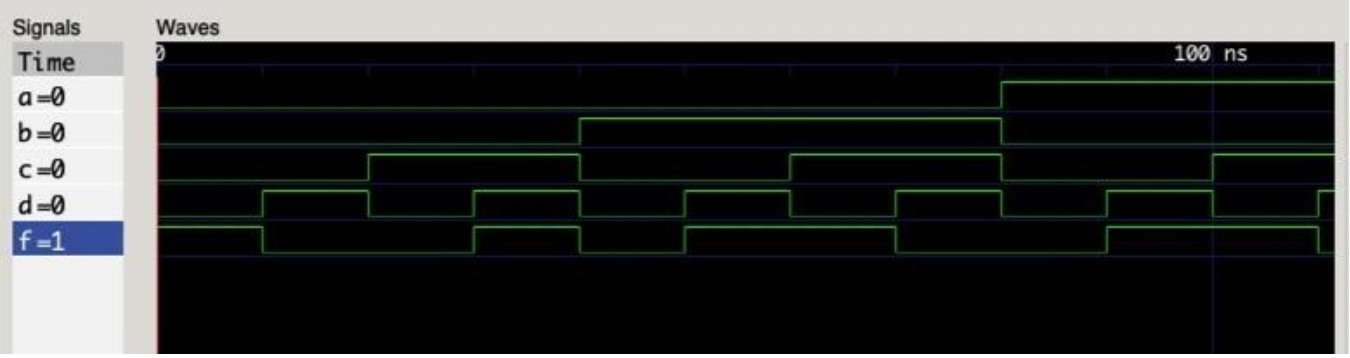
Lab Week 2 **NAME:** Case Chrisbacher

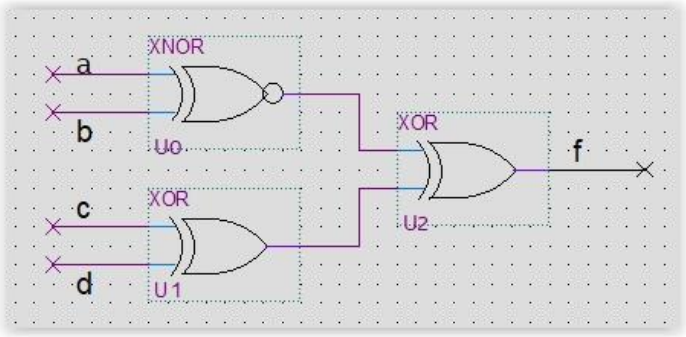
Due: Wednesday, September 9, 2020

Part1 (**10 Pts)**:



a	b	c	d	f
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

5. SOP = (~a)*(~b)*(~c)*(~d) + (~a)*(~b)*(c)*(d) + (~a)*(b)*(~c)*(d) + (~a)*(b)*(c)*(~d) + (a)*(~b)*(~c)*(d) + (a)*(~b)*(c)*(~d) + (a)*(b)*(~c)*(~d) + (a)*(b)*(c)*(d)

6. 

a	b	c	d	f
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

7. Yes, the truth tables do match, the Verilog simulation is running the gate displayed in problem six.

Complete the Lab:

Values (8 pts): 0000, 0011, 0101, 0110, 1001, 1010, 1100, 1111

= (~a)*(~b)*(~c)*(~d) + (~a)*(~b)*(c)*(d) + (~a)*(b)*(~c)*(d) + (~a)*(b)*(c)*(~d) + (a)*(~b)*(~c)*(d) + (a)*(~b)*(c)*(~d) + (a)*(b)*(~c)*(~d) + (a)*(b)*(c)*(d)

The Verilog description of the circuit is the exact same as the Sum of Products, because they are both describing the same schematic.