HEWLETT PACKARD

8 Character 5 mm and 7 mm Smart Alphanumeric Displays

Technical Data

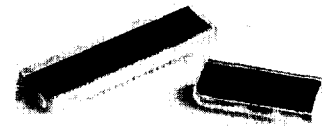
HDSP-211X Series
HDSP-212X Series
New **HDSP-250X Series**

Features

- **X Stackable (HDSP-211X/ -212X)**
- **XY Stackable (HDSP-250X)**
- **128 Character ASCII Decoder or 128 Character Katakana Decoder**
- **Programmable Functions**
- **16 User Definable Characters**
- **Multi-Level Dimming and Blanking**
- **TTL Compatible CMOS IC**
- **Wave Solderable**

Description

The HDSP-211X/-212X/-250X series of products is ideal for applications where displaying eight or more characters of dot matrix information in an aesthetically pleasing manner is required. These devices are 8-digit, 5 x 7 dot matrix, alphanumeric displays and are all packaged in a standard 15.24 mm (0.6 inch) 28 pin DIP. The on-board CMOS IC has the ability to decode 128 ASCII characters (HDSP-211X/-250X) or 128 Katakana characters (HDSP-212X), which are permanently stored in ROM. In addition, 16 programmable symbols may be stored in on-board ROM, allowing considerable flexibility for displaying additional symbols and icons. Seven brightness levels provide versatility in adjusting the display intensity and power consumption. The HDSP-211X/-212X/-250X products are designed for standard microprocessor interface techniques. The display and special features are accessed through a bidirectional 8-bit data bus.



Applications

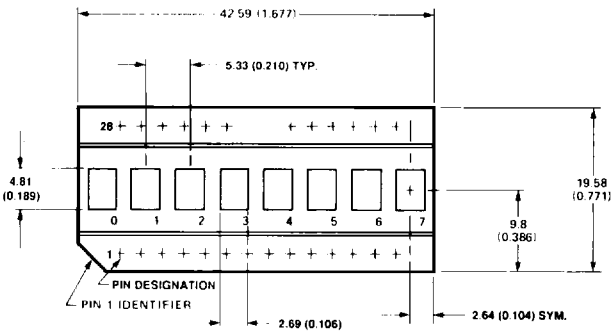
- **Computer Peripherals**
- **Industrial Instrumentation**
- **Medical Equipment**
- **Portable Data Entry Devices**
- **Cellular Phones**
- **Telecommunications Equipment**
- **Test Equipment**

Device Selection Guide

Font Height	Character Set	High Efficiency Red	Orange	Yellow	Green
0.2 inches	ASCII	HDSP-2112	HDSP-2110	HDSP-2111	HDSP-2113
0.2 inches	Katakana*	HDSP-2122	–	HDSP-2121	HDSP-2123
0.27 inches	ASCII	HDSP-2502	HDSP-2500	HDSP-2501	HDSP-2503

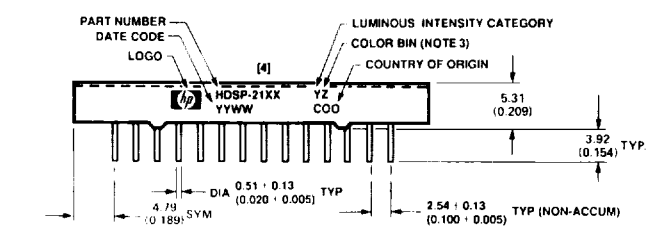
*Katakana is a simplified version of the Japanese alphabet.

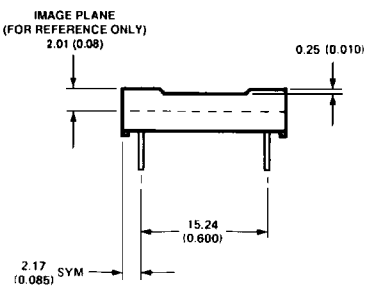
Package Dimensions



Pin Function Assignment Table

Pin No.	Function	Pin No.	Function
1	$\overline{RST}$	15	GND(SUPPLY)
2	FL	16	GND (LOGIC)
3	A_0	17	$\overline{CE}$
4	A_1	18	$\overline{RD}$
5	A_2	19	D_0
6	A_3	20	D_1
7	DO NOT CONNECT	21	NO PIN
8	DO NOT CONNECT	22	NO PIN
9	DO NOT CONNECT	23	D_2
10	A_4	24	D_3
11	CLS	25	D_4
12	CLK	26	D_5
13	$\overline{WR}$	27	D_6
14	V_{DD}	28	D_7





NOTES:
1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED, TOLERANCE ON ALL DIMENSIONS IS ± 0.25 mm (0.010 INCH).
3. FOR YELLOW AND GREEN DEVICES ONLY.
4. MARKING IS ON SIDE OPPOSITE PIN 1.

HDSP-21XX

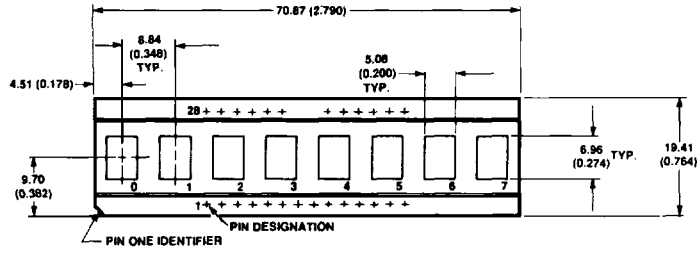
Absolute Maximum Ratings

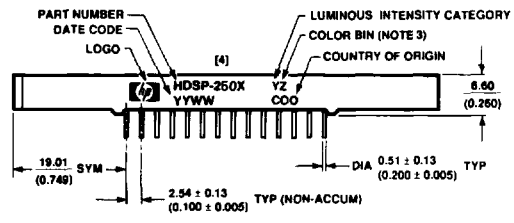
Supply Voltage, V_{DD} to Ground[1] ..... -0.3 to 7.0 V
Operating Voltage, V_{DD} to Ground[2] ..... 5.5 V
Input Voltage, Any Pin to Ground ..... -0.3 to V_{DD} +0.3 V
Free Air Operating Temperature Range, T_A[3] ..... -45°C to +85°C
Storage Temperature Range, T_S ..... -55°C to +100°C
Relative Humidity (non-condensing) 85%
Maximum Solder Temperature
(Below Seating Plane), t < 5 sec ..... 260°C
ESD Protection @ 1.5 kΩ, 100 pF ..... V_Z = 4 kV (each pin)

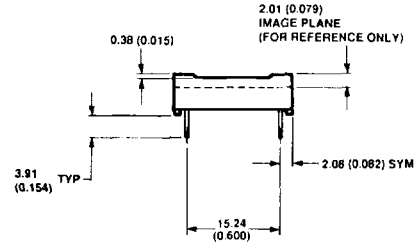
Notes:
1. Maximum Voltage is with no LEDs illuminated.
2. 20 dots ON in all locations at full brightness.
3. Maximum supply voltage is 5.25 V for operation above 70°C.

ESD WARNING: STANDARD CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED TO AVOID STATIC DISCHARGE.

Package Dimensions







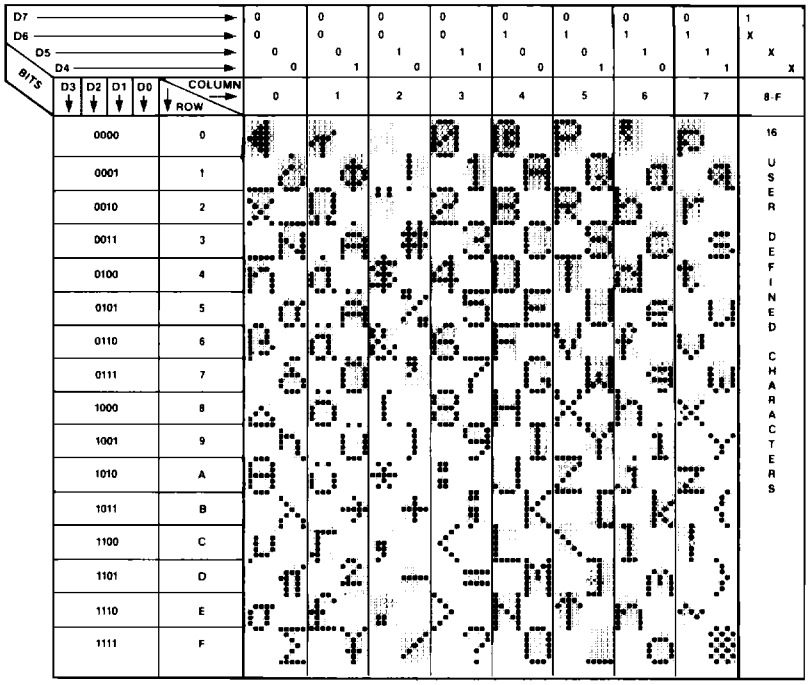
Pin Function Assignment Table

Pin No.	Function	Pin No.	Function
1	$\overline{RST}$	15	GND(SUPPLY)
2	$\overline{FL}$	16	GND (LOGIC)
3	A_0	17	$\overline{CE}$
4	A_1	18	$\overline{RD}$
5	A_2	19	D_0
6	A_3	20	D_1
7	DO NOT CONNECT	21	NO PIN
8	DO NOT CONNECT	22	NO PIN
9	DO NOT CONNECT	23	D_2
10	A_4	24	D_3
11	CLS	25	D_4
12	CLK	26	D_5
13	$\overline{WR}$	27	D_6
14	V_{DD}	28	D_7

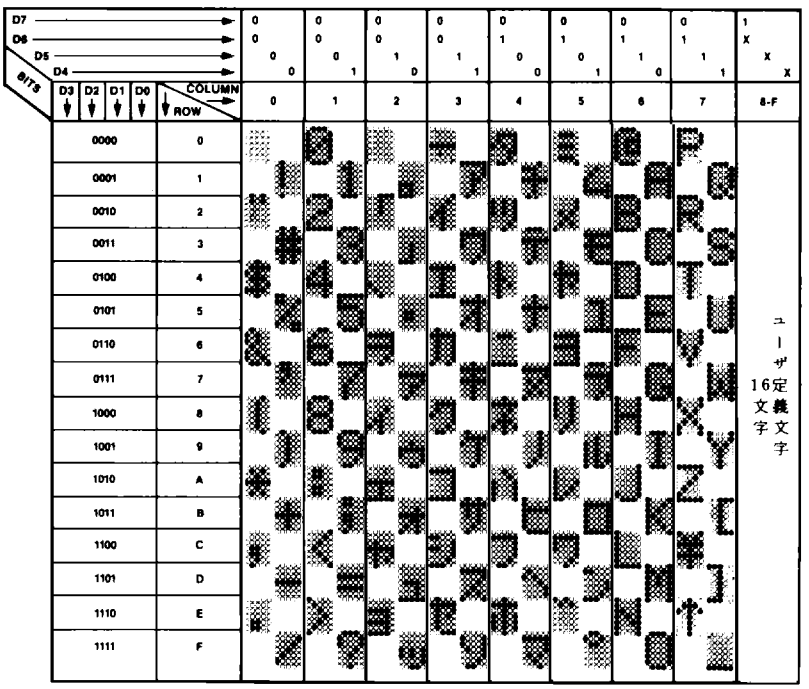
NOTES:
1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED, TOLERANCE ON ALL DIMENSIONS IS ± 0.25 mm (0.010 INCH).
3. FOR YELLOW AND GREEN DEVICES ONLY.
4. MARKING IS ON SIDE OPPOSITE PIN 1.

HDSP-250X

ASCII Character Set HDSP-211X, HDSP-250X Series



Katakana Character Set HDSP-212X Series



Recommended Operating Conditions

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Supply Voltage	V_{DD}	4.5	5.0	5.5	V

Electrical Characteristics Over Operating Temperature Range (-45°C to +85°C)

4.5 V < V_{DD} < 5.5 V, unless otherwise specified

Parameter	Symbol	T_A = 25°C, V_{DD} = 5.0 V		-45°C < T_A < + 85°C, 4.5 V < V_{DD} < 5.5 V		Units	Test Conditions
		Typ.	Max.	Min.	Max.		
Input Leakage (Input without pullup)	I_{IH} I_{IL}				1.0 -1.0	µA	V_{IN} = 0 to V_{DD}, pins CLK, D_0-D_7, A_0-A_4
Input Current (Input with pullup)	I_{IPL}	-11	-18		-30	µA	V_{IN} = 0 to V_{DD}, pins $\overline{CLS}$, $\overline{RST}$, $\overline{WR}$, $\overline{RD}$, $\overline{CE}$, $\overline{FL}$
I_{DD} Blank	I_{DD}(BLK)	0.5	3.0		4.0	mA	V_{IN} = V_{DD}
I_{DD} 8 digits 12 dots/character[1,2]	I_{DD}(V)	200	255		330	mA	"V" on in all 8 locations
I_{DD} 8 digits 20 dots/character[1,2,3,4]	I_{DD}(#)	300	370		430	mA	"#" on in all locations
Input Voltage High	V_{IH}			2.0	V_{DD} +0.3	V	
Input Voltage Low	V_{IL}			GND -0.3 V	0.8	V	
Output Voltage High	V_{OH}			2.4		V	V_{DD} = 4.5 V, I_{OH} = -40 µA
Output Voltage Low D_0-D_7	V_{OL}				0.4	V	V_{DD} = 4.5 V, I_{OL} = 1.6 mA
Output Voltage Low CLK	V_{OL}				0.4	V	V_{DD} = 4.5 V, I_{OL} = 40 µA
High Level Output Current	I_{OH}				-60	mA	V_{DD} = 5.0 V
Low Level Output Current	I_{OL}				50	mA	V_{DD} = 5.0 V
Thermal Resistance IC Junction-to-Case	$R\theta_{J\text{-}C}$	15				°C/W	

Notes:
1. Average I_{DD} measured at full brightness. See Table 2 in Control Word Section for I_{DD} at lower brightness levels. Peak I_{DD} = 28/15 x I_{DD} (#).
2. Maximum I_{DD} occurs at -55°C.
3. Maximum I_{DD}(#) = 355 mA at V_{DD} = 5.25 V and IC T_J = 150°C.
4. Maximum I_{DD}(#) = 375 mA at V_{DD} = 5.5 V and IC T_J = 150°C.

Optical Characteristics at 25°C[1]

V_{DD} = 5.0 V at Full Brightness

Description	Part Number	Luminous Intensity Character Average (#) Iv (mcd) Min.	Typ.	Peak Wavelength λ_{Peak} (nm)	Dominant Wavelength λ_d (nm)
HER	HDSP-2112 -2122 -2502	2.5	7.5	635	626
Orange	HDSP-2110 -2500	2.5	7.5	600	602
Yellow	HDSP-2111 -2121 -2501	2.5	7.5	583	585
High Performance Green	HDSP-2113 -2123 -2503	2.5	7.5	568	574

Note: 1. Refers to the initial case temperature of the device immediately prior to measurement.

AC Timing Characteristics Over Temperature Range (-45°C to +85°C)

4.5 V < V_{DD} < 5.5 V, unless otherwise specified

Reference Number	Symbol	Description	Min.[1]	Units
1	t_{ACC}	Display Access Time Write Read	 210 230	 ns
2	t_{ACS}	Address Setup Time to Chip Enable	10	ns
3	t_{CE}	Chip Enable Active Time[2, 3] Write Read	 140 160	 ns
4	t_{ACH}	Address Hold Time to Chip Enable	20	ns
5	t_{CER}	Chip Enable Recovery Time	60	ns
6	t_{CES}	Chip Enable Active Prior to Rising Edge of[2, 3] Write Read	 140 160	 ns
7	t_{CEH}	Chip Enable Hold Time to Rising Edge of Read/Write Signal[2, 3]	0	ns
8	t_W	Write Active Time	100	ns
9	t_{WSU}	Data Write Setup Time	50	ns
10	t_{WH}	Data Write Hold Time	20	ns
11	t_R	Chip Enable Active Prior to Valid Data	160	ns
12	t_{RD}	Read Active Prior to Valid Data	75	ns
13	t_{DF}	Read Data Float Delay	10	ns
	t_{RC}	Reset Active Time[4]	300	ns

Notes:

1. Worst case values occur at an IC junction temperature of 150°C.
2. For designers who do not need to read from the display, the Read line can be tied to V_{DD} and the Write and Chip Enable lines can be tied together.
3. Changing the logic levels of the Address lines when $\overline{CE}$ = "0" may cause erroneous data to be entered into the Character RAM, regardless of the logic levels of the $\overline{WR}$ and $\overline{RD}$ lines.
4. The display must not be accessed until after 3 clock pulses (110 µs min. using the internal refresh clock) after the rising edge of the reset line.

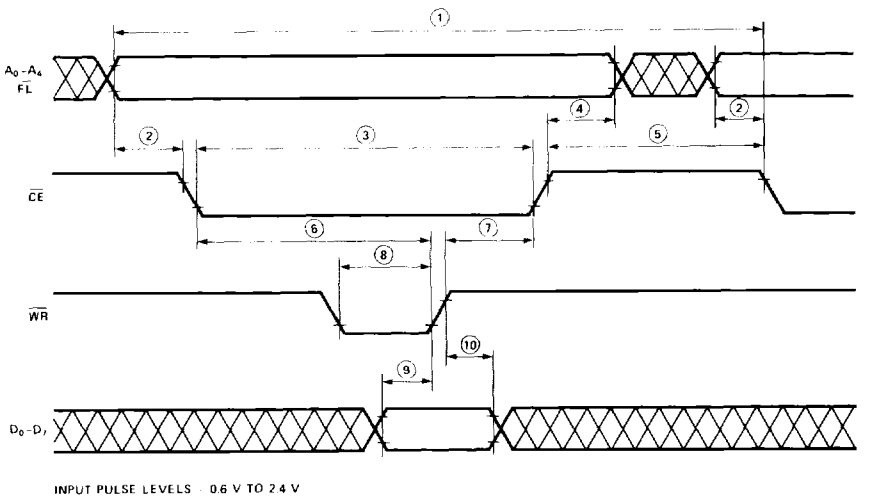
AC Timing Characteristics Over Temperature Range (-45°C to +85°C)

4.5 V < V_{DD} < 5.5 V, unless otherwise specified

Symbol	Description	25°C Typ.	Min.[1]	Units
F_{OSC}	Oscillator Frequency	57	28	kHz
F_{RF}[2]	Display Refresh Rate	256	128	Hz
F_{FL}[3]	Character Flash Rate	2	1	Hz
t_{ST}[4]	Self Test Cycle Time	4.6	9.2	sec

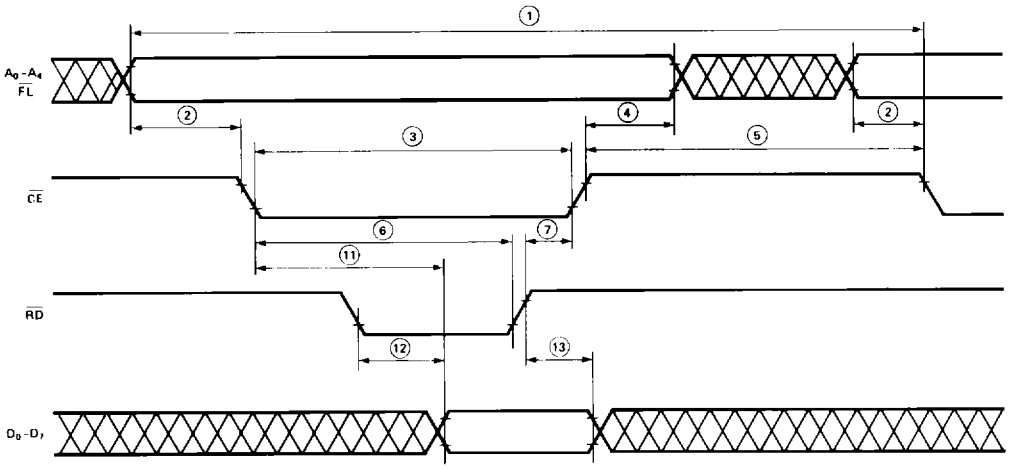
Notes:
1. Worst case values occur at an IC junction temperature of 150°C.
2. $F_{RF} = F_{OSC}/224$
3. $F_{FL} = F_{OSC}/28{,}672$
4. $t_{ST} = 262{,}144/F_{OSC}$

Write Cycle Timing Diagram



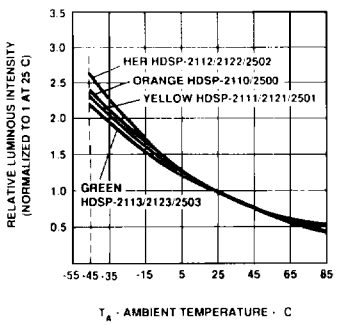
INPUT PULSE LEVELS 0.6 V TO 2.4 V

Read Cycle Timing Diagram



INPUT PULSE LEVELS: 0.6 V TO 2.4 V
OUTPUT REFERENCE LEVELS: 0.6 V TO 2.2 V
OUTPUT LOADING = 1 TTL LOAD AND 100pFd

Relative Luminous Intensity vs. Temperature



Electrical Description

Pin Function	Description
RESET ($\overline{RST}$, pin 1)	Initializes the display.
FLASH ($\overline{FL}$, pin 2)	$\overline{FL}$ low indicates an access to the Flash RAM and is unaffected by the state of address lines A_3-A_4.
ADDRESS INPUTS (A_0-A_4, pins 3-6, 10)	Each location in memory has a distinct address. Address inputs (A_0-A_2) select a specific location in the Character RAM, the Flash RAM or a particular row in the UDC (User-Defined Character) RAM. A_3-A_4 are used to select which section of memory is accessed. Table 1 shows the logic levels needed to access each section of memory.

Table 1. Logic Levels to Access Memory

Section of Memory	$\overline{FL}$	A_4	A_3	A_2 A_1 A_0
Flash RAM	0	X	X	Char. Address
UDC Address Register	1	0	0	Don't Care
UDC RAM	1	0	1	Row Address
Control Word Register	1	1	0	Don't Care
Character RAM	1	1	1	Character Address

CLOCK SELECT (CLS, pin 11)	Used to select either an internal or external clock source.
CLOCK INPUT/OUTPUT (CLK, pin 12)	Outputs the master clock (CLS = 1) or inputs a clock (CLS = 0) for slave displays.
WRITE ($\overline{WR}$, pin 13)	Data is written into the display when the $\overline{WR}$ input is low and the $\overline{CE}$ input is low.
CHIP ENABLE ($\overline{CE}$, pin 17)	Must be at a logic low to read or write data to the display and must go high between each read and write cycle.
READ ($\overline{RD}$, pin 18)	Data is read from the display when the $\overline{RD}$ input is low and the $\overline{CE}$ input is low.
DATA Bus (D_0-D_7, pins 19, 20, 23-28)	Used to read from or write to the display.
GND (SUPPLY) (pin 15)	Analog ground for the LED drivers.
GND (LOGIC) (pin 16)	Digital ground for internal logic.
V_{DD} (POWER) (pin 14)	Positive power supply input.

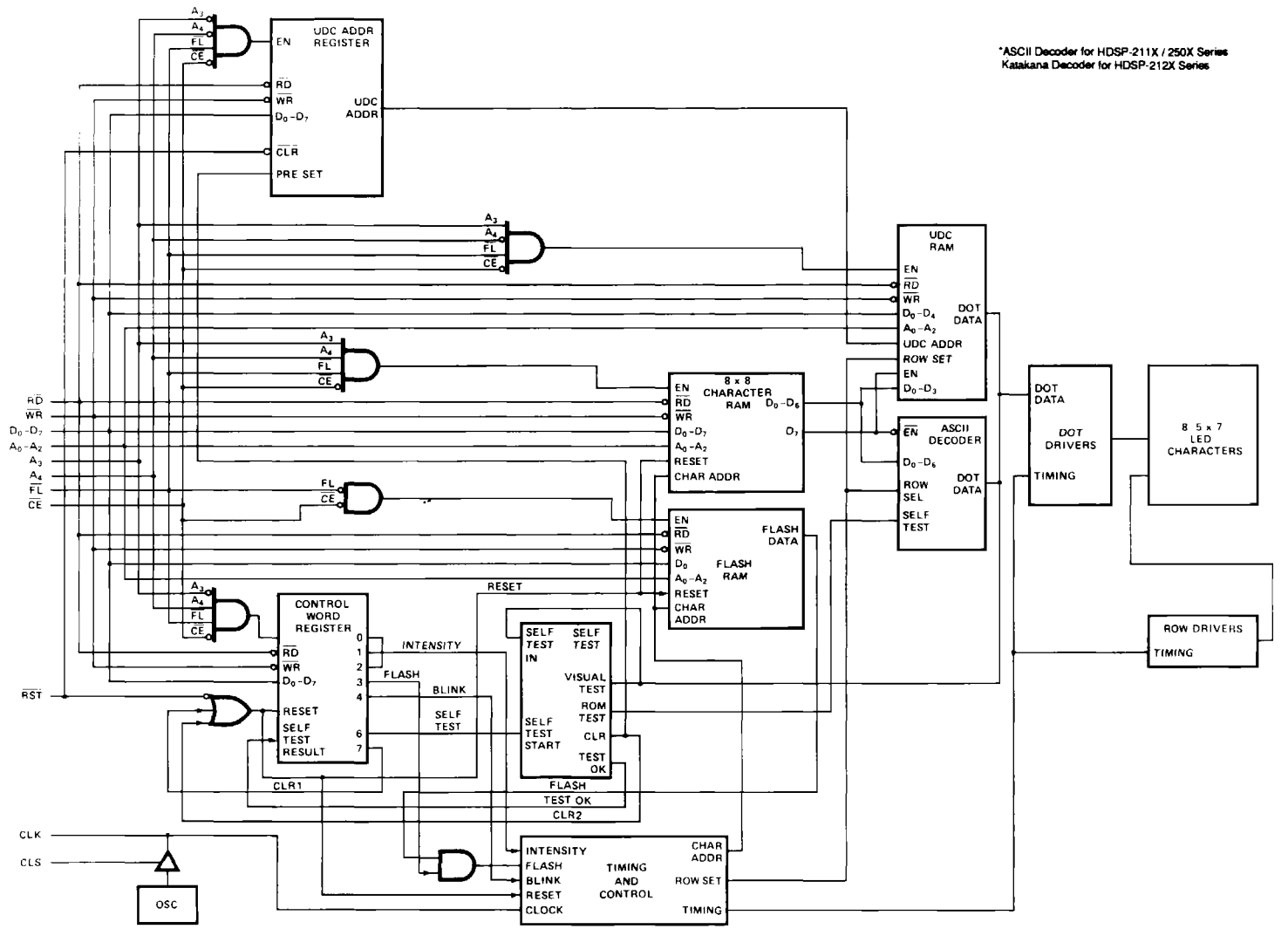


Figure 1. HDSP-211X/-212X/-250X Internal Block Diagram.

Display Internal Block Diagram

Figure 1 shows the internal block diagram of the HDSP-211X/-212X/-250X displays. The CMOS IC consists of an 8 byte Character RAM, an 8 bit Flash RAM, a 128 character ASCII (Katakana) decoder, a 16 character UDC RAM, a UDC Address Register, a Control Word Register, and refresh circuitry necessary to synchronize the decoding and driving of eight 5 x 7 dot matrix characters. The major user-accessible portions of the display are listed below:

Character RAM	This RAM stores either ASCII (Katakana) character data or a UDC RAM address.
Flash RAM	This is a 1 x 8 RAM which stores Flash data.
User-Defined Character RAM (UDC RAM)	This RAM stores the dot pattern for custom characters.
User-defined Character Address Register (UDC Address Register)	This register is used to provide the address to the UDC RAM when the user is writing or reading a custom character.
Control Word Register	This register allows the user to adjust the display brightness, flash individual characters, blink, self test, or clear the display.

Character Ram

Figure 2 shows the logic levels needed to access the HDSP-211X/-212X/-250X Character RAM. During a normal access, the $\overline{CE}$ = "0" and either $\overline{RD}$ = "0" or $\overline{WR}$ = "0". However, erroneous data may be written into the Character RAM if the address lines are unstable when $\overline{CE}$ = "0" regardless of the logic levels of the $\overline{RD}$ or $\overline{WR}$ lines. Address lines A_0-A_2 are used to select the location in the Character RAM. Two types of data can be stored in each Character RAM location: an ASCII (Katakana) code or a UDC RAM address. Data bit D_7 is used to differentiate between the ASCII (Katakana) character and a UDC RAM address. D_7 = 0 enables the ASCII (Katakana) decoder and D_7 = 1 enables the UDC RAM. D_0-D_6 are used to input ASCII (Katakana) data and D_0-D_3 are used to input a UDC address.

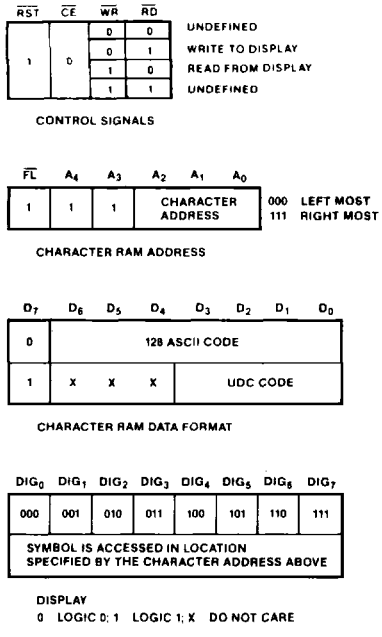


Figure 2. Logic Levels to Access the Character RAM.

UDC RAM and UDC Address Register

Figure 3 shows the logic levels needed to access the UDC RAM and the UDC Address Register. The UDC Address Register is eight bits wide. The lower four bits (D_0-D_3) are used to select one of the 16 UDC locations. The upper four bits (D_4-D_7) are not used. Once the UDC address has been stored in the UDC Address Register, the UDC RAM can be accessed.

To completely specify a 5 x 7 character, eight write cycles are required. One cycle is used to store the UDC RAM address in the UDC Address Register and seven cycles are used to store dot data in the UDC RAM. Data is entered by rows and one cycle is needed to access each row. Figure 4 shows the organization of a UDC character assuming the symbol to be stored is an "F". A_0-A_2 are used to select the row to be accessed and D_0-D_4 are used to transmit the row dot data. The upper three bits (D_5-D_7) are ignored. D_0 (least significant bit) corresponds to the right most column of the 5 x 7 matrix and D_4 (most significant bit) corresponds to the left most column of the 5 x 7 matrix.

Flash RAM

Figure 5 shows the logic levels needed to access the Flash RAM. The Flash RAM has one bit associated with each location of the Character RAM. The Flash input is used to select the Flash RAM while address lines A_3-A_4 are ignored. Address lines A_0-A_2 are used to select the location in the Flash RAM to store the attribute. D_0 is used to store or remove the flash attribute. D_0 = "1" stores the attribute and D_0 = "0" removes the attribute.

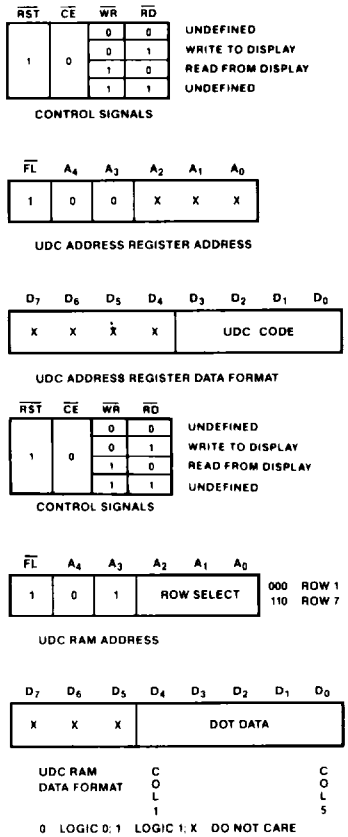


Figure 3. Logic Levels to Access a UDC Character.

COL 1	COL 2	COL 3	COL 4	COL 5		UDC CHARACTER	HEX CODE
D_4	D_3	D_2	D_1	D_0			
1	1	1	1	1	ROW 1	* * * * *	1F
1	0	0	0	0	ROW 2	*	10
1	0	0	0	0	ROW 3	*	10
1	1	1	1	0	ROW 4	* * * *	1D
1	0	0	0	0	ROW 5	*	10
1	0	0	0	0	ROW 6	*	10
1	0	0	0	0	ROW 7	*	10

IGNORED

0 = LOGIC 0; 1 = LOGIC 1; * = ILLUMINATED LED.

Figure 4. Data to Load "F" into the UDC RAM.

When the attribute is enabled through bit 3 of the Control Word and a "1" is stored in the Flash RAM, the corresponding character will flash at approximately 2 Hz. The actual rate is dependent on the clock frequency. For an external clock the flash rate can be calculated by dividing the clock frequency by 28,672.

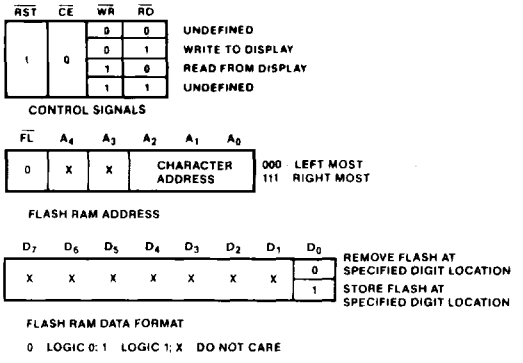


Figure 5. Logic Levels to Access the Flash RAM.

Control Word Register

Figure 6 shows how to access the Control Word Register. This 8-bit register performs five functions: Brightness control, Flash RAM control, Blinking, Self Test, and Clear. Each function is independent of the others; however, all bits are updated during each Control Word write cycle.

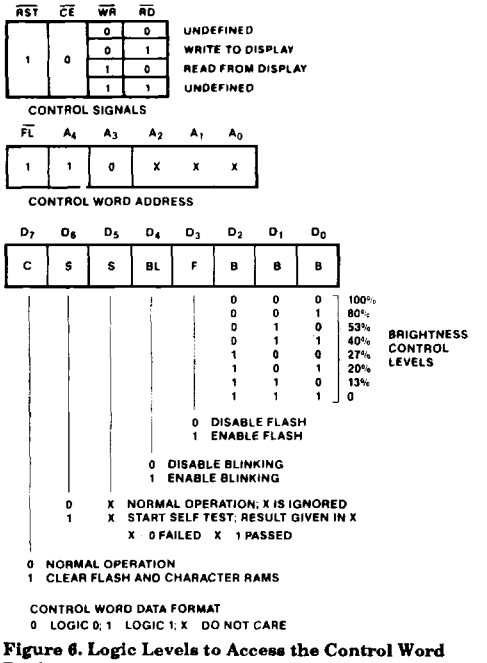


Figure 6. Logic Levels to Access the Control Word Register

Brightness (Bits 0-2)

Bits 0-2 of the Control Word adjust the brightness of the display. Bits 0-2 are interpreted as a three bit binary code with code (000) corresponding to maximum brightness and code (111) corresponding to a blanked display. In addition to varying the display brightness, bits 0-2 also vary the average value of I_{DD}. I_{DD} can be calculated at any brightness level by multiplying the percent brightness level by the value of I_{DD} at the 100% brightness level. These values of I_{DD} are shown in Table 2.

Table 2. Current Requirements at Different Brightness Levels V_{DD} = 5.0 V

Symbol	D_2	D_1	D_0	% Brightness	Current at 25°C Typ.	Units
I_{DD} (V)	0	0	0	100	200	mA
	0	0	1	80	160	mA
	0	1	0	53	106	mA
	0	1	1	40	80	mA
	1	0	0	27	54	mA
	1	0	1	20	40	mA
	1	1	0	13	26	mA

Flash Function (Bit 3)

Bit 3 determines whether the flashing character attribute is on or off. When bit 3 is a "1", the output of the Flash RAM is checked. If the content of a location in the Flash RAM is a "1", the associated digit will flash at approximately 2 Hz. For an external clock, the blink rate can be calculated by driving the clock frequency by 28,672. If the flash enable bit of the Control Word is a "0", the content of the Flash RAM is ignored. To use this function with multiple display systems, see the Display Reset section.

Blink Function (Bit 4)

Bit 4 of the Control Word is used to synchronize blinking of all eight digits of the display. When this bit is a "1" all eight digits of the display will blink at approximately 2 Hz. The actual rate is dependent on the clock frequency. For an external clock, the blink rate can be calculated by dividing the clock frequency by 28,672. This function will override the Flash function when it is active. To use this function with multiple display systems, see the Display Reset section.

Self Test Function (Bits 5, 6)
Bit 6 of the Control Word Register is used to initiate the self test function. Results of the internal self test are stored in bit 5 of the Control Word. Bit 5 is a read only bit where bit 5 = "1" indicates a passed self test and bit 5 = "0" indicates a failed self test.

Setting bit 6 to a logic 1 will start the self test function. The built-in self test function of the IC consists of two internal routines which exercise major portions of the IC and illuminate all of the LEDs. The first routine cycles the ASCII (Katakana) decoder ROM through all states and performs a checksum on the output. If the checksum agrees with the correct value, bit 5 is set to "1". The second routine provides a visual test of the LEDs using the drive circuitry. This is accomplished by writing checkered and inverse checkered patterns to the display. Each pattern is displayed for approximately 2 seconds.

During the self test function the display must not be accessed. The time needed to execute the self test function is calculated by multiplying the clock period by 262,144. For example, assume a clock frequency of 58 KHz, then the time to execute the self test function frequency is equal to (262,144/58,000) = 4.5 second duration.

At the end of the self test function, the Character RAM is loaded with blanks, the Control Word Register is set to zeros except for bit 5, the Flash RAM is cleared, and the UDC Address Register is set to all ones.

Clear Function (Bit 7)
Bit 7 of the Control Word will clear the Character RAM and the Flash RAM. Setting bit 7 to a "1" will start the clear function. Three clock cycles (110 µs minimum using the internal refresh clock) are required to complete the clear function. The display must not be accessed while the display is being cleared. When the clear function has been completed, bit 7 will be reset to a "0". The ASCII (Katakana) character code for a space (20H) will be loaded into the Character RAM to blank the display and the Flash RAM will be loaded with "0"s. The UDC RAM, UDC Address Register, and the remainder of the Control Word are unaffected.

Display Reset

Figure 7 shows the logic levels needed to Reset the display. The display should be Reset on Power-up. The external Reset clears the Character RAM, Flash RAM, Control Word and resets the internal counters. After the rising edge of the Reset signal, three clock cycles (110 µs minimum using the internal refresh clock) are required to complete the reset sequence. The display must not be accessed while the display is being reset. The ASCII (Katakana) Character code for a space (20H) will be loaded into the Character RAM to blank the display. The Flash RAM and Control Word Register are loaded with all "0"s. The UDC RAM and UDC Address Register are unaffected. All displays which operate with the same clock source must be simultaneously reset to synchronize the Flashing and Blinking functions.

$\overline{RST}$	$\overline{CE}$	$\overline{WR}$	$\overline{RD}$	$\overline{FL}$	A_4-A_0	D_7-D_0
0	1	X	X	X	X	X

0 LOGIC 0; 1 LOGIC 1; X DO NOT CARE

NOTE:
IF RST, CE AND WR ARE LOW, UNKNOWN DATA MAY BE WRITTEN INTO THE DISPLAY

Figure 7. Logic Levels to Reset the Display.

Mechanical and Electrical Considerations

The HDSP-211X/-212X/-250X are 28 pin dual-in-line packages with 26 external pins. The devices can be stacked horizontally and vertically to create arrays of any size. The HDSP-211X/212X/250X are designed to operate continuously from -45°C to +85°C with a maximum of 20 dots on per character at 5.25 V. Illuminating all thirty-five dots at full brightness is not recommended.

The HDSP-211X/-212X/250X are assembled by die attaching and wire bonding 280 LED chips and a CMOS IC to a thermally conductive printed circuit board. A polycarbonate lens is placed over the PC board creating an air gap over the LED wire bonds. A protective cap creates an air gap over the CMOS IC. Backfill epoxy environmentally seals the display package. This package construction makes the display highly tolerant to temperature cycling and allows wave soldering.

The inputs to the IC are protected against static discharge and input current latchup. However, for best results standard CMOS handling precautions should be used. Prior to use, the HDSP-211X/-212X/250X should be stored in antistatic tubes or

in conductive material. During assembly, a grounded conductive work area should be used, and assembly personnel should wear conductive wrist straps. Lab coats made of synthetic material should be avoided since they are prone to static buildup. Input current latchup is caused when the CMOS inputs are subjected to either a voltage below ground (V_{IN} < ground) or to a voltage higher than V_{DD} (V_{IN} > V_{DD}) and when a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected either to ground or to V_{DD}. Voltages should not be applied to the inputs until V_{DD} has been applied to the display.

Thermal Considerations

The HDSP-211X/-212X/250X have been designed to provide a low thermal resistance path for the CMOS IC to the 26 package pins. Heat is typically conducted through the traces of the printed circuit board to free air. For most applications no additional heatsinking is required.

Measurements were made on a 32 character display string to determine the thermal resistance of the display assembly. Several display boards were constructed using .062. in. thick printed circuit material, and one ounce copper .020 in. traces. Some of the device pins were connected to a heatsink formed by etching a copper area on the printed circuit board surrounding the display. A maximally metalized printed circuit board was also evaluated. The junction temperature was measured for displays soldered directly to these PC boards, displays installed in sockets, and finally displays installed in sockets with a filter over the display to restrict airflow. The results of these thermal resistance measurements, $R\theta_{J-A}$ are shown in Table 3 and include the effects of $R\theta_{J-C}$.

Ground Connections

Two ground pins are provided to keep the internal IC logic ground clean. The designer can, when necessary, route the analog ground for the LED drivers separately from the logic ground until an appropriate ground plane is available. On long interconnections between the display and the host system, the designer can keep voltage drops on the analog ground from affecting the display logic levels by isolating the two grounds.

The logic ground should be connected to the same ground potential as the logic interface circuitry. The analog ground and the logic ground should be connected at a common ground which can withstand the current introduced by the switching LED drivers. When separate ground connections are used, the analog ground can vary from -0.3 V to +0.3 V with respect to the logic ground. Voltage below -0.3 V can cause all dots to be on. Voltage above +0.3 V can cause dimming and dot mismatch.

Soldering and Post Solder Cleaning Instructions for the HDSP-211X/-212X/-250X

The HDSP-211X/-212X/-250X may be hand soldered or wave soldered with SN63 solder. When hand soldering, it is recommended that an electronically temperature controlled and securely grounded soldering iron be used. For best results, the iron tip temperature should be set at 315°C (600°F). For wave soldering, a rosin-based RMA flux can be used. The solder wave temperature should be set at 245°C ± 5°C (473°F ± 9°F), and the dwell in the wave should be set between 1-1/2 to 3 seconds for optimum soldering. The preheat temperature should not exceed 105°C (221°F) as measured on the solder side of the PC board.

Post solder cleaning may be performed with a solvent or aqueous process. For solvent cleaning, Allied Chemical's Genesolv DES, Baron Blakeslee's Blaco-Tron TES or DuPont's Freon TE may be

Table 3. Thermal Resistance, θ_{JA}, Using Various Amounts of Heatsinking Material

Heatsinking Metal per Device sq. in.	W/Sockets W/O Filter (Avg.)	W/O Sockets W/O Filter (Avg.)	W/Sockets W/Filter (Avg.)	Units
0	31	30	35	°C/W
1	31	28	33	°C/W
3	30	26	33	°C/W
Max. Metal	29	25	32	°C/W
4 Board Avg	30	27	33	°C/W

used. These solvents are azeotropes of trichlorotrifluoroethane FC-113 with low concentrations of ethanol (5%). The maximum exposure time in the solvent vapors at boiling temperature should not exceed 2 minutes. Solvents containing high concentrations of alcohols such as methanol, ketones such as acetone, or chlorinated solvents should not be used as they will chemically attack the polycarbonate lens. Solvents containing trichloroethylene (TCE), FC-111, FC-112, or trichloroethylane (TCA) are also not recommended.

An aqueous cleaning process may be used. A saponifier, such as Kesterbio-kleen Formula 5799 or its equivalent, may be added to the wash cycle of an aqueous process to remove rosin flux residues. Organic acid flux residues must be thoroughly removed by an aqueous cleaning process to prevent corrosion of the leads and solder connections. The optimum water temperature is 60°C (140°F). The maximum cumulative exposure of the HDSP-211X/-212X/-250X to wash and rinse cycles should not exceed 15 minutes. For additional information on soldering and post solder cleaning, see Application Note 1027, *Soldering LED Components.*

Contrast Enhancement

The objective of contrast enhancement is to provide good readability in a variety of ambient lighting conditions. For information on contrast enhancement see Application Note 1015, *Contrast Enhancement Techniques for LED Displays.*