Solutions PDF Generated from: solutions-openai-generated/labs/lab-02-solutions-set-03.json

Question A

Fill out the truth table, which describes the operation of a full adder. We use the inputs A, B, CI and the outputs are called S and CO.

A	B	CI	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Question B

Derive the Boolean equations for both outputs of a full adder. Apply logic minimization techniques to come up with a simplified full adder circuit.

```
Boolean equations:

Output Sum (S) =   ABCin

Output Carry (Cout) = AB + ACin + BCin

Simplified full adder circuit:

S =  ABCin

Cout = A+B(Cin)
```

Question C

Draw the schematic of the full adder circuit according to the equations you have derived.

```
![Full Adder Circuit](./full_adder.jpg)
```

Question D

Generate full adder Verilog code for outputs co (carry out) and s (sum)

```
module full_adder(a, b, c_in, s, c_out);

   input a;
   input b;
   input c_in;

   output s;
   output c_out;

   wire t1, t2, t3;

   xor (t1, a, b);      // t1 = a xor b
   and (t2, a, b);      // t2 = a and b
   xor (s, t1, c_in);   // s = t1 xor c_in
   and (t3, t1, c_in);  // t3 = t1 and c_in
   or  (c_out, t2, t3); // c_out = t2 or t3

endmodule
```

Execution Time

0:00:32.162663

OpenAI Parameters

Model: text-davinci-003, Max. Tokens: 1024, Temperature: 1, N: 1