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Question A

Fill out the truth table, which describes the operation of a full adder. We use the inputs A, B, CI and the outputs are called S and CO.

A	B	CI	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Question B

Derive the Boolean equations for both outputs of a full adder. Apply logic minimization techniques to come up with a simplified full adder circuit.

```
Answer:
Boolean equations for A and B outputs of a full adder are:
A= Cin XOR AIN XOR BIN
B= Cout = AIN AND BIN OR Cin AND (AIN XOR BIN)

Logic minimization technique:
A= Cin XOR AIN XOR BIN
B = AIN AND BIN OR Cin (AIN XOR BIN) // simplified equation

Simplified full adder circuit:

A = AIN XOR BIN
B = AIN XOR Cin (AIN XOR BIN)
```

Question C

Draw the schematic of the full adder circuit according to the equations you have derived.

```
The full adder circuit is given in the following diagram:

[Full Adder Circuit diagram]
```

Question D

Generate full adder Verilog code for outputs co (carry out) and s (sum)

```
module full_adder( input a,
                   input b,
                   input cin,
                   output co,
                   output s);
    wire t1, t2;

    // Half adders
    xor (s, a, b);
    and (t1, a , b);

    // Full Adder
    xor (t2, s, cin);
    or (co, t1, t2);

endmodule
```

Execution Time

0:00:30.761409

OpenAI Parameters

Model: text-davinci-003, Max. Tokens: 1024, Temperature: 1, N: 1