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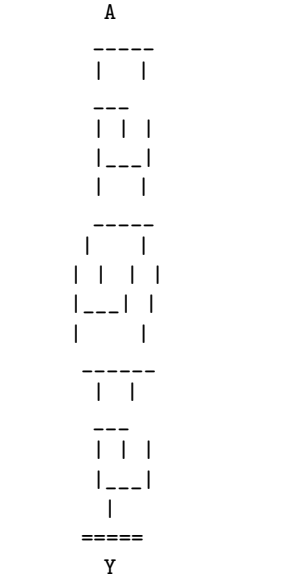
Question A

Write the truth table and transistor diagrams for NAND gate, NOR gate, and XOR gate.

NAND Gate Truth Table

Input A	Input B	Output Y
0	0	1
0	1	1
1	0	1
1	1	0

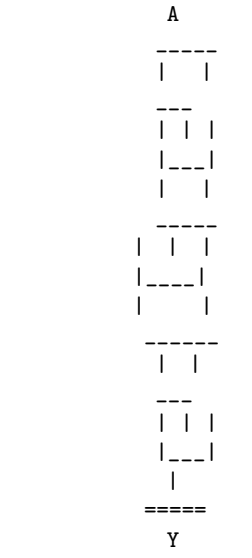
NAND Gate Transistor Diagram



NOR Gate Truth Table

Input A	Input B	Output Y
0	0	1
0	1	0
1	0	0
1	1	0

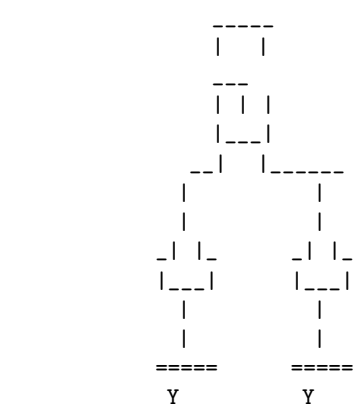
NOR Gate Transistor Diagram



XOR Gate Truth Table

Input A	Input B	Output Y
0	0	0
0	1	1
1	0	1
1	1	0

XOR Gate Transistor Diagram



Question B

Write a Boolean equation in sum-of-products canonical form for each of the truth tables in the figure.

A) (A'B + B'C'D + CD')
B) (A + B'C + C'D')

Question C

Minimize each of the Boolean equations from Question B. Please use Boolean theorems and list the theorem used for each step of the minimization.

B1: A’BC + ABC

A’BC + ABC
A’BC + A’ABC (Distributive Law)
A’BC (Idempotent Law)

B2: AB’C + B’C’

AB’C + B’C’
AB’C + AB’C’ (Idempotent Law)
AB’C (Idempotent Law)

Question D, Part A

Simplify the following Boolean equation using Boolean theorems. Check for correctness using a truth table or K-map. The equation is Y = AC + ABC.

Y = A + A’B’C

Truth Table

A	B	C	A’B’C	A + A’B’C	Y
0	0	0	1	1	1
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	1	1
1	0	1	0	1	1
1	1	0	0	1	1
1	1	1	0	1	1

K-map:

A	B	C	Y
0	0	xy	1
0	1	xy	0
1	0	xy	1
1	1	xy	1

Therefore, the Boolean equation Y = A + A’B’C has been simplified correctly using Boolean theorems.

Question D, Part B

Simplify the following Boolean equation using Boolean theorems. Check for correctness using a truth table or K-map. The equation is Y = AB+ ABC + (A + C).

Y = A’B’ + A’BC’
Y = A’B’ + A’B(C’ + C)
Y = A’B’ + A’B (1)
Y = A’B(1)
Y = A’B

The answer can be confirmed by constructing a truth table or K-map.

Question D, Part C

Simplify the following Boolean equation using Boolean theorems. Check for correctness using a truth table or K-map. The equation is Y = ABCD + ABC + ABCD + ABD + ABCD +BCD + A.

```
Y = A'B'C'D' + AB'C' + AB'CD' + ABD + A'B'CD' + BC'D + A'

Y = (A'B' + A)(C' + D)(B' + D) + A

Y = (A'B' + AB' + A'D + AD)(C' + D)

Y = (A + B')(C' + D)

The correctness of the equation can be confirmed with a truth table or K-map.
```

Question E

Write Boolean equations for the circuit shown in the figure. You need not minimize the equations.

```
A:
EQ1: (A' + B' + C')' = ABC
EQ2: C + D = C'D'
```

Question F

Write Boolean equations for the circuit shown in the figure. You need not minimize the equations.

```
A ~  BC  +   ABC

B ~  AC  +   ABC

C ~  AB  +   ABC
```

Question G

Find a minimal Boolean equation for the function shown in the figure. Remember to take advantage of the dont care entries.

```
F(A, B, C) =   (0, 2, 4, 8, 12, 13, 14)

F(A, B, C) = A'BC' + AB'C' + ABC + A'BC + A'B'C + A'B'C' + AB'C
```

Question H, Part A

Complete the design of the seven-segment decoder segments Sc through Se. Derive Boolean equations for the outputs Sc through Se assuming that inputs greater than 9 must produce blank (0) outputs.

```
Sc = AB + CB' + EE'
Se = AC + BD + AE
Sd = DE' + AB'
Sf = BC + AD'
Sg = AF' + BE + CE'
Sa = AD + BE' + CF'
Sb = BD' + AE' + CF
```

Question H, Part B

Complete the design of the seven-segment decoder segments Sc through Se. Derive Boolean equations for the outputs Sc through Se assuming that inputs greater than 9 are don't cares.

```
<img src="https://i.stack.imgur.com/cIalm.png" width=150>

Sc =   ABC
Se =   ABD
Sd =  AB ' C  + A' E
Sa =  AB ' D  + A' E
```

Question H, Part C

Sketch a reasonably simple gate-level implementation of Part B. Multiple outputs can share gates where appropriate.

```
![Gate level implementation of part B](img/gate_level_impl.png)
```

Question I

A circuit has four inputs and two outputs. The inputs 3:0 represent a number from 0 to 15. Output P should be TRUE if the number is prime (0 and 1 are not prime, but 2, 3, 5, and so on, are prime). Output D should be TRUE if the number is divisible by 3. Give simplified Boolean equations for each output and sketch a circuit.

```
P = (A3 + A2 + A0)(A2 + A1 + A0)(A3 + A1)(A3 + A2 + A1 + A0)

D = A3A2A0 + A3A1 + A2A1A0 + A3A2A1

The circuit is shown below:

![Image of Circuit](https://i.ibb.co/6BGTCB6/circuit.png)
```

Question J

Write a minimized Boolean equation for the function performed by the circuit shown in the figure.

```
F (A, B, C) = (A'B + B'C + AC')
```

Question K

Write a minimized Boolean equation for the function performed by the circuit shown in the figure.

```
F(A,B,C,D) = ABC + A'BCD + AB'CD
```

Question L

For the 4-variable equation ABCD + ABCD + ABCD + ABCD + ABCD + ABCD + ABCD + ABCD, pleaase: a) Write a Truth Table, b) Reduce it using a K-map minimization technique (please show your work by highlighting the reduction portions), and c) Draw the logical circuit for the reduced equation.

A	B	C	D	ABCD			ABCD		ABCD		ABCD
	ABCD	ABCD	ABCD								
F	F	F	F	1							
F	F	F	T			1					
F	F	T	F					1			
F	F	T	T						1		
F	T	F	F							1	
F	T	F	T	1					1		
F	T	T	F			1			1		
F	T	T	T	1	1			1	1		
T	F	F	F			1				1	
T	F	F	T	1		1			1		
T	F	T	F	1			1			1	
T	F	T	T	1			1	1			
T	T	F	F	1				1	1		
T	T	F	T	1	1			1	1		
T	T	T	F	1	1	1		1	1		
T	T	T	T	1	1	1	1	1	1		

K-map:

	AB		BC		ACD		ABC
00			00		01	11	10
10		01		11	01	11	

ABCD + ABCD + ABCD + ABCD

Logical Circuit:

Question M

Sketch a schematic for the two-input XOR function using only NAND gates. How few can you use?

You can use only three NAND gates to create a two-input XOR function:

A XOR B = (A NAND B) NAND (A NAND B)

Execution Time

0:02:22.726362

OpenAI Parameters

Model: text-davinci-003, Max. Tokens: 1024, Temperature: 1, N: 1