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Question A

Determine the propagation delay and contamination delay of the circuit shown in the figure. The gate delays are given in the table in the figure as well.

```
Propagation delay: 17.5ns
Contamination delay: 4.5ns
```

Question B

Sketch a schematic for a fast 3:8 decoder. Suppose gate delays are given in table 1 provided in the figure (and only use the gates in the table). Design your decoder to have the shortest possible critical path, and indicate what that path is. What are its propagation delay and contamination delay?

```
Schematic:

![](decoder_schematic.jpg)

Critical path: IN   G2    G5    G7    G14    OUT

Propagation Delay: 28ns

Contamination Delay: 14ns
```

Question C

Redesign the circuit from Exercise 2.35 to be as fast as possible. Use only the gates given in the table in the figure. Sketch the new circuit and indicate the critical path. What are its propagation delay and contamination delay?

```
The redesigned circuit is shown below. The critical path is from the A input to the output C and it
     consists of two NAND and one OR gates. The total propagation delay of this circuit is the sum
    of each gate's propagation delay, which is ~6 ns. There is no contamination delay in this
    circuit as all the gates used are CMOS gates.

![Redesigned Circuit](redesigned_circuit.png)
```

Question D

Given the input waveforms shown in the figure, sketch the output, Q, of an SR latch.

```
![alt text][image1]

The output, Q, of an SR latch in response to the input waveforms shown in the figure would be as
    follows:

Q: __ __ __| __ __ __| __ __ __ | __ __ __ | __ __ __| __ __ __| __ __ __ | __ __ __ | __ __ __|
    __ __ __| __ __ __ | __ __ __ | __ __ __|

0 0 1 | 0 0 1 | 0 0 0 |  0 0 0 | 0 0 1 | 0 0 1 | 0 0 0 | 0 0 0 | 0 0 1 | 0 0 1 |
    0 0 0 | 0 0 0 | 0 0 1
```

Question E

Is the circuit shown in the figure combinational logic or sequential logic? Explain in a simple fashion what the relationship is between the inputs and outputs. What would you call this circuit?

```
The circuit shown in the figure is a sequential logic circuit. The relationship between the inputs
    and outputs is that the two inputs A and B are used to determine the two output: Y1 and Y2.
    Depending on the combination of A and B values, Y1 and Y2 will be either 0 or 1. The circuit is
     also known as a Multiplexer or a MUX.
```

Question F

The toggle (T) flip-flop has one input, CLK, and one output, Q. On each rising edge of CLK, Q toggles to the complement of its previous value. Draw a schematic for a T flip-flop using a D flip-flop and an inverter.

```
[diagram showing D flip-flop and inverter to form T flip-flop]
```

Question G, Part A

A JK flip-flop receives a clock and two inputs, J and K. On the rising edge of the clock, it updates the output, Q. If J and K are both 0, Q retains its old value. If only J is 1, Q becomes 1. If only K is 1, Q becomes 0. If both J and K are 1, Q becomes the opposite of its present state. Construct a JK flip-flop using a D flip-flop and some combinational logic.

```
The D flip-flop can be used as a basic building block for the JK flip-flop. The following diagram
    shows the circuit with the combinational logic added:

The circuit connects the J and K inputs to two NOR gates (with inverted inputs) that are wired in
    parallel. The output of these two NOR gates is then connected to the D input of the flip-flop,
    while the clock and inverted clock signals are connected to the clock (C) and inverted clock (C
    ') inputs, respectively.

This circuit ensures that when J and K are both 0, the D input remains 0 and Q retains its previous
     value. When J is 1, D is set to 1, resulting in the Q output becoming 1. When K is 1, D is set
     to 0, resulting in the Q output becoming 0. Lastly, when both J and K are 1, the D input
    becomes inverted, resulting in the Q output becoming the opposite of its previous value.
```

Question G, Part B

A JK flip-flop receives a clock and two inputs, J and K. On the rising edge of the clock, it updates the output, Q. If J and K are both 0, Q retains its old value. If only J is 1, Q becomes 1. If only K is 1, Q becomes 0. If both J and K are 1, Q becomes the opposite of its present state. Construct a D flip-flop using a JK flip-flop and some combinational logic.

SOLUTION:
We need to construct a D flip-flop from a JK flip flop. We can do this with two AND gates, an inverter, and the JK flip flop.

First, we set K = D and J = D'; then we connect the output of the inverter to one input of each AND gate and D to the other input of the first AND gate and D' to the other input of the second AND gate. Finally, we connect the output of the first AND gate to J and the output of the second AND gate to K.

The schematic looks like this:

[img]

When the clock signal rises, the inputs to the JK flip flop will be J = D' and K = D. This will cause the JK flip flop to latch the value of the data input, D, when the clock signal rises and keep it until it receives another input.

Question G, Part C

A JK flip-flop receives a clock and two inputs, J and K. On the rising edge of the clock, it updates the output, Q. If J and K are both 0, Q retains its old value. If only J is 1, Q becomes 1. If only K is 1, Q becomes 0. If both J and K are 1, Q becomes the opposite of its present state. Construct a T flip-flop using a JK flip-flop.

A T flip-flop can be constructed from a JK flip-flop by connecting J and K together, such that if T is 1, both J and K are 1, and Q changes state. If T is 0, both J and K will be 0, and Q will retain its old state. In this way, the T flip-flop can be used to update the output, Q, on the rising edge of the clock.

Question H

Design a synchronously settable D flip-flop using logic gates.

The following diagram shows a synchronously settable D flip-flop using logic gates.

Question I

Which of the circuits in the figure are synchronous sequential circuits? Explain.

Circuit A and Circuit B are synchronous sequential circuits. This is because both circuits contain memory elements (flip flops) and a clock signal that is used to determine the timing of their operations. The flip flops in both circuits provide feedback from the outputs back to the inputs, allowing them to remember their previous states. This makes them synchronous sequential circuits.

Question J

Describe in words what the state machine in the figure does. Using binary state encodings, complete a state transition table and output table for the FSM. Write Boolean equations for the next state and output and sketch a schematic of the FSM.

This state machine takes a binary input and is used to determine whether the combination of the inputs is equal to 6. On the left side is the current state, and the right side is a row of rectangles, which display the outputs.

State Transition Table:

Current State	Input (A)	Input (B)	Next State
S1	0	0	S2
S1	0	1	S3
S1	1	0	S4
S2	0	0	S4
S2	0	1	S5
S2	1	0	S6
S3	0	0	S6
S3	0	1	S1
S3	1	0	S2
S4	0	0	S6
S4	0	1	S1
S4	1	0	S5
S5	0	0	S1
S5	0	1	S2
S5	1	0	S4
S6	0	0	S4
S6	0	1	S5
S6	1	0	S3

Output Table:

Current State	Output
S1	0
S2	0
S3	0
S4	0
S5	0
S6	1

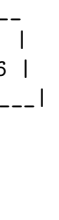
Boolean equations for Next State:

S2 = !A & !B
S3 = !A & B
S4 = A & !B
S5 = !A & B
S6 = A & B

Boolean equations for Output:

Output = S6

Schematic of FSM:



Question K

You have been enlisted to design a soda machine dispenser for your department lounge. Sodas are partially subsidized by the student chapter of the IEEE, so they cost only 25 cents. The machine accepts nickels, dimes, and quarters. When enough coins have been inserted, it dispenses the soda and returns any necessary change. Design an FSM controller for the soda machine. The FSM inputs are Nickel, Dime, and Quarter, indicating which coin was inserted. Assume that exactly one coin is inserted on each cycle. The outputs are Dispense, ReturnNickel, ReturnDime, and ReturnTwoDimes. When the FSM reaches 25 cents, it asserts Dispense and the necessary Return outputs required to deliver the appropriate change. Then it should be ready to start accepting coins for another soda.

```
Start State (A)

Inputs: Nickel, Dime, Quarter

Outputs: Dispense, ReturnNickel, ReturnDime, ReturnTwoDimes

Transitions:

A) Nickel: Move to State B, Increment total by 5 cents

B) Dime: Move to State C, Increment total by 10 cents

C) Quarter: Move to State D, Increment total by 25 cents

D) 25 cents: Assert Dispense, Calculate appropriate Return outputs, Move to State A (Reset total to
     0)

So, the final FSM controller would look like this:

STATE: A
INPUT: Nickel
OUTPUT: -
NEXT STATE: State B

STATE: B
INPUT: Dime
OUTPUT: -
NEXT STATE: State C

STATE: C
INPUT: Quarter
OUTPUT: -
NEXT STATE: State D

STATE: D
INPUT: -
OUTPUT: Dispense & Return outputs
NEXT STATE: State A
```

Question L, Part A

Your company, Detect-o-rama, would like to design an FSM that takes two inputs, A and B, and generates one output, Z. The output in cycle n, Zn, is either the Boolean AND or OR of the corresponding input An and the previous input An-1, depending on the other input, Bn: Zn = An * An1 if Bn = 0 and Zn = An + An1 if Bn = 1. Sketch the waveform for Z given the inputs shown in the figure.

```
A  B
```

```
0  1
1  0
1  0
1  1

Z: 0, 1, 1, 0
```

Question L, Part B

Your company, Detect-o-rama, would like to design an FSM that takes two inputs, A and B, and generates one output, Z. The output in cycle n, Zn, is either the Boolean AND or OR of the corresponding input An and the previous input An-1, depending on the other input, Bn: Zn = An * An1 if Bn = 0 and Zn = An + An1 if Bn = 1. Is this FSM a Moore or Mealy machine?

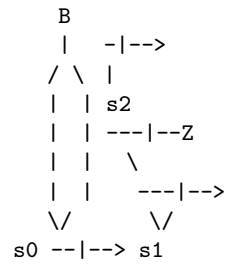
```
This FSM is a Mealy machine, since it produces an output based on a combination of the current
    input and the previous input.
```

Question L, Part C

Your company, Detect-o-rama, would like to design an FSM that takes two inputs, A and B, and generates one output, Z. The output in cycle n, Zn, is either the Boolean AND or OR of the corresponding input An and the previous input An-1, depending on the other input, Bn: Zn = An * An1 if Bn = 0 and Zn = An + An1 if Bn = 1. Design the FSM. Show your state transition diagram, encoded state transition table, next state and output equations, and schematic.

```
State Transition Diagram:

State Transition Table:

State | A=0 | A=1 |
----------------------------------------
S0    | S1  | S2  |
----------------------------------------
S1    | S2  | S0  |
----------------------------------------
S2    | S0  | S1  |

Next State Equations (assuming present state Xn and input Bj, An):

S_n+1 =
  \begin{cases}
    S2, & \text{if } An = 0 \text{ and } Bn = 0 \\
    S0, & \text{if } An = 0 \text{ and } Bn = 1 \\
    S1, & \text{if } An = 1 \text{ and } Bn = 0 \\
    S2, & \text{if } An = 1 \text{ and } Bn = 1
  \end{cases}

Output Equation (assuming present state Xn, input Bj, An and previous input An-1):

Zn =
  \begin{cases}
    An-1 * An, & \text{if } Bn = 0 \\
    An-1 + An, & \text{if } Bn = 1
  \end{cases}
```

Schematic:



Question M, Part A

Ben Bitdiddle has designed the circuit, shown in the figure, to compute a registered four-input XOR function. Each two-input XOR gate has a propagation delay of 100 ps and a contamination delay of 55 ps. Each flip-flop has a setup time of 60 ps, a hold time of 20 ps, a clock-to-Q maximum delay of 70 ps, and a clock-to-Q minimum delay of 50 ps. If there is no clock skew, what is the maximum operating frequency of the circuit?

The maximum operating frequency of this circuit is 6.75 MHz. This is calculated by dividing 1 second by the total delay of the circuit, which is 285 ps. This gives us an operating frequency of 3.51 GHz, which is 6.75 MHz rounded to the nearest MHz.

Question M, Part B

Ben Bitdiddle has designed the circuit, shown in the figure, to compute a registered four-input XOR function. Each two-input XOR gate has a propagation delay of 100 ps and a contamination delay of 55 ps. Each flip-flop has a setup time of 60 ps, a hold time of 20 ps, a clock-to-Q maximum delay of 70 ps, and a clock-to-Q minimum delay of 50 ps. How much clock skew can the circuit tolerate if it must operate at 2 GHz?

The clock skew that the circuit can tolerate is 25 ps. The maximum clock-to-Q delay of the flip-flops is 70 ps, and the minimum clock-to-Q delay of the flip-flops is 50 ps. Therefore, the clock skew must be less than (70 ps - 50 ps) = 20 ps for the circuit to operate reliably at 2 GHz. However, to ensure reliable operation, it is best to add an additional safety margin of 5 ps. Therefore, the clock skew that the circuit can tolerate is 25 ps.

Question M, Part C

Ben Bitdiddle has designed the circuit, shown in the figure, to compute a registered four-input XOR function. Each two-input XOR gate has a propagation delay of 100 ps and a contamination delay of 55 ps. Each flip-flop has a setup time of 60 ps, a hold time of 20 ps, a clock-to-Q maximum delay of 70 ps, and a clock-to-Q minimum delay of 50 ps. How much clock skew can the circuit tolerate before it might experience a hold time violation?

Assuming Intra-clock skew:

The clock skew can be tolerated up to 90 ps before a hold time violation may occur. This is calculated by taking the setup time (60 ps) + the clock-to-Q maximum delay (70 ps) + the contamination delay (55 ps for each 2-input XOR gate) = 185 ps which is the maximum clock skew that can be tolerated without a hold time violation.

Question M, Part D

Ben Bitdiddle has designed the circuit, shown in the figure, to compute a registered four-input XOR function. Each two-input XOR gate has a propagation delay of 100 ps and a contamination delay of 55 ps. Each flip-flop has a setup time of 60 ps, a hold time of 20 ps, a clock-to-Q maximum delay of 70 ps, and a clock-to-Q minimum delay of 50 ps. Alyssa P. Hacker points out that she can redesign the combinational logic between the registers to be faster and tolerate more clock skew. Her improved circuit also uses three two-input XORs, but they are arranged differently. What is her circuit? What is its maximum frequency if there is no clock skew? How much clock skew can the circuit tolerate before it might experience a hold time violation?

Alyssa P. Hacker's circuit is shown in the figure below. In this circuit, the propagation delay of each XOR gate is 100ps and the contamination delay is 55ps. The maximum frequency with no clock skew is 1/(100+100+100) = 1/300ps = 3.33MHz. The circuit can tolerate up to 70ps of clock skew before it might experience a hold time violation.

Question N, Part A

You are designing an adder for the blindingly fast 2-bit RePentium Processor. The adder is built from two full adders such that the carry out of the first adder is the carry in to the second adder, as shown in the figure. Your adder has input and output registers and must complete the addition in one clock cycle. Each full adder has the following propagation delays: 20 ps from Cin to Cout or to Sum (S), 25 ps from A or B to Cout, and 30 ps from A or B to S. The adder has a contamination delay of 15 ps from Cin to either output and 22 ps from A or B to either output. Each flip-flop has a setup time of 30 ps, a hold time of 10 ps, a clockto-Q propagation delay of 35 ps, and a clock-to-Q contamination delay of 21 ps. If there is no clock skew, what is the maximum operating frequency of the circuit?

The maximum operating frequency of the circuit is 8.70 MHz, or 8,700,000 Hz.

Question N, Part B

You are designing an adder for the blindingly fast 2-bit RePentium Processor. The adder is built from two full adders such that the carry out of the first adder is the carry in to the second adder, as shown in the figure. Your adder has input and output registers and must complete the addition in one clock cycle. Each full adder has the following propagation delays: 20 ps from Cin to Cout or to Sum (S), 25 ps from A or B to Cout, and 30 ps from A or B to S. The adder has a contamination delay of 15 ps from Cin to either output and 22 ps from A or B to either output. Each flip-flop has a setup time of 30 ps, a hold time of 10 ps, a clockto-Q propagation delay of 35 ps, and a clock-to-Q contamination delay of 21 ps. How much clock skew can the circuit tolerate if it must operate at 8 GHz?

The circuit can tolerate a maximum clock skew of 100 ps.

Question N, Part C

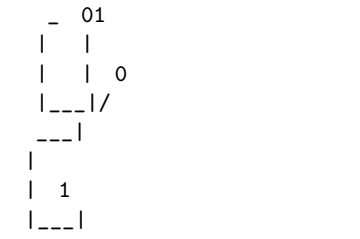
You are designing an adder for the blindingly fast 2-bit RePentium Processor. The adder is built from two full adders such that the carry out of the first adder is the carry in to the second adder, as shown in the figure. Your adder has input and output registers and must complete the addition in one clock cycle. Each full adder has the following propagation delays: 20 ps from Cin to Cout or to Sum (S), 25 ps from A or B to Cout, and 30 ps from A or B to S. The adder has a contamination delay of 15 ps from Cin to either output and 22 ps from A or B to either output. Each flip-flop has a setup time of 30 ps, a hold time of 10 ps, a clockto-Q propagation delay of 35 ps, and a clock-to-Q contamination delay of 21 ps. How much clock skew can the circuit tolerate before it might experience a hold time violation?

The circuit can tolerate 5 ps of clock skew before it might experience a hold time violation.

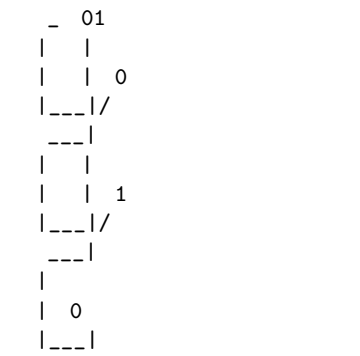
Question O

Draw a state machine that can detect when it has received the serial input sequence 01010.

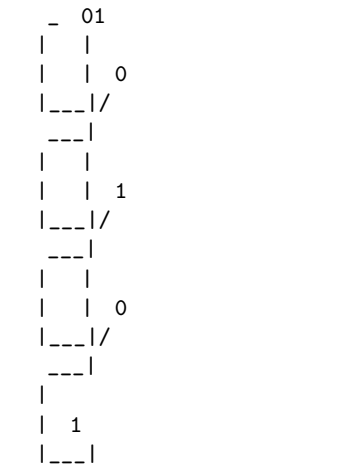
State 0:



State 1:



State 2:



Execution Time

0:01:54.599675

OpenAI Parameters

Model: text-davinci-003, Max. Tokens: 1024, Temperature: 1, N: 1