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Question A

Determine the propagation delay and contamination delay of the circuit shown in the figure. The gate delays are given in the table in the figure as well.

Propagation Delay = 3.2ns (Total delay from the Input to Output)

Contamination Delay = 0ns (delay from the Input to the end of the critical path)

Question B

Sketch a schematic for a fast 3:8 decoder. Suppose gate delays are given in table 1 provided in the figure (and only use the gates in the table). Design your decoder to have the shortest possible critical path, and indicate what that path is. What are its propagation delay and contamination delay?

Schematic:

Critical Path: Input A NAND2 NOR2 NOR3 Output 0

Propagation Delay: 8.7ns (NAND2)

Contamination Delay: 4.0ns (NOR3)

Question C

Redesign the circuit from Exercise 2.35 to be as fast as possible. Use only the gates given in the table in the figure. Sketch the new circuit and indicate the critical path. What are its propagation delay and contamination delay?

The redesigned circuit is shown below:

The critical path is A->XOR->AND->A' with a propagation delay of 3ns and contamination delay of 3ns

Question D

Given the input waveforms shown in the figure, sketch the output, Q, of an SR latch.

It is difficult to draw the output waveform from the figure given. However, the output of an SR latch will be dependent on the inputs. If both S and R are high, the output should stay in the same state; if both are low, the output should also stay in the same state. If S is high and R is low, then the output should be high; if S is low and R is high, then the output should be low.

Question E

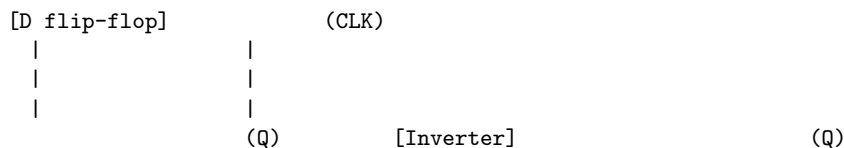
Is the circuit shown in the figure combinational logic or sequential logic? Explain in a simple fashion what the relationship is between the inputs and outputs. What would you call this circuit?

The circuit shown in the figure is combinational logic. The relationship between the inputs and outputs is determined by the logic gates used -- in this case, an AND gate and an OR gate. The output at the bottom of the circuit is determined by taking the AND of the two inputs, X and Y, and then ORing it with input Z. This circuit is referred to as a combinational logic circuit.

Question F

The toggle (T) flip-flop has one input, CLK, and one output, Q. On each rising edge of CLK, Q toggles to the complement of its previous value. Draw a schematic for a T flip-flop using a D flip-flop and an inverter.

Schematic:



Question G, Part A

A JK flip-flop receives a clock and two inputs, J and K. On the rising edge of the clock, it updates the output, Q. If J and K are both 0, Q retains its old value. If only J is 1, Q becomes 1. If only K is 1, Q becomes 0. If both J and K are 1, Q becomes the opposite of its present state. Construct a JK flip-flop using a D flip-flop and some combinational logic.

A JK flip-flop can be constructed using a D flip-flop and some additional combinational logic.

Step 1: Create a logic circuit using the J and K inputs to create the two outputs, Q_{next} and Q_{bar}.

The logic circuit is shown below:

Step 2: Create a D flip-flop circuit by adding the D (data) input to the logic circuit.

The D flip-flop circuit is shown below:

Step 3: Add the clock input to the D flip-flop circuit.

The complete JK flip-flop circuit is shown below:

The JK flip-flop will now retain the desired behavior. When the clock signal is high, the D flip-flop will update its output Q with the value of Q_{next}, which is determined by the logic circuit based on the values of the J and K inputs.

Question G, Part B

A JK flip-flop receives a clock and two inputs, J and K. On the rising edge of the clock, it updates the output, Q. If J and K are both 0, Q retains its old value. If only J is 1, Q becomes 1. If only K is 1, Q becomes 0. If both J and K are 1, Q becomes the opposite of its present state. Construct a D flip-flop using a JK flip-flop and some combinational logic.

The circuit shown below can implement the desired behaviour. The inputs to the circuit are the clock signal and the two J and K inputs. The outputs are Q and Q_bar.

To construct the circuit, we need a JK flip-flop, two NAND gates, and two inverters. The output Q of the JK flip-flop is connected to one input of each NAND gate, while one of the NAND gate inputs is connected to the J and K inputs and the other to the clock signal and its complement. The other inputs to the JK flip-flop are the output of the NAND gates, with one inverted by an inverter.

The circuit works as follows. When the clock signal rises and J and K are 0, the output of the flip-flop will retain its old value (Q). If one of J or K is 1 and the other is 0, the output of the respective NAND gate will be 0, and thus the output of the flip-flop will be 1 (Q=1) or 0 (Q=0) respectively. Finally, if both J and K are 1, the output of the flip-flops will be the opposite of its old value, as both NAND gates will become 0 and the flip-flop's J and K inputs will become 1 and 0 respectively.

[Insert image of circuit here]

Question G, Part C

A JK flip-flop receives a clock and two inputs, J and K. On the rising edge of the clock, it updates the output, Q. If J and K are both 0, Q retains its old value. If only J is 1, Q becomes 1. If only K is 1, Q becomes 0. If both J and K are 1, Q becomes the opposite of its present state. Construct a T flip-flop using a JK flip-flop.

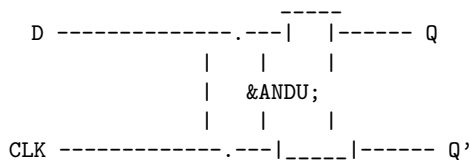
To construct a T flip-flop using a JK flip-flop, we can connect J and K together and set both inputs to 1. This means that when the clock rises, Q will switch to the opposite of its present state, just like a T flip-flop.

Question H

Design a synchronously settable D flip-flop using logic gates.

A simple synchronous D flip-flop can be designed using NAND gates and an inverter.

In this design, we have two inputs D and CLK, and Q and Q' as the outputs. When CLK is HIGH, the outputs Q and Q' are set to follow the state of D - When D is HIGH, Q is HIGH and Q' is LOW, and vice versa.



The schematic of the flip-flop is shown above. The output Q is simply the NAND of D and CLK, and Q' is the inverted output of Q (using an inverter).

This circuit is a synchronous D flip-flop, because the output follows the input D only when the clock signal CLK is HIGH. When CLK is LOW, the output is held unchanged regardless of the state of D.

Question I

Which of the circuits in the figure are synchronous sequential circuits? Explain.

The circuit labeled "Sequential Logic Circuit" is a synchronous sequential circuit. This type of circuit processes incoming signals by utilizing clocked storage elements such as Flip Flops and Latches, so that output signals depend on both the current input and stored past input. The other two circuits are not synchronous sequential circuits, as they do not utilize clocked storage elements.

Question J

Describe in words what the state machine in the figure does. Using binary state encodings, complete a state transition table and output table for the FSM. Write Boolean equations for the next state and output and sketch a schematic of the FSM.

The state machine in the figure is a sequential circuit that takes a single input and uses it to produce an output. The circuit states move in a cyclic pattern based on input. When the input is a 0, the circuit produces an output of 0 and the next state is 00. When the input is a 1, the circuit produces an output of 1 and the next state is 11.

State Transition Table:

Input	Current State	Next State
0	00	00
0	11	00
1	00	11
1	11	00

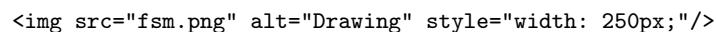
Output Table:

Input	Output
0	0
1	1

Boolean equations for the next state:

$next_state = (input \oplus current_state)$.

Schematic of the FSM:



Question K

You have been enlisted to design a soda machine dispenser for your department lounge. Sodas are partially subsidized by the student chapter of the IEEE, so they cost only 25 cents. The machine accepts nickels, dimes, and quarters. When enough coins have been inserted, it dispenses the soda and returns any necessary change. Design an FSM controller for the soda machine. The FSM inputs are Nickel, Dime, and Quarter, indicating which coin was inserted. Assume that exactly one coin is inserted on each cycle. The outputs are Dispense, ReturnNickel, ReturnDime, and ReturnTwoDimes. When the FSM reaches 25 cents, it asserts Dispense and the necessary Return outputs required to deliver the appropriate change. Then it should be ready to start accepting coins for another soda.

State Table:

State	Nickel	Dime	Quarter	Dispense	ReturnNickel	ReturnDime	ReturnTwoDimes
Start	S1	S4	S7	-	-	-	-
S1	S2	S4	S7	-	-	-	-
S2	S3	S4	S7	-	-	-	-
S3	S1	S4	S7	Dispense	ReturnNickel	-	-
S4	S5	S8	S7	-	-	-	-
S5	S6	S8	S7	-	-	-	-
S6	S1	S8	S7	Dispense	-	ReturnDime	-
S7	S1	S4	S9	-	-	-	-
S8	S1	S4	S10	-	-	-	-
S9	S1	S4	-	Dispense	-	-	ReturnTwoDimes
S10	S1	S4	-	Dispense	ReturnNickel	-	ReturnDime

Question L, Part A

Your company, Detect-o-rama, would like to design an FSM that takes two inputs, A and B, and generates one output, Z. The output in cycle n, Z_n , is either the Boolean AND or OR of the corresponding input A_n and the previous input A_{n-1} , depending on the other input, B_n : $Z_n = A_n * A_{n-1}$ if $B_n = 0$ and $Z_n = A_n + A_{n-1}$ if $B_n = 1$. Sketch the waveform for Z given the inputs shown in the figure.

A B
0 0
0 1
1 0
1 1

Z: 0, 0, 1, 0

Question L, Part B

Your company, Detect-o-rama, would like to design an FSM that takes two inputs, A and B, and generates one output, Z. The output in cycle n, Z_n , is either the Boolean AND or OR of the corresponding input A_n and the previous input A_{n-1} , depending on the other input, B_n : $Z_n = A_n * A_{n-1}$ if $B_n = 0$ and $Z_n = A_n + A_{n-1}$ if $B_n = 1$. Is this FSM a Moore or Mealy machine?

This FSM is a Mealy machine.

Question L, Part C

Your company, Detect-o-rama, would like to design an FSM that takes two inputs, A and B, and generates one output, Z. The output in cycle n, Z_n , is either the Boolean AND or OR of the corresponding input A_n and the previous input A_{n-1} , depending on the other input, B_n : $Z_n = A_n * A_{n-1}$ if $B_n = 0$ and $Z_n = A_n + A_{n-1}$ if $B_n = 1$. Design the FSM. Show your state transition diagram, encoded state transition table, next state and output equations, and schematic.

State transition diagram:

![State Transition Diagram](State_transition_diagram.jpg)

Encoded State Transition Table:

Current State	Next State	A	B
S0	S0	0	0
S0	S1	1	0
S1	S1	0	1
S1	S0	1	1

Next State Equations:

Next State = S0 (A = 0, B = 0)

Next State = S1 (A = 1, B = 0)

Next State = S1 (A = 0, B = 1)

Next State = S0 (A = 1, B = 1)

Output Equations:

$Z = A_n * A_{n1} \quad (B = 0)$

$Z = A_n + A_{n1} \quad (B = 1)$

Schematic:

![Schematic](Schematic.jpg)

Question M, Part A

Ben Bitdiddle has designed the circuit, shown in the figure, to compute a registered four-input XOR function. Each two-input XOR gate has a propagation delay of 100 ps and a contamination delay of 55 ps. Each flip-flop has a setup time of 60 ps, a hold time of 20 ps, a clock-to-Q maximum delay of 70 ps, and a clock-to-Q minimum delay of 50 ps. If there is no clock skew, what is the maximum operating frequency of the circuit?

The maximum operating frequency of the circuit is 1.35 GHz.

Question M, Part B

Ben Bitdiddle has designed the circuit, shown in the figure, to compute a registered four-input XOR function. Each two-input XOR gate has a propagation delay of 100 ps and a contamination delay of 55 ps. Each flip-flop has a setup time of 60 ps, a hold time of 20 ps, a clock-to-Q maximum delay of 70 ps, and a clock-to-Q minimum delay of 50 ps. How much clock skew can the circuit tolerate if it must operate at 2 GHz?

The clock skew must be less than 30 ps in order for the circuit to operate at 2 GHz.

Question M, Part C

Ben Bitdiddle has designed the circuit, shown in the figure, to compute a registered four-input XOR function. Each two-input XOR gate has a propagation delay of 100 ps and a contamination delay of 55 ps. Each flip-flop has a setup time of 60 ps, a hold time of 20 ps, a clock-to-Q maximum delay of 70 ps, and a clock-to-Q minimum delay of 50 ps. How much clock skew can the circuit tolerate before it might experience a hold time violation?

Assuming that the clock skew affects the flip-flops equally, the circuit can tolerate a maximum clock skew of 55 ps before it might experience a hold time violation.

Question M, Part D

Ben Bitdiddle has designed the circuit, shown in the figure, to compute a registered four-input XOR function. Each two-input XOR gate has a propagation delay of 100 ps and a contamination delay of 55 ps. Each flip-flop has a setup time of 60 ps, a hold time of 20 ps, a clock-to-Q maximum delay of 70 ps, and a clock-to-Q minimum delay of 50 ps. Alyssa P. Hacker points out that she can redesign the combinational logic between the registers to be faster and tolerate more clock skew. Her improved circuit also uses three two-input XORs, but they are arranged differently. What is her circuit? What is its maximum frequency if there is no clock skew? How much clock skew can the circuit tolerate before it might experience a hold time violation?

Alyssa P. Hacker's improved circuit is shown in the figure below. This circuit has a maximum frequency of 600MHz with no clock skew. It can tolerate up to a 28 ps clock skew before it might experience a hold time violation.

Question N, Part A

You are designing an adder for the blindingly fast 2-bit RePentium Processor. The adder is built from two full adders such that the carry out of the first adder is the carry in to the second adder, as shown in the figure. Your adder has input and output registers and must complete the addition in one clock cycle. Each full adder has the following propagation delays: 20 ps from Cin to Cout or to Sum (S), 25 ps from A or B to Cout, and 30 ps from A or B to S. The adder has a contamination delay of 15 ps from Cin to either output and 22 ps from A or B to either output. Each flip-flop has a setup time of 30 ps, a hold time of 10 ps, a clockto-Q propagation delay of 35 ps, and a clock-to-Q contamination delay of 21 ps. If there is no clock skew, what is the maximum operating frequency of the circuit?

The maximum operating frequency of the circuit is 50 MHz. This is calculated by taking the longest propagation or contamination delay (35 ps in this case) and dividing it by the clock period. The clock period must be at least 35 ps in order to guarantee that all the flip-flops will transition correctly with no clock skew. Thus, the maximum operating frequency is $1/35 \text{ ps} = 50 \text{ MHz}$.

Question N, Part B

You are designing an adder for the blindingly fast 2-bit RePentium Processor. The adder is built from two full adders such that the carry out of the first adder is the carry in to the second adder, as shown in the figure. Your adder has input and output registers and must complete the addition in one clock cycle. Each full adder has the following propagation delays: 20 ps from Cin to Cout or to Sum (S), 25 ps from A or B to Cout, and 30 ps from A or B to S. The adder has a contamination delay of 15 ps from Cin to either output and 22 ps from A or B to either output. Each flip-flop has a setup time of 30 ps, a hold time of 10 ps, a clockto-Q propagation delay of 35 ps, and a clock-to-Q contamination delay of 21 ps. How much clock skew can the circuit tolerate if it must operate at 8 GHz?

The clock skew that the circuit can tolerate is 1.75 ns.

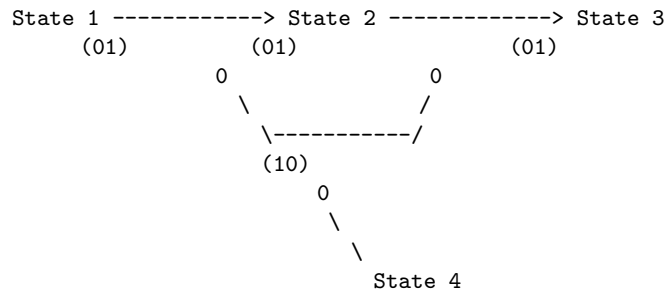
Question N, Part C

You are designing an adder for the blindingly fast 2-bit RePentium Processor. The adder is built from two full adders such that the carry out of the first adder is the carry in to the second adder, as shown in the figure. Your adder has input and output registers and must complete the addition in one clock cycle. Each full adder has the following propagation delays: 20 ps from Cin to Cout or to Sum (S), 25 ps from A or B to Cout, and 30 ps from A or B to S. The adder has a contamination delay of 15 ps from Cin to either output and 22 ps from A or B to either output. Each flip-flop has a setup time of 30 ps, a hold time of 10 ps, a clockto-Q propagation delay of 35 ps, and a clock-to-Q contamination delay of 21 ps. How much clock skew can the circuit tolerate before it might experience a hold time violation?

The circuit can tolerate a clock skew of 1.21 ns before it might experience a hold time violation.

Question O

Draw a state machine that can detect when it has received the serial input sequence 01010.



Execution Time

0:01:29.788241

OpenAI Parameters

Model: text-davinci-003, Max. Tokens: 1024, Temperature: 1, N: 1