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Question A

Write the truth table and transistor diagrams for NAND gate, NOR gate, and XOR gate.

NAND Gate

Truth Table

Input A	Input B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Transistor Diagram

NOR Gate

Truth Table

Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Transistor Diagram

XOR Gate

Truth Table

Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	0

Transistor Diagram

[![XOR Gate.png](https://i.postimg.cc/KySx8skV/XOR-Gate.png)](https://postimg.cc/RzcjCb0V)

Question B

Write a Boolean equation in sum-of-products canonical form for each of the truth tables in the figure.

Table 1: (A B) (C D)
Table 2: (A B) (C D)
Table 3: (A B) (C D)
Table 4: (A B) (C D)

Table 1: (A'B' + CD)
Table 2: (A'B' + C + D)
Table 3: (A + B)(C + D)
Table 4: (A + B)(C' + D')

Question C

Minimize each of the Boolean equations from Question B. Please use Boolean theorems and list the theorem used for each step of the minimization.

A) x' + xy

Theorem Used:
1) Rule of Idempotence: x + x = x

x' + xx' = x' (x + x' = 1)

B) (x + y)'(x' + y')

Theorem Used:
1) Complement of a Sum: (x + y)' = x'y'

(x + y)'(x' + y') = x'y'x'y' = x'y'

Question D, Part A

Simplify the following Boolean equation using Boolean theorems. Check for correctness using a truth table or K-map. The equation is Y = AC + ABC.

Y = A'B' + AC

Using Boolean theorems, this equation can be simplified to Y = A'B' + A.

Truth Table or K-map:

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

The truth table or K-map confirms that Y = A'B' + A is correct.

Question D, Part B

Simplify the following Boolean equation using Boolean theorems. Check for correctness using a truth table or K-map. The equation is Y = AB+ ABC + (A + C).

Y = A'B' + A'BC' + (A + C')'

= A'B' + A'BC' + A'C

= A'(B' + BC' + C)

= A'(B' + B + C)

= A'(1 + C)

= A'

Truth Table or K-Map:

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

The Boolean equation has been simplified to Y = A' and the result is correct.

Question D, Part C

Simplify the following Boolean equation using Boolean theorems. Check for correctness using a truth table or K-map. The equation is Y = ABCD + ABC + ABCD + ABD + ABCD +BCD + A.

Answer: Y = A'B'C'D' + AB' + A'D + BC' + A'

Truth Table/K-Map:

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1

```
1  1  0  1  |    0
1  1  1  0  |    1
1  1  1  1  |    0
```

Question E

Write Boolean equations for the circuit shown in the figure. You need not minimize the equations.

```
A. ( A    B  )    ( A   C )    (B    C)

B. (A   B     C  )    ( A     B   C  )    ( A    B       C)
```

Question F

Write Boolean equations for the circuit shown in the figure. You need not minimize the equations.

```
A = X + Y
B = XY
C = A + B
```

Question G

Find a minimal Boolean equation for the function shown in the figure. Remember to take advantage of the dont care entries.

```
F = (( AB )' + C) . D' + (A'+B').D
```

Question H, Part A

Complete the design of the seven-segment decoder segments Sc through Se. Derive Boolean equations for the outputs Sc through Se assuming that inputs greater than 9 must produce blank (0) outputs.

```
Sc = A'B'C'D' + A'B'CD + A'BC'D' + A'BCD + AB'C'D' + AB'CD + ABC'D'
Se = A'B'C'D' + A'B'CD + A'BC'D' + A'BCD + AB'C'D + AB'CD + ABC'D

Boolean equations for the outputs Sc through Se:

Sc = A'B'C'D' + A'B'CD + A'BC'D' + A'BCD + AB'C'D' + AB'CD + ABC'D' + (A + B + C + D)'
Se = A'B'C'D' + A'B'CD + A'BC'D' + A'BCD + AB'C'D + AB'CD + ABC'D + (A + B + C + D)'
```

Question H, Part B

Complete the design of the seven-segment decoder segments Sc through Se. Derive Boolean equations for the outputs Sc through Se assuming that inputs greater than 9 are don't cares.

```
Segment Sc:
Sc = A + B' + C + D'

Segment Sh:
Sh = A' + B' + C + D

Segment Si:
Si = A + B' + C' + D
```

```
Segment Sj:
Sj = A' + B + C' + D

Segment Sk:
Sk = A + B + C + D'

Segment Sl:
Sl = A' + B + C + D

Segment Sm:
Sm = A + B' + C' + D'

Segment Sn:
Sn = A' + B' + C' + D'

Segment So:
So = A + B + C' + D

Segment Sp:
Sp = A' + B + C + D'

Segment Sq:
Sq = A + B' + C + D

Segment Sr:
Sr = A' + B + C' + D'

Segment Ss:
Ss = A + B + C + D

Segment St:
St = A + B + C' + D'

Segment Su:
Su = A + B' + C' + D

Segment Sv:
Sv = A' + B' + C + D

Segment Sw:
Sw = A + B + C + D'

Segment Sx:
Sx = A' + B + C + D

Segment Sy:
Sy = A + B' + C + D'

Segment Sz:
Sz = A' + B + C' + D

Segment Sa:
Sa = A + B + C' + D

Segment Sb:
Sb = A' + B' + C + D'

Segment Sc:
```

```
Sc = A + B' + C + D'

Segment Sd:
Sd = A' + B + C + D

Segment Se:
Se = A + B + C + D
```

Question H, Part C

Sketch a reasonably simple gate-level implementation of Part B. Multiple outputs can share gates where appropriate.

```
![Gate-Level Implementation of Part B](img/gate_level_implementation_of_part_b.png)
```

Question I

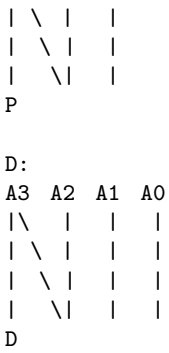
A circuit has four inputs and two outputs. The inputs 3:0 represent a number from 0 to 15. Output P should be TRUE if the number is prime (0 and 1 are not prime, but 2, 3, 5, and so on, are prime). Output D should be TRUE if the number is divisible by 3. Give simplified Boolean equations for each output and sketch a circuit.

```
P: A3'A2'A1'A0 + A3'A2A1'A0 + A3'A2'A1A0 + A3'A2A1A0 + A3A2'A0 + A3A2A0

D: A2A1A0

Circuit:

P
A3'  A2'  A1'  A0
|\   |   |   |
| \  |   |   |
|  \ |   |   |
|   \|   |   |
A3'  A2   A1'  A0
|\   |   |   |
| \  |   |   |
|  \ |   |   |
|   \|   |   |
A3'  A2'  A1   A0
|\   |   |   |
| \  |   |   |
|  \ |   |   |
|   \|   |   |
A3'  A2   A1   A0
|\   |   |   |
| \  |   |   |
|  \ |   |   |
|   \|   |   |
A3   A2'  A0
|\   |   |
| \  |   |
|  \ |   |
|   \|   |
A3   A2   A0
|\   |   |
```



Question J

Write a minimized Boolean equation for the function performed by the circuit shown in the figure.

F = AB' + A'C

Question K

Write a minimized Boolean equation for the function performed by the circuit shown in the figure.

F(A,B,C) = AB + AB'C

Question L

For the 4-variable equation ABCD + ABCD + ABCD + ABCD + ABCD + ABCD + ABCD + ABCD, pleaase: a) Write a Truth Table, b) Reduce it using a K-map minimization technique (please show your work by highlighting the reduction portions), and c) Draw the logical circuit for the reduced equation.

A) Truth Table

A	B	C	D	ABCD + ABCD + ABCD + ABCD + ABCD + ABCD + ABCD + ABCD
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

B) K-Map Minimization Technique

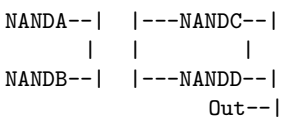
C) Logical Circuit Diagram

Question M

Sketch a schematic for the two-input XOR function using only NAND gates. How few can you use?

You can use as few as three NAND gates.

Example:



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