# Solutions PDF Generated from: solutions-openai-generated/labs/lab-02-solutions-set- 01.json

## Question A

Fill out the truth table, which describes the operation of a full adder. We use the inputs A, B, CI and the outputs are called S and CO.

## Question B

| |--|--|--|

Derive the Boolean equations for both outputs of a full adder. Apply logic minimization techniques to come up with a simplified full adder circuit.

```
Full Adder Boolean Equations:
```

## Question C

Draw the schematic of the full adder circuit according to the equations you have derived.

![Full Adder Schematic](full\_adder\_schematic.png)

## Question D

```
Generate full adder Verilog code for outputs co (carry out) and s (sum) module full_adder( input a,input b,input ci, output co,output s);

//assign the variables with their respective values assign s = a ^ b ^ ci; assign co = (a & b) | (ci & (a ^ b));
endmodule
```

#### **Execution Time**

0:00:28.109315

## **OpenAI Parameters**

```
Model: text-davinci-003, Max. Tokens: 1024, Temperature: 1, N: 1
```