Department Of Computer Engineering

Subject : Microprocessor Class: SE Computer MCQ : Unit I and II

Question	Option1	Option2	Option3	Option4	CorrectOption
80386DX is a _____ bit microprocessor?	32	16	8	64	1
The 803806DX can address upto _____ vitual memory	1 TeraByte	64 TeraByte	16 TeraByte	8 TeraByte	2
The 32-bit control register, that is used to hold global machine status, independent of the executed task is	CR0	CR3	CR2	all of the mentioned	4
Which of the following is a data segment register of 80386	ES	FS	GS	all of the mentioned	4
During the instruction cycle of 80386, any debug fault can be ignc	VM flag is set	VM flag is cleared	RF is cleared	RF is set	4
Which of the following pin when activated, allows address pipeli	ADS	READY	AP	NA	4
The unit that provides a four level protection mechanism, for system's code and data against application program is	central processing unit	segmentation unit	Paging Unit	Bus Control Unit	2
The Shortest time unit of bus activity is called as_____	Idle State	Bus State	Wait State	None of These	2
The unit that interfaces the internal data bus with the system bus	bus sizing unit	data buffer	bus control unit	execution unit	2
The maximum length of the string in a bit string of contiguous b	2 MB	4 MB	2 GB	4 GB	4
Among eight debug registers, DR0-DR7, the registers that are reserved by Intel are	DR0, DR1, DR2	DR4, DR5	DR1, DR4	DR5, DR6, DR7	2
The registers that are used to store four program controllable break point addresses are	DR5-DR7	DR0-DR1	DR6-DR7	DR0-DR3	4
The test register(s) that is provided by 80386 for page caching is	test control registers	page cache registers	test control and test status registers	test control and page cache registers	3
Which of the units is not a part of internal architecture of 80386	central processing unit	Memory Management Unit	Bus Interface Unit	None of the Mentione	4
The Unit that increases the speed of all shift and rotate operation	Memory Management Unit	Execution Unit	Instruction Unit	Barrel Shifter	4
The register DR6 hold	break point status	break point control information	break point status and break point control information	none of the mentioned	1
The signal that is used to insert WAIT states in a bus cycle in 8038	HOLD	HLDA	READY	PEREQ	3
The Rgister width used by the 32 bit addressing mode is	8 Bits	16 Bits	32 bits	all of the mentioned	4
The VM(Virtual Mode) flag is to be set only when 80386 is in	Virtual Mode	Protected Mode	Either Virtual or Protected Mode	all of the mentioned	2
The segment descriptor register is used to store	Attributes	Limit Address of segment	Base address of segmer	all of the mentioned	4
The descriptor table that the 80386 supports is	GDT (Global descriptor table)	IDT (Interrupt descriptor table)	TSS (Task state segment descriptor)	all of the mentioned	4
The registers that are togethor known as system address registers	GDTR and IDTR	IDTR and LDTR	TR and GDTR	LDTR and TR	1

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The flag bits that indicate the privilege level of current IO operati	virtual mode flag bits	IOPL flag bits	resume flag bits	none of the mentioned	2
80386DX is available in a grid array package of	64 pin	128 pin	132 pin	142 pin	3
The INTR signal can be masked by resetting the	TRAP flag	INTERRUPT flag	VM Flag	Resume Flag	2
In a 32-bit register, ESP, the lower 16-bits of the register can be represented by	RSP	SP	LSP	FSP	2
Contents of an index register are multiplied by a scale factor that may be added further to get the operand offset inmultiplied	base scaled indexed mode	scaled indexed mode	indexed mode	none of the mentioned	2
The bit that indicates whether the segment is page addressable is	base address	attribute bit	present bit	granularity bit	4
Which of the following is not a bit test instruction?	BTC	BSF	BTS	BTR	2
If a '1' is encountered when an operand is scanned by BSF, then	zero flag is reset	zero flag is set	VM flag is set	RF flag is reset	2
Which of the following is not a data copy/transfer instruction?	MOV	PUSH	POP	DAS	4
Which of the following instruction is not valid?	MOV AX, BX	MOV DS, 5000H	MOV AX, 5000H	PUSH AX	2
In PUSH instruction, after each execution of the instruction, the stack pointer is	incremented by 1	decremented by 1	incremented by 2	decremented by 2	4
The following instruction is an example of_____ addressibg mode MOV EBX, [EDX*4] [ECX]	base scaled indexed mode	scaled indexed mode	indexed mode	based scaled indexed mode with displacement mode	1
The instruction that is used to swap the contents of operands is	XLAT	XCHG	COPY	TYPE	2
To form a physical memory address, appropriate segment register contents are	shifted by left by 4 positions	added to 16-bit offset address	operated using one of addressing modes	all of the mentioned	4
The instruction that loads the AH register with the lower byte of the flag register is	SAHF	AH	LAHF	PUSHF	3
The instruction that supports addition when carry exists is	ADD	ADC	ADD and ADC	SBB	2
In 32 bit division the remainder is stored in which register	EDX	EAX	ECX	EBP	1
The 80386 can perform_____ Machine Cycles	Pipelined	Nonpipelined	Both 1 and 2	None of these	3