

**CMPEN 331 – Computer Organization and Design,  
Lab 1**

**Due Sunday, September 22, 2019 at 11:59 pm (Drop box on Canvas)**

In this lab, you will obtain experience with sequential logic design, and study digital design using the Xilinx design package for FPGAs. It is assumed that the students are familiar with the operation of the Xilinx design package for Field Programmable Gate Arrays (FPGAs) through the Xilinx tutorial available in the class website.

1. A finite state machine is a way of modeling system in which the system's output will depend on not only the current inputs but also the past history of inputs. It defines a finite set of states and behaviors, and how the system transits from one state to another when certain conditions are true. The module of output function is a combinational circuit that generates the outputs based on the current state (Moore model) or the combination of the current state and the current inputs (Mealy model).
2. Suppose we design a radix of six up/down counters as shown in Figure 1. The state of the counter changes on the positive (rising) edge of the clock. If the input  $u$  is a 1, the counter value will change in the sequence 0, 1, 2, 3, 4, 5, 0, 1, 2, ... . If  $u$  is a 0, the counter value will change in the sequence 0, 5, 4, 3, 2, 1, 0, 5, 4, ... . There are seven output signals, with each connecting to a segment of LED. A segment of the LED will be on if its control signal is a 0 (active-low).
3. There are six states, the circuit of the counter is shown in Figure 2. The module of dff3 contains three DFFs. The other module is a combinational circuit that generates signals of the next state ( $ns[2:0]$ ) and LED control signals ( $a, b, c, d, e, f$ , and  $g$ ). The current state (the outputs of dff3) is denoted with  $q[2:0]$ .
4. Figure 3 shows the state transition diagram. The arrowed lines indicate the transitions of the states under the condition of the input. Figure 3 also shows that a 3-bit unique code is assigned to a state. Any code can be assigned to any state as long as all the codes are unique.
5. Table 1 is the truth table for the next state.
6. **For students who took this class as an (honor option).** Figure 4 shows the Karnaugh maps for each of the next state signals. From the Karnaugh maps, you can get the expressions of the next state signals. Figure 5 shows the truth table and Karnaugh maps of the output signals. You can get the expressions of the output signals from the Karnaugh maps.

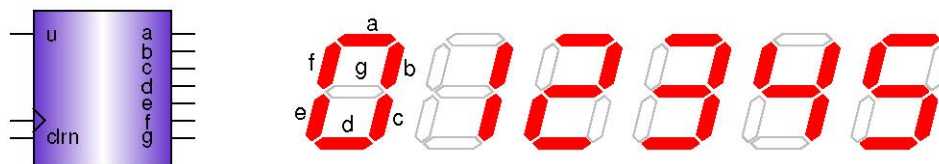


Figure 1 A counter with a seven-segment LED

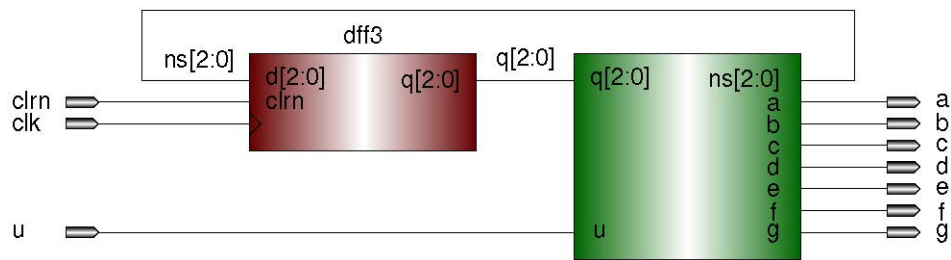


Figure 2 Block diagram of a counter with a seven segment LED

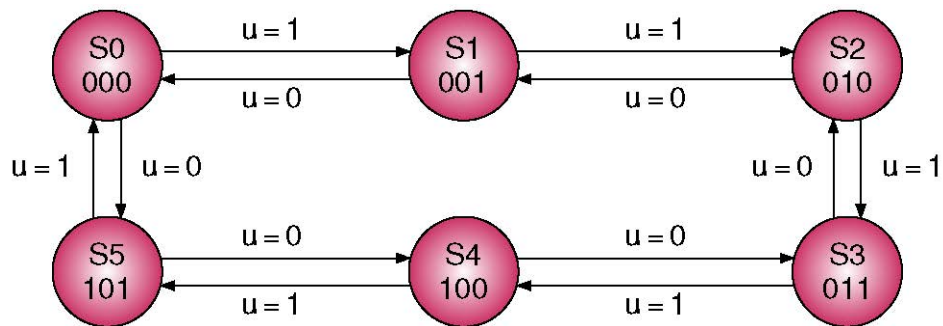


Figure 3 State transition diagram of the counter

Table 1 State transition table

Current state				Input	Next state			
	$q[2]$	$q[1]$	$q[0]$	$u$		$ns[2]$	$ns[1]$	$ns[0]$
S0	0	0	0	1	S1	0	0	1
				0	S5	1	0	1
S1	0	0	1	1	S2	0	1	0
				0	S0	0	0	0
S2	0	1	0	1	S3	0	1	1
				0	S1	0	0	1
S3	0	1	1	1	S4	1	0	0
				0	S2	0	1	0
S4	1	0	0	1	S5	1	0	1
				0	S3	0	1	1
S5	1	0	1	1	S0	0	0	0
				0	S4	1	0	0

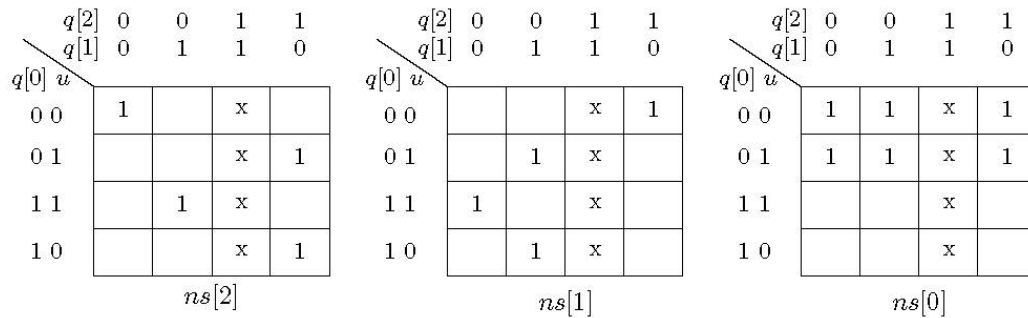


Figure 4 Karnaugh map for next state of the counter

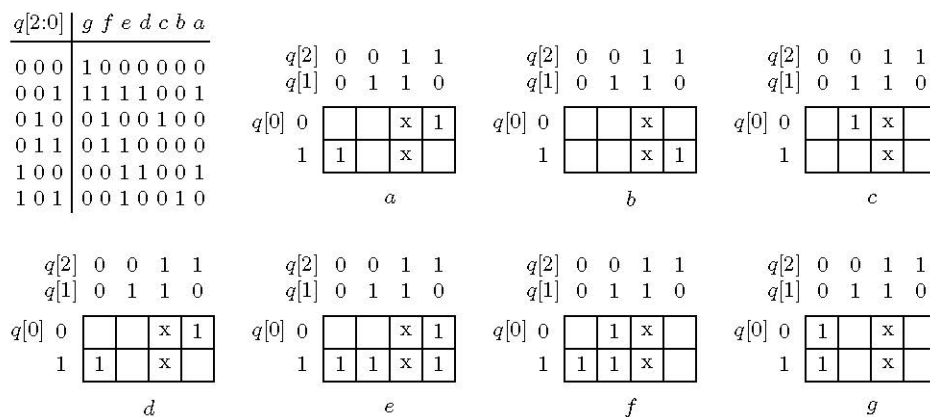


Figure 5 Karnaugh map for the output function of the counter

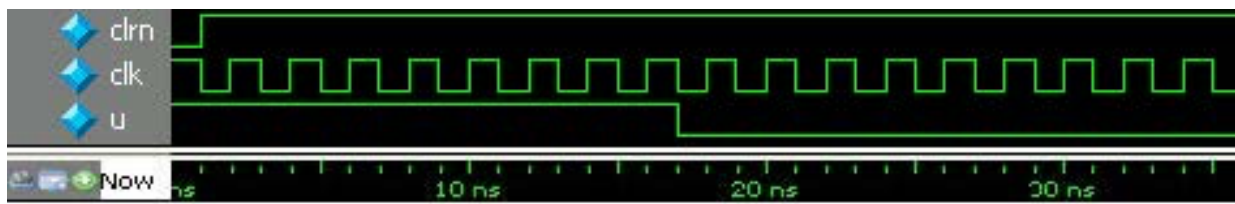


Figure 6 Test wave form

7. Write a behavioral Verilog code description using the states shown in Figure 1, 2, 3 and Table 1. Compile and simulate your code using the test sequence shown in Figure 6.
8. Write a report that contains the following:
  - a. Your Verilog design code. Use:
    - i. Device: XC7Z010- -1CLG400C
  - b. Your Verilog® Test Bench design code (use the test sequence shown in Figure 6). Add “timescale 1ns/1ps” as the first line of your test bench file.
  - c. The waveforms resulting from the verification of your design with ModelSim showing all the outputs of the following signals (**q**, **a**, **b**, **c**, **d**, **e**, **f**, **g**).
  - d. The design schematics from the Xilinx synthesis of your design. Do not use any area constraints.

- e. Snapshot of the I/O Planning and
- f. Snapshot of the floor planning

9. REPORT FORMAT: Free form, but it must be:

- a. One report per student.
- b. Have a cover sheet with identification: Title, Class, Your Name, etc.
- c. Using Microsoft word and it should be uploaded in word format not PDF. If you know LaTeX, you should upload the Tex file in addition to the PDF file.
- d. Double spaced

**10. You have to upload the whole project design file zipped with the word file.**

**11. For students who took this class as an (honor option).** In addition to all of the above requirements, you need to get the expressions of the next state and the output signals from Karnaugh maps. Compare the results that you get from Karnaugh map and the results you got from the behavioral model of the Verilog code.