

ECE 3750 Fundamentals III Final Project: EKG Printed Circuit Board

May 12, 2017

Honor Code:

On our honor, we have not given or received any unauthorized aid on this report.

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Bobby Stephens: Responsible for 30% of board testing, including final testing, mathematical calculations, and sections of the lab report.

Cassie Willis : Responsible for chosen circuit board layout, 90% of board soldering, and 70% of board testing as well as sections of the lab report.

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1 Background

1.1 Overall Approach

For this project, a functioning EKG must be built. The EKG takes in two inputs from one's pulse and a common-mode voltage, and converts these to a waveform that can be seen in the V-Out Measurement in the Virtual Bench. Building a device that could complete this task required several steps, and also the cascading of several components that are used together to provide the waveform. These components, or subsystems, are the test points, power system, shield driver, the instrumentation amplifier and the Butterworth Filter. The Power system is the first subsystem, which drives the board. This power is provided by either a 9V battery, Virtualbench source, MSP430, or myRio, and the output signal is provided by connecting the device up to a person in order to generate the signal on the Virtual Bench so that it can be seen. The power system then feeds into the instrumentation amplifier, shield driver, and 4th order Butterworth filter. The shield driver acts to eliminate the common mode voltage by acting as an artificial ground.

The Instrumentation Amplifier combines two stages. The first stage sets a very high Common Mode Rejection Ratio (CMRR), which filters out any background signal noise from the body. The second stage acts as a difference amplifier that isolates the heartbeat signal so that it can be seen, and ensures that there is no interference. This feeds into the

Butterworth system. The Butterworth filter serves as an anti-aliasing filter to make sure there is not another signal on the board that is being misinterpreted. This completes the approach to the actual PCB board that is designed. In order for the device to be fully functional, the myRio must be connected to the circuit so that the output can be read and verified to be as accurate. This project combines the concepts learned through the various modules of the class. The Power Module informed about the various power systems needed to supply a constant voltage. The third module showed how instrumentation amplifiers work, which became part of the backbone of this project. The fourth module showed how filters work, which provides the basis for the functions of the Butterworth filter, as well as helping us to understand how to read and interpret the signal output from the board using digital signal processing (Module 5) so that one can see how this works.

1.2 Expected Signal Levels and Gain Required

As stated in class, the expected input signal was between 10 uV and 100 uV. This input signal came from two different body parts (each wrist), and the difference between the two signals had to be amplified enough to be read by oscilloscope probes and the myRio microcontroller. There was also a common mode voltage (positive voltage offset), in each of the two input signals that needed to be removed. The third input signal was placed in the elbow area to measure the common mode voltage (the ambient level of electrical signal that was the positive offset), which acted as the ground for our circuit.

The gain was chosen to be about 2000, to amplify the input signal between 20 mV and 200 mV. The gain was low enough so that if for some reason the body produced an output voltage higher than the 100 uV range, it could still be amplified without saturation. To get a gain of 2000, the following gain equation was used for the AD623AN instrumentation amp:

$$Av = 1 + 2\left(\frac{100,000}{Rg1+Rg2}\right)$$

Where R_{g1} and R_{g2} are the two values of gain setting resistors. We originally chose two $56\ \Omega$ resistors to act as gain setting resistors, yielding a gain of 1962, approximately 2000. As discussed in the testing difficulties section, we changed the values of these resistors to $220\ \Omega$ and later $440\ \Omega$ in an effort to reduce the amount of noise that was being picked up in the circuit and causing the instrumentation amp to saturate.

1.3 Filtering Requirements

The main requirements for the filter were:

1. Filter out frequencies above 1 KHz in order to prevent aliasing in the digital signal.
2. Have as smooth of a filter as possible to prevent certain harmonics from being blown up.
3. Be cheap and easy to design and implement

The optimal solution for these constraints was a 4th order butterworth filter with a cutoff frequency of 100 Hz. This provided the smoothest decrease in magnitude, and a gain of -80 dB would affect frequencies at 1 KHz. In addition, with butterworth tables providing the necessary Q values, and websites that generate the best possible list of components using the Q value, the process of designing the Butterworth filter was relatively easy.

2 Schematics

2.1 Multisim Schematics

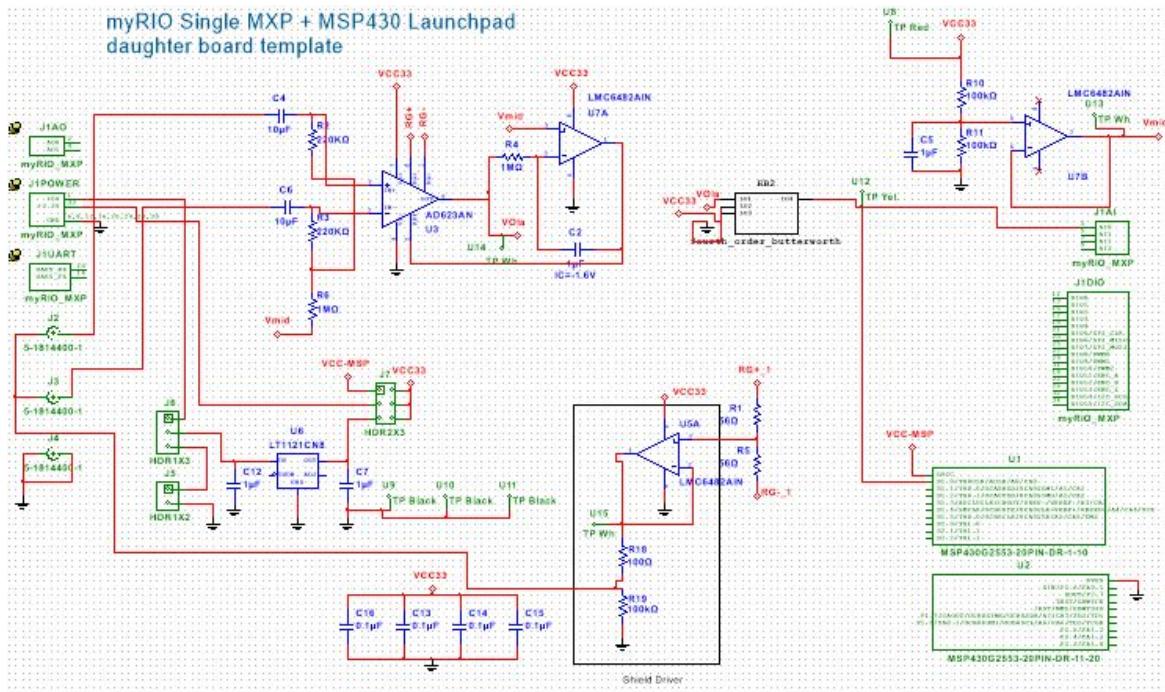


Figure 1: Entire Circuit Schematic

2.1.1 Power Supply Subsystem and Shield Driver

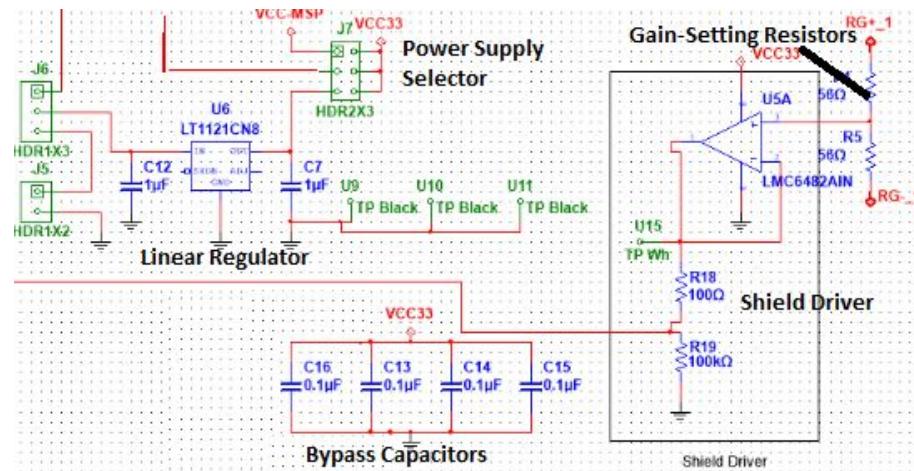


Figure 2: Power Supply and Shield Driver Subsystems

The above subcircuit is divided into two main parts. On the left is the power supply, on the right is the shield driver.

The power supply can come from 3 sources, which are on the left side of J7: the top left is the MSP430, the middle left is the MYRIO, and the bottom left is the linear regulator, fed by a 9V battery. We used jumpers to select the proper power supply in J7 for VCC33.

The purpose of the LT1121CN8 linear regulator was to keep a constant output voltage of 3.3 V despite varying input voltages affected by noise. The power supply for this part was the 9 V battery.

The purpose of the bypass capacitors was to smooth out VCC33 if it picked up any noise, so that VCC33 could continue to be a consistent power supply that did not affect the rest of the circuit due to saturation or its power supply rejection ratio.

The shield driver contained the two gain-setting resistors for the instrumentation amp. At the center point of the two gain-setting resistors, was the common mode voltage from the input of the circuit. This common mode voltage was fed through a voltage buffer, and then a voltage divider set it to 99.9% of its original voltage. This was then fed to the two inputs of the EKG and acted as a ground to cancel out the common mode voltage of the inputs.

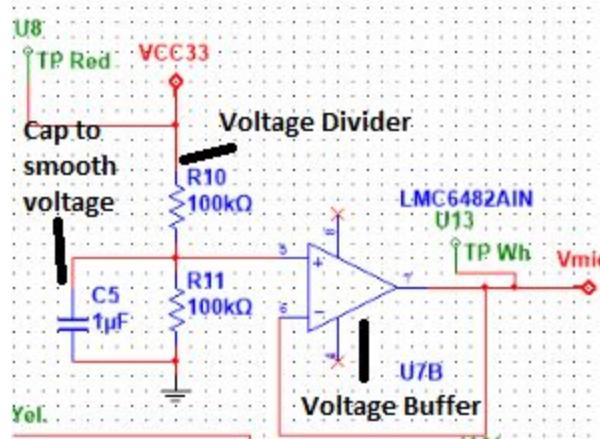


Figure 3: Vmid Voltage Divider

The above schematic shows the voltage divider that was used for Vmid. It was set to half of VCC33, at 1.65V. A voltage buffer was then used to make sure Vmid was constant and did not affect the VCC33 voltage. The capacitor C5 was used to smooth out VCC33 if it picked up any noise near the op amp.

2.1.2 Instrumentation Amplifier

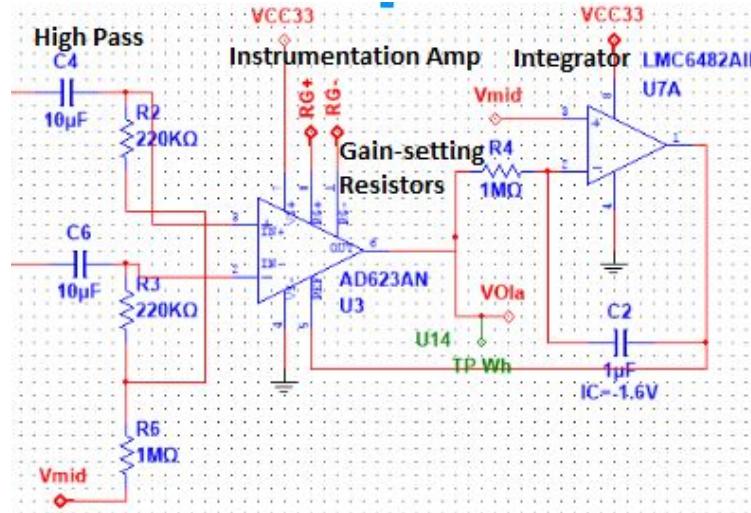


Figure 4: Instrumentation amp and Integrator

The above schematic shows the instrumentation amp subcircuit. On the left is two high pass filters for each of the two input signals with a cutoff frequency of about 0.1 Hz. This got rid of DC signals as they went into the instrumentation amp. Then, the instrumentation amp provided a gain of about 1000, to boost the 10-100 uV signal to about 10 - 100 mV. Rg+ and Rg- were pins to the instrumentation amp, which were part of the shield driver circuit.

On the right, the integrator integrated the difference between Vmid and the output of the instrumentation amp. This integrated difference was then added to the instrumentation amp as the reference voltage. The reason for this was to keep the output voltage of the instrumentation amp to be centered at Vmid (1.65 V). The integrator

essentially acted as a “servo” that kept the output at a constant offset iff 1.65 V, allowing EKG signals to be more visible.

2.1.3 4th Order Butterworth Filter

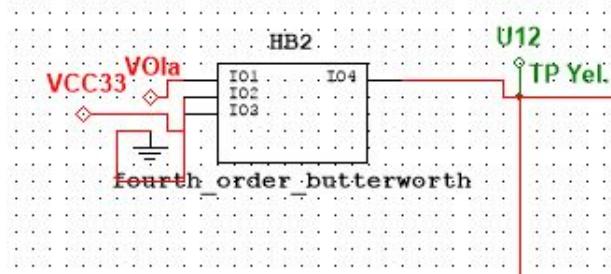


Figure 5: Butterworth box model

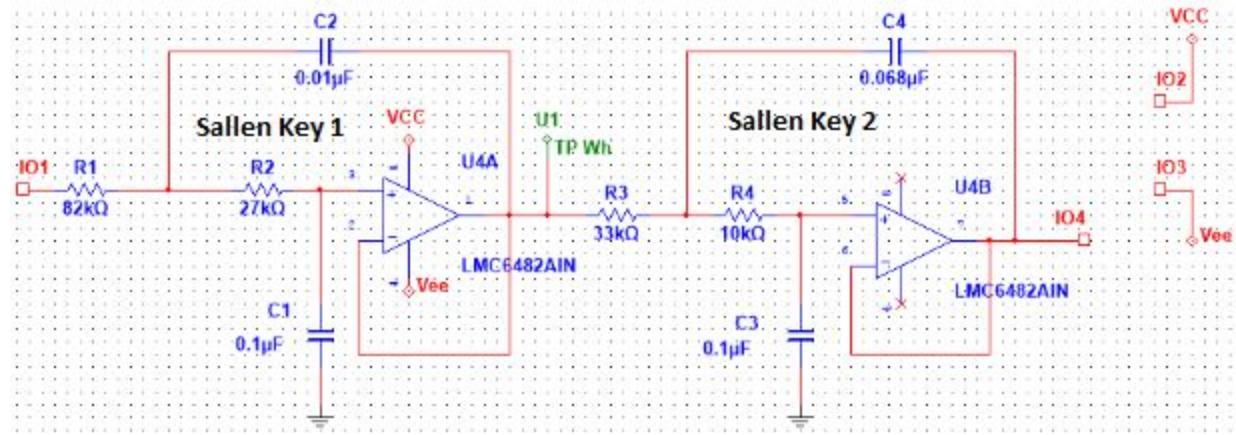


Figure 6: 4th Order Low-Pass Butterworth Filter

The above schematic shows the 4th order butterworth filter. The cutoff frequency was set to 100 Hz, and Q values of 1.306 and 0.5411 were chosen, matching up with the butterworth table. This allowed signals at 1 KHz to be at -80 dB so that no aliased signals would be measured by the digital signal processor in the myRio.

2.2 Ultiboard Schematics

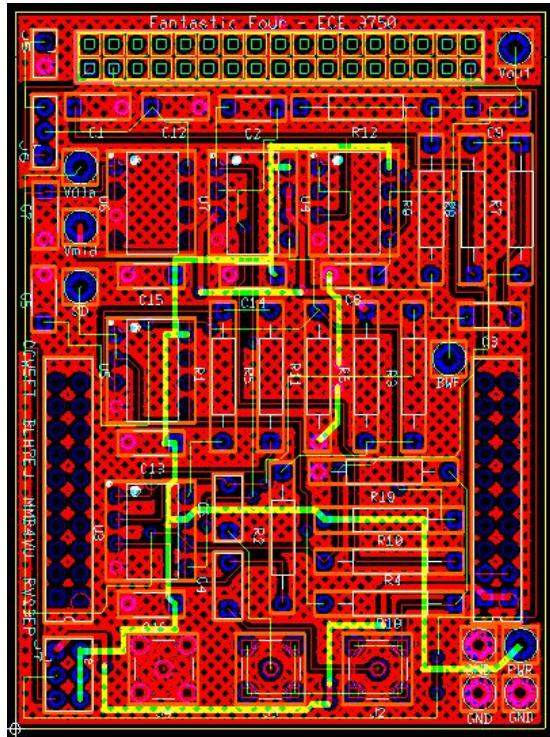


Figure 7: Entire Board Layout

2.2.1 Silkscreen Layer

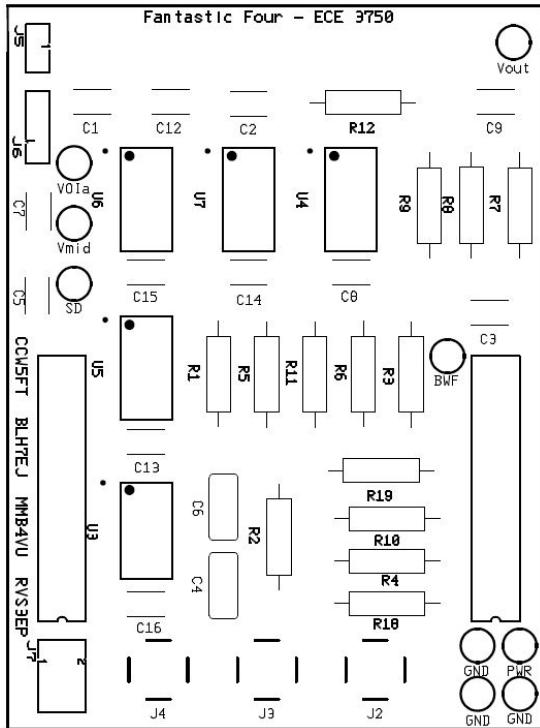


Figure 8: Silkscreen Layer of Board

The board's design layout was chosen specifically to make the design easy to debug, maximize power efficiency, and minimize signal loss by placing components close to other components they are connected to - allowing for shorter wires.

The instrumentation amplifier, part U3 on the silkscreen above, was placed as close to the signal input ports as possible (J2, J3, and J4) so that the signal loss before the amplification could be minimized; due to the input signal being in the order of millivolts, this was an imperative part of the board design.

The butterworth filter is entirely contained in the top right section of the board. This location is the farthest on the board from the instrumentation amplifier and the input ports because it is the last subsection of the board before the output pin. Putting it farthest away allows room for the other subsections in-between to be closer to the instrumentation

amplifier, creating a natural flow to the board's signal and minimizing loss with shorter wires between connecting components.

The test points were also placed in significant locations on the board to make sure they were close to the components of the board they were measuring. This both provided clarity in debugging as well as the most accurate signal measurement since the wires connecting the test point and the measured signal were minimized. Three ground test pins were added to allow powering the board and testing two subsections of the board at the same time. Intuitive naming was added to the test points on the silkscreen layer to make testing components easier to identify.

Finally, the designers ensured that all of the layout components were facing in either the downward or left direction. This was done for both cleanliness and to more quickly identify board components.

2.2.2 Copper Top Layer

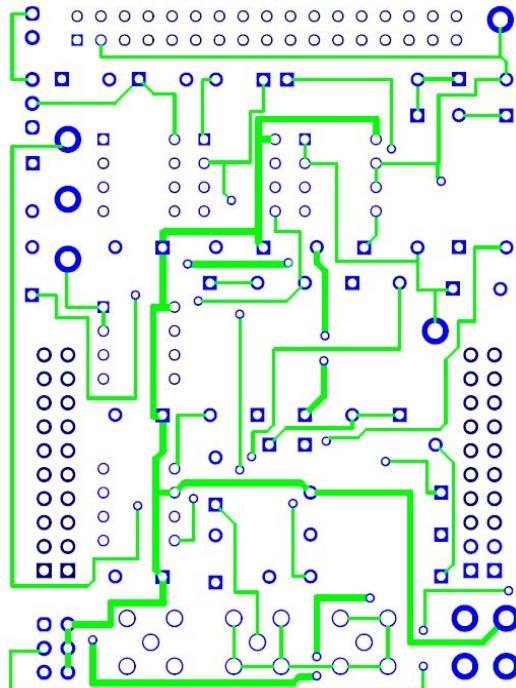


Figure 9: Copper Top Layer of Board

The figure above shows the copper top layer of the board. The wiring was completed in as many right angles as possible, with an emphasis on horizontal wiring wherever possible. This copper top layer was wired first so that the copper bottom layer could leave the ground plane as open as possible.

2.2.3 Copper Bottom Layer

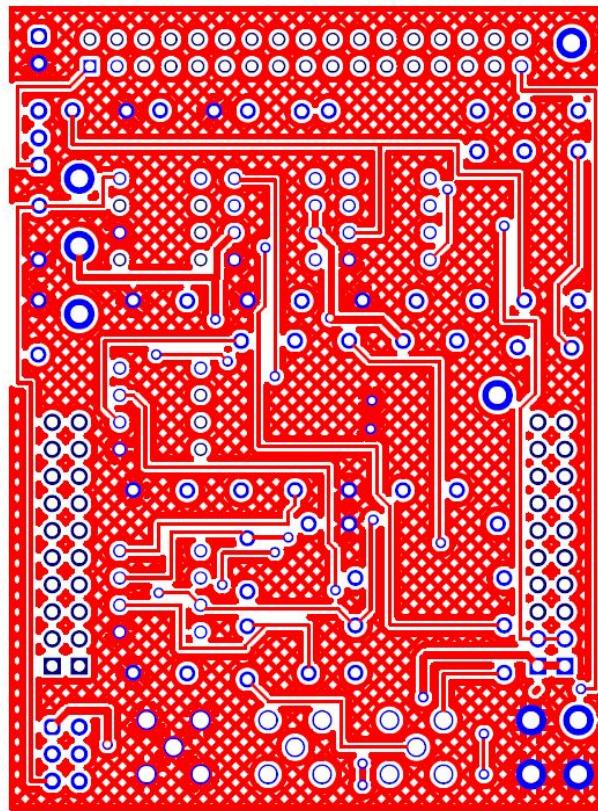


Figure 10: Copper Bottom Layer of Board with Ground Plane

The figure above is the copper bottom layer of the board. This layer has cross hatching that represents a ground plane that was added to this layer of the board. The ground plane was added to reduce the amount of wiring needed to connect every component. An emphasis was placed on trying to place the bottom wires in the vertical direction, however wiring on the bottom layer was completed after wiring on the top layer, so any gaps were filled in

where needed to ensure all components were wired correctly. For the bottom layer, the designers had to ensure that no ground plane areas were isolated by the presence of wires surrounding the area. This would have made the isolated section of the ground plane dysfunctional.

3 Simulation and Testing

3.1 CAM Files and FreeDFM Checks

DRC and netlist check [Untitled] - Saturday, April 08, 2017, 4:32:05 PM
Completed; 0 error(s), 0 warning(s), 0 filtered error(s); Time: 0:00.25

Connectivity check [Untitled] - Saturday, April 08, 2017, 4:32:23 PM
Completed; 0 error(s), 0 warning(s); Time: 0:00.25

Figure 11: DRC and Connectivity Checks Results

The screenshot shows the FreeDFM.com interface. At the top, there's a header with a logo and the text "What FreeDFM found on your design". Below it, a large red banner says "Show Stoppers" and "We Found None!". Another red banner below says "Problems Automatically Fixed". Underneath, there are two lists of issues with links to view them: "Insufficient Soldermask Clearance (49 violations)" and "Insufficient Silkscreen Line Width (868 violations)". Each list has a link to "View 1 2 3 4 5".

Figure 12: FreeDFM Check Results

The board was tested for connectivity, DRC, netlist, and show stopper errors. The DRC, netlist, and connectivity checks were performed in Ultiboard. The showstopper errors were completed by creating CAM (Gerber) files and submitting the files to FreeDFM.com. The process went smoothly, with the board coming back with no showstoppers after the

first submission to FreeDFM, so no errors had to be accounted for. The designer who submitted the CAM files had done so previously in other courses as well as in a robotics club where they work on board design, and this experience helped minimize errors in the board design.

3.2 Multisim Simulations

When performing the board simulations, the important subcircuits such as the Butterworth were simulated separately, and then the overall circuit was tested. The subcircuits tested include the 4th order Butterworth filter and the power supply. Since simulations for the entire circuit were supplied in the “hcp7ad-FUN3-S17-Top-Sim-ad623-hcp.ms14” file, the designers used those simulations for the entire circuit after changing the Shield Driver resistor values.

The Butterworth filter was simulated with an input of 0.2V pk-pk, and then the results after the first sallen key and the second sallen key were measured for frequencies of 10 Hz, 100 Hz, and 1KHz. The peak to peak values recorded were 0.166 V (1st Sallen Key), and 0.161 V (2nd Sallen Key) for 10 Hz, 0.0291V and 0.0107 V for 100 Hz, and 1.8 mV and 19.6 uV for 1 KHz.

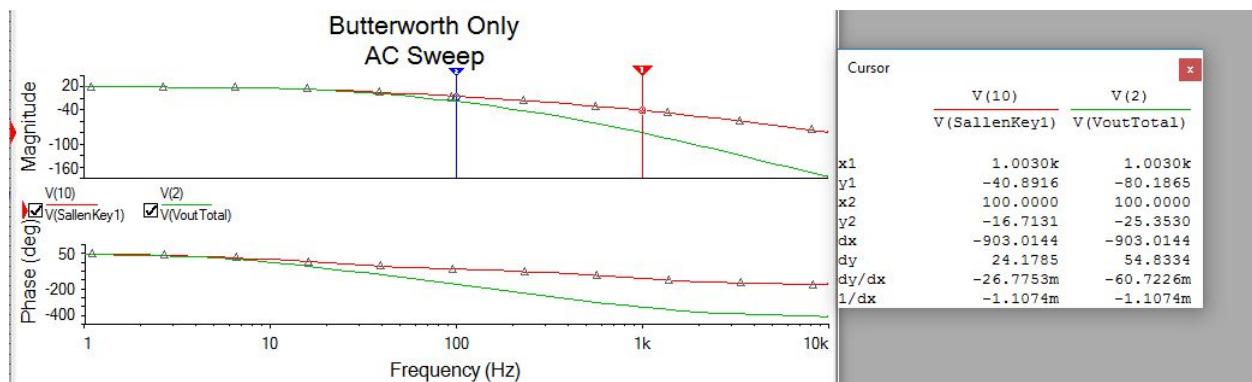


Figure 13: AC Sweep of Butterworth V(10) - Sallen Key 1, V(2) - Output

An AC sweep was performed on the 1st Sallen Key in the Butterworth filter (green) and the overall output (red). The value at 1 KHz was about -40 dB on the first filter and -80

dB on the overall output. The AC sweep also shows a smooth decrease in magnitude, as should be seen from a Butterworth filter.

Next, the values at the power supply section (linear regulator and Vmid Op-amp) were tested. All the values at VCC33 were 3.3V and Vmid was 1.65 V.

The complete circuit values were given by the hcp7ad-FUN3-S17-Top-Sim-ad623-hcp.ms14.ms14 file.

3.3 Soldering Process

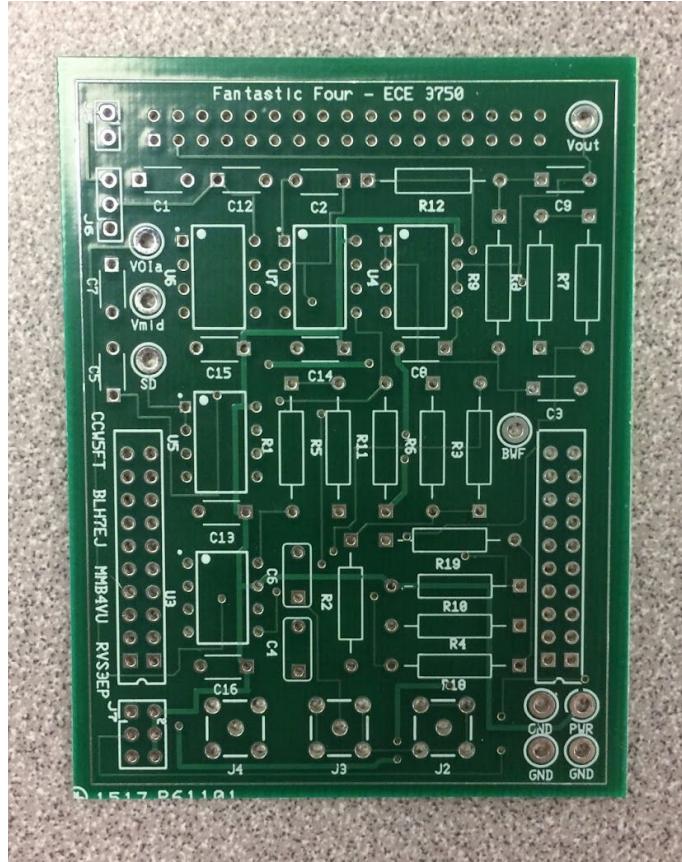


Figure 14: Initial PCB, without components

Above is a picture of the initial PCB design without soldered subsystems.

The board was soldered according to the test plan created a few weeks prior to receiving the board. The first components soldered on the board were the test points and the op-amp sockets. The test points were soldered first to make it easier to test the board as the soldering process continued, and the sockets were soldered second because they were some of the largest components to be added to the board and they could not affect any board testing as they were only sockets and not valued or operational components.

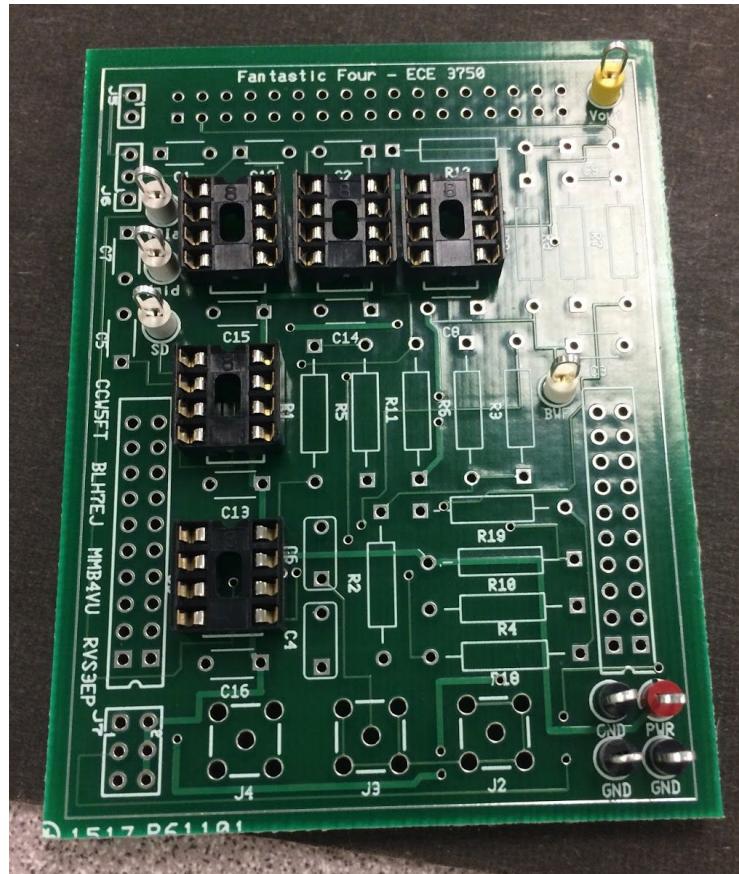


Figure 15: PCB with op amp sockets and test points soldered

The power subsystem was added to the board next, including the resistors, capacitors, and CMD ports associated with the power subsystem. The appropriate op-amps were also plugged into their sockets while testing was being performed, however the designers made sure to remove the op-amps from the board before continuing the soldering process in order to avoid overheating or accidentally damaging any of these components while soldering.

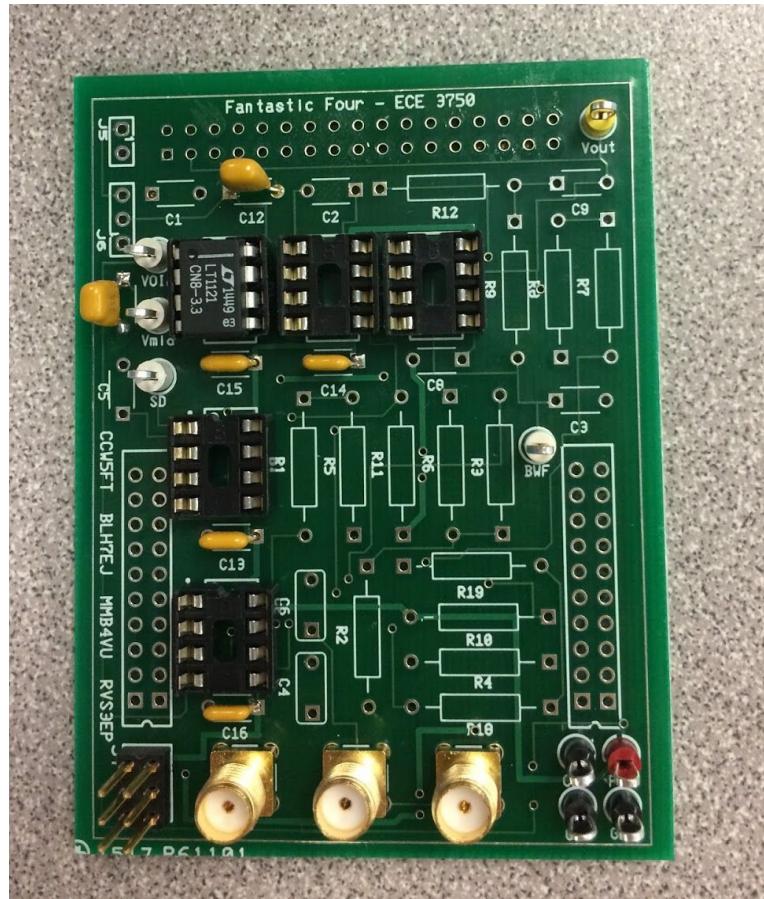


Figure 16: PCB after Power Subsystem Solder

The Butterworth subsystem was then added to the board. These components were all resistors and capacitors. The op-amp was also plugged in here for testing, but removed before the soldering process continued.

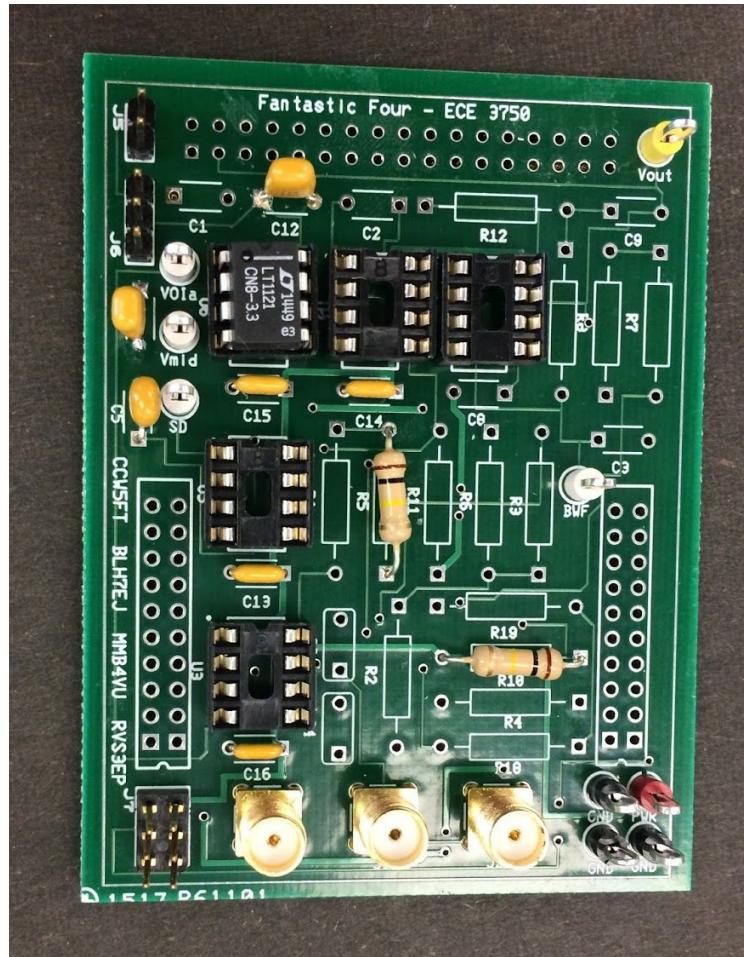
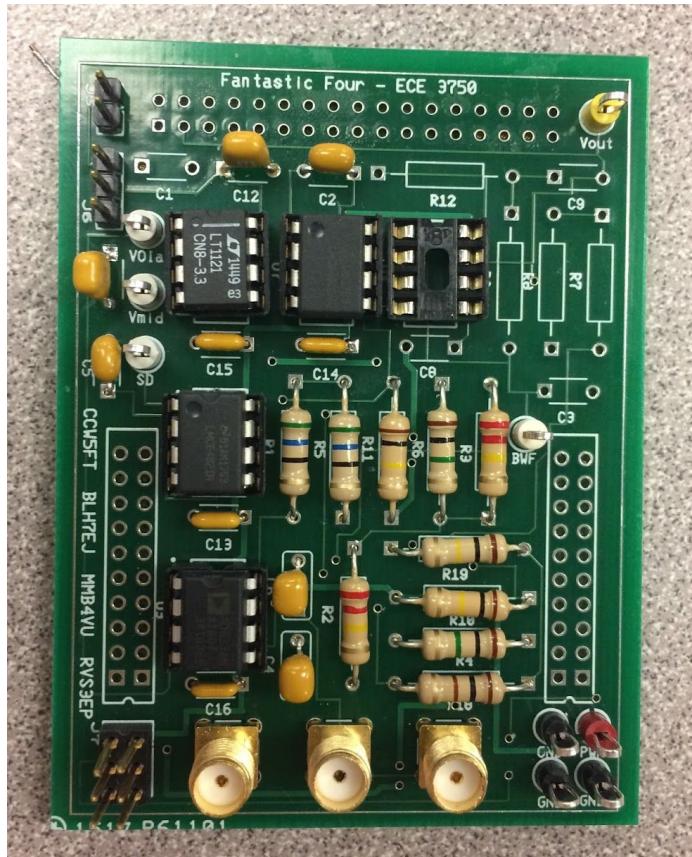


Figure 17: PCB after Butterworth Subsystem Solder

Next, the instrumentation amplifier and shield driver components were soldered onto the board. These resistors and capacitors completed the primary soldering, and the instrumentation amplifier and other op-amps were added to the board for testing. Two of these capacitors needed were not available to the designers, so a parallel configuration of capacitors was created by soldering two capacitors together to create the necessary capacitance desired for those components.



and the designers believed additional header boards could be placed on top of the current ones to make adequate room for the MSP430.

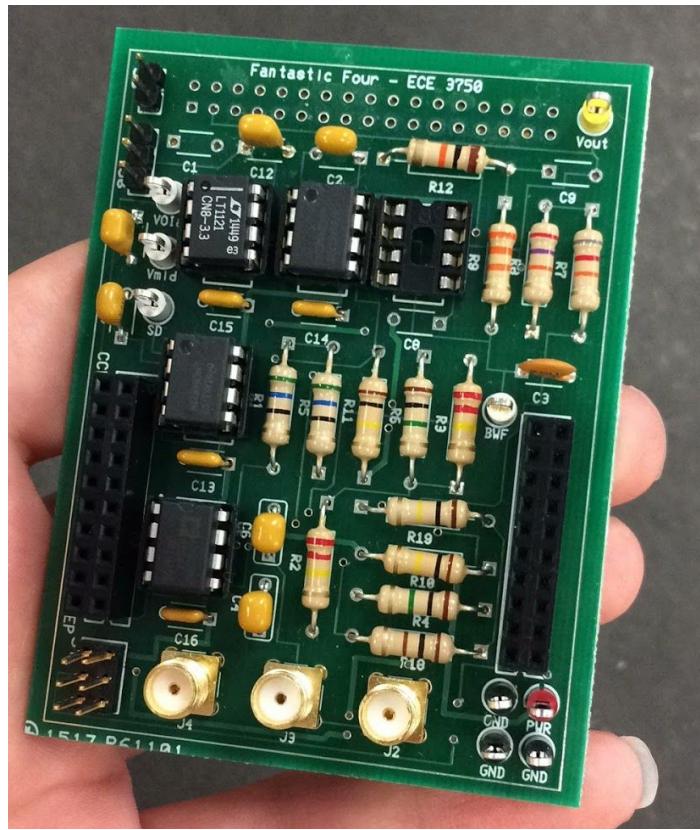


Figure 19: Final soldered PCB

The soldering was primarily completed by one team member, with another team member verifying component values, correct placement of the components, and solid solder joints at every hole.

3.4 Board Testing

The board was thoroughly tested throughout the soldering process. The first testing step that the designers implemented upon receiving the board was connectivity checks. The designers used the Multisim and Ultiboard schematics, along with a multimeter, to check for connectivity throughout the board before any components were added. The multimeter

used had a connectivity function built in, which beeped to indicate connectivity between two points. It was found that every point that was supposed to be connected was indeed connected as required.

The next step in testing came after the test points, op-amp sockets, and the power components were added to the board - testing the power subsystem. It was imperative to test this subsystem first, because all of the other subsystems relied on power. As components were added to the board, continuity was double checked to ensure that the solder joints provided solid connections. The VirtualBench was used to supply 5 V to the system at J6. The voltage on the “PWR” test point, representing VCC-33 was tested, as well as the voltage at Vmid, with successful values of 3.3V and 1.65V respectively.

The Butterworth filter subsystem was tested next. This subsystem was first tested on a breadboard using the VirtualBench. Testing was done on the breadboard first to ensure the wanted cutoff frequency was found without the other components already on the PCB affecting the signal. After it was verified that the components for the Butterworth filter were correct, these components were added to the board. Connectivity checks were again performed to ensure good solder joints.

The last subsystem to test was the Instrumentation Amplifier and Shield Driver. These subsystems were combined as one even though they include separate components because the two subsystems rely on each other, particularly with the gain setting resistors. These components were added to the board, and the VirtualBench was used both to supply power and measure the DC voltages at VOIa and the SD (Shield Driver) test points. Both points gave approximately the expected values of 1.65V and 0 V respectively. Connectivity checks were repeated here as well before the VirtualBench testing was completed.

Finally, the entire system was tested after all of the components were added to the board. This was done in two ways. First, the VirtualBench was used to produce a small 0.01Vpp sinusoidal signal. This signal was connected to the CMD ports to be run through the board, and the signal at Vout was measured. To power the board correctly, a 2-pin connector was used on J7 to connect VCC-33 and the 3.3V regulator output in order to correctly power the

op-amps. At 100 Hz, a value of 177 mV was measured, which was close to the Multisim value of 166 mV.

After testing with the function generator on the VirtualBench, one of the designers was connected to BioTech EKG electrodes - one positive lead on each wrist and one ground lead on an inside elbow. This placement was to ensure the largest possible potential difference - which was needed to most accurately measure heart rate. The electrodes were connected to the CMD ports with appropriate wiring, and an oscilloscope probe was placed at Vout to measure the heartbeat results. Because of the sensitivity of the electrodes and the millivolt-scale nature of the heartbeats, the participant had to remain completely still to get accurate heart rate measurements and to avoid measuring noise such as muscle movement.

It was found that several of the participants did not have a strong enough heartbeat to be measured using the EKG PCB. One participant, however, did have a strong heartbeat, and an accurate measurement was found on the Vout signal.



Figure 19: Heart rate signal (100mV/Div, 500ms/Div)

3.4.1 Testing Difficulties and Differences

One of the testing difficulties encountered was figuring out how many different frequencies to test the filters at in order to ensure that they were working. There was also a difficulty in troubleshooting the board once the testing was complete. When the board was first assembled, the entire EKG device was in fine working order. But then, later in the process, when the board was being prepared for the myRio, the signal was not appearing. In order to try and troubleshoot the board a number of steps were taken.

First of all, the board was connectivity checked, and all of those checks came out ok. Then, a series of tests was done involving the gain resistors on the shield driver and a variety of other parts. The resistors were originally 56 Ohms for the gain section of the shield driver. The resistors were changed to 220 Ohms, then to 460 Ohms in an attempt to increase the gain so that the board would have the filtering noise reduced so that the EKG signal could be unearthed. Unfortunately, this chain of processes did not work, as the EKG signal that was once present was never recovered. As discussed later in this report, the presumed cause was a short somewhere on the EKG board which was on one of the thin traces connecting the board. This caused the board to behave in a way that was not what was expected, and prevented the EKG signal from being present from the device.

4 Images

4.1 Soldering

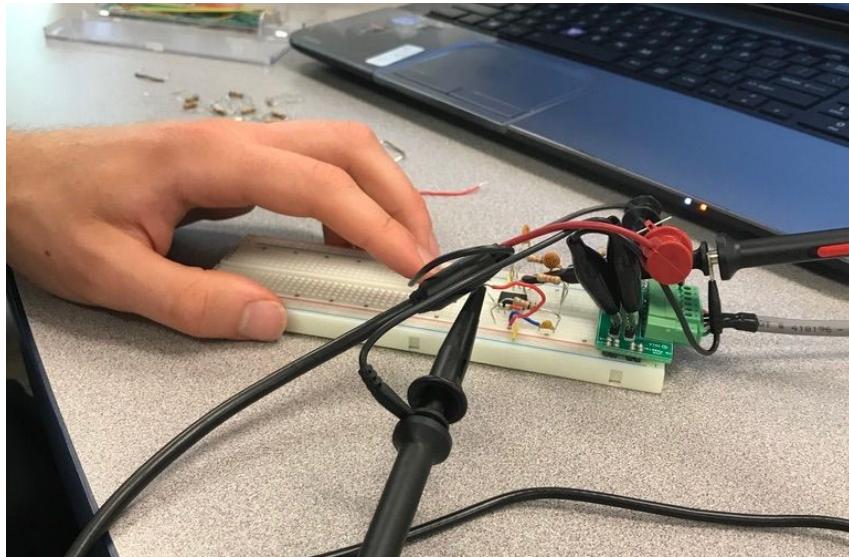


Figure 20: Butterworth pre-solder testing

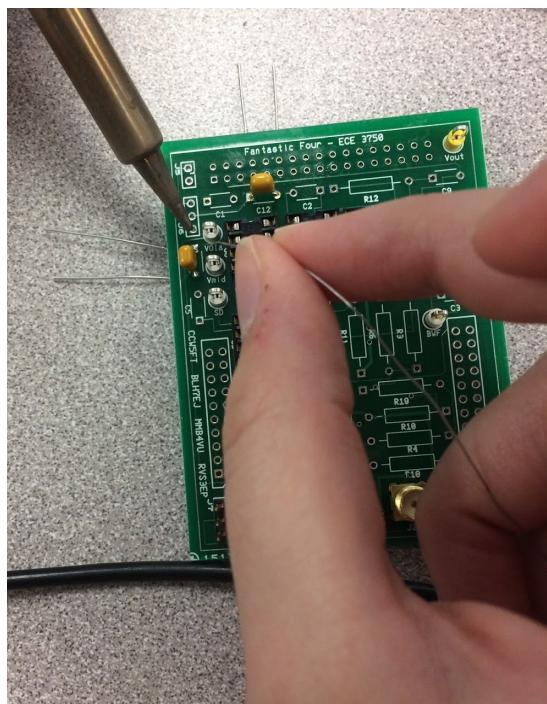


Figure 21: Soldering action shot 1

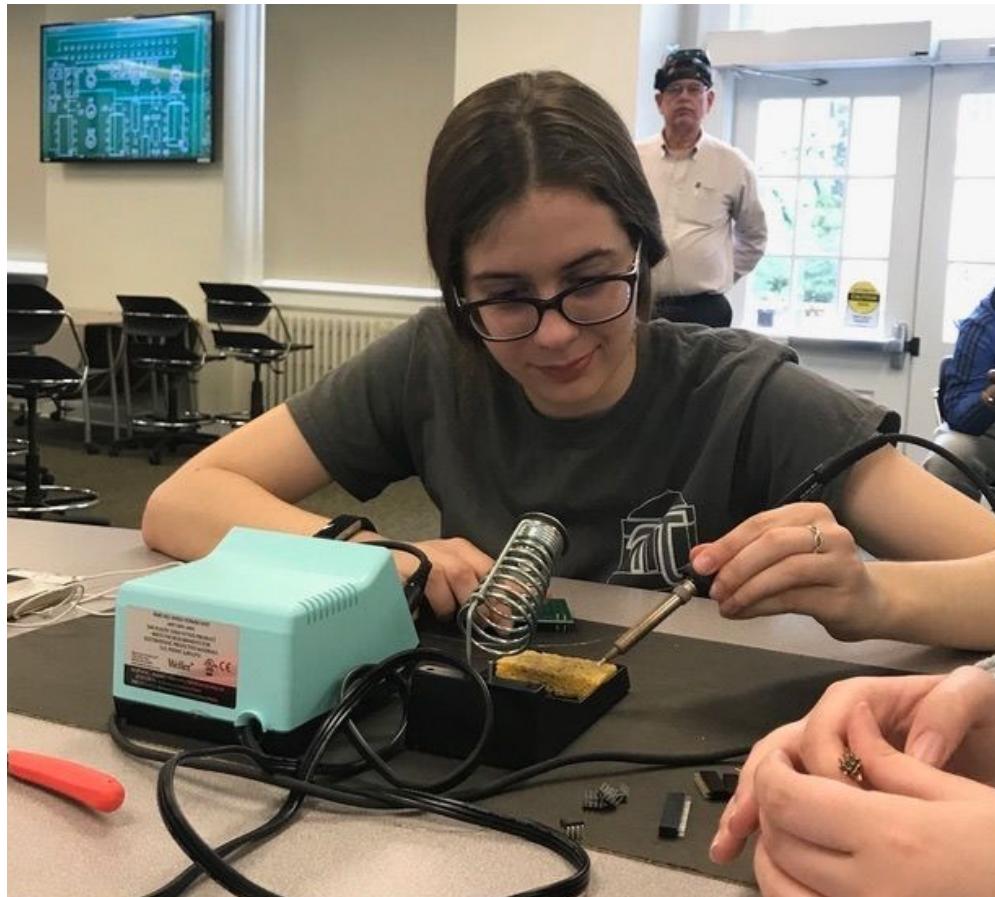


Figure 22: Soldering action shot 2



Figure 23: Soldering action shot 3

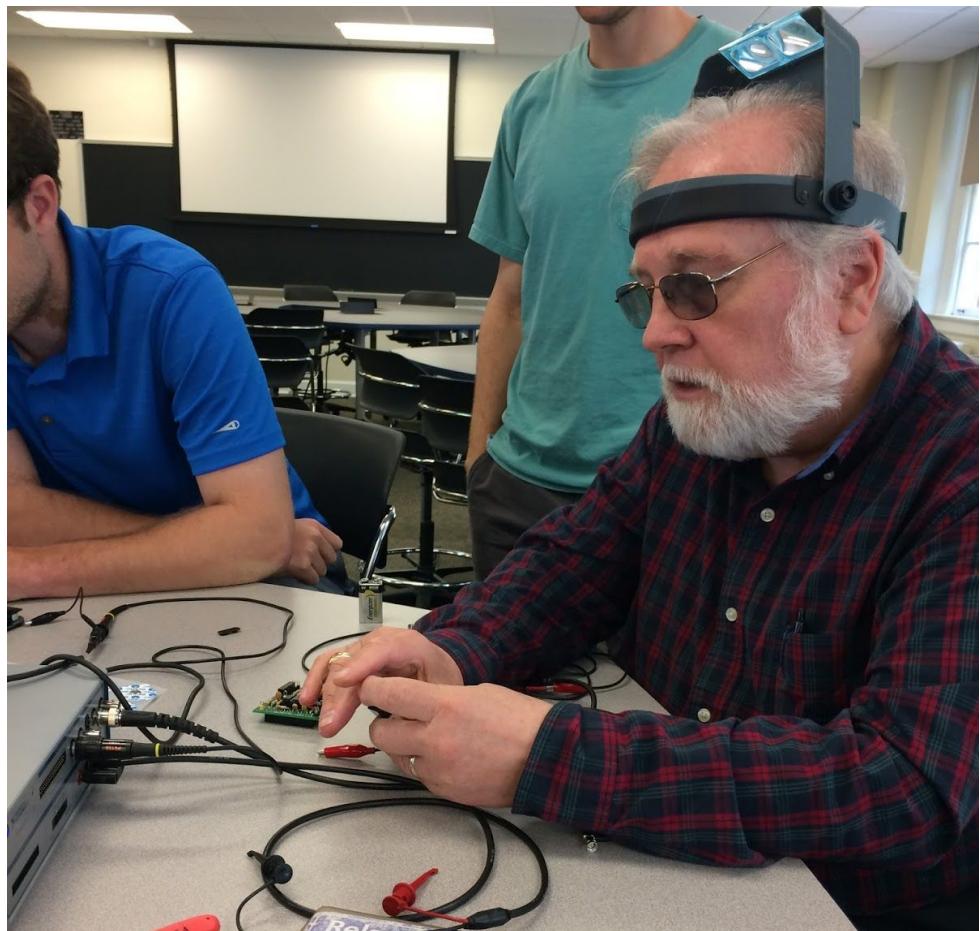


Figure 24: Debugging action shot

4.2 Test Setup

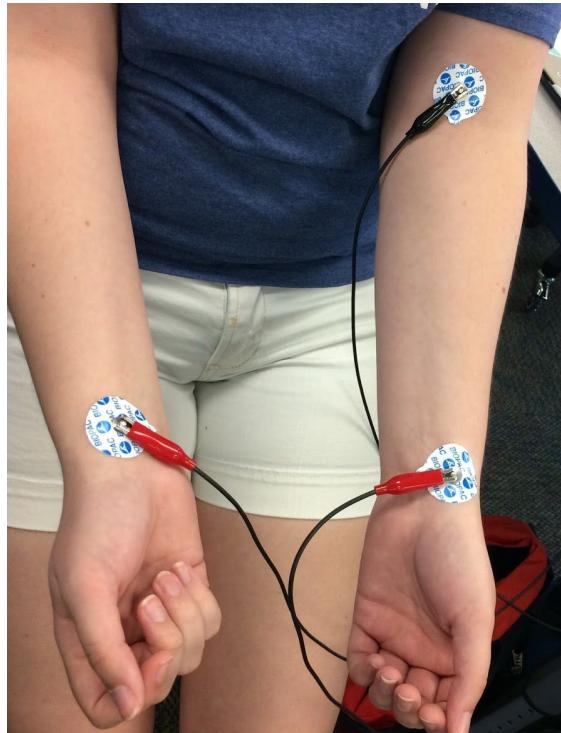


Figure 25: Final Test Setup 1

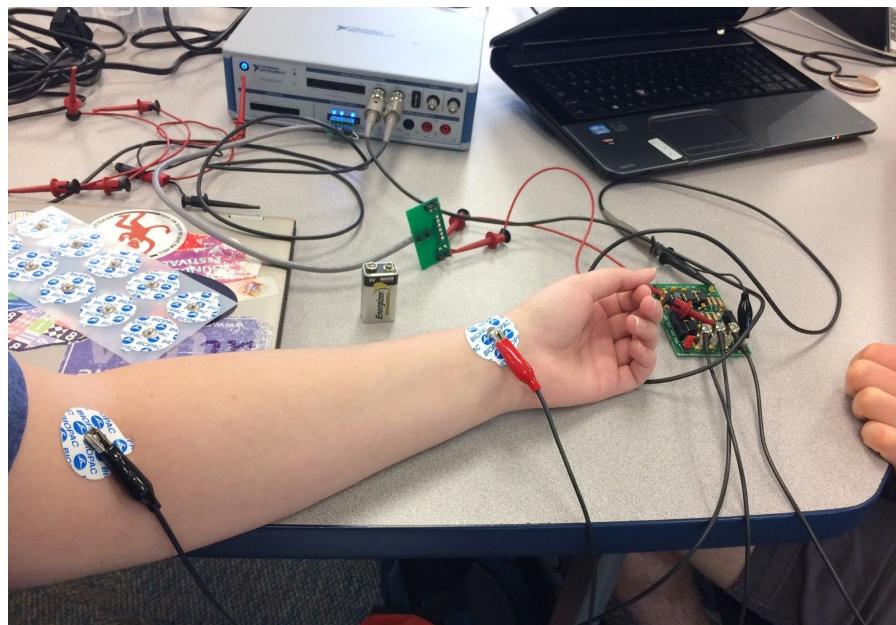


Figure 26: Final Test Setup 2

4.3 Board

Below is the final board with each component correctly soldered onto the board and the operational amplifiers, instrumentation amplifier, and 3.3V regulator all plugged into their respective sockets.

The components were all soldered facing the same orientation (resistors with the gold on the bottom or left, test points facing horizontally) to ensure the cleanest design possible. On the back side, as well as on top of the front side, all of the components were soldered with the least amount of solder necessary to fill the holes. This was both to ensure cleanliness as well as ensure that none of the components were shorted by touching solder points.

The two header board on the front side were supposed to go onto the back side to ensure an easier fit between the board and the MSP430, but unfortunately this was not done and attempts to desolder the points was unsuccessful. Though the MSP430 was not needed for this project, if any of the designers were to use it later, additional header board may be added on top of the two existing header boards to create room for the MSP430.

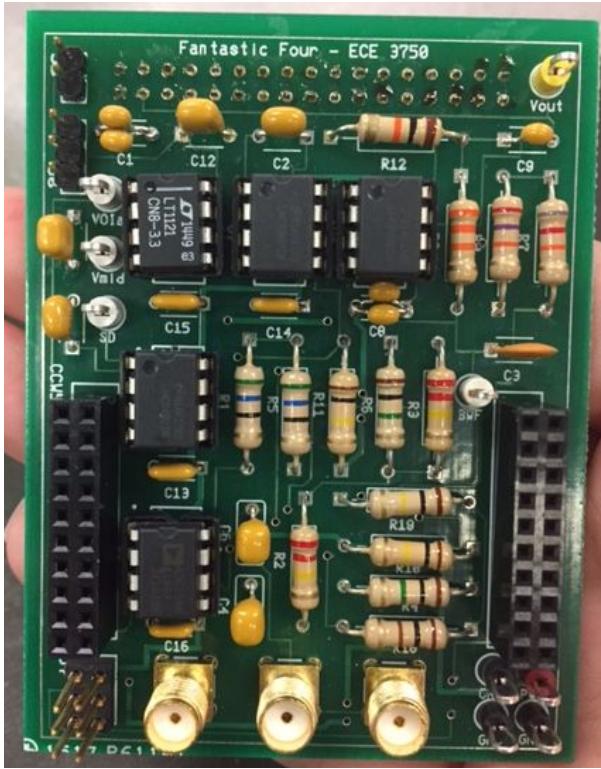


Figure 27: Final EKG Board - Front

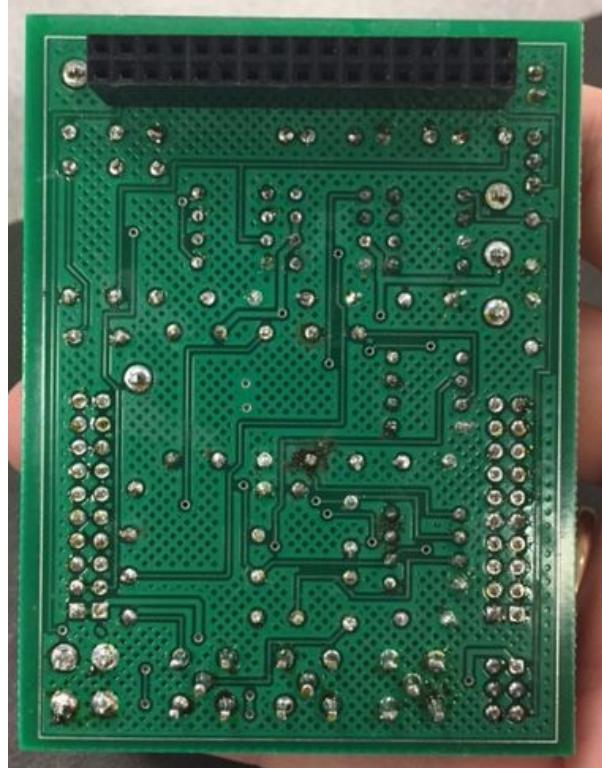


Figure 28: Final EKG Board - Back

4.4 VirtualBench Screenshots

The first test we ran is to build the fourth order Butterworth filter on a breadboard with the components that are going to be used on the PCB and verify that the board works correctly. The first test that was run is to verify that the output signal at 0.1 Vpp and 10 Hz is correct. This is shown in the screenshot below.

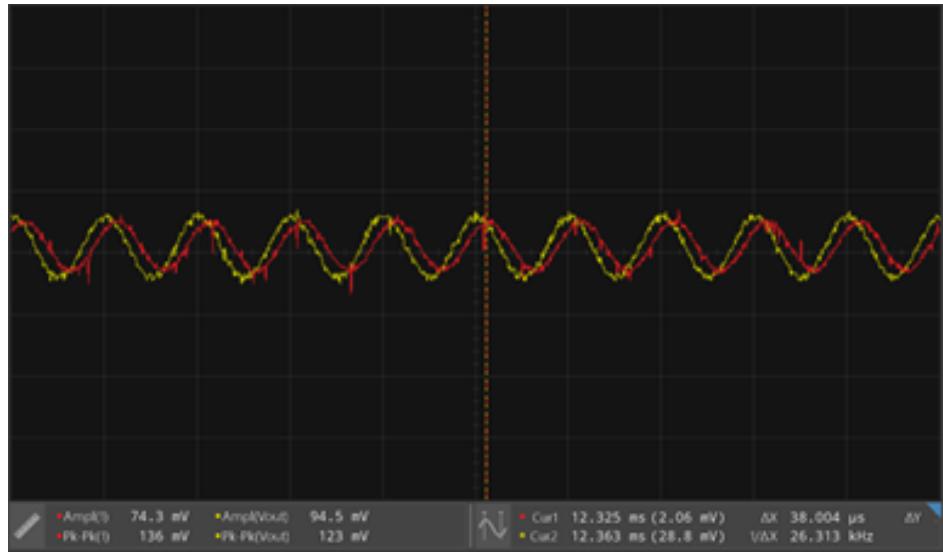


Figure 29:: verifying output signal, 100mV/Div, 100ms/Div

The Amplitude of the wave is 0.074 mV, which verifies with the expected value. The next component of the Butterworth filter that was tested is the amplitude of the output waveform with the 0.2 Vpp at 10 Hz input. The screenshot for this is shown below:

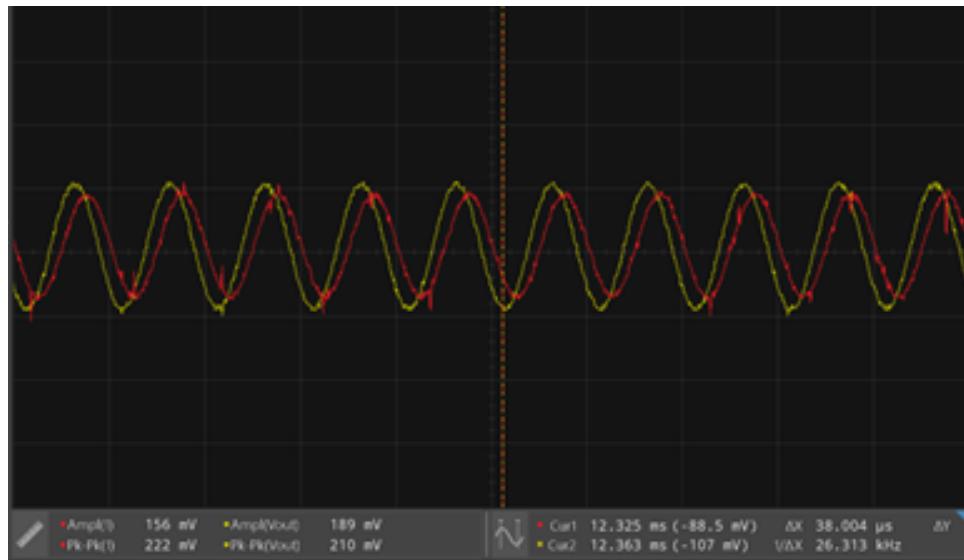


Figure 30: Verifying Butterworth output 100mV/Div, 100ms/Div

The output wave form shows an amplitude of 0.156 mV, which shows that for these components for the Butterworth, the filter output is scaling appropriately with the output.

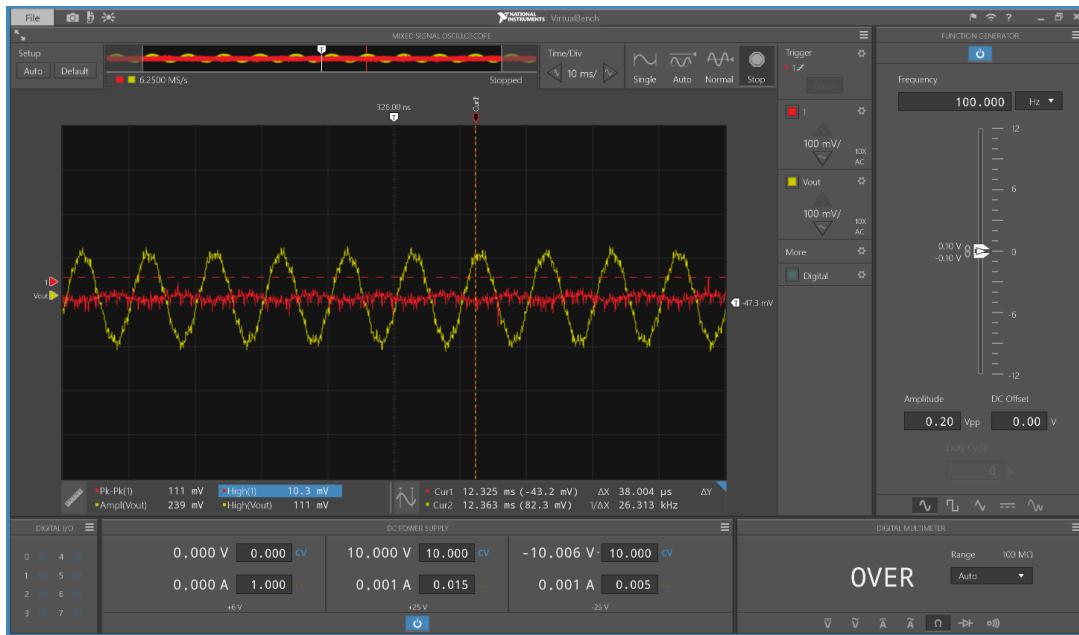


Figure 31: Verifying Butterworth output 100 Hz, 100 mV/div, 10 ms

The next figure, shown above, provides the Butterworth output verified at 100 Hz frequency. The output is producing the expected values for a filter according to the specifications. The filter was also verified at 1000 Hz, as shown below, and successfully found to be adequate for the EKG project.



Figure 32: Verifying Butterworth output 1000 Hz, 100 mV/div, 2 ms

The next Virtual Bench Verification is the 3.3 Volt Regulator. The voltage was supposed to be at 3.3 V, and the following screenshot verifies that the output is at 3.3 Volts as shown on the digital multimeter.

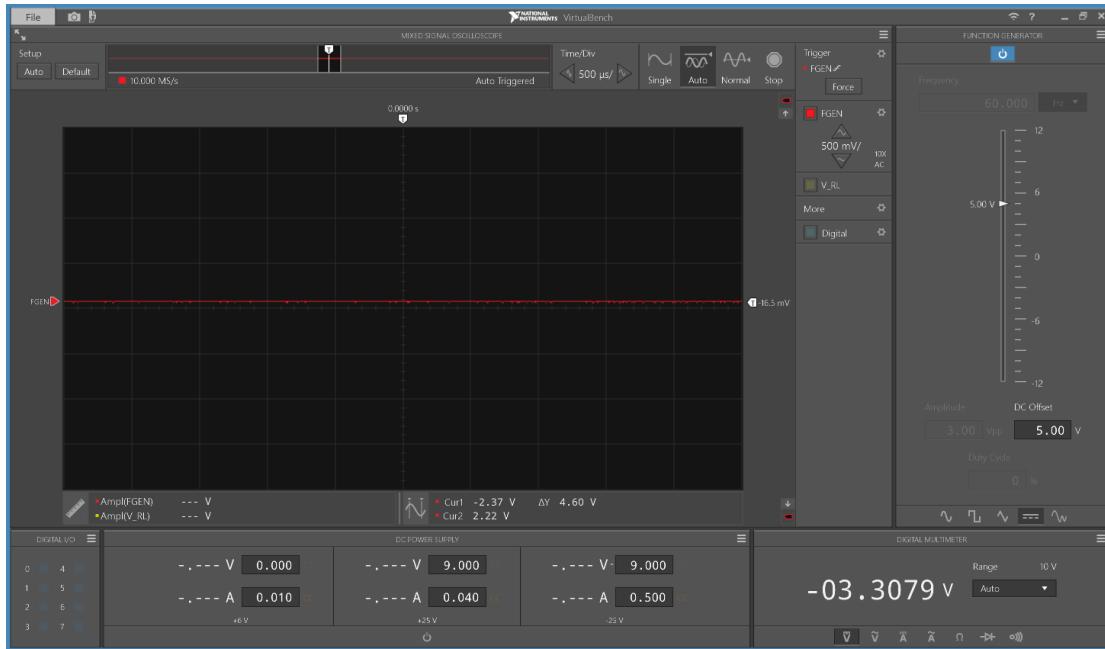


Figure 33: Verifying Regulator at 3.3 Volts

The regulator was also verified at 5 Volts, and the value is shown on the digital multimeter below:

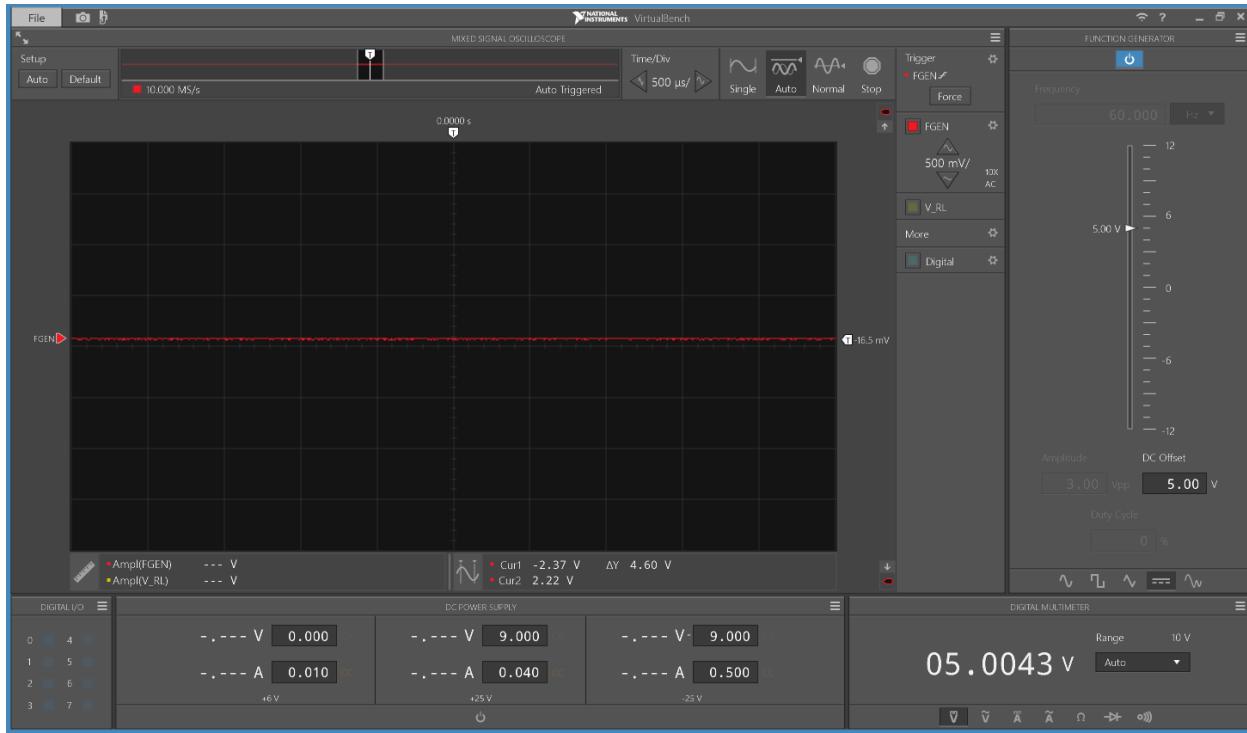


Figure 34: Verifying Regulator at 5 Volts

The 3.3 Volt regulator was also verified across C7, and the results of that verification are shown in the image below:

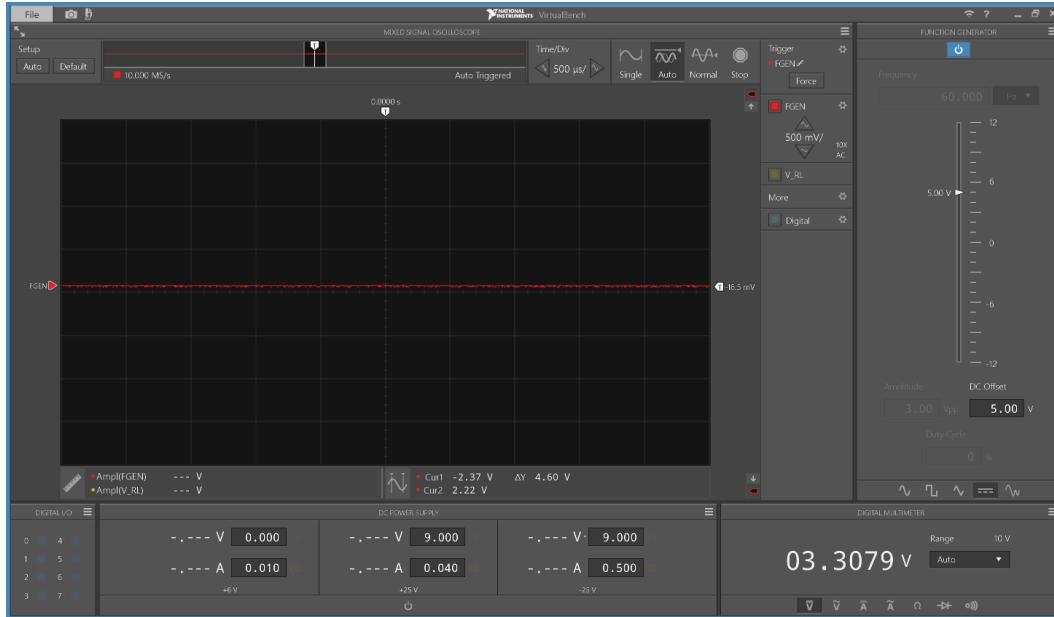


Figure 35: Verification of Regulator Across C7 at 3.3 V

The test pin J7 was tested to ensure that it also met the 3.3 Volt requirement and it did. The

Virtual Bench image for this test is below:

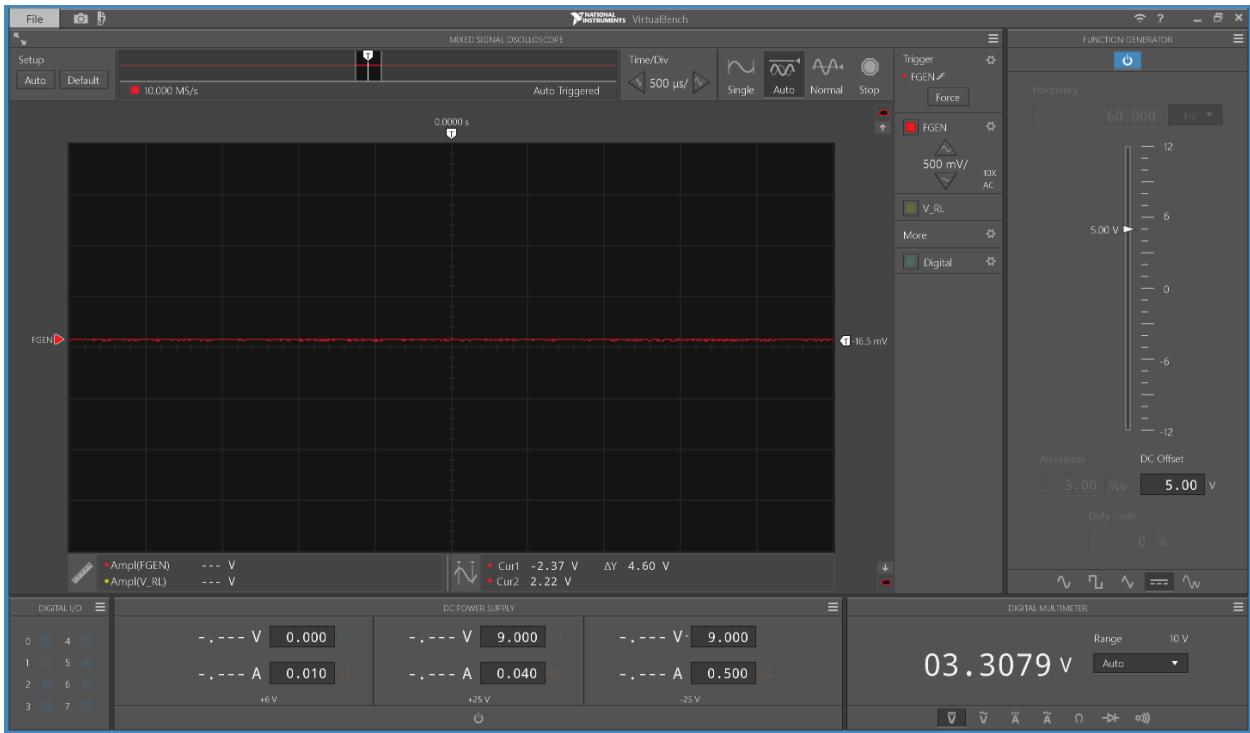


Figure 36: Verification of Regulator at Test Point J7 at 3.3 V

Next, V_{mid} was verified at 1.65 Volts. This is shown in the digital multimeter picture below, which verifies that 1.65 volts is the correct voltage at V_{mid} :

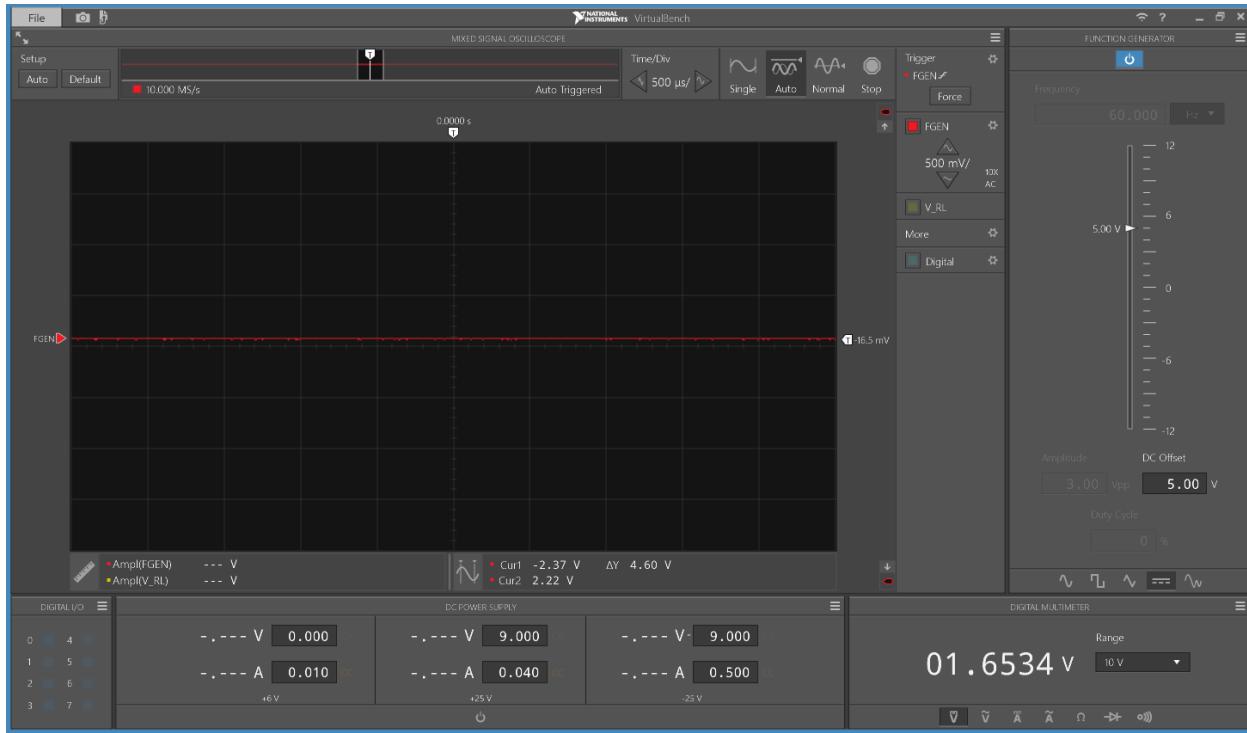


Figure 37: Verification of V_{mid} at 1.65 Volts

The Butterworth Filter response was the last piece tested. Shown below is the Butterworth Filter response, with the correct amplitude verified as shown in the snapshot:

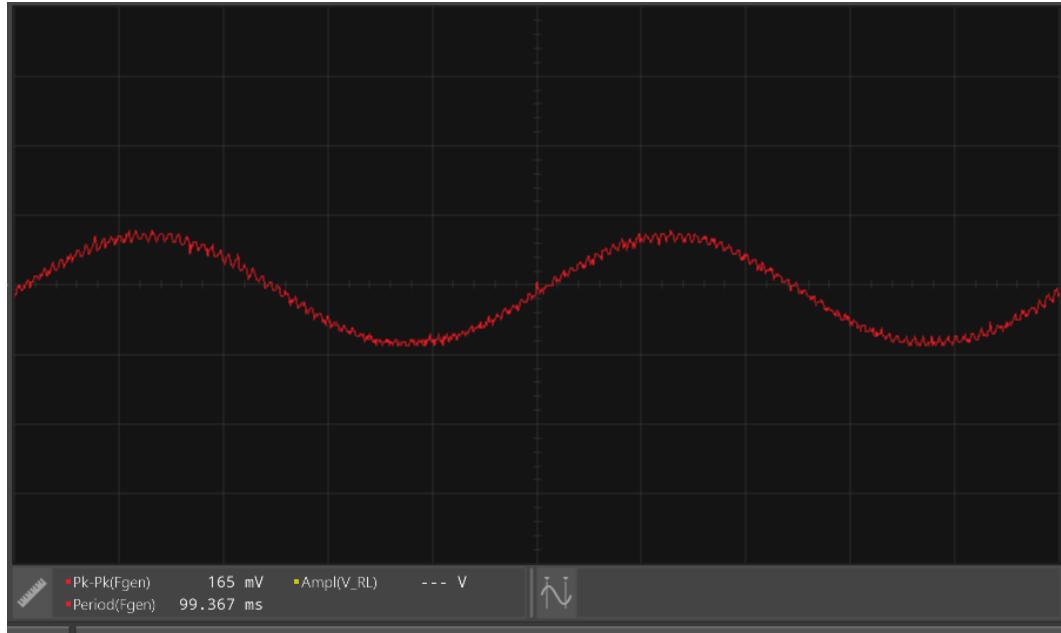


Figure 38: Verification of Butterworth Filter at 10 Hz, 100mV/Div, 20ms/Div

The Butterworth Filter was then tested at 100 Hz in order to verify that it is functioning correctly. This test is shown here:

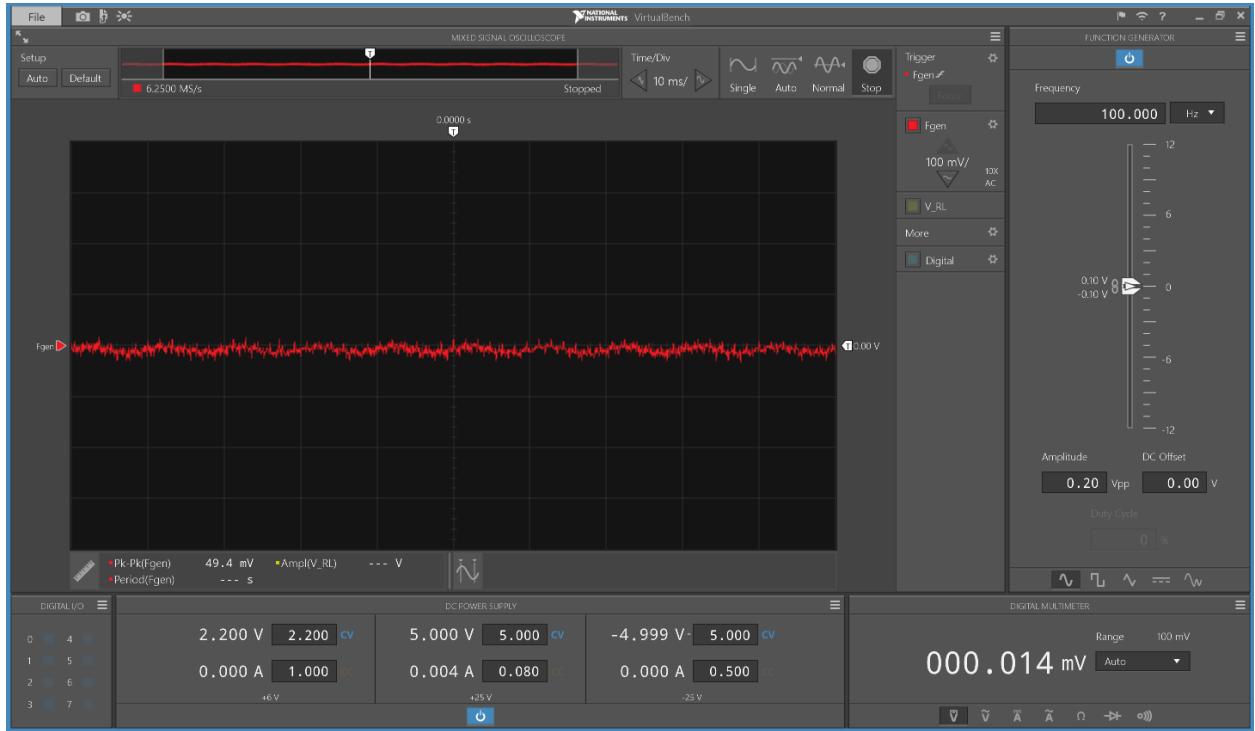


Figure 39: Verification of Butterworth Filter at 10 Hz, 100mV/Div, 20ms/Div

After all of these tests, a heartbeat was tested. Provided below are two heartbeats. One is the noisy heartbeat, showing the lack of the signal. The other is the actual heartbeat for testing, which verifies that a working EKG was built by the project group.

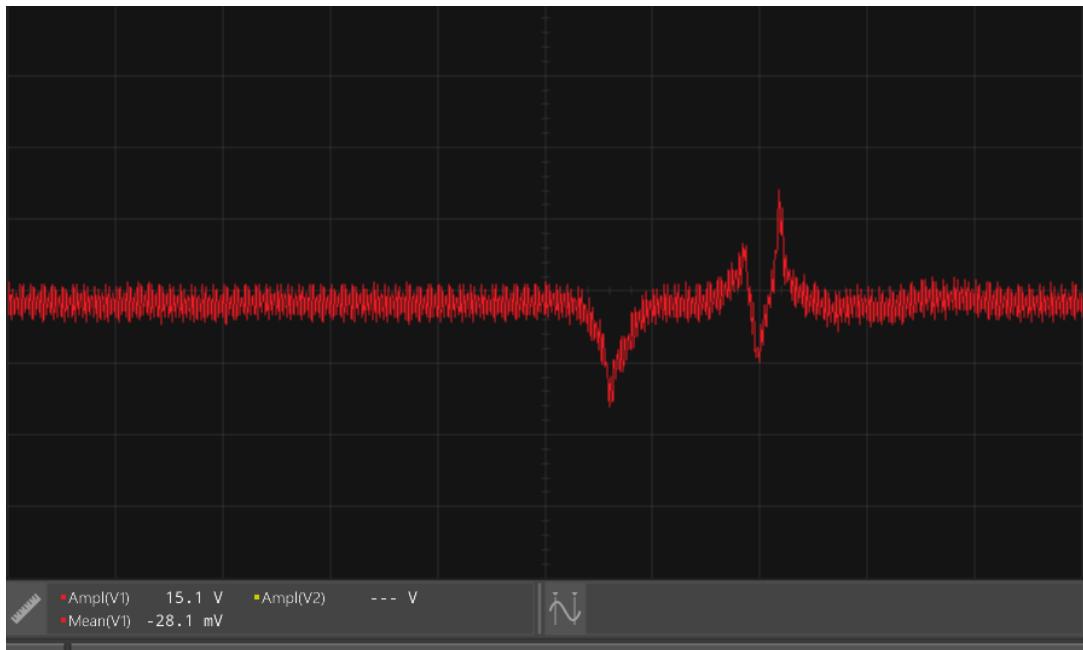


Figure 40: A Noisy Heartbeat Signal, 1V/Div, 500ms/Div



Figure 41: Accurate Heartbeat, Verification EKG works, 1V/Div, 500ms/Div

5 Conclusions

5.1 Future Project Improvement

Some improvements could be made in the future in order to ensure that the project runs more smoothly. From a personal standpoint, the project board used in the design for the EKG was not as reliable as was expected. This is because, in looking back over the design, there were a few areas in the design that could have been better optimized to produce a better result. For one thing, the resistor R4 was placed very far away from the integrator which it was supposed to work with, which could have led to some voltage drop. Additionally, the trace connecting the operational amplifier to this resistor, and some of the other traces were very thin, and this made the board highly susceptible to shorts, or burning out the traces.

Also, throughout the process, a few mistakes were made in terms of putting resistors or other components onto the board in the incorrect place or misaligned in the proper socket. It would be helpful in the future to have the solderer verify the location of the pieces with the group before completing the final solder. Lastly, the project could be improved for the class as a whole by spending more time verifying and testing each individual portion of the circuit. This would have saved time later on when the group spent 5-6 hours trying to debug the circuit. Certain parts of the circuit such as the Butterworth Filter and other parts could have been tested independently more to explore the characteristics. Overall, the project did a great job on involving all the various aspects of the class together to create a cohesive final project that made all of the concepts come together for the class.

Appendix A: Calculations

To actually calculate the values for the Butterworth filter, the <http://sim.okawa-denshi.jp/en/OPseikiLowkeisan.htm> website was used, which was posted on the Collab site. Before discovering this site, Brad created a Mathematica program that looped through all possible component values and chose the closest values to the cutoff frequency of 1 KHz and Q values of 1.306 and 0.5411. The Mathematica file is seen below. It is comprised of four for loops that loop through all possible capacitor and resistor values in our circuit. If the component values minimize the difference between the component's cutoff frequency and the desired cutoff frequency and the component's Q value and the desired Q value, then it is stored as the best component value in the loop.

```

R = {820 k, 82 k, 8.2 k, 680 k, 68 k, 6.8 k, 560 k, 56 k, 5.6 k
c = {0.001 u, 0.0047 u, 0.01 u, 0.047 u, 0.02 u, 0.1 u, 1 u, 4

Q1 = 1.306 *100;
Q2 = 0.5411 *100;

dQ1Min = 100;
dQ2Min = 100;
W = 99;
Q = 76;
x = 1;
y = 1;
w = 1;
z = 1;

Do[
  Do[
    Do[
      Do[
        W = N[1 / (R[[x]] R[[y]] c[[z]] c[[w]])];
        Q = N[1 / (R[[x]] c[[z]]) + 1 / (R[[y]] c[[z]])];
        dQ1 = (Abs[100 - W] + Abs[Q1 - Q]);
        If[dQ1 < dQ1Min,
          R1Q1 = R[[x]];
          R2Q1 = R[[y]];
          C1Q1 = c[[z]];
          C2Q1 = c[[w]];
          dQ1Min = dQ1;
          , 0
        ];
      ];
    ];
  ];
];

```

```

dQ2 = Abs[100 - W] + Abs[Q2 - Q];
If[dQ2 < dQ2Min,
  R1Q2 = R[[x]];
  R2Q2 = R[[y]];
  C1Q2 = c[[z]];
  C2Q2 = c[[w]];
  dQ2 = dQ2Min;
  , 0
]

, {x, 1, Length[Resistors]}]
, {y, 1, Length[Resistors]}]
, {z, 1, Length[Capacitors]}]
, {w, 1, Length[Capacitors]}]

Print[R1Q1]
Print[R2Q1]
Print[C1Q1]
Print[C2Q1]
Print[R1Q2]
Print[R2Q2]
Print[C1Q2]
Print[C2Q2]
N[1 / (R1Q1 R2Q1 C1Q1 C2Q1)]
N[1 / (R1Q1 C1Q1) + 1 / (R2Q1 C1Q1)]
N[1 / (R1Q2 R2Q2 C1Q2 C2Q2)]
N[1 / (R1Q2 C1Q2) + 1 / (R2Q2 C1Q2)]

```

Figure 42: Mathematica Calculation of Component Values