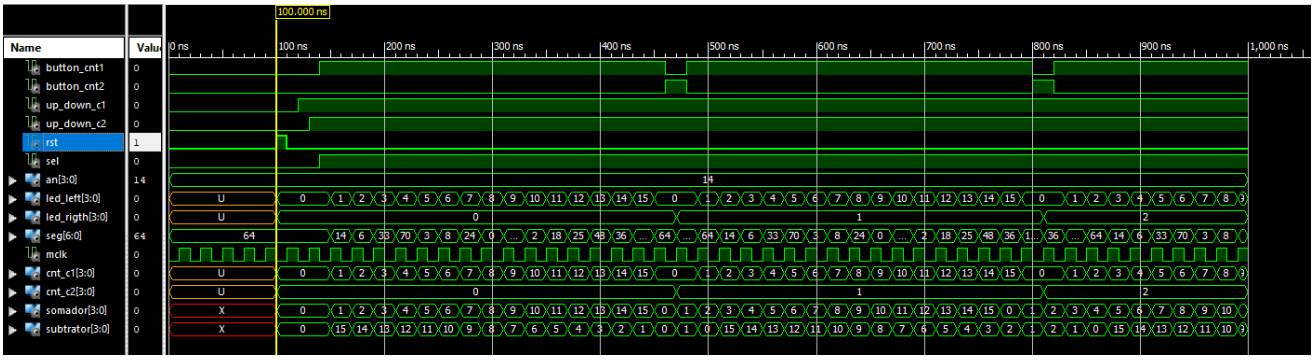
Universidade Federal do Rio Grande do Sul
Instituto de Informática
Departamento de Informática Aplicada
INF01175 – Sistemas Digitais para Computação

Trabalho 1
Somador e Subtrator 4bits

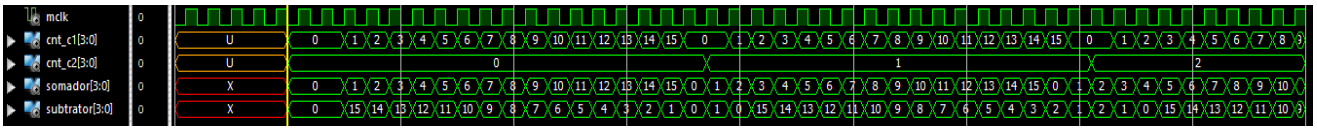
Cássio Miguel Entrudo

Porto Alegre, 10 de outubro de 2017

Imagem do testbench contendo todos os sinais importantes:



Aqui podemos verificar os contadores cnt_1 e cnt_2 e os registradores somador e subtrator alterando seus valores a cada borda de clock.



Informações:

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	24	1,920	1%	
Number of 4 input LUTs	32	1,920	1%	
Number of occupied Slices	27	960	2%	
Number of Slices containing only related logic	27	27	100%	
Number of Slices containing unrelated logic	0	27	0%	
Total Number of 4 input LUTs	33	1,920	1%	
Number used as logic	32			
Number used as a route-thru	1			
Number of bonded IOBs	26	83	31%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	3.20			

```
=========================================================================
*                            HDL Synthesis                              *
=========================================================================

    Found 16x7-bit ROM for signal <saida_7bits>.
    Found 4-bit updown counter for signal <cnt_c1>.
    Found 4-bit updown counter for signal <cnt_c2>.
    Found 8-bit register for signal <reg1>.
    Found 8-bit register for signal <reg2>.
    Found 4-bit subtractor for signal <subtrator>.
    Summary:
    inferred   1 ROM(s).
    inferred   2 Counter(s).
    inferred  16 D-type flip-flop(s).
    inferred   1 Adder/Subtractor(s).
Unit <trabalho1> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# ROMs                                                 : 1
 16x7-bit ROM                                          : 1
# Adders/Subtractors                                   : 1
 4-bit subtractor                                      : 1
# Counters                                             : 2
 4-bit updown counter                                  : 2
# Registers                                            : 16
 1-bit register                                        : 16

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# ROMs                                                 : 1
 16x7-bit ROM                                          : 1
# Adders/Subtractors                                   : 1
 4-bit subtractor                                      : 1
# Counters                                             : 2
 4-bit updown counter                                  : 2
# Registers                                            : 16
 Flip-Flops                                            : 16
```

```
================================================================================
*                            Final Report                                      *
================================================================================

Clock Information:

   Minimum period: 4.262ns (Maximum Frequency: 234.632MHz)
   Minimum input arrival time before clock: 3.819ns
   Maximum output required time after clock: 10.083ns
   Maximum combinational path delay: 8.330ns

================================================================================

Design Summary:
Number of errors:      0
Number of warnings:    0
Logic Utilization:
  Number of Slice Flip Flops:            24 out of   1,920    1%
  Number of 4 input LUTs:                32 out of   1,920    1%
Logic Distribution:
  Number of occupied Slices:             27 out of     960    2%
    Number of Slices containing only related logic:      27 out of      27 100%
    Number of Slices containing unrelated logic:          0 out of      27   0%
      *See NOTES below for an explanation of the effects of unrelated logic.
  Total Number of 4 input LUTs:          33 out of   1,920    1%
    Number used as logic:                32
    Number used as a route-thru:          1
```