Contact

cassiofragadantas@gmail.com

www.linkedin.com/in/cassio-dantas (LinkedIn)

Top Skills

Signal Processing
Machine Learning
Python

Languages

French (Full Professional)
English (Full Professional)
Portuguese (Native or Bilingual)

Certifications

Internet History, Technology, and Security
Machine Learning
Circuits and Electronics
Fondamentaux pour le Big Data
Artificial Intelligence Planning

Honors-Awards

Graduation with Highest Honors

Cassio F. Dantas

PhD Candidate at INRIA & Université de Rennes 1
Brittany

Summary

I obtained a double degree in Electrical Engineering at University of Campinas (Bachelor) and École Polytechnique in 2014 and a Master's degree from University of Campinas in 2016. I also have three years of R&D experience at Idea! Electronic Systems, UPMC and Schneider Electric.

Currently, I am a PhD candidate at Inria and Univerité de Rennes 1. My recent research activities lie on the frontier between signal processing and machine learning. More precisely, on sparsity-constrained inverse problems.

Experience

Inria
PhD Researcher
October 2016 - Present (4 years 6 months)
Rennes, France

- Domain: Signal processing and Machine Learning
- Brief description: Accelarating convex optimization algorithms for high-dimensional sparse regression problems.
- Supervisor: Rémi Gribonval

Idea! Electronic Systems
Digital Communications Engineer
January 2014 - December 2015 (2 years)

Research, Development and Modelling of physical layer algorithms (equalization/synchronization/coding) for digital communication systems. ISDB-Tb Demodulator.

University P.Curie UPMC-Paris6
Design Engineer
February 2013 - July 2013 (6 months)

LIP6 (Paris 6 Informatics Laboratory) System on Chip department.

VHDL implementation of a multi-channel Ethernet Medium Access Controller (MAC), following the IEEE 802.3 standard.

Laboratoire d'Informatique de Paris 6
Internship
April 2012 - August 2012 (5 months)

Collaborated on TSAR (Tera-Scale ARchitecture) project, a European project in cooperation with BULL Company for defining a scalable, coherent shared memory, multi-core architecture, and developing its virtual prototype. I worked on defining, modeling in SystemC and integrating to the current architecture a dedicated Network on Chip to interface with DMA peripherals.

Schneider Electric
Internship
July 2011 - August 2011 (2 months)
Pacy sur Eure, France

Worked on the product cost estimation on a starting project of variable speed drives. Developed an estimation tool for Excel (using VBA routines) to electronic components on the product.

3e Unicamp
Administrative and Financial Manager
March 2008 - December 2009 (1 year 10 months)

Voluntary work at JUNIOR ENTERPRISE 3E UNICAMP. Analyzed and developed contracts and internal documents. Cash flow measurement and forecasting. Learned notions of accountancy.

Education

Université de Rennes I
Doctor of Philosophy - PhD, Computational and Applied Mathematics · (2016 - 2019)

Universidade Estadual de Campinas
Master’s Degree, Signal Processing · (2015 - 2016)

École Polytechnique
Cycle Polytechnicien, Ingénierie · (2010 - 2012)

Universidade Estadual de Campinas

Graduation, Electrical Engineering · (2008 - 2014)