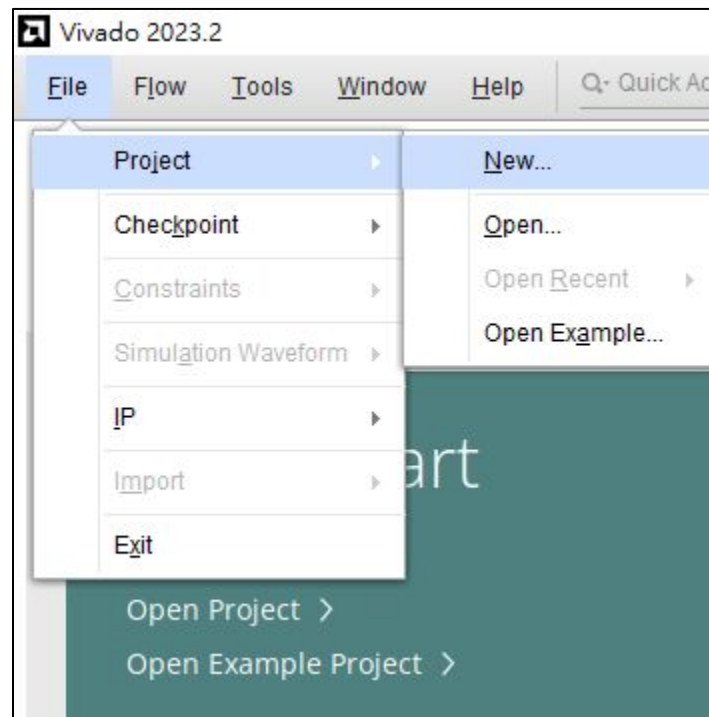


Lab 0

Create a Project in Vivado &
Do a Verilog Practice

Create New Project (1/4)

- Create a new project.



Create New Project (2/4)

- Fill in Project name and Project location.

Project Name






Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

Project location:

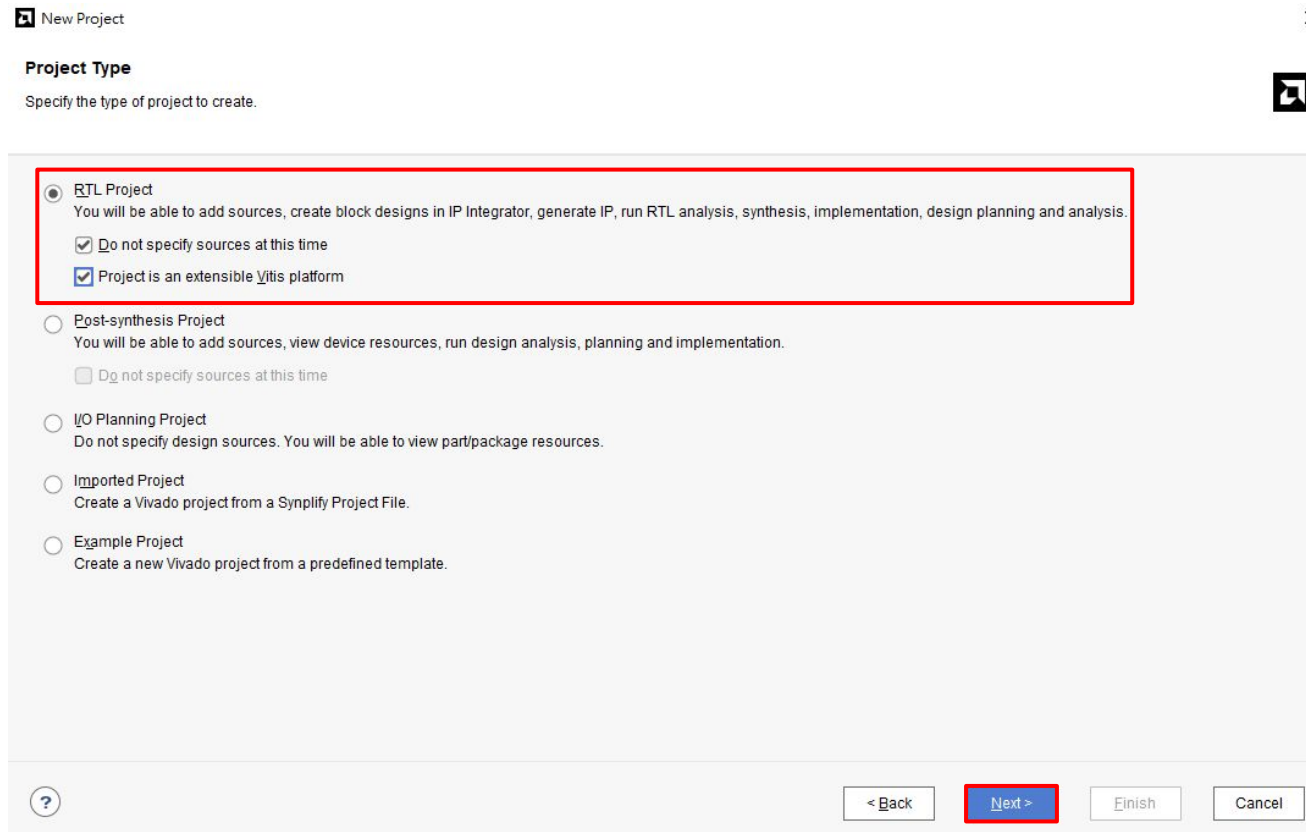
☒ Create project subdirectory

Project will be created at: D:/NYCU_EDA_LAB/ComputerOrganization112_2/Lab0

Create New Project (3/4)

- Choose RTL Project.



New Project

Project Type

Specify the type of project to create.






☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
☒ Do not specify sources at this time
☒ Project is an extensible Vitis platform

☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.
☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.


☐ **Imported Project**
Create a Vivado project from a Synplify Project File.


☐ **Example Project**
Create a new Vivado project from a predefined template.

Create New Project (4/4)

- Select parts(boards) arbitrarily since we don't have to implement the design on FPGA.

 New Project ✕

Default Part
Choose a default AMD part or board for your project. 

Parts | Boards

[Reset All Filters](#)

Category: All

Family: All

Package: All

Speed: All

Temperature: All

Static power: All

Search: Q-

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	BUFGs	Gb Transceivers	GTPE
xc7z007sc1g400-1	400	100	14400	28800	50	0	66	32	0	0
xc7z010clg225-3	225	54	17600	35200	60	0	80	32	0	0
xc7z010clg225-2	225	54	17600	35200	60	0	80	32	0	0
xc7z010clg225-1	225	54	17600	35200	60	0	80	32	0	0
xc7z010clg400-3	400	100	17600	35200	60	0	80	32	0	0
xc7z010clg400-2	400	100	17600	35200	60	0	80	32	0	0
xc7z010clg400-1	400	100	17600	35200	60	0	80	32	0	0
xc7z010clg225-1L	225	54	17600	35200	60	0	80	32	0	0
xc7z010clg400-1L	400	100	17600	35200	60	0	80	32	0	0

?

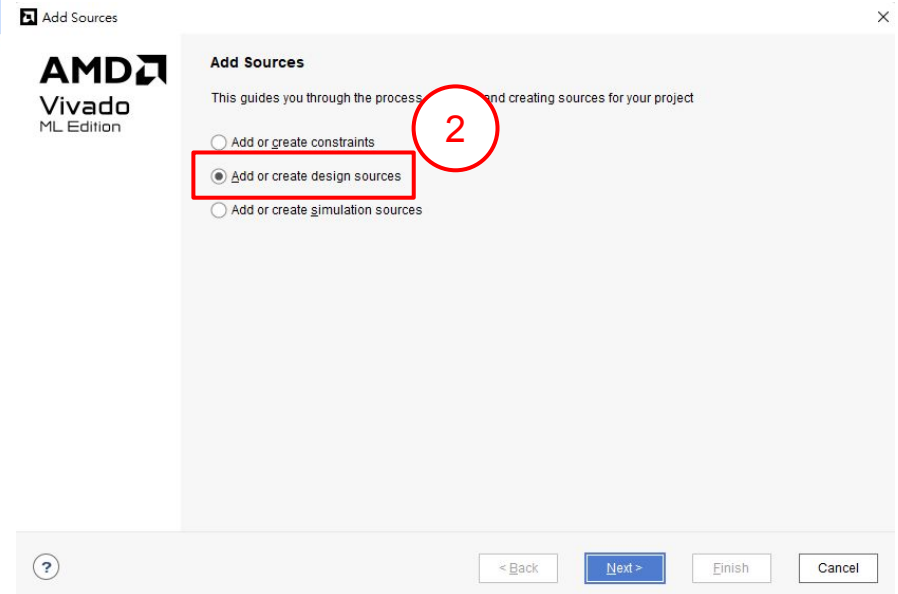
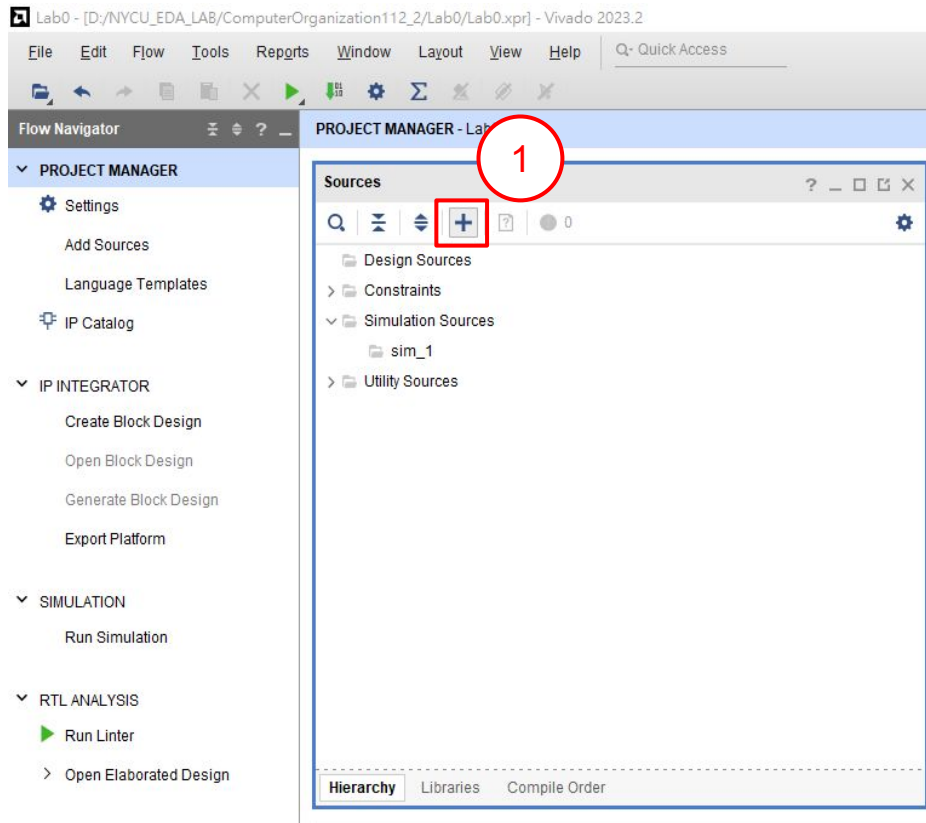
< Back

Next >

Finish


Cancel


Add Design Source (.v files) (1/2)



Add Design Source (.v files) (2/2)

- Add design sources
 - Not including testbench.v

 Add Sources ×

Add or Create Design Sources 

Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.

	Index	Name	Library	Location
●	1	full_subtractor.v	xil_defaultlib	D:/NYCU_EDA_LAB/ComputerOrganization112_2/Lab0/code
●	2	half_subtractor.v	xil_defaultlib	D:/NYCU_EDA_LAB/ComputerOrganization112_2/Lab0/code

1

Add Files

Add Directories

Create File

☐ Scan and add RTL include files into project
☐ Copy sources into project
☒ Add sources from subdirectories

?

< Back

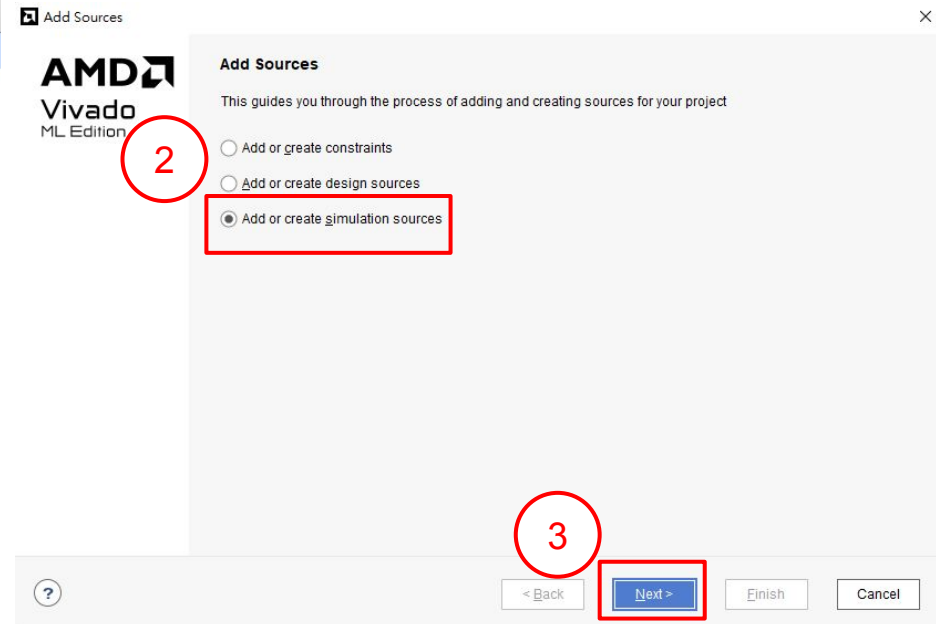
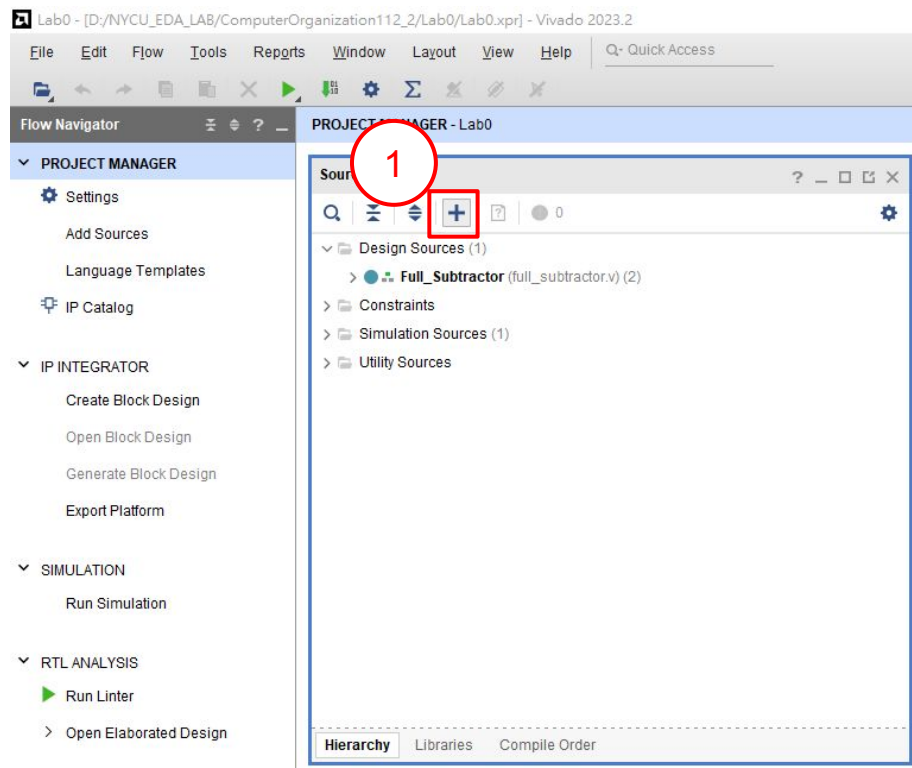
Next >

2

Finish


Cancel

Add Simulation Source (testbench.v) (1/2)




Add Simulation Source (testbench.v) (2/2)


- Add testbench.v

 Add Sources ✕

Add or Create Simulation Sources

Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project. 

Specify simulation set: sim_1

	Index	Name	Library	Location
	1	testbench.v	xil_defaultlib	D:/NYCU_EDA_LAB/ComputerOrganization112_2/Lab0/code

1

Add Files Add Directories Create File

☐ Scan and add RTL include files into project

☐ Copy sources into project

☒ Add sources from subdirectories

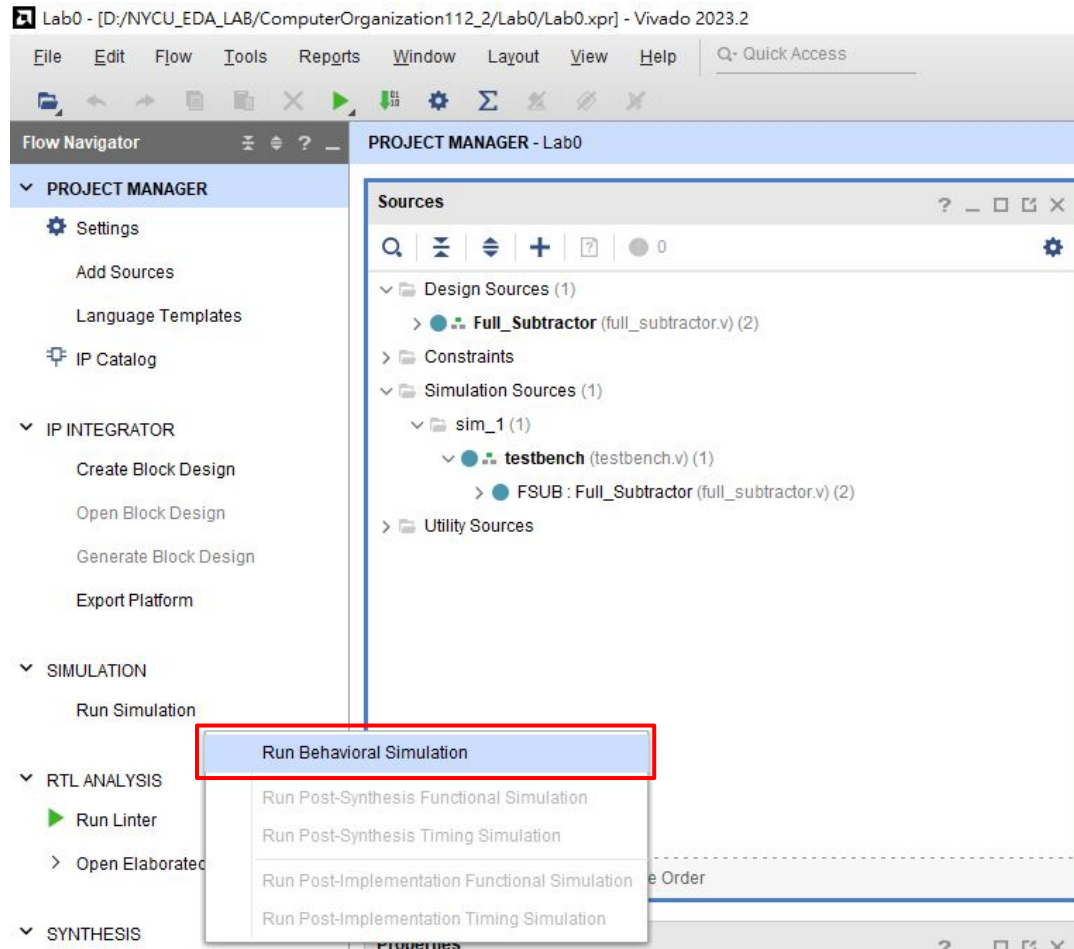
☒ Include all design sources for simulation

? < Back Next > **2** Finish Cancel

How to Run Simulation (1/2)

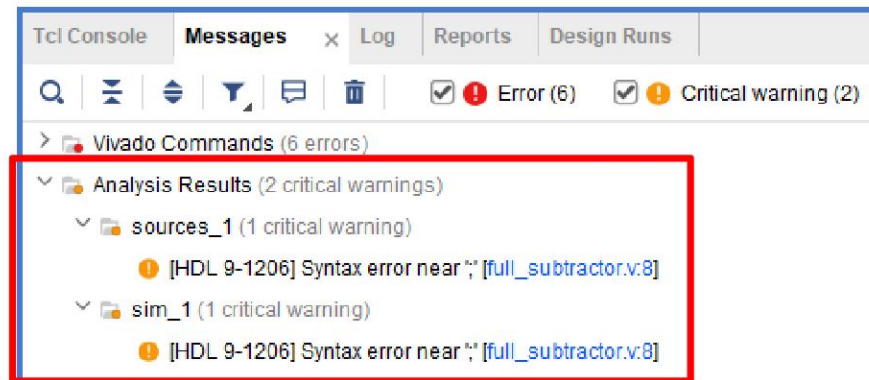
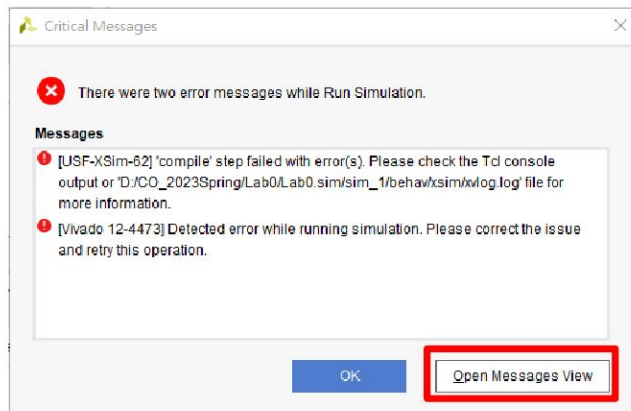
- After adding testbench into project, you can execute the behavioral simulation.
- It can help you debug with the signal waveform and check the correctness of your design.

How to Run Simulation (2/2)



Useful Information (1/3)

You can check out design error messages in Messages.

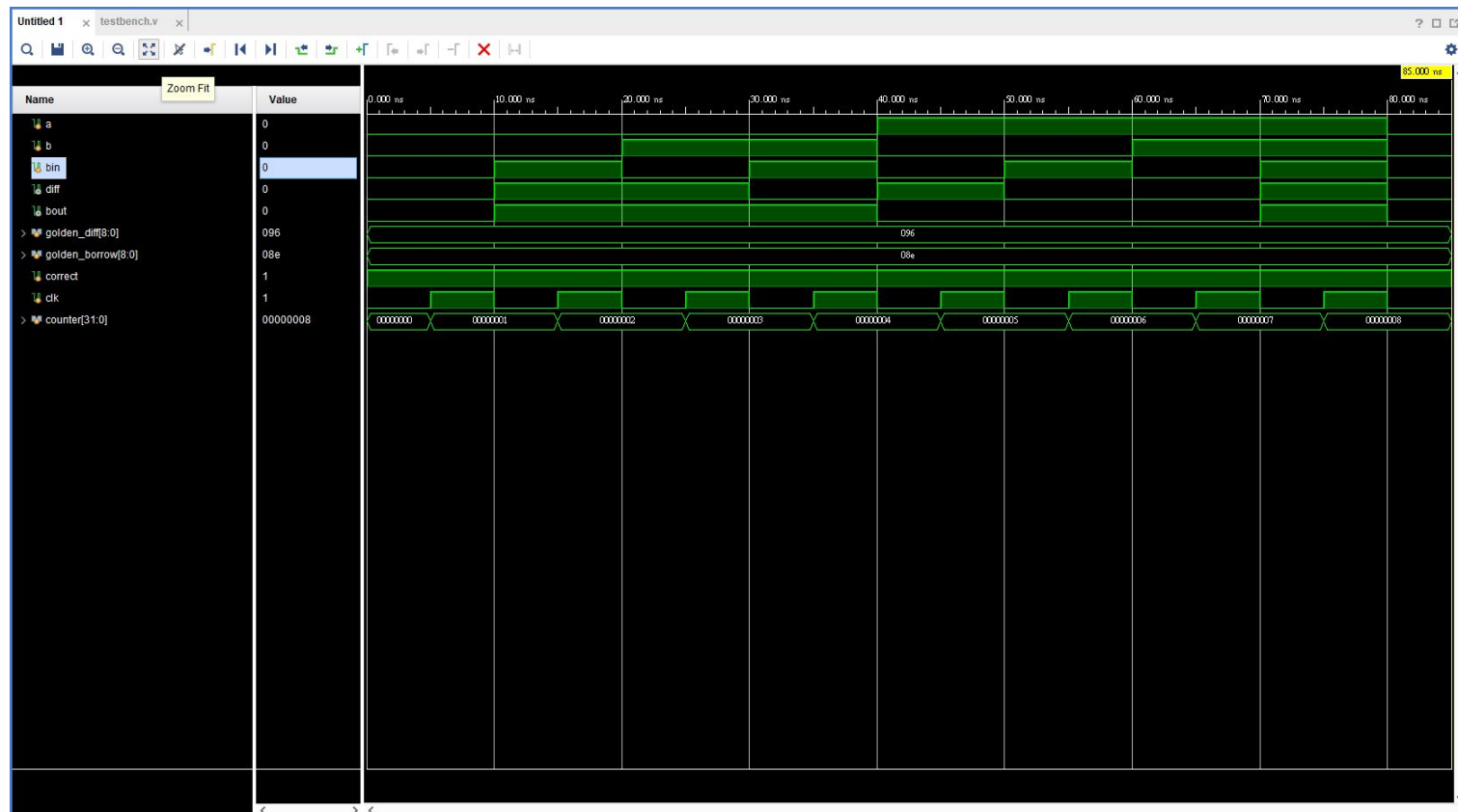


Possible design errors would be underlined in red.

```
module Full_Subtractor(  
    In_A, In_B, Borrow_in, Difference, Borrow_out  
);  
    input In_A, In_B, Borrow_in;  
    output Difference, Borrow_out;  
    wire ;
```

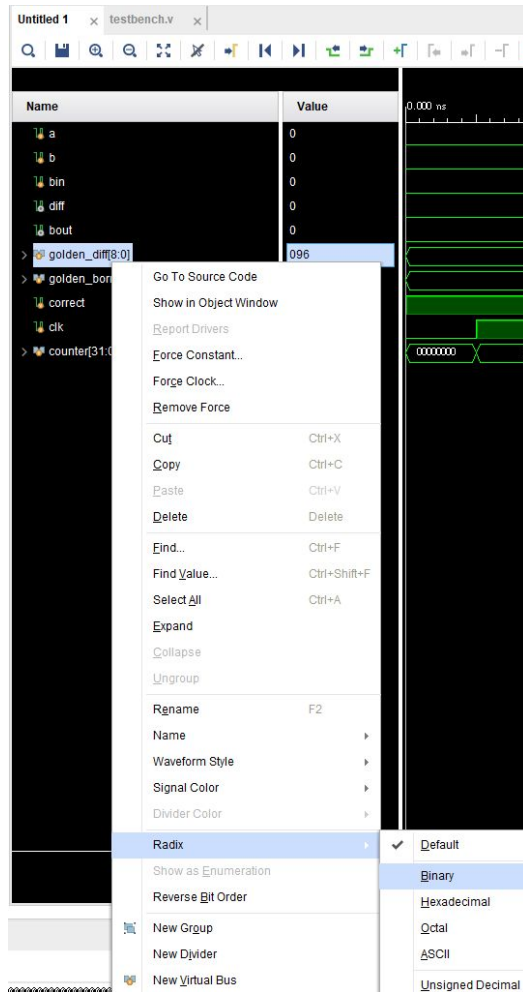
Useful Information (2/3)

- This button makes your complete waveform fit your window size.



Useful Information (3/3)

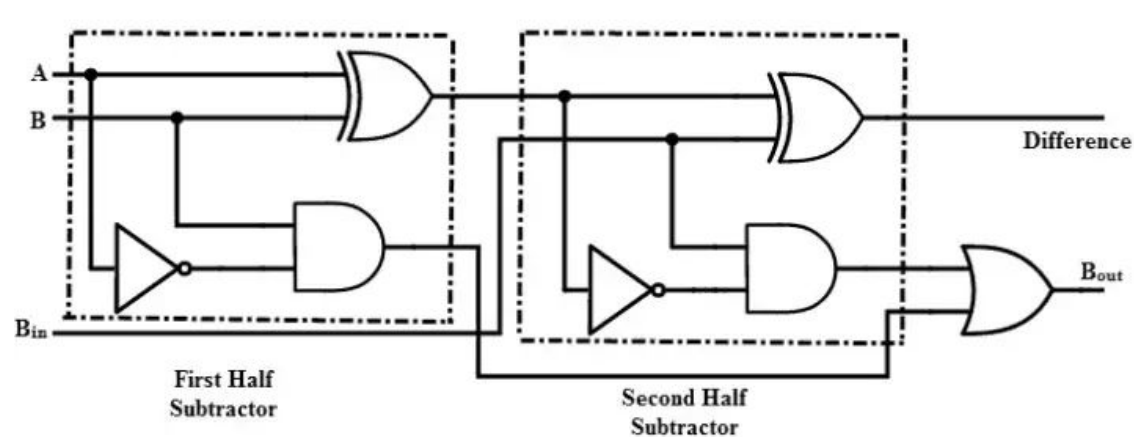
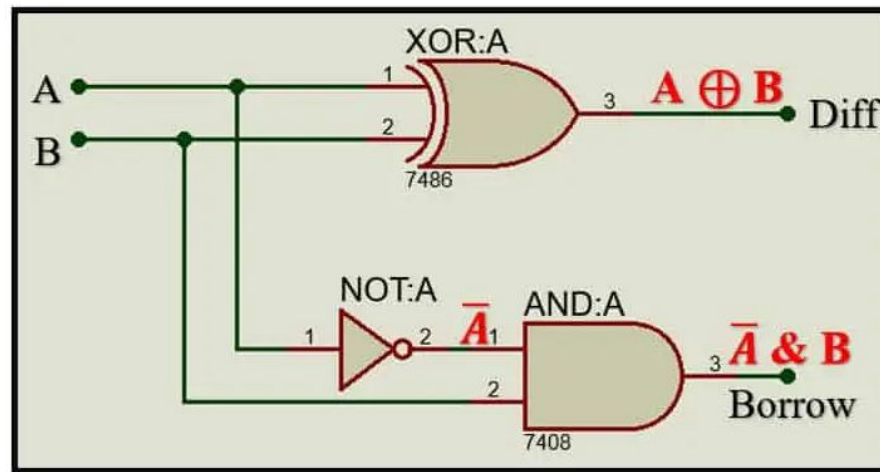
- You can change the radix of the signal. (default radix is decimal)



Lab0: Half Subtractor and Full Subtractor

- Implement the half subtractor and full subtractor without using '-' operation.
- We want you to practice how to implement the signal connection within the given circuit. We will give you example design sources and testbench.v.

Half Subtractor and Full Subtractor Circuit



Truth Table of Full Subtractor

A	B	Bin	Difference (D)	Borrow (Bout)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Verify the Correctness of Your Design

- We have enumerated all input cases in testbench.v.
- After simulation with our testbench.v, if your design is correct, you should find the message shown below in Tcl Console.

Tcl Console x Messages Log

Q Z A || [] [] []

```

*****

Congratulation! All data are correct!

*****

$finish called at time : 85 ns : File "D:/NYCU_EDA_LAB/ComputerOrganization112_2/Lab0/code/testbench.v" Line 153
INFO: [USF-XSim-96] XSim completed. Design snapshot 'testbench_behav' loaded.
INFO: INFO: XSim 021 XSim simulation was for 100ns

```

Note

- You don't have to submit anything in this lab.
- However, we recommend you to do this lab, so that you get familiar with Vivado and Verilog. Both of them would be used in future labs.

QA

- If you have any questions, feel free to ask on the Microsoft Teams discussion forum. Your questions may also be other people's questions.