電子學(一)　HW4

1. It is required to bias the MOS amplifier of Fig. 7.3 at point Q for which $V_{OV} = 0.2$ V and $V_{DS} = 1$ V. Find the required value of R_D when $V_{DD} = 5$ V, $V_{th} = 0.5$ V, and $k_n = 10$ mA/V^2. Also specify the coordinates of the VTC end point B. What is the small-signal voltage gain of this amplifier? Assuming linear operation, what is the maximum allowable negative signal swing at the output? What is the corresponding peak input signal?

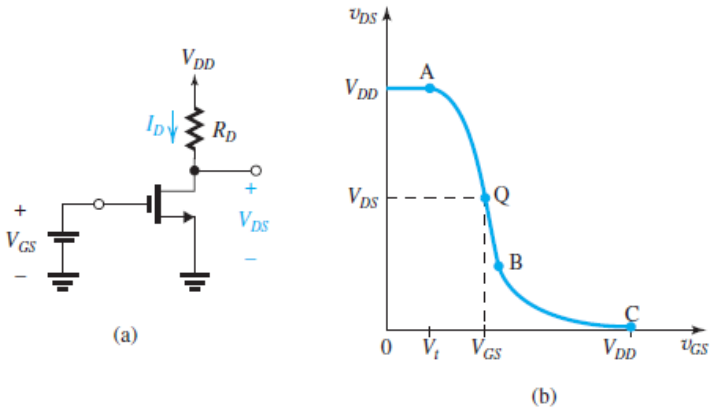


Fig. 7.3

2. Design the MOS amplifier of Fig. 7.4(a) to obtain maximum gain while allowing for an output voltage swing of at least ±0.5 V. Let $V_{DD} = 5$ V, and utilize an overdrive voltage of approximately 0.2 V.

(a) Specify V_{DS} at the bias point.

(b) What is the gain achieved? What is the signal amplitude v_{gs} that results in the 0.5-V signal amplitude at the output?

(c) If the dc bias current in the drain is to be 100 μA, what value of R_D is needed?

(d) If $k_n' = \mu_n C_{ox} = 200$ μA/V^2, what W/L ratio is required for the MOSFET?

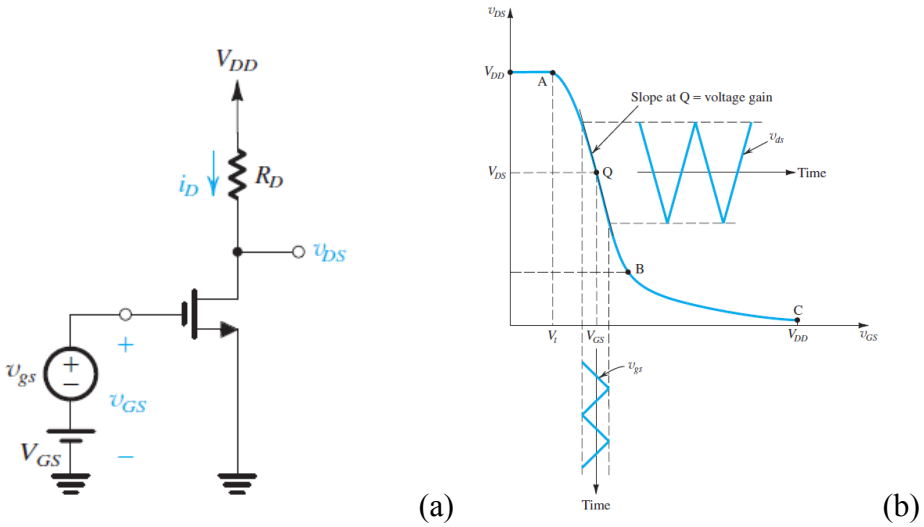


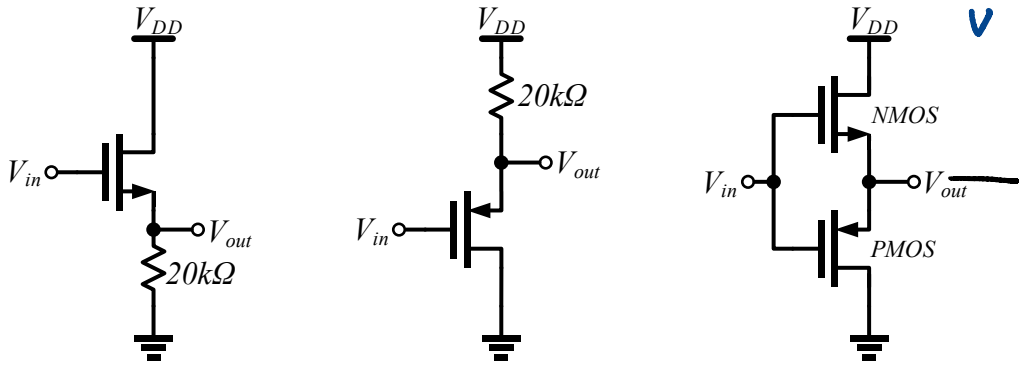
Fig. 7.4

3. Threshold voltage V_{th} = 0.7 V, $\mu_n C_{ox}$ = 200 μA/V^2, $\mu_p C_{ox}$ = 200 μA/V^2, W/L = 5. Ignore channel length modulation λ = 0 and body effect. V_{DD} = 1.8V.

(a) In Fig. 3(a), draw the voltage transfer curve of V_{out} when V_{in} is DC from 0V to 1.8V. Specify the operating point V_{out} and Vin at cut-off, linear, saturation region

(b) In Fig. 3(b), draw the VTC.

(c) In Fig. 3(c), draw the VTC.



(a) (b) (c)

Fig. 3

4. When body effect must be taken into account, and using V_{SB}=1V to simply your calculation. Redraw the problem 3 (a), (b), (c).

$$V_{th}=V_{th0}+\gamma\left[\sqrt{2\phi_f+V_{SB}}-\sqrt{2\phi_f}\right];2\phi_f=0.7V,\gamma=0.4V^{1/2}$$

5. Consider the FET amplifier of Fig. 7.10 for the case V_{th} = 0.4 V, k_n = 5 mA/V^2, V_{GS} = 0.6 V, V_{DD} = 1.8 V, and R_D = 10 kΩ.

(a) Find the dc quantities I_D and V_{DS}.

(b) Calculate the value of g_m at the bias point.

(c) Calculate the value of the voltage gain.

(d) If the MOSFET has λ = 0.1 V^{-1}, find r_o at the bias point and calculate the voltage gain.

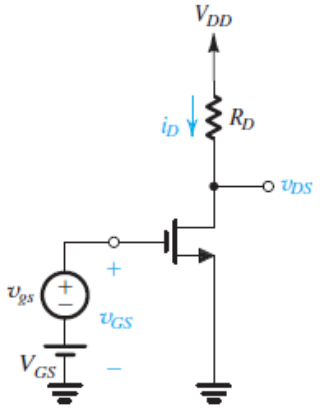


Fig. 7.10

6. An NMOS amplifier is to be designed to provide a 0.20-V peak output signal across a 20-kΩ load that can be used as a drain resistor. If a gain of at least 10 V/V is needed, what *gm* is required? Using a dc supply of 1.8 V, what values of I_D and V_{OV} would you choose? What *W*/*L* ratio is required if $\mu_n C_{ox} = 200\ \mu A/V^2$? If $V_{th} = 0.4$ V, find V_{GS}.