Joo-Young Kim

Microsoft Research, 1 Microsoft Way, Redmond, WA 98052
jooyoung@microsoft.com
Mobile: 425-786-7485
Website: http://research.microsoft.com/en-us/people/jooyoung

Research Interests

VLSI design, computer architecture, FPGA, domain specific processors, processing-in-memory, hardware/software co-design, datacenter accelerators, distributed storage system, data compression, computer vision, machine learning

Education

Ph.D. in Electrical Engineering, KAIST, February 2010.
Advisor: Professor Hoi-Jun Yoo
Dissertation: "High Performance Low Power Real-Time Multi-Object Recognition Processor with Visual Perception Engine"
M.S. in Electrical Engineering and Computer Science, KAIST, February 2007.
B.S. in Electrical Engineering, Magna cum Laude, KAIST, February 2005.

Employment

- Senior Research Hardware Design Engineer, Microsoft Research. (2/2014 – Present)
- Research Hardware Design Engineer II, Microsoft Research. (2/2012 – 1/2014)
- Visiting Researcher, Microsoft Research. (9/2010 – 8/2011)
- Post-doctoral Researcher, KAIST. (2/2010 – 1/2012)
- Research Intern, SoC Solutions. (1/2006 – 3/2006)
- Research Assistant, KAIST. (3/2005 – 1/2010)

Honors & Awards

- **2017**: Project Catapult won Geekwire's **Innovation of the Year Award.**
- **2016**: "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services" selected for **Communications of the ACM Research Highlights**.
- **2016**: "A Cloud-Scale Acceleration Architecture" selected for **IEEE Micro Top Picks** in Computer Architecture.
- **2015**: "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services" selected for **IEEE Micro Top Picks** in Computer Architecture.
- **2010**: "A Real-time Embedded Vision System with 201.4GOPS 496mW Object Recognition Processor" won **Design Contest Award** at *47th Design Automation Conference*.
- **2008**: "Vision Platform for Mobile Intelligent Robot based on 81.6GOPS Object Recognition Processor" won **Design Contest Award** at *45th Design Automation Conference*.
- **2006**: "A TCAM based Periodic Event Generator for Multi-Node Management in Body Sensor Network" won **Design Contest Award** at *2nd Asian Solid-State Circuits Conference*.

Publications

Refereed Conference paper

1. Adrian Caulfield, Eric Chung, Andrew Putnam, Hari Angepat, Jeremy Fowers, Michael Haselman, Stephen Heil, Matt Humphrey, Puneet Kaur, **Joo-Young Kim**, Daniel Lo, Todd Massengill, Kalin Ovtcharov, Michael Papamichael, Lisa Woods, Sitaram Lanka, Derek Chiou, and Doug Burger, "A Cloud-Scale Acceleration Architecture," *49th International Symposium on Microarchitecture* (MICRO), October 2016.
2. Kalin Ovtcharov, Olatunji Ruwase, **Joo-Young Kim**, Jeremy Fowers, Karin Strauss, Eric Chung, "Toward Accelerating Deep Learning at Scale Using Specialized Logic," *Hot Chips: A Symposium on High Performance Chips* (HOTCHIPS), August 2015.
3. Jeremy Fowers, **Joo-Young Kim**, Scott Hauck, and Doug Burger, "A Scalable High-Bandwidth Architecture for Lossless Compression on FPGAs," *23rd International Symposium on Field-Programmable Custom Computing Machines* (FCCM), May 2015.

4. Andrew Putnam, Adrian M. Caulfield, Eric S. Chung, Derek Chiou, Kypros Constantinides, John Demme, Hadi Esmaeilzadeh, Jeremy Fowers, Jan Gray, Michael Haselman, Scott Hauck, Stephen Heil, Amir Hormati, **Joo-Young Kim**, Sitaram Lanka, James R. Larus, Eric Peterson, Gopi Prashanth, Aaron Smith, Jason Thong, Phillip Yi Xiao, and Doug Burger, "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services," *41st International Symposium on Computer Architecture* (ISCA), June 2014.
5. Janarbek Matai, **Joo-Young Kim** and Ryan Kastner, "Energy Efficient Canonical Huffman Encoding," *25th International Conference on Application-specific Systems, Architectures and Processors* (ASAP), June 2014.
6. **Joo-Young Kim**, Scott Hauck, and Doug Burger, "A Scalable Multi-engine Xpress9 Compressor with Asynchronous Data Transfer," *22nd International Symposium on Field-Programmable Custom Computing Machines* (FCCM), May 2014.
7. Seungjin Lee, Jinwook Oh, Minsu Kim, Junyoung Park, Joonsoo Kwon, **Joo-Young Kim**, and Hoi-Jun Yoo, "Intelligent NoC with Neuro-Fuzzy Bandwidth Regulation for a 51 IP Object Recognition Processor," *IEEE Custom Integrated Circuits Conference* (CICC), September 2010.
8. Jinwook Oh, Seungjin Lee, Minsu Kim, Joonsoo Kwon, Junyoung Park, **Joo-Young Kim**, and Hoi-Jun Yoo, "A 1.2mW On-Line Learning Mixed Mode Intelligent Inference Engine for Robust Object Recognition," *IEEE Symposium on VLSI Circuits* (VLSI), June 2010.
9. Seungjin Lee, Jinwook Oh, Minsu Kim, Joonyoung Park, Joonsoo Kwon, **Joo-Young Kim**, and Hoi-Jun Yoo, "A 36 Heterogeneous Core Architecture with Resource-Aware Fine-grained Task Scheduling for Feedback Attention based Object Recognition," *IEEE Symposium on Low-Power and High-Speed Chips* (COOLCHIPS), April 2010.
10. **Joo-Young Kim**, Kwanho Kim, Minsu Kim, Seungjin Lee, Jinwook Oh, and Hoi-Jun Yoo, "A 118.4GB/s Multi-Casting Network-on-Chip for Real-Time Object Recognition Processor," *IEEE European Solid-State Circuits Conference* (ESSCIRC), September 2009.
11. **Joo-Young Kim**, Seungjin Lee, Jinwook Oh, Minsu Kim, and Hoi-Jun Yoo, "A 60fps 496mW Multi-Object Recognition Processor with Workload-Aware Dynamic Power Management," *ACM/IEEE International Symposium on Low Power Electronics and Design* (ISLPED), August 2009.
12. Minsu Kim, **Joo-Young Kim**, Seungjin Lee, Jinwook Oh, and Hoi-Jun Yoo, "A 22.8GOPS 2.83mW Neuro-fuzzy Object Detection Engine for Fast Multi-Object Recognition," *IEEE Symposium on VLSI Circuits* (VLSI), June 2009.
13. **Joo-Young Kim**, Minsu Kim, Seungjin Lee, Jinwook Oh, Kwanho Kim, and Hoi-Jun Yoo, "An Energy Efficient Real-Time Object Recognition Processor with Neuro-Fuzzy Controlled Task Pipelining," *IEEE Symposium on Low-Power and High-Speed Chips* (COOLCHIPS), April 2009.
14. **Joo-Young Kim**, Minsu Kim, Seungjin Lee, Jinwook Oh, Kwanho Kim, Sejong Oh, Jeong-Ho Woo, Donghyun Kim, and Hoi-Jun Yoo, "A 201.4GOPS 496mW Real-Time Multi-Object Recognition Processor with Bio-Inspired Neural Perception Engine," *IEEE International Solid-State Circuits Conference* (ISSCC), February 2009.
15. **Joo-Young Kim**, Kwanho Kim, Seungjin Lee, Minsu Kim, and Hoi-Jun Yoo, "A 66fps 38mW Nearest Neighbor Matching Processor with Hierarchical VQ Algorithm for Real-Time Object Recognition," *IEEE Asian Solid-State Circuits Conference* (A-SSCC), November 2008.
16. Kwanho Kim, **Joo-Young Kim**, Seungjin Lee, Minsu Kim, and Hoi-Jun Yoo, "A 76.8 GB/s 46 mW Low-latency Network-on-Chip for Real-time Object Recognition Processor," *IEEE Asian Solid-State Circuits Conference* (A-SSCC), November 2008.
17. Kwanho Kim, **Joo-Young Kim**, Seungjin Lee, Minsu Kim, and Hoi-Jun Yoo, "A 211 GOPS/W Dual-Mode Real-Time Object Recognition Processor with Network-on-Chip," *IEEE European Solid-State Circuits Conference* (ESSCIRC), September 2008.
18. Seungjin Lee, Kwanho Kim, Minsu Kim, **Joo-Young Kim**, and Hoi-Jun Yoo, "The Brain Mimicking Visual Attention Engine: An 80x60 Digital Cellular Neural Network for Rapid Global Feature Extraction," *IEEE Symposium on VLSI Circuits* (VLSI), June 2008.
19. Donghyun Kim, Kwanho Kim, **Joo-Young Kim**, Seungjin Lee, and Hoi-Jun Yoo, "Vision Platform for Mobile Intelligent Robots Based on 81.6 GOPS Objects Recognition Processor," *ACM Design Automation Conference* (DAC), June 2008.
20. Joonsung Bae, **Joo-Young Kim**, and Hoi-Jun Yoo, "A 0.6pJ/b 3Gb/s/ch Transceiver in 0.18 um CMOS for 10mm On-chip interconnects," *IEEE International Symposium on Circuit and Systems* (ISCAS), May 2008.
21. Kwanho Kim, Seungjin Lee, **Joo-Young Kim**, Minsu Kim, Donghyun Kim, Jeong-Ho Woo, and Hoi-Jun Yoo, "A 125GOPS 583mW Network-on-Chip Based Parallel Processor with Bio-inspired Visual Attention Engine," *IEEE International Solid-State Circuits Conference* (ISSCC), February 2008.
22. **Joo-Young Kim**, and Hoi-Jun Yoo, "Bitwise Competition Logic for Compact Digital Comparator," *IEEE Asian Solid-State Circuits Conference* (A-SSCC), November 2007.
23. Donghyun Kim, Kwanho Kim, **Joo-Young Kim**, Seungjin Lee, and Hoi-Jun Yoo, "Implementation of Memory-Centric NoC for 81.6 GOPS Object Recognition Processor," *IEEE Asian Solid-State Circuits Conference* (A-SSCC),

November 2007.

24. **Joo-Young Kim**, Donghyun Kim, Seungjin Lee, Kwanho Kim, and Hoi-Jun Yoo, "Visual Image Processing RAM for Fast 2-D Data Location Search," *IEEE European Solid-State Circuits Conference* (ESSCIRC), September 2007.
25. Donghyun Kim, Kwanho Kim, **Joo-Young Kim**, Seungjin Lee, and Hoi-Jun Yoo, "An 81.6 GOPS Object Recognition Processor Based on NoC and Visual Image Processing Memory," *IEEE Custom Circuits Conference* (CICC), September 2007.
26. Donghyun Kim, Kwanho Kim, **Joo-Young Kim**, Seungjin Lee, and Hoi-Jun Yoo, "Solutions for Real Chip Implementation Issues of NoC and Their Application to Memory-Centric NoC," *IEEE International Symposium on Network-on-Chip* (NOCS), May 2007.
27. **Joo-Young Kim**, Kangmin Lee, and Hoi-Jun Yoo, "A 372ps 64-bit Adder using Fast Pull-up Logic in 0.18-um CMOS," *IEEE International Symposium on Circuit and Systems* (ISCAS), May 2006.
28. Sungdae Choi, Kyomin Sohn, **Jooyoung Kim**, Jerald Yoo, and Hoi-Jun Yoo, "A TCAM-based Periodic Event Generator for Multi-Node Management in the Body Sensor Network," *IEEE Asian Solid-State Circuits Conference* (A-SSCC), November 2006.
29. Kyomin Sohn, Sungdae Choi, Jeong-Ho Woo, **Jooyoung Kim**, and Hoi-Jun Yoo, "A 0.6-V, 6.8-uW Embedded SRAM for Ultra-low Power SoC," *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, November 2006.
30. Sungdae Choi, Seong-Jun Song, Kyomin Sohn, Hyejung Kim, **Jooyoung Kim**, Namjun Cho, Jeong-Ho Woo, Jerald Yoo and Hoi-Jun Yoo, "A 24.2-uW Dual-Mode Human Body Communication Controller for Body Sensor Network," *IEEE European Solid-State Circuits Conference* (ESSCIRC), Sepember 2006.
31. Sungdae Choi, Seong-Jun Song, Kyomin Sohn, Hyejung Kim, **Jooyoung Kim**, Namjun Cho, Jeong-Ho Woo, Jerald Yoo and Hoi-Jun Yoo, "A Multi-Nodes Human Body Communication Sensor Network Control Processor," *IEEE Custom Circuits Conference* (CICC), September 2006.
32. Sungdae Choi, Seong-Jun Song, Kyomin Sohn, Hyejung Kim, **Jooyoung Kim**, Jerald Yoo, and Hoi-Jun Yoo, "A Low-power Star-topology Body Area Network Controller for Periodic Data Monitoring Around and Inside the Human Body," *IEEE International Symposium on Wearable Computers* (ISWC), June 2006.

Journal Papers

33. Adrian Caulfield, Eric Chung, Andrew Putnam, Hari Angepat, Daniel Firestone, Jeremy Fowers, Michael Haselman, Stephen Heil, Matt Humphrey, Puneet Kaur, **Joo-Young Kim**, Daniel Lo, Todd Massengill, Kalin Ovtcharov, Michael Papamichael, Lisa Woods, Sitaram Lanka, Derek Chiou, Doug Burger, "Configurable Clouds," *IEEE Micro*, Vol. 37, No. 3, May/June 2017.
34. Andrew Putnam, Adrian Caulfield, Eric Chung, Derek Chiou, Kypros Constantinides, John Demme, Hadi Esmaeilzadeh, Jeremy Fowers, Gopi Prashanth Gopal, Jan Gray, Michael Haselman, Scott Hauck, Stephen Heil, Amir Hormati, **Joo-Young Kim**, Sitaram Lanka, James Larus, Eric Peterson, Simon Pope, Aaron Smith, Jason Thong, Phillip Yi Xiao, Doug Burger, "A Reconfigurable Fabric For Accelerating Large-Scale Datacenter Services," *Communications of the ACM*, Vol. 59, No. 11, November 2016.
35. Andrew Putnam, Adrian M. Caulfield, Eric S. Chung, Derek Chiou, Kypros Constantinides, John Demme, Hadi Esmaeilzadeh, Jeremy Fowers, Jan Gray, Michael Haselman, Scott Hauck, Stephen Heil, Amir Hormati, **Joo-Young Kim**, Sitaram Lanka, James R. Larus, Eric Peterson, Gopi Prashanth, Aaron Smith, Jason Thong, Phillip Yi Xiao, and Doug Burger, "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services," *IEEE Micro*, May 2015.
36. Kalin Ovtcharov, Olatunji Ruwase, **Joo-Young Kim**, Jeremy Fowers, Karin Strauss, and Eric S. Chung, "Accelerating Deep Convolutional Neural Networks Using Specialized Hardware," *Microsoft White paper*, February 2015.
37. Jinwook Oh, Gyeonghoon Kim, Junyoung Park, Injoon Hong, Seungjin Lee, **Joo-Young Kim**, Jeong-Ho Woo, and Hoi-Jun Yoo, "A 320mW 342GOPS Real-Time Dynamic Object Recognition Processor for HD 720p Video Streams," *IEEE Journal of Solid-State Circuits* (JSSC), Vol. 48, No. 1, January 2013.
38. Jinwook Oh, Gyeonghoon Kim, Junyoung Park, Injoon Hong, Seungjin Lee, **Joo-Young Kim**, Jeong-Ho Woo, and Hoi-Jun Yoo, "Low-Power, Real-Time Object Recognition Processor for Mobile Vision Systems," *IEEE Micro*, Vol. 32, No. 6, November/December 2012.
39. Junyoung Park, Joonsoo Kwon, Jinwook Oh, Seungjin Lee, **Joo-Young Kim**, and Hoi-Jun Yoo, "A 92mW Real-Time Traffic Sign Recognition System with Robust Illumination Adaptation and Support Vector Machine," *IEEE Journal of Solid-State Circuits* (JSSC), Vol. 47, No. 11, November 2012.
40. Seungjin Lee, Minsu Kim, Kwanho Kim, **Joo-Young Kim**, and Hoi-Jun Yoo, "24-GOPS 4.5-mm2 Digital Cellular Neural Network for Rapid Visual Attention in an Object-Recognition SoC," *IEEE Transactions on Neural Networks*, Vol. 22, No. 1, January 2011.
41. **Joo-Young Kim**, Junyoung Park, Seungjin Lee, Minsu Kim, Jinwook Oh, and Hoi-Jun Yoo, "A 118.4GB/s Multi-Casting Network-on-Chip with Hierarchical Star-Ring Combined Topology for Real-Time Object Recognition,"

IEEE Journal of Solid-State Circuits (JSSC), Vol. 45, No. 7, July 2010.

42. **Joo-Young Kim**, Sejong Oh, Seungjin Lee, Minsu Kim, Jinwook Oh, and Hoi-Jun Yoo, "An Attention Controlled Multi-Core Architecture for Energy Efficient Object Recognition," *Elsevier Signal Processing: Image Communication*, Vol. 25, No. 5, June 2010.
43. **Joo-Young Kim**, Donghyun Kim, Kwanho Kim, Seungjin Lee, and Hoi-Jun Yoo, "Visual Image Processing RAM: Memory Architecture with 2-D Data Location Search and Data Consistency Management for a Multi-Core Object Recognition Processor," *IEEE Transactions on Circuits and Systems for Video Technology*, Vol. 20, No. 4, April 2010.
44. Seungjin Lee, Kwanho Kim, **Joo-Young Kim**, Minsu Kim, and Hoi-Jun Yoo, "Familiarity Based Unified Visual Attention Model for Fast and Robust Object Recognition," *Elsevier Pattern Recognition*, Vol. 43, No. 3, March 2010.
45. **Joo-Young Kim**, Minsu Kim, Seungjin Lee, Jinwook Oh, Kwanho Kim and Hoi-Jun Yoo, "A 201.4GOPS 496mW Real-Time Multi-Object Recognition Processor with Bio-Inspired Neural Perception Engine," *IEEE Journal of Solid-State Circuits* (JSSC), Vol. 45, No. 1, January 2010.
46. **Joo-Young Kim**, Minsu Kim, Seungjin Lee, Jinwook Oh, Sejong Oh, and Hoi-Jun Yoo, "Real-Time Object Recognition with Neuro-Fuzzy Controlled Workload-aware Task Pipelining," *IEEE Micro*, Vol. 29, No. 6, November/December 2009.
47. Kwanho Kim, Seungjin Lee, **Joo-Young Kim**, Minsu Kim, and Hoi-Jun Yoo, "A Configurable Heterogeneous Multicore Architecture with Cellular Neural Network for Real-Time Object Recognition," *IEEE Transactions on Circuits and Systems for Video Technology*, Vol. 19, No. 11, November 2009.
48. Donghyun Kim, Kwanho Kim, Seungjin Lee, **Joo-Young Kim**, Minsu Kim, and Hoi-Jun Yoo, "Memory-Centric Network-on-Chip for Power Efficient Execution of Task-Level Pipeline on a Multi-Core Processor," *IET Computers & Digital Techniques*, Vol. 3, No. 5, September 2009.
49. Donghyun Kim, Kwanho Kim, **Joo-Young Kim**, Seungjin Lee, Se-Joong Lee, and Hoi-Jun Yoo, "81.6 GOPS Object Recognition Processor Based on a Memory-Centric NoC," *IEEE Transactions on Very Large Scale Integration*, Vol. 17, No. 3, March 2009.
50. Kwanho Kim, Seungjin Lee, **Joo-Young Kim**, Minsu Kim, and Hoi-Jun Yoo, "A 125 GOPS 583 mW Network-on-Chip Based Parallel Processor with Bio-Inspired Visual Attention Engine," *IEEE Journal of Solid-State Circuits* (JSSC), Vol. 44, No. 1, January 2009.

Patents

51. **Joo-Young Kim**, Doug Burger, Jeremy Fowers, and Scott Hauck, "Scalable high-bandwidth architecture for lossless compression," U.S. Patent 9,590,655, Issued on March 7, 2017.
52. Eric Chung, Karin Strauss, Kalin Ovtcharov, **Joo-Young Kim**, and Olatunji Ruwase, "Deep Neural network partitioning on servers," U.S. Patent App. 14/754,384.
53. Eric Chung, Karin Strauss, Kalin Ovtcharov, **Joo-Young Kim**, and Olatunji Ruwase, "Convolutional neural networks on hardware accelerators," US Patent App. 14/754,367.
54. Minsu Kim, **Joo-Young Kim**, and Hoi-Jun Yoo, "Binary Number Comparator," Korean Patent No.10-10916840000, Issued on November 2, 2011.
55. **Joo-Young Kim** and Hoi-Jun Yoo, "Network on Chip and Network on Chip Systems," Korean Patent No.10-10775390000, Issued on October 21, 2011.
56. Jinwook Oh, **Joo-Young Kim**, and Hoi-Jun Yoo, "Computer System Combining Neuro-Fuzzy System and Parallel Processor and Objects Recognizing System using Thereof," Korean Patent No.10-10696020000, Issued on September 27, 2011.
57. **Joo-Young Kim** and Hoi-Jun Yoo, "Multi Casting Network on Chip, Systems Thereof and Network Switch," Korean Patent No.10-10334250000, Issued on April 29, 2011.
58. **Joo-Young Kim** and Hoi-Jun Yoo, "Method and Apparatus for Recognizing Objects in an Image," Korean Patent No.10-10279060000, Issued on April 1, 2011.
59. Minsu Kim, **Joo-Young Kim**, and Hoi-Jun Yoo, "Apparatus and Method for Detecting a Plurality of Objects In an Image," Korean Patent No.10-10182990000, February 22, 2011.
60. **Joo-Young Kim** and Hoi-Jun Yoo, "Apparatus and Method Transmitting-Receiving Data," Korean Patent No.10-09461770000, Issued on March 2, 2010.
61. **Joo-Young Kim** and Hoi-Jun Yoo, "High Speed Serializing-Deserializing System and Method," Korean Patent No.10-09364450000, Issued on January 5, 2010.
62. **Joo-Young Kim** and Hoi-Jun Yoo, "Arithmetic Apparatus of Microprocessor," Korean Patent No.10-09188150000, Issued on August 17, 2009.

Research Experience

Catapult (March 2011 – Present)

At Microsoft Research, I am involved in the Catapult project which aims to advance data-center capabilities beyond commodity server designs with reconfigurable accelerators. We have designed a composable, reconfigurable fabric consisting of a 6x8 2-D torus of high-end Stratix V FPGAs embedded into a half-rack of 48 machines. For the very first pilot, we deployed the fabric on a bed of 1,632 servers accelerating Bing web search engine by 2X [4, 34, 35].
For the second version, we propose a new cloud architecture named Configurable Cloud which uses reconfigurable logic to accelerate both network functions and applications. This architecture places a layer of reconfigurable logic (FPGAs) between the network switches and the servers, enabling network flows to be programmably transformed at line rate, enabling acceleration of local applications running on the server, and enabling the FPGAs to communicate directly to harvest remote FPGAs unused by their local servers at datacenter scale [1, 33].
As a senior member of the team, I am currently leading an effort to accelerate high-valued cloud applications including machine learning, storage system, data compression, and data encryption.

Deep Neural Networks (March 2014 – Present)

I led the design of a convolutional neural network accelerator that runs on Catapult FPGA platform. The accelerator outperformed then latest accelerators by more than 3X [2, 36]. We demoed that the throughput/watt is significantly higher than for a GPU and projected the performance when ported to an Arria 10 FPGA. I am also contributing to the design of a DNN processor for BrainWave, a large-scale machine learning platform on Catapult.

Distributed Storage System (September 2012 – Present)

I led a development of a high throughput data compressor for distributed storage servers in datacenter. Targeting a high-quality compression comparable to popular GZIP's best optimization, we implemented an Xpress compressor on Stratix V FPGA which can achieve 1.6-2.4Gbps throughput and support up to 128 thread contexts [6]. To satisfy line-rate demands for network compression, we also developed a high-bandwidth compressor whose bandwidth can be as high as 40Gbps with fully pipelined design [3].
I am currently leading an effort to develop a software library that allows upper-level cloud services to access a variety of hardware IPs such as compression, encryption, and integrity check.

Real-time Camera Tracking and Scene Reconstruction (September 2010 – August 2011)

At Microsoft Research, I created a real-time camera tracking and geometry reconstruction system using multimodal sensors for immersive augmented reality experience. A compute-intensive computer vision algorithm consisting of 2d natural feature extraction and 3d bundle adjustment was accelerated by GPU and CUDA programming language to achieve 30 frames per second rate.

Embedded Microprocessor for Intelligent Car Systems (February 2010 – August 2010)

At KAIST, we partnered with Hyundai Motors to develop an embedded microprocessor for their intelligent car systems, more specifically, Forward Collision Warning System and Lane Departure Warning System. As a lead hardware designer, I was responsible for demonstrating and shipping the processor and its low-level C compiler with specialized instruction sets. The processor was successfully fabricated and verified by Hyundai Motors.

Machine Vision System-on-Chips (March 2005 – January 2010)

At KAIST, I led the design of third generation of BONE-V machine vision SoCs with a team of 1 post-doc researcher, 3 graduate students, and 2 full-time engineers. The fabricated SoC had 7x7mm^2 die area in 130nm process and featured 16 vector processors as well as two specialized engines to achieve real-time recognition tasks with sub-watt power consumption [14, 10, 11]. Its real-time operation was successfully demonstrated on a vision system that integrated a 640x480 camera, PXA270 microprocessor, and Xilinx FPGA [45].
Before that, I was involved in the design of first and second generation of SoCs as a component designer. I designed a coherent shared memory [24], a RISC processor with custom instruction sets, and a vector matching processor [15].

Professional Activities

Technical Program Committee

- International Symposium on Highly-Efficient Accelerators and Reconfigurable Technologies (HEART), 2014, 2015, 2016, 2017, 2018.
- Technical Committee Chair, KAIST EE-CS joint workshop, January 2012.

- Technical Committee Chair, KAIST-Keio-Tsinghua (KKT) workshop, August 2009.

Invited Talks / Tutorials

1. Tutorial: "Accelerating Deep Convolutional Neural Networks Using Specialized Hardware in the Datacenter," *IEEE Asian Solid-State Circuits Conference* (A-SSCC), Toyama, Japan, November 2016.
2. Invited Talk: "Accelerating Deep Convolutional Neural Networks Using Specialized Hardware in the Datacenter," KAIST, *Deep Neural SoC Workshop*, *KAIST*, Daejeon, South Korea, August 2016.
3. Invited Talk: "Accelerating Deep Convolutional Neural Networks Using Specialized Hardware in the Datacenter," *Samsung Advanced Institute of Technology*, Suwon, South Korea, August 2016.
4. Invited Talk: "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services," *Naver Labs*, Seongnam, South Korea, April 2015.
5. Invited Talk: "Hardware Accelerators on FPGA," *Northwest Regional Conference*, Seattle, WA, September 2013.
6. Invited Talk: "Robust 6-DOF camera tracking for mobile augmented reality", *Chung-Nam National University*, Daejeon, South Korea, December 2011.
7. Invited Talk: "High Performance Low Power Real-Time Multi-Object Recognition Processor with Visual Perception Engine," *Intel*, Santa Clara, CA, August 2009.
8. Invited Talk: "High Performance Low Power Real-Time Multi-Object Recognition Processor with Visual Perception Engine," *Nvidia*, Santa Clara, CA, August 2009.
9. Invited Talk: "High Performance Low Power Real-Time Multi-Object Recognition Processor with Visual Perception Engine," *Texas Instruments*, Dallas, TX, August 2009.
10. Invited Talk: "High Performance Low Power Real-Time Multi-Object Recognition Processor with Visual Perception Engine," *IMEC*, Leuven, Belgium, August 2009.
11. Invited Talk: "High Performance Low Power Real-Time Multi-Object Recognition Processor with Visual Perception Engine," *Technical University of Eindhoven*, Eindhoven, Netherlands, August 2009.

External Reviewer

Served as an external reviewer for various conference and journal papers including IEEE JSSC, IEEE ISSCC, IEEE TCAS, IEEE TCAS-II, IEEE VLSI, IEEE A-SSCC, ACM/IEEE NOCS, IEEE ISCAS.

Intern Supervision

David Ojika, University of Florida
Ming Liu, Massachusetts Institute of Technology
Peipei Zhou, University of California Los Angeles
Janarbek Matai, University of California San Diego
Jinwook Oh, Korea Advanced Institute of Science and Technology

Personal

Citizen of South Korea, United States permanent resident.