

DECADE COUNTER; DIVIDE-BY-TWELVE COUNTER; 4-BIT BINARY COUNTER

The SN54/74LS90, SN54/74LS92 and SN54/74LS93 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS90), divide-by-six (LS92) or divide-by-eight (LS93) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{\text{CP}}$) to form BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

- Low Power Consumption . . . Typically 45 mW
- High Count Rates . . . Typically 42 MHz
- Choice of Counting Modes . . . BCD, Bi-Quinary, Divide-by-Twelve, Binary
- Input Clamp Diodes Limit High Speed Termination Effects

PIN NAMES LOADING (Note a) HIGH LOW \overline{CP}_0 Clock (Active LOW going edge) Input to 0.5 U.L. 1.5 U.L. ÷2 Section CP₁ Clock (Active LOW going edge) Input to 0.5 U.L. 2.0 U.L. ÷5 Section (LS90), ÷6 Section (LS92) Clock (Active LOW going edge) Input to CP₁ 1.0 U.L. 0.5 U.L. ÷8 Section (LS93) MR₁, MR₂ Master Reset (Clear) Inputs 0.5 U.L. 0.25 U.L. 0.5 U.L. MS₁, MS₂ Master Set (Preset-9, LS90) Inputs 0.25 U.L. Output from ÷2 Section (Notes b & c) 10 U.L. 5 (2.5) U.L. Q_0 10 U.L. Q₁, Q₂, Q₃ Outputs from ÷5 (LS90), ÷6 (LS92), 5 (2.5) U.L. ÷8 (LS93) Sections (Note b)

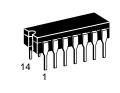
NOTES

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military, (54) and 5 U.L. for commercial (74) Temperature Ranges.
- c. The Q₀ Outputs are guaranteed to drive the full fan-out plus the CP₁ input of the device.
- d. To insure proper operation the rise (t_f) and fall time (t_f) of the clock must be less than 100 ns.

SN54/74LS90 SN54/74LS92 SN54/74LS93

DECADE COUNTER; DIVIDE-BY-TWELVE COUNTER; 4-BIT BINARY COUNTER

LOW POWER SCHOTTKY



J SUFFIX CERAMIC CASE 632-08



N SUFFIX PLASTIC CASE 646-06



D SUFFIX SOIC CASE 751A-02

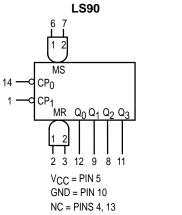
ORDERING INFORMATION

SN54LSXXJ Ceramic SN74LSXXN Plastic SN74LSXXD SOIC

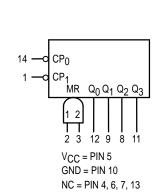
LS93

LOGIC SYMBOL

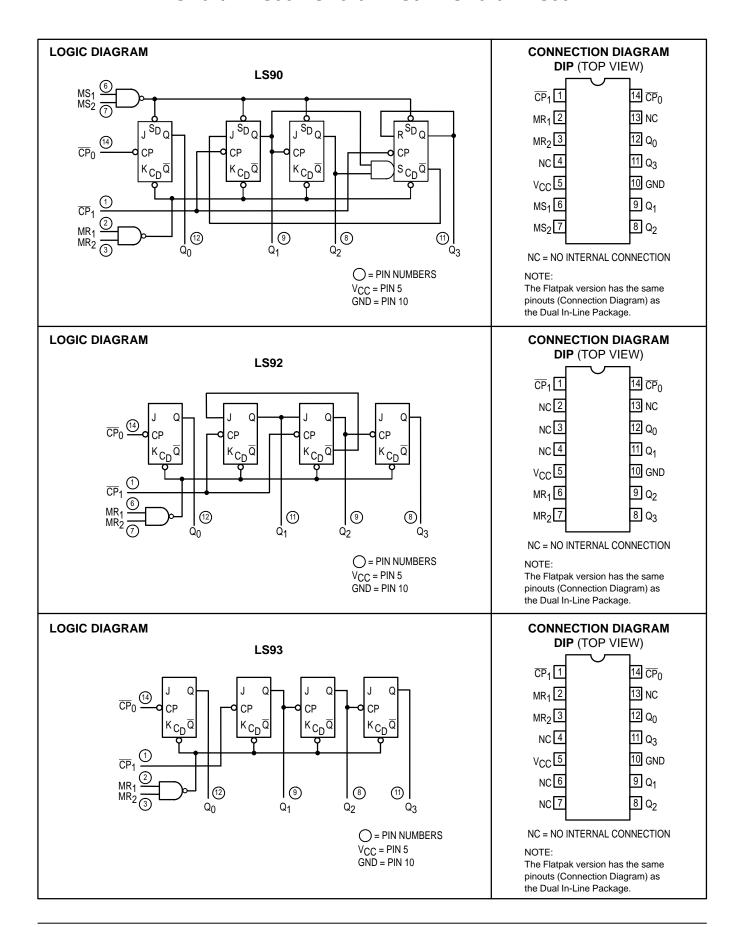
LS92



14 — CP₀ 1 — CP₁ MR Q₀ Q₁ Q₂ Q₃ 1 2 | 1 9 8 V_{CC} = PIN 5 GND = PIN 10



NC = PINS 2, 3, 4, 13



FUNCTIONAL DESCRIPTION

The LS90, LS92, and LS93 are 4-bit ripple type Decade, Divide-By-Twelve, and Binary Counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS90), divide-by-six (LS92), or divide-by-eight (LS93) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The $\rm Q_0$ output of each device is designed and specified to drive the rated fan-out plus the $\overline{\rm CP}_1$ input of the device.

A gated AND asynchronous Master Reset (MR₁ \bullet MR₂) is provided on all counters which overrides and clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set (MS₁ \bullet MS₂) is provided on the LS90 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

LS90

- A. BCD Decade (8421) Counter The \overline{CP}_1 input must be externally connected to the Q₀ output. The \overline{CP}_0 input receives the incoming count and a BCD count sequence is produced.
- B. Symmetrical Bi-quinary Divide-By-Ten Counter The Q₃ output must be externally connected to the CP₀ input. The input count is then applied to the CP₁ input and a divide-byten square wave is obtained at output Q₀.

C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (\overline{CP}_0 as the input and Q_0 as the output). The \overline{CP}_1 input is used to obtain binary divide-by-five operation at the Q_3 output.

LS92

- A. Modulo 12, Divide-By-Twelve Counter The \overline{CP}_1 input must be externally connected to the Q₀ output. The \overline{CP}_0 input receives the incoming count and Q₃ produces a symmetrical divide-by-twelve square wave output.
- B. Divide-By-Two and Divide-By-Six Counter —No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The \overline{CP}_1 input is used to obtain divide-by-three operation at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

LS93

- A. 4-Bit Ripple Counter The output Q_0 must be externally connected to input \overline{CP}_1 . The input count pulses are applied to input \overline{CP}_0 . Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0 , Q_1 , Q_2 , and Q_3 outputs as shown in the truth table.
- B. 3-Bit Ripple Counter— The input count pulses are applied to input \overline{CP}_1 . Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1 , Q_2 , and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

LS90
MODE SELECTION

RESET/SET INPUTS				OUTP	UTS						
MR ₁	MR ₂	MS ₁	MS ₂	Q ₀	Q ₁	Q_2	Q_3				
Н	Н	L	Χ	L	L	L	L				
Н	Н	Х	L	L	L	L	L				
X	Х	Н	Н	Н	L	L	Н				
L	Х	L	X		Count						
X	L	Х	L	Count							
L	Х	Х	L	Count							
Ιx	ΙL	ΙL	l x l		Count						

H = HIGH Voltage Level
L = LOW Voltage Level

X = Don't Care

LS92 AND LS93 MODE SELECTION

	SET UTS	OUTPUTS							
MR ₁	MR ₂	Q ₀	Q ₁	Q_2	Q_3				
Н	Н	L	L	L	L				
L	Н	Count							
Н	L	Count							
L	L		Col	unt					

H = HIGH Voltage Level L = LOW Voltage Level

X = Don't Care

LS90 BCD COUNT SEQUENCE

COUNT		OUTPUT						
COUNT	Q_0	Q ₁	Q_2	Q_3				
0	L	L	L	L				
1	Н	L	L	L				
2 3	L	Н	L	L				
3	Н	Н	L	L				
4	L	L	Н	L				
5	Н	L	Н	L				
6	L	Н	Н	L				
7	Н	Н	Н	L				
8	L	L	L	Н				
9	Н	L	L	Н				

 $\underline{\text{NO}}\text{TE} \colon \text{Output } \mathsf{Q}_0$ is connected to Input CP_1 for BCD count.

LS92 TRUTH TABLE

COUNT		OUT	PUT	
COUNT	Q ₀	Q ₁	Q_2	Q_3
0	L	L	L	Г
1	Н	L	L	L
2	L	Н	L	L
3	Н	Н	L	L
4	L	L	Н	L
5	Н	L	Н	L
6	L	L	L	Н
7	Н	L	L	Н
8	L	Н	L	Н
9	Н	Н	L	Н
10	L	L	Н	Н
11	Н	L	Н	Н

 $\underline{\mathsf{NO}}\mathsf{TE} \colon \mathsf{Output}\ \mathsf{Q}_0$ is connected to Input $\mathsf{CP}_1.$

LS93 TRUTH TABLE

COUNT		OUTPUT							
COUNT	Q ₀	Q_1	Q_2	Q_3					
0	L	L	L	Г					
1	Н	L	L	L					
2 3	L	Н	L	L					
	Н	Н	L	L					
4	L	L	Н	L					
5	Н	L	Н						
6	L	Н	Н	L					
7	Н	Н	Н	L					
8	L	L	L	Н					
9	Н	L	L	Н					
10	L	Н	L	Н					
11	Н	Н	L	Н					
12	L	L	Н	Н					
13	Н	L	Н	Н					
14	L	Н	Н	Н					
15	Н	Н	Н	Н					

 ${\hbox{NO}{\mbox{TE}}}\colon \mbox{Output } \mbox{Q}_0$ is connected to Input $\mbox{CP}_1.$

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Тур	Max	Unit
Vcc	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
IOH	Output Current — High	54, 74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

				Limits				
Symbol	Parameter		Min	Тур	Max	Unit	Test Co	onditions
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
\/	Input I OW Voltage	54			0.7	V	Guaranteed Input	LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} =	–18 mA
V	Output HICH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} :	= MAX, V _{IN} = V _{IH}
Vон	Output HIGH Voltage	74	2.7	3.5		V	or V _{IL} per Truth Ta	able
V	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	$V_{CC} = V_{CC} MIN,$ $V_{IN} = V_{IL} \text{ or } V_{IH}$
VOL	Output LOW voltage	74		0.35	0.5	V	I _{OL} = 8.0 mA	per Truth Table
l	Input HICH Current				20	μΑ	$V_{CC} = MAX$, $V_{IN} = 2.7 V$	
ΊΗ	Input HIGH Current				0.1	mA	V _{CC} = MAX, V _{IN}	= 7.0 V
IIL	Input LOW Current MS, MR CP ₀ CP ₁ (LS90, LS92) CP ₁ (LS93)				-0.4 -2.4 -3.2 -1.6	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$	
los	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX	
ICC	Power Supply Current	·			15	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, $\underline{V_{CC}}$ = 5.0 V, C_L = 15 pF)

		Limits									
			LS90		LS92			LS93			
Symbol	Parameter	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
fMAX	CP ₀ Input Clock Frequency	32			32			32			MHz
fMAX	CP ₁ Input Clock Frequency	16			16			16			MHz
^t PLH ^t PHL	Propagation Delay, CP ₀ Input to Q ₀ Output		10 12	16 18		10 12	16 18		10 12	16 18	ns
^t PLH ^t PHL	CP ₀ Input to Q ₃ Output		32 34	48 50		32 34	48 50		46 46	70 70	ns
^t PLH ^t PHL	CP₁ Input to Q₁ Output		10 14	16 21		10 14	16 21		10 14	16 21	ns
^t PLH ^t PHL	CP ₁ Input to Q ₂ Output		21 23	32 35		10 14	16 21		21 23	32 35	ns
^t PLH ^t PHL	CP₁ Input to Q₃ Output		21 23	32 35		21 23	32 35		34 34	51 51	ns
^t PLH	MS Input to Q ₀ and Q ₃ Outputs		20	30							ns
^t PHL	MS Input to Q ₁ and Q ₂ Outputs		26	40							ns
^t PHL	MR Input to Any Output		26	40		26	40		26	40	ns

AC SETUP REQUIREMENTS (TA = 25° C, V_{CC} = 5.0 V)

			Limits						
		LS90		LS92		LS93			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit	
t _W	CP ₀ Pulse Width	15		15		15		ns	
t _W	CP₁ Pulse Width	30		30		30		ns	
t _W	MS Pulse Width	15						ns	
t _W	MR Pulse Width	15		15		15		ns	
t _{rec}	Recovery Time MR to CP	25		25		25		ns	

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs

AC WAVEFORMS

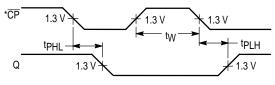


Figure 1

*The number of Clock Pulses required between the tpHL and tpLH measurements can be determined from the appropriate Truth Tables.



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