

# Course Syllabus

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<http://class.ece.iastate.edu/cpre381/>

## Course Information

CPR E 381 - Computer Organization and Assembly Level Programming

**Course Description:** (3-2) Cr. 4. Introduction to computer organization, evaluating performance of computer systems, instruction set design. Assembly level programming: arithmetic operations, control flow instructions, procedure calls, stack management. Processor design. Datapath and control, scalar pipelines, introduction to memory and I/O systems.

**Prerequisite:** CPRE 288.

### Meeting Times and Places:

Lecture: Mon, Wed, Fri, 9:00am-9:50am, Gilman 1352

Laboratory: All labs are in Coover 2050.

### Instructor and TAs:

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**Required Textbook:** Computer Organization and Design: The Hardware/Software Interface, 5th Edition, D. A. Patterson and J. L. Hennessy, Morgan Kaufmann, 2013.

**Reference Books:** (not required)

- VHDL Tutorial, Petter J. Ashenden, on the companion CD of the textbook.
- The Designer' Guide to VHDL, 2nd Edition, Peter J. Ashenden, Morgan Kaufman Publishers.

## Course Goals

- To learn the principles of computer architecture using solid engineering fundamentals and quantitative cost/performance tradeoffs.
- To understand the performance, cost and power aspects of computer systems.
- To comprehend the design of instruction set architecture, computer arithmetic, CPUs, memories, and storage and I/Os.
- For future software designers, to understand how the basic hardware techniques work in a system.
- For future hardware designers, to understand how new hardware designs may affect software systems.

## Learning Objectives

By the end of this course, a student should be able to

- Quantitatively analyze the performance/power optimization of computer systems and understand the Amdahl's Law
- Program in MIPS assembly language and understand how C program is translated into MIPS assembly code
- Design integer arithmetic and logic units, and understand how floating-point units work
- Design single-cycle processor including its control and datapath
- Design in-order processor pipeline with handling of control and data hazards
- Understand cache and main memory systems
- Understand storage systems and I/O

## Grading

- The following grading scheme will be used:
  - Homework: 11%
  - Regular Laboratory Exercises and Mini-Projects: 35%
  - Exams: 54% (see below)
    - Midterm 1 (18%) - Oct 8
    - Midterm 2 (18%) - Nov 12
    - Midterm 3 (18%) - Dec 11 (7:30-9:30AM)
  - TOTAL: 100%

Note: The last mini-project will be due in the dead week.

## Homework Policies

Homework is individual work. Homework will be assigned weekly and distributed through BlackBoard Learn. Completed homework should be submitted on BlackBoard. Late homework is accepted within three days from the due date. Late penalty is 10% per day.

## Lab Policies



Pay special attention to the items in **bold**.

- **Lab attendance is mandatory.** If you will be absent, you must notify the lab instructor by email or phone *before* the absence for it to be an excused absence. Unexcused absences may result in a zero for the corresponding lab(s). The instructor reserves the right to dismiss a student of excessive lab absences.
- Students will typically work with partners or groups on lab work. Lab partners and roles may be rotated during the term to give students different learning experiences. The same score will be awarded on group work unless there is evidence to support differential scores.
- The lab should be worked on during its corresponding lab period. If the lab is not completed during the lab period, it may be finished during any other unscheduled/open lab time. **The lab must be demonstrated to your lab instructor no later than the beginning of the next regular scheduled lab time, otherwise it is considered late** (it must be ready to demonstrate by then).
- Work can be done outside formal lab times. Software design tools (ModelSim PE Student Edition) can be downloaded free of charge to a home computer.
- All code must be commented.

**Integrity of Scholarship and Grades:** All students are to adhere to the University's policy relating to integrity of scholarship and grades as presented in the Student Information Handbook. (See <http://catalog.iastate.edu/academiclife/#regulationstext> (<http://catalog.iastate.edu/academiclife/#regulationstext>), on Academic Dishonesty)

**Students with Disabilities:** If you have a disability and require accommodations, please contact the instructor early in the semester so that your learning needs may be appropriately met. You will need to provide documentation of your disability to the Student Disability Resources (DR), Dean of Students Office, located on the main floor of the Student Services Building, Room 1076, 515-294-7220.

## Course Summary:

Date	Details	
Fri Sep 7, 2018	 <a href="https://canvas.iastate.edu/courses/53484/assignments/667554">Lab 1</a> ( <a href="https://canvas.iastate.edu/courses/53484/assignments/667554">https://canvas.iastate.edu/courses/53484/assignments/667554</a> )	due by 11:59pm
Mon Sep 10, 2018	 <a href="https://canvas.iastate.edu/courses/53484/assignments/671502">HW1</a> ( <a href="https://canvas.iastate.edu/courses/53484/assignments/671502">https://canvas.iastate.edu/courses/53484/assignments/671502</a> )	due by 11:59pm