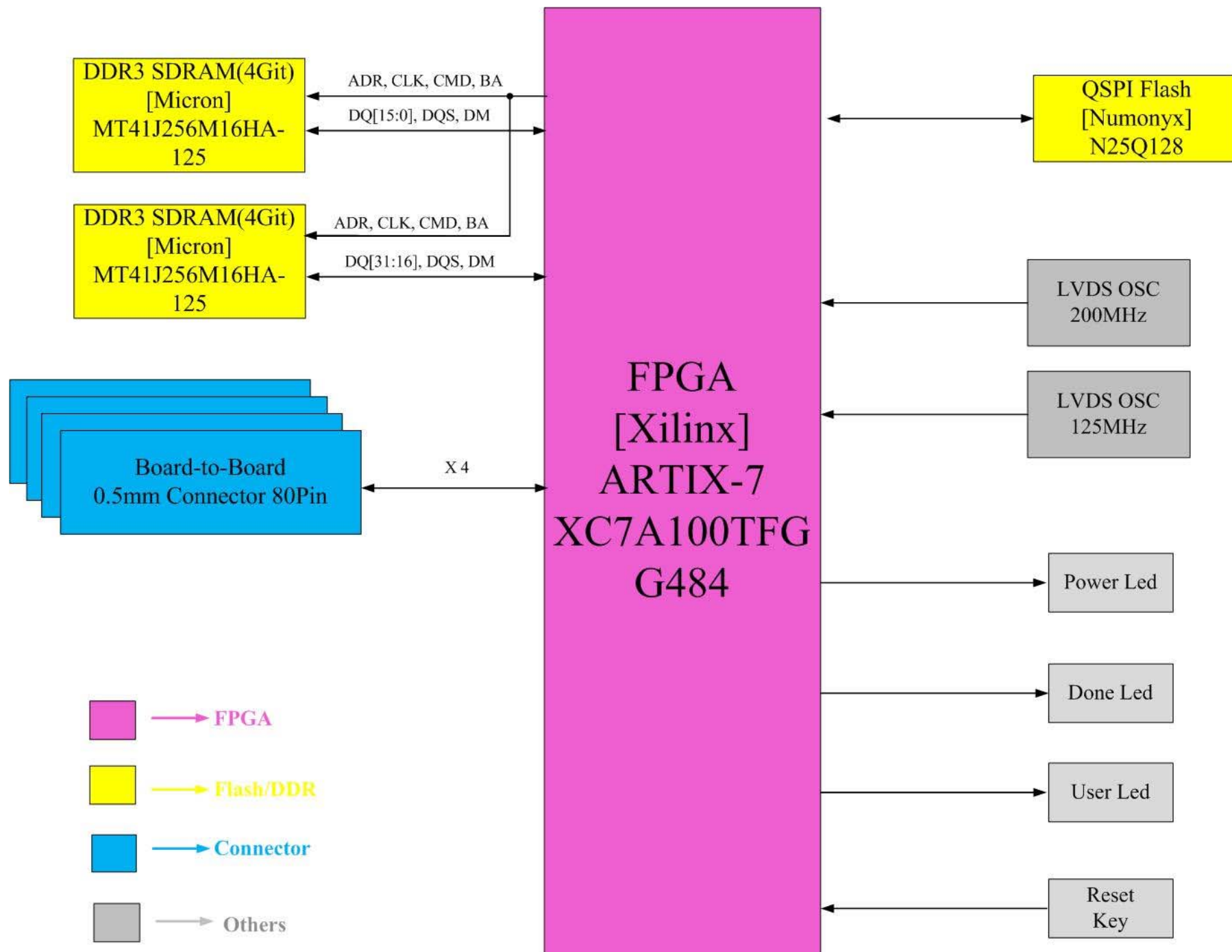


REV	Description	Date
V1.0	First Release	2018-3-06

# FPGA 核心板

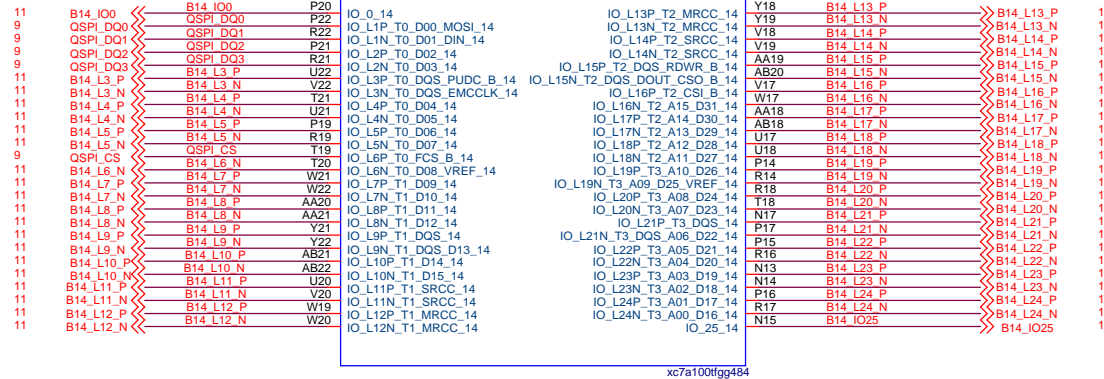
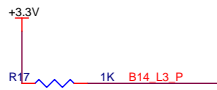
## AC7100 Schematics

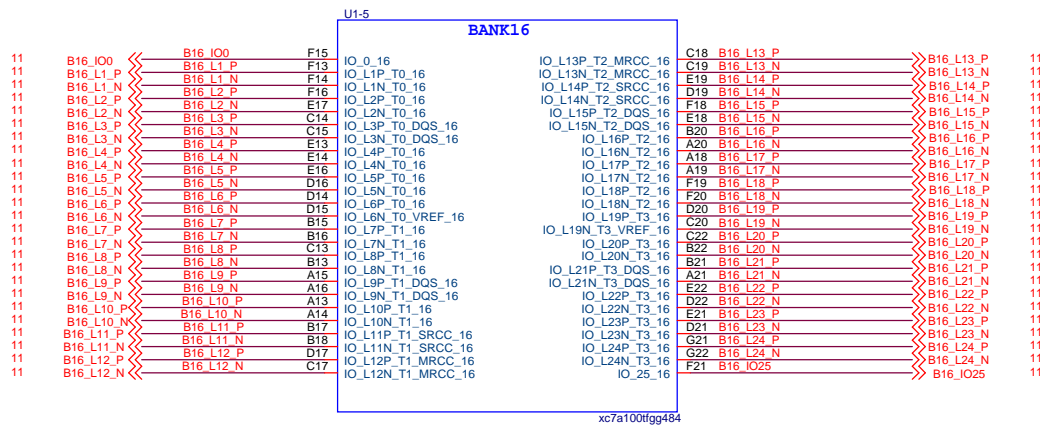
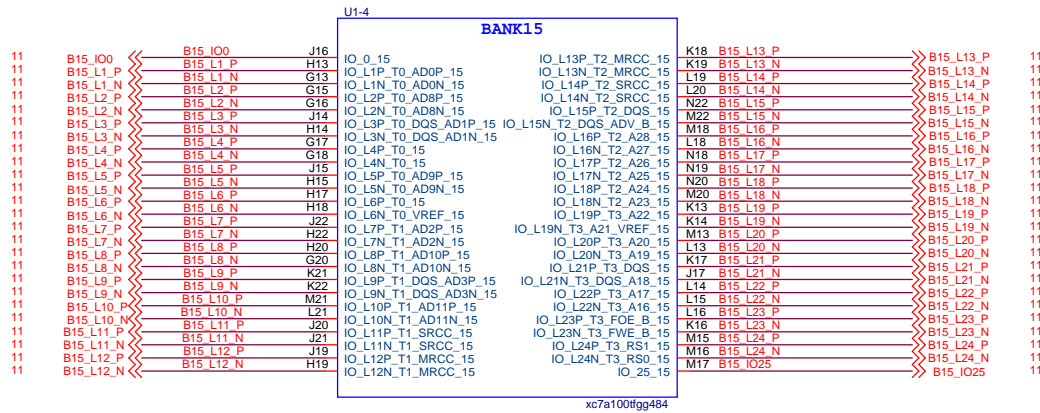
Page Number	Description
Page01	Cover Page
Page02	Block Diagram
Page03	FPGA BANK0
Page04	FPGA BANK13/14
Page05	FPGA BANK15/16
Page06	FPGA BANK34/35
Page07	FPGA BAN216
Page08	FPGA Power
Page09	DDR3
Page10	CLOCK&FLASH
Page11	POWER
Page12	Connector

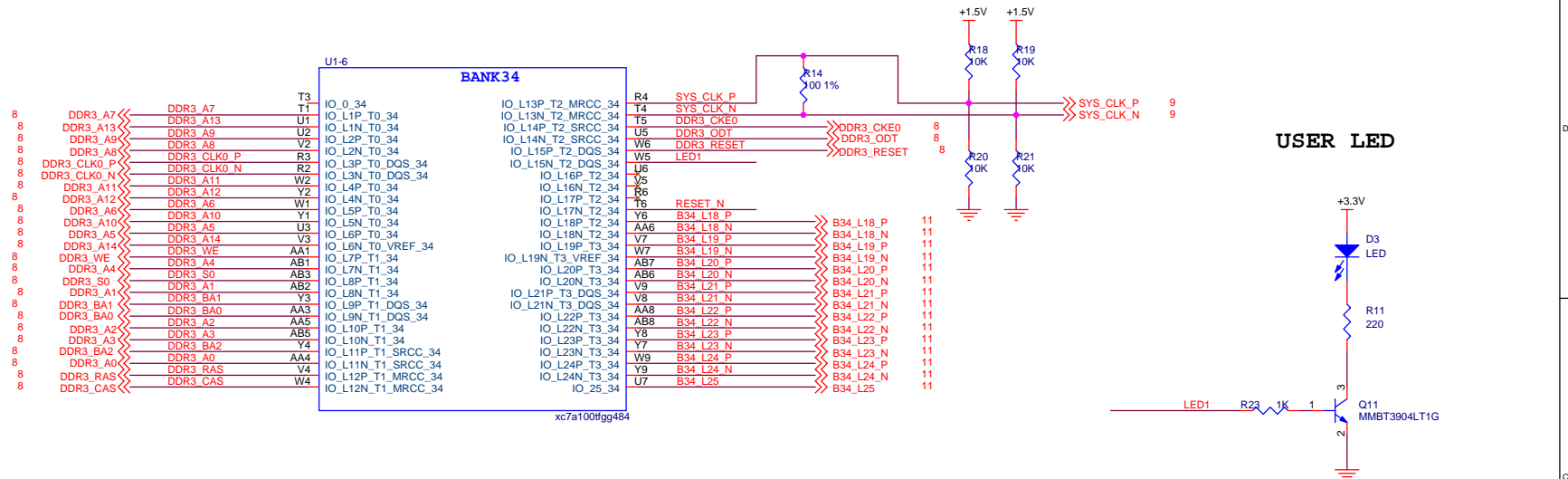




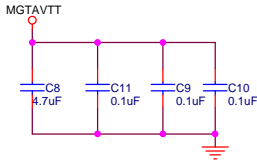
PUDC\_B=1: Deactive internal Pull up Resister



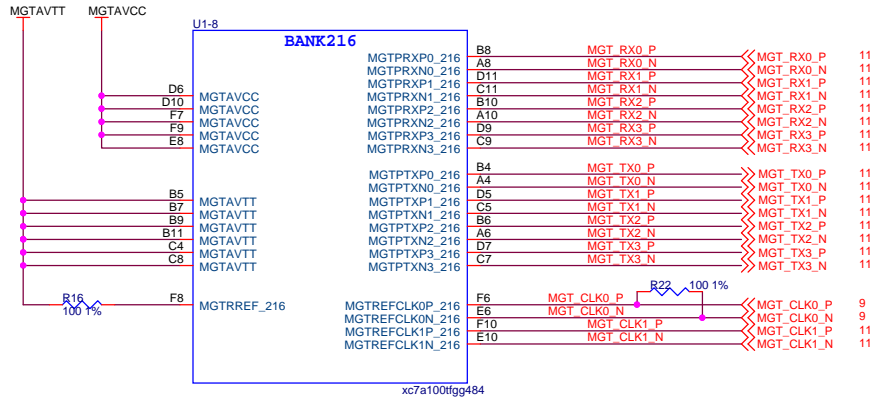
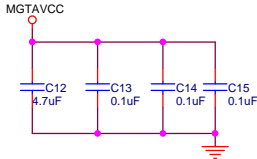




MGTAVTT 4.7uF(1) 0.1uF(2)



MGTAVCC 4.7uF(1) 0.1uF(2)





For VCCO\_13



For VCCO\_34



For VCCO\_14



For VCCO\_35



For VCCO\_15



For VCCO\_16

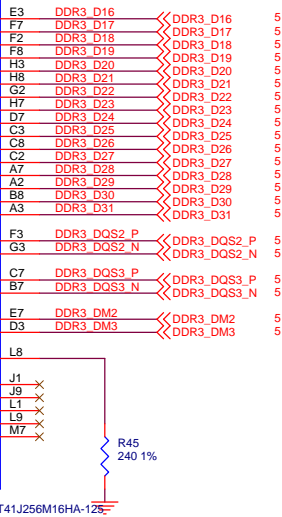
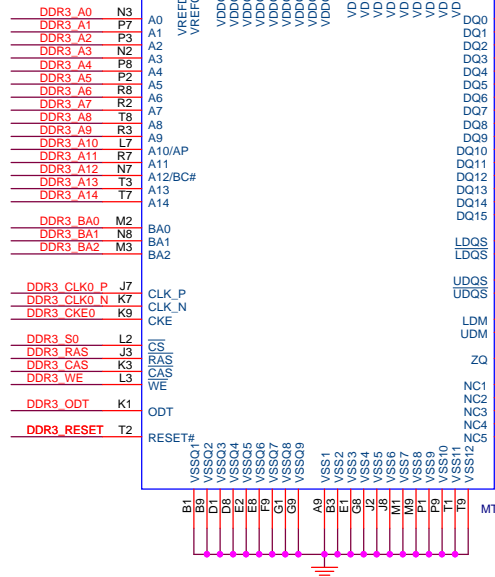
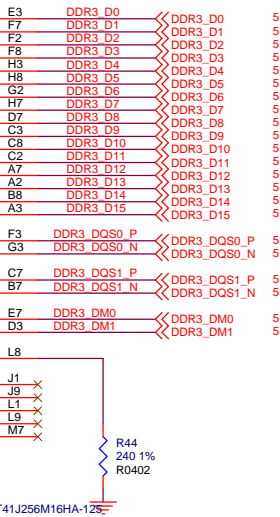
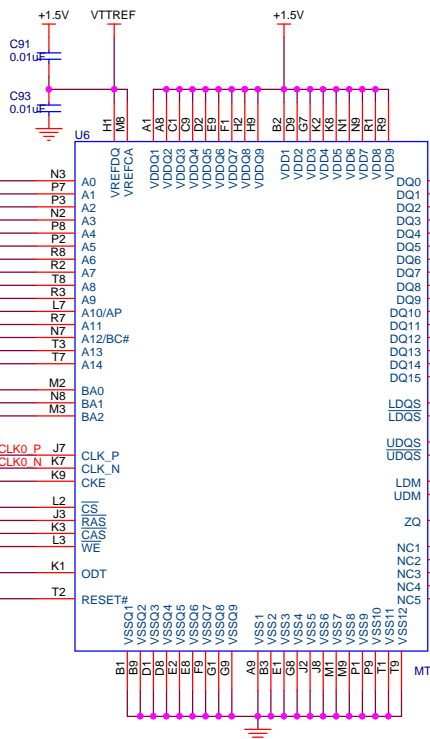
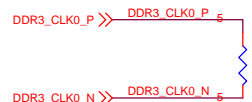
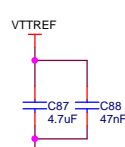
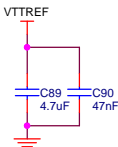
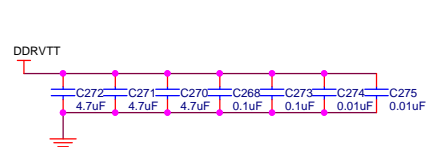
For VCCAUX

For VCCINT

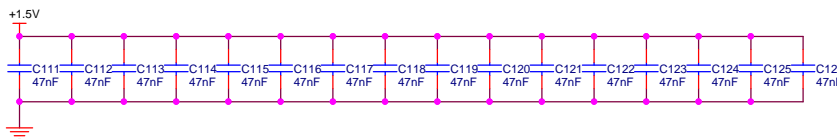
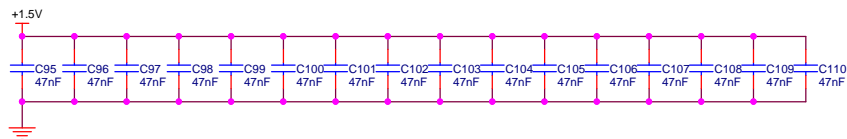
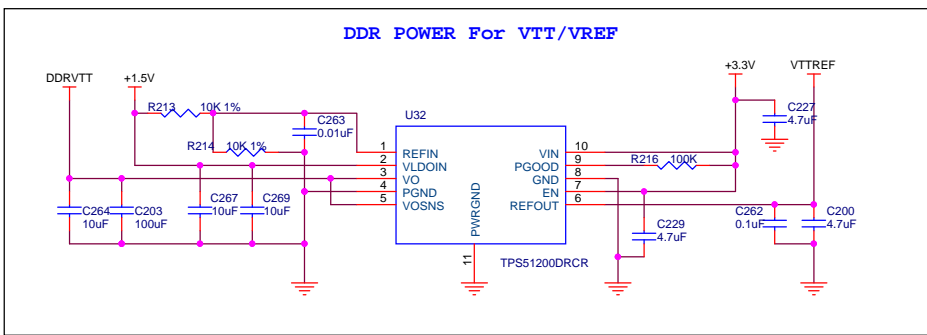


For VCCBRAM

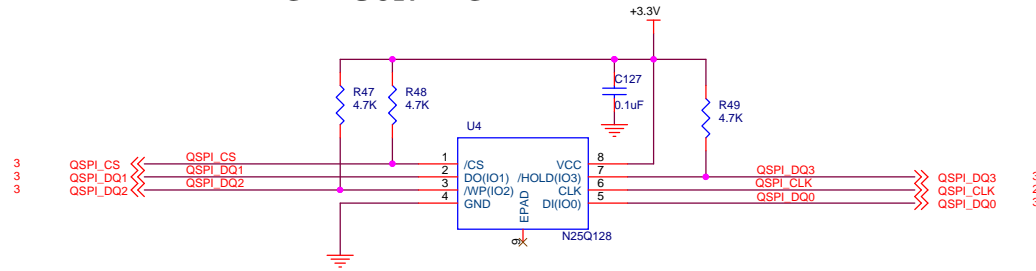




### DDR POWER For VTT/VREF

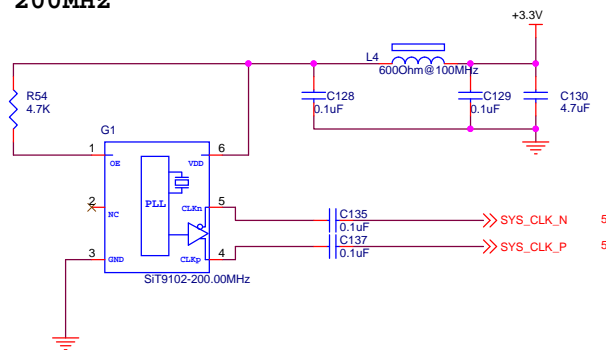


## FPGA CONFIG SPI



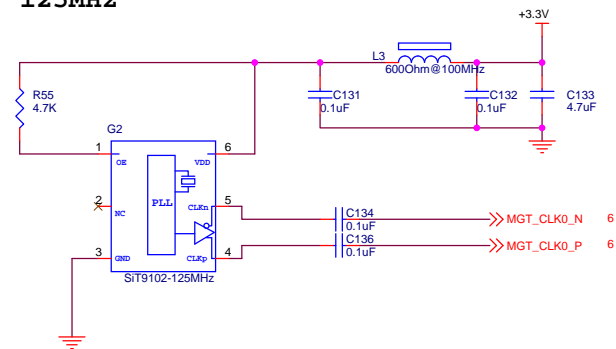
## SYSTEM CLOCK

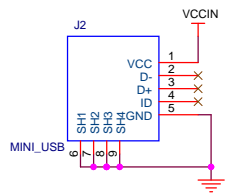
200MHz



## GTP CLOCK

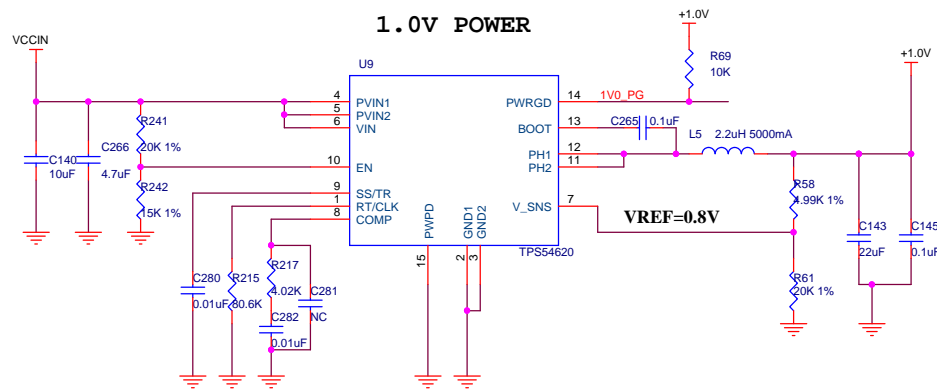
125MHz



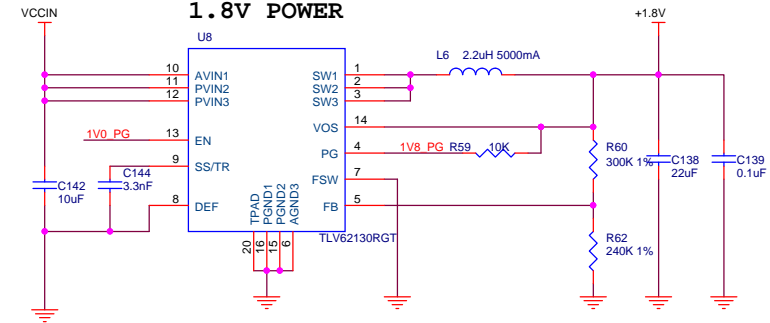


POWER ON: VCCINT(1.0V)->VCCBRAM(1.0V)->VCCAUX-(1.8V)>VCCO(1.5V and 3.3V)

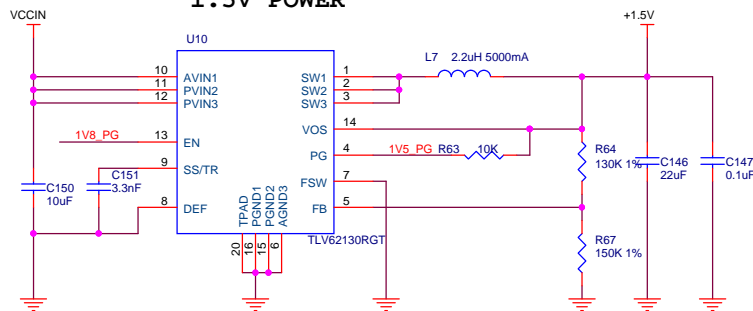
### 1.0V POWER



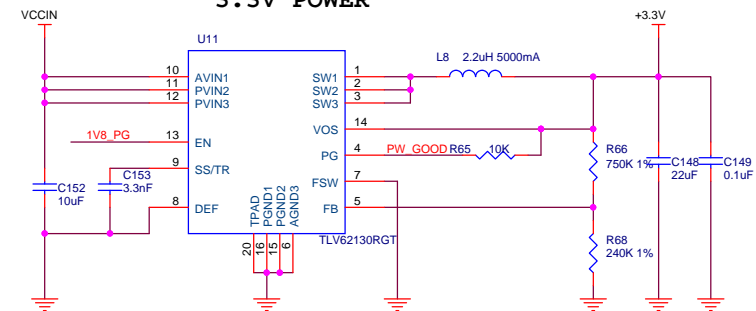
### 1.8V POWER



### 1.5V POWER

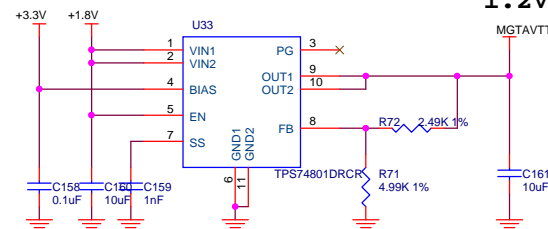


### 3.3V POWER

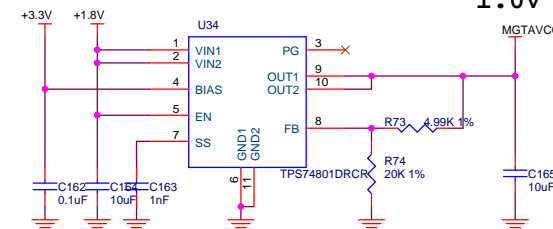


POWER ON: VCCINT(1.0V)->VMGTAVCC(1.0V)->VMGTAVTT(1.2V)

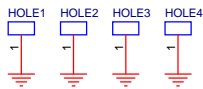
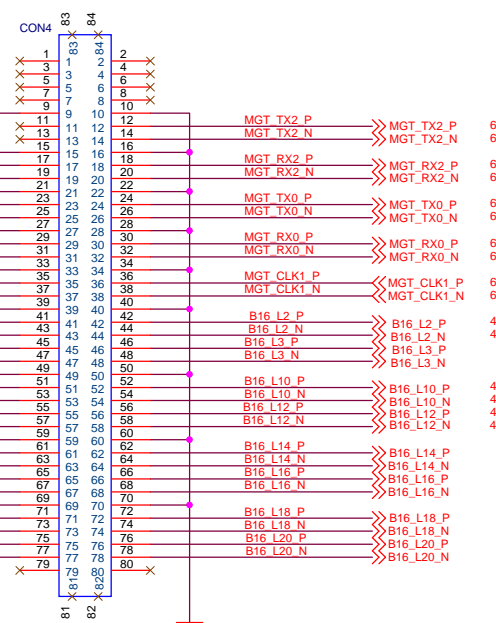
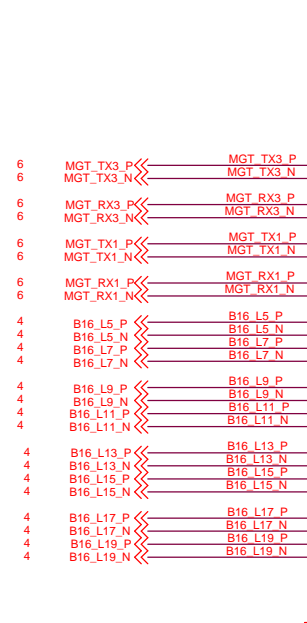
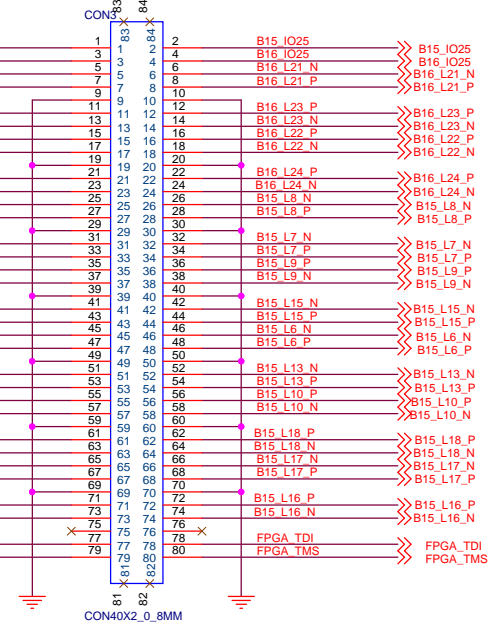
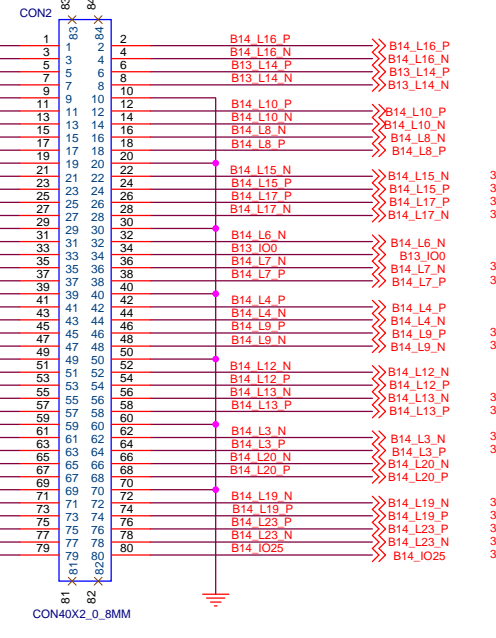
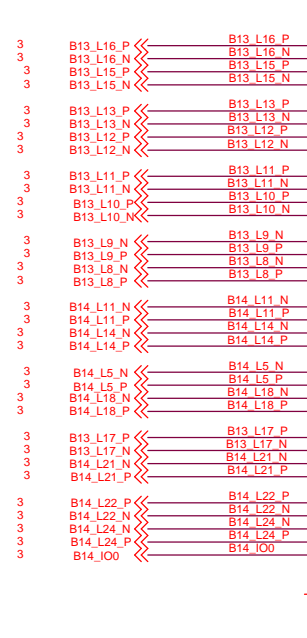
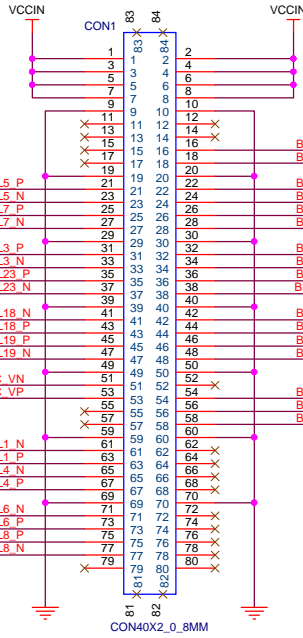
### 1.2V



### 1.0V



These IOs are on BANK34, Voltage is 1.5V!!!



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