Circuit Theory and Electronics Fundamentals

Lab 4: Audio Amplifier

Technological Physics Engineering

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Contents

1 Introduction

The main objective of this laboratory assignment is to study the circuit depicted in 1. We decided to separate this work in three different sections.

In the first one,Theoretical Analysis 2, we will analyze the circuit in 3 different time intervals, $t < 0$, $t = 0$ and $t > 0$. For the first 2 time intervals we will obtain linear equations using methods learnt in the TCFE class, which can be solved with $Octave$. These equation allow to find the voltage in each node and the current in each branch. With $t \to \infty$, a first order linear equation is obtained, which can be solved to obtain and plot the total solution of the circuit.

Using Ngspice tools, in the second section Simulation 3, we will present a simulation of the circuit and compare it with the previous theoretical results.

Lastly, Conclusion 4, the contents of the report will be summarised and the achieved results discussed.

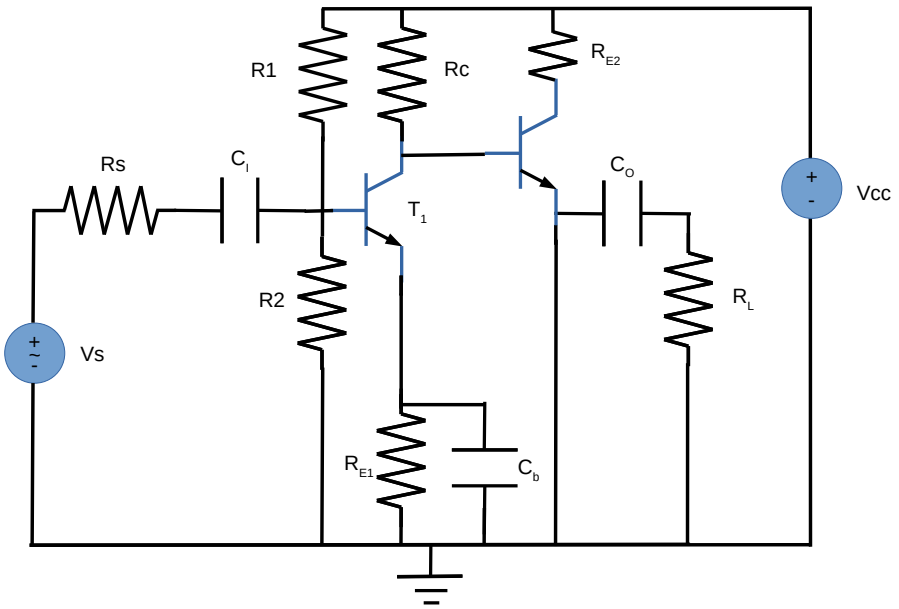

Figure 1: Complet circuit

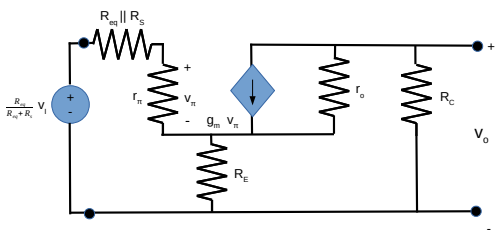

Figure 2: Circuit for the op analysis

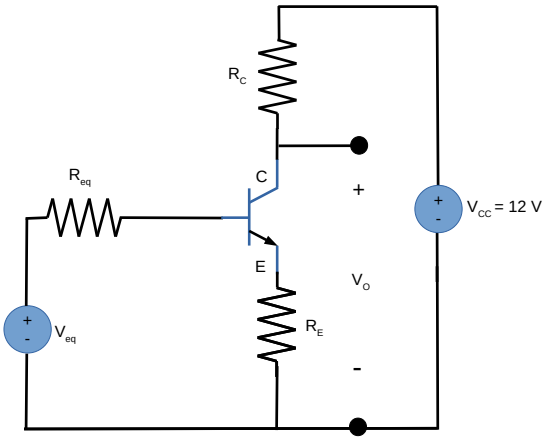

Figure 3: Complet for the incremental analysis

2 Theoretical Analysis

The configuration we decided to use for the gain stage of the audio amplifier circuit is the degenerated common emitter amplifier. The amplifier's power supply is at 12V, whereas the input source is just a small signal varying with time (10 mV). Unlike the amplifier's power supply it doesn't have a DC component. Therefore, if we connect the source directly into the input of the amplifier there will be a problem because there will not be enough voltage for the base emitter junction (BEJ) to be forwardly biased. If the BEJ is not forwardly biased the transistor is in the off state, it doesn't conduct current.

Consequently, we must find a way to ensure the transistor is always conducting while handling the low input signal. What we need is a coupling capacitor that works as a DC block, it separates the DC component at the base of the transistor and the DC component at the input, which is most likely zero. It allows the transistor to operate at its preferred point and not be disturbed by the input. Therefore, it has to be quite the large capacitor because it has to block frequency zero (DC).

In fact, VS can have any DC component because the capacitor works as a highpass filter, it only lets through frequencies higher than a certain value. Therefore, it blocks some low frequencies, which is one of the reasons why amplifiers struggle with lower cutoff frequencies. So, besides the coupling capacitor, we also need a bias circuit. The bias circuit connects two resistors RB1 and RB2 in series to a DC voltage source VCC so that by voltage dividision we get a suitable DC voltage going in to the base of the transistor, so that it is conducting. It is also very important that the transistor is in the forward active region so that it has a high current gain. It cannot be saturated and it cannot be in the cutoff state, it must be up and running.

2.1 Operating Point Analysis

In order to analyse this circuit, we start off with operating point (OP) analysis. In order to get rid of the complexity of the bias circuit, we can do a simple modification by using the Thévenin's equivalent of the bias circuit. Since we are doing OP analysis, we can ignore the input voltage source and the capacitor. The removal of the capacitor results in an open circuit so we can remove it and just consider the bias circuit and the transistor. In order to get the Thévenin's

equivalent of the bias circuit we "position" ourselves on the node connected to the base of the transistor and realise that resistors R_{B1} and R_{B2} can be put in parallel. Then, the voltage at that point will be the equivalent voltage given by

$$V_{eq} = -\frac{R_{B2}}{(R_{B1} + R_{B2})V_{CC}} \tag{1}$$

R_{eq} is given by $(R_{B1}R_{B2})/(R_{B1} + R_{B2})$. In order to compute the current going into the base of the transistor I_B we run mesh analysis and get

$$V_{eq} + R_{eq}I_B + V_{BEON} + R_E I_E = 0 \tag{2}$$

We can consider that $V_{BEON} = 0.7V$ when the BE junction is forwardly biased, like we did for the diode, especially when we have a base resistor, which is the case. Given that the transistor is in the forward active region, we know that $I_E = (1+\beta_F)I_B$, where β_F is the forward current gain. Therefore, we can replace I_E in the initial expression and we get

$$I_B = \frac{(V_{eq} + V_{BEON}}{R_B + (1 + \beta_F)R_E} \tag{3}$$

With the value of I_B we can compute the values of I_E and $I_C = \beta_F I_B$.

Having at these values and applying mesh analysis to the other mesh we get that the static output voltage is

$$V_O = V_{CC} – R_C I_C \tag{4}$$

The voltage at the emitter is given by $V_E = R_E I_E$. In order to confirm that the transistor is working in the forward active region (FAR) we compute V_{CE}, the voltage between the collector and the emitter, given by $V_{CE} = V_O - V_E$. If the value of V_{CE} is greater than V_{BEON} then the transistor is working in the FAR.

2.2 Incremental Analysis

Moving onto the incremental analysis of the circuit, we only consider the resistors, the capacitors and the incremental components of voltage and current. The coupling capacitor vanishes since we are working at medium frequencies, at which the capacitor is already a short circuit. The transistor is caracterized by 3 incremental parameters: resistor r_π between base and emitter, transconductance g_m between collector and emitter and output impedance of the transistor r_o between the collector and emitter, given by

$$g_m = \frac{I_C}{V_T} \tag{5}$$

$$r_\pi = \beta_F / g_m \tag{6}$$

$$r_o \approx V_A / I_C \tag{7}$$

Table 1: Simulation Analysis

Name	Value [A or V]
@vimb1[i]	5.054419e-05
@vimc1[i]	-8.75200e-03
@re[i]	8.802546e-03
v(emit)	6.601909e-01
vcc-v(coll1)	6.828931e+00
v(coll)-v(emit)	4.510878e+00
vcc-v(coll1)	6.828931e+00
@rout[i]	-8.00952e-02
i(vimc2)	7.947284e-02
vcc-v(emit2)	6.007137e+00

Table 2: Theoretical Analysis

Name	Value [A or V]
IB1	0.0000500
IC1	0.0089427
IE1	0.0089928
VE1	0.6744587
VO1	4.4880993
VCE	3.8136407
VI2	4.4880993
IE2	0.0908253
IC2	0.0904275
VO2	5.1880993

3 Simulation Analysis

Starting with the analysis of the oeprating point OP we obtain the following results.

Moving on to the next step, we obtain the input and output impedances and the gain. The results are showed below

Table 3: Simulation Analysis

Name	Value [A or V]
gain	3.859693e+01
zi	5.784117e-01
z0	8.000000e-03

Table 4: Theoretical Analysis

Name	Value [A or V]
AV1	-10.4237377
ZI1	480.3691691
ZO1	797.7437538
AV2	0.9913183
ZI2	7238.2775714
ZO2	0.2740644
ZOout	0.0058514

As we can see it is very obvious that the results of the voltages and currents are quite similar. Also the gain and the impedances are quite similar to what is expected. The results were very good overall.

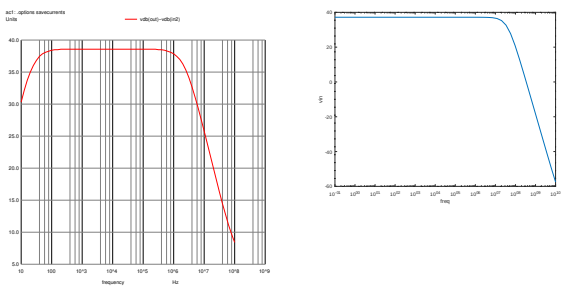

Figure 4: Representation of Vo(f)/Vi(f) in a logarithmic scale.

The graphics are very similar to each other so we can conclude that the results are good.

4 Conclusion

In this laboratory assignment the objective of develop a audio amplifier circuit has been achieved. The simulation results have matched with the theoretical results almost perfectly, means that the gain, the input and output impedances and Vo(f)/Vi(f) are similar in the two parts of this work.