浙江大学

本科实验报告

课程名称：计算机逻辑设计基础

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一、 实验目的和要求

1　实验目的

1.1　掌握七数码管显示原理

1.2　掌握七段码显示译码设计

1.3　进一步熟悉 Xilinx ISE 环境及 SWORD 实验平台

2　实验任务

2.1　任务 1：原理图设计实现显示译码 MyMC14495 模块

2.2　任务 2：用 MyMC14495 模块实现数码管显示

二、 实验内容和原理

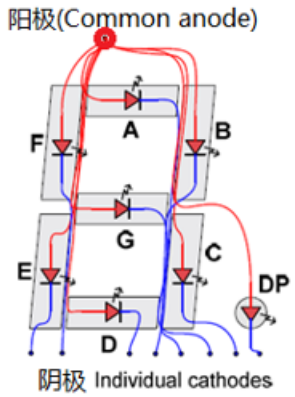
1　实验内容

1.1　原理图设计实现显示译码 MyMC14495 模块

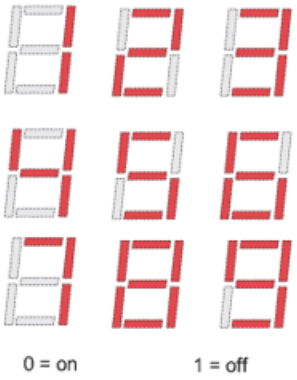
1.2　用 MyMC14495 模块实现数码管显示

2　实验原理

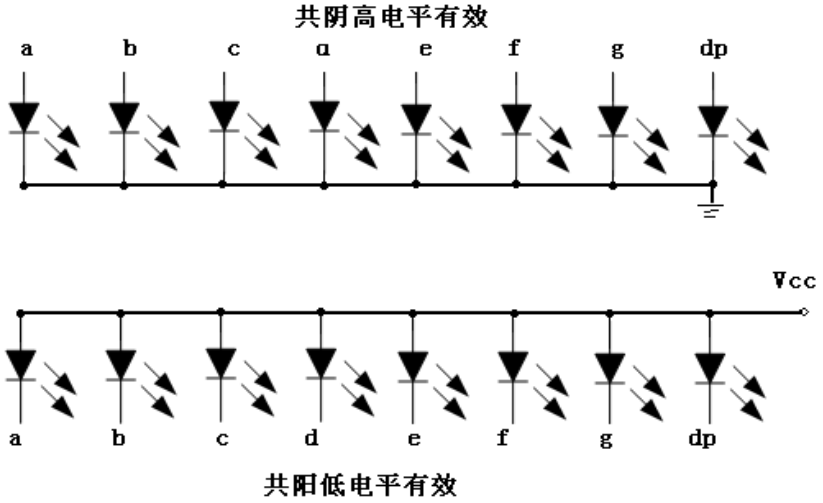
2.1　由 7+1 个 LED 构成的数字显示器件。每个 LED 显示数字的一段，另一个为小数点。



X	a	b	c	d	e	f	g
0	0	0	0	0	0	0	1
1	1	0	0	1	1	1	1
2	0	0	1	0	0	1	0
3	0	0	0	0	1	1	0
4	1	0	0	1	1	0	0
5	0	1	0	0	1	0	0
6	0	1	0	0	0	0	0
7	0	0	0	1	1	1	1
8	0	0	0	0	0	0	0
9	0	0	0	0	1	0	0
A	0	0	0	1	0	0	0
B	1	1	0	0	0	0	0
C	0	1	1	0	0	0	1
D	1	0	0	0	0	1	0
E	0	1	1	0	0	0	0
F	0	1	1	1	0	0	0



2.2　LED 的正极(负极)连在一起，另一端作为点亮的控制。共阳：正极连在一起，负极＝0，点亮；共阴：负极连在一起，正极＝1，点亮 。



2.3 根据真值表，化简逻辑函数

Hex	$D_3D_2D_1D_0$	BI/LE	a	b	c	d	e	f	g	p
0	0 0 0 0	0	0	0	0	0	0	0	1	p
1	0 0 0 1	0	1	0	0	1	1	1	1	p
2	0 0 1 0	0	0	0	1	0	0	1	0	p
3	0 0 1 1	0	0	0	0	0	1	1	0	p
4	0 1 0 0	0	1	0	0	1	1	0	0	p
5	0 1 0 1	0	0	1	0	0	1	0	0	p
6	0 1 1 0	0	0	1	0	0	0	0	0	p
7	0 1 1 1	0	0	0	0	1	1	1	1	p
8	1 0 0 0	0	0	0	0	0	0	0	0	P
9	1 0 0 1	0	0	0	0	0	1	0	0	P
A	1 0 1 0	0	0	0	0	1	0	0	0	P
B	1 0 1 1	0	1	1	0	0	0	0	0	P
C	1 1 0 0	0	0	1	1	0	0	0	1	P
D	1 1 0 1	0	1	0	0	0	0	1	0	P
E	1 1 1 0	0	0	1	1	0	0	0	0	P
F	1 1 1 1	0	0	1	1	1	0	0	0	P
X	x x x x	1	1	1	1	1	1	1	1	1

$$a=\bar{D}_3\bar{D}_2\bar{D}_1D_0+\bar{D}_3D_2\bar{D}_1\bar{D}_0+D_3\bar{D}_2D_1D_0+D_3D_2\bar{D}_1D_0$$

$$b=\bar{D}_3D_2\bar{D}_1D_0+D_2D_1\bar{D}_0+D_3D_2\bar{D}_0+D_3D_1\bar{D}_0$$

$$c=\bar{D}_3\bar{D}_2D_1\bar{D}_0+D_3D_2\bar{D}_0+D_3D_2D_1$$

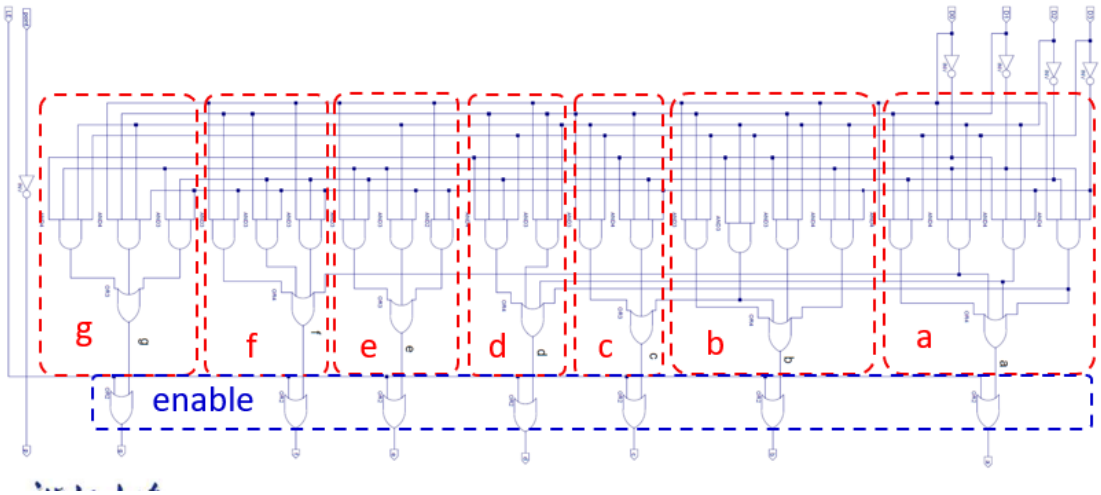
$$d=\bar{D}_3\bar{D}_2\bar{D}_1D_0+\bar{D}_3D_2\bar{D}_1\bar{D}_0+D_2D_1D_0+D_3\bar{D}_2D_1\bar{D}_0$$

$$e=\bar{D}_3D_0+\bar{D}_3D_2\bar{D}_1+\bar{D}_2\bar{D}_1D_0$$

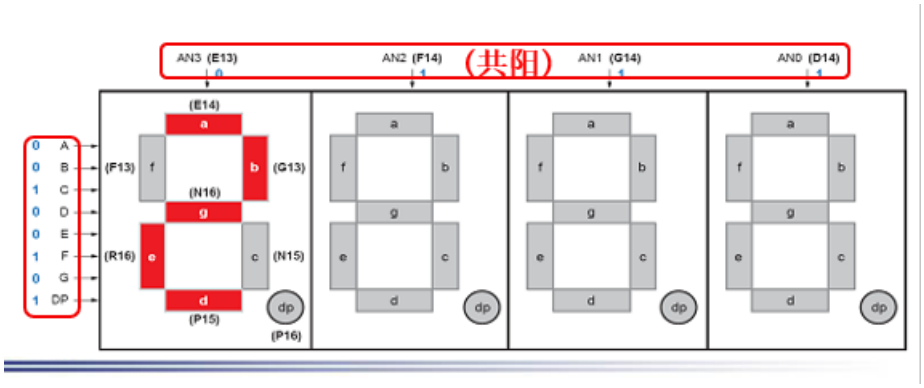
$$f=\bar{D}_3\bar{D}_2D_0+\bar{D}_3D_2D_1+\bar{D}_3D_1D_0+D_3D_2\bar{D}_1D_0$$

$$g=\bar{D}_3\bar{D}_2\bar{D}_1+\bar{D}_3D_2D_1D_0+D_3D_2\bar{D}_1\bar{D}_0$$

2.4 根据化简结果设计电路图



2.5 静态显示：每个 7 段码对应一个显示译码电路；动态扫描显示：时分复用显示，利用人眼视觉残留，一个 7 段码译码电路分时为每个 7 段码提供译码。控制时序：用定时计数信号控制公共极，分时输出对应七段码的显示信号动态扫描。：4 位七段码结构：正极：公共端，七段信号并联。



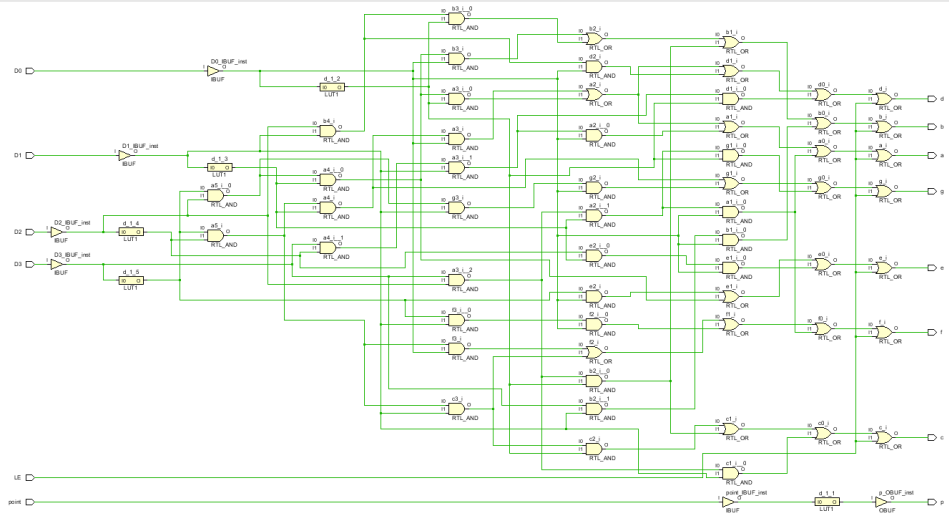
2.6 动态扫描：低电平与输入显示对应，共阳：低电平控制，分时送 a~g，p，可用序列信号控制。

三、 实验过程和数据记录

1 原理图设计实现显示译码 MyMC14495 模块

1.1 新建工程，工程名称用 MyMC14495。新建源文件，文件名称用 MyMC14495。原理图方式进行设计。Check Design Rules，检查错误。View HDL Functional Model，查看并学习 Verilog HDL 代

码



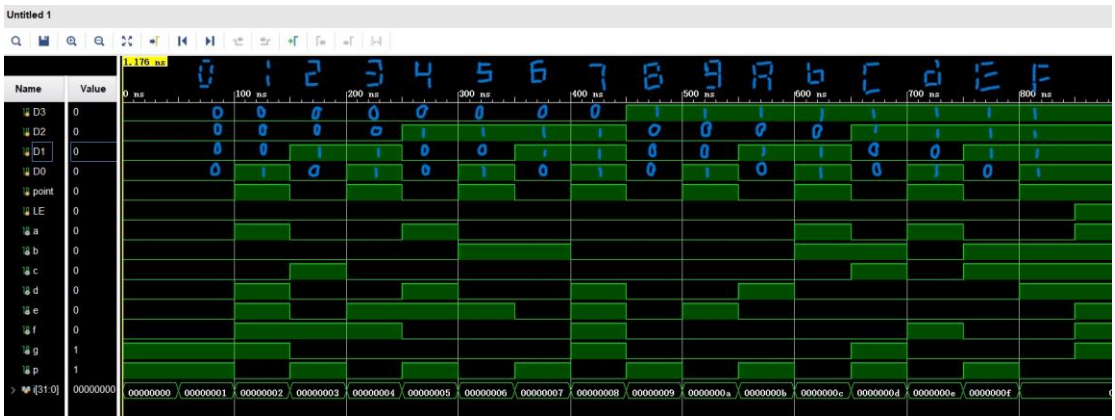
```
`timescale 1ns / 1ps
module MyMC14495 (
    D0,
    D1,
    D2,
    D3,
    point,
    LE,
    a,
    b,
    c,
    d,
    e,
    f,
    g,
    p
);
  input wire D0, D1, D2, D3, point, LE;
  output wire a, b, c, d, e, f, g, p;
  wire D0_N, D1_N, D2_N, D3_N;
  INV
      d_1_1 (
          p,
          point
      ),
      d_1_2 (
          D0_N,
          D0
      ),
```

```
    d_1_3 (
        D1_N,
        D1
    ),
    d_1_4 (
        D2_N,
        D2
    ),
    d_1_5 (
        D3_N,
        D3
    );
  assign a = (D3_N & D2_N & D1_N & D0 | D3_N & D2 & D1_N & D0_N | D3 &
D2_N & D1 & D0 | D3 & D2 & D1_N & D0)|LE;
  assign b = (D3_N & D2 & D1_N & D0 | D2 & D1 & D0_N | D3 & D2 & D0_N |
D3 & D1 & D0) | LE;
  assign c = (D3_N & D2_N & D1 & D0_N | D3 & D2 & D0_N | D3 & D2 & D1) |
LE;
  assign d = (D3_N & D2_N & D1_N& D0 | D3_N & D2 & D1_N & D0_N | D2 & D1
& D0 | D3 & D2_N & D1 & D0_N)|LE;
  assign e = (D3_N & D0 | D3_N & D2 & D1_N | D2_N & D1_N & D0) | LE;
  assign f = (D3_N & D2_N & D0 | D3_N & D2_N & D1 | D3_N & D1 & D0 | D3
& D2 & D1_N & D0) | LE;
  assign g = (D3_N & D2_N & D1_N | D3_N & D2 & D1 & D0 | D3 & D2 & D1_N
& D0_N) | LE;

endmodule
```

1.2 对 MyMC14495 模块进行仿真。

```
`timescale 1ns / 1ps
module MyMC14495_test ();
  reg D0, D1, D2, D3, point, LE;
  wire a, b, c, d, e, f, g, p;
  MyMC14495 UUT1 (

      D0,
      D1,
      D2,
      D3,
      point,
      LE,
      a,
      b,
```

```
      c,
      d,
      e,
      f,
      g,
      p
  );

  integer i;
  initial begin
    D3 = 0;
    D2 = 0;
    D1 = 0;
    D0 = 0;
    LE = 0;
    point = 0;
    for (i = 0; i <= 15; i = i + 1) begin
      #50;
      {D3, D2, D1, D0} = i;
      point = i;
    end

    #50;
    LE = 1;
  end

endmodule
```



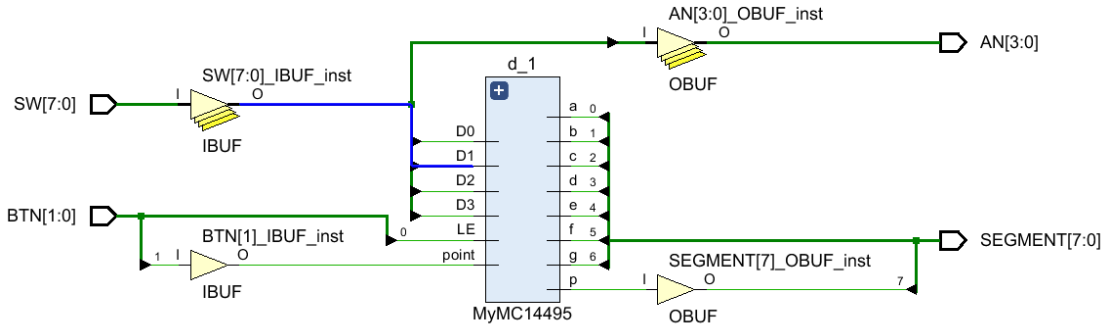
1.3 Create Schematic Symbol，系统生成 MyMC14495 模块的逻辑符号图文件，文件后缀.sym。符号图位于工程根目录。自动生成的符号可修改：可以用 Tools 菜单的 Symbol Wizard，也可以打

开.sym 文件直接修改。使用时必须复制.sym 和.sch 到对应工程目录

2 实现数码管显示

2.1 新建工程 DispNumber_sch。新建 schematic 文件 DispNumber_sch。复制 MyMC14495.sym 和.sch 到工程根目录。在 symbols 框里的第一个元件，就是 MyMC14495。

```
`timescale 1ns / 1ps
module DispNumber (
    SW,
    BTN,
    SEGMENT,
    AN
);
  input wire [7:0] SW;
  input wire [1:0] BTN;
  output wire [7:0] SEGMENT;
  output wire [3:0] AN;
  MyMC14495 d_1 (
      SW[0],
      SW[1],
      SW[2],
      SW[3],
      BTN[1],
      BTN[0],
      SEGMENT[0],
      SEGMENT[1],
      SEGMENT[2],
      SEGMENT[3],
      SEGMENT[4],
      SEGMENT[5],
      SEGMENT[6],
      SEGMENT[7]
  );
  assign AN[3:0]=~SW[7:4];

endmodule
```



2.2 UCF 引脚定义

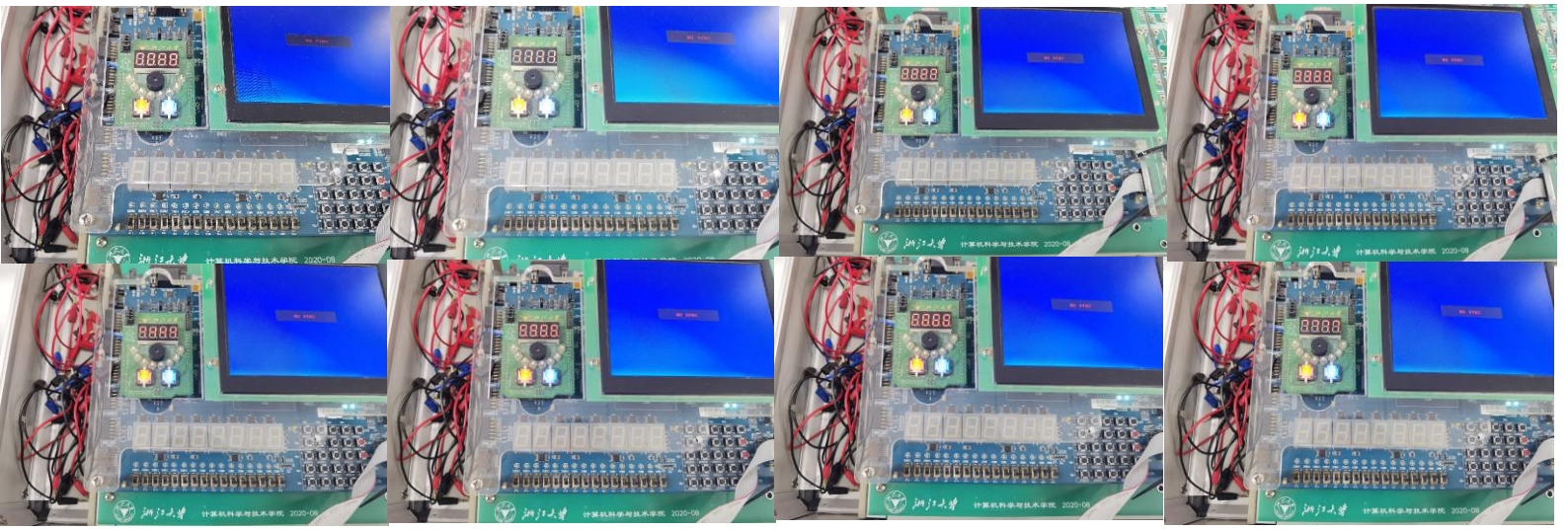
```
set_property IOSTANDARD LVCMOS33 [get_ports {AN[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {AN[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {AN[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {AN[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {SEGMENT[7]}]
set_property IOSTANDARD LVCMOS33 [get_ports {SEGMENT[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {SEGMENT[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {SEGMENT[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {SEGMENT[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {SEGMENT[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {SEGMENT[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {SEGMENT[0]}]
set_property IOSTANDARD LVCMOS15 [get_ports {BTN[1]}]
set_property IOSTANDARD LVCMOS15 [get_ports {BTN[0]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[7]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[6]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[5]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[4]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[3]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[2]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[1]}]
set_property IOSTANDARD LVCMOS15 [get_ports {SW[0]}]
set_property PACKAGE_PIN AF10 [get_ports {BTN[1]}]
set_property PACKAGE_PIN AF13 [get_ports {BTN[0]}]
set_property PACKAGE_PIN AA10 [get_ports {SW[0]}]
set_property PACKAGE_PIN AB10 [get_ports {SW[1]}]
set_property PACKAGE_PIN AA13 [get_ports {SW[2]}]
set_property PACKAGE_PIN AA12 [get_ports {SW[3]}]
set_property PACKAGE_PIN Y13 [get_ports {SW[4]}]
set_property PACKAGE_PIN Y12 [get_ports {SW[5]}]
set_property PACKAGE_PIN AD11 [get_ports {SW[6]}]
```

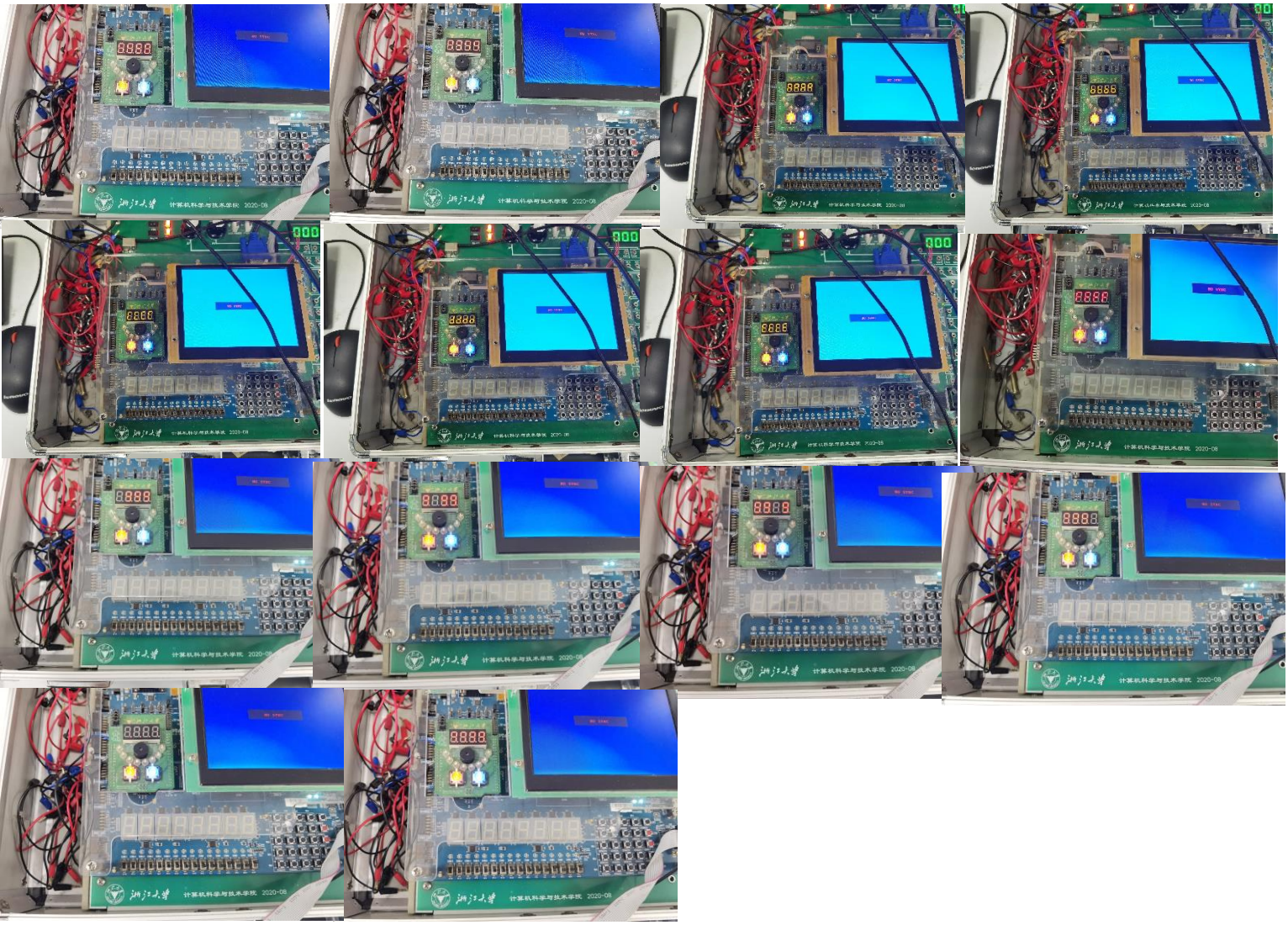
```
set_property PACKAGE_PIN AD10 [get_ports {SW[7]}]
set_property PACKAGE_PIN AB22 [get_ports {SEGMENT[0]}]
set_property PACKAGE_PIN AD24 [get_ports {SEGMENT[1]}]
set_property PACKAGE_PIN AD23 [get_ports {SEGMENT[2]}]
set_property PACKAGE_PIN Y21 [get_ports {SEGMENT[3]}]
set_property PACKAGE_PIN W20 [get_ports {SEGMENT[4]}]
set_property PACKAGE_PIN AC24 [get_ports {SEGMENT[5]}]
set_property PACKAGE_PIN AC23 [get_ports {SEGMENT[6]}]
set_property PACKAGE_PIN AA22 [get_ports {SEGMENT[7]}]
set_property PACKAGE_PIN AD21 [get_ports {AN[0]}]
set_property PACKAGE_PIN AC21 [get_ports {AN[1]}]
set_property PACKAGE_PIN AB21 [get_ports {AN[2]}]
set_property PACKAGE_PIN AC22 [get_ports {AN[3]}]
```

Tcl Console | Messages | Log | Reports | Design Runs | I/O Ports

Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip Ter
All ports (12)												
LED (7)	OUT			✓	12	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50
LED[6]	OUT		W23	✓	12	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50
LED[5]	OUT		AB26	✓	12	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50
LED[4]	OUT		Y25	✓	12	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50
LED[3]	OUT		AA23	✓	12	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50
LED[2]	OUT		Y23	✓	12	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50
LED[1]	OUT		Y22	✓	12	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50
LED[0]	OUT		AE21	✓	12	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50
Scalar ports (5)												
clk	IN		AC18	✓	32	LVCMOS18	1.800				NONE	NONE
F	OUT		AF24	✓	12	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50
S1	IN		AA10	✓	33	LVCMOS15*	1.500				NONE	NONE
S2	IN		AB10	✓	33	LVCMOS15*	1.500				NONE	NONE
S3	IN		AA13	✓	33	LVCMOS15*	1.500				NONE	NONE

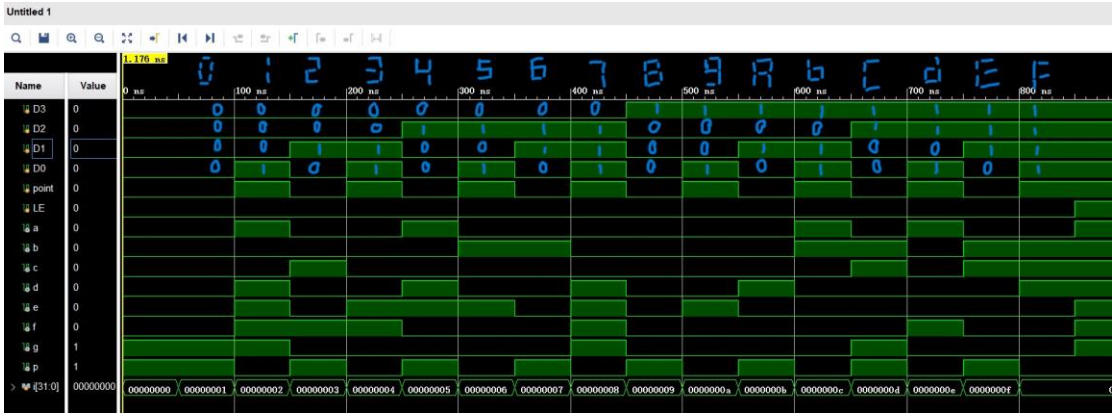
2.3 下载验证





四、 实验结果分析

1　仿真波形分析



先看最前面一段，D3~D0 为 b000 即，此时应当 a~f 数码管亮起，图中 a~f 为 0，其余为 1，符合预期，之后分析同理均符合预期。

2　下载验证分析，随着开关从 b0000 到 b1111，数码管显示从 0 到符合预期。

五、 讨论心得

本次实验是用七段数码管显示数字，从问题的提出到解决，里面运用了很多硬件的思维，这是与软件不同的，这个过程让我学到了很多这方面的思考方式。这次实验运用了理论课上学习到的卡诺图的知识，让我真切感受到了卡诺图的优越性。实验的 MyMC14495 数码管的原理图连线和开关都非常多，画起来很麻烦，通过自己的学习我发现用代码实现会简单不少，我会在今后学习更多 verilog 代码的知识。