# FSM in Verilog

Given the following device

Изображение выглядит как диаграмма, Технический чертеж, План, схематичный

Автоматически созданное описаниеPicture 1 – Computational Device

Device protocol

1. Inputs:

* clk: Clock signal.
* reset: Resets signal.
* req: Request signal to determine paths *a* or *b*.
* x and y: Operands inputs.
* op: Operation code.

1. Process:
   1. The device performs a computation (F) based on the opcode.
   2. It selects either a or b, depending on the req signal:
      * When req = 1, selected bus *a* (computation).
      * When req = 0, selected bus *b* (output).
   3. On a positive edge of clk, the computation (F) happens based on the current opcode.
   4. If reset != 1 device uses as *x* a result from previous computation.

1. Output:
   1. The result is shown when req = 0.
2. Reset:
   1. Reset signal sets all registers and inputs to 0.
3. Opcode encoding:
   * + opcode = 00: AND (x & y).
     + opcode = 01: NAND ~(x & y).
     + opcode = 10: NOR ~(x | y).
     + opcode = 11: XOR (a ^ b).

## Tasks

1.Draw the FSM diagram for this device.

Hint. Answer the following questions:

* 1. What states this device can be in?
  2. How does the transition between states happen (e.g. what signals change)?

2.Write a Verilog code.

## Code Run

iverilog -o FSM\_sim solution.v computation\_device\_tb.v

vvp FSM\_sim