Design of 800×2 Low-Noise Readout Circuit for Near-Infrared InGaAs Focal Plane Array

Huang Zhangcheng*[a], Huang Songlei[a], Fang Jiaxiong[a]
[a] State Key Laboratory of Transducer Technology, Shanghai Institute of Technical Physics, Chinese Academy of Sciences, Shanghai 200083, China

ABSTRACT

InGaAs near-infrared (NIR) focal plane arrays (FPA) have important applications in space remote sensing. A design of 800×2 low-noise readout integrated circuit (T800 ROIC) with a pitch of 25 μm is presented for a dual-band monolithic InGaAs FPA. Mathematical analysis and transient noise simulations have been presented for predicting and lowering the noise in T800 ROIC. Thermal noise from input-stage amplifier which plays a dominant role in ROIC is reduced by increasing load capacitor under tradeoff and a low input offset voltage in the range of ±5 mV is obtained by optimizing transistors in the input-stage amplifier. T800 ROIC has been fabricated with 0.5-μm 5V mixed signal CMOS process and interfaced with InGaAs detector arrays. Test results show that ROIC noise is around 90 μV and input offset voltage shows a good correspondence with simulation results. 800×2 InGaAs FPA has a peak detectivity (D^*) of about 1.1×10^{12} $cmHz^{1/2}/W$, with dynamic range of above 80dB.

Keywords: infrared FPA, ROIC, low noise, input offset voltage

INTRODUCTION

InGaAs near-infrared focal plane array has wide applications in space remote sensing, NIR spectroscopy and night vision [1][2]. As InGaAs detector has a high detectivity from 0.9 μm to 1.7 μm at room temperature with its lattice matched to InP substrate, there has been strong interest in developing InGaAs FPA as optoelectronic sensor for remote sensing [3]. In general, InGaAs FPA consists of two major parts, namely InGaAs detector arrays and the readout integrated circuit. In the past years, the advances of detector fabrication technology have led to the rapid development of InGaAs detector array [4]. At present, for many mature InGaAs FPA detector technologies, it is the readout electronics that limit performance rather than the detector itself.

In this paper, a design of low-noise 800×2 CMOS ROIC for near-infrared InGaAs focal plane array is presented. The first section describes basic architecture of ROIC. The second section presents a mathematical analysis of total noise and the design method of low-noise ROIC circuit. To obtain low dark current in FPA, the next section discusses the input offset voltage of input amplifier. The last section will present performance measurements and comparison with calculation results.

800×2 ROIC ARCHITECTURE

InGaAs near-infrared focal plane array has been studied in Shanghai Institute of Technical Physics (SITP) for several years [5][6]. Now there is a great interest in developing an 800×2 InGaAs NIR focal plane array for dual-band detection. This paper reports the development of 800×2 low-noise ROIC (T800) suitable for dual-band monolithic InGaAs detector arrays.

T800 ROIC consists of two parallel 800×1 linear arrays with 25μm pixel pitch. Figure 1 shows the architecture of unit circuit in T800 ROIC.

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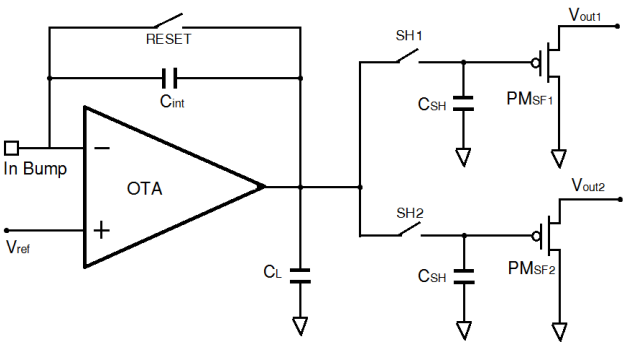

Figure 1. Architecture of unit circuit in T800 ROIC

The input stage of unit circuit is based on capacitive-feedback transimpedance amplifier (CTIA), which interfaces the InGaAs pixel and performs current-to-voltage conversion. It consists of an operational transimpedance amplifier (OTA) with a capacitor (C_{int}) connected in feedback loop. High ratio of current-to-voltage can be achieved if the integration capacitor is small; however it leads a low dynamic range as the full well capacity directly scales with integration capacitor. For our design we chose an integration capacitor of 0.5 pF for the high dynamic range need of the application.

It is necessary to consider how to realize low-noise performance in the design trade-off of a high-dynamic-range ROIC pixel. The load capacitor (C_L) is added at output node of OTA to reduce the input stage noise by lowering the close loop bandwidth of CTIA, meanwhile, Correlated Double Sampling (CDS) is used to remove KTC noise and reduce the low-frequency noise from InGaAs detector and input stage amplifier. By CDS, T800 reads pixel signal two times – once at the beginning of the integration time, and another at the end. Effective signal is obtained by subtraction of the two samples. At the output stage, source follower is involved to transfer parallel to serial and drive the bus.

NOISE ANALYSIS AND OPTIMIZATION

In low-noise design, a careful analysis of each noise source is necessary. In InGaAs FPA, typical noise mechanisms include InGaAs detector thermal noise, shot noise, CTIA KTC noise, amplifier thermal noise, 1/f noise, KTC noise from sample circuit, SF output stage noise, and so on.

The detector thermal noise σ_{TH} and shot noise σ_{DK} (from dark current) can be given [7]:

$$\sigma_{TH} = \sqrt{2kTt_{\text{int}} / R_{\text{det}}} / q \tag{1}$$

$$\sigma_{DK} = \sqrt{|I_{DK}| t_{\text{int}} / q} \tag{2}$$

where R_{det} is detector resistance, t_{int} is integration time, I_{DK} is dark current, T is temperature, and k is the Boltzmann constant.

When CTIA starts working in integration mode, the noise from last reset mode will be added in integration voltage at the beginning. The CTIA KTC noise, σ_{RST}, consists of two terms: one comes from reset switch and another originates from the amplifier noise, which can be given [8]:

$$\sigma_{RST} = \sqrt{kT(C_{\text{int}} + C_{\text{det}}(C_L + 2\alpha C_{\text{det}}) / C_{tot})} / q \tag{3}$$

where $C_{tot} = C_{int} + C_{det} + C_L$, $\alpha = 2(1+g_{m7}/g_{m1})/3$, C_{det} is detector capacitor, g_{m1} and g_{m7} are transconductance of input transistor and load transistor in OTA respectively.

Mostly the thermal noise of CTIA amplifier is one of the dominant noise sources in the circuit. The small signal equivalent circuit for OTA thermal noise analysis is shown in Figure 2.

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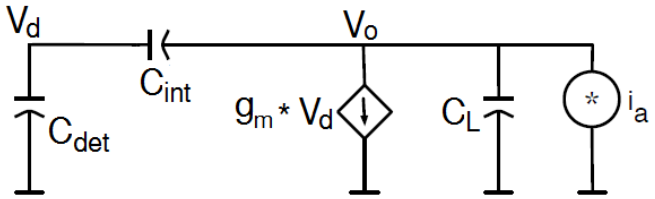

Figure 2. Small signal equivalent circuit for OTA thermal noise analysis

The transfer function from the amplifier noise current to output voltage is

$$H_a(s) = \frac{v_o}{i_a} = \frac{C_{\det} + C_{\text{int}}}{C_x s + g_m C_{\text{int}}} \tag{4}$$

where $C_x = C_{int}C_{det} + C_{det}C_L + C_LC_{int}$, g_m is transconductance of OTA.

The one-sided noise current power spectral density (PSD) in units (A^2/Hz) from differential amplifier is

$$S_a(f) = 8\alpha kTg_m \tag{5}$$

The equivalent input noise in units (e-) can be written:

$$\sigma_{AMP} = \frac{C_{\text{int}}}{q}\sqrt{\int_0^\infty |H_a(f)|^2 S_a(f)df} = \frac{C_{\det} + C_{\text{int}}}{q}\sqrt{2\alpha kTC_{\text{int}} / C_x} \tag{6}$$

The S&H noise, σ_{SH}, can be given:

$$\sigma_{SH} = \frac{C_{\text{int}}}{q}\sqrt{\frac{2kT}{C_{SH}}} \tag{7}$$

where C_{SH} is sample capacitor.

And the noise from SF output stage:

$$\sigma_{SF} = \frac{C_{\text{int}}}{q}\sqrt{\frac{2}{\pi R_{out}C_{out}}\frac{4kT}{g_{m,SF}}} \tag{8}$$

CTIA KTC noise σ_{RST} and low-frequency (smaller than $1/t_{int}$) 1/f noise can be greatly cancelled by CDS, however, CDS will increase the thermal noise from CTIA OTA by a square root of two because of double samples. The OTA thermal noise after CDS in units (e-) can be written:

$$\sigma_{AMP,CDS} = \frac{C_{\det} + C_{\text{int}}}{q}\sqrt{4\alpha kTC_{\text{int}} / C_x} \tag{9}$$

Table 1 summarizes the expressions and calculation results of noise in T800 ROIC and 800×2 InGaAs NIR FPA.

As shown in table 1, noise level in ROIC after CDS is 331 e- which is better than noise level (488 e-) without CDS. The OTA thermal noise plays a dominant role in whole ROIC noise mechanisms.

Equation 7 and 9 show that ROIC noise can be reduced by increasing load capacitor C_L and sample capacitor, C_{SH}, however, this also increase the layout area of unit circuit. It is necessary to compare ROIC noise to InGaAs noise, for it is useless to lower FPA noise with load capacitor increment if the global FPA noise performance is limited by detectors [9].

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Table 1. FPA and ROIC Noise Calculation Results

Item	Expression	Noise (CDS) /e-	Noise (non CDS) /e-
detector thermal noise, σ_{TH}	$\sqrt{2kTt_{\text{int}} / R_{\text{det}}} / q$	450	450
dark shot noise, σ_{DK}	$\sqrt{\lvert I_{DK}\rvert t_{\text{int}} / q}$	125	125
reset noise, σ_{RST}	$\sqrt{kT(C_{\text{int}} + C_{\text{det}}(C_L + 2\alpha C_{\text{det}}) / C_{tot})} / q$	0	402
OTA thermal noise, $\sigma_{AMP,CDS}$	$(C_{\text{det}} + C_{\text{int}})\sqrt{4\alpha kTC_{\text{int}} / C_x} / q$	258	182 ①
S&H noise, σ_{SH}	$C_{\text{int}}\sqrt{2kT / C_{SH}} / q$	201	201
SF output noise, σ_{SF}	$C_{\text{int}}\sqrt{8kT / \pi g_{m,SF} R_{out} C_{out}} / q$	59	59
total detector noise, σ_{DET}	$\sqrt{\sigma_{TH}^2 + \sigma_{DK}^2}$	466	466
total ROIC noise, σ_{ROIC}	$\sqrt{\sigma_{AMP,CDS}^2 + \sigma_{SH}^2 + \sigma_{SF}^2}$	331	488
total FPA noise, σ_{FPA}	$\sqrt{\sigma_{DET}^2 + \sigma_{ROIC}^2}$	573	676

① The expression of OTA thermal noise without CDS is shown in Equation 6.

The value of C_L and C_{SH} are specified when ROIC noise power is a half of InGaAs detector noise power. Transient noise simulation results of T800 ROIC versus C_L and C_{SH} are shown in Fig 3. T800 ROIC noise is less than 320 e- if we choose C_L = 3 pF, C_{SH} = 2 pF. Results of 800 transient noise simulations are shown in Fig 4. The standard deviation is found to be 321 e-, which approaches the calculation results.

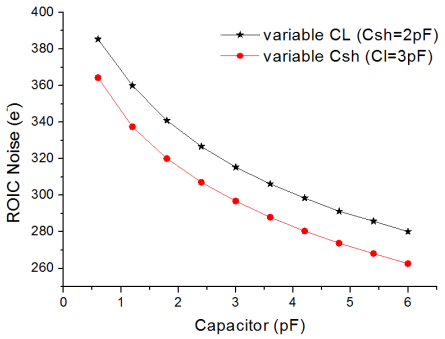

Figure 3. ROIC noise simulation results vs. C_L, C_{SH}

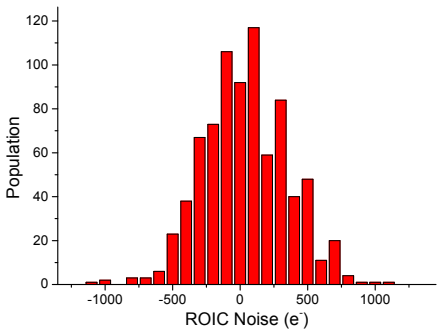

Figure 4. Histogram of ROIC noise simulation results

INPUT OFFSET VOLTAGE ANALYSIS

Another key element is dark current in FPA. Low dark current is needed for lowering shot noise from dark current and fixed pattern noise. Under a simplifying assumption, the detector resistance near zero-bias is invariable. The dark current in InGaAs FPA can be given as:

$$I_{DK} = V_{os} / R_{\text{det}} \tag{10}$$

where V_{os} is input offset voltage of CTIA OTA.

For FPA, it is useful to achieve small dark current by reducing V_{os} in CTIA OTA [10]. The architecture of CTIA OTA is shown in Fig 5.

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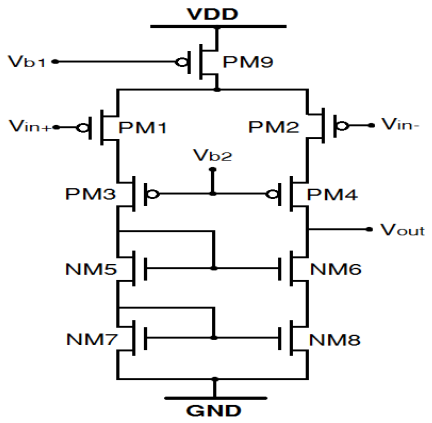

Figure 5. CTIA OTA

V_{os} is determined primarily by input transistor (M1, M2)and load transistor (M7, M8), which is given as:

$$V_{os,in} = \left\{ \frac{\left|V_{GS} - V_{TH,P}\right|_1}{2} \left[\frac{\Delta(W/L)}{(W/L)} \right]_1 + \Delta V_{TH,P} \right\} + \left\{ \frac{\left|V_{GS} - V_{TH,N}\right|_7}{2} \left[\frac{\Delta(W/L)}{(W/L)} \right]_7 + \Delta V_{TH,N} \right\} \frac{g_{m7}}{g_{m1}} \qquad (11)$$

$\Delta V_{TH,P}$ and $\Delta V_{TH,N}$ will be greatly reduced if the layout of transistors using multiple fingers are perfectly symmetrical, then the next approach is to specify $(W/L)_1$ and $(W/L)_7$. Monte Carlo simulation results of V_{os} versus $(W/L)_1$ are illustrated in Fig 6. The standard deviation of V_{os} is about 5mV when $(W/L)_1 = 10$ and $(W/L)_7 = 4$, and the increment improvement in V_{os} decreases slightly for larger $(W/L)_1$ and $(W/L)_7$. Results of 800 Mento Carlo simulations are shown in Fig 7. Substituting simulation results of V_{os} into Eq. (10) gives $I_{DK} \approx 0.67$ pA.

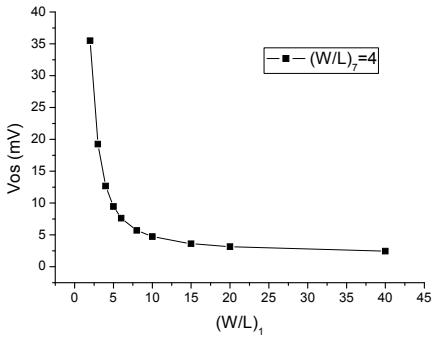

Figure 6. V_{os} simulation results vs. $(W/L)_1$

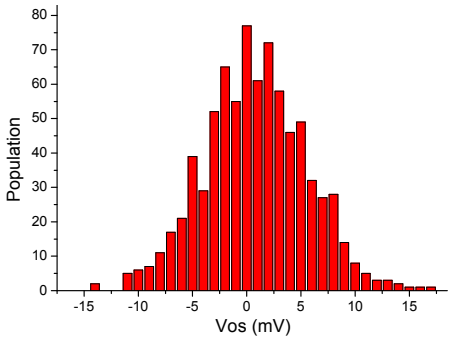

Figure 7. Histogram of V_{os} simulation results

MEASUREMENTS

T800 ROIC is fabricated using a 5 V 0.5-μm CMOS technology, which measures 21.2 mm × 6.1 mm of one die. The measured T800 ROIC and FPA performances are summarized in table 2.

Noise measurements were conducted by sampling 100 consecutive frames and performing standard deviation calculation for each pixel. The ROIC noise is 352 e- which is slightly more than results of mathematical calculation (331 e-) and transient noise simulations (321 e-). Additional noise may originate from bias voltage and clocks. The dynamic range of 800×2 InGaAs FPA is above 80 dB, and peak detectivity is about 1.1×10^{12} cmHz$^{1/2}$/ W. These attributes result in a high image quality for remote sensing.

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Table 2. T800 ROIC Measurement

Parameter	Typical Value	Comments
Array Format	800×2	
Pixel Pitch	25 μm	
ROIC Noise	352 e- / 90 μV	rms@25℃
FPA Noise	586 e- / 150 μV	rms@5ms, 25℃
Full Well Capacity	6,640,000 e-	
Power Consumption	36 mW	
Dynamic Range	81 dB	InGaAs FPA@5ms, 25℃
Peak Detectivity	1.1×10^{12} cmHz$^{1/2}$/ W	@5 ms, 25℃
Non-Linearity	<5%	
Dark Current	-0.6 pA~0.6 pA	FPA@25℃

FPA Noise measurements and calculated results versus integration time are plotted in Fig 8. The measurement results performed shows an approximate correspondence with theoretic analysis. Dark current distribution of measurements is shown in Fig 9. Dark currents in 800×2 InGaAs FPA are measured to be in the range of ±0.6 pA at 25℃, which coinciding well with calculation results. Dark current tests show that V_{os} of CTIA OTA is about in the range of ±5 mV

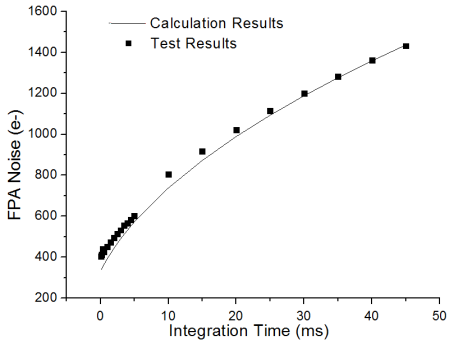

Figure 8 Comparison of tests and calculations

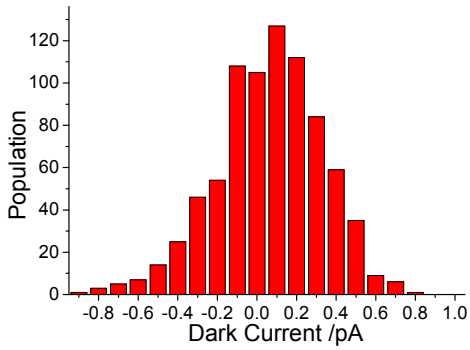

Figure 9 Histogram of I_{DK} test results

CONCLUSIONS

A 25 μm pixel-pitch, 800×2 CTIA ROIC (T800) for a dual-band monolithic InGaAs FPA has been developed. Mathematical analysis and transient noise simulations have been presented for predicting and lowering the noise in T800 ROIC. Its pixel has a full-well-capacity of about 6,640,000 e- with an input referred read noise of 352 e-. The T800 ROIC runs on 5 V supply voltage and dissipates about 36 mW. Input offset voltage has been limited in the range of ±5 mV to decrease the dark current in InGaAs FPA. It has been fabricated using a 0.5-μm CMOS process and interfaced with InGaAs detector arrays. Due to low-noise and low-input-offset performance of ROIC, InGaAs FPA has a peak detectivity of about 1.1×10^{12} cmHz$^{1/2}$/ W, with dynamic range of above 80 dB.

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