OmniVision

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datasheet

PRODUCT SPECIFICATION

companion ISP processor

OV490

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companion ISP processor

datasheet (BGA)
PRODUCT SPECIFICATION

version 2.0
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To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- rear view camera
- surround view system
- camera monitoring system

ordering information

- **OV00490-B00G-1B** (lead-free)
  100-pin BGA, packed in tray
- **OV00490-B00G-TB** (lead-free)
  100-pin BGA, packed in tape and reel

features

- feature set optimized for next generation surround view applications
- simultaneous output of fully processed YUV for display based applications and RAW only to enable machine vision downstream processing
- parallel processing of two input streams
- industry leading HDR technology, third generation HDR technology allows capturing of more details in bright and dark environments
- JTAG boundary scan
- high speed serial data transfer with MIPI CSI-2
- embedded information including: frame counter, temperature and register data in each image to enable critical automotive safety applications
- industry's first features to improve image harmonization and synchronization for surround view applications
- SCCB master interface for automatic sensor configuration at power-on
- SCCB slave interface for OV490 configuration by host
- on chip PLL to generate stable internal clock frequency
- on chip voltage regulator 3.3V/1.8V to 1.2V
- brown-out detection circuit and output flag
- embedded 32-bit RISC processor for high performance and great flexibility
- supports 1K bits of one time programmable memory (OTP)
- advanced ISP for high quality image capturing and video streaming
- advanced auto white balance (AWB)
- AEC/AGC with statistical data from hardware engine and algorithm running on RISC
- support of four user-defined ROI windows for statistics
- DNS (RAW de-noise) and CIP (de-mosaic)
- supports power cut mode designed for power saving during system quiescence
- AEC-Q100 grade 2 qualification

key specifications

- **power supply:**
  core: 1.2V ± 10%
  I/O: 1.8V ± 10% or 3.3V ± 10%
- **temperature range:**
  operating: -40°C to +105°C ambient temperature
- **power requirements:** 250 mA
- **package dimensions:** 7 mm x 7 mm

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table of contents

1 signal descriptions 1-1
1.1 2x2 lane MIPI configuration 1-1
1.2 1x4 lane MIPI configuration 1-4
1.3 power domain 1-9
2 system level description 2-1
2.1 overview 2-1
2.2 input and output formats 2-2
2.3 voltage regulator 2-3
2.4 system clock (PLL) 2-4
2.4.1 clock network 2-5
2.5 power-on sequence 2-7
2.6 power-off sequence 2-8
2.7 4-wire serial interface 2-9
2.8 SCCB interface 2-10
2.8.1 SCCB master mode program 2-10
2.9 direct memory access (DMA) 2-13
2.10 input data conversion (IDC) 2-13
2.11 VFIFO 2-13
2.12 system control (SC) 2-14
2.13 system boot up 2-14
2.13.1 boot from host by 4-wire serial interface master flash 2-14
2.13.2 boot by 4-wire serial interface slave 2-18
2.13.3 boot up from EEPROM by SCCB master 2-21
2.13.4 boot from host by SCCB slave 2-24
2.14 RISC CPU 2-26
2.15 general purpose I/O (GPIO) 2-26
2.16 UART 2-26
2.17 brown-out detection 2-27
2.18 temperature sensor 2-27
2.19 embedded line 2-28
2.19.1 check-sum algorithm 2-29
2.20 host command control 2-30
2.20.1 host control concept 2-30

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2.20.2 host command list 2-30
2.21 color bar 0/1/2 2-31
2.22 one time programmable memory (OTP) 2-31
3 image processor digital functions 3-1
3.1 image processor 3-1
3.2 test pattern 3-3
3.3 color bar 3-3
3.4 square 3-4
3.5 random data 3-4
3.6 transparent effect 3-4
3.7 rolling bar effect 3-5
3.8 lens correction (LENC) 3-5
3.8.1 multi LENC function 3-53
3.9 auto white balance (AWB) 3-56
3.9.1 WB gain 3-56
3.9.2 AWB statistics 3-61
3.9.3 AWB gain mode 3-67
3.9.4 AWB algorithm 3-70
3.9.5 advanced AWB 3-71
3.10 defect pixel correction (DPC) 3-74
3.11 de-noise (DNS) 3-105
3.11.1 noise list 3-106
3.11.2 RAW DNS 3-106
3.11.3 UVDNS 3-113
3.12 combine 3-116
3.13 HDR gain 3-124
3.14 tone mapping 3-125
3.14.1 global tone mapping 3-126
3.14.2 local tone mapping 3-129
3.14.3 tone mapping curve 3-136
3.15 piecewise linear (PWL) 3-145
3.16 linear stretch 3-146
3.17 color interpolation (CIP) 3-150
3.17.1 color interpolation 3-150
3.17.2 DNS in CIP 3-151
3.17.3 edge sharpening 3-153

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3.18 color matrix (CMX) 3-156
3.19 RGB gamma 3-166
3.20 RGB2YUV 3-174
3.21 YUV ROI statistics 3-174
3.22 window 3-175
3.23 AEC/AGC 3-175
3.23.1 position weight 3-176
3.23.2 combination weight 3-180
3.23.3 luminance weight 3-181
3.23.4 exposure/gain control 3-195
3.23.5 manual exposure/gain control 3-197
3.23.6 ABC context switch 3-200
3.24 high temperature control 3-204
3.24.1 type 0 ratio 3-204
3.24.2 type 1 ratio 3-205
3.24.3 HDR gain control 3-207
3.24.4 saturation control 3-208
3.24.5 LENC control 3-209
3.24.6 gamma control 3-210
3.24.7 BLC control 3-211
4 register tables 4-1
4.1 chip address and memory allocation 4-1
4.2 CPU interrupt 4-3
4.3 embedded line control 4-6
4.4 color bar 0/1/2 control 4-19
4.4.1 color bar 0 (pre) 4-19
4.4.2 color bar 1 (pre) 4-20
4.4.3 color bar 2 (post) 4-21
4.5 CIF control 4-22
4.6 DVP control 4-24
4.7 UART control 4-28
4.7.1 UART0 control 4-28
4.7.2 UART1 control 4-34
4.7.3 UART2 control 4-40
4.7.4 UART3 control 4-46
4.8 MIPI RX control 4-52

OVT Confidential Neusoft Only

4.8.1 MIPI RX0 control 4-52
4.8.2 MIPI RX1 control 4-64
4.9 MIPI TX control 4-76
4.10 4-wire serial interface control 4-85
4.10.1 4-wire serial interface master 4-85
4.10.2 4-wire serial interface slave 4-96
4.11 DMA control 4-102
4.12 VFIFO control 4-107
4.13 SCCB slave control 4-113
4.14 SCCB master control 4-116
4.15 IDC control 4-126
4.16 temperature sensor control 4-142
4.17 ODS control 4-144
4.18 system control (SC) control 4-147
4.19 OTP control 4-178
4.20 ISP sub-module base address summary 4-180
4.21 auto exposure/gain correction (AEC/AGC) 4-181
4.22 AEC PK control 4-193
4.23 auto white balance gain (AWBG) control 4-200
4.24 color interpolation (CIP) control 4-207
4.25 color correction matrix (CMX) control 4-210
4.26 combine control 4-217
4.27 curve AWB control 4-226
4.28 defect pixel correction (DPC) control 4-243
4.29 high dynamic range RAW data de-noise (HDR RAW DNS) control 4-257
4.30 ISP control 4-261
4.31 lens correction (LENC) control 4-268
4.32 RAW data de-noise (RAW DNS) control 4-314
4.33 pre ISP control 4-315
4.34 RGBH data de-noise (RGBH DNS) control 4-317
4.35 RGB gamma control 4-319
4.36 special digital effect (SDE) control 4-325
4.37 RAW stretch control 4-330
4.38 tone mapping control 4-334
4.39 YUV data de-noise (UVDNS) control 4-367

OVT Confidential Neusoft Only

4.40 YUV (ROI based) statistics (YUV stat) control 4-368
4.41 firmware register table 4-383
5 operating specifications 5-1
5.1 absolute maximum ratings 5-1
5.2 functional temperature 5-1
5.3 DC characteristics 5-2
6 mechanical specifications 6-1
6.1 physical specifications 6-1
6.2 IR reflow specifications 6-3

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OVT Confidential Neusoft Only

list of figures

figure 1-1	pin diagram	1-12
figure 2-1	OV490 system block diagram	2-1
figure 2-2	voltage regulator	2-3
figure 2-3	PLL structure	2-4
figure 2-4	clock network diagram	2-5
figure 2-5	power on sequence	2-7
figure 2-6	power off sequence	2-8
figure 2-7	4-wire serial interface timing	2-9
figure 2-8	SCCB interface timing	2-11
figure 2-9	boot from host by 4-wire serial interface master flash	2-14
figure 2-10	working flow - boot from host by 4-wire serial interface master flash	2-17
figure 2-11	boot by 4-wire serial interface slave	2-18
figure 2-12	working flow - boot by 4-wire serial interface slave	2-20
figure 2-13	boot from EEPROM by SCCB master	2-21
figure 2-14	working flow - boot from EEPROM by SCCB master	2-23
figure 2-15	boot from host by SCCB slave	2-24
figure 2-16	working flow - boot from host by SCCB slave	2-26
figure 2-17	brown-out detection	2-27
figure 2-18	embedded line diagram	2-28
figure 2-19	embedded line detail structure	2-28
figure 2-20	host control flow chart	2-31
figure 3-1	image processor block diagram	3-1
figure 3-2	color bar types	3-3
figure 3-3	color black and white square bars	3-4
figure 3-4	transparent effect	3-4
figure 3-5	rolling bar effect	3-5
figure 3-6	LENC control points	3-5
figure 3-7	lens correction graph	3-47
figure 3-8	AWB statistics ROI window diagram	3-62
figure 3-9	AWB gain mode diagram	3-68
figure 3-10	advanced AWB LUT example	3-71
figure 3-11	threshold gain curve in auto threshold mode	3-74

OVT Confidential Neusoft Only

figure 3-12	types of white pixels	3-76
figure 3-13	example of different channels connected	3-76
figure 3-14	example of same channel connected	3-77
figure 3-15	example of white cluster	3-77
figure 3-16	example of tailing pixel	3-78
figure 3-17	example of tailing pixel 2	3-78
figure 3-18	threshold for T-cluster diagram	3-79
figure 3-19	HDR RAW DNS diagram	3-107
figure 3-20	UV DNS diagram	3-114
figure 3-21	combination weight graph	3-117
figure 3-22	global gamma curve	3-126
figure 3-23	tone mapping statistics diagram	3-129
figure 3-24	local tone mapping grid diagram	3-130
figure 3-25	local tone mapping gamma gain diagram	3-131
figure 3-26	contrast level threshold	3-137
figure 3-27	contrast level restriction	3-137
figure 3-28	linear out	3-145
figure 3-29	stretch graph	3-146
figure 3-30	CIP block diagram	3-150
figure 3-31	CIP DNS diagram	3-151
figure 3-32	sharpen curve	3-154
figure 3-33	CMX curve diagram	3-157
figure 3-34	gamma curve diagram	3-166
figure 3-35	gain of high frequency information	3-167
figure 3-36	YUV ROI diagram	3-174
figure 3-37	position window diagram	3-176
figure 3-38	statistics window diagram	3-178
figure 3-39	position weight diagram	3-179
figure 3-40	combination weight diagram	3-180
figure 3-41	luminance threshold curve	3-182
figure 3-42	automatic adjustment step mode diagram	3-195
figure 3-43	ABC mode diagram	3-200
figure 3-44	type 0 ratio	3-204
figure 3-45	type 1 ratioT	3-205
figure 3-46	type 1 ratioG	3-206

OVT Confidential Neusoft Only

figure 3-47	HDR gain control	3-207
figure 3-48	saturation factor control	3-208
figure 3-49	LENC factor control	3-209
figure 3-50	gamma control	3-210
figure 6-1	package specifications	6-1
figure 6-2	IR reflow ramp rate requirements	6-3

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list of tables

table 1-1 2x2 lane MIPI signal descriptions 1-1
table 1-2 1x4 lane MIPI signal descriptions 1-4
table 1-3 power domain description 1-9
table 2-1 input formats 2-2
table 2-2 output formats 2-2
table 2-3 PLL descriptions 2-4
table 2-4 clock network descriptions 2-5
table 2-5 4-wire serial interface master interface timing 2-9
table 2-6 SCCB interface timing 2-11
table 2-7 system boot mode 2-14
table 2-8 flash memory arrangement 2-15
table 2-9 header format (4-wire serial interface master) 2-15
table 2-10 quick set instruction format (4-wire serial interface master) 2-16
table 2-11 header format (4-wire serial interface slave) 2-18
table 2-12 quick set instruction (4-wire serial interface slave) 2-19
table 2-13 header format (SCCB master) 2-21
table 2-14 quick set instruction (SCCB master) 2-22
table 2-15 host command descriptions 2-30
table 3-1 ISP references 3-1
table 3-2 LENC registers 3-6
table 3-3 LENC scale registers 3-48
table 3-4 multi LENC firmware registers 3-54
table 3-5 AWB gain control registers 3-56
table 3-6 manual AWB gain firmware registers 3-60
table 3-7 AWB statistics firmware registers 3-62
table 3-8 AWB statistics registers 3-63
table 3-9 AWB gain mode firmware registers 3-69
table 3-10 AWB algorithm control registers 3-70
table 3-11 curve AWB LUT map firmware registers 3-72
table 3-12 AWB speed and stable firmware registers 3-72
table 3-13 post AWB shift firmware registers 3-73
table 3-14 threshold gain curve 3-75

OVT Confidential Neusoft Only

table 3-15 DPC registers 3-80
table 3-16 HDR RAW DNS control registers 3-107
table 3-17 OVPB RAW DNS registers 3-111
table 3-18 UV DNS control registers 3-114
table 3-19 combine control registers 3-119
table 3-20 pre CMX firmware registers 3-122
table 3-21 HDR gain saturated pixel threshold registers 3-124
table 3-22 HDR gain firmware registers 3-125
table 3-23 global tone mapping firmware registers 3-127
table 3-24 global tone mapping control registers 3-128
table 3-25 tone mapping registers 3-132
table 3-26 tone mapping firmware registers 3-135
table 3-27 contrast level restriction firmware registers 3-138
table 3-28 linear stretch registers 3-147
table 3-29 CIP registers 3-151
table 3-30 sharpness registers 3-155
table 3-31 CMX registers 3-158
table 3-32 RGB gamma registers 3-168
table 3-33 AEC window and weight control registers 3-183
table 3-34 exposure time and gain 3-196
table 3-35 AEC control firmware registers 3-198
table 3-36 context switch control firmware registers 3-201
table 3-37 high temperature control firmware registers 3-211
table 4-1 AHB bus address allocation 4-1
table 4-2 group 1 interrupts 4-3
table 4-3 group 2 interrupts 4-4
table 4-4 embedded line control registers 4-6
table 4-5 color bar 0 pre registers 4-19
table 4-6 color bar 1 pre registers 4-20
table 4-7 color bar2 post registers 4-21
table 4-8 CIF registers 4-22
table 4-9 DVP registers 4-24
table 4-10 UART0 control registers 4-28
table 4-11 UART1 control registers 4-34
table 4-12 UART2 control registers 4-40

OVT Confidential Neusoft Only

table 4-13	UART3 control registers	4-46
table 4-14	MIPI RX0 registers	4-52
table 4-15	MIPI RX1 registers	4-64
table 4-16	MIPI TX registers	4-76
table 4-17	4-wire serial interface master registers	4-85
table 4-18	4-wire serial interface slave registers	4-96
table 4-19	DMA control registers	4-103
table 4-20	DMA control registers	4-105
table 4-21	VFIFO registers	4-107
table 4-22	SCCB slave registers	4-113
table 4-23	SCCB master0 registers	4-116
table 4-24	SCCB master1 registers	4-121
table 4-25	IDC registers	4-126
table 4-26	temperature sensor registers	4-142
table 4-27	ODS registers	4-144
table 4-28	SC registers	4-147
table 4-29	OTP control registers	4-178
table 4-30	ISP sub-module base address summary	4-180
table 4-31	AEC/AGC registers	4-181
table 4-32	AEC PK control registers	4-193
table 4-33	AWBG control registers	4-200
table 4-34	CIP registers	4-207
table 4-35	CMX registers	4-210
table 4-36	combine registers	4-217
table 4-37	curve AWB registers	4-226
table 4-38	DPC registers	4-243
table 4-39	HDR RAW DNS registers	4-257
table 4-40	ISP control registers	4-261
table 4-41	LENC registers	4-268
table 4-42	RAW DNS registers	4-314
table 4-43	pre ISP registers	4-315
table 4-44	RGBH DNS registers	4-317
table 4-45	RGB gamma registers	4-319
table 4-46	SDE registers	4-325
table 4-47	RAW stretch registers	4-330

OVT Confidential Neusoft Only

table 4-48 tone mapping registers 4-334
table 4-49 UVDNS registers 4-367
table 4-50 YUV stat registers 4-368
table 4-51 ISP general control register 4-383
table 4-52 AWB firmware registers 4-383
table 4-53 HDR firmware registers 4-389
table 4-54 AEC firmware registers 4-401
table 4-55 LSC firmware registers 4-408
table 4-56 high temperature function firmware registers 4-411
table 5-1 absolute maximum ratings 5-1
table 5-2 functional temperature 5-1
table 5-3 DC characteristics 5-2
table 6-1 package dimensions 6-1
table 6-2 reflow conditions 6-3

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV490 bridge chip. The OV490 has one package with two configurations for MIPI (2x2 lane and 1x4 lane MIPI). The package information is shown in **section 6**.

1.1 2x2 lane MIPI configuration

table 1-1 2x2 lane MIPI signal descriptions (sheet 1 of 4)

pin number	signal name	pin type	description
A1	CVSSPK	ground	digital core ground
A2	HREFO	output	DVP horizontal reference
A3	SDO_7	output	DVP pixel data output bit 7 (shared with MTXDN1)
A4	SDO_6	output	DVP pixel data output bit 6 (shared with MTXDP1)
A5	SDO_1	output	DVP pixel data output bit 1 (shared with MTXDN2)
A6	SDO_0	output	DVP pixel data output bit 0 (LSB) (shared with MTXDP2)
A7	FSIN1	I/O	digital sensor frame sync control signal / boot selection pin during boot up
A8	TXD1	output	UART1, data transmission
A9	RXD1	input	UART1, data receiving
A10	CVSSPK	ground	digital core ground
B1	PCLKO	output	DVP pixel clock
B2	SDO_9	output	DVP pixel data output bit 9 (shared with MTXDN3)
B3	SDO_8	output	DVP pixel data output bit 8 (shared with MTXDP3)
B4	SDO_5	output	DVP pixel data output bit 5 (shared with MTXCN)
B5	SDO_3	output	DVP pixel data output bit 3 (shared with MTXDN0)
B6	SCK1	I/O	SCCB clock (requires 4.7kΩ pull up resistor)
B7	CCLK1	output	reference clock to digital sensor
B8	TXD0	output	UART0, data transmission
B9	RXD0	input	UART0, data receiving
B10	CCLK0	output	reference clock to digital sensor
C1	VSYNCO	output	DVP vertical sync
C2	SDO_11	output	DVP pixel data output bit 11 (MSB)

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table 1-1 2x2 lane MIPI signal descriptions (sheet 2 of 4)

pin number	signal name	pin type	description
C3	MTXAVDD33	power	3.3V analog power supply for MIPI TX in MIPI output mode and DVP supply in DVP output mode
C4	SDO_4	output	DVP pixel data output bit 4 (shared with MTXCP)
C5	SDO_2	output	DVP pixel data output bit 2 (shared with MTXDP0)
C6	SD1	I/O	SCCB data (requires 4.7kΩ pull up resistor)
C7	SPWDN1	output	digital sensor power down control
C8	GPIO1	I/O	general purpose input/output pin 1
C9	FSIN0	I/O	digital sensor frame sync control signal / boot selection pin during boot up
C10	GPIO0	I/O	general purpose input/output pin 0
D1	SD	I/O	SCCB slave data (requires 4.7kΩ pull up resistor)
D2	PLLAVDD	power	PLL analog power supply
D3	SDO_10	output	DVP pixel data output bit 10
D4	MTXAVSS	ground	MIPI TX analog ground in MIPI output mode and DVP analog ground in DVP output mode
D5	MTXDVDD	power	MIPI TX digital power supply
D6	CVDDPD	power	1.2V digital core power supply for power-down
D7	PADVSS18	ground	ground for 1.8V I/O
D8	PADVDD18	power	1.8V I/O power supply
D9	SD0	I/O	SCCB data (requires 4.7kΩ pull up resistor)
D10	SCK0	I/O	SCCB clock (requires 4.7kΩ pull up resistor)
E1	XI	input	crystal input/reference clock input
E2	SCK	I/O	SCCB slave clock (requires 4.7kΩ pull up resistor)
E3	TSAVDD	power	analog power supply for temperature sensor
E4	PLLDVDD	power	PLL digital power supply
E5	PADVSS33	ground	ground for 3.3V I/O
E6	CVDDPK	power	digital core power supply for power-keep
E7	SPWDN0	output	digital sensor power down control
E8	VROPD2	power	1.2V regulator power output
E9	VROPD1	power	1.2V regulator power output
E10	VROPD0	power	1.2V regulator power output

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table 1-1 2x2 lane MIPI signal descriptions (sheet 3 of 4)

pin number	signal name	pin type	description
F1	XO	output	crystal out
F2	PWDN	input	power down control (active high)
F3	TMODE	input	test mode (active high)
F4	PADVDD33	power	3.3V I/O power supply
F5	FSIN	I/O	frame sync control to OV490
F6	CVDDPD	power	digital core power supply for power-down
F7	VMON	input	brown-out detection voltage threshold input 1
F8	VROPK	power	1.2V regulator power output
F9	VRIB	power	1.8V/3.3V regulator power input
F10	VRIA	power	1.8V/3.3V regulator power input
G1	SICK	I/O	4-wire serial interface master/slave bit clock
G2	MISO	I/O	4-wire serial interface master/slave data
G3	MOSI	I/O	4-wire serial interface master/slave data
G4	RESETB	input	system reset (active low)
G5	GPIO5	I/O	general purpose input/output pin 5
G6	M0RXDVDD	power	MIPI RX digital power supply
G7	VRGND	ground	regulator ground
G8	SDI_5	input	digital sensor pixel data input bit 5 (shared with M1RXDN0)
G9	SDI_4	input	digital sensor pixel data input bit 4 (shared with M1RXDP0)
G10	VMONL	input	brown-out detection voltage threshold input 2
H1	SSN	I/O	serial interface chip select
H2	BWNFLG	output	brown-out detection flag (active low)
H3	GPIO3	I/O	general purpose input/output pin 3
H4	GPIO4	I/O	general purpose input/output pin 4
H5	TMS	input	JTAG test mode select
H6	HREFI	input	digital sensor horizontal reference
H7	VSYNCI	input	digital sensor vertical sync
H8	SDI_7	input	digital sensor pixel data input bit 7 (shared with M0RXCN)
H9	SDI_3	input	digital sensor pixel data input bit 3 (shared with M1RXDN1)
H10	SDI_2	input	digital sensor pixel data input bit 2 (shared with M1RXDP1)

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table 1-1 2x2 lane MIPI signal descriptions (sheet 4 of 4)

pin number	signal name	pin type	description
J1	SCCBID1	input	SCCB ID select signal
J2	SCCBID0	input	SCCB ID select signal
J3	GPIO2	I/O	general purpose input/output pin 2
J4	TRST	input	JTAG test reset (active low)
J5	TDO	output	JTAG test output data
J6	SDI_11	input	digital sensor pixel data input bit 11 (shared with M0RXDN0)
J7	SDI_10	input	digital sensor pixel data input bit 10 (shared with M0RXDP0)
J8	SDI_6	input	digital sensor pixel data input bit 6 (shared with M0RXCP)
J9	SDI_1	input	digital sensor pixel data input bit 1 (shared with M1RXCN)
J10	SDI_0	input	digital sensor pixel data input bit 0 (shared with M1RXCP)
K1	CVSSPK	ground	digital core ground
K2	RXD	input	UART, data receiving
K3	TXD	output	UART, data transmission
K4	TCK	input	JTAG test clock
K5	TDI	input	JTAG test input data
K6	PCLKI	input	digital sensor pixel clock
K7	SDI_9	input	digital sensor pixel data input bit 9 (shared with M0RXDN1)
K8	SDI_8	input	digital sensor pixel data input bit 8 (shared with M0RXDP1)
K9	M0RXAVDD18	power	MIPI RX analog power supply
K10	CVSSPK	ground	digital core ground

1.2 1x4 lane MIPI configuration

table 1-2 1x4 lane MIPI signal descriptions (sheet 1 of 5)

pin number	signal name	pin type	description
A1	CVSSPK	ground	digital core ground
A2	HREFO	output	DVP horizontal reference
A3	SDO_7	output	DVP pixel data output bit 7 (shared with MTXDN1)

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table 1-2 1x4 lane MIPI signal descriptions (sheet 2 of 5)

pin number	signal name	pin type	description
A4	SDO_6	output	DVP pixel data output bit 6 (shared with MTXDP1)
A5	SDO_1	output	DVP pixel data output bit 1 (shared with MTXDN2)
A6	SDO_0	output	DVP pixel data output bit 0 (shared with MTXDP2)
A7	FSIN1	I/O	digital sensor frame sync control signal / boot selection pin during boot up
A8	TXD1	output	UART1, data transmission
A9	RXD1	input	UART1, data receiving
A10	CVSSPK	ground	digital core ground
B1	PCLKO	output	DVP pixel clock
B2	SDO_9	output	DVP pixel data output bit 9 (shared with MTXDN3)
B3	SDO_8	output	DVP pixel data output bit 8 (shared with MTXDP3)
B4	SDO_5	output	DVP pixel data output bit 5 (shared with MTXCN)
B5	SDO_3	output	DVP pixel data output bit 3 (shared with MTXDN0)
B6	SCK1	I/O	SCCB clock (require 4.7kΩ pull up resistor)
B7	CCLK1	output	reference clock to digital sensor
B8	TXD0	output	UART0, data transmission
B9	RXD0	input	UART0, data receiving
B10	CCLK0	output	reference clock to digital sensor
C1	VSYNCO	output	DVP vertical sync
C2	SDO_11	output	DVP pixel data output bit 11
C3	MTXAVDD33	power	3.3V analog power supply for MIPI TX in MIPI output mode and DVP supply in DVP output mode
C4	SDO_4	output	DVP pixel data output bit 4 (shared with MTXCP)
C5	SDO_2	output	DVP pixel data output bit 2 (shared with MTXDP0)
C6	SD1	I/O	SCCB data (requires 4.7kΩ pull up resistor)
C7	SPWDN1	output	digital sensor power down control
C8	GPIO1	I/O	general purpose input/output pin 1
C9	FSIN0	I/O	digital sensor frame sync control signal / boot selection pin during boot up
C10	GPIO0	I/O	general purpose input/output pin 0
D1	SD	I/O	SCCB slave data (requires 4.7kΩ pull up resistor)

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table 1-2 1x4 lane MIPI signal descriptions (sheet 3 of 5)

pin number	signal name	pin type	description
D2	PLLAVDD	power	PLL analog power supply
D3	SDO_10	output	DVP pixel data output bit 10
D4	MTXAVSS	ground	MIPI TX analog ground in MIPI output mode and DVP analog ground in DVP output mode
D5	MTXDVDD	power	MIPI TX digital power supply
D6	CVDDPD	power	1.2V digital core power supply for power-down
D7	PADVSS18	ground	ground for 1.8V I/O
D8	PADVDD18	power	1.8V I/O power supply
D9	SD0	I/O	SCCB data (requires 4.7kΩ pull up resistor)
D10	SCK0	I/O	SCCB clock (requires 4.7kΩ pull up resistor)
E1	XI	input	crystal input/reference clock input
E2	SCK	I/O	SCCB slave clock (requires 4.7kΩ pull up resistor)'
E3	TSAVDD	power	analog power supply for temperature sensor
E4	PLLDVDD	power	PLL digital power supply
E5	PADVSS33	ground	ground for 3.3V I/O
E6	CVDDPK	power	digital core power supply for power-keep
E7	SPWDN0	output	digital sensor power down control
E8	VROPD2	power	1.2V regulator power output
E9	VROPD1	power	1.2V regulator power output
E10	VROPD0	power	1.2V regulator power output
F1	XO	output	crystal out
F2	PWDN	input	power down control (active high)
F3	TMODE	input	test mode (active high)
F4	PADVDD33	power	3.3V I/O power supply
F5	FSIN	I/O	frame sync control to OV490
F6	CVDDPD	power	digital core power supply for power-down
F7	VMON	input	brown-out detection voltage threshold input 1
F8	VROPK	power	1.2V regulator power output
F9	VRIB	power	1.8V/3.3V regulator power input
F10	VRIA	power	1.8V/3.3V regulator power input

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table 1-2 1x4 lane MIPI signal descriptions (sheet 4 of 5)

pin number	signal name	pin type	description
G1	SICK	I/O	4-wire serial interface master/slave bit clock
G2	MISO	I/O	4-wire serial interface master/slave data
G3	MOSI	I/O	4-wire serial interface master/slave data
G4	RESETB	input	system reset (active low)
G5	GPIO5	I/O	general purpose input/output pin 5
G6	M0RXDVDD	power	MIPI RX digital power supply
G7	VRGND	ground	regulator ground
G8	SDI_5	input	digital sensor pixel data input bit 5 (shared with M0RXDN2)
G9	SDI_4	input	digital sensor pixel data input bit 4 (shared with M0RXDP2)
G10	VMONL	input	brown-out detection voltage threshold input 2
H1	SSN	I/O	serial interface chip select
H2	BWNFLG	output	brown-out detection flag (active low)
H3	GPIO3	I/O	general purpose input/output pin 3
H4	GPIO4	I/O	general purpose input/output pin 4
H5	TMS	input	JTAG test mode select
H6	HREFI	input	digital sensor horizontal reference
H7	VSYNCI	input	digital sensor vertical sync
H8	SDI_7	input	digital sensor pixel data input bit 7 (shared with M0RXCN)
H9	SDI_3	input	digital sensor pixel data input bit 3 (shared with M0RXDN3)
H10	SDI_2	input	digital sensor pixel data input bit 2 (shared with M0RXDP3)
J1	SCCBID1	input	SCCB ID select signal
J2	SCCBID0	input	SCCB ID select signal
J3	GPIO2	I/O	general purpose input/output pin 2
J4	TRST	input	JTAG test reset (active low)
J5	TDO	output	JTAG test output data
J6	SDI_11	input	digital sensor pixel data input bit 11 (shared with M0RXDN0)
J7	SDI_10	input	digital sensor pixel data input bit 10 (shared with M0RXDP0)
J8	SDI_6	input	digital sensor pixel data input bit 6 (shared with M0RXCP)
J9	SDI_1	input	digital sensor pixel data input bit 1 (shared with M1RXCN)
J10	SDI_0	input	digital sensor pixel data input bit 0 (shared with M1RXCP)

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table 1-2 1x4 lane MIPI signal descriptions (sheet 5 of 5)

pin number	signal name	pin type	description
K1	CVSSPK	ground	digital core ground
K2	RXD	input	UART, data receiving
K3	TXD	output	UART, data transmission
K4	TCK	input	JTAG test clock
K5	TDI	input	JTAG test input data
K6	PCLKI	input	digital sensor pixel clock
K7	SDI_9	input	digital sensor pixel data input bit 9 (shared with M0RXDN1)
K8	SDI_8	input	digital sensor pixel data input bit 8 (shared with M0RXDP1)
K9	M0RXAVDD18	power	MIPI RX analog power supply
K10	CVSSPK	ground	digital core ground

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1.3 power domain

table 1-3 power domain description (sheet 1 of 3)

pin number	signal name	I/O bank
B10	CCLK0	powered by PADVDD18
C9	FSIN0	
C10	GPIO0	
E7	SPWDN0	
D9	SD0	
D10	SCK0	
B9	RXD0	
B8	TXD0	
B7	CCLK1	
A7	FSIN1	
C8	GPIO1	
C7	SPWDN1	
C6	SD1	
B6	SCK1	
A9	RXD1	
A8	TXD1	

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table 1-3 power domain description (sheet 2 of 3)

pin number	signal name	I/O bank
E1	XI	
F1	XO	
G1	SICK	
G2	MISO	
G3	MOSI	
H1	SSN	
K3	TXD	
K2	RXD	
J4	TRST	
H5	TMS	
K4	TCK	
J5	TDO	
K5	TDI	
F2	PWDN	powered by PADVDD33/PADVSS33
F3	TMODE	
G4	RESETB	
J3	GPIO2	
H3	GPIO3	
H4	GPIO4	
G5	GPIO5	
F5	FSIN	
H2	BWNFLG	
J2	SCCBID0	
J1	SCCBID1	
D1	SD	
E2	SCK	

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table 1-3 power domain description (sheet 3 of 3)

pin number	signal name	I/O bank
K6	PCLKI	
H7	VSYNCI	
H6	HREFI	
J10	M1RXCP/SDI_0	
J9	M1RXCN/SDI_1	
H10	M1RXDP1/SDI_2	
H9	M1RXDN1/SDI_3	
G9	M1RXDP0/SDI_4	powered by M0RXAVDD18
G8	M1RXDN0/SDI_5	
J8	M0RXCP/SDI_6	
H8	M0RXCN/SDI_7	
K8	M0RXDP1/SDI_8	
K7	M0RXDN1/SDI_9	
J7	M0RXDP0/SDI_10	
J6	M0RXDN0/SDI_11	
B1	PCLKO	
C1	VSYNCO	
A2	HREFO	
A6	MTXDP2/SDO_0	
A5	MTXDN2/SDO_1	
C5	MTXDP0/SDO_2	
B5	MTXDN0/SDO_3	
C4	MTXCP/SDO_4	powered by MTXAVDD33
B4	MTXCN/SDO_5	
A4	MTXDP1/SDO_6	
A3	MTXDN1/SDO_7	
B3	MTXDP3/SDO_8	
B2	MTXDN3/SDO_9	
D3	SDO_10	
C2	SDO_11	

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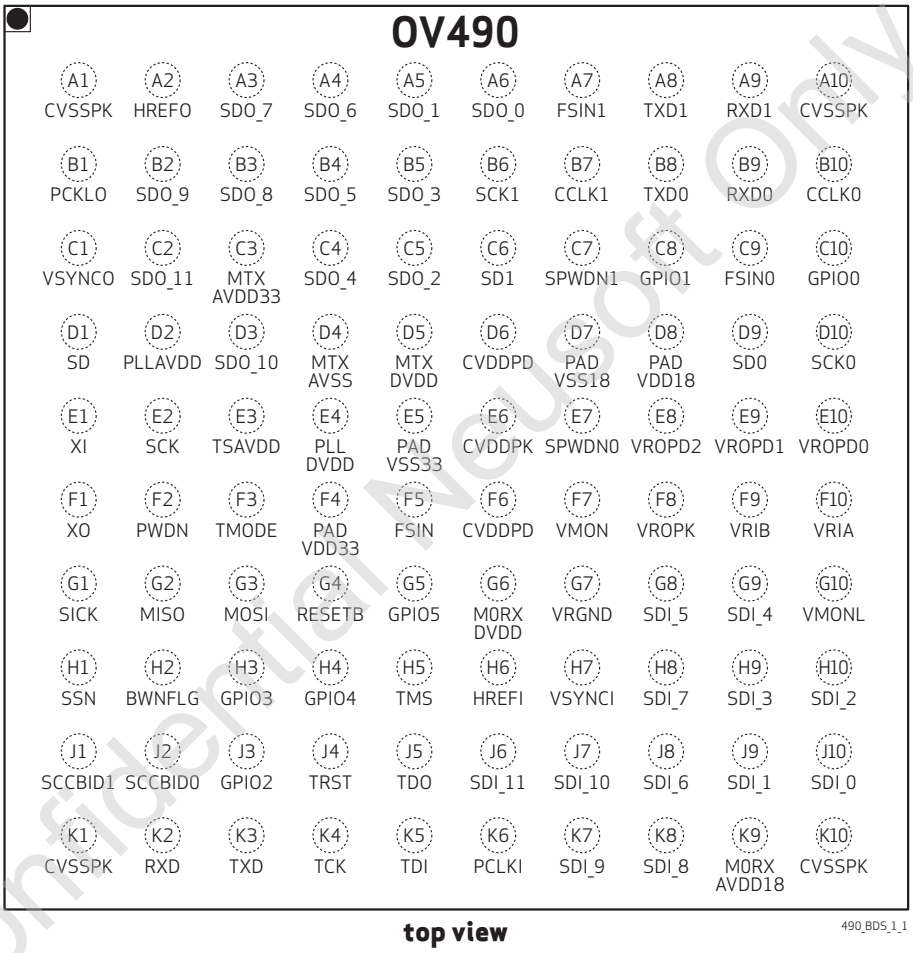
figure 1-1 pin diagram



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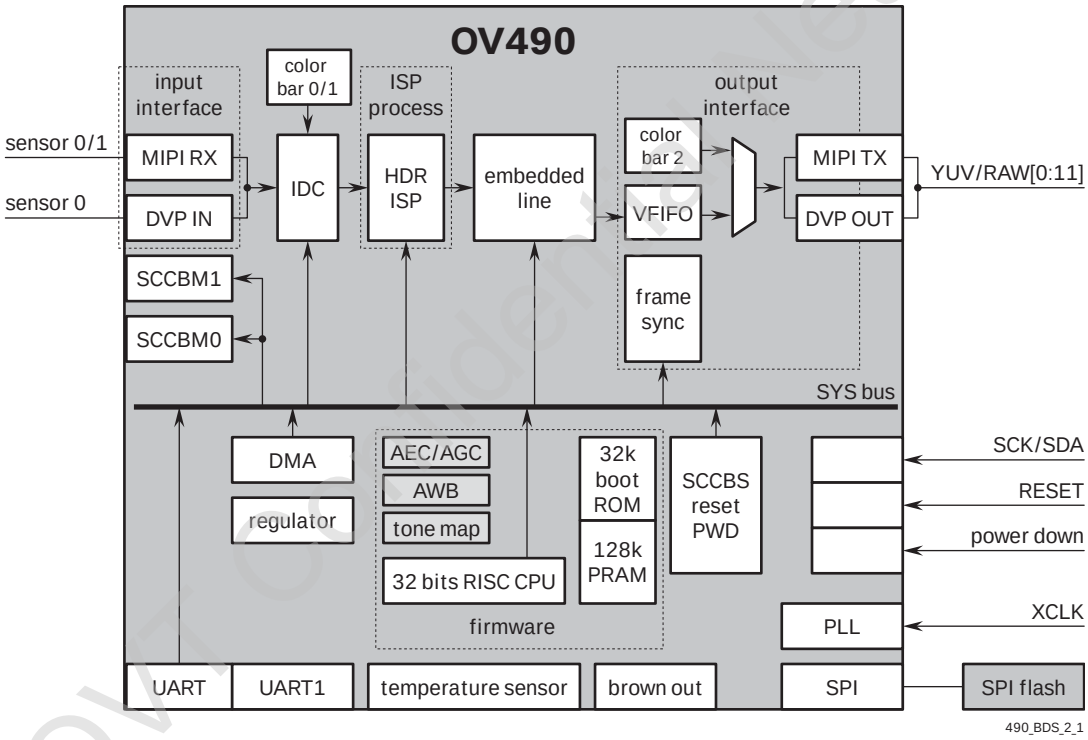
2 system level description

2.1 overview

The OV490 is a companion ISP processor for the OV10640 (and similar sensors) to provide a full system solution for display-based applications. The OV490 integrates a high performance ISP with improved HDR functionality for high quality images. Furthermore, the OV490 enables RAW output for machine vision downstream processing in parallel with fully processed YUV for display based applications via MIPI CSI-2 interface. It is designed to process single and dual stream input data. The OV490 is equipped with a 32-bit RISC processor for special applications. The RISC CPU acts as a master controlling the whole chip with the firmware code embedded in ROM or in the program RAM. It can access all sub-modules and run complicated algorithms for flexibility.

figure 2-1 OV490 system block diagram



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2.2 input and output formats

table 2-1 input formats

format	resolution	output	interface	DVP pixel clock or MIPI data rate
3x12 bits unprocessed RAW	1280x1080	30 fps	4-lane MIPI RX	450Mbps
3x12 bits unprocessed RAW	1280x1080	20 fps	12-bit DVP	100MHz
2x11 bits compressed RAW	1280x1080	60 fps	4-lane MIPI RX	600Mbps/lane
2x11 bits compressed RAW	1280x1080	30 fps	12-bit DVP	100MHz
3x12 bits unprocessed RAW	1920x1080	30 fps	4-lane MIPI RX	670Mbps/lane
2x11 bits compressed RAW	1920x1080	30 fps	4-lane MIPI RX	420Mbps/lane
2x11 bits compressed RAW	1280x1080	30 fps	2-lane MIPI RX	600Mbps/lane

table 2-2 output formats

format	resolution	output	interface	DVP pixel clock or MIPI data rate
8/10/12-bit YUV422	1280x1080	30 fps	12-bit DVP	100MHz
8-bit BT.656/BT.601	1280x1080	30 fps	12-bit DVP	100MHz
RGB565	1280x1080	30 fps	12-bit DVP	100MHz
RGB888	1280x1080	30 fps	12-bit DVP	100MHz
RGB565	1280x1080	60 fps	4-lane MIPI TX	600Mbps/lane
12-bit YUV422	1280x1080	60 fps	4-lane MIPI TX	600Mbps/lane
12-bit YUV422 and 12-bit RAW	1280x1080	30 fps	4-lane MIPI TX	450Mbps/lane
12-bit YUV422	1920x1080	30 fps	4-lane MIPI TX	450Mbps/lane
8-bit BT.656/BT.601	1920x1080	20 fps	12-bit DVP	100MHz
RGB565	1920x1080	20 fps	12-bit DVP	100MHz
RGB888	1920x1080	20 fps	12-bit DVP	100MHz

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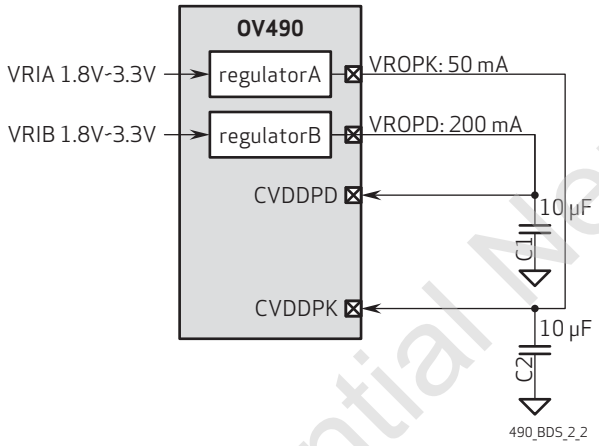
2.3 voltage regulator

There are two on-chip voltage regulators in the OV490. One is for the power-keep domain with an average output current of 50 mA and the other is for the power-down domain with an average output current of 200mA. They will take a 1.8V~3.3V input and produce 1.2V ± 10% output. If the on-chip voltage regulator is used, then the regulator output can be looped back to power the corresponding digital domain (see **figure 2-2**).

figure 2-2 voltage regulator



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2.4 system clock (PLL)

Two independent on-chip PLLs (PLL1, PLL2) are available to supply various MIPI clocks and system clock for the desired application. The PLLs take a reference clock from the platform system (such as a crystal), ranging from 6MHz ~ 27MHz, to generate the required clocks. A programmable clock divider is built inside the PLL as well as digital logic to generate various clock frequencies so that the OV490 can run at different speeds to achieve system performance as well as saving power.

figure 2-3 PLL structure

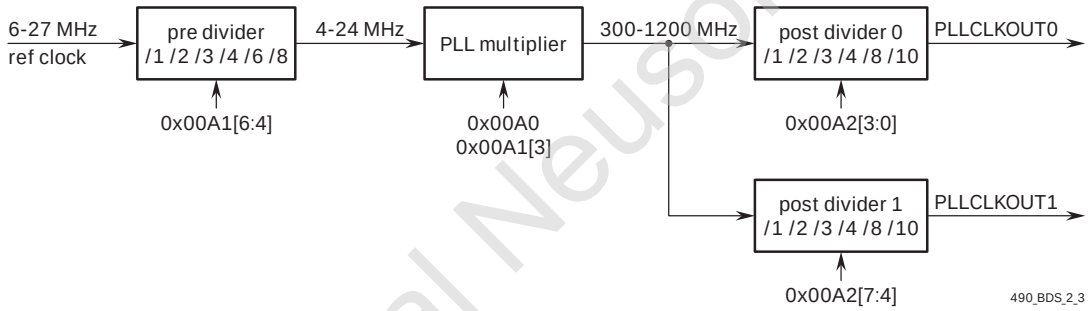

table 2-3 PLL descriptions

address	parameter name	default value	R/W	description
PLL1				
0x808000A0	VLDIV	0x1D	RW	For Loop Div
0x808000A1	PREDIV	0x02	RW	Bit[6:4]: Pre divider of PLL
0x808000A1	SDIV	0x01	RW	Bit[3]: For loop div
0x808000A2	POSTDIV0	0x07	RW	Bit[3:0]: Post divider of PLLCLKOUT0
0x808000A2	POSTDIV1	0x07	RW	Bit[7:4]: Post divider of PLLCLKOUT1
PLL2				
0x808000A4	VLDIV	0x1D	RW	For Loop Div
0x808000A5	PREDIV	0x02	RW	Bit[6:4]: Pre divider of PLL
0x808000A5	SDIV	0x01	RW	Bit[3]: For loop div
0x808000A6	POSTDIV0	0x00	RW	Bit[3:0]: Post divider of PLLCLKOUT0
0x808000A6	POSTDIV1	0x07	RW	Bit[7:4]: Post divider of PLLCLKOUT1

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2.4.1 clock network

figure 2-4 clock network diagram

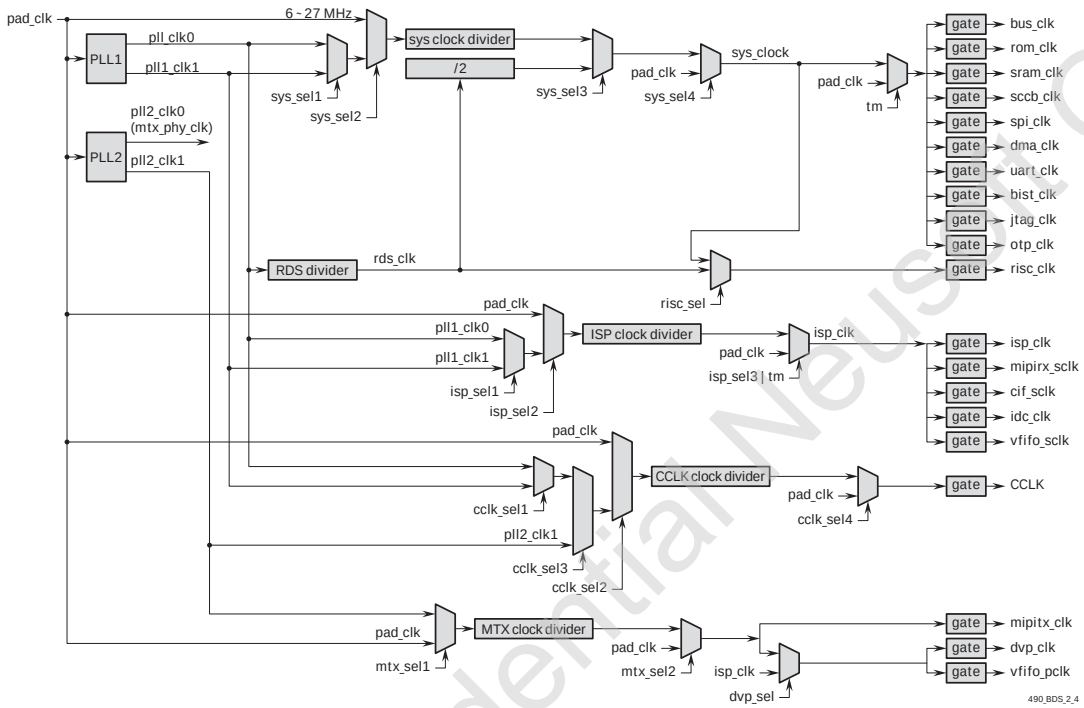

table 2-4 clock network descriptions (sheet 1 of 2)

address	parameter name	default value	R/W	description
0x80800021	SYS_SEL1	0x00	RW	Bit[0]: System select1 0: From PLL1 clk0 (400MHz) 1: From PLL1 clk1 (200MHz)
0x80800021	SYS_SEL2	0x00	RW	Bit[1]: Select source of system divider 0: From pad_clk (crystal) 1: From output of MUX (sys_sel1)
0x80800020	SYS CLOCK DIVIDER	0x04	RW	Bit[7:0]: System clock divider
0x80800021	SYS_SEL3	0x00	RW	Bit[3]: System select3 0: Select system clock divider 1: Select RDS divider

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table 2-4 clock network descriptions (sheet 2 of 2)

address	parameter name	default value	R/W	description
0x80800021	SYS_SEL4	0x00	RW	Bit[2]: System select4 0: Select pad clock 1: Select output of MUX (sys_sel3)
0x8080002B	RISC_SEL	0x00	RW	Bit[2]: RISC select 0: From system clock divider 1: From RDS clock divider
0x80800023	ISP_SEL1	0x00	RW	Bit[0]: ISP select1 0: Select pll1_clk0 (400MHz) 1: Select pll1_clk1 (200MHz)
0x80800023	ISP_SEL2	0x00	RW	Bit[1]: ISP select2 0: Select pad clock (crystal) 1: Select output of MUX (isp_sel1)
0x80800023	ISP_SEL3	0x00	RW	Bit[2]: ISP select3 0: Select pad clock 1: Select ISP clock divider
0x80800025	CCLK_SEL1	0x00	RW	Bit[0]: CCLK select1 0: Select pll1_clk0 (400MHz) 1: Select pll1_clk1 (200MHz)
0x80800025	CCLK_SEL3	0x00	RW	Bit[3]: CCLK select3 0: From PLL1 1: From PLL2
0x80800025	CCLK_SEL2	0x00	RW	Bit[1]: CCLK select2 0: From pad clock 1: From PLL1 or PLL2
0x80800025	CCLK_SEL4	0x00	RW	Bit[2]: CCLK select4 0: From pad clock 1: From CCLK clock divider
0x80800029	MTX_SEL1	0x00	RW	Bit[1]: MTX select1 0: From pad clock 1: From PLL2
0x80800029	MTX_SEL2	0x00	RW	Bit[2]: MTX select2 0: From pad clock 1: From MTX clock divider
0x80800023	DVP_SEL	0x00	RW	Bit[6]: DVP select 0: From MTX clock 1: From ISP clock

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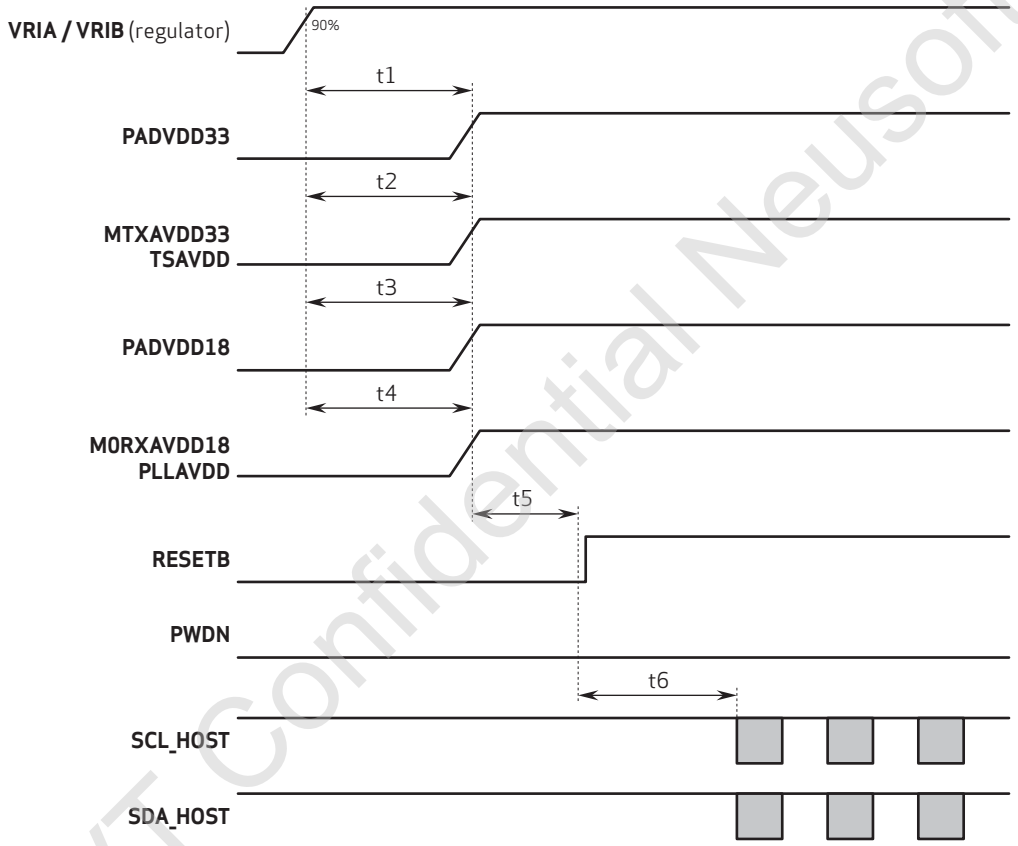
2.5 power-on sequence

The OV490 requires 3.3V and 1.8V power inputs (PADVDD and AVDD) from an external power source. The embedded voltage regulators take 1.8V~3.3V input and produce 1.2V to supply the digital core. The regulator needs set-up time to output stable 1.2V. For safety's sake, the application system should take the set-up time into account when powering up the OV490. **figure 2-5** shows the recommended power on sequence.

figure 2-5 power on sequence



note 1 t1 should be larger than 250 µs.

note 2 t2 should be larger than 250 µs.

note 3 t3 should be larger than 250 µs.

note 4 t4 should be larger than 250 µs.

note 5 t5 should be larger than 250 µs.

note 6 t6 should be larger than 1 ms.

490_BDS_2_5

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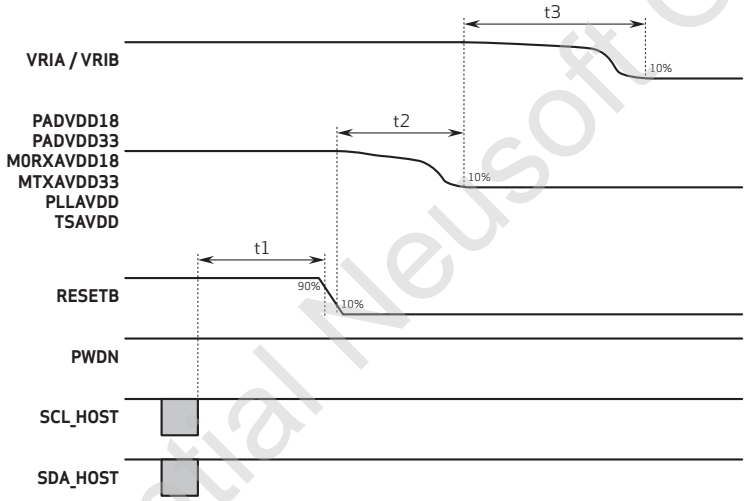
2.6 power-off sequence

To avoid an unknown state on the I/O, resetting the OV490 is recommended before powering off. Please refer to **figure 2-6**.

figure 2-6 power off sequence



note 1 t1 >= 1 frame, delay from SCCB stream off command to RESETB pull low

note 2 t2 >= 100 µs, delay from RESETB pull low to PADVDD18 / PADVDD33 / M0RXAVDD18 / MTXAVDD33 / PLLAVDD / TSAVDD power off

note 3 t3 >= 0 µs, delay from PADVDD18 / PADVDD33 / M0RXAVDD18 / MTXAVDD33 / PLLAVDD / TSAVDD power off to VRIA/VRIB power off

490_BDS_2_6

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2.7 4-wire serial interface

The OV490 supports a 4-wire serial interface for external storage of device configuration settings and communication with other OV490s. The OV490 can operate in 4-wire serial master/slave mode. In master mode, it can select up to two slaves, due to chip-select pin limit, to start the data communication one at a time. It supports bit-rate data communication up to 24Mbps. A hardware mailbox communication protocol is supported by slave mode.

figure 2-7 4-wire serial interface timing

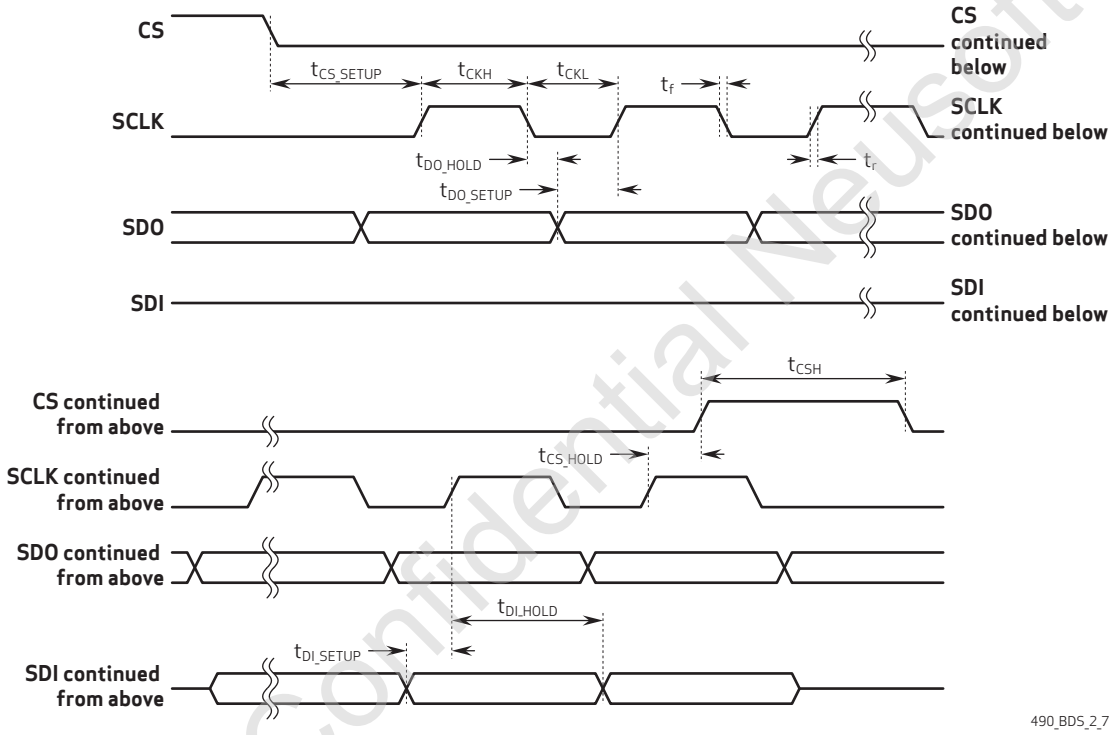

table 2-5 4-wire serial interface master interface timing (sheet 1 of 2)

symbol	parameter	condition	min	typ	max	unit
F_{SCLK}	clock frequency	V_{PADVDD} = 3.3V		25		MHz
t_{CKH}	clock high time	V_{PADVDD} = 3.3V		19.68		ns
t_{CKL}	clock low time	V_{PADVDD} = 3.3V		19.86		ns
t_r	clock rise time	V_{PADVDD} = 3.3V, 30~70%		2.70		ns
t_f	clock fall time	V_{PADVDD} = 3.3V, 30~70%		1.74		ns

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table 2-5 4-wire serial interface master interface timing (sheet 2 of 2)

symbol	parameter	condition	min	typ	max	unit
t_{CS_SETUP}	chip select active set up time	V_{PADVDD} = 3.3 V		20.00		ns
t_{CS_HOLD}	chip select active hold time	V_{PADVDD} = 3.3 V		20.08		ns
t_{DO_SETUP}	output setup time	V_{PADVDD} = 3.3V		19.32		ns
t_{DO_HOLD}	output hold time	V_{PADVDD} = 3.3V		0.65		ns
t_{CS_HIGH}	CS deselect time	V_{PADVDD} = 3.3V		417.82		ns

2.8 SCCB interface

There are two sets of SCCB master/slave and one set of SCCB slave. The master SCCB interface is dedicated for configuring digital sensors and obtaining parameters from each sensor on-the-fly so as to dynamically adjust its performance parameters. The slave SCCB allows users to read and write to the OV490 internal registers to control the chip or to use for debug purposes. A hardware mailbox communication protocol is supported by the SCCB slave. Both SCCB master and slave can run at speeds up to 400kbps.

In order to distinguish between the OV490 from other SCCB slave devices in the system, the slave ID can be set to different values by enabling the SCCBID0/SCCBID1 pin.

2.8.1 SCCB master mode program

```
//SCCB master register, please refer to 4.14
//For SCCB Master0: SCCB_MS_BASE_ADDR=0x80900000
//For SCCB Master1: SCCB_MS_BASE_ADDR=0x80910000
//set BIT7 of SCCB_ctrl_3 to 1'b1, Enable SCCB_MS module;
WRITE (SCCB_MS_BASE_ADDR+0x03, BIT7);
//set BIT6 of SCCB_ctrl_3 to 1'b1 for master mode
WRITE (SCCB_MS_BASE_ADDR+0x03, BIT6);
//set high bits of base_value which is related with bit-rate:
//base_value = system clock / (4 * bit-rate) -1
WRITE (SCCB_MS_BASE_ADDR+0x0d, base_value[11:8]);
//set low bits of base_value
WRITE (SCCB_MS_BASE_ADDR+0x0c, base_value[7:0]);
//enable interrupt which you need:
WRITE (SCCB_MS_BASE_ADDR+0x18, BITx);
```

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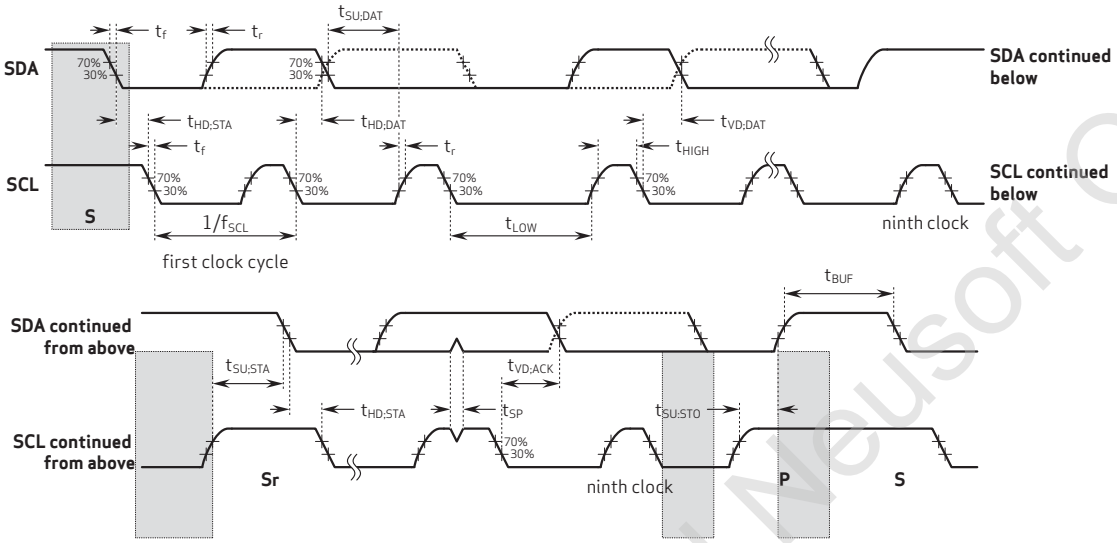
figure 2-8 SCCB interface timing



note 1 $V_{IL} = 0.3V_{DD}$

note 2 $V_{IH} = 0.7V_{DD}$

490_BDS_2_8

table 2-6 SCCB interface timing (sheet 1 of 2)

symbol	parameter	condition	min	typ	max	FS spec min	FS spec max
slave interface timing CCLK = 27MHz							
f_{SCL}	SCL clock frequency			400 kHz		0	400 kHz
t_{HIGH}	SCL clock high time	V_{PADVDD}=3.3V	40.32ns			0.6µs	-
t_{LOW}	SCL clock low time	V_{PADVDD}=3.3V	240.62ns			1.3µs	-
t_{BUF}	bus free time before new start cycle	V_{PADVDD}=3.3V	0ns			1.3µs	-
$t_{HD: STA}$	start of transmission hold time	V_{PADVDD}=3.3V	11.50ns			0.6µs	-
$t_{su: STA}$	start of transmission setup time	V_{PADVDD}=3.3V	0ns			0.6µs	-
$t_{SU: STO}$	stop of transmission setup time	V_{PADVDD}=3.3V	57.00ns			0.6µs	-
$t_{SU: DAT}$	input data setup time	V_{PADVDD}=3.3V	24.92ns			100ns	-
$t_{HD: DAT}$	input data hold time	V_{PADVDD}=3.3V	0			0	-
$t_{VD: DAT}$	time for data signal from SCL low to SDA output	V_{PADVDD}=3.3V			314.95ns	-	0.9µs

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table 2-6 SCCB interface timing (sheet 2 of 2)

symbol	parameter	condition	min	typ	max	FS spec min	FS spec max
$t_{VD: ACK}$	time for ACK signal from SCL low to SDA output	V_{PADVDD}=3.3V			113.20ns	-	0.9µs
t_{r_SDA}	SDA clock rising time	V_{PADVDD}=3.3V, 30~70%			193.70ns	20	300ns
t_{f_SDA}	SDA clock falling time	V_{PADVDD}=3.3V, 30~70%			18.85ns	20× (VDD/5.5V) =12ns	300ns
master interface timing CCLK = 27MHz							
	SCL clock frequency			400kHz		0	400kHz
t_{HIGH}	SCL clock high time	V_{PADVDD}=1.8V		943.50ns		0.6µs	-
t_{LOW}	SCL clock low time	V_{PADVDD}=1.8V		1365.00ns		1.3µs	-
t_{BUF}	bus free time before new start cycle	V_{PADVDD}=1.8V		136.58ms		1.3µs	-
$t_{HD: STA}$	start of transmission hold time	V_{PADVDD}=1.8V		1141.36ns		0.6µs	-
$t_{SU: STO}$	stop of transmission setup time	V_{PADVDD}=1.8V		1244.60ns		0.6µs	-
$t_{SU: DAT}$	input data setup time	V_{PADVDD}=1.8V		751.93ns		100ns	-
$t_{HD: DAT}$	input data hold time	V_{PADVDD}=1.8V		588.55ns		0	-
t_{r_SDA}	SDA clock rising time	V_{PADVDD}=3.3V, 30~70%		208.50ns		20	300ns
t_{f_SDA}	SDA clock falling time	V_{PADVDD}=3.3V, 30~70%		26.60ns		20× (VDD/5.5V) =12ns	300ns

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2.9 direct memory access (DMA)

DMA is used for transferring data from one source address into another destination address. It supports the action of reading data of continuous or fixed addresses, then writing them into continuous or fixed addresses. DMA also supports reading the data in many blocks, which are comprised of continuous addresses, and writing them to fixed addresses or a continuous address. The major features of DMA are:

- reads 32-bit data from source address, then writes 32-bit data to destination
- reads 32-bit data from source address, the writes 8-bit to continuous destination address 4 times
- reads 4x8-bit data from source address, then writes to 32-bit destination
- reads 4x8-bit data from source address, then writes to 4x8-bit destination
- reads 8-bit data from source address, then writes to 8-bit destination
- reads 8-bit data from source address, then writes to 32-bit destination
- supports handshaking with 4-wire serial interface for data communication
- supports several block data transfers
- supports address/data write

2.10 input data conversion (IDC)

The main function of IDC is collecting image data from the MIPI RX or DVP and converting them to a desired format and sequence. IDC is the main control module in the data path. All the video/image data input from the outside sensor should be fed into the IDC module first.This module can then be used to convert the data format, re-timing the pixel line, separating embedded data and normal video stream data, and other functions. The input image data can be 3xRAW12, 2xRAW12, 1xRAW12, 12-bit YUV422, 2x11 bits RAW. Key features of the IDC are:

- supports dual image with 1280x1080 or single image with 2592x1944
- supports several HDR data format, pure RAW format and 12-bit YUV422
- supports full frame control
- buffer size: 2x648x72 bits
- supports converting 2x11-bit RAW to 3xRAW12

For further information on IDC registers, see **section 4.15**.

2.11 VFIFO

The VFIFO module is dedicated to MIPI TX and DVP output. Since MIPI or DVP out needs to transmit data continuously, the data input from ISP or IDC may be discontinuous, the VFIFO acts as an accumulator to store the received data, then transmits the data out to MIPI TX or DVP as soon as required. Key features of VFIFO are:

- input formats: YUV422 8/10/12-bit, RAW 8/10/12/16/20-bit, RGB565, RGB888
- supports one image with one format, one image with two formats, two images with same format, two images with different format input
- supports a maximum of four virtual channels for MIPI TX
- includes one pair of internal SRAM: 1920x2 with 96-bit width.

For further information on VFIFO registers, see **section 4.12**.

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2.12 system control (SC)

The SC includes all system level control registers, such as clock gating and select, reset control, GPIO, PLL control, pin sharing control, and so on. Please refer to **section 4.18** for more detailed information.

2.13 system boot up

The OV490 has an embedded 32KB ROM and 128KB program RAM. The boot code is stored in ROM. The OV490 reads ROM first, then runs the boot code to check the status of the boot pins (FSIN0, FSIN1) which indicate the four boot modes of the OV490 (see **table 2-7**). Secondly, the OV490 loads program codes from the external memory device or host into the program RAM, which is determined by the boot mode. Finally, the OV490 reboots from the program RAM.

At any time during the boot-up process, the external host can force the RISC CPU into idle mode by the SCCB slave interface.

table 2-7 system boot mode

FSIN1	FSIN0	boot mode
0	0	SCCB slave boot
0	1	SCCB master boot
1	0	4-wire serial interface master boot
1	1	4-wire serial interface slave boot

2.13.1 boot from host by 4-wire serial interface master flash

figure 2-9 boot from host by 4-wire serial interface master flash

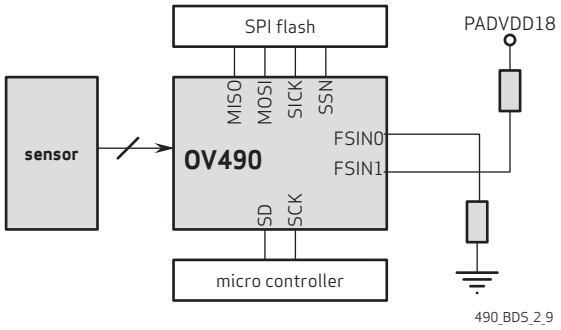

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table 2-8 flash memory arrangement

byte index	content
0~39	header
start address of header info	firmware

The OV490 will boot up at low speed (4MHz) to load the header (and quick_set instruction if any) and speeds up to 12MHz or 24MHz for loading the main firmware.

The first 40 bytes in 4-wire serial interface flash is the configuration for boot ROM. The format is as shown in **table 2-9**.

table 2-9 header format (4-wire serial interface master) (sheet 1 of 2)[a]

DWORD	item	description
0	0x4F565449	Magic Number
1	CONFIG	Bit[31]: set_div2zero_en 0: No change allowed 1: Can change 4-wire serial interface divider to zero Bit[7:0]: div div= (sysclk/(4-wire serial interface_clk*2))-1
2	SOURCE START ADDRESS	Flash/EEPROM Start Address
3	DESTINATION START ADDRESS	Memory Start Address
4	LENGTH	Firmware Data Length
5	SYS_CONFIG	Bit[7]: New format mode Bit[4]: CRC16 check FW flag 0: Do not check 1: Check Bit[3]: Load firmware select 0: CPU mode 1: Load firmware in DMA mode Bit[2]: DMA 32-bit R/W enable 0: Disable 1: Enable Bit[1]: Dcache enable 0: Disable 1: Enable Bit[0]: Lcache enable 0: Disable 1: Enable
6	DELAY	Interval of Read Firmware
7	RD_SIZE	Read Size per Read Command (0~0x1FF)

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table 2-9 header format (4-wire serial interface master) (sheet 2 of 2)[a]

DWORD	item	description
8	QUICK_SET	Bit[31]: Quick set flag 0: Do not set 1: Set flag Bit[23:0]: Quick set table address in 4-wire serial interface flash
9	CRC	Bit[31:16]: Quick set table length Bit15:0]: Header CRC (CRC of 38 byte in header)

a. RD_SIZE should be 4 bytes aligned if SYS_CONFIG[2] is set to 1

table 2-10 quick set instruction format (4-wire serial interface master)

DWORD	item	description
0	0x6F767469	Magic Number
1	CRC	Bit[15:0]: Quick set table CRC 16 value
2	REG0_ADDR	Register Address
3	REG0_DATA	Data Set to Register
...	...	...
2+ (n-1) × 2	REG (n-1)_ADDR	Register Address
2+(n-1) × 2 +1	REG (n-1)_DATA	Data Set to Register

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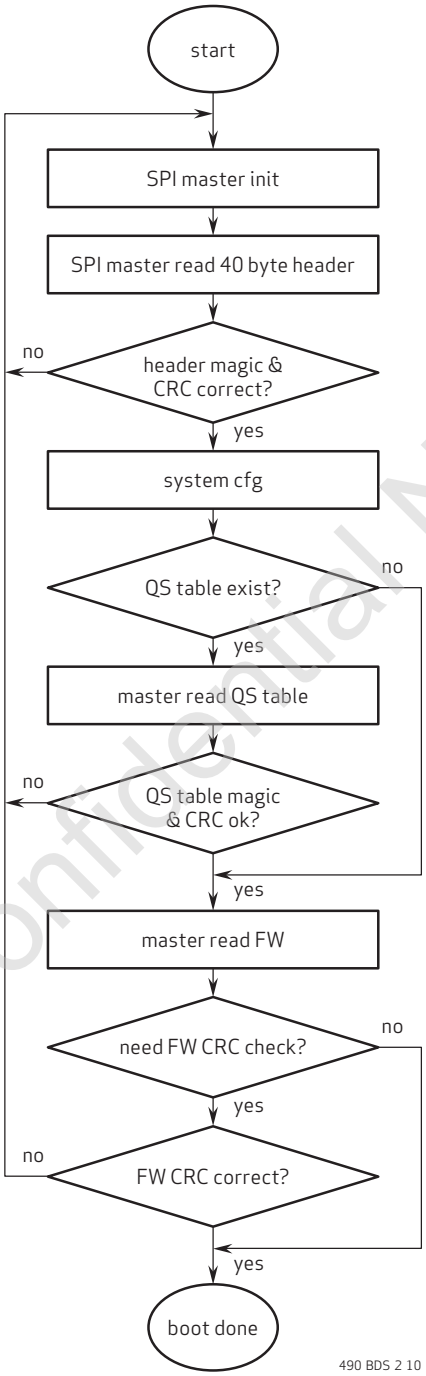
figure 2-10 working flow - boot from host by 4-wire serial interface master flash



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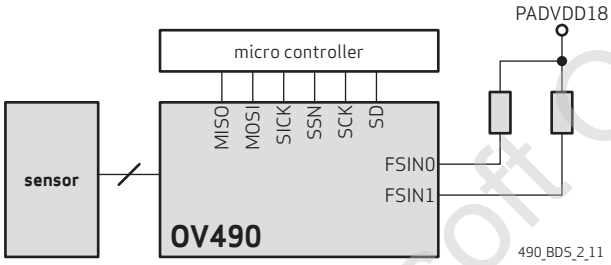
2.13.2 boot by 4-wire serial interface slave

figure 2-11 boot by 4-wire serial interface slave



2.13.2.1 protocol

1. Master resets slave and delays some time.
2. Master sends 32 bytes header to slave, delays some time and then receives the ACK.
3. Slave parses the header and responses to the master with 4 bytes ACK1 "0x55CC55CC".
4. If master receives ACK1 "0x55CC55CC", go to step 5; otherwise, go to 1.
5. If the quick set table exists, master sends quick set table to slave, delays some time and then receives the ACK, go to step 6; otherwise, go to step 8.
6. Slave parses the quick set table and responses to the master with 4 bytes ACK2 "0x11AA11AA".
7. If master receives ACK2 "0x11AA11AA", go to step 8; otherwise, go to step 1.
8. Master sends firmware to slave, delays some time and then receives the ACK.
9. Slave checks the firmware and responses to the master with 4 bytes ACK3 "0x22DD22DD".
10. If master receives ACK3 "0x22DD22DD", go to step 11; otherwise, go to step 1.
11. Boot done

table 2-11 header format (4-wire serial interface slave[a]) (sheet 1 of 2)

DWORD	item	description
0	0x4F565449	Magic Number
1	DESTINATION START	Memory Start Address
2	LENGTH	Firmware Data Length

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table 2-11 header format (4-wire serial interface slave[a]) (sheet 2 of 2)

DWORD	item	description
3	SYS_CONFIG	Bit[7]: New format mode Bit[4]: CRC16 check FW flag 0: Do not check 1: Check Bit[3]: Load firmware select 0: CPU mode 1: Load firmware in DMA mode Bit[2]: DMA 32-bit R/W enable 0: Disable 1: Enable Bit[1]: D-cache enable 0: Disable 1: Enable Bit[0]: L-cache enable 0: Disable 1: Enable
4	RD_SIZE	Size per Packet in Quick Set/Firmware Download Stage
5	QUICK_SET	Bit[0]: Quick set flag 0: Do not set 1: Set flag
6	DELAY_TIME	Delay for Synchronizing with Master
7	CRC	Bit[31:16]: Quick set table length Bit15:0]: Header CRC

a. RD_SIZE should be 4 bytes aligned if SYS_CONFIG[2] is set to 1

table 2-12 quick set instruction (4-wire serial interface slave)

DWORD	item	description
0	0x6F767469	Magic Number
1	CRC	Bit[15:0]: Quick set table CRC 16 value
2	REG0_ADDR	Register Address
3	REG0_DATA	Data Set to Register
...	...	...
2+ (n-1) × 2	REG(n-1)_ADDR	Register Address
2+(n-1) × 2 +1	REG(n-1)_DATA	Data Set to Register

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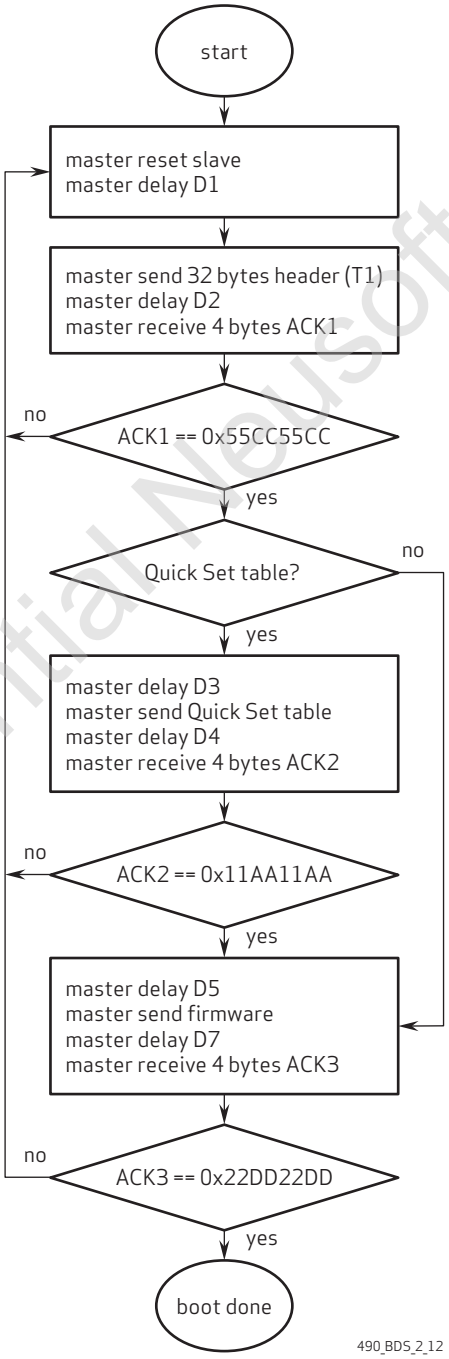
figure 2-12 working flow - boot by 4-wire serial interface slave



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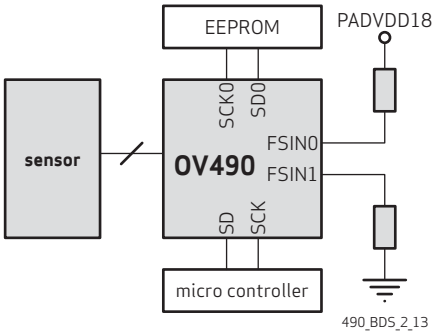
2.13.3 boot up from EEPROM by SCCB master

figure 2-13 boot from EEPROM by SCCB master



The first 32 bytes in EEPROM is the configuration for the boot loader.

table 2-13 header format (SCCB master)[a] (sheet 1 of 2)

DWORD	item	description
0	0x4F565449	Magic Number
1	BAUD_CFG	Value to be Written to the SCCB Baud Configure Register
2	SOURCE START ADDRESS	Flash/EEPROM Start Address
3	LENGTH	Memory Start Address
4	SYS_CONFIG	Firmware Data Length
5	QUICK_SET	Bit[7]: New format mode Bit[4]: CRC16 check FW flag 0: Do not check 1: Check Bit[3]: Load firmware select 0: CPU mode 1: Load firmware in DMA mode Bit[2]: DMA 32-bit R/W enable 0: Disable 1: Enable Bit[1]: D-cache enable 0: Disable 1: Enable Bit[0]: L-cache enable 0: Disable 1: Enable
6	CRC	Bit[0]: Quick set flag 0: Do not set 1: Set flag

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table 2-13 header format (SCCB master)[a] (sheet 2 of 2)

DWORD	item	description
7	CRC	Bit[31:16]: Quick set table length Bit15:0]: Header CRC

a. RD_SIZE should be 4 bytes aligned if SYS_CONFIG[2] is set to 1

table 2-14 quick set instruction (SCCB master)

DWORD	item	description
0	0x6F767469	Magic Number
1	CRC	Bit[15:0]: Quick set table CRC 16 value
2	REG0_ADDR	Register Address
3	REG0_DATA	Data Set to Register
...	...	...
2+ (n-1) * 2	REG(n-1)_ADDR	Register Address
2+(n-1) * 2 +1	REG(n-1)_DATA	Data Set to Register

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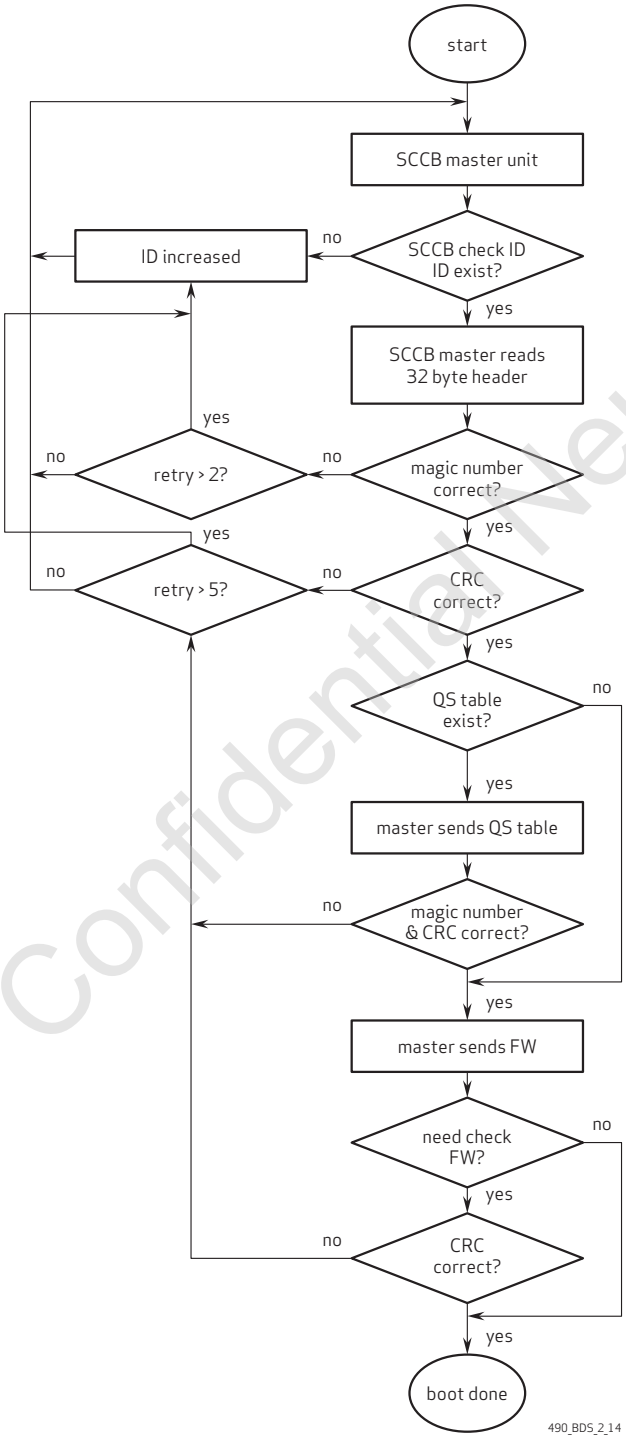
figure 2-14 working flow - boot from EEPROM by SCCB master



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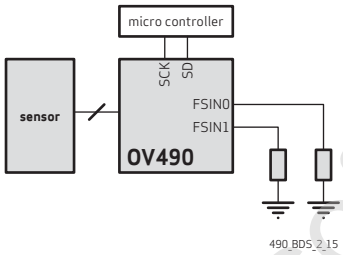
2.13.4 boot from host by SCCB slave

figure 2-15 boot from host by SCCB slave



2.13.4.1 Protocol

Below are boot flag states definitions:

```
#define SCCB_BOOT_RDY                    (0xa1)

#define SCCB_BOOT_JUMPBOOT_START         (0xc2)

#define SCCB_BOOT_JUMPBOOT_START_CACHE   (0xc5)

#define SCCB_BOOT_JUMPBOOT_OK            (0xc3)

#define SCCB_BOOT_JUMPBOOT_ERR           (0xc4)
```

Note:

– SCCB_BOOT_JUMPBOOT_START_CACHE means checking CRC with I-Cache and D-Cache enabled
– SCCB_BOOT_JUMPBOOT_OK means CRC check is OK
– SCCB_BOOT_JUMPBOOT_ERR means CRC check is ERROR

Furthermore, the following definitions are used in the protocol:

```
#define SRAM_FLAG_ADDR      (0x8019ffC8)

#define SRAM_FW_ADDR_BOOT   (0x8019ffC4)

#define SRAM_FW_START       (0x801900f8)

#define ADDR_FW_BOOT        (0x00190000)

#define SCCB_BURST_ADDR     (0x802a6000)
```

1. Master reads the boot flag from SRAM address SRAM_FLAG_ADDR and waits until the value is changed to SCCB_BOOT_RDY
2. Master writes value 0x01 to SCCB_BURST_ADDR in order to enable the OV490 SCCB slave burst writing function
3. Master changes OV490 system clock to 160MHz as following:
   - `writes value 0x01 to register 0x80800020`
   - `writes value 0x16 to register 0x80800021`

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- `writes value 0x1d to register 0x808000a0`
- `writes value 0xa1 to register 0x808000a1`
- `writes value 0x74 to register 0x808000a2`
- `writes value 0x29 to register 0x808000a3`

4. Master downloads the firmware to SRAM address SRAM_FW_START
5. Master writes value ADDR_FW_BOOT to SRAM address SRAM_FW_ADDR_BOOT
   - `writes value 0x00 to register 0x8019ffc4`
   - `writes value 0x19 to register 0x8019ffc5`
   - `writes value 0x00 to register 0x8019ffc6`
   - `writes value 0x00 to register 0x8019ffc7`
6. Master writes value SCCB_BOOT_JUMPBOOT_START or SCCB_BOOT_JUMPBOOT_START_CACHE to inform OV490 to start the CRC check
   - writes value 0xC2 or 0xC5 to register 0x8019FFC8
7. Master checks the boot flag
   - if the flag is SCCB_BOOT_JUMPBOOT_ERR, then jump to step 2 to download firmware again
   - if the flag is SCCB_BOOT_JUMPBOOT_OK, then boot ok and go to step 8
8. Boot done

Note: SRAM_FW_START can be defined by user, but the sum of SRAM_FW_START and firmware length (FW_SIZE) should be less than 0x8019A000 (i.e., SRAM_FW_START + FW_SIZE < 0x8019A000)

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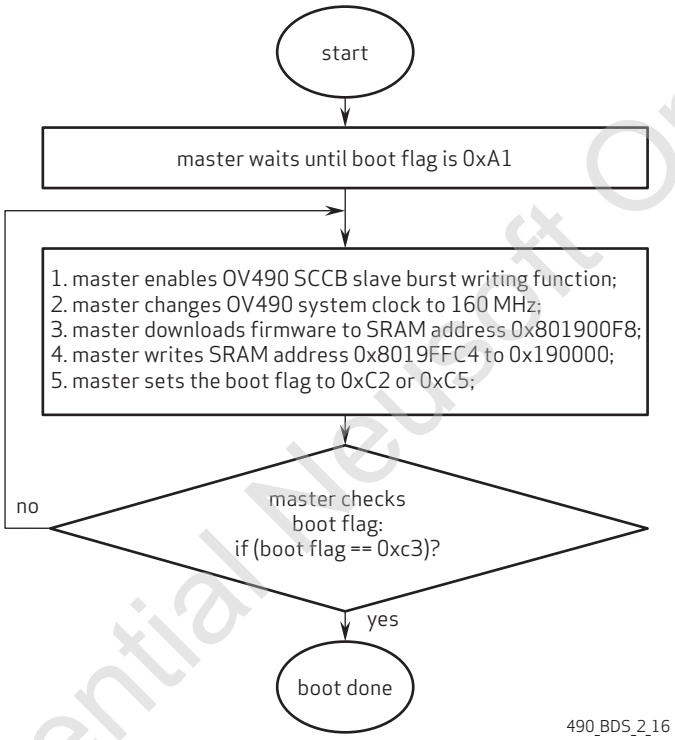
figure 2-16 working flow - boot from host by SCCB slave



2.14 RISC CPU

The OV490 features a 32-bit RISC CPU with 8KB I-cache and 8KB D-cache. The RISC CPU acts as a master controlling the whole chip with the firmware code in embedded ROM or in program RAM. It can access all sub-modules and run more complicated algorithms for flexibility.

2.15 general purpose I/O (GPIO)

The OV490 supports GPIO mode. The GPIO pins can be controlled via the external host.

GPIO pins can be read at any time by reading GPIO input registers, or controlled via the GPIO output enable registers as the values in the output registers will be driven to the pins. The de-bounce circuit is provided to improve noise immunity.

2.16 UART

Two UART interfaces to the back channel of the LVDS sensor chip are used to communicate with the MCU inside the camera module. One UART supports remote control through the RS232 port or is used for debug purposes.

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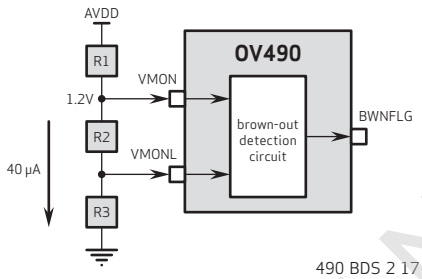
2.17 brown-out detection

The brown-out detection circuit can detect if the power source drops below a pre-selected trigger voltage. The trigger voltage is selected via a resistor network at pins VMON and VMONL. A brown-out condition detection is signaled with BWNFLG (active low). The BWNFLG signal is de-asserted when the power source remains stable above the release voltage.

figure 2-17 brown-out detection



Vtrigger is the voltage below AVDD at which the BWNFLG will be asserted. Vrelease is the voltage above Vtrigger at which the BWNFLG will be de-asserted. When Vtrigger is less than Vrelease, a hysteresis effect is present on the BWNFLG pin. The existence of the hysteresis width avoids malfunction caused by noise and an unstable situation applied to the input power signal.

2.18 temperature sensor

The built-in temperature sensor provides a simple way to do temperature monitoring and is capable of measuring temperatures within 5°C of accuracy over a temperature range of -40°C to 125°C. Temperature sensor power supply range is from 2.5V to 3.6V. The result of the temperature sensor can be read from registers 0x80260015 and 0x80260016.

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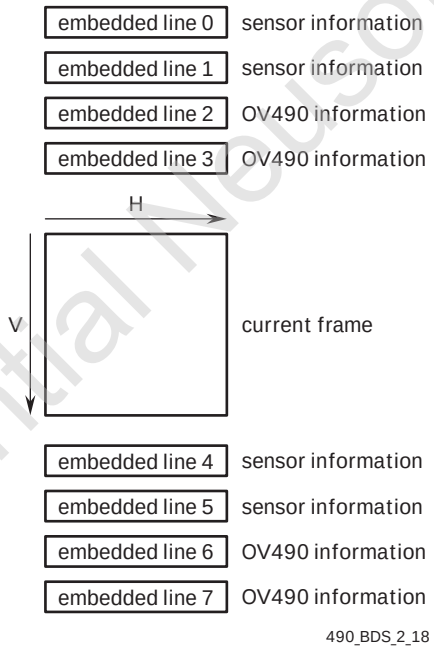
2.19 embedded line

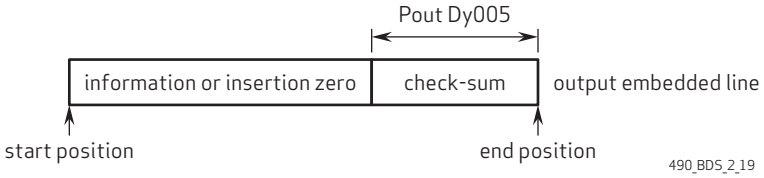
Additional information about set up and configuration of the sensor and OV490 can be embedded in the video stream. The embedded data contains programmable list values to describe the frame state including frame counter, exposure time, gain, etc. The OV490 supports embedded line mode regardless of MIPI or DVP interface. The OV490 can receive the input/output embedded line from the sensor and can also append it to the output stream. **figure 2-18** displays the position of each embedded line that can be configured.

figure 2-18 embedded line diagram



As for the detail structure of each embedded line, the OV490 will put the valid information into the embedded line from the start-position and the remaining positions except for the last four positions will be filled by zeros. The last four positions are for check sum. Please refer to **figure 2-19**.

figure 2-19 embedded line detail structure



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Example of insert one line information before/after frame:

```
//EMB_BASE_ADDR=0x8029e000, please refer to 4.3 about detail information.
WRITE(EMB_BASE_ADDR + 0x00, 0x11);              //enable embline in raw, single sensor
WRITE(EMB_BASE_ADDR + IMAGE_WIDTH1,0x500);      //image width is 1280
WRITE(EMB_BASE_ADDR + IMAGE_HEIGHT1,0x438);     //image height is 1080
//one OV490 information line before/after frame, and when sram is empty, don't read sram.

WRITE(EMB_BASE_ADDR + 0x0b,0x19);
WRITE(EMB_BASE_ADDR + 0x0d,0x10);      // one byte per cycle when inserting information
to lines
// low byte of horizontal line cycle number
WRITE(EMB_BASE_ADDR + 0x20, READ(EMB_BASE_ADDR + 0x10));
// high byte of horizontal line cycle number
WRITE(EMB_BASE_ADDR + 0x21, READ(EMB_BASE_ADDR + 0x11);
// low byte of horizontal blanking cycle number
WRITE(EMB_BASE_ADDR + 0x22, READ(EMB_BASE_ADDR + 0x12))
// high byte of horizontal blanking cycle number
WRITE(EMB_BASE_ADDR + 0x23, READ(EMB_BASE_ADDR + 0x13))
// low byte of vertical blanking cycle number
WRITE(EMB_BASE_ADDR + 0x24, READ(EMB_BASE_ADDR + 0x14))
// middle byte of vertical blanking cycle number
WRITE(EMB_BASE_ADDR + 0x25, READ(EMB_BASE_ADDR + 0x15))
// low byte of vertical blanking cycle number
WRITE(EMB_BASE_ADDR + 0x26, READ(EMB_BASE_ADDR + 0x16))
// 640 valid byte per line, include crc 4 byte, the line is before image
WRITE(VALID_BYTES2, 0x280);
//1280 byte per line totally and it must be the same as image line.
WRITE(TOTAL_BYTES2, 0x500);
//r_byte_order = 2, put byte at high location, such as {data[7:0],4'b0}.
WRITE(R_BYTE_ORDER, 0x02);
//640 valid byte per line, include crc 4 byte, the line is after image
WRITE(OVI_VALID_BYTES2, 0x280);
```

2.19.1 check-sum algorithm

The check-sum (CRC32) algorithm is applied to protect the embedded data. The polynomial is 0x1EDC6F41.

note Note that C is the previous CRC value, while D is the new data bit. The CRC is sent as the last data of the embedded data, most significant byte first.

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2.20 host command control

2.20.1 host control concept

Advantages and features of the host control command are:

- Host does not need to directly access the OV490's 32-bit registers. A task command with one or more parameters is sent to the OV490, then OV490 waits for the task to accomplish, checking one status register of the OV490 or one GPIO interrupt of the OV490.
- Host does not need to care about the task timing. For some tasks which need to be accomplished in the interval of adjacent frames, the OV490's firmware can arrange to do this in the interrupt of EOF. If the host directly accesses OV490's registers, it cannot ensure the correct timing and may cause poor image output.
- Increased speeds when many registers are in need of being accessed. The DMA of the OV490 can be arranged to speed up these tasks.
- For host control via I2C protocol, there can be 256 types of host control at the maximum but not limited to. It depends on the design of host control protocol

2.20.2 host command list

The host command is programmable by firmware. It can be added or removed by commands according to the application requirements. For reference of basic commands, see **table 2-15**.

table 2-15 host command descriptions

function	description
color hue level adjust	adjusts image color hue value
brightness level adjust	adjusts image brightness
sharpness level adjust	enhances or weaken image sharpness
contrast level adjust	adjusts image contrast value
manual exposure/gain set	disables auto AEC/AGC and allows manual configuration of sensor exposure and gain value
manual white balance gain set	disables auto AWB and allows manual setting of R/G/B gain white balance value
frame rate change	changes sensor frame rate
stream on/off	enables stream output or stop stream output
test pattern select	enables test pattern output

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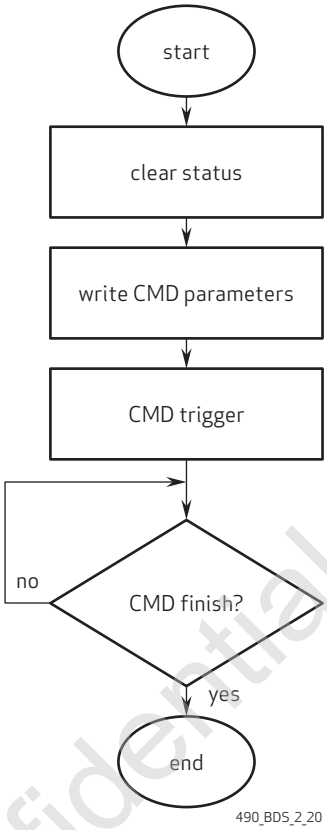
figure 2-20 host control flow chart



2.21 color bar 0/1/2

There are three color bar modules in the OV490 system: color bar 0/1/2 (see **figure 2-1**). Color bar 0/1 are located in front of the IDC module and color bar 2 is located in front of the DVP OUT/MIPI TX. The color bar modules can generate standard color bar image data and timing to support data-path debugging. The output format includes 8/10/12-bit RAW and 8/10/12-bit YUV422. For further information on color bar 0/1/2 registers, see **section 4.4**.

2.22 one time programmable memory (OTP)

The OV490 integrates 1024 bits of OTP memory. Production information and chip identification are stored in the memory to trace each part. The memory is also to used to store the calibration data for internal functions (e.g., the offset of temperature sensor). The OTP is organized into 8 memory banks. Each memory storage bank consists of 128 bits, which can be accessed through 16 registers. Some bytes in the first bank are reserved for OmniVision use only, while byte0~byte3 are used for chip identification. Byte4~byte7 are used for temperature sensor calibration and the bank selection is controlled by register 0x8028E084[2:0].

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OTP memory has three operation modes: program, read and inactive. OTP operates in inactive mode by default. When OTP enters program mode through the setting of registers, the data stored in internal registers will be sequentially burned into the OTP. When OTP enters read mode, the data stored in OTP is read and loaded into internal registers. Since the OTP memory can only be programmed once, caution is advised prior to overwriting any OTP setting.

The OTP memory is programmed using analog power: VDDQ. The VDDQ is bonded with PADVDD33 and the voltage setting is 2.5V±10%.

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3 image processor digital functions

The OV490 uses two kinds of registers for ISP processing: hardware registers and firmware registers. ISP hardware register addresses start from 0x80206000. ISP firmware registers base addresses start from 0x80180120. This section shows all firmware register addresses as offsets and not as an absolute addresses. The OV490 uses host commands to access firmware registers. For information on firmware registers R/W commands, refer to the OV490 application notes for details.

3.1 image processor

figure 3-1 shows the top level block diagram of the OV490 image processor.

figure 3-1 image processor block diagram

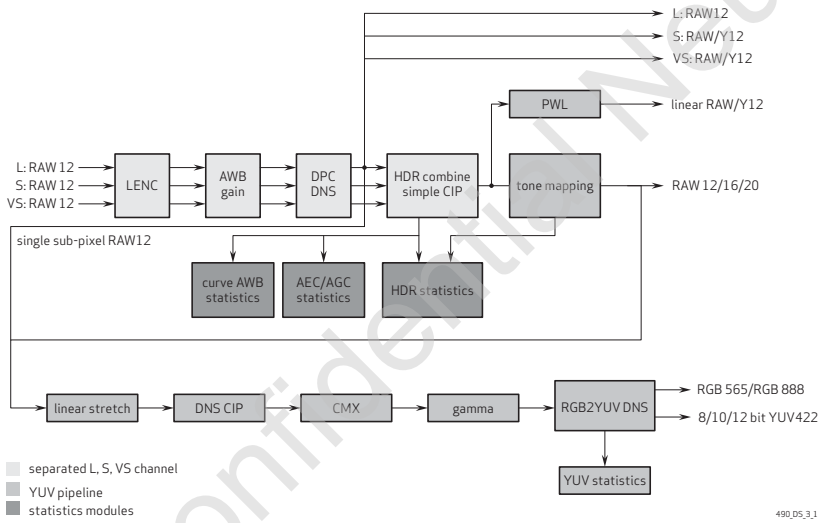

table 3-1 ISP references (sheet 1 of 2)

sub-module	description
AEC/AGC	auto exposure/gain correction (see **section 3.23**)
HDR	high dynamic range
LENC	lens correction (see **section 3.8**)
AWB	auto white balance (see **section 3.9**)
AWBG	auto white balance gain (to apply white balance gain of R/G/B channel separately)
DPC	defect pixel correction (see **section 3.10**)

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table 3-1 ISP references (sheet 2 of 2)

sub-module	description
DNS	de-noise descriptions include: RAW de-noise (RAW DNS) (see **section 3.11.2**) RGBH de-noise (RGBH DNS) UV de-noise (UV DNS) (see **section 3.11.3**)
PWL	piecewise linear (see **section 3.15**)
CIP	color interpolation (see **section 3.17**)

The image processor pipeline (ISP) receives image data from the sensor core. The video stream arrives as 12-bit parallel data separated in long exposure (L), short exposure (S) and very short exposure (VS) channels. Unused rows and columns are cut before further processing. One of the first processing steps in the ISP is to correct the shading caused by lens fall off (LENC). Digital gain is then applied to make the image white balanced (AWB gain). Defect pixel and clusters (DPC) are corrected on-the-fly for each exposure channel, and the de-noise filter (RAW DNS) reduces the noise in the raw image. RAW 12 for separated exposure channels can be output from here.

Before the exposure channels are combined (HDR combine), a simple color interpolation is applied. The image data in the dark area of the HDR image is from the L channel, while the data in the bright area is from the S and VS channels. In the transition area, the data is linearly combined. The weighting used in the combination feeds back to the AEC/AGC and HDR blocks to calculate the statistics.

Tone mapping is applied to compress the dynamic range of the full 20-bit representation to output combined tone-mapped RAW 12/16/20. The combined tone-mapped RAW data used further down stream in the YUV pipeline is stretched to enhance the contrast of the image.

The PWL module is used to compress the 20-bit combined linear raw/Y to 12-bit linear raw/Y. A compressed curve is used for the bit-conversion.

Color interpolation (CIP) recovers the missing color channels of each pixel from the neighboring pixels. To reduce noise and enhance edges, the video data noise and sharpness filter is applied. A color correction matrix (CMX) is applied on the R, G and B values of each pixel to improve the color fidelity due to spectrum crosstalk.

A global gamma correction is applied to the image to further improve the image rendering.

YUV statistics (YUV stat) is an ROI-based statistics module to assist the user in the case of using surround view harmonization. In total, four ROI windows are provided to get Y, U, V average and 16-bin Y histogram. Each ROI can be configured to father statistics from two accompanying sensors.

- if ISP is disabled (0x8020xxxx[0]), all processing-pipe sub-modules will be disabled
- if output format is RAW only and no YUV ROI statistics are required, all YUV processing modules will be automatically disabled
- if long exposure mode is enabled, combine, tone mapping and HDR statistic will be disabled

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3.2 test pattern

For testing purposes, the OV490 offers different test patterns, which include color bar, square pattern and random data. The OV490 also offers two digital effects for the test patterns: transparent effect and rolling bar effect. The test pattern function is enabled by register 0x80206081[7] for first sensor (0x80206090[7] for the second sensor) and the test pattern is selected by register 0x80206081[6:0] for first sensor (0x80206090[6:0] for the second sensor).

3.3 color bar

There are four types of color bars shown in color bar types selected from register 0x80206081[3:2] (and 0x80206090[3:2] for the second sensor).

figure 3-2 color bar types

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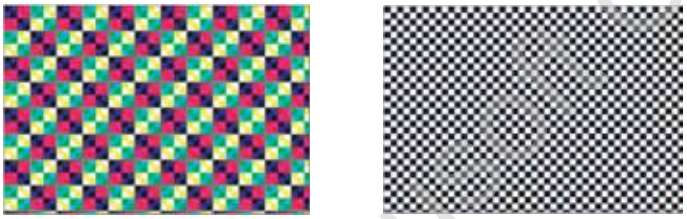
3.4 square

There are two types of square test patterns: color square and black-white square (setting registers 0x80206081[4] or 0x80206090[4] to low will select color square and setting these registers to high will select black-white square).

figure 3-3 color black and white square bars



color square black-white square

490_BDS_3_3

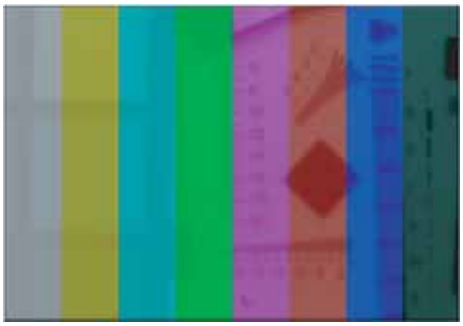
3.5 random data

There are two types of random data test patterns: frame-changing and frame-fixed random data selected by register 0x80206080[4].

3.6 transparent effect

Transparent color bar image is selected by register 0x80206081[5] (and 0x80206090[5] for the second sensor).

figure 3-4 transparent effect



490_BDS_3_4

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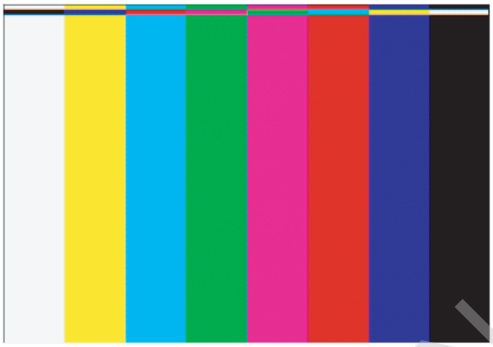
3.7 rolling bar effect

Rolling bar on color bar image is selected by register 0x80206081[6] (and 0x80206090[6] for the second sensor).

figure 3-5 rolling bar effect



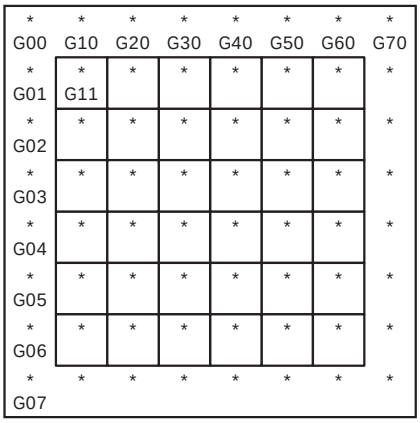
490_BDS_3_5

Since the digital test patterns pass through the pipeline to get a consistent output pattern, it may be required to turn off some of the ISP processing (LENC, DNS, DPC, and so).

3.8 lens correction (LENC)

The first step in the image processing pipeline is to correct the shading due to light fall off in the edges and corner areas. The correction is done by multiplying each pixel with a gain based on the area where each pixel is located. The gain to apply is calculated from a 8x8 grid with control points for both luminance (G) and each color channel (B,R) separately. The control points are separated for LPD (L,VS) and SPD (S). LENC is disabled by default and can be enabled by register 0x80206010[2] (and 0x80206030[2] for the second sensor).

figure 3-6 LENC control points



490_BDS_3_6

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The control points are selected according to the absolute coordinates of the input pixel in the sensor array. In other words, if y_offset and x_offset are bigger than 0, where values of registers (0x80206018~0x8020601B for the first sensor) (0x80206038~0x8020603B for the second sensor) are bigger than 0), the control point (0,0) cannot be used. Or, if the image is flipped, control points will be selected from the back. The control points are located in the center of each sub-array and contain data on the lens artifacts in their respective locations in the pixel array.

The OV490 supports sub-sampling and flip in both horizontal and vertical directions while LENC is enabled.

The LENC control registers are separate for L, S and VS exposures. The following explanation is for L/VS, please see LENC control registers for S.

Under dark conditions, the signal-to-noise ratio (SNR) drops off in the corner areas. The noise can be significantly amplified by the lens correction gain and will result in a brighter corner. The OV490 can automatically adjust gain for the pixels to adapt to lighting conditions (m_nQ). This is accomplished by following the sensor analog gain for LPD (enabled by default).

When scene brightness increases, the sensor analog gain decreases towards its minimum (min-gain) and correspondingly, the LENC gain increases towards its maximum (max-q) (see **figure 3-7**). When scene brightness decreases, the sensor analog gain increases towards its maximum (max-gain), and the LENC gain decreases towards its minimum (min-q).

table 3-2 LENC registers (sheet 1 of 41)

address	register name	default value	R/W	description
0x80206400	SNR0_LENC_LV_G00	0x00	RW	Bit[7:0]: G00 of 8x8 G control point array for L/VS of sensor 0
0x80206401	SNR0_LENC_LV_G01	0x00	RW	Bit[7:0]: G01 of 8x8 G control point array for L/VS of sensor 0
0x80206402	SNR0_LENC_LV_G02	0x00	RW	Bit[7:0]: G02 of 8x8 G control point array for L/VS of sensor 0
0x80206403	SNR0_LENC_LV_G03	0x00	RW	Bit[7:0]: G03 of 8x8 G control point array for L/VS of sensor 0
0x80206404	SNR0_LENC_LV_G04	0x00	RW	Bit[7:0]: G04 of 8x8 G control point array for L/VS of sensor 0
0x80206405	SNR0_LENC_LV_G05	0x00	RW	Bit[7:0]: G05 of 8x8 G control point array for L/VS of sensor 0
0x80206406	SNR0_LENC_LV_G06	0x00	RW	Bit[7:0]: G06 of 8x8 G control point array for L/VS of sensor 0
0x80206407	SNR0_LENC_LV_G07	0x00	RW	Bit[7:0]: G07 of 8x8 G control point array for L/VS of sensor 0
0x80206408	SNR0_LENC_LV_G10	0x00	RW	Bit[7:0]: G10 of 8x8 G control point array for L/VS of sensor 0

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table 3-2 LENC registers (sheet 2 of 41)

address	register name	default value	R/W	description
0x80206409	SNR0_LENC_LV_G11	0x00	RW	Bit[7:0]: G11 of 8x8 G control point array for L/VS of sensor 0
0x8020640A	SNR0_LENC_LV_G12	0x00	RW	Bit[7:0]: G12 of 8x8 G control point array for L/VS of sensor 0
0x8020640B	SNR0_LENC_LV_G13	0x00	RW	Bit[7:0]: G13 of 8x8 G control point array for L/VS of sensor 0
0x8020640C	SNR0_LENC_LV_G14	0x00	RW	Bit[7:0]: G14 of 8x8 G control point array for L/VS of sensor 0
0x8020640D	SNR0_LENC_LV_G15	0x00	RW	Bit[7:0]: G15 of 8x8 G control point array for L/VS of sensor 0
0x8020640E	SNR0_LENC_LV_G16	0x00	RW	Bit[7:0]: G16 of 8x8 G control point array for L/VS of sensor 0
0x8020640F	SNR0_LENC_LV_G17	0x00	RW	Bit[7:0]: G17 of 8x8 G control point array for L/VS of sensor 0
0x80206410	SNR0_LENC_LV_G20	0x00	RW	Bit[7:0]: G20 of 8x8 G control point array for L/VS of sensor 0
0x80206411	SNR0_LENC_LV_G21	0x00	RW	Bit[7:0]: G21 of 8x8 G control point array for L/VS of sensor 0
0x80206412	SNR0_LENC_LV_G22	0x00	RW	Bit[7:0]: G22 of 8x8 G control point array for L/VS of sensor 0
0x80206413	SNR0_LENC_LV_G23	0x00	RW	Bit[7:0]: G23 of 8x8 G control point array for L/VS of sensor 0
0x80206414	SNR0_LENC_LV_G24	0x00	RW	Bit[7:0]: G24 of 8x8 G control point array for L/VS of sensor 0
0x80206415	SNR0_LENC_LV_G25	0x00	RW	Bit[7:0]: G25 of 8x8 G control point array for L/VS of sensor 0
0x80206416	SNR0_LENC_LV_G26	0x00	RW	Bit[7:0]: G26 of 8x8 G control point array for L/VS of sensor 0
0x80206417	SNR0_LENC_LV_G27	0x00	RW	Bit[7:0]: G27 of 8x8 G control point array for L/VS of sensor 0
0x80206418	SNR0_LENC_LV_G30	0x00	RW	Bit[7:0]: G30 of 8x8 G control point array for L/VS of sensor 0
0x80206419	SNR0_LENC_LV_G31	0x00	RW	Bit[7:0]: G31 of 8x8 G control point array for L/VS of sensor 0
0x8020641A	SNR0_LENC_LV_G32	0x00	RW	Bit[7:0]: G32 of 8x8 G control point array for L/VS of sensor 0
0x8020641B	SNR0_LENC_LV_G33	0x00	RW	Bit[7:0]: G33 of 8x8 G control point array for L/VS of sensor 0

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table 3-2 LENC registers (sheet 3 of 41)

address	register name	default value	R/W	description
0x8020641C	SNR0_LENC_LV_G34	0x00	RW	Bit[7:0]: G34 of 8x8 G control point array for L/VS of sensor 0
0x8020641D	SNR0_LENC_LV_G35	0x00	RW	Bit[7:0]: G35 of 8x8 G control point array for L/VS of sensor 0
0x8020641E	SNR0_LENC_LV_G36	0x00	RW	Bit[7:0]: G36 of 8x8 G control point array for L/VS of sensor 0
0x8020641F	SNR0_LENC_LV_G37	0x00	RW	Bit[7:0]: G37 of 8x8 G control point array for L/VS of sensor 0
0x80206420	SNR0_LENC_LV_G40	0x00	RW	Bit[7:0]: G40 of 8x8 G control point array for L/VS of sensor 0
0x80206421	SNR0_LENC_LV_G41	0x00	RW	Bit[7:0]: G41 of 8x8 G control point array for L/VS of sensor 0
0x80206422	SNR0_LENC_LV_G42	0x00	RW	Bit[7:0]: G42 of 8x8 G control point array for L/VS of sensor 0
0x80206423	SNR0_LENC_LV_G43	0x00	RW	Bit[7:0]: G43 of 8x8 G control point array for L/VS of sensor 0
0x80206424	SNR0_LENC_LV_G44	0x00	RW	Bit[7:0]: G44 of 8x8 G control point array for L/VS of sensor 0
0x80206425	SNR0_LENC_LV_G45	0x00	RW	Bit[7:0]: G45 of 8x8 G control point array for L/VS of sensor 0
0x80206426	SNR0_LENC_LV_G46	0x00	RW	Bit[7:0]: G46 of 8x8 G control point array for L/VS of sensor 0
0x80206427	SNR0_LENC_LV_G47	0x00	RW	Bit[7:0]: G47 of 8x8 G control point array for L/VS of sensor 0
0x80206428	SNR0_LENC_LV_G50	0x00	RW	Bit[7:0]: G50 of 8x8 G control point array for L/VS of sensor 0
0x80206429	SNR0_LENC_LV_G51	0x00	RW	Bit[7:0]: G51 of 8x8 G control point array for L/VS of sensor 0
0x8020642A	SNR0_LENC_LV_G52	0x00	RW	Bit[7:0]: G52 of 8x8 G control point array for L/VS of sensor 0
0x8020642B	SNR0_LENC_LV_G53	0x00	RW	Bit[7:0]: G53 of 8x8 G control point array for L/VS of sensor 0
0x8020642C	SNR0_LENC_LV_G54	0x00	RW	Bit[7:0]: G54 of 8x8 G control point array for L/VS of sensor 0
0x8020642D	SNR0_LENC_LV_G55	0x00	RW	Bit[7:0]: G55 of 8x8 G control point array for L/VS of sensor 0
0x8020642E	SNR0_LENC_LV_G56	0x00	RW	Bit[7:0]: G56 of 8x8 G control point array for L/VS of sensor 0

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table 3-2 LENC registers (sheet 4 of 41)

address	register name	default value	R/W	description
0x8020642F	SNR0_LENC_LV_G57	0x00	RW	Bit[7:0]: G57 of 8x8 G control point array for L/VS of sensor 0
0x80206430	SNR0_LENC_LV_G60	0x00	RW	Bit[7:0]: G60 of 8x8 G control point array for L/VS of sensor 0
0x80206431	SNR0_LENC_LV_G61	0x00	RW	Bit[7:0]: G61 of 8x8 G control point array for L/VS of sensor 0
0x80206432	SNR0_LENC_LV_G62	0x00	RW	Bit[7:0]: G62 of 8x8 G control point array for L/VS of sensor 0
0x80206433	SNR0_LENC_LV_G63	0x00	RW	Bit[7:0]: G63 of 8x8 G control point array for L/VS of sensor 0
0x80206434	SNR0_LENC_LV_G64	0x00	RW	Bit[7:0]: G64 of 8x8 G control point array for L/VS of sensor 0
0x80206435	SNR0_LENC_LV_G65	0x00	RW	Bit[7:0]: G65 of 8x8 G control point array for L/VS of sensor 0
0x80206436	SNR0_LENC_LV_G66	0x00	RW	Bit[7:0]: G66 of 8x8 G control point array for L/VS of sensor 0
0x80206437	SNR0_LENC_LV_G67	0x00	RW	Bit[7:0]: G67 of 8x8 G control point array for L/VS of sensor 0
0x80206438	SNR0_LENC_LV_G70	0x00	RW	Bit[7:0]: G70 of 8x8 G control point array for L/VS of sensor 0
0x80206439	SNR0_LENC_LV_G71	0x00	RW	Bit[7:0]: G71 of 8x8 G control point array for L/VS of sensor 0
0x8020643A	SNR0_LENC_LV_G72	0x00	RW	Bit[7:0]: G72 of 8x8 G control point array for L/VS of sensor 0
0x8020643B	SNR0_LENC_LV_G73	0x00	RW	Bit[7:0]: G73 of 8x8 G control point array for L/VS of sensor 0
0x8020643C	SNR0_LENC_LV_G74	0x00	RW	Bit[7:0]: G74 of 8x8 G control point array for L/VS of sensor 0
0x8020643D	SNR0_LENC_LV_G75	0x00	RW	Bit[7:0]: G75 of 8x8 G control point array for L/VS of sensor 0
0x8020643E	SNR0_LENC_LV_G76	0x00	RW	Bit[7:0]: G76 of 8x8 G control point array for L/VS of sensor 0
0x8020643F	SNR0_LENC_LV_G77	0x00	RW	Bit[7:0]: G77 of 8x8 G control point array for L/VS of sensor 0
0x80206440	SNR0_LENC_LV_B00	0x20	RW	Bit[7:0]: B00 of 8x8 B control point array for L/VS of sensor 0
0x80206441	SNR0_LENC_LV_B01	0x20	RW	Bit[7:0]: B01 of 8x8 B control point array for L/VS of sensor 0

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table 3-2 LENC registers (sheet 5 of 41)

address	register name	default value	R/W	description
0x80206442	SNR0_LENC_LV_B02	0x20	RW	Bit[7:0]: B02 of 8x8 B control point array for L/VS of sensor 0
0x80206443	SNR0_LENC_LV_B03	0x20	RW	Bit[7:0]: B03 of 8x8 B control point array for L/VS of sensor 0
0x80206444	SNR0_LENC_LV_B04	0x20	RW	Bit[7:0]: B04 of 8x8 B control point array for L/VS of sensor 0
0x80206445	SNR0_LENC_LV_B05	0x20	RW	Bit[7:0]: B05 of 8x8 B control point array for L/VS of sensor 0
0x80206446	SNR0_LENC_LV_B06	0x20	RW	Bit[7:0]: B06 of 8x8 B control point array for L/VS of sensor 0
0x80206447	SNR0_LENC_LV_B07	0x20	RW	Bit[7:0]: B07 of 8x8 B control point array for L/VS of sensor 0
0x80206448	SNR0_LENC_LV_B10	0x20	RW	Bit[7:0]: B10 of 8x8 B control point array for L/VS of sensor 0
0x80206449	SNR0_LENC_LV_B11	0x20	RW	Bit[7:0]: B11 of 8x8 B control point array for L/VS of sensor 0
0x8020644A	SNR0_LENC_LV_B12	0x20	RW	Bit[7:0]: B12 of 8x8 B control point array for L/VS of sensor 0
0x8020644B	SNR0_LENC_LV_B13	0x20	RW	Bit[7:0]: B13 of 8x8 B control point array for L/VS of sensor 0
0x8020644C	SNR0_LENC_LV_B14	0x20	RW	Bit[7:0]: B14 of 8x8 B control point array for L/VS of sensor 0
0x8020644D	SNR0_LENC_LV_B15	0x20	RW	Bit[7:0]: B15 of 8x8 B control point array for L/VS of sensor 0
0x8020644E	SNR0_LENC_LV_B16	0x20	RW	Bit[7:0]: B16 of 8x8 B control point array for L/VS of sensor 0
0x8020644F	SNR0_LENC_LV_B17	0x20	RW	Bit[7:0]: B17 of 8x8 B control point array for L/VS of sensor 0
0x80206450	SNR0_LENC_LV_B20	0x20	RW	Bit[7:0]: B20 of 8x8 B control point array for L/VS of sensor 0
0x80206451	SNR0_LENC_LV_B21	0x20	RW	Bit[7:0]: B21 of 8x8 B control point array for L/VS of sensor 0
0x80206452	SNR0_LENC_LV_B22	0x20	RW	Bit[7:0]: B22 of 8x8 B control point array for L/VS of sensor 0
0x80206453	SNR0_LENC_LV_B23	0x20	RW	Bit[7:0]: B23 of 8x8 B control point array for L/VS of sensor 0
0x80206454	SNR0_LENC_LV_B24	0x20	RW	Bit[7:0]: B24 of 8x8 B control point array for L/VS of sensor 0

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table 3-2 LENC registers (sheet 6 of 41)

address	register name	default value	R/W	description
0x80206455	SNR0_LENC_LV_B25	0x20	RW	Bit[7:0]: B25 of 8x8 B control point array for L/VS of sensor 0
0x80206456	SNR0_LENC_LV_B26	0x20	RW	Bit[7:0]: B26 of 8x8 B control point array for L/VS of sensor 0
0x80206457	SNR0_LENC_LV_B27	0x20	RW	Bit[7:0]: B27 of 8x8 B control point array for L/VS of sensor 0
0x80206458	SNR0_LENC_LV_B30	0x20	RW	Bit[7:0]: B30 of 8x8 B control point array for L/VS of sensor 0
0x80206459	SNR0_LENC_LV_B31	0x20	RW	Bit[7:0]: B31 of 8x8 B control point array for L/VS of sensor 0
0x8020645A	SNR0_LENC_LV_B32	0x20	RW	Bit[7:0]: B32 of 8x8 B control point array for L/VS of sensor 0
0x8020645B	SNR0_LENC_LV_B33	0x20	RW	Bit[7:0]: B33 of 8x8 B control point array for L/VS of sensor 0
0x8020645C	SNR0_LENC_LV_B34	0x20	RW	Bit[7:0]: B34 of 8x8 B control point array for L/VS of sensor 0
0x8020645D	SNR0_LENC_LV_B35	0x20	RW	Bit[7:0]: B35 of 8x8 B control point array for L/VS of sensor 0
0x8020645E	SNR0_LENC_LV_B36	0x20	RW	Bit[7:0]: B36 of 8x8 B control point array for L/VS of sensor 0
0x8020645F	SNR0_LENC_LV_B37	0x20	RW	Bit[7:0]: B37 of 8x8 B control point array for L/VS of sensor 0
0x80206460	SNR0_LENC_LV_B40	0x20	RW	Bit[7:0]: B40 of 8x8 B control point array for L/VS of sensor 0
0x80206461	SNR0_LENC_LV_B41	0x20	RW	Bit[7:0]: B41 of 8x8 B control point array for L/VS of sensor 0
0x80206462	SNR0_LENC_LV_B42	0x20	RW	Bit[7:0]: B42 of 8x8 B control point array for L/VS of sensor 0
0x80206463	SNR0_LENC_LV_B43	0x20	RW	Bit[7:0]: B43 of 8x8 B control point array for L/VS of sensor 0
0x80206464	SNR0_LENC_LV_B44	0x20	RW	Bit[7:0]: B44 of 8x8 B control point array for L/VS of sensor 0
0x80206465	SNR0_LENC_LV_B45	0x20	RW	Bit[7:0]: B45 of 8x8 B control point array for L/VS of sensor 0
0x80206466	SNR0_LENC_LV_B46	0x20	RW	Bit[7:0]: B46 of 8x8 B control point array for L/VS of sensor 0
0x80206467	SNR0_LENC_LV_B47	0x20	RW	Bit[7:0]: B47 of 8x8 B control point array for L/VS of sensor 0

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table 3-2 LENC registers (sheet 7 of 41)

address	register name	default value	R/W	description
0x80206468	SNR0_LENC_LV_B50	0x20	RW	Bit[7:0]: B50 of 8x8 B control point array for L/VS of sensor 0
0x80206469	SNR0_LENC_LV_B51	0x20	RW	Bit[7:0]: B51 of 8x8 B control point array for L/VS of sensor 0
0x8020646A	SNR0_LENC_LV_B52	0x20	RW	Bit[7:0]: B52 of 8x8 B control point array for L/VS of sensor 0
0x8020646B	SNR0_LENC_LV_B53	0x20	RW	Bit[7:0]: B53 of 8x8 B control point array for L/VS of sensor 0
0x8020646C	SNR0_LENC_LV_B54	0x20	RW	Bit[7:0]: B54 of 8x8 B control point array for L/VS of sensor 0
0x8020646D	SNR0_LENC_LV_B55	0x20	RW	Bit[7:0]: B55 of 8x8 B control point array for L/VS of sensor 0
0x8020646E	SNR0_LENC_LV_B56	0x20	RW	Bit[7:0]: B56 of 8x8 B control point array for L/VS of sensor 0
0x8020646F	SNR0_LENC_LV_B57	0x20	RW	Bit[7:0]: B57 of 8x8 B control point array for L/VS of sensor 0
0x80206470	SNR0_LENC_LV_B60	0x20	RW	Bit[7:0]: B60 of 8x8 B control point array for L/VS of sensor 0
0x80206471	SNR0_LENC_LV_B61	0x20	RW	Bit[7:0]: B61 of 8x8 B control point array for L/VS of sensor 0
0x80206472	SNR0_LENC_LV_B62	0x20	RW	Bit[7:0]: B62 of 8x8 B control point array for L/VS of sensor 0
0x80206473	SNR0_LENC_LV_B63	0x20	RW	Bit[7:0]: B63 of 8x8 B control point array for L/VS of sensor 0
0x80206474	SNR0_LENC_LV_B64	0x20	RW	Bit[7:0]: B64 of 8x8 B control point array for L/VS of sensor 0
0x80206475	SNR0_LENC_LV_B65	0x20	RW	Bit[7:0]: B65 of 8x8 B control point array for L/VS of sensor 0
0x80206476	SNR0_LENC_LV_B66	0x20	RW	Bit[7:0]: B66 of 8x8 B control point array for L/VS of sensor 0
0x80206477	SNR0_LENC_LV_B67	0x20	RW	Bit[7:0]: B67 of 8x8 B control point array for L/VS of sensor 0
0x80206478	SNR0_LENC_LV_B70	0x20	RW	Bit[7:0]: B70 of 8x8 B control point array for L/VS of sensor 0
0x80206479	SNR0_LENC_LV_B71	0x20	RW	Bit[7:0]: B71 of 8x8 B control point array for L/VS of sensor 0
0x8020647A	SNR0_LENC_LV_B72	0x20	RW	Bit[7:0]: B72 of 8x8 B control point array for L/VS of sensor 0

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table 3-2 LENC registers (sheet 8 of 41)

address	register name	default value	R/W	description
0x8020647B	SNR0_LENC_LV_B73	0x20	RW	Bit[7:0]: B73 of 8x8 B control point array for L/VS of sensor 0
0x8020647C	SNR0_LENC_LV_B74	0x20	RW	Bit[7:0]: B74 of 8x8 B control point array for L/VS of sensor 0
0x8020647D	SNR0_LENC_LV_B75	0x20	RW	Bit[7:0]: B75 of 8x8 B control point array for L/VS of sensor 0
0x8020647E	SNR0_LENC_LV_B76	0x20	RW	Bit[7:0]: B76 of 8x8 B control point array for L/VS of sensor 0
0x8020647F	SNR0_LENC_LV_B77	0x20	RW	Bit[7:0]: B77 of 8x8 B control point array for L/VS of sensor 0
0x80206480	SNR0_LENC_LV_R00	0x20	RW	Bit[7:0]: R00 of 8x8 R control point array for L/VS of sensor 0
0x80206481	SNR0_LENC_LV_R01	0x20	RW	Bit[7:0]: R01 of 8x8 R control point array for L/VS of sensor 0
0x80206482	SNR0_LENC_LV_R02	0x20	RW	Bit[7:0]: R02 of 8x8 R control point array for L/VS of sensor 0
0x80206483	SNR0_LENC_LV_R03	0x20	RW	Bit[7:0]: R03 of 8x8 R control point array for L/VS of sensor 0
0x80206484	SNR0_LENC_LV_R04	0x20	RW	Bit[7:0]: R04 of 8x8 R control point array for L/VS of sensor 0
0x80206485	SNR0_LENC_LV_R05	0x20	RW	Bit[7:0]: R05 of 8x8 R control point array for L/VS of sensor 0
0x80206486	SNR0_LENC_LV_R06	0x20	RW	Bit[7:0]: R06 of 8x8 R control point array for L/VS of sensor 0
0x80206487	SNR0_LENC_LV_R07	0x20	RW	Bit[7:0]: R07 of 8x8 R control point array for L/VS of sensor 0
0x80206488	SNR0_LENC_LV_R10	0x20	RW	Bit[7:0]: R10 of 8x8 R control point array for L/VS of sensor 0
0x80206489	SNR0_LENC_LV_R11	0x20	RW	Bit[7:0]: R11 of 8x8 R control point array for L/VS of sensor 0
0x8020648A	SNR0_LENC_LV_R12	0x20	RW	Bit[7:0]: R12 of 8x8 R control point array for L/VS of sensor 0
0x8020648B	SNR0_LENC_LV_R13	0x20	RW	Bit[7:0]: R13 of 8x8 R control point array for L/VS of sensor 0
0x8020648C	SNR0_LENC_LV_R14	0x20	RW	Bit[7:0]: R14 of 8x8 R control point array for L/VS of sensor 0
0x8020648D	SNR0_LENC_LV_R15	0x20	RW	Bit[7:0]: R15 of 8x8 R control point array for L/VS of sensor 0

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table 3-2 LENC registers (sheet 9 of 41)

address	register name	default value	R/W	description
0x8020648E	SNR0_LENC_LV_R16	0x20	RW	Bit[7:0]: R16 of 8x8 R control point array for L/VS of sensor 0
0x8020648F	SNR0_LENC_LV_R17	0x20	RW	Bit[7:0]: R17 of 8x8 R control point array for L/VS of sensor 0
0x80206490	SNR0_LENC_LV_R20	0x20	RW	Bit[7:0]: R20 of 8x8 R control point array for L/VS of sensor 0
0x80206491	SNR0_LENC_LV_R21	0x20	RW	Bit[7:0]: R21 of 8x8 R control point array for L/VS of sensor 0
0x80206492	SNR0_LENC_LV_R22	0x20	RW	Bit[7:0]: R22 of 8x8 R control point array for L/VS of sensor 0
0x80206493	SNR0_LENC_LV_R23	0x20	RW	Bit[7:0]: R23 of 8x8 R control point array for L/VS of sensor 0
0x80206494	SNR0_LENC_LV_R24	0x20	RW	Bit[7:0]: R24 of 8x8 R control point array for L/VS of sensor 0
0x80206495	SNR0_LENC_LV_R25	0x20	RW	Bit[7:0]: R25 of 8x8 R control point array for L/VS of sensor 0
0x80206496	SNR0_LENC_LV_R26	0x20	RW	Bit[7:0]: R26 of 8x8 R control point array for L/VS of sensor 0
0x80206497	SNR0_LENC_LV_R27	0x20	RW	Bit[7:0]: R27 of 8x8 R control point array for L/VS of sensor 0
0x80206498	SNR0_LENC_LV_R30	0x20	RW	Bit[7:0]: R30 of 8x8 R control point array for L/VS of sensor 0
0x80206499	SNR0_LENC_LV_R31	0x20	RW	Bit[7:0]: R31 of 8x8 R control point array for L/VS of sensor 0
0x8020649A	SNR0_LENC_LV_R32	0x20	RW	Bit[7:0]: R32 of 8x8 R control point array for L/VS of sensor 0
0x8020649B	SNR0_LENC_LV_R33	0x20	RW	Bit[7:0]: R33 of 8x8 R control point array for L/VS of sensor 0
0x8020649C	SNR0_LENC_LV_R34	0x20	RW	Bit[7:0]: R34 of 8x8 R control point array for L/VS of sensor 0
0x8020649D	SNR0_LENC_LV_R35	0x20	RW	Bit[7:0]: R35 of 8x8 R control point array for L/VS of sensor 0
0x8020649E	SNR0_LENC_LV_R36	0x20	RW	Bit[7:0]: R36 of 8x8 R control point array for L/VS of sensor 0
0x8020649F	SNR0_LENC_LV_R37	0x20	RW	Bit[7:0]: R37 of 8x8 R control point array for L/VS of sensor 0
0x802064A0	SNR0_LENC_LV_R40	0x20	RW	Bit[7:0]: R40 of 8x8 R control point array for L/VS of sensor 0

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table 3-2 LENC registers (sheet 10 of 41)

address	register name	default value	R/W	description
0x802064A1	SNR0_LENC_LV_R41	0x20	RW	Bit[7:0]: R41 of 8x8 R control point array for L/VS of sensor 0
0x802064A2	SNR0_LENC_LV_R42	0x20	RW	Bit[7:0]: R42 of 8x8 R control point array for L/VS of sensor 0
0x802064A3	SNR0_LENC_LV_R43	0x20	RW	Bit[7:0]: R43 of 8x8 R control point array for L/VS of sensor 0
0x802064A4	SNR0_LENC_LV_R44	0x20	RW	Bit[7:0]: R44 of 8x8 R control point array for L/VS of sensor 0
0x802064A5	SNR0_LENC_LV_R45	0x20	RW	Bit[7:0]: R45 of 8x8 R control point array for L/VS of sensor 0
0x802064A6	SNR0_LENC_LV_R46	0x20	RW	Bit[7:0]: R46 of 8x8 R control point array for L/VS of sensor 0
0x802064A7	SNR0_LENC_LV_R47	0x20	RW	Bit[7:0]: R47 of 8x8 R control point array for L/VS of sensor 0
0x802064A8	SNR0_LENC_LV_R50	0x20	RW	Bit[7:0]: R50 of 8x8 R control point array for L/VS of sensor 0
0x802064A9	SNR0_LENC_LV_R51	0x20	RW	Bit[7:0]: R51 of 8x8 R control point array for L/VS of sensor 0
0x802064AA	SNR0_LENC_LV_R52	0x20	RW	Bit[7:0]: R52 of 8x8 R control point array for L/VS of sensor 0
0x802064AB	SNR0_LENC_LV_R53	0x20	RW	Bit[7:0]: R53 of 8x8 R control point array for L/VS of sensor 0
0x802064AC	SNR0_LENC_LV_R54	0x20	RW	Bit[7:0]: R54 of 8x8 R control point array for L/VS of sensor 0
0x802064AD	SNR0_LENC_LV_R55	0x20	RW	Bit[7:0]: R55 of 8x8 R control point array for L/VS of sensor 0
0x802064AE	SNR0_LENC_LV_R56	0x20	RW	Bit[7:0]: R56 of 8x8 R control point array for L/VS of sensor 0
0x802064AF	SNR0_LENC_LV_R57	0x20	RW	Bit[7:0]: R57 of 8x8 R control point array for L/VS of sensor 0
0x802064B0	SNR0_LENC_LV_R60	0x20	RW	Bit[7:0]: R60 of 8x8 R control point array for L/VS of sensor 0
0x802064B1	SNR0_LENC_LV_R61	0x20	RW	Bit[7:0]: R61 of 8x8 R control point array for L/VS of sensor 0
0x802064B2	SNR0_LENC_LV_R62	0x20	RW	Bit[7:0]: R62 of 8x8 R control point array for L/VS of sensor 0
0x802064B3	SNR0_LENC_LV_R63	0x20	RW	Bit[7:0]: R63 of 8x8 R control point array for L/VS of sensor 0

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table 3-2 LENC registers (sheet 11 of 41)

address	register name	default value	R/W	description
0x802064B4	SNR0_LENC_LV_R64	0x20	RW	Bit[7:0]: R64 of 8x8 R control point array for L/VS of sensor 0
0x802064B5	SNR0_LENC_LV_R65	0x20	RW	Bit[7:0]: R65 of 8x8 R control point array for L/VS of sensor 0
0x802064B6	SNR0_LENC_LV_R66	0x20	RW	Bit[7:0]: R66 of 8x8 R control point array for L/VS of sensor 0
0x802064B7	SNR0_LENC_LV_R67	0x20	RW	Bit[7:0]: R67 of 8x8 R control point array for L/VS of sensor 0
0x802064B8	SNR0_LENC_LV_R70	0x20	RW	Bit[7:0]: R70 of 8x8 R control point array for L/VS of sensor 0
0x802064B9	SNR0_LENC_LV_R71	0x20	RW	Bit[7:0]: R71 of 8x8 R control point array for L/VS of sensor 0
0x802064BA	SNR0_LENC_LV_R72	0x20	RW	Bit[7:0]: R72 of 8x8 R control point array for L/VS of sensor 0
0x802064BB	SNR0_LENC_LV_R73	0x20	RW	Bit[7:0]: R73 of 8x8 R control point array for L/VS of sensor 0
0x802064BC	SNR0_LENC_LV_R74	0x20	RW	Bit[7:0]: R74 of 8x8 R control point array for L/VS of sensor 0
0x802064BD	SNR0_LENC_LV_R75	0x20	RW	Bit[7:0]: R75 of 8x8 R control point array for L/VS of sensor 0
0x802064BE	SNR0_LENC_LV_R76	0x20	RW	Bit[7:0]: R76 of 8x8 R control point array for L/VS of sensor 0
0x802064BF	SNR0_LENC_LV_R77	0x20	RW	Bit[7:0]: R77 of 8x8 R control point array for L/VS of sensor 0
0x802064C0	SNR0_LENC_S_G00	0x00	RW	Bit[7:0]: G00 of 8x8 G control point array for S of sensor 0
0x802064C1	SNR0_LENC_S_G01	0x00	RW	Bit[7:0]: G01 of 8x8 G control point array for S of sensor 0
0x802064C2	SNR0_LENC_S_G02	0x00	RW	Bit[7:0]: G02 of 8x8 G control point array for S of sensor 0
0x802064C3	SNR0_LENC_S_G03	0x00	RW	Bit[7:0]: G03 of 8x8 G control point array for S of sensor 0
0x802064C4	SNR0_LENC_S_G04	0x00	RW	Bit[7:0]: G04 of 8x8 G control point array for S of sensor 0
0x802064C5	SNR0_LENC_S_G05	0x00	RW	Bit[7:0]: G05 of 8x8 G control point array for S of sensor 0
0x802064C6	SNR0_LENC_S_G06	0x00	RW	Bit[7:0]: G06 of 8x8 G control point array for S of sensor 0

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table 3-2 LENC registers (sheet 12 of 41)

address	register name	default value	R/W	description
0x802064C7	SNR0_LENC_S_G07	0x00	RW	Bit[7:0]: G07 of 8x8 G control point array for S of sensor 0
0x802064C8	SNR0_LENC_S_G10	0x00	RW	Bit[7:0]: G10 of 8x8 G control point array for S of sensor 0
0x802064C9	SNR0_LENC_S_G11	0x00	RW	Bit[7:0]: G11 of 8x8 G control point array for S of sensor 0
0x802064CA	SNR0_LENC_S_G12	0x00	RW	Bit[7:0]: G12 of 8x8 G control point array for S of sensor 0
0x802064CB	SNR0_LENC_S_G13	0x00	RW	Bit[7:0]: G13 of 8x8 G control point array for S of sensor 0
0x802064CC	SNR0_LENC_S_G14	0x00	RW	Bit[7:0]: G14 of 8x8 G control point array for S of sensor 0
0x802064CD	SNR0_LENC_S_G15	0x00	RW	Bit[7:0]: G15 of 8x8 G control point array for S of sensor 0
0x802064CE	SNR0_LENC_S_G16	0x00	RW	Bit[7:0]: G16 of 8x8 G control point array for S of sensor 0
0x802064CF	SNR0_LENC_S_G17	0x00	RW	Bit[7:0]: G17 of 8x8 G control point array for S of sensor 0
0x802064D0	SNR0_LENC_S_G20	0x00	RW	Bit[7:0]: G20 of 8x8 G control point array for S of sensor 0
0x802064D1	SNR0_LENC_S_G21	0x00	RW	Bit[7:0]: G21 of 8x8 G control point array for S of sensor 0
0x802064D2	SNR0_LENC_S_G22	0x00	RW	Bit[7:0]: G22 of 8x8 G control point array for S of sensor 0
0x802064D3	SNR0_LENC_S_G23	0x00	RW	Bit[7:0]: G23 of 8x8 G control point array for S of sensor 0
0x802064D4	SNR0_LENC_S_G24	0x00	RW	Bit[7:0]: G24 of 8x8 G control point array for S of sensor 0
0x802064D5	SNR0_LENC_S_G25	0x00	RW	Bit[7:0]: G25 of 8x8 G control point array for S of sensor 0
0x802064D6	SNR0_LENC_S_G26	0x00	RW	Bit[7:0]: G26 of 8x8 G control point array for S of sensor 0
0x802064D7	SNR0_LENC_S_G27	0x00	RW	Bit[7:0]: G27 of 8x8 G control point array for S of sensor 0
0x802064D8	SNR0_LENC_S_G30	0x00	RW	Bit[7:0]: G30 of 8x8 G control point array for S of sensor 0
0x802064D9	SNR0_LENC_S_G31	0x00	RW	Bit[7:0]: G31 of 8x8 G control point array for S of sensor 0

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table 3-2 LENC registers (sheet 13 of 41)

address	register name	default value	R/W	description
0x802064DA	SNR0_LENC_S_G32	0x00	RW	Bit[7:0]: G32 of 8x8 G control point array for S of sensor 0
0x802064DB	SNR0_LENC_S_G33	0x00	RW	Bit[7:0]: G33 of 8x8 G control point array for S of sensor 0
0x802064DC	SNR0_LENC_S_G34	0x00	RW	Bit[7:0]: G34 of 8x8 G control point array for S of sensor 0
0x802064DD	SNR0_LENC_S_G35	0x00	RW	Bit[7:0]: G35 of 8x8 G control point array for S of sensor 0
0x802064DE	SNR0_LENC_S_G36	0x00	RW	Bit[7:0]: G36 of 8x8 G control point array for S of sensor 0
0x802064DF	SNR0_LENC_S_G37	0x00	RW	Bit[7:0]: G37 of 8x8 G control point array for S of sensor 0
0x802064E0	SNR0_LENC_S_G40	0x00	RW	Bit[7:0]: G40 of 8x8 G control point array for S of sensor 0
0x802064E1	SNR0_LENC_S_G41	0x00	RW	Bit[7:0]: G41 of 8x8 G control point array for S of sensor 0
0x802064E2	SNR0_LENC_S_G42	0x00	RW	Bit[7:0]: G42 of 8x8 G control point array for S of sensor 0
0x802064E3	SNR0_LENC_S_G43	0x00	RW	Bit[7:0]: G43 of 8x8 G control point array for S of sensor 0
0x802064E4	SNR0_LENC_S_G44	0x00	RW	Bit[7:0]: G44 of 8x8 G control point array for S of sensor 0
0x802064E5	SNR0_LENC_S_G45	0x00	RW	Bit[7:0]: G45 of 8x8 G control point array for S of sensor 0
0x802064E6	SNR0_LENC_S_G46	0x00	RW	Bit[7:0]: G46 of 8x8 G control point array for S of sensor 0
0x802064E7	SNR0_LENC_S_G47	0x00	RW	Bit[7:0]: G47 of 8x8 G control point array for S of sensor 0
0x802064E8	SNR0_LENC_S_G50	0x00	RW	Bit[7:0]: G50 of 8x8 G control point array for S of sensor 0
0x802064E9	SNR0_LENC_S_G51	0x00	RW	Bit[7:0]: G51 of 8x8 G control point array for S of sensor 0
0x802064EA	SNR0_LENC_S_G52	0x00	RW	Bit[7:0]: G52 of 8x8 G control point array for S of sensor 0
0x802064EB	SNR0_LENC_S_G53	0x00	RW	Bit[7:0]: G53 of 8x8 G control point array for S of sensor 0
0x802064EC	SNR0_LENC_S_G54	0x00	RW	Bit[7:0]: G54 of 8x8 G control point array for S of sensor 0

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table 3-2 LENC registers (sheet 14 of 41)

address	register name	default value	R/W	description
0x802064ED	SNR0_LENC_S_G55	0x00	RW	Bit[7:0]: G55 of 8x8 G control point array for S of sensor 0
0x802064EE	SNR0_LENC_S_G56	0x00	RW	Bit[7:0]: G56 of 8x8 G control point array for S of sensor 0
0x802064EF	SNR0_LENC_S_G57	0x00	RW	Bit[7:0]: G57 of 8x8 G control point array for S of sensor 0
0x802064F0	SNR0_LENC_S_G60	0x00	RW	Bit[7:0]: G60 of 8x8 G control point array for S of sensor 0
0x802064F1	SNR0_LENC_S_G61	0x00	RW	Bit[7:0]: G61 of 8x8 G control point array for S of sensor 0
0x802064F2	SNR0_LENC_S_G62	0x00	RW	Bit[7:0]: G62 of 8x8 G control point array for S of sensor 0
0x802064F3	SNR0_LENC_S_G63	0x00	RW	Bit[7:0]: G63 of 8x8 G control point array for S of sensor 0
0x802064F4	SNR0_LENC_S_G64	0x00	RW	Bit[7:0]: G64 of 8x8 G control point array for S of sensor 0
0x802064F5	SNR0_LENC_S_G65	0x00	RW	Bit[7:0]: G65 of 8x8 G control point array for S of sensor 0
0x802064F6	SNR0_LENC_S_G66	0x00	RW	Bit[7:0]: G66 of 8x8 G control point array for S of sensor 0
0x802064F7	SNR0_LENC_S_G67	0x00	RW	Bit[7:0]: G67 of 8x8 G control point array for S of sensor 0
0x802064F8	SNR0_LENC_S_G70	0x00	RW	Bit[7:0]: G70 of 8x8 G control point array for S of sensor 0
0x802064F9	SNR0_LENC_S_G71	0x00	RW	Bit[7:0]: G71 of 8x8 G control point array for S of sensor 0
0x802064FA	SNR0_LENC_S_G72	0x00	RW	Bit[7:0]: G72 of 8x8 G control point array for S of sensor 0
0x802064FB	SNR0_LENC_S_G73	0x00	RW	Bit[7:0]: G73 of 8x8 G control point array for S of sensor 0
0x802064FC	SNR0_LENC_S_G74	0x00	RW	Bit[7:0]: G74 of 8x8 G control point array for S of sensor 0
0x802064FD	SNR0_LENC_S_G75	0x00	RW	Bit[7:0]: G75 of 8x8 G control point array for S of sensor 0
0x802064FE	SNR0_LENC_S_G76	0x00	RW	Bit[7:0]: G76 of 8x8 G control point array for S of sensor 0
0x802064FF	SNR0_LENC_S_G77	0x00	RW	Bit[7:0]: G77 of 8x8 G control point array for S of sensor 0

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table 3-2 LENC registers (sheet 15 of 41)

address	register name	default value	R/W	description
0x80206500	SNR0_LENC_S_B00	0x20	RW	Bit[7:0]: B00 of 8x8 B control point array for S of sensor 0
0x80206501	SNR0_LENC_S_B01	0x20	RW	Bit[7:0]: B01 of 8x8 B control point array for S of sensor 0
0x80206502	SNR0_LENC_S_B02	0x20	RW	Bit[7:0]: B02 of 8x8 B control point array for S of sensor 0
0x80206503	SNR0_LENC_S_B03	0x20	RW	Bit[7:0]: B03 of 8x8 B control point array for S of sensor 0
0x80206504	SNR0_LENC_S_B04	0x20	RW	Bit[7:0]: B04 of 8x8 B control point array for S of sensor 0
0x80206505	SNR0_LENC_S_B05	0x20	RW	Bit[7:0]: B05 of 8x8 B control point array for S of sensor 0
0x80206506	SNR0_LENC_S_B06	0x20	RW	Bit[7:0]: B06 of 8x8 B control point array for S of sensor 0
0x80206507	SNR0_LENC_S_B07	0x20	RW	Bit[7:0]: B07 of 8x8 B control point array for S of sensor 0
0x80206508	SNR0_LENC_S_B10	0x20	RW	Bit[7:0]: B10 of 8x8 B control point array for S of sensor 0
0x80206509	SNR0_LENC_S_B11	0x20	RW	Bit[7:0]: B11 of 8x8 B control point array for S of sensor 0
0x8020650A	SNR0_LENC_S_B12	0x20	RW	Bit[7:0]: B12 of 8x8 B control point array for S of sensor 0
0x8020650B	SNR0_LENC_S_B13	0x20	RW	Bit[7:0]: B13 of 8x8 B control point array for S of sensor 0
0x8020650C	SNR0_LENC_S_B14	0x20	RW	Bit[7:0]: B14 of 8x8 B control point array for S of sensor 0
0x8020650D	SNR0_LENC_S_B15	0x20	RW	Bit[7:0]: B15 of 8x8 B control point array for S of sensor 0
0x8020650E	SNR0_LENC_S_B16	0x20	RW	Bit[7:0]: B16 of 8x8 B control point array for S of sensor 0
0x8020650F	SNR0_LENC_S_B17	0x20	RW	Bit[7:0]: B17 of 8x8 B control point array for S of sensor 0
0x80206510	SNR0_LENC_S_B20	0x20	RW	Bit[7:0]: B20 of 8x8 B control point array for S of sensor 0
0x80206511	SNR0_LENC_S_B21	0x20	RW	Bit[7:0]: B21 of 8x8 B control point array for S of sensor 0
0x80206512	SNR0_LENC_S_B22	0x20	RW	Bit[7:0]: B22 of 8x8 B control point array for S of sensor 0

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table 3-2 LENC registers (sheet 16 of 41)

address	register name	default value	R/W	description
0x80206513	SNR0_LENC_S_B23	0x20	RW	Bit[7:0]: B23 of 8x8 B control point array for S of sensor 0
0x80206514	SNR0_LENC_S_B24	0x20	RW	Bit[7:0]: B24 of 8x8 B control point array for S of sensor 0
0x80206515	SNR0_LENC_S_B25	0x20	RW	Bit[7:0]: B25 of 8x8 B control point array for S of sensor 0
0x80206516	SNR0_LENC_S_B26	0x20	RW	Bit[7:0]: B26 of 8x8 B control point array for S of sensor 0
0x80206517	SNR0_LENC_S_B27	0x20	RW	Bit[7:0]: B27 of 8x8 B control point array for S of sensor 0
0x80206518	SNR0_LENC_S_B30	0x20	RW	Bit[7:0]: B30 of 8x8 B control point array for S of sensor 0
0x80206519	SNR0_LENC_S_B31	0x20	RW	Bit[7:0]: B31 of 8x8 B control point array for S of sensor 0
0x8020651A	SNR0_LENC_S_B32	0x20	RW	Bit[7:0]: B32 of 8x8 B control point array for S of sensor 0
0x8020651B	SNR0_LENC_S_B33	0x20	RW	Bit[7:0]: B33 of 8x8 B control point array for S of sensor 0
0x8020651C	SNR0_LENC_S_B34	0x20	RW	Bit[7:0]: B34 of 8x8 B control point array for S of sensor 0
0x8020651D	SNR0_LENC_S_B35	0x20	RW	Bit[7:0]: B35 of 8x8 B control point array for S of sensor 0
0x8020651E	SNR0_LENC_S_B36	0x20	RW	Bit[7:0]: B36 of 8x8 B control point array for S of sensor 0
0x8020651F	SNR0_LENC_S_B37	0x20	RW	Bit[7:0]: B37 of 8x8 B control point array for S of sensor 0
0x80206520	SNR0_LENC_S_B40	0x20	RW	Bit[7:0]: B40 of 8x8 B control point array for S of sensor 0
0x80206521	SNR0_LENC_S_B41	0x20	RW	Bit[7:0]: B41 of 8x8 B control point array for S of sensor 0
0x80206522	SNR0_LENC_S_B42	0x20	RW	Bit[7:0]: B42 of 8x8 B control point array for S of sensor 0
0x80206523	SNR0_LENC_S_B43	0x20	RW	Bit[7:0]: B43 of 8x8 B control point array for S of sensor 0
0x80206524	SNR0_LENC_S_B44	0x20	RW	Bit[7:0]: B44 of 8x8 B control point array for S of sensor 0
0x80206525	SNR0_LENC_S_B45	0x20	RW	Bit[7:0]: B45 of 8x8 B control point array for S of sensor 0

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table 3-2 LENC registers (sheet 17 of 41)

address	register name	default value	R/W	description
0x80206526	SNR0_LENC_S_B46	0x20	RW	Bit[7:0]: B46 of 8x8 B control point array for S of sensor 0
0x80206527	SNR0_LENC_S_B47	0x20	RW	Bit[7:0]: B47 of 8x8 B control point array for S of sensor 0
0x80206528	SNR0_LENC_S_B50	0x20	RW	Bit[7:0]: B50 of 8x8 B control point array for S of sensor 0
0x80206529	SNR0_LENC_S_B51	0x20	RW	Bit[7:0]: B51 of 8x8 B control point array for S of sensor 0
0x8020652A	SNR0_LENC_S_B52	0x20	RW	Bit[7:0]: B52 of 8x8 B control point array for S of sensor 0
0x8020652B	SNR0_LENC_S_B53	0x20	RW	Bit[7:0]: B53 of 8x8 B control point array for S of sensor 0
0x8020652C	SNR0_LENC_S_B54	0x20	RW	Bit[7:0]: B54 of 8x8 B control point array for S of sensor 0
0x8020652D	SNR0_LENC_S_B55	0x20	RW	Bit[7:0]: B55 of 8x8 B control point array for S of sensor 0
0x8020652E	SNR0_LENC_S_B56	0x20	RW	Bit[7:0]: B56 of 8x8 B control point array for S of sensor 0
0x8020652F	SNR0_LENC_S_B57	0x20	RW	Bit[7:0]: B57 of 8x8 B control point array for S of sensor 0
0x80206530	SNR0_LENC_S_B60	0x20	RW	Bit[7:0]: B60 of 8x8 B control point array for S of sensor 0
0x80206531	SNR0_LENC_S_B61	0x20	RW	Bit[7:0]: B61 of 8x8 B control point array for S of sensor 0
0x80206532	SNR0_LENC_S_B62	0x20	RW	Bit[7:0]: B62 of 8x8 B control point array for S of sensor 0
0x80206533	SNR0_LENC_S_B63	0x20	RW	Bit[7:0]: B63 of 8x8 B control point array for S of sensor 0
0x80206534	SNR0_LENC_S_B64	0x20	RW	Bit[7:0]: B64 of 8x8 B control point array for S of sensor 0
0x80206535	SNR0_LENC_S_B65	0x20	RW	Bit[7:0]: B65 of 8x8 B control point array for S of sensor 0
0x80206536	SNR0_LENC_S_B66	0x20	RW	Bit[7:0]: B66 of 8x8 B control point array for S of sensor 0
0x80206537	SNR0_LENC_S_B67	0x20	RW	Bit[7:0]: B67 of 8x8 B control point array for S of sensor 0
0x80206538	SNR0_LENC_S_B70	0x20	RW	Bit[7:0]: B70 of 8x8 B control point array for S of sensor 0

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table 3-2 LENC registers (sheet 18 of 41)

address	register name	default value	R/W	description
0x80206539	SNR0_LENC_S_B71	0x20	RW	Bit[7:0]: B71 of 8x8 B control point array for S of sensor 0
0x8020653A	SNR0_LENC_S_B72	0x20	RW	Bit[7:0]: B72 of 8x8 B control point array for S of sensor 0
0x8020653B	SNR0_LENC_S_B73	0x20	RW	Bit[7:0]: B73 of 8x8 B control point array for S of sensor 0
0x8020653C	SNR0_LENC_S_B74	0x20	RW	Bit[7:0]: B74 of 8x8 B control point array for S of sensor 0
0x8020653D	SNR0_LENC_S_B75	0x20	RW	Bit[7:0]: B75 of 8x8 B control point array for S of sensor 0
0x8020653E	SNR0_LENC_S_B76	0x20	RW	Bit[7:0]: B76 of 8x8 B control point array for S of sensor 0
0x8020653F	SNR0_LENC_S_B77	0x20	RW	Bit[7:0]: B77 of 8x8 B control point array for S of sensor 0
0x80206540	SNR0_LENC_S_R00	0x20	RW	Bit[7:0]: R00 of 8x8 R control point array for S of sensor 0
0x80206541	SNR0_LENC_S_R01	0x20	RW	Bit[7:0]: R01 of 8x8 R control point array for S of sensor 0
0x80206542	SNR0_LENC_S_R02	0x20	RW	Bit[7:0]: R02 of 8x8 R control point array for S of sensor 0
0x80206543	SNR0_LENC_S_R03	0x20	RW	Bit[7:0]: R03 of 8x8 R control point array for S of sensor 0
0x80206544	SNR0_LENC_S_R04	0x20	RW	Bit[7:0]: R04 of 8x8 R control point array for S of sensor 0
0x80206545	SNR0_LENC_S_R05	0x20	RW	Bit[7:0]: R05 of 8x8 R control point array for S of sensor 0
0x80206546	SNR0_LENC_S_R06	0x20	RW	Bit[7:0]: R06 of 8x8 R control point array for S of sensor 0
0x80206547	SNR0_LENC_S_R07	0x20	RW	Bit[7:0]: R07 of 8x8 R control point array for S of sensor 0
0x80206548	SNR0_LENC_S_R10	0x20	RW	Bit[7:0]: R10 of 8x8 R control point array for S of sensor 0
0x80206549	SNR0_LENC_S_R11	0x20	RW	Bit[7:0]: R11 of 8x8 R control point array for S of sensor 0
0x8020654A	SNR0_LENC_S_R12	0x20	RW	Bit[7:0]: R12 of 8x8 R control point array for S of sensor 0
0x8020654B	SNR0_LENC_S_R13	0x20	RW	Bit[7:0]: R13 of 8x8 R control point array for S of sensor 0

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table 3-2 LENC registers (sheet 19 of 41)

address	register name	default value	R/W	description
0x8020654C	SNR0_LENC_S_R14	0x20	RW	Bit[7:0]: R14 of 8x8 R control point array for S of sensor 0
0x8020654D	SNR0_LENC_S_R15	0x20	RW	Bit[7:0]: R15 of 8x8 R control point array for S of sensor 0
0x8020654E	SNR0_LENC_S_R16	0x20	RW	Bit[7:0]: R16 of 8x8 R control point array for S of sensor 0
0x8020654F	SNR0_LENC_S_R17	0x20	RW	Bit[7:0]: R17 of 8x8 R control point array for S of sensor 0
0x80206550	SNR0_LENC_S_R20	0x20	RW	Bit[7:0]: R20 of 8x8 R control point array for S of sensor 0
0x80206551	SNR0_LENC_S_R21	0x20	RW	Bit[7:0]: R21 of 8x8 R control point array for S of sensor 0
0x80206552	SNR0_LENC_S_R22	0x20	RW	Bit[7:0]: R22 of 8x8 R control point array for S of sensor 0
0x80206553	SNR0_LENC_S_R23	0x20	RW	Bit[7:0]: R23 of 8x8 R control point array for S of sensor 0
0x80206554	SNR0_LENC_S_R24	0x20	RW	Bit[7:0]: R24 of 8x8 R control point array for S of sensor 0
0x80206555	SNR0_LENC_S_R25	0x20	RW	Bit[7:0]: R25 of 8x8 R control point array for S of sensor 0
0x80206556	SNR0_LENC_S_R26	0x20	RW	Bit[7:0]: R26 of 8x8 R control point array for S of sensor 0
0x80206557	SNR0_LENC_S_R27	0x20	RW	Bit[7:0]: R27 of 8x8 R control point array for S of sensor 0
0x80206558	SNR0_LENC_S_R30	0x20	RW	Bit[7:0]: R30 of 8x8 R control point array for S of sensor 0
0x80206559	SNR0_LENC_S_R31	0x20	RW	Bit[7:0]: R31 of 8x8 R control point array for S of sensor 0
0x8020655A	SNR0_LENC_S_R32	0x20	RW	Bit[7:0]: R32 of 8x8 R control point array for S of sensor 0
0x8020655B	SNR0_LENC_S_R33	0x20	RW	Bit[7:0]: R33 of 8x8 R control point array for S of sensor 0
0x8020655C	SNR0_LENC_S_R34	0x20	RW	Bit[7:0]: R34 of 8x8 R control point array for S of sensor 0
0x8020655D	SNR0_LENC_S_R35	0x20	RW	Bit[7:0]: R35 of 8x8 R control point array for S of sensor 0
0x8020655E	SNR0_LENC_S_R36	0x20	RW	Bit[7:0]: R36 of 8x8 R control point array for S of sensor 0

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table 3-2 LENC registers (sheet 20 of 41)

address	register name	default value	R/W	description
0x8020655F	SNR0_LENC_S_R37	0x20	RW	Bit[7:0]: R37 of 8x8 R control point array for S of sensor 0
0x80206560	SNR0_LENC_S_R40	0x20	RW	Bit[7:0]: R40 of 8x8 R control point array for S of sensor 0
0x80206561	SNR0_LENC_S_R41	0x20	RW	Bit[7:0]: R41 of 8x8 R control point array for S of sensor 0
0x80206562	SNR0_LENC_S_R42	0x20	RW	Bit[7:0]: R42 of 8x8 R control point array for S of sensor 0
0x80206563	SNR0_LENC_S_R43	0x20	RW	Bit[7:0]: R43 of 8x8 R control point array for S of sensor 0
0x80206564	SNR0_LENC_S_R44	0x20	RW	Bit[7:0]: R44 of 8x8 R control point array for S of sensor 0
0x80206565	SNR0_LENC_S_R45	0x20	RW	Bit[7:0]: R45 of 8x8 R control point array for S of sensor 0
0x80206566	SNR0_LENC_S_R46	0x20	RW	Bit[7:0]: R46 of 8x8 R control point array for S of sensor 0
0x80206567	SNR0_LENC_S_R47	0x20	RW	Bit[7:0]: R47 of 8x8 R control point array for S of sensor 0
0x80206568	SNR0_LENC_S_R50	0x20	RW	Bit[7:0]: R50 of 8x8 R control point array for S of sensor 0
0x80206569	SNR0_LENC_S_R51	0x20	RW	Bit[7:0]: R51 of 8x8 R control point array for S of sensor 0
0x8020656A	SNR0_LENC_S_R52	0x20	RW	Bit[7:0]: R52 of 8x8 R control point array for S of sensor 0
0x8020656B	SNR0_LENC_S_R53	0x20	RW	Bit[7:0]: R53 of 8x8 R control point array for S of sensor 0
0x8020656C	SNR0_LENC_S_R54	0x20	RW	Bit[7:0]: R54 of 8x8 R control point array for S of sensor 0
0x8020656D	SNR0_LENC_S_R55	0x20	RW	Bit[7:0]: R55 of 8x8 R control point array for S of sensor 0
0x8020656E	SNR0_LENC_S_R56	0x20	RW	Bit[7:0]: R56 of 8x8 R control point array for S of sensor 0
0x8020656F	SNR0_LENC_S_R57	0x20	RW	Bit[7:0]: R57 of 8x8 R control point array for S of sensor 0
0x80206570	SNR0_LENC_S_R60	0x20	RW	Bit[7:0]: R60 of 8x8 R control point array for S of sensor 0
0x80206571	SNR0_LENC_S_R61	0x20	RW	Bit[7:0]: R61 of 8x8 R control point array for S of sensor 0

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table 3-2 LENC registers (sheet 21 of 41)

address	register name	default value	R/W	description
0x80206572	SNR0_LENC_S_R62	0x20	RW	Bit[7:0]: R62 of 8x8 R control point array for S of sensor 0
0x80206573	SNR0_LENC_S_R63	0x20	RW	Bit[7:0]: R63 of 8x8 R control point array for S of sensor 0
0x80206574	SNR0_LENC_S_R64	0x20	RW	Bit[7:0]: R64 of 8x8 R control point array for S of sensor 0
0x80206575	SNR0_LENC_S_R65	0x20	RW	Bit[7:0]: R65 of 8x8 R control point array for S of sensor 0
0x80206576	SNR0_LENC_S_R66	0x20	RW	Bit[7:0]: R66 of 8x8 R control point array for S of sensor 0
0x80206577	SNR0_LENC_S_R67	0x20	RW	Bit[7:0]: R67 of 8x8 R control point array for S of sensor 0
0x80206578	SNR0_LENC_S_R70	0x20	RW	Bit[7:0]: R70 of 8x8 R control point array for S of sensor 0
0x80206579	SNR0_LENC_S_R71	0x20	RW	Bit[7:0]: R71 of 8x8 R control point array for S of sensor 0
0x8020657A	SNR0_LENC_S_R72	0x20	RW	Bit[7:0]: R72 of 8x8 R control point array for S of sensor 0
0x8020657B	SNR0_LENC_S_R73	0x20	RW	Bit[7:0]: R73 of 8x8 R control point array for S of sensor 0
0x8020657C	SNR0_LENC_S_R74	0x20	RW	Bit[7:0]: R74 of 8x8 R control point array for S of sensor 0
0x8020657D	SNR0_LENC_S_R75	0x20	RW	Bit[7:0]: R75 of 8x8 R control point array for S of sensor 0
0x8020657E	SNR0_LENC_S_R76	0x20	RW	Bit[7:0]: R76 of 8x8 R control point array for S of sensor 0
0x8020657F	SNR0_LENC_S_R77	0x20	RW	Bit[7:0]: R77 of 8x8 R control point array for S of sensor 0
0x80206580	SNR1_LENC_LV_G00	0x00	RW	Bit[7:0]: G00 of 8x8 G control point array for L/VS of sensor 1
0x80206581	SNR1_LENC_LV_G01	0x00	RW	Bit[7:0]: G01 of 8x8 G control point array for L/VS of sensor 1
0x80206582	SNR1_LENC_LV_G02	0x00	RW	Bit[7:0]: G02 of 8x8 G control point array for L/VS of sensor 1
0x80206583	SNR1_LENC_LV_G03	0x00	RW	Bit[7:0]: G03 of 8x8 G control point array for L/VS of sensor 1
0x80206584	SNR1_LENC_LV_G04	0x00	RW	Bit[7:0]: G04 of 8x8 G control point array for L/VS of sensor 1

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table 3-2 LENC registers (sheet 22 of 41)

address	register name	default value	R/W	description
0x80206585	SNR1_LENC_LV_G05	0x00	RW	Bit[7:0]: G05 of 8x8 G control point array for L/VS of sensor 1
0x80206586	SNR1_LENC_LV_G06	0x00	RW	Bit[7:0]: G06 of 8x8 G control point array for L/VS of sensor 1
0x80206587	SNR1_LENC_LV_G07	0x00	RW	Bit[7:0]: G07 of 8x8 G control point array for L/VS of sensor 1
0x80206588	SNR1_LENC_LV_G10	0x00	RW	Bit[7:0]: G10 of 8x8 G control point array for L/VS of sensor 1
0x80206589	SNR1_LENC_LV_G11	0x00	RW	Bit[7:0]: G11 of 8x8 G control point array for L/VS of sensor 1
0x8020658A	SNR1_LENC_LV_G12	0x00	RW	Bit[7:0]: G12 of 8x8 G control point array for L/VS of sensor 1
0x8020658B	SNR1_LENC_LV_G13	0x00	RW	Bit[7:0]: G13 of 8x8 G control point array for L/VS of sensor 1
0x8020658C	SNR1_LENC_LV_G14	0x00	RW	Bit[7:0]: G14 of 8x8 G control point array for L/VS of sensor 1
0x8020658D	SNR1_LENC_LV_G15	0x00	RW	Bit[7:0]: G15 of 8x8 G control point array for L/VS of sensor 1
0x8020658E	SNR1_LENC_LV_G16	0x00	RW	Bit[7:0]: G16 of 8x8 G control point array for L/VS of sensor 1
0x8020658F	SNR1_LENC_LV_G17	0x00	RW	Bit[7:0]: G17 of 8x8 G control point array for L/VS of sensor 1
0x80206590	SNR1_LENC_LV_G20	0x00	RW	Bit[7:0]: G20 of 8x8 G control point array for L/VS of sensor 1
0x80206591	SNR1_LENC_LV_G21	0x00	RW	Bit[7:0]: G21 of 8x8 G control point array for L/VS of sensor 1
0x80206592	SNR1_LENC_LV_G22	0x00	RW	Bit[7:0]: G22 of 8x8 G control point array for L/VS of sensor 1
0x80206593	SNR1_LENC_LV_G23	0x00	RW	Bit[7:0]: G23 of 8x8 G control point array for L/VS of sensor 1
0x80206594	SNR1_LENC_LV_G24	0x00	RW	Bit[7:0]: G24 of 8x8 G control point array for L/VS of sensor 1
0x80206595	SNR1_LENC_LV_G25	0x00	RW	Bit[7:0]: G25 of 8x8 G control point array for L/VS of sensor 1
0x80206596	SNR1_LENC_LV_G26	0x00	RW	Bit[7:0]: G26 of 8x8 G control point array for L/VS of sensor 1
0x80206597	SNR1_LENC_LV_G27	0x00	RW	Bit[7:0]: G27 of 8x8 G control point array for L/VS of sensor 1

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table 3-2 LENC registers (sheet 23 of 41)

address	register name	default value	R/W	description
0x80206598	SNR1_LENC_LV_G30	0x00	RW	Bit[7:0]: G30 of 8x8 G control point array for L/VS of sensor 1
0x80206599	SNR1_LENC_LV_G31	0x00	RW	Bit[7:0]: G31 of 8x8 G control point array for L/VS of sensor 1
0x8020659A	SNR1_LENC_LV_G32	0x00	RW	Bit[7:0]: G32 of 8x8 G control point array for L/VS of sensor 1
0x8020659B	SNR1_LENC_LV_G33	0x00	RW	Bit[7:0]: G33 of 8x8 G control point array for L/VS of sensor 1
0x8020659C	SNR1_LENC_LV_G34	0x00	RW	Bit[7:0]: G34 of 8x8 G control point array for L/VS of sensor 1
0x8020659D	SNR1_LENC_LV_G35	0x00	RW	Bit[7:0]: G35 of 8x8 G control point array for L/VS of sensor 1
0x8020659E	SNR1_LENC_LV_G36	0x00	RW	Bit[7:0]: G36 of 8x8 G control point array for L/VS of sensor 1
0x8020659F	SNR1_LENC_LV_G37	0x00	RW	Bit[7:0]: G37 of 8x8 G control point array for L/VS of sensor 1
0x802065A0	SNR1_LENC_LV_G40	0x00	RW	Bit[7:0]: G40 of 8x8 G control point array for L/VS of sensor 1
0x802065A1	SNR1_LENC_LV_G41	0x00	RW	Bit[7:0]: G41 of 8x8 G control point array for L/VS of sensor 1
0x802065A2	SNR1_LENC_LV_G42	0x00	RW	Bit[7:0]: G42 of 8x8 G control point array for L/VS of sensor 1
0x802065A3	SNR1_LENC_LV_G43	0x00	RW	Bit[7:0]: G43 of 8x8 G control point array for L/VS of sensor 1
0x802065A4	SNR1_LENC_LV_G44	0x00	RW	Bit[7:0]: G44 of 8x8 G control point array for L/VS of sensor 1
0x802065A5	SNR1_LENC_LV_G45	0x00	RW	Bit[7:0]: G45 of 8x8 G control point array for L/VS of sensor 1
0x802065A6	SNR1_LENC_LV_G46	0x00	RW	Bit[7:0]: G46 of 8x8 G control point array for L/VS of sensor 1
0x802065A7	SNR1_LENC_LV_G47	0x00	RW	Bit[7:0]: G47 of 8x8 G control point array for L/VS of sensor 1
0x802065A8	SNR1_LENC_LV_G50	0x00	RW	Bit[7:0]: G50 of 8x8 G control point array for L/VS of sensor 1
0x802065A9	SNR1_LENC_LV_G51	0x00	RW	Bit[7:0]: G51 of 8x8 G control point array for L/VS of sensor 1
0x802065AA	SNR1_LENC_LV_G52	0x00	RW	Bit[7:0]: G52 of 8x8 G control point array for L/VS of sensor 1

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table 3-2 LENC registers (sheet 24 of 41)

address	register name	default value	R/W	description
0x802065AB	SNR1_LENC_LV_G53	0x00	RW	Bit[7:0]: G53 of 8x8 G control point array for L/VS of sensor 1
0x802065AC	SNR1_LENC_LV_G54	0x00	RW	Bit[7:0]: G54 of 8x8 G control point array for L/VS of sensor 1
0x802065AD	SNR1_LENC_LV_G55	0x00	RW	Bit[7:0]: G55 of 8x8 G control point array for L/VS of sensor 1
0x802065AE	SNR1_LENC_LV_G56	0x00	RW	Bit[7:0]: G56 of 8x8 G control point array for L/VS of sensor 1
0x802065AF	SNR1_LENC_LV_G57	0x00	RW	Bit[7:0]: G57 of 8x8 G control point array for L/VS of sensor 1
0x802065B0	SNR1_LENC_LV_G60	0x00	RW	Bit[7:0]: G60 of 8x8 G control point array for L/VS of sensor 1
0x802065B1	SNR1_LENC_LV_G61	0x00	RW	Bit[7:0]: G61 of 8x8 G control point array for L/VS of sensor 1
0x802065B2	SNR1_LENC_LV_G62	0x00	RW	Bit[7:0]: G62 of 8x8 G control point array for L/VS of sensor 1
0x802065B3	SNR1_LENC_LV_G63	0x00	RW	Bit[7:0]: G63 of 8x8 G control point array for L/VS of sensor 1
0x802065B4	SNR1_LENC_LV_G64	0x00	RW	Bit[7:0]: G64 of 8x8 G control point array for L/VS of sensor 1
0x802065B5	SNR1_LENC_LV_G65	0x00	RW	Bit[7:0]: G65 of 8x8 G control point array for L/VS of sensor 1
0x802065B6	SNR1_LENC_LV_G66	0x00	RW	Bit[7:0]: G66 of 8x8 G control point array for L/VS of sensor 1
0x802065B7	SNR1_LENC_LV_G67	0x00	RW	Bit[7:0]: G67 of 8x8 G control point array for L/VS of sensor 1
0x802065B8	SNR1_LENC_LV_G70	0x00	RW	Bit[7:0]: G70 of 8x8 G control point array for L/VS of sensor 1
0x802065B9	SNR1_LENC_LV_G71	0x00	RW	Bit[7:0]: G71 of 8x8 G control point array for L/VS of sensor 1
0x802065BA	SNR1_LENC_LV_G72	0x00	RW	Bit[7:0]: G72 of 8x8 G control point array for L/VS of sensor 1
0x802065BB	SNR1_LENC_LV_G73	0x00	RW	Bit[7:0]: G73 of 8x8 G control point array for L/VS of sensor 1
0x802065BC	SNR1_LENC_LV_G74	0x00	RW	Bit[7:0]: G74 of 8x8 G control point array for L/VS of sensor 1
0x802065BD	SNR1_LENC_LV_G75	0x00	RW	Bit[7:0]: G75 of 8x8 G control point array for L/VS of sensor 1

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table 3-2 LENC registers (sheet 25 of 41)

address	register name	default value	R/W	description
0x802065BE	SNR1_LENC_LV_G76	0x00	RW	Bit[7:0]: G76 of 8x8 G control point array for L/VS of sensor 1
0x802065BF	SNR1_LENC_LV_G77	0x00	RW	Bit[7:0]: G77 of 8x8 G control point array for L/VS of sensor 1
0x802065C0	SNR1_LENC_LV_B00	0x20	RW	Bit[7:0]: B00 of 8x8 B control point array for L/VS of sensor 1
0x802065C1	SNR1_LENC_LV_B01	0x20	RW	Bit[7:0]: B01 of 8x8 B control point array for L/VS of sensor 1
0x802065C2	SNR1_LENC_LV_B02	0x20	RW	Bit[7:0]: B02 of 8x8 B control point array for L/VS of sensor 1
0x802065C3	SNR1_LENC_LV_B03	0x20	RW	Bit[7:0]: B03 of 8x8 B control point array for L/VS of sensor 1
0x802065C4	SNR1_LENC_LV_B04	0x20	RW	Bit[7:0]: B04 of 8x8 B control point array for L/VS of sensor 1
0x802065C5	SNR1_LENC_LV_B05	0x20	RW	Bit[7:0]: B05 of 8x8 B control point array for L/VS of sensor 1
0x802065C6	SNR1_LENC_LV_B06	0x20	RW	Bit[7:0]: B06 of 8x8 B control point array for L/VS of sensor 1
0x802065C7	SNR1_LENC_LV_B07	0x20	RW	Bit[7:0]: B07 of 8x8 B control point array for L/VS of sensor 1
0x802065C8	SNR1_LENC_LV_B10	0x20	RW	Bit[7:0]: B10 of 8x8 B control point array for L/VS of sensor 1
0x802065C9	SNR1_LENC_LV_B11	0x20	RW	Bit[7:0]: B11 of 8x8 B control point array for L/VS of sensor 1
0x802065CA	SNR1_LENC_LV_B12	0x20	RW	Bit[7:0]: B12 of 8x8 B control point array for L/VS of sensor 1
0x802065CB	SNR1_LENC_LV_B13	0x20	RW	Bit[7:0]: B13 of 8x8 B control point array for L/VS of sensor 1
0x802065CC	SNR1_LENC_LV_B14	0x20	RW	Bit[7:0]: B14 of 8x8 B control point array for L/VS of sensor 1
0x802065CD	SNR1_LENC_LV_B15	0x20	RW	Bit[7:0]: B15 of 8x8 B control point array for L/VS of sensor 1
0x802065CE	SNR1_LENC_LV_B16	0x20	RW	Bit[7:0]: B16 of 8x8 B control point array for L/VS of sensor 1
0x802065CF	SNR1_LENC_LV_B17	0x20	RW	Bit[7:0]: B17 of 8x8 B control point array for L/VS of sensor 1
0x802065D0	SNR1_LENC_LV_B20	0x20	RW	Bit[7:0]: B20 of 8x8 B control point array for L/VS of sensor 1

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table 3-2 LENC registers (sheet 26 of 41)

address	register name	default value	R/W	description
0x802065D1	SNR1_LENC_LV_B21	0x20	RW	Bit[7:0]: B21 of 8x8 B control point array for L/VS of sensor 1
0x802065D2	SNR1_LENC_LV_B22	0x20	RW	Bit[7:0]: B22 of 8x8 B control point array for L/VS of sensor 1
0x802065D3	SNR1_LENC_LV_B23	0x20	RW	Bit[7:0]: B23 of 8x8 B control point array for L/VS of sensor 1
0x802065D4	SNR1_LENC_LV_B24	0x20	RW	Bit[7:0]: B24 of 8x8 B control point array for L/VS of sensor 1
0x802065D5	SNR1_LENC_LV_B25	0x20	RW	Bit[7:0]: B25 of 8x8 B control point array for L/VS of sensor 1
0x802065D6	SNR1_LENC_LV_B26	0x20	RW	Bit[7:0]: B26 of 8x8 B control point array for L/VS of sensor 1
0x802065D7	SNR1_LENC_LV_B27	0x20	RW	Bit[7:0]: B27 of 8x8 B control point array for L/VS of sensor 1
0x802065D8	SNR1_LENC_LV_B30	0x20	RW	Bit[7:0]: B30 of 8x8 B control point array for L/VS of sensor 1
0x802065D9	SNR1_LENC_LV_B31	0x20	RW	Bit[7:0]: B31 of 8x8 B control point array for L/VS of sensor 1
0x802065DA	SNR1_LENC_LV_B32	0x20	RW	Bit[7:0]: B32 of 8x8 B control point array for L/VS of sensor 1
0x802065DB	SNR1_LENC_LV_B33	0x20	RW	Bit[7:0]: B33 of 8x8 B control point array for L/VS of sensor 1
0x802065DC	SNR1_LENC_LV_B34	0x20	RW	Bit[7:0]: B34 of 8x8 B control point array for L/VS of sensor 1
0x802065DD	SNR1_LENC_LV_B35	0x20	RW	Bit[7:0]: B35 of 8x8 B control point array for L/VS of sensor 1
0x802065DE	SNR1_LENC_LV_B36	0x20	RW	Bit[7:0]: B36 of 8x8 B control point array for L/VS of sensor 1
0x802065DF	SNR1_LENC_LV_B37	0x20	RW	Bit[7:0]: B37 of 8x8 B control point array for L/VS of sensor 1
0x802065E0	SNR1_LENC_LV_B40	0x20	RW	Bit[7:0]: B40 of 8x8 B control point array for L/VS of sensor 1
0x802065E1	SNR1_LENC_LV_B41	0x20	RW	Bit[7:0]: B41 of 8x8 B control point array for L/VS of sensor 1
0x802065E2	SNR1_LENC_LV_B42	0x20	RW	Bit[7:0]: B42 of 8x8 B control point array for L/VS of sensor 1
0x802065E3	SNR1_LENC_LV_B43	0x20	RW	Bit[7:0]: B43 of 8x8 B control point array for L/VS of sensor 1

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table 3-2 LENC registers (sheet 27 of 41)

address	register name	default value	R/W	description
0x802065E4	SNR1_LENC_LV_B44	0x20	RW	Bit[7:0]: B44 of 8x8 B control point array for L/VS of sensor 1
0x802065E5	SNR1_LENC_LV_B45	0x20	RW	Bit[7:0]: B45 of 8x8 B control point array for L/VS of sensor 1
0x802065E6	SNR1_LENC_LV_B46	0x20	RW	Bit[7:0]: B46 of 8x8 B control point array for L/VS of sensor 1
0x802065E7	SNR1_LENC_LV_B47	0x20	RW	Bit[7:0]: B47 of 8x8 B control point array for L/VS of sensor 1
0x802065E8	SNR1_LENC_LV_B50	0x20	RW	Bit[7:0]: B50 of 8x8 B control point array for L/VS of sensor 1
0x802065E9	SNR1_LENC_LV_B51	0x20	RW	Bit[7:0]: B51 of 8x8 B control point array for L/VS of sensor 1
0x802065EA	SNR1_LENC_LV_B52	0x20	RW	Bit[7:0]: B52 of 8x8 B control point array for L/VS of sensor 1
0x802065EB	SNR1_LENC_LV_B53	0x20	RW	Bit[7:0]: B53 of 8x8 B control point array for L/VS of sensor 1
0x802065EC	SNR1_LENC_LV_B54	0x20	RW	Bit[7:0]: B54 of 8x8 B control point array for L/VS of sensor 1
0x802065ED	SNR1_LENC_LV_B55	0x20	RW	Bit[7:0]: B55 of 8x8 B control point array for L/VS of sensor 1
0x802065EE	SNR1_LENC_LV_B56	0x20	RW	Bit[7:0]: B56 of 8x8 B control point array for L/VS of sensor 1
0x802065EF	SNR1_LENC_LV_B57	0x20	RW	Bit[7:0]: B57 of 8x8 B control point array for L/VS of sensor 1
0x802065F0	SNR1_LENC_LV_B60	0x20	RW	Bit[7:0]: B60 of 8x8 B control point array for L/VS of sensor 1
0x802065F1	SNR1_LENC_LV_B61	0x20	RW	Bit[7:0]: B61 of 8x8 B control point array for L/VS of sensor 1
0x802065F2	SNR1_LENC_LV_B62	0x20	RW	Bit[7:0]: B62 of 8x8 B control point array for L/VS of sensor 1
0x802065F3	SNR1_LENC_LV_B63	0x20	RW	Bit[7:0]: B63 of 8x8 B control point array for L/VS of sensor 1
0x802065F4	SNR1_LENC_LV_B64	0x20	RW	Bit[7:0]: B64 of 8x8 B control point array for L/VS of sensor 1
0x802065F5	SNR1_LENC_LV_B65	0x20	RW	Bit[7:0]: B65 of 8x8 B control point array for L/VS of sensor 1
0x802065F6	SNR1_LENC_LV_B66	0x20	RW	Bit[7:0]: B66 of 8x8 B control point array for L/VS of sensor 1

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table 3-2 LENC registers (sheet 28 of 41)

address	register name	default value	R/W	description
0x802065F7	SNR1_LENC_LV_B67	0x20	RW	Bit[7:0]: B67 of 8x8 B control point array for L/VS of sensor 1
0x802065F8	SNR1_LENC_LV_B70	0x20	RW	Bit[7:0]: B70 of 8x8 B control point array for L/VS of sensor 1
0x802065F9	SNR1_LENC_LV_B71	0x20	RW	Bit[7:0]: B71 of 8x8 B control point array for L/VS of sensor 1
0x802065FA	SNR1_LENC_LV_B72	0x20	RW	Bit[7:0]: B72 of 8x8 B control point array for L/VS of sensor 1
0x802065FB	SNR1_LENC_LV_B73	0x20	RW	Bit[7:0]: B73 of 8x8 B control point array for L/VS of sensor 1
0x802065FC	SNR1_LENC_LV_B74	0x20	RW	Bit[7:0]: B74 of 8x8 B control point array for L/VS of sensor 1
0x802065FD	SNR1_LENC_LV_B75	0x20	RW	Bit[7:0]: B75 of 8x8 B control point array for L/VS of sensor 1
0x802065FE	SNR1_LENC_LV_B76	0x20	RW	Bit[7:0]: B76 of 8x8 B control point array for L/VS of sensor 1
0x802065FF	SNR1_LENC_LV_B77	0x20	RW	Bit[7:0]: B77 of 8x8 B control point array for L/VS of sensor 1
0x80206600	SNR1_LENC_LV_R00	0x20	RW	Bit[7:0]: R00 of 8x8 R control point array for L/VS of sensor 1
0x80206601	SNR1_LENC_LV_R01	0x20	RW	Bit[7:0]: R01 of 8x8 R control point array for L/VS of sensor 1
0x80206602	SNR1_LENC_LV_R02	0x20	RW	Bit[7:0]: R02 of 8x8 R control point array for L/VS of sensor 1
0x80206603	SNR1_LENC_LV_R03	0x20	RW	Bit[7:0]: R03 of 8x8 R control point array for L/VS of sensor 1
0x80206604	SNR1_LENC_LV_R04	0x20	RW	Bit[7:0]: R04 of 8x8 R control point array for L/VS of sensor 1
0x80206605	SNR1_LENC_LV_R05	0x20	RW	Bit[7:0]: R05 of 8x8 R control point array for L/VS of sensor 1
0x80206606	SNR1_LENC_LV_R06	0x20	RW	Bit[7:0]: R06 of 8x8 R control point array for L/VS of sensor 1
0x80206607	SNR1_LENC_LV_R07	0x20	RW	Bit[7:0]: R07 of 8x8 R control point array for L/VS of sensor 1
0x80206608	SNR1_LENC_LV_R10	0x20	RW	Bit[7:0]: R10 of 8x8 R control point array for L/VS of sensor 1
0x80206609	SNR1_LENC_LV_R11	0x20	RW	Bit[7:0]: R11 of 8x8 R control point array for L/VS of sensor 1

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table 3-2 LENC registers (sheet 29 of 41)

address	register name	default value	R/W	description
0x8020660A	SNR1_LENC_LV_R12	0x20	RW	Bit[7:0]: R12 of 8x8 R control point array for L/VS of sensor 1
0x8020660B	SNR1_LENC_LV_R13	0x20	RW	Bit[7:0]: R13 of 8x8 R control point array for L/VS of sensor 1
0x8020660C	SNR1_LENC_LV_R14	0x20	RW	Bit[7:0]: R14 of 8x8 R control point array for L/VS of sensor 1
0x8020660D	SNR1_LENC_LV_R15	0x20	RW	Bit[7:0]: R15 of 8x8 R control point array for L/VS of sensor 1
0x8020660E	SNR1_LENC_LV_R16	0x20	RW	Bit[7:0]: R16 of 8x8 R control point array for L/VS of sensor 1
0x8020660F	SNR1_LENC_LV_R17	0x20	RW	Bit[7:0]: R17 of 8x8 R control point array for L/VS of sensor 1
0x80206610	SNR1_LENC_LV_R20	0x20	RW	Bit[7:0]: R20 of 8x8 R control point array for L/VS of sensor 1
0x80206611	SNR1_LENC_LV_R21	0x20	RW	Bit[7:0]: R21 of 8x8 R control point array for L/VS of sensor 1
0x80206612	SNR1_LENC_LV_R22	0x20	RW	Bit[7:0]: R22 of 8x8 R control point array for L/VS of sensor 1
0x80206613	SNR1_LENC_LV_R23	0x20	RW	Bit[7:0]: R23 of 8x8 R control point array for L/VS of sensor 1
0x80206614	SNR1_LENC_LV_R24	0x20	RW	Bit[7:0]: R24 of 8x8 R control point array for L/VS of sensor 1
0x80206615	SNR1_LENC_LV_R25	0x20	RW	Bit[7:0]: R25 of 8x8 R control point array for L/VS of sensor 1
0x80206616	SNR1_LENC_LV_R26	0x20	RW	Bit[7:0]: R26 of 8x8 R control point array for L/VS of sensor 1
0x80206617	SNR1_LENC_LV_R27	0x20	RW	Bit[7:0]: R27 of 8x8 R control point array for L/VS of sensor 1
0x80206618	SNR1_LENC_LV_R30	0x20	RW	Bit[7:0]: R30 of 8x8 R control point array for L/VS of sensor 1
0x80206619	SNR1_LENC_LV_R31	0x20	RW	Bit[7:0]: R31 of 8x8 R control point array for L/VS of sensor 1
0x8020661A	SNR1_LENC_LV_R32	0x20	RW	Bit[7:0]: R32 of 8x8 R control point array for L/VS of sensor 1
0x8020661B	SNR1_LENC_LV_R33	0x20	RW	Bit[7:0]: R33 of 8x8 R control point array for L/VS of sensor 1
0x8020661C	SNR1_LENC_LV_R34	0x20	RW	Bit[7:0]: R34 of 8x8 R control point array for L/VS of sensor 1

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table 3-2 LENC registers (sheet 30 of 41)

address	register name	default value	R/W	description
0x8020661D	SNR1_LENC_LV_R35	0x20	RW	Bit[7:0]: R35 of 8x8 R control point array for L/VS of sensor 1
0x8020661E	SNR1_LENC_LV_R36	0x20	RW	Bit[7:0]: R36 of 8x8 R control point array for L/VS of sensor 1
0x8020661F	SNR1_LENC_LV_R37	0x20	RW	Bit[7:0]: R37 of 8x8 R control point array for L/VS of sensor 1
0x80206620	SNR1_LENC_LV_R40	0x20	RW	Bit[7:0]: R40 of 8x8 R control point array for L/VS of sensor 1
0x80206621	SNR1_LENC_LV_R41	0x20	RW	Bit[7:0]: R41 of 8x8 R control point array for L/VS of sensor 1
0x80206622	SNR1_LENC_LV_R42	0x20	RW	Bit[7:0]: R42 of 8x8 R control point array for L/VS of sensor 1
0x80206623	SNR1_LENC_LV_R43	0x20	RW	Bit[7:0]: R43 of 8x8 R control point array for L/VS of sensor 1
0x80206624	SNR1_LENC_LV_R44	0x20	RW	Bit[7:0]: R44 of 8x8 R control point array for L/VS of sensor 1
0x80206625	SNR1_LENC_LV_R45	0x20	RW	Bit[7:0]: R45 of 8x8 R control point array for L/VS of sensor 1
0x80206626	SNR1_LENC_LV_R46	0x20	RW	Bit[7:0]: R46 of 8x8 R control point array for L/VS of sensor 1
0x80206627	SNR1_LENC_LV_R47	0x20	RW	Bit[7:0]: R47 of 8x8 R control point array for L/VS of sensor 1
0x80206628	SNR1_LENC_LV_R50	0x20	RW	Bit[7:0]: R50 of 8x8 R control point array for L/VS of sensor 1
0x80206629	SNR1_LENC_LV_R51	0x20	RW	Bit[7:0]: R51 of 8x8 R control point array for L/VS of sensor 1
0x8020662A	SNR1_LENC_LV_R52	0x20	RW	Bit[7:0]: R52 of 8x8 R control point array for L/VS of sensor 1
0x8020662B	SNR1_LENC_LV_R53	0x20	RW	Bit[7:0]: R53 of 8x8 R control point array for L/VS of sensor 1
0x8020662C	SNR1_LENC_LV_R54	0x20	RW	Bit[7:0]: R54 of 8x8 R control point array for L/VS of sensor 1
0x8020662D	SNR1_LENC_LV_R55	0x20	RW	Bit[7:0]: R55 of 8x8 R control point array for L/VS of sensor 1
0x8020662E	SNR1_LENC_LV_R56	0x20	RW	Bit[7:0]: R56 of 8x8 R control point array for L/VS of sensor 1
0x8020662F	SNR1_LENC_LV_R57	0x20	RW	Bit[7:0]: R57 of 8x8 R control point array for L/VS of sensor 1

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table 3-2 LENC registers (sheet 31 of 41)

address	register name	default value	R/W	description
0x80206630	SNR1_LENC_LV_R60	0x20	RW	Bit[7:0]: R60 of 8x8 R control point array for L/VS of sensor 1
0x80206631	SNR1_LENC_LV_R61	0x20	RW	Bit[7:0]: R61 of 8x8 R control point array for L/VS of sensor 1
0x80206632	SNR1_LENC_LV_R62	0x20	RW	Bit[7:0]: R62 of 8x8 R control point array for L/VS of sensor 1
0x80206633	SNR1_LENC_LV_R63	0x20	RW	Bit[7:0]: R63 of 8x8 R control point array for L/VS of sensor 1
0x80206634	SNR1_LENC_LV_R64	0x20	RW	Bit[7:0]: R64 of 8x8 R control point array for L/VS of sensor 1
0x80206635	SNR1_LENC_LV_R65	0x20	RW	Bit[7:0]: R65 of 8x8 R control point array for L/VS of sensor 1
0x80206636	SNR1_LENC_LV_R66	0x20	RW	Bit[7:0]: R66 of 8x8 R control point array for L/VS of sensor 1
0x80206637	SNR1_LENC_LV_R67	0x20	RW	Bit[7:0]: R67 of 8x8 R control point array for L/VS of sensor 1
0x80206638	SNR1_LENC_LV_R70	0x20	RW	Bit[7:0]: R70 of 8x8 R control point array for L/VS of sensor 1
0x80206639	SNR1_LENC_LV_R71	0x20	RW	Bit[7:0]: R71 of 8x8 R control point array for L/VS of sensor 1
0x8020663A	SNR1_LENC_LV_R72	0x20	RW	Bit[7:0]: R72 of 8x8 R control point array for L/VS of sensor 1
0x8020663B	SNR1_LENC_LV_R73	0x20	RW	Bit[7:0]: R73 of 8x8 R control point array for L/VS of sensor 1
0x8020663C	SNR1_LENC_LV_R74	0x20	RW	Bit[7:0]: R74 of 8x8 R control point array for L/VS of sensor 1
0x8020663D	SNR1_LENC_LV_R75	0x20	RW	Bit[7:0]: R75 of 8x8 R control point array for L/VS of sensor 1
0x8020663E	SNR1_LENC_LV_R76	0x20	RW	Bit[7:0]: R76 of 8x8 R control point array for L/VS of sensor 1
0x8020663F	SNR1_LENC_LV_R77	0x20	RW	Bit[7:0]: R77 of 8x8 R control point array for L/VS of sensor 1
0x80206640	SNR1_LENC_S_G00	0x00	RW	Bit[7:0]: G00 of 8x8 G control point array for S of sensor 1
0x80206641	SNR1_LENC_S_G01	0x00	RW	Bit[7:0]: G01 of 8x8 G control point array for S of sensor 1
0x80206642	SNR1_LENC_S_G02	0x00	RW	Bit[7:0]: G02 of 8x8 G control point array for S of sensor 1

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table 3-2 LENC registers (sheet 32 of 41)

address	register name	default value	R/W	description
0x80206643	SNR1_LENC_S_G03	0x00	RW	Bit[7:0]: G03 of 8x8 G control point array for S of sensor 1
0x80206644	SNR1_LENC_S_G04	0x00	RW	Bit[7:0]: G04 of 8x8 G control point array for S of sensor 1
0x80206645	SNR1_LENC_S_G05	0x00	RW	Bit[7:0]: G05 of 8x8 G control point array for S of sensor 1
0x80206646	SNR1_LENC_S_G06	0x00	RW	Bit[7:0]: G06 of 8x8 G control point array for S of sensor 1
0x80206647	SNR1_LENC_S_G07	0x00	RW	Bit[7:0]: G07 of 8x8 G control point array for S of sensor 1
0x80206648	SNR1_LENC_S_G10	0x00	RW	Bit[7:0]: G10 of 8x8 G control point array for S of sensor 1
0x80206649	SNR1_LENC_S_G11	0x00	RW	Bit[7:0]: G11 of 8x8 G control point array for S of sensor 1
0x8020664A	SNR1_LENC_S_G12	0x00	RW	Bit[7:0]: G12 of 8x8 G control point array for S of sensor 1
0x8020664B	SNR1_LENC_S_G13	0x00	RW	Bit[7:0]: G13 of 8x8 G control point array for S of sensor 1
0x8020664C	SNR1_LENC_S_G14	0x00	RW	Bit[7:0]: G14 of 8x8 G control point array for S of sensor 1
0x8020664D	SNR1_LENC_S_G15	0x00	RW	Bit[7:0]: G15 of 8x8 G control point array for S of sensor 1
0x8020664E	SNR1_LENC_S_G16	0x00	RW	Bit[7:0]: G16 of 8x8 G control point array for S of sensor 1
0x8020664F	SNR1_LENC_S_G17	0x00	RW	Bit[7:0]: G17 of 8x8 G control point array for S of sensor 1
0x80206650	SNR1_LENC_S_G20	0x00	RW	Bit[7:0]: G20 of 8x8 G control point array for S of sensor 1
0x80206651	SNR1_LENC_S_G21	0x00	RW	Bit[7:0]: G21 of 8x8 G control point array for S of sensor 1
0x80206652	SNR1_LENC_S_G22	0x00	RW	Bit[7:0]: G22 of 8x8 G control point array for S of sensor 1
0x80206653	SNR1_LENC_S_G23	0x00	RW	Bit[7:0]: G23 of 8x8 G control point array for S of sensor 1
0x80206654	SNR1_LENC_S_G24	0x00	RW	Bit[7:0]: G24 of 8x8 G control point array for S of sensor 1
0x80206655	SNR1_LENC_S_G25	0x00	RW	Bit[7:0]: G25 of 8x8 G control point array for S of sensor 1

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table 3-2 LENC registers (sheet 33 of 41)

address	register name	default value	R/W	description
0x80206656	SNR1_LENC_S_G26	0x00	RW	Bit[7:0]: G26 of 8x8 G control point array for S of sensor 1
0x80206657	SNR1_LENC_S_G27	0x00	RW	Bit[7:0]: G27 of 8x8 G control point array for S of sensor 1
0x80206658	SNR1_LENC_S_G30	0x00	RW	Bit[7:0]: G30 of 8x8 G control point array for S of sensor 1
0x80206659	SNR1_LENC_S_G31	0x00	RW	Bit[7:0]: G31 of 8x8 G control point array for S of sensor 1
0x8020665A	SNR1_LENC_S_G32	0x00	RW	Bit[7:0]: G32 of 8x8 G control point array for S of sensor 1
0x8020665B	SNR1_LENC_S_G33	0x00	RW	Bit[7:0]: G33 of 8x8 G control point array for S of sensor 1
0x8020665C	SNR1_LENC_S_G34	0x00	RW	Bit[7:0]: G34 of 8x8 G control point array for S of sensor 1
0x8020665D	SNR1_LENC_S_G35	0x00	RW	Bit[7:0]: G35 of 8x8 G control point array for S of sensor 1
0x8020665E	SNR1_LENC_S_G36	0x00	RW	Bit[7:0]: G36 of 8x8 G control point array for S of sensor 1
0x8020665F	SNR1_LENC_S_G37	0x00	RW	Bit[7:0]: G37 of 8x8 G control point array for S of sensor 1
0x80206660	SNR1_LENC_S_G40	0x00	RW	Bit[7:0]: G40 of 8x8 G control point array for S of sensor 1
0x80206661	SNR1_LENC_S_G41	0x00	RW	Bit[7:0]: G41 of 8x8 G control point array for S of sensor 1
0x80206662	SNR1_LENC_S_G42	0x00	RW	Bit[7:0]: G42 of 8x8 G control point array for S of sensor 1
0x80206663	SNR1_LENC_S_G43	0x00	RW	Bit[7:0]: G43 of 8x8 G control point array for S of sensor 1
0x80206664	SNR1_LENC_S_G44	0x00	RW	Bit[7:0]: G44 of 8x8 G control point array for S of sensor 1
0x80206665	SNR1_LENC_S_G45	0x00	RW	Bit[7:0]: G45 of 8x8 G control point array for S of sensor 1
0x80206666	SNR1_LENC_S_G46	0x00	RW	Bit[7:0]: G46 of 8x8 G control point array for S of sensor 1
0x80206667	SNR1_LENC_S_G47	0x00	RW	Bit[7:0]: G47 of 8x8 G control point array for S of sensor 1
0x80206668	SNR1_LENC_S_G50	0x00	RW	Bit[7:0]: G50 of 8x8 G control point array for S of sensor 1

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table 3-2 LENC registers (sheet 34 of 41)

address	register name	default value	R/W	description
0x80206669	SNR1_LENC_S_G51	0x00	RW	Bit[7:0]: G51 of 8x8 G control point array for S of sensor 1
0x8020666A	SNR1_LENC_S_G52	0x00	RW	Bit[7:0]: G52 of 8x8 G control point array for S of sensor 1
0x8020666B	SNR1_LENC_S_G53	0x00	RW	Bit[7:0]: G53 of 8x8 G control point array for S of sensor 1
0x8020666C	SNR1_LENC_S_G54	0x00	RW	Bit[7:0]: G54 of 8x8 G control point array for S of sensor 1
0x8020666D	SNR1_LENC_S_G55	0x00	RW	Bit[7:0]: G55 of 8x8 G control point array for S of sensor 1
0x8020666E	SNR1_LENC_S_G56	0x00	RW	Bit[7:0]: G56 of 8x8 G control point array for S of sensor 1
0x8020666F	SNR1_LENC_S_G57	0x00	RW	Bit[7:0]: G57 of 8x8 G control point array for S of sensor 1
0x80206670	SNR1_LENC_S_G60	0x00	RW	Bit[7:0]: G60 of 8x8 G control point array for S of sensor 1
0x80206671	SNR1_LENC_S_G61	0x00	RW	Bit[7:0]: G61 of 8x8 G control point array for S of sensor 1
0x80206672	SNR1_LENC_S_G62	0x00	RW	Bit[7:0]: G62 of 8x8 G control point array for S of sensor 1
0x80206673	SNR1_LENC_S_G63	0x00	RW	Bit[7:0]: G63 of 8x8 G control point array for S of sensor 1
0x80206674	SNR1_LENC_S_G64	0x00	RW	Bit[7:0]: G64 of 8x8 G control point array for S of sensor 1
0x80206675	SNR1_LENC_S_G65	0x00	RW	Bit[7:0]: G65 of 8x8 G control point array for S of sensor 1
0x80206676	SNR1_LENC_S_G66	0x00	RW	Bit[7:0]: G66 of 8x8 G control point array for S of sensor 1
0x80206677	SNR1_LENC_S_G67	0x00	RW	Bit[7:0]: G67 of 8x8 G control point array for S of sensor 1
0x80206678	SNR1_LENC_S_G70	0x00	RW	Bit[7:0]: G70 of 8x8 G control point array for S of sensor 1
0x80206679	SNR1_LENC_S_G71	0x00	RW	Bit[7:0]: G71 of 8x8 G control point array for S of sensor 1
0x8020667A	SNR1_LENC_S_G72	0x00	RW	Bit[7:0]: G72 of 8x8 G control point array for S of sensor 1
0x8020667B	SNR1_LENC_S_G73	0x00	RW	Bit[7:0]: G73 of 8x8 G control point array for S of sensor 1

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table 3-2 LENC registers (sheet 35 of 41)

address	register name	default value	R/W	description
0x8020667C	SNR1_LENC_S_G74	0x00	RW	Bit[7:0]: G74 of 8x8 G control point array for S of sensor 1
0x8020667D	SNR1_LENC_S_G75	0x00	RW	Bit[7:0]: G75 of 8x8 G control point array for S of sensor 1
0x8020667E	SNR1_LENC_S_G76	0x00	RW	Bit[7:0]: G76 of 8x8 G control point array for S of sensor 1
0x8020667F	SNR1_LENC_S_G77	0x00	RW	Bit[7:0]: G77 of 8x8 G control point array for S of sensor 1
0x80206680	SNR1_LENC_S_B00	0x20	RW	Bit[7:0]: B00 of 8x8 B control point array for S of sensor 1
0x80206681	SNR1_LENC_S_B01	0x20	RW	Bit[7:0]: B01 of 8x8 B control point array for S of sensor 1
0x80206682	SNR1_LENC_S_B02	0x20	RW	Bit[7:0]: B02 of 8x8 B control point array for S of sensor 1
0x80206683	SNR1_LENC_S_B03	0x20	RW	Bit[7:0]: B03 of 8x8 B control point array for S of sensor 1
0x80206684	SNR1_LENC_S_B04	0x20	RW	Bit[7:0]: B04 of 8x8 B control point array for S of sensor 1
0x80206685	SNR1_LENC_S_B05	0x20	RW	Bit[7:0]: B05 of 8x8 B control point array for S of sensor 1
0x80206686	SNR1_LENC_S_B06	0x20	RW	Bit[7:0]: B06 of 8x8 B control point array for S of sensor 1
0x80206687	SNR1_LENC_S_B07	0x20	RW	Bit[7:0]: B07 of 8x8 B control point array for S of sensor 1
0x80206688	SNR1_LENC_S_B10	0x20	RW	Bit[7:0]: B10 of 8x8 B control point array for S of sensor 1
0x80206689	SNR1_LENC_S_B11	0x20	RW	Bit[7:0]: B11 of 8x8 B control point array for S of sensor 1
0x8020668A	SNR1_LENC_S_B12	0x20	RW	Bit[7:0]: B12 of 8x8 B control point array for S of sensor 1
0x8020668B	SNR1_LENC_S_B13	0x20	RW	Bit[7:0]: B13 of 8x8 B control point array for S of sensor 1
0x8020668C	SNR1_LENC_S_B14	0x20	RW	Bit[7:0]: B14 of 8x8 B control point array for S of sensor 1
0x8020668D	SNR1_LENC_S_B15	0x20	RW	Bit[7:0]: B15 of 8x8 B control point array for S of sensor 1
0x8020668E	SNR1_LENC_S_B16	0x20	RW	Bit[7:0]: B16 of 8x8 B control point array for S of sensor 1

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table 3-2 LENC registers (sheet 36 of 41)

address	register name	default value	R/W	description
0x8020668F	SNR1_LENC_S_B17	0x20	RW	Bit[7:0]: B17 of 8x8 B control point array for S of sensor 1
0x80206690	SNR1_LENC_S_B20	0x20	RW	Bit[7:0]: B20 of 8x8 B control point array for S of sensor 1
0x80206691	SNR1_LENC_S_B21	0x20	RW	Bit[7:0]: B21 of 8x8 B control point array for S of sensor 1
0x80206692	SNR1_LENC_S_B22	0x20	RW	Bit[7:0]: B22 of 8x8 B control point array for S of sensor 1
0x80206693	SNR1_LENC_S_B23	0x20	RW	Bit[7:0]: B23 of 8x8 B control point array for S of sensor 1
0x80206694	SNR1_LENC_S_B24	0x20	RW	Bit[7:0]: B24 of 8x8 B control point array for S of sensor 1
0x80206695	SNR1_LENC_S_B25	0x20	RW	Bit[7:0]: B25 of 8x8 B control point array for S of sensor 1
0x80206696	SNR1_LENC_S_B26	0x20	RW	Bit[7:0]: B26 of 8x8 B control point array for S of sensor 1
0x80206697	SNR1_LENC_S_B27	0x20	RW	Bit[7:0]: B27 of 8x8 B control point array for S of sensor 1
0x80206698	SNR1_LENC_S_B30	0x20	RW	Bit[7:0]: B30 of 8x8 B control point array for S of sensor 1
0x80206699	SNR1_LENC_S_B31	0x20	RW	Bit[7:0]: B31 of 8x8 B control point array for S of sensor 1
0x8020669A	SNR1_LENC_S_B32	0x20	RW	Bit[7:0]: B32 of 8x8 B control point array for S of sensor 1
0x8020669B	SNR1_LENC_S_B33	0x20	RW	Bit[7:0]: B33 of 8x8 B control point array for S of sensor 1
0x8020669C	SNR1_LENC_S_B34	0x20	RW	Bit[7:0]: B34 of 8x8 B control point array for S of sensor 1
0x8020669D	SNR1_LENC_S_B35	0x20	RW	Bit[7:0]: B35 of 8x8 B control point array for S of sensor 1
0x8020669E	SNR1_LENC_S_B36	0x20	RW	Bit[7:0]: B36 of 8x8 B control point array for S of sensor 1
0x8020669F	SNR1_LENC_S_B37	0x20	RW	Bit[7:0]: B37 of 8x8 B control point array for S of sensor 1
0x802066A0	SNR1_LENC_S_B40	0x20	RW	Bit[7:0]: B40 of 8x8 B control point array for S of sensor 1
0x802066A1	SNR1_LENC_S_B41	0x20	RW	Bit[7:0]: B41 of 8x8 B control point array for S of sensor 1

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table 3-2 LENC registers (sheet 37 of 41)

address	register name	default value	R/W	description
0x802066A2	SNR1_LENC_S_B42	0x20	RW	Bit[7:0]: B42 of 8x8 B control point array for S of sensor 1
0x802066A3	SNR1_LENC_S_B43	0x20	RW	Bit[7:0]: B43 of 8x8 B control point array for S of sensor 1
0x802066A4	SNR1_LENC_S_B44	0x20	RW	Bit[7:0]: B44 of 8x8 B control point array for S of sensor 1
0x802066A5	SNR1_LENC_S_B45	0x20	RW	Bit[7:0]: B45 of 8x8 B control point array for S of sensor 1
0x802066A6	SNR1_LENC_S_B46	0x20	RW	Bit[7:0]: B46 of 8x8 B control point array for S of sensor 1
0x802066A7	SNR1_LENC_S_B47	0x20	RW	Bit[7:0]: B47 of 8x8 B control point array for S of sensor 1
0x802066A8	SNR1_LENC_S_B50	0x20	RW	Bit[7:0]: B50 of 8x8 B control point array for S of sensor 1
0x802066A9	SNR1_LENC_S_B51	0x20	RW	Bit[7:0]: B51 of 8x8 B control point array for S of sensor 1
0x802066AA	SNR1_LENC_S_B52	0x20	RW	Bit[7:0]: B52 of 8x8 B control point array for S of sensor 1
0x802066AB	SNR1_LENC_S_B53	0x20	RW	Bit[7:0]: B53 of 8x8 B control point array for S of sensor 1
0x802066AC	SNR1_LENC_S_B54	0x20	RW	Bit[7:0]: B54 of 8x8 B control point array for S of sensor 1
0x802066AD	SNR1_LENC_S_B55	0x20	RW	Bit[7:0]: B55 of 8x8 B control point array for S of sensor 1
0x802066AE	SNR1_LENC_S_B56	0x20	RW	Bit[7:0]: B56 of 8x8 B control point array for S of sensor 1
0x802066AF	SNR1_LENC_S_B57	0x20	RW	Bit[7:0]: B57 of 8x8 B control point array for S of sensor 1
0x802066B0	SNR1_LENC_S_B60	0x20	RW	Bit[7:0]: B60 of 8x8 B control point array for S of sensor 1
0x802066B1	SNR1_LENC_S_B61	0x20	RW	Bit[7:0]: B61 of 8x8 B control point array for S of sensor 1
0x802066B2	SNR1_LENC_S_B62	0x20	RW	Bit[7:0]: B62 of 8x8 B control point array for S of sensor 1
0x802066B3	SNR1_LENC_S_B63	0x20	RW	Bit[7:0]: B63 of 8x8 B control point array for S of sensor 1
0x802066B4	SNR1_LENC_S_B64	0x20	RW	Bit[7:0]: B64 of 8x8 B control point array for S of sensor 1

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table 3-2 LENC registers (sheet 38 of 41)

address	register name	default value	R/W	description
0x802066B5	SNR1_LENC_S_B65	0x20	RW	Bit[7:0]: B65 of 8x8 B control point array for S of sensor 1
0x802066B6	SNR1_LENC_S_B66	0x20	RW	Bit[7:0]: B66 of 8x8 B control point array for S of sensor 1
0x802066B7	SNR1_LENC_S_B67	0x20	RW	Bit[7:0]: B67 of 8x8 B control point array for S of sensor 1
0x802066B8	SNR1_LENC_S_B70	0x20	RW	Bit[7:0]: B70 of 8x8 B control point array for S of sensor 1
0x802066B9	SNR1_LENC_S_B71	0x20	RW	Bit[7:0]: B71 of 8x8 B control point array for S of sensor 1
0x802066BA	SNR1_LENC_S_B72	0x20	RW	Bit[7:0]: B72 of 8x8 B control point array for S of sensor 1
0x802066BB	SNR1_LENC_S_B73	0x20	RW	Bit[7:0]: B73 of 8x8 B control point array for S of sensor 1
0x802066BC	SNR1_LENC_S_B74	0x20	RW	Bit[7:0]: B74 of 8x8 B control point array for S of sensor 1
0x802066BD	SNR1_LENC_S_B75	0x20	RW	Bit[7:0]: B75 of 8x8 B control point array for S of sensor 1
0x802066BE	SNR1_LENC_S_B76	0x20	RW	Bit[7:0]: B76 of 8x8 B control point array for S of sensor 1
0x802066BF	SNR1_LENC_S_B77	0x20	RW	Bit[7:0]: B77 of 8x8 B control point array for S of sensor 1
0x802066C0	SNR1_LENC_S_R00	0x20	RW	Bit[7:0]: R00 of 8x8 R control point array for S of sensor 1
0x802066C1	SNR1_LENC_S_R01	0x20	RW	Bit[7:0]: R01 of 8x8 R control point array for S of sensor 1
0x802066C2	SNR1_LENC_S_R02	0x20	RW	Bit[7:0]: R02 of 8x8 R control point array for S of sensor 1
0x802066C3	SNR1_LENC_S_R03	0x20	RW	Bit[7:0]: R03 of 8x8 R control point array for S of sensor 1
0x802066C4	SNR1_LENC_S_R04	0x20	RW	Bit[7:0]: R04 of 8x8 R control point array for S of sensor 1
0x802066C5	SNR1_LENC_S_R05	0x20	RW	Bit[7:0]: R05 of 8x8 R control point array for S of sensor 1
0x802066C6	SNR1_LENC_S_R06	0x20	RW	Bit[7:0]: R06 of 8x8 R control point array for S of sensor 1
0x802066C7	SNR1_LENC_S_R07	0x20	RW	Bit[7:0]: R07 of 8x8 R control point array for S of sensor 1

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table 3-2 LENC registers (sheet 39 of 41)

address	register name	default value	R/W	description
0x802066C8	SNR1_LENC_S_R10	0x20	RW	Bit[7:0]: R10 of 8x8 R control point array for S of sensor 1
0x802066C9	SNR1_LENC_S_R11	0x20	RW	Bit[7:0]: R11 of 8x8 R control point array for S of sensor 1
0x802066CA	SNR1_LENC_S_R12	0x20	RW	Bit[7:0]: R12 of 8x8 R control point array for S of sensor 1
0x802066CB	SNR1_LENC_S_R13	0x20	RW	Bit[7:0]: R13 of 8x8 R control point array for S of sensor 1
0x802066CC	SNR1_LENC_S_R14	0x20	RW	Bit[7:0]: R14 of 8x8 R control point array for S of sensor 1
0x802066CD	SNR1_LENC_S_R15	0x20	RW	Bit[7:0]: R15 of 8x8 R control point array for S of sensor 1
0x802066CE	SNR1_LENC_S_R16	0x20	RW	Bit[7:0]: R16 of 8x8 R control point array for S of sensor 1
0x802066CF	SNR1_LENC_S_R17	0x20	RW	Bit[7:0]: R17 of 8x8 R control point array for S of sensor 1
0x802066D0	SNR1_LENC_S_R20	0x20	RW	Bit[7:0]: R20 of 8x8 R control point array for S of sensor 1
0x802066D1	SNR1_LENC_S_R21	0x20	RW	Bit[7:0]: R21 of 8x8 R control point array for S of sensor 1
0x802066D2	SNR1_LENC_S_R22	0x20	RW	Bit[7:0]: R22 of 8x8 R control point array for S of sensor 1
0x802066D3	SNR1_LENC_S_R23	0x20	RW	Bit[7:0]: R23 of 8x8 R control point array for S of sensor 1
0x802066D4	SNR1_LENC_S_R24	0x20	RW	Bit[7:0]: R24 of 8x8 R control point array for S of sensor 1
0x802066D5	SNR1_LENC_S_R25	0x20	RW	Bit[7:0]: R25 of 8x8 R control point array for S of sensor 1
0x802066D6	SNR1_LENC_S_R26	0x20	RW	Bit[7:0]: R26 of 8x8 R control point array for S of sensor 1
0x802066D7	SNR1_LENC_S_R27	0x20	RW	Bit[7:0]: R27 of 8x8 R control point array for S of sensor 1
0x802066D8	SNR1_LENC_S_R30	0x20	RW	Bit[7:0]: R30 of 8x8 R control point array for S of sensor 1
0x802066D9	SNR1_LENC_S_R31	0x20	RW	Bit[7:0]: R31 of 8x8 R control point array for S of sensor 1
0x802066DA	SNR1_LENC_S_R32	0x20	RW	Bit[7:0]: R32 of 8x8 R control point array for S of sensor 1

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table 3-2 LENC registers (sheet 40 of 41)

address	register name	default value	R/W	description
0x802066DB	SNR1_LENC_S_R33	0x20	RW	Bit[7:0]: R33 of 8x8 R control point array for S of sensor 1
0x802066DC	SNR1_LENC_S_R34	0x20	RW	Bit[7:0]: R34 of 8x8 R control point array for S of sensor 1
0x802066DD	SNR1_LENC_S_R35	0x20	RW	Bit[7:0]: R35 of 8x8 R control point array for S of sensor 1
0x802066DE	SNR1_LENC_S_R36	0x20	RW	Bit[7:0]: R36 of 8x8 R control point array for S of sensor 1
0x802066DF	SNR1_LENC_S_R37	0x20	RW	Bit[7:0]: R37 of 8x8 R control point array for S of sensor 1
0x802066E0	SNR1_LENC_S_R40	0x20	RW	Bit[7:0]: R40 of 8x8 R control point array for S of sensor 1
0x802066E1	SNR1_LENC_S_R41	0x20	RW	Bit[7:0]: R41 of 8x8 R control point array for S of sensor 1
0x802066E2	SNR1_LENC_S_R42	0x20	RW	Bit[7:0]: R42 of 8x8 R control point array for S of sensor 1
0x802066E3	SNR1_LENC_S_R43	0x20	RW	Bit[7:0]: R43 of 8x8 R control point array for S of sensor 1
0x802066E4	SNR1_LENC_S_R44	0x20	RW	Bit[7:0]: R44 of 8x8 R control point array for S of sensor 1
0x802066E5	SNR1_LENC_S_R45	0x20	RW	Bit[7:0]: R45 of 8x8 R control point array for S of sensor 1
0x802066E6	SNR1_LENC_S_R46	0x20	RW	Bit[7:0]: R46 of 8x8 R control point array for S of sensor 1
0x802066E7	SNR1_LENC_S_R47	0x20	RW	Bit[7:0]: R47 of 8x8 R control point array for S of sensor 1
0x802066E8	SNR1_LENC_S_R50	0x20	RW	Bit[7:0]: R50 of 8x8 R control point array for S of sensor 1
0x802066E9	SNR1_LENC_S_R51	0x20	RW	Bit[7:0]: R51 of 8x8 R control point array for S of sensor 1
0x802066EA	SNR1_LENC_S_R52	0x20	RW	Bit[7:0]: R52 of 8x8 R control point array for S of sensor 1
0x802066EB	SNR1_LENC_S_R53	0x20	RW	Bit[7:0]: R53 of 8x8 R control point array for S of sensor 1
0x802066EC	SNR1_LENC_S_R54	0x20	RW	Bit[7:0]: R54 of 8x8 R control point array for S of sensor 1
0x802066ED	SNR1_LENC_S_R55	0x20	RW	Bit[7:0]: R55 of 8x8 R control point array for S of sensor 1

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table 3-2 LENC registers (sheet 41 of 41)

address	register name	default value	R/W	description
0x802066EE	SNR1_LENC_S_R56	0x20	RW	Bit[7:0]: R56 of 8x8 R control point array for S of sensor 1
0x802066EF	SNR1_LENC_S_R57	0x20	RW	Bit[7:0]: R57 of 8x8 R control point array for S of sensor 1
0x802066F0	SNR1_LENC_S_R60	0x20	RW	Bit[7:0]: R60 of 8x8 R control point array for S of sensor 1
0x802066F1	SNR1_LENC_S_R61	0x20	RW	Bit[7:0]: R61 of 8x8 R control point array for S of sensor 1
0x802066F2	SNR1_LENC_S_R62	0x20	RW	Bit[7:0]: R62 of 8x8 R control point array for S of sensor 1
0x802066F3	SNR1_LENC_S_R63	0x20	RW	Bit[7:0]: R63 of 8x8 R control point array for S of sensor 1
0x802066F4	SNR1_LENC_S_R64	0x20	RW	Bit[7:0]: R64 of 8x8 R control point array for S of sensor 1
0x802066F5	SNR1_LENC_S_R65	0x20	RW	Bit[7:0]: R65 of 8x8 R control point array for S of sensor 1
0x802066F6	SNR1_LENC_S_R66	0x20	RW	Bit[7:0]: R66 of 8x8 R control point array for S of sensor 1
0x802066F7	SNR1_LENC_S_R67	0x20	RW	Bit[7:0]: R67 of 8x8 R control point array for S of sensor 1
0x802066F8	SNR1_LENC_S_R70	0x20	RW	Bit[7:0]: R70 of 8x8 R control point array for S of sensor 1
0x802066F9	SNR1_LENC_S_R71	0x20	RW	Bit[7:0]: R71 of 8x8 R control point array for S of sensor 1
0x802066FA	SNR1_LENC_S_R72	0x20	RW	Bit[7:0]: R72 of 8x8 R control point array for S of sensor 1
0x802066FB	SNR1_LENC_S_R73	0x20	RW	Bit[7:0]: R73 of 8x8 R control point array for S of sensor 1
0x802066FC	SNR1_LENC_S_R74	0x20	RW	Bit[7:0]: R74 of 8x8 R control point array for S of sensor 1
0x802066FD	SNR1_LENC_S_R75	0x20	RW	Bit[7:0]: R75 of 8x8 R control point array for S of sensor 1
0x802066FE	SNR1_LENC_S_R76	0x20	RW	Bit[7:0]: R76 of 8x8 R control point array for S of sensor 1
0x802066FF	SNR1_LENC_S_R77	0x20	RW	Bit[7:0]: R77 of 8x8 R control point array for S of sensor 1

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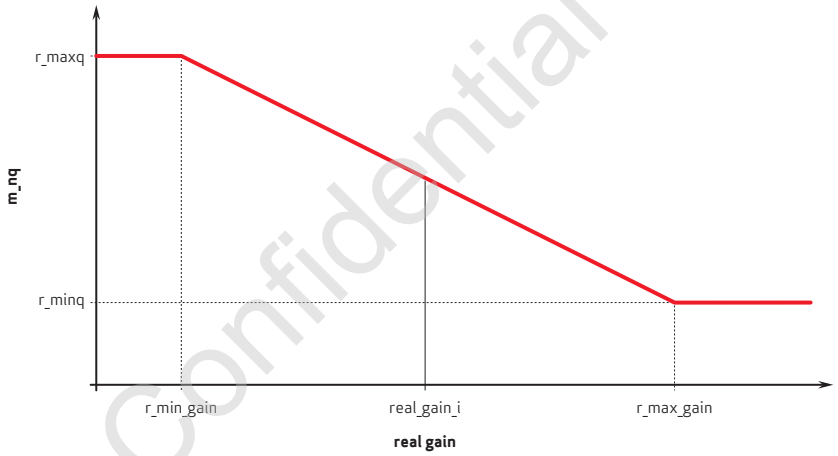
Besides the control point registers and mirror flip flag, H scale and V scale registers 0x80206715~0x8020671C (0x80206739~0x80206740 for the second sensor) must be set for different input sensor array sizes.

- BRHScale = 6<<20×1.0/input_width
- BRVScale = 6<<20×1.0/input_height
- GHScale = 6<<20×1.0/input_width
- GVScale = 6<<19×1.0/input_height

Under dark conditions, the signal-to-noise ratio (SNR) drops off in the corner areas. Noise can be significantly amplified by the lens correction gain and will result in a brighter corner. The OV490 can automatically adjust gain for the pixels to adapt to lighting conditions (m_nQ). This is accomplished by following OV490's real gain.The auto Q function is enabled by registers 0x80206700[0] for L, 0x80206707[0] for S and 0x8020670E[0] for VS.

When scene brightness increases, OV490's real gain decreases towards its minimum (min-gain) and correspondingly the LENC gain increases towards its maximum value (max-q) (see **figure 3-7**). When scene brightness decreases, the sensor analog gain increases towards its maximum (max-gain), and the LENC gain decreases towards its minimum value (min-q).

figure 3-7 lens correction graph



note 1 register settings for r_maxq first sensor: (L) 0x80206706, (S) 0x8020670D, (V) 0x80206714
register settings for r_maxq second sensor: (L) 0x8020672A, (S) 0x80206731, (V) 0x80206738

note 2 register settings for r_minq first sensor: (L) 0x80206705, (S) 0x8020670C, (V) 0x80206713
register settings for r_minq second sensor: (L) 0x80206729, (S) 0x80206730, (V) 0x80206737

note 3 register settings for r_min_gain first sensor: (L) 0x80206703/0x80206704, (S) 0x8020670A/0x8020670B, (V) 0x80206711/0x80206712
register settings for r_min_gain second sensor: (L) 0x80206727/0x80206728, (S) 0x8020672E/0x8020672F, (V) 0x80206735/0x80206736

note 4 register settings for r_max_gain first sensor: (L) 0x80206701/0x80206702, (S) 0x80206708/0x80206709, (V) 0x8020670F/0x80206710
register settings for r_max_gain second sensor: (L) 0x80206725/0x80206726, (S) 0x8020672C/0x8020672D, (V) 0x80206733/0x80206734

490_BDS_3_7

The L/S/VS channels can share the same value of m_nQ calculated by any one of the three channels and can also use the value calculated by themselves separately. The 8x8 control point matrix are, however, independent for L/VS (LPD) and S (SPD) channels, correspondingly.

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LENC control point parameters must be calibrated with a specific tool. Please contact your regional OmniVision FAE for assistance.

table 3-3 LENC scale registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x80206700	SNR0_LENC_CTRL10	0x05	RW	Bit[7:3]: Reserved Bit[2]: Less than 1x gain enable for L of sensor 0 Bit[1]: Add random bits enable for L of sensor 0 Bit[0]: Auto lens switch enable for L of sensor 0
0x80206701	SNR0_MAXGAIN_L_BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensor gain2 for L of sensor 0[11:8]
0x80206702	SNR0_MAXGAIN_L_BYTE0	0x60	RW	Bit[7:0]: m_nSensor gain2 for L of sensor 0[7:0]
0x80206703	SNR0_MINGAIN_L_BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensor gain1 for L of sensor 0[11:8]
0x80206704	SNR0_MINGAIN_L_BYTE0	0x20	RW	Bit[7:0]: m_nSensor gain1 for L of sensor 0[7:0]
0x80206705	SNR0_MINQ_L	0x18	RW	Bit[7]: Reserved Bit[6:0]: Minimum Q for L of sensor 0
0x80206706	SNR0_MAXQ_L	0x40	RW	Bit[7]: Reserved Bit[6:0]: Maximum Q for L of sensor 0
0x80206707	SNR0_LENC_CTRL11	0x05	RW	Bit[7:3]: Reserved Bit[2]: Less than 1x gain enable for S of sensor 0 Bit[1]: Add random bits enable for S of sensor 0 Bit[0]: Auto lens switch enable for S of sensor 0
0x80206708	SNR0_MAXGAIN_S_BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensor gain2 for S of sensor 0[11:8]
0x80206709	SNR0_MAXGAIN_S_BYTE0	0x60	RW	Bit[7:0]: m_nSensor gain2 for S of sensor 0[7:0]
0x8020670A	SNR0_MINGAIN_S_BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensor gain1 for S of sensor 0[11:8]
0x8020670B	SNR0_MINGAIN_S_BYTE0	0x20	RW	Bit[7:0]: m_nSensor gain1 for S of sensor 0[7:0]

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table 3-3 LENC scale registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x8020670C	SNR0_MINQ_S	0x18	RW	Bit[7]: Reserved Bit[6:0]: Minimum Q for S of sensor 0
0x8020670D	SNR0_MAXQ_S	0x40	RW	Bit[7]: Reserved Bit[6:0]: Maximum Q for S of sensor 0
0x8020670E	SNR0_LENC_CTRL12	0x05	RW	Bit[7:3]: Reserved Bit[2]: Less than 1x gain enable for VS of sensor 0 Bit[1]: Add random bits enable for VS of sensor 0 Bit[0]: Auto lens switch enable for VS of sensor 0
0x8020670F	SNR0_MAXGAIN_VS_BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensor gain2 for VS of sensor 0[11:8]
0x80206710	SNR0_MAXGAIN_VS_BYTE0	0x60	RW	Bit[7:0]: m_nSensor gain2 for VS of sensor 0[7:0]
0x80206711	SNR0_MINGAIN_VS_BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensor gain1 for VS of sensor 0[11:8]
0x80206712	SNR0_MINGAIN_VS_BYTE0	0x20	RW	Bit[7:0]: m_nSensor gain1 for VS of sensor 0[7:0]
0x80206713	SNR0_MINQ_VS	0x18	RW	Bit[7]: Reserved Bit[6:0]: Minimum Q for VS of sensor 0
0x80206714	SNR0_MAXQ_VS	0x40	RW	Bit[7]: Reserved Bit[6:0]: Maximum Q for VS of sensor 0
0x80206715	SNR0_BR_HSCALE_BYTE1	0x02	RW	Bit[7:0]: H scale for sensor 0[15:8]
0x80206716	SNR0_BR_HSCALE_BYTE0	0x0A	RW	Bit[7:0]: H scale for sensor 0[7:0]
0x80206717	SNR0_BR_VSCALE_BYTE1	0x02	RW	Bit[7:0]: V scale for sensor 0[15:8]
0x80206718	SNR0_BR_VSCALE_BYTE0	0xF4	RW	Bit[7:0]: V scale for sensor 0[7:0]
0x80206719	SNR0_G_HSCALE_BYTE1	0x02	RW	Bit[7:0]: H scale for sensor 0[15:8]
0x8020671A	SNR0_G_HSCALE_BYTE0	0x0A	RW	Bit[7:0]: H scale for sensor 0[7:0]
0x8020671B	SNR0_G_VSCALE_BYTE1	0x01	RW	Bit[7:0]: V scale for sensor 0[15:8]

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table 3-3 LENC scale registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x8020671C	SNR0_G_VSCALE_BYTE0	0x7A	RW	Bit[7:0]: V scale for sensor 0[7:0]
0x8020671D	SNR0_MQ_OPTION	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 m_nQ option 001: L/S/VS all use m_nQ of VS 010: L/S/VS all use m_nQ of S 100: L/S/VS all use m_nQ of L 111: L/S/VS use their own m_nQ Others: Reserved
0x80206724	SNR1_LENC_CTRL10	0x05	RW	Bit[7:3]: Reserved Bit[2]: Less than 1x gain enable for L of sensor 1 Bit[1]: Add random bits enable for L of sensor 1 Bit[0]: Auto lens switch enable for L of sensor 1
0x80206725	SNR1_MAXGAIN_L_BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensor gain2 for L of sensor 1[11:8]
0x80206726	SNR1_MAXGAIN_L_BYTE0	0x60	RW	Bit[7:0]: m_nSensor gain2 for L of sensor 1[7:0]
0x80206727	SNR1_MINGAIN_L_BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensor gain1 for L of sensor 1[11:8]
0x80206728	SNR1_MINGAIN_L_BYTE0	0x20	RW	Bit[7:0]: m_nSensor gain1 for L of sensor 1[7:0]
0x80206729	SNR1_MINQ_L	0x18	RW	Bit[7]: Reserved Bit[6:0]: Minimum Q for L of sensor 1
0x8020672A	SNR1_MAXQ_L	0x40	RW	Bit[7]: Reserved Bit[6:0]: Maximum Q for L of sensor 1
0x8020672B	SNR1_LENC_CTRL11	0x05	RW	Bit[7:3]: Reserved Bit[2]: Less than 1x gain enable for S of sensor 1 Bit[1]: Add random bits enable for S of sensor 1 Bit[0]: Auto lens switch enable for S of sensor 1

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table 3-3 LENC scale registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x8020672C	SNR1_MAXGAIN_S_ BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensor gain2 for S of sensor 1[11:8]
0x8020672D	SNR1_MAXGAIN_S_ BYTE0	0x60	RW	Bit[7:0]: m_nSensor gain2 for S of sensor 1[7:0]
0x8020672E	SNR1_MINGAIN_S_ BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensor gain1 for S of sensor 1[11:8]
0x8020672F	SNR1_MINGAIN_S_ BYTE0	0x20	RW	Bit[7:0]: m_nSensor gain1 for S of sensor 1[7:0]
0x80206730	SNR1_MINQ_S	0x18	RW	Bit[7]: Reserved Bit[6:0]: Minimum Q for S of sensor 1
0x80206731	SNR1_MAXQ_S	0x40	RW	Bit[7]: Reserved Bit[6:0]: Maximum Q for S of sensor 1
0x80206732	SNR1_LENC_CTRL12	0x05	RW	Bit[7:3]: Reserved Bit[2]: Less than 1x gain enable for VS of sensor 1 Bit[1]: Add random bits enable for VS of sensor 1 Bit[0]: Auto lens switch enable for VS of sensor 1
0x80206733	SNR1_MAXGAIN_VS_ BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensor gain2 for VS of sensor 1[11:8]
0x80206734	SNR1_MAXGAIN_VS_ BYTE0	0x60	RW	Bit[7:0]: m_nSensor gain2 for VS of sensor 1[7:0]
0x80206735	SNR1_MINGAIN_VS_ BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensor gain1 for VS of sensor 1[11:8]
0x80206736	SNR1_MINGAIN_VS_ BYTE0	0x20	RW	Bit[7:0]: m_nSensor gain1 for VS of sensor 1[7:0]
0x80206737	SNR1_MINQ_VS	0x18	RW	Bit[7]: Reserved Bit[6:0]: Minimum Q for VS of sensor 1
0x80206738	SNR1_MAXQ_VS	0x40	RW	Bit[7]: Reserved Bit[6:0]: Maximum Q for VS of sensor 1
0x80206739	SNR1_BR_HSCALE_ BYTE1	0x02	RW	Bit[7:0]: H scale for sensor 1[15:8]
0x8020673A	SNR1_BR_HSCALE_ BYTE0	0x0A	RW	Bit[7:0]: H scale for sensor 1[7:0]

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table 3-3 LENC scale registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x8020673B	SNR1_BR_VSCALE_BYTE1	0x02	RW	Bit[7:0]: V scale for sensor 1[15:8]
0x8020673C	SNR1_BR_VSCALE_BYTE0	0xF4	RW	Bit[7:0]: V scale for sensor 1[7:0]
0x8020673D	SNR1_G_HSCALE_BYTE1	0x02	RW	Bit[7:0]: H scale for sensor 1[15:8]
0x8020673E	SNR1_G_HSCALE_BYTE0	0x0A	RW	Bit[7:0]: H scale for sensor 1[7:0]
0x8020673F	SNR1_G_VSCALE_BYTE1	0x01	RW	Bit[7:0]: V scale for sensor 1[15:8]
0x80206740	SNR1_G_VSCALE_BYTE0	0x7A	RW	Bit[7:0]: V scale for sensor 1[7:0]
0x80206741	SNR1_MQ_OPTION	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 m_nQ option 001: L/S/VS all use m_nQ of VS 010: L/S/VS all use m_nQ of S 100: L/S/VS all use m_nQ of L 111: L/S/VS use their own m_nQ Others: Reserved

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3.8.1 multi LENC function

The OV490 can also support multi LENC function by firmware. It can support a maximum of 3 groups of different LENC settings based on different CT. Generally, three different lens correction parameters can be calibrated under D65/CWF/A. The OV490 will automatically apply lens correction parameters based on the current CT calculated from AWB gain.

CT is defined as: CT = (blue channel AWB gain × 128)/(red channel AWB gain)

The function can be enabled by firmware register 0x85C. If the function is enabled, the OV490 will update the LENC setting to registers 0x80206400~0x802064BF (0x80206580~0x8020663F for the second sensor) for L/VS exposure and 0x802064C0~0x8020657F (0x80206640~0x802066FF for the second sensor) for S exposure based on CT. So these hardware LENC registers cannot be changed successfully if the firmware multi LENC function is enabled.

$$L=\begin{cases} L_{day}, ct \le ct_0 \\ L_{day}+\dfrac{(L_{cwf}-L_{day})(ct-ct_0)}{ct_1-ct_0}, ct_0 < ct \le ct_1 \\ L_{cwf}, ct_1 < ct \le ct_2 \\ L_{cwf}+\dfrac{(L_a-L_{cwf})(ct-ct_2)}{ct_3-ct_2}, ct_2 < ct \le ct_3 \\ L_a, ct_3 < ct \end{cases}$$

note 1 if the current $ct < ct_0$, the LENC correction result will be used in the D65 lenc calibration result

note 2 if $ct_0 <$ the current $ct < ct_1$, the LENC correction result will be used in the interpolation of D65 and CWF LENC calibration results

note 3 if $ct_1 <$ the current $ct < ct_2$, the LENC correction result will be used in the CWFLENC calibration result

note 4 if $ct_2 <$ the current $ct < ct_3$, the LENC correction result will be used in the interpolation of CWF and A LENC calibration results

note 5 if the current $ct > ct_3$, the LENC correction result will be used in the A lenc calibration result

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The registers for multi LENC's three groups of LENC settings are in firmware registers 0x3DC~0x85C.

table 3-4 multi LENC firmware registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x85C	MANUALLENCEN	0x01	RW	Bit[0]: Manual LENC enable 0: multi_lenc enable 1: multi_lenc disable
0x3B2	LENSCTTHRE [0][0]_H	0x00	RW	Bit[7:0]: CT0 for long channel[15:8]
0x3B3	LENSCTTHRE [0][0]_L	0xA0	RW	Bit[7:0]: CT0 for long channel[7:0]
0x3B4	LENSCTTHRE [0][1]_H	0x00	RW	Bit[7:0]: CT1 for long channel[15:8]
0x3B5	LENSCTTHRE [0][1]_L	0xF0	RW	Bit[7:0]: CT1 for long channel[7:0]
0x3B6	LENSCTTHRE [0][2]_H	0x01	RW	Bit[7:0]: CT2 for long channel[15:8]
0x3B7	LENSCTTHRE [0][2]_L	0xB0	RW	Bit[7:0]: CT2 for long channel[7:0]
0x3B8	LENSCTTHRE [0][3]_H	0x01	RW	Bit[7:0]: CT3 for long channel[15:8]
0x3B9	LENSCTTHRE [0][3]_L	0xC0	RW	Bit[7:0]: CT3 for long channel[7:0]
0x3BA	LENSCTTHRE [1][0]_H	0x00	RW	Bit[7:0]: CT0 for short channel[15:8]
0x3BB	LENSCTTHRE [1][0]_L	0xA0	RW	Bit[7:0]: CT0 for short channel[7:0]
0x3BC	LENSCTTHRE [1][1]_H	0x00	RW	Bit[7:0]: CT1 for short channel[15:8]
0x3BD	LENSCTTHRE [1][1]_L	0xF0	RW	Bit[7:0]: CT1 for short channel[7:0]
0x3BE	LENSCTTHRE [1][2]_H	0x01	RW	Bit[7:0]: CT2 for short channel[15:8]
0x3BF	LENSCTTHRE [1][2]_L	0xB0	RW	Bit[7:0]: CT2 for short channel[7:0]
0x3C0	LENSCTTHRE [1][3]_H	0x01	RW	Bit[7:0]: CT3 for short channel[15:8]
0x3C1	LENSCTTHRE [1][3]_L	0xC0	RW	Bit[7:0]: CT3 for short channel[7:0]
0x3C2	LENSCTTHRE [2][0]_H	0x00	RW	Bit[7:0]: CT0 for very short channel[15:8]

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table 3-4 multi LENC firmware registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3C3	LENSCTTHRE [2][0]_L	0xA0	RW	Bit[7:0]: CT0 for very short channel[7:0]
0x3C4	LENSCTTHRE [2][1]_H	0x00	RW	Bit[7:0]: CT1 for very short channel[15:8]
0x3C5	LENSCTTHRE [2][1]_L	0xF0	RW	Bit[7:0]: CT1 for very short channel[7:0]
0x3C6	LENSCTTHRE [2][2]_H	0x01	RW	Bit[7:0]: CT2 for very short channel[15:8]
0x3C7	LENSCTTHRE [2][2]_L	0xB0	RW	Bit[7:0]: CT2 for very short channel[7:0]
0x3C8	LENSCTTHRE [2][3]_H	0x01	RW	Bit[7:0]: CT3 for very short channel [15:8]
0x3C9	LENSCTTHRE [2][3]_L	0xC0	RW	Bit[7:0]: CT3 for very short channel[7:0]
0x3DC	LENSCPARRAY[1]_LVS_D65	0x00	RW	Bit[7:0]: L/VS exposure LENC setting point 1 for D65
0x49B	LENSCPARRAY[192]_LVS_D65	0x00	RW	Bit[7:0]: L/VS exposure LENC setting point 192 for D65
0x49C	LENSCPARRAY[1]_LVS_CWF	0x00	RW	Bit[7:0]: L/VS exposure LENC setting point 1 for CWF
0x55B	LENSCPARRAY[192]_LVS_CWF	0x00	RW	Bit[7:0]: L/VS exposure LENC setting point 192 for CWF
0x55C	LENSCPARRAY[1]_LVS_A	0x00	RW	Bit[7:0]: L/VS exposure LENC setting point 1 for A
0x61B	LENSCPARRAY[192]_LVS_A	0x00	RW	Bit[7:0]: L/VS exposure LENC setting point 192 for A
0x61C	LENSCPARRAY[1]_S_D65	0x00	RW	Bit[7:0]: S exposure LENC setting point 1 for D65
0x6DB	PLENSCPARRAY[192]_S_D65	0x00	RW	Bit[7:0]: S exposure LENC setting point 192 for D65
0x6DC	PLENSCPARRAY[1]_S_CWF	0x00	RW	Bit[7:0]: S exposure LENC setting point 1 for CWF
0x79B	LENSCPARRAY[192]_S_CWF	0x00	RW	Bit[7:0]: S exposure LENC setting point 192 for CWF
0x 79C	LENSCPARRAY[1]_S_A	0x00	RW	Bit[7:0]: S exposure LENC setting point 1 for A
0X85B	LENSCPARRAY[192]_S_A	0x00	RW	Bit[7:0]: S exposure LENC setting point 192 for A

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3.9 auto white balance (AWB)

The next process in the pipeline is auto white balance. The RAW R, G and B values of a gray object vary with the light source spectrum and the pixel QE spectrum response. Light source spectrum is usually described by "color temperature", which is the surface temperature of a black body radiating equivalent spectrum. In the real world, the light color temperature ranges from very low (reddish) to very high (bluish) value. For example, the color temperature of an incandescent lamp is about 2850K, while the color temperature of an overcast day is about 6500K.

To make sure that a gray image is truly gray regardless of the light spectrum, the sensor needs to adjust the gain for each RGB channel according to color temperature. This process is called white balance (WB).

3.9.1 WB gain

The OV490 supports AWB and manual WB. Manual WB can be enabled through manual WB command set. The detailed command set information is described in the OV490 application notes.

In AWB mode, the WB gain value is auto updated by the AWB algorithm. The WB gain to be applied can be always read back from registers 0x80206100~0x80206117 for L/S/VS channel. Registers 0x80206119~0x80206197 are the AWB gain offset for L/S/VS channel.

In manual WB mode, the host can change the WB value manually. The OV490 will use the manual WB gain registers value (firmware 0x7C~0x93) to change the WB gain and these WB gain values will be updated to hardware registers 0x80206100~0x80206117. So for both AWB mode and manual WB mode, the host can determine the applied WB gain value by registers 0x80206100~0x80206117. Refer to the OV490 application notes for the more detailed information on the host commands.

The OV490 can also control AWB gain enable or disable by register 0x80206010[4] (0x80206030[4] for the second sensor). The AWB gain is enabled by default. When it is disabled, all the WB gains will not take effect.

The maximum WB gain is set by firmware registers 0x0C~0x11.

table 3-5 AWB gain control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x80206010	SNR0_ISP_CTRL_0	0xF7	RW	Bit[7]: Sensor 0 simple CIP enable Bit[6]: Sensor 0 HDR DNS enable Bit[5]: Sensor 0 DPC enable Bit[4]: Sensor 0 AWB gain enable Bit[3]: Sensor 0 make virtual long enable Bit[2]: Sensor 0 LENC enable Bit[1]: Sensor 0 digital gain enable Bit[0]: Sensor 0 enable

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table 3-5 AWB gain control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x80206030	SNR1_ISP_CTRL_0	0xF7	RW	Bit[7]: Sensor 1 simple CIP enable Bit[6]: Sensor 1 HDR DNS enable Bit[5]: Sensor 1 DPC enable Bit[4]: Sensor 1 AWB gain enable Bit[3]: Sensor 1 make virtual long enable Bit[2]: Sensor 1 LENC enable Bit[1]: Sensor 1 digital gain enable Bit[0]: Sensor 1 enable flag
0x80206100	SNR0_AWBG_R_ GAIN_L_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 R gain[11:8] for long exposure
0x80206101	SNR0_AWBG_R_ GAIN_L_L	0x00	RW	Bit[7:0]: Sensor 0 R gain[7:0] for long exposure
0x80206102	SNR0_AWBG_GR_ GAIN_L_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 Gr gain[11:8] for long exposure
0x80206103	SNR0_AWBG_GR_ GAIN_L_L	0x00	RW	Bit[7:0]: Sensor 0 Gr gain[7:0] for long exposure
0x80206104	SNR0_AWBG_GB_ GAIN_L_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 Gb gain[11:8] for long exposure
0x80206105	SNR0_AWBG_GB_ GAIN_L_L	0x00	RW	Bit[7:0]: Sensor 0 Gb gain[7:0] for long exposure
0x80206106	SNR0_AWBG_B_ GAIN_L_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 B gain[11:8] for long exposure
0x80206107	SNR0_AWBG_B_ GAIN_L_L	0x00	RW	Bit[7:0]: Sensor 0 B gain[7:0] for long exposure
0x80206108	SNR0_AWBG_R_ GAIN_S_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 R gain[11:8] for short exposure
0x80206109	SNR0_AWBG_R_ GAIN_S_L	0x00	RW	Bit[7:0]: Sensor 0 R gain[7:0] for short exposure
0x8020610A	SNR0_AWBG_GR_ GAIN_S_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 Gr gain[11:8] for short exposure
0x8020610B	SNR0_AWBG_GR_ GAIN_S_L	0x00	RW	Bit[7:0]: Sensor 0 Gr gain[7:0] for short exposure
0x8020610C	SNR0_AWBG_GB_ GAIN_S_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 Gb gain[11:8] for short exposure

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table 3-5 AWB gain control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x8020610D	SNR0_AWBG_GB_GAIN_S_L	0x00	RW	Bit[7:0]: Sensor 0 Gb gain[7:0] for short exposure
0x8020610E	SNR0_AWBG_B_GAIN_S_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 B gain[11:8] for short exposure
0x8020610F	SNR0_AWBG_B_GAIN_S_L	0x00	RW	Bit[7:0]: Sensor 0 B gain[7:0] for short exposure
0x80206110	SNR0_AWBG_R_GAIN_V_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 R gain[11:8] for very short exposure
0x80206111	SNR0_AWBG_R_GAIN_V_L	0x00	RW	Bit[7:0]: Sensor 0 R gain[7:0] for very short exposure
0x80206112	SNR0_AWBG_GR_GAIN_V_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 Gr gain[11:8] for very short exposure
0x80206113	SNR0_AWBG_GR_GAIN_V_L	0x00	RW	Bit[7:0]: Sensor 0 Gr gain[7:0] for very short exposure
0x80206114	SNR0_AWBG_GB_GAIN_V_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 Gb gain[11:8] for very short exposure
0x80206115	SNR0_AWBG_GB_GAIN_V_L	0x00	RW	Bit[7:0]: Sensor 0 Gb gain[7:0] for very short exposure
0x80206116	SNR0_AWBG_B_GAIN_V_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 B gain[11:8] for very short exposure
0x80206117	SNR0_AWBG_B_GAIN_V_L	0x00	RW	Bit[7:0]: Sensor 0 B gain[7:0] for very short exposure
0x80206150	SNR1_AWBG_R_GAIN_L_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 R gain[11:8] for long exposure
0x80206151	SNR1_AWBG_R_GAIN_L_L	0x00	RW	Bit[7:0]: Sensor 1 R gain[7:0] for long exposure
0x80206152	SNR1_AWBG_GR_GAIN_L_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 Gr gain[11:8] for long exposure
0x80206153	SNR1_AWBG_GR_GAIN_L_L	0x00	RW	Bit[7:0]: Sensor 1 Gr gain[7:0] for long exposure
0x80206154	SNR1_AWBG_GB_GAIN_L_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 Gb gain[11:8] for long exposure

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table 3-5 AWB gain control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x80206155	SNR1_AWBG_GB_GAIN_L_L	0x00	RW	Bit[7:0]: Sensor 1 Gb gain[7:0] for long exposure
0x80206156	SNR1_AWBG_B_GAIN_L_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 B gain[11:8] for long exposure
0x80206157	SNR1_AWBG_B_GAIN_L_L	0x00	RW	Bit[7:0]: Sensor 1 B gain[7:0] for long exposure
0x80206158	SNR1_AWBG_R_GAIN_S_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 R gain[11:8] for short exposure
0x80206159	SNR1_AWBG_R_GAIN_S _L	0x00	RW	Bit[7:0]: Sensor 1 R gain[7:0] for short exposure
0x8020615A	SNR1_AWBG_GR_GAIN_S_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 Gr gain[11:8] for short exposure
0x8020615B	SNR1_AWBG_GR_GAIN_S _L	0x00	RW	Bit[7:0]: Sensor 1 Gr gain[7:0] for short exposure
0x8020615C	SNR1_AWBG_GB_GAIN_S_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 Gb gain[11:8] for short exposure
0x8020615D	SNR1_AWBG_GB_GAIN_S _L	0x00	RW	Bit[7:0]: Sensor 1 Gb gain[7:0] for short exposure
0x8020615E	SNR1_AWBG_B_GAIN_S_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 B gain[11:8] for short exposure
0x8020615F	SNR1_AWBG_B_GAIN_S _L	0x00	RW	Bit[7:0]: Sensor 1 B gain[7:0] for short exposure
0x80206160	SNR1_AWBG_R_GAIN_V_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 R gain[11:8] for very short exposure
0x80206161	SNR1_AWBG_R_GAIN_V _L	0x00	RW	Bit[7:0]: Sensor 1 R gain[7:0] for very short exposure
0x80206162	SNR1_AWBG_GR_GAIN_V_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 Gr gain[11:8] for very short exposure
0x80206163	SNR1_AWBG_GR_GAIN_V _L	0x00	RW	Bit[7:0]: Sensor 1 Gr gain[7:0] for very short exposure
0x80206164	SNR1_AWBG_GB_GAIN_V_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 Gb gain[11:8] for very short exposure

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table 3-5 AWB gain control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x80206165	SNR1_AWBG_GB_ GAIN_V _L	0x00	RW	Bit[7:0]: Sensor 1 Gb gain[7:0] for very short exposure
0x80206166	SNR1_AWBG_B_ GAIN_V_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 B gain[11:8] for very short exposure
0x80206167	SNR1_AWBG_B_ GAIN_V _L	0x00	RW	Bit[7:0]: Sensor 1 B gain[7:0] for very short exposure

table 3-6 manual AWB gain firmware registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x0C	MAXAWBGAIN_0_H	0x07	RW	Max AWB Gain (B Gain) for L Channel
0x0D	MAXAWBGAIN_0_L	0xFF	RW	Max AWB Gain (B Gain) for L Channel
0x0E	MAXAWBGAIN_1_H	0x07	RW	Max AWB Gain (G Gain) for S Channel
0x0F	MAXAWBGAIN_1_L	0xFF	RW	Max AWB Gain (G Gain) for S Channel
0x10	MAXAWBGAIN_2_H	0x07	RW	Max AWB Gain (R Gain) for VS Channel
0x11	MAXAWBGAIN_2_L	0xFF	RW	Max AWB Gain (R Gain) for VS Channel
0x7C	MANUALAWBGAIN_0_0_H	0x01	RW	Manual AWB R Gain for L Channel
0x7D	MANUALAWBGAIN_0_0_L	0x28	RW	Manual AWB R Gain for L Channel
0x7E	MANUALAWBGAIN_0_1_H	0x01	RW	Manual AWB Gr Gain for L Channel
0x7F	MANUALAWBGAIN_0_1_L	0x00	RW	Manual AWB Gr Gain for L Channel
0x8 0	MANUALAWBGAIN_0_2_H	0x01	RW	Manual AWB Gb Gain for L Channel
0x81	MANUALAWBGAIN_0_2_L	0x00	RW	Manual AWB Gb Gain for L Channel
0x82	MANUALAWBGAIN_0_3_H	0x02	RW	Manual AWB B Gain for L Channel
0x83	MANUALAWBGAIN_0_3_L	0x00	RW	Manual AWB B Gain for L Channel
0x84	MANUALAWBGAIN_1_0_H	0x01	RW	Manual AWB R Gain for S Channel
0x85	MANUALAWBGAIN_1_0_L	0x28	RW	Manual AWB R Gain for S Channel
0x86	MANUALAWBGAIN_1_1_H	0x01	RW	Manual AWB Gr Gain for S Channel
0x87	MANUALAWBGAIN_1_1_L	0x00	RW	Manual AWB Gr Gain for S Channel
0x88	MANUALAWBGAIN_1_2_H	0x01	RW	Manual AWB Gb Gain for S Channel

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table 3-6 manual AWB gain firmware registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x89	MANUALAWBGAIN_1_2_L	0x00	RW	Manual AWB Gb Gain for S Channel
0x8A	MANUALAWBGAIN_1_3_H	0x02	RW	Manual AWB B Gain for S Channel
0x8B	MANUALAWBGAIN_1_3_L	0x00	RW	Manual AWB B Gain for S Channel
0x8C	MANUALAWBGAIN_2_0_H	0x01	RW	Manual AWB R Gain for VS Channel
0x8D	MANUALAWBGAIN_2_0_L	0x28	RW	Manual AWB R Gain for VS Channel
0x8E	MANUALAWBGAIN_2_1_H	0x01	RW	Manual AWB Gr Gain for VS Channel
0x8F	MANUALAWBGAIN_2_1_L	0x00	RW	Manual AWB Gr Gain for VS Channel
0x90	MANUALAWBGAIN_2_2_H	0x01	RW	Manual AWB Gb Gain for VS Channel
0x91	MANUALAWBGAIN_2_2_L	0x00	RW	Manual AWB Gb Gain for VS Channel
0x92	MANUALAWBGAIN_2_3_H	0x02	RW	Manual AWB B Gain for VS Channel
0x93	MANUALAWBGAIN_2_3_L	0x00	RW	Manual AWB B Gain for VS Channel

3.9.2 AWB statistics

The OV490 uses a 5x5 sub window and a ROI window for AWB data statistics.

3.9.2.1 5x5 sub window

The total image is divided to a 5x5 sub window by defining the width and height of each window. The 5x5 window's start point and end point is same as the total image's left-top point and right-bottom point.

If the total image cannot be divided evenly into 5 times of the sub window, each 5x5 window will be not same area. The OV490 will divide the window at the beginning of point (0,0), then set the window in order. If total image width or height is not 5 times that of the small window size, the sub window size of the last column or row will be different with smaller win-width and win-height. The OV490 will adjust the small window size of the last column or row to confirm the 5x5 window is filled with the total image window.

The width and height of the windows are defined in registers {0x80206C31, 0x80206C32} and {0x80206C33, 0x80206C34} ({0x80206CD1, 0x80206CD2} and {0x80206CD3, 0x80206CD4} for the second sensor). Each sub-window can be enabled/disabled by a control bit of registers 0x80206C2C~0x80206C30 (0x80206CCC~0x80206CD0 for the second sensor).

3.9.2.2 ROI window

Besides the 5x5 sub window, the ROI function is also supported for advanced AWB statistics and is enabled by register 0x80206C00[1] (0x80206CA0[1] for the second sensor). The coordinates for ROI window is set by registers 0x80206C01~0x80206C08 (0x80206CA1~0x80206CA8 for the second sensor).

The AWB statistics will integrate the 5x5 window and ROI window to get the final statistics. All pixels outside of ROI window will not be calculated.

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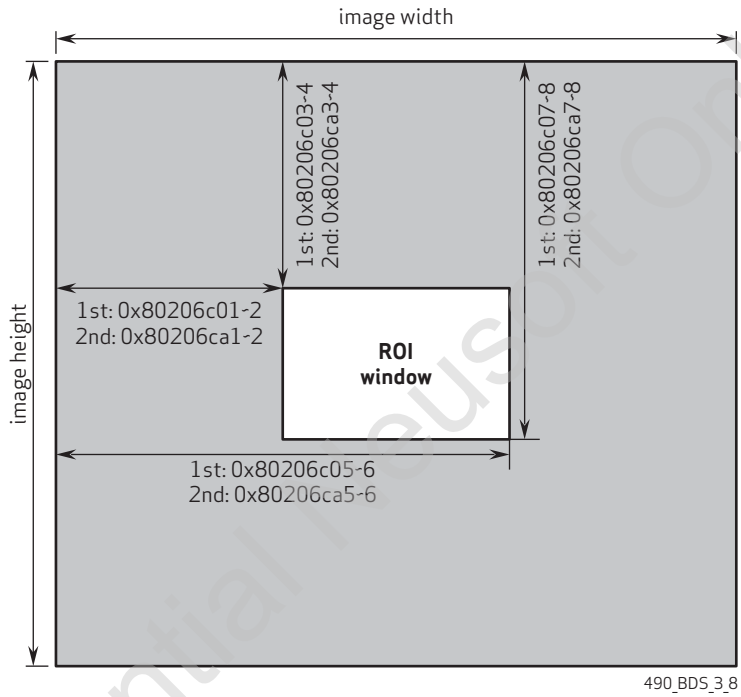
figure 3-8 AWB statistics ROI window diagram



Pixels that are too dark or bright are excluded from the statistics. When the value (10-bit) is greater than registers 0x80206C0A~0x80206C0B (0x80206CAA~0x80206CAB for the second sensor) or less than registers 0x80206C0C~0x80206C0D (0x80206CAC~0x80206CAD for the second sensor), it is excluded from the statistics.

The more number of gray pixels in the scene, the more accurate the AWB is. In order to increase AWB accuracy, the sensor starts to adjust WB gain only when the gray pixel number exceeds a certain threshold. The threshold is defined by firmware registers 0x20~0x21.

AWB statistics can be calculated from sub-sampled image. The horizontal and vertical sub-sampling ratio is set by registers 0x80206C09 (0x80206CA9 for the second sensor).

table 3-7 AWB statistics firmware registers

address	register name	default value	R/W	description
0x20	CURVEAWBMINNUM_H	0x04	RW	AWB Minimum Statistics Number High Byte
0x21	CURVEAWBMINNUM_L	0x00	RW	AWB Minimum Statistics Number Low Byte

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table 3-8 AWB statistics registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x80206C00	SNR0_CURVE_AWB_ CTRL	0x00	RW	Sensor 0 Curve AWB Control Bit[7:5]: Reserved Bit[4:3]: Statistic exposure select 00: Long 01: Short 1x: Very short Bit[2]: Simple enable 1: Simple mode enable Bit[1]: Statistic rectangle enable 0: Statistic all 1: Statistic rectangle Bit[0]: InterP mode enable (m_bInterpModeEnable)
0x80206C01	SNR0_AWB_STAT_ RECT_LEFT_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 statistic rectangle left coordinate[11:8]
0x80206C02	SNR0_AWB_STAT_ RECT_LEFT_L	0x00	RW	Bit[7:0]: Sensor 0 statistic rectangle left coordinate[7:0]
0x80206C03	SNR0_AWB_STAT_ RECT_TOP_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 statistic rectangle top coordinate[10:8]
0x80206C04	SNR0_AWB_STAT_ RECT_TOP_L	0x00	RW	Bit[7:0]: Sensor 0 statistic rectangle top coordinate[7:0]
0x80206C05	SNR0_AWB_STAT_ RECT_RIGHT_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 statistic rectangle right coordinate[11:8]
0x80206C06	SNR0_AWB_STAT_ RECT_RIGHT_L	0x00	RW	Bit[7:0]: Sensor 0 statistic rectangle right coordinate[7:0]
0x80206C07	SNR0_AWB_STAT_ RECT_BOTTOM_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 statistic rectangle bottom coordinate[10:8]
0x80206C08	SNR0_AWB_STAT_ RECT_BOTTOM_L	0x00	RW	Bit[7:0]: Sensor 0 statistic rectangle bottom coordinate[7:0]
0x80206C09	SNR0_AWB_ STATISTIC_RATE	0x44	RW	Bit[7:4]: Sensor 0 X statistic sample rate Bit[3:0]: Sensor 0 Y statistic sample rate
0x80206C0A	SNR0_AWB_MAX_ ALUE_H	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 statistic maximum value[9:8]
0x80206C0B	SNR0_AWB_MAX_ VALUE_L	0xE0	RW	Bit[7:0]: Sensor 0 statistic maximum value[7:0]

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table 3-8 AWB statistics registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x80206C0C	SNR0_AWB_MIN_VALUE_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 statistic minimum value[9:8]
0x80206C12	SNR0_AWB_SCALE_BITS	0x0A	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 scale bits (can be 0x8 or 0xA only)
0x80206C2C	SNR0_AWB_ROW0_WIN_EN	0x1F	RW	Sensor 0 Sub-windows [0][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 00 enable Bit[3]: Sub-window 01 enable Bit[2]: Sub-window 02 enable Bit[1]: Sub-window 03 enable Bit[0]: Sub-window 04 enable
0x80206C2D	SNR0_AWB_ROW1_WIN_EN	0x1F	RW	Sensor 0 Sub-windows [1][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 10 enable Bit[3]: Sub-window 11 enable Bit[2]: Sub-window 12 enable Bit[1]: Sub-window 13 enable Bit[0]: Sub-window 14 enable
0x80206C2E	SNR0_AWB_ROW2_WIN_EN	0x1F	RW	Sensor 0 Sub-windows [2][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 20 enable Bit[3]: Sub-window 21 enable Bit[2]: Sub-window 22 enable Bit[1]: Sub-window 23 enable Bit[0]: Sub-window 24 enable
0x80206C2F	SNR0_AWB_ROW3_WIN_EN	0x1F	RW	Sensor 0 Sub-windows [3][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 30 enable Bit[3]: Sub-window 31 enable Bit[2]: Sub-window 32 enable Bit[1]: Sub-window 33 enable Bit[0]: Sub-window 34 enable
0x80206C30	SNR0_AWB_ROW4_WIN_EN	0x1F	RW	Sensor 0 Sub-windows [4][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 40 enable Bit[3]: Sub-window 41 enable Bit[2]: Sub-window 42 enable Bit[1]: Sub-window 43 enable Bit[0]: Sub-window 44 enable
0x80206C31	SNR0_AWB_SUB_WIN_WIDTH_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 sub-window width[9:8]
0x80206C32	SNR0_AWB_SUB_WIN_WIDTH_L	0x96	RW	Bit[7:0]: Sensor 0 sub-window width[7:0]

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table 3-8 AWB statistics registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x80206C33	SNR0_AWB_SUB_WIN_HEIGHT_H	0x00	RW	Bit[7:1]: Reserved Bit[0]: Sensor 0 sub-window height[8]
0x80206C34	SNR0_AWB_SUB_WIN_HEIGHT_L	0x68	RW	Bit[7:0]: Sensor 0 sub-window height[7:0]
0x80206CA0	SNR1_CURVE_AWB_CTRL	0x00	RW	Sensor 1 Curve AWB Control Signals Bit[7:5]: Reserved Bit[4:3]: Statistic exposure select 00: Long 01: Short 1x: Very short Bit[2]: Simple enable 1: Simple mode enable Bit[1]: Statistic rectangle enable 0: Statistic all 1: Statistic rectangle Bit[0]: InterP mode enable (m_bInterpModeEnable)
0x80206CA1	SNR1_AWB_STAT_RECT_LEFT_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 statistic rectangle left coordinate[11:8]
0x80206CA2	SNR1_AWB_STAT_RECT_LEFT_L	0x00	RW	Bit[7:0]: Sensor 1 statistic rectangle left coordinate[7:0]
0x80206CA3	SNR1_AWB_STAT_RECT_TOP_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 statistic rectangle top coordinate[10:8]
0x80206CA4	SNR1_AWB_STAT_RECT_TOP_L	0x00	RW	Bit[7:0]: Sensor 1 statistic rectangle top coordinate[7:0]
0x80206CA5	SNR1_AWB_STAT_RECT_RIGHT_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 statistic rectangle right coordinate[11:8]
0x80206CA6	SNR1_AWB_STAT_RECT_RIGHT_L	0x00	RW	Bit[7:0]: Sensor 1 statistic rectangle right coordinate[7:0]
0x80206CA7	SNR1_AWB_STAT_RECT_BOTTOM_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 statistic rectangle bottom coordinate[10:8]
0x80206CA8	SNR1_AWB_STAT_RECT_BOTTOM_L	0x00	RW	Bit[7:0]: Sensor 1 statistic rectangle bottom coordinate[7:0]
0x80206CAA	SNR1_AWB_MAX_VALUE_H	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 statistic maximum value[9:8]
0x80206CAB	SNR1_AWB_MAX_VALUE_L	0xE0	RW	Bit[7:0]: Sensor 1 statistic maximum value[7:0]

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table 3-8 AWB statistics registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x80206CAC	SNR1_AWB_MIN_VALUE_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 statistic minimum value[9:8]
0x80206CAD	SNR1_AWB_MIN_VALUE_L	0x0E	RW	Bit[7:0]: Sensor 1 statistic minimum value[7:0]
0x80206CB2	SNR1_AWB_SCALE_BITS	0x0A	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 scale bits (can be 0x8 or 0xA only)
0x80206CB3	SNR1_AWB_WEIGHT_TH	0x00	RW	Bit[7:0]: Sensor 1 weight threshold
0x80206CCC	SNR1_AWB_ROW0_WIN_EN	0x1F	RW	Sensor 1 Sub-windows [0][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 00 enable Bit[3]: Sub-window 01 enable Bit[2]: Sub-window 02 enable Bit[1]: Sub-window 03 enable Bit[0]: Sub-window 04 enable
0x80206CCD	SNR1_AWB_ROW1_WIN_EN	0x1F	RW	Sensor 1 Sub-windows [1][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 10 enable Bit[3]: Sub-window 11 enable Bit[2]: Sub-window 12 enable Bit[1]: Sub-window 13 enable Bit[0]: Sub-window 14 enable
0x80206CCE	SNR1_AWB_ROW2_WIN_EN	0x1F	RW	Sensor 1 Sub-windows [2][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 20 enable Bit[3]: Sub-window 21 enable Bit[2]: Sub-window 22 enable Bit[1]: Sub-window 23 enable Bit[0]: Sub-window 24 enable
0x80206CCF	SNR1_AWB_ROW3_WIN_EN	0x1F	RW	Sensor 1 Sub-windows [3][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 30 enable Bit[3]: Sub-window 31 enable Bit[2]: Sub-window 32 enable Bit[1]: Sub-window 33 enable Bit[0]: Sub-window 34 enable
0x80206CD0	SNR1_AWB_ROW4_WIN_EN	0x1F	RW	Sensor 1 Sub-windows [4][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 40 enable Bit[3]: Sub-window 41 enable Bit[2]: Sub-window 42 enable Bit[1]: Sub-window 43 enable Bit[0]: Sub-window 44 enable

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table 3-8 AWB statistics registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x80206CD1	SNR1_AWB_SUB_WIN_WIDTH_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 sub-window width[9:8]
0x80206CD2	SNR1_AWB_SUB_WIN_WIDTH_L	0x96	RW	Bit[7:0]: Sensor 1 sub-window width[7:0]
0x80206CD3	SNR1_AWB_SUB_WIN_HEIGHT_H	0x00	RW	Bit[7:1]: Reserved Bit[0]: Sensor 1 sub-window height[8]
0x80206CD4	SNR1_AWB_SUB_WIN_HEIGHT_L	0x68	RW	Bit[7:0]: Sensor 1 sub-window height[7:0]

3.9.3 AWB gain mode

The OV490 uses long channel data to calculate AWB value, but the QE spectrum of the long and short channels are not identical due to different pixels, so the AWB gain obtained from the long channel cannot be directly applied to the short channel. The very short channel is captured by the same sub-pixel as the long channel. In order to compensate for the difference, a programmable ratio is applied on the long channel gain to derive the gain for short channel. This feature is enabled by register 0x4C. The B/G gain ratio is set by registers {0x58, 0x59} and {0x5E, 0x5F} and the R/G ratio is set by registers {0x64, 0x65} and {0x5E, 0x5F}.The ratio is adaptive to color temperature, which can be enabled by firmware register 0x4D. Color temperature is defined as 128×B/R where B and R values are AWB gain at different color temperatures. Firmware registers {0x4E, 0x4F} are for Day light threshold. Firmware registers {0x50, 0x51} are for CWF light threshold. Firmware registers {0x52, 0x53} are for A light threshold.

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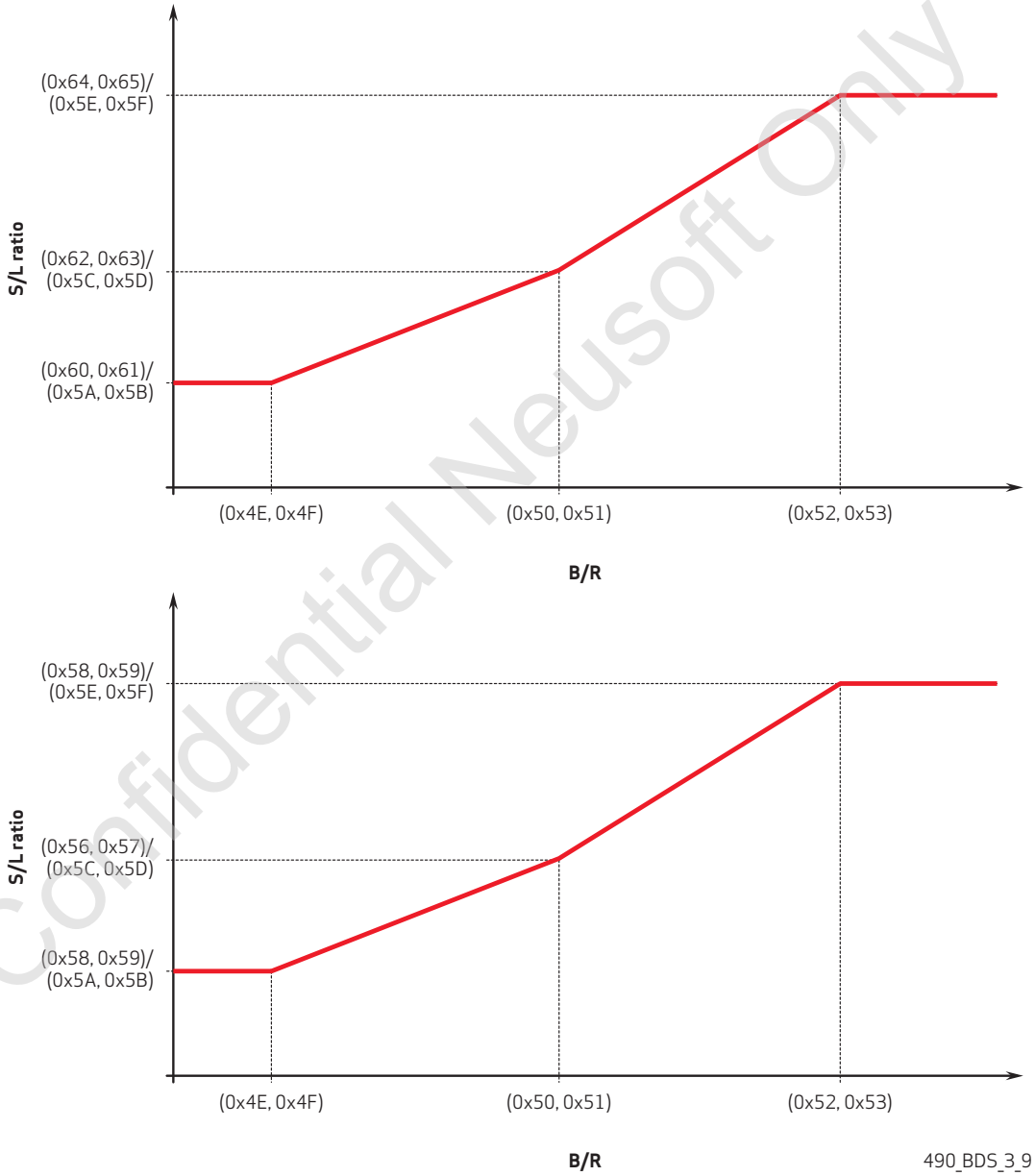
figure 3-9 AWB gain mode diagram



490_BDS_3_9

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table 3-9 AWB gain mode firmware registers

address	register name	default value	R/W	description
0x4C	ADJUSTSMALLPDGAIN ENABLE	0x01	RW	Bit[7:0]: Adjust short channel AWB gain enable
0x4D	ADAPTIVEPDGAIN ENABLE	0x00	RW	Bit[7:0]: Adaptive short channel AWB gain enable
0x4E	BRGAINTH_0_H	0x00	RW	Bit[7:0]: Day light threshold for B/G[15:8]
0x4F	BRGAINTH_0_L	0x81	RW	Bit[7:0]: Day light threshold for B/G[7:0]
0x50	BRGAINTH_1_H	0x00	RW	Bit[7:0]: CWF light threshold for B/G[15:8]
0x51	BRGAINTH_1_L	0xB0	RW	Bit[7:0]: CWF light threshold for B/G[7:0]
0x52	BRGAINTH_2_H	0x01	RW	Bit[7:0]: A light threshold for B/G[15:8]
0x53	BRGAINTH_2_L	0x1E	RW	Bit[7:0]: A light threshold for B/G[7:0]
0x54	PDGAINB_0_H	0x00	RW	Bit[7:0]: Blue gain for Day light[15:8]
0x55	PDGAINB_0_L	0x80	RW	Bit[7:0]: Blue gain for Day light[7:0]
0x56	PDGAINB_1_H	0x00	RW	Bit[7:0]: Blue gain for CWF light[15:8]
0x57	PDGAINB_1_L	0x80	RW	Bit[7:0]: Blue gain for CWF light[7:0]
0x58	PDGAINB_2_H	0x00	RW	Bit[7:0]: Blue gain for A light[15:8]
0x59	PDGAINB_2_L	0x80	RW	Bit[7:0]: Blue gain for A light[7:0]
0x5A	PDGAING_0_H	0x00	RW	Bit[7:0]: Green gain for Day light[15:8]
0x5B	PDGAING_0_L	0x94	RW	Bit[7:0]: Green gain for Day light[7:0]
0x5C	PDGAING_1_H	0x00	RW	Bit[7:0]: Green gain for CWF light[15:8]
0x5D	PDGAING_1_L	0x94	RW	Bit[7:0]: Green gain for CWF light[7:0]
0x5E	PDGAING_2_H	0x00	RW	Bit[7:0]: Green gain for A light[15:8]
0x5F	PDGAING_2_L	0x94	RW	Bit[7:0]: Green gain for A light[7:0]
0x60	PDGAINR_0_H	0x00	RW	Bit[7:0]: Red gain for Day light[15:8]
0x61	PDGAINR_0_L	0xA0	RW	Bit[7:0]: Red gain for Day light[7:0]
0x62	PDGAINR_1_H	0x00	RW	Bit[7:0]: Red gain for CWF light[15:8]
0x63	PDGAINR_1_L	0xA0	RW	Bit[7:0]: Red gain for CWF light[7:0]
0x64	PDGAINR_2_H	0x00	RW	Bit[7:0]: Red gain for A light[15:8]
0x65	PDGAINR_2_L	0xA0	RW	Bit[7:0]: Red gain for A light[7:0]

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3.9.4 AWB algorithm

The OV490 uses an AWB algorithm to achieve white balance. The OV490 has two kinds of AWB mode: simple AWB and advance AWB. The AWB algorithm works in either simple or advanced mode based on different AWB control options. The AWB algorithm can also be disabled so the WB gains are fully controlled by the backend processor.

3.9.4.1 simple AWB algorithm

Simple AWB algorithm is based on the gray world assumption, meaning the OV490 will make the R, G and B average of all pixels equal to each other by adjusting the gain of each color channel. This is accomplished by taking the statistics of all pixels on the whole image. Setting register 0x80206C00[2] =1 enables simple AWB (register 0x80206CA0[2] is for the second sensor).

table 3-10 AWB algorithm control registers

address	register name	default value	R/W	description
0x80206C00	SNR0_CURVE_AWB_CTRL	0x00	RW	Sensor 0 Curve AWB Control Bit[2]: Simple enable 0: Curve mode enable 1: Simple mode enable
0x80206CA0	SNR1_CURVE_AWB_CTRL	0x00	RW	Sensor 1 Curve AWB Control Bit[2]: Simple enable 0: Curve mode enable 1: Simple mode enable

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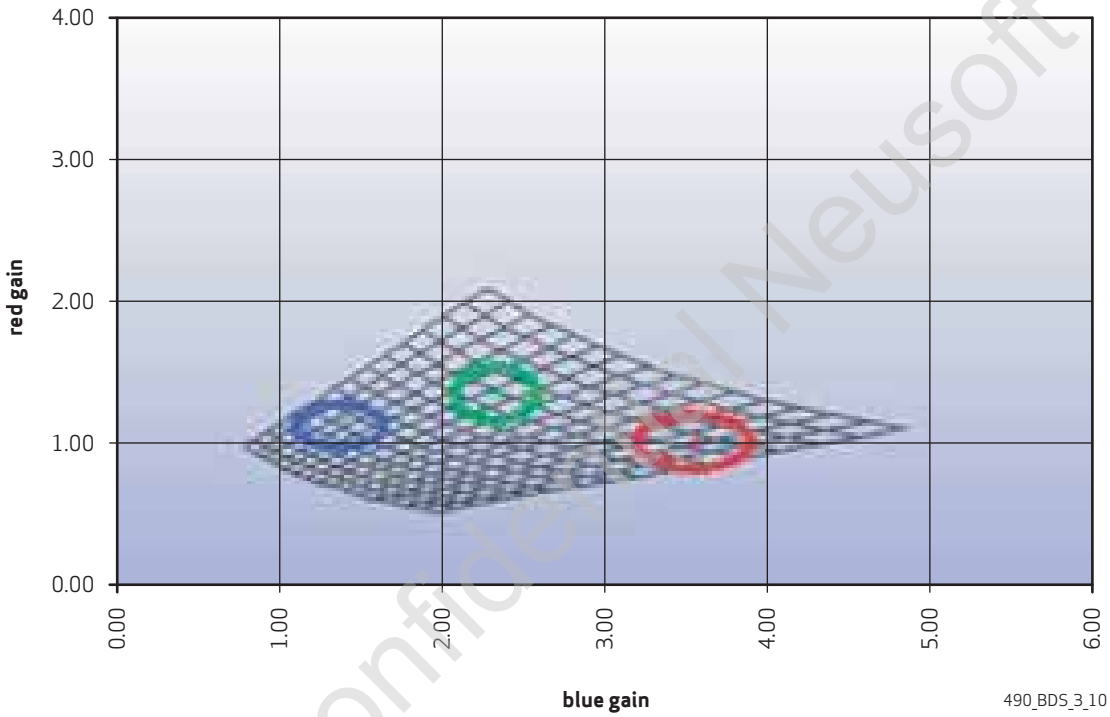
3.9.5 advanced AWB

The OV490 implements an advanced AWB algorithm. Based on the AWB statistics, the RGB color is one-to-one mapped to the x-y axis of the input of a 2D look up table (LUT). For any given input RGB color, the LUT indicates the probability of being a gray object. Then, AWB gains for the different channels are obtained by indexing the LUT. Advanced AWB offers flexible control over the corner cases, such as scenes with dominant color and/or skin tone.

figure 3-10 advanced AWB LUT example



Advanced AWB is a calibration-based algorithm. The calibration procedure uses a gray chart as a target and captures RAW images under different light sources with different color temperatures. The minimum color temperatures to cover should include outdoor (e.g., sunshine, cloudy) and typical artificial lightening sources (e.g., incandescent, fluorescent, etc.).

Instead of finding the gain area on the entire color temperature, the advanced AWB takes the normalized red and blue gain in representative low, middle and high color temperature illumination, and automatically extends them to define the gain area. This is shown in **figure 3-10**. In the LUT space, four different rectangular regions are defined, which will be used for different purposes.

In the advanced algorithm, the gain area is divided into 16x16 blocks and the user can adjust the weighting of each block. The weight of each block represents the likelihood of the corresponding color temperature appearing in the real world. If the block's weight value is 0, it means that this block is excluded from the gain area. The block's weight values can be set to a proper number to prevent color wash out from a solid color object, skin, etc.

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In the curve AWB LUT map is stored in 128 byte map registers, where each byte saves 2 rectangle weight tables, for a total 256 LUT. Firmware registers 0xC3~0x142 define the weighting of the 16x16 blocks. The weight value is from 0x0 to 0xF. The higher the weighting, the more emphasis on that color temperature. Natural lighting usually spans a certain range, so it is better to avoid big weight changes between the adjacent blocks.

table 3-11 curve AWB LUT map firmware registers

address	register name	default value	R/W	description
0xC3	AWBMAP_0	0x08	RW	Bit[7:0]: AWB map_0
0x142	AWBMAP_127	0x08	RW	Bit[7:0]: AWB map_127

3.9.5.1 AWB speed and stable range

From a white balance state, the AWB algorithm will start to adjust the WB gain again once the difference between color channels is greater than the threshold set by register 0x196/256. The AWB algorithm will keep adjusting them until the difference is less than the threshold set by register 0x195/256.

Firmware register 0x66 is the relative WB gain adjustment step, which determines WB gain adjustment based on the distance from current WB gain to target WB gain. Firmware register 0x67 sets the maximum of adjustment the algorithm will take before stopping.

table 3-12 AWB speed and stable firmware registers

address	register name	default value	R/W	description
0x66	AWBStep1	0x08	RW	Relative AWB Adjustment Step
0x67	AWBStep2	0x80	RW	Maximum Number of Adjustments
0x195	AWBStableRange_1	0x20	RW	AWB Stable Range Threshold 1
0x196	AWBStableRange_2	0x40	RW	AWB Stable Range Threshold 2

3.9.5.2 advanced AWB tuning guidelines

The AWB control parameters must be calibrated using the target lens because the lens transmittance affects the color ratio.

The lens correction profile will also slightly change the overall color ratio. So lens shading correction has to be fine tuned before AWB tuning.

Tuning the AWB in a light box with a low, middle, and high color temperature illuminator is the fastest way to achieve the correct setting. Either the WB gain, to achieve good white balance for a gray scene, or the raw images, that contain some gray object without WB gain, can be used to determine the advanced AWB parameters.

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However, the R, G, and B gain in various lighting conditions with good white balance (by either manual adjustment or by simple AWB with a neutral scene) are helpful for checking and improving the AWB setting coverage.

The WB gain of artificial light can vary by large amounts. It is important to check the WB gain in these conditions if the target application is required to run in these lighting conditions.

There is a trade-off between the AWB accuracy and the coverage. A smaller WB gain area provides a more accurate WB result, but the coverage is lower and the AWB accuracy may not be so good in certain light conditions.

3.9.5.3 AWB shift

For some users, certain color tints are preferred over the accurate white balance. Post AWB shift function is designed to allow the user to render a certain tint.

If enabling this post AWB shift function, the calculated AWB gain will be adjusted by multiplying the adjust factor.

table 3-13 post AWB shift firmware registers

address	register name	default value	R/W	description
0xBC	BGAINSHIFT_H	0x01	RW	Bit[7:0]: Long channel blue gain adjustment[15:8] Bgain= Bgain x BgainShift/128
0xBD	BGAINSHIFT_L	0x01	RW	Bit[7:0]: Long channel blue gain adjustment[7:0]
0xBE	GGAINSHIFT_H	0x01	RW	Bit[7:0]: Long channel green gain adjustment[15:8] Ggain = Ggain × GgainShift/128
0xBF	GGAINSHIFT_L	0x00	RW	Bit[7:0]: Long channel green gain adjustment[7:0]
0xC0	RGAINSHIFT_H	0x01	RW	Bit[7:0]: Long channel red gain adjustment[15:8] Rgain = Rgain × RgainShift/128
0xC1	RGAINSHIFT_L	0x00	RW	Bit[7:0]: Long channel red gain adjustment[7:0]
0xC2	MANUALAWBGAIN SHIFTENABLE	0x01	RW	Bit[0]: Post AWB shift function control 0: Disable 1: Enable

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3.10 defect pixel correction (DPC)

The DPC function detects defect pixels/clusters by using a programmable white/black threshold. The threshold can be automatically calculated based on analog gain from a programmable threshold gain curve or set manually. In the OV490, the DPC module is enabled/disabled with same signal for L/S/VS channels 0x80206010[5] (0x80206030[5] for the second sensor), but white/black defect pixel process can be set with different values for L/S/VS channels (see **figure 3-11** and **table 3-14**).

figure 3-11 threshold gain curve in auto threshold mode

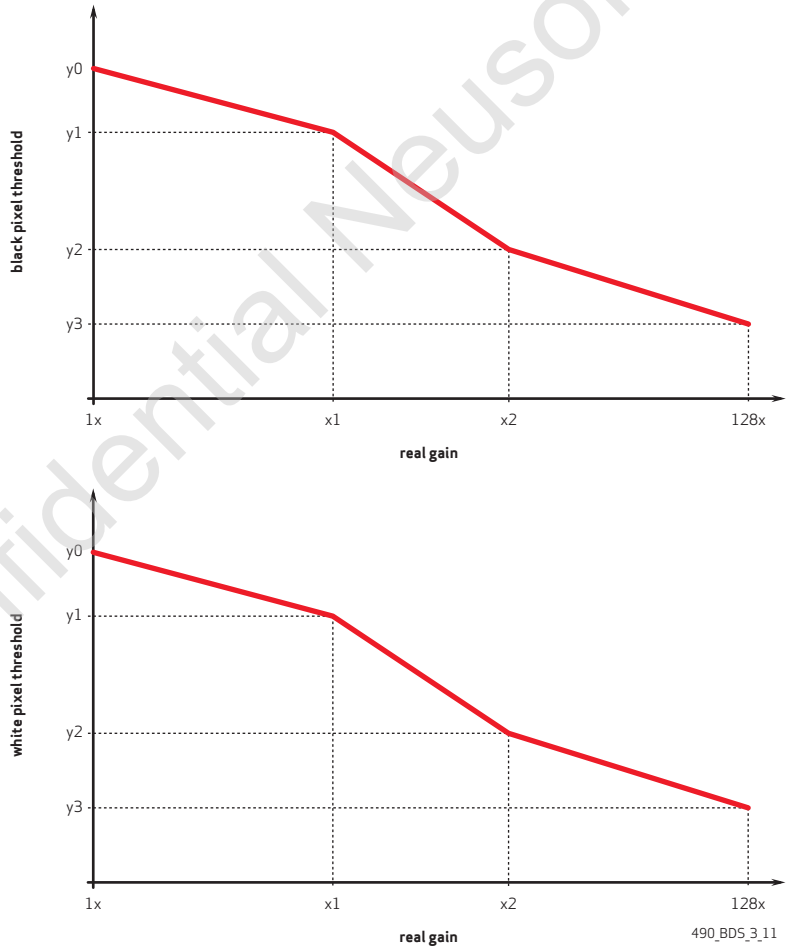

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table 3-14 threshold gain curve

axis	L	S	VS
first sensor white pixel threshold and real gain curve			
x1	0x80206203	0x80206223	0x80206243
x2	0x80206204	0x80206224	0x80206244
y0	0x80206209	0x80206229	0x80206249
y1	0x8020620A	0x8020622A	0x8020624A
y2	0x8020620B	0x8020622B	0x8020624B
y3	0x8020620C	0x8020622C	0x8020624C
second sensor white pixel threshold and real gain curve			
x1	0x80206283	0x802062A3	0x802062C3
x2	0x80206284	0x802062A4	0x802062C4
y0	0x80206289	0x802062A9	0x802062C9
y1	0x8020628A	0x802062AA	0x802062CA
y2	0x8020628B	0x802062AB	0x802062CB
y3	0x8020628C	0x802062AC	0x802062CC
first sensor black pixel threshold and real gain curve			
x1	0x80206203	0x80206223	0x80206243
x2	0x80206204	0x80206224	0x80206244
y0	0x8020620D	0x8020622D	0x8020624D
y1	0x8020620E	0x8020622E	0x8020624E
y2	0x8020620F	0x8020622F	0x8020624F
y3	0x80206210	0x80206230	0x80206250
second sensor black pixel threshold and real gain curve			
x1	0x80206283	0x802062A3	0x802062C3
x2	0x80206284	0x802062A4	0x802062C4
y0	0x8020628D	0x802062AD	0x802062CD
y1	0x8020628E	0x802062AE	0x802062CE
y2	0x8020628F	0x802062AF	0x802062CF
y3	0x80206290	0x802062B0	0x802062D0

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The DPC can correct single, couplets, cross types and tail types defect pixels. **figure 3-12** to **figure 3-17** illustrate defect patterns that can be detected.

figure 3-12 types of white pixels

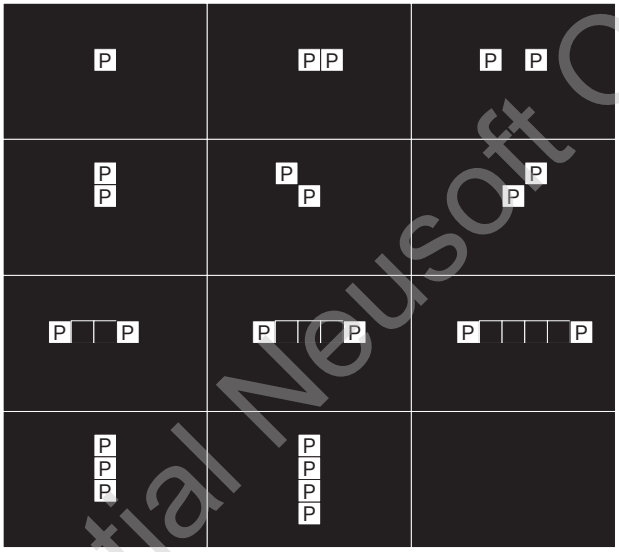
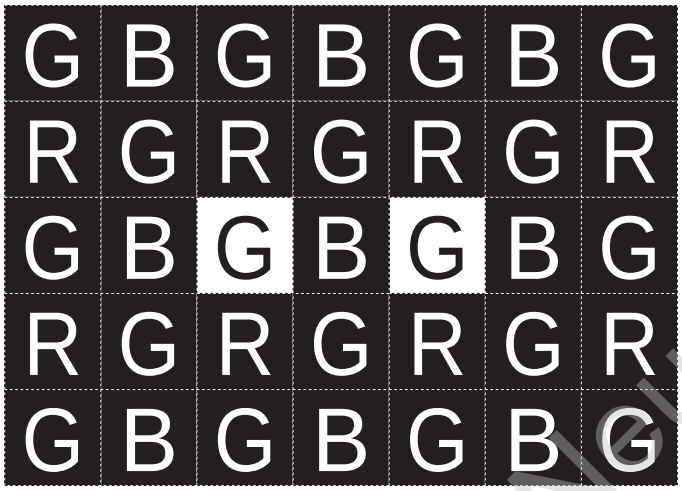
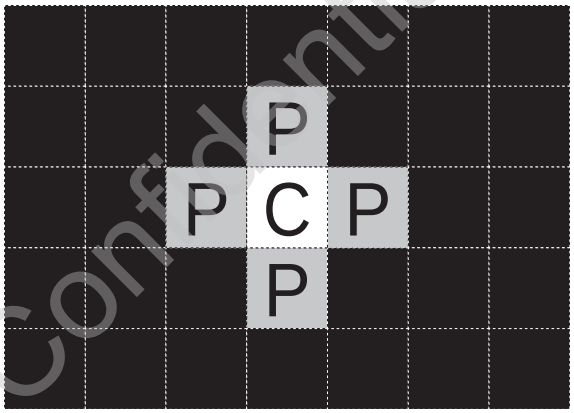

P
P P
P P
P
P

figure 3-14 example of same channel connected



490_BDS_3_14

figure 3-15 example of white cluster



490_BDS_3_15

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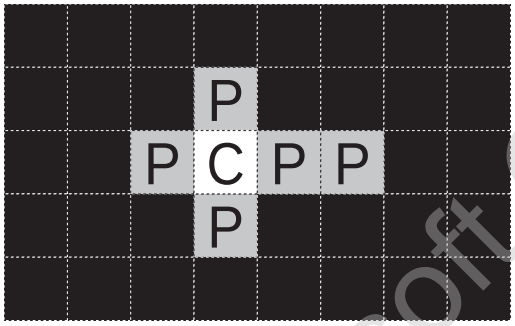
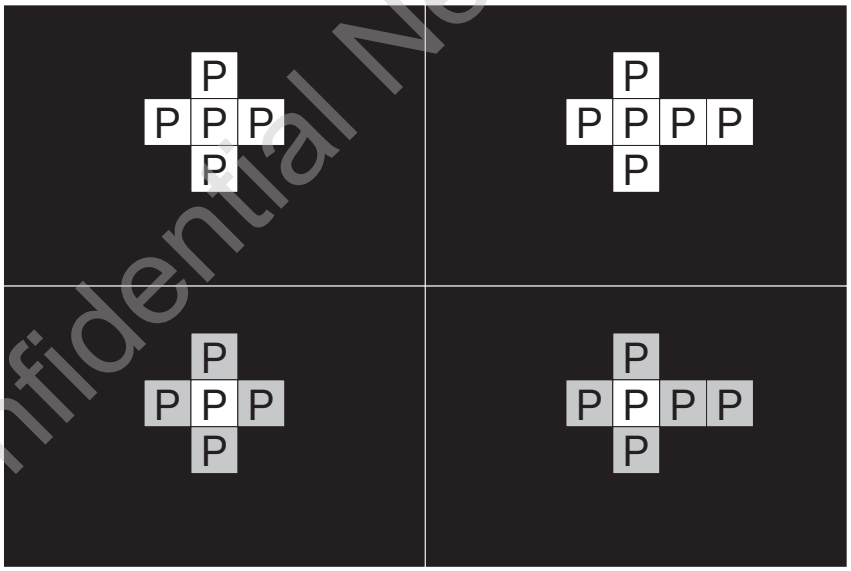
figure 3-16 example of tailing pixel



490_BDS_3_16

figure 3-17 example of tailing pixel 2



490_BDS_3_17

Threshold for T-cluster can be manually set or changed automatically according to real gain (see **figure 3-18**).

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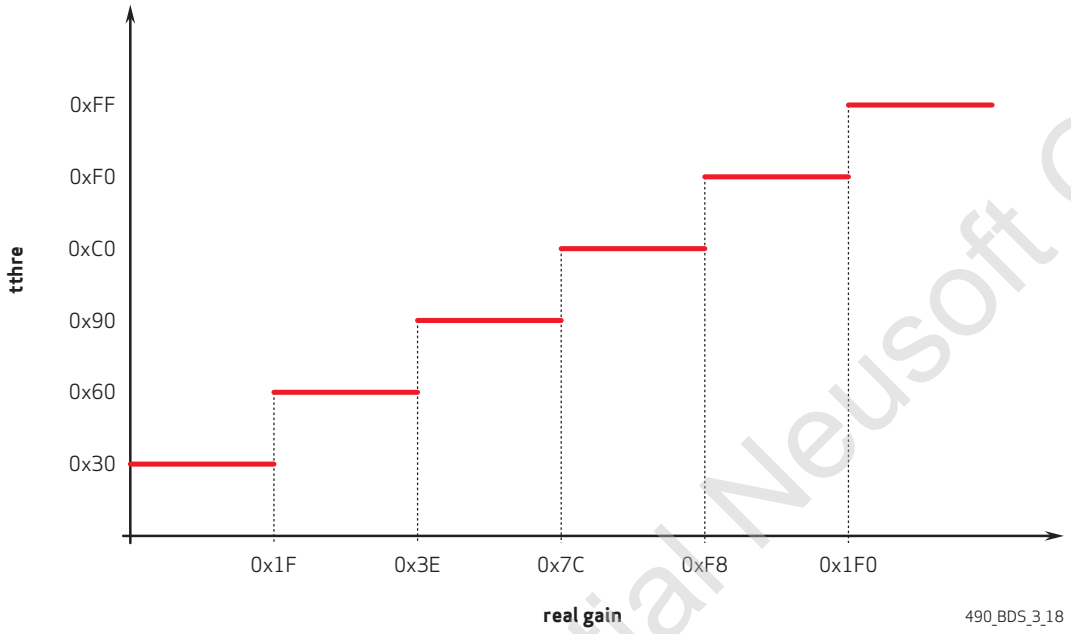
figure 3-18 threshold for T-cluster diagram



Threshold for T-cluster can be manually set or changed automatically according to real gain.

If vertical black pixel detection mode is enabled by setting register 0x80206201[5] to high for the first sensor and register 0x80206281[5] to high for the second sensor, the vertical black pixel detection function automatically activates according to the relationship between sensor real gain and two thresholds. If real gain is not less than the first threshold, activate; otherwise, if real gain is not larger than second threshold, deactivate. The two thresholds are controlled by registers 0x80206211~ 0x80206212. (registers 0x80206291~0x80206292 for second sensor). The long channel example is similar to registers for short channel and very short channel.

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table 3-15 DPC registers (sheet 1 of 26)

address	register name	default value	R/W	description
0x80206200	SNR0_L_DPC_CTRL00	0x18	RW	Sensor 0 Long Exposure DPC Control Bit[7]: m_bEnableTail Tail type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: m_bEnableSaturateCC Saturation type cross cluster correction enable, works only when cross cluster correction is enable 0: Disable 1: Enable Bit[5]: m_bEnableCrossCluster Cross cluster correction enable Bit[4]: m_bEnableSameChannelConnected Horizontal same color plane couplet correction enable 0: Disable 1: Enable Bit[3]: m_bEnableDiffChannelConnected Horizontal couplet correction enable 0: Disable 1: Enable Bit[2]: m_bEnableSmooth Bit[1]: m_bBWSensorEnable Bit[0]: m_bManualmode Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on the analog gain 1: Manual mode in which defect pixel threshold is set manually by register

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table 3-15 DPC registers (sheet 2 of 26)

address	register name	default value	R/W	description
0x80206201	SNR0_L_DPC_ CTRL01	0xDF	RW	Sensor 0 Long Exposure DPC Control Bit[7]: Set threshold for T-cluster 0: Automatically 1: Manually Bit[6]: r_comp_en Bit[5]: Vertical black pixel detection 0: Disable 1: Enable Bit[4]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[3]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable Bit[2]: T-cluster detection 0: Disable 1: Enable Bit[1:0]: Padding method of edge pixels 00: Pad with 0 01: Pad with 255 10: Pad with (255+1)/2 11: Pad with nearby same channel pixel This option will affect defect pixel detection of boundary pixels
0x80206202	SNR0_L_DPC_ CTRL02	0xFF	RW	Sensor 0 Long Exposure DPC Control Bit[7]: White defect pixel detection 0: Disable 1: Enable Bit[6]: Black defect pixel detection 0: Disable 1: Enable Bit[5:4]: Pixel number threshold for detection of cross-cluster Bit[3:2]: Pixel number threshold for detection of T-cluster Bit[1:0]: Number of vertical connected white pixels removed 00: Remove the upper one white pixel 01: Remove two vertical white pixels 10: Remove three or less vertical connected white pixel 11: Reserved

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table 3-15 DPC registers (sheet 3 of 26)

address	register name	default value	R/W	description
0x80206203	SNR0_L_DPC_WTHRE	0x08	RW	Bit[7]: Reserved Bit[6:0]: Threshold value for detecting white pixel in manual More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x80206204	SNR0_L_DPC_BTHRE	0x20	RW	Bit[7]: Reserved Bit[6:0]: Threshold value for detecting black pixel in manual mode More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x80206205	SNR0_L_DPC_THRE1	0x10	RW	For Sensor 0 Long Exposure Bit[7]: Reserved Bit[6:0]: Threshold value used in recovery of defect pixel for long channel The bigger the value, the more details retained, but the less effective of recovering defect
0x80206206	SNR0_L_DPC_THRE2	0x20	RW	For Sensor 0 Long Exposure Bit[7]: Reserved Bit[6:0]: Threshold for registering defect pixel to detect cross cluster for long channel The greater the threshold, the more defect pixels will be removed
0x80206207	SNR0_L_DPC_THRE3	0x10	RW	For Sensor 0 Long Exposure Bit[7:0]: Threshold to determine high frequency area where the DPC will keep the fine details for long channel The greater the threshold, the more details will be removed by DPC
0x80206207	SNR0_L_DPC_THRE3	0x10	RW	For Sensor 0 Long Exposure Bit[7:0]: Threshold to determine high frequency area where the DPC will keep the fine details for long channel The greater the threshold, the more details will be removed by DPC
0x80206208	SNR0_L_DPC_THRE4	0x18	RW	For Sensor 0 Long Exposure Bit[7]: Reserved Bit[6:0]: Threshold for detecting horizontal couplet for long channel This threshold should be greater than the threshold for single white/black pixel

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table 3-15 DPC registers (sheet 4 of 26)

address	register name	default value	R/W	description
0x80206209	SNR0_L_DPC_ WTHRE_LIST0	0x08	RW	For Sensor 0 Long Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 0 in auto mode
0x8020620A	SNR0_L_DPC_ WTHRE_LIST1	0x04	RW	For Sensor 0 Long Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 1 in auto mode
0x8020620B	SNR0_L_DPC_ WTHRE_LIST2	0x02	RW	For Sensor 0 Long Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 2 in auto mode
0x8020620C	SNR0_L_DPC_ WTHRE_LIST3	0x02	RW	For Sensor 0 Long Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 3 in auto mode
0x8020620D	SNR0_L_DPC_ BTHRE_LIST0	0x0C	RW	For Sensor 0 Long Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 0 in auto mode
0x8020620E	SNR0_L_DPC_ BTHRE_LIST1	0x06	RW	For Sensor 0 Long Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 1 in auto mode
0x8020620F	SNR0_L_DPC_ BTHRE_LIST2	0x02	RW	For Sensor 0 Long Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 2 in auto mode
0x80206210	SNR0_L_DPC_ BTHRE_LIST3	0x02	RW	For Sensor 0 Long Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 3 in auto mode
0x80206211	SNR0_L_DPC_ SAT	0xFF	RW	For Sensor 0 Long Exposure Bit[7:0]: Threshold of the center pixel for saturation type of cross cluster. To qualify a saturation type of cross cluster, the center pixel must be greater than this threshold
0x80206212	SNR0_L_DPC_ VB_GAIN_TH1	0x07	RW	For Sensor 0 Long Exposure Bit[7]: Reserved Bit[6:0]: Vertical black pixel detection threshold 1
0x80206213	SNR0_L_DPC_ VB_GAIN_TH2	0x03	RW	For Sensor 0 Long Exposure Bit[7]: Reserved Bit[6:0]: Vertical black pixel detection threshold 2
0x80206214	SNR0_L_DPC_ SMOOTH_ GLIST0	0x03	RW	For Sensor 0 Long Exposure Bit[7]: Reserved Bit[6:0]: Smooth gain list 0
0x80206215	SNR0_L_DPC_ SMOOTH_ GLIST1	0x07	RW	For Sensor 0 Long Exposure Bit[7]: Reserved Bit[6:0]: Smooth gain list 1

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table 3-15 DPC registers (sheet 5 of 26)

address	register name	default value	R/W	description
0x80206216	SNR0_L_DPC_SMOOTH_GLIST2	0x0F	RW	For Sensor 0 Long Exposure Bit[7]: Reserved Bit[6:0]: Smooth gain list 2
0x80206217	SNR0_L_DPC_SMGAIN_TH1	0x07	RW	For Sensor 0 Long Exposure Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC smooth gain threshold 1
0x80206218	SNR0_L_DPC_SMGAIN_TH2	0x03	RW	For Sensor 0 Long Exposure Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC smooth gain threshold 2
0x80206219	SNR0_L_DPC_UNSAT	0xF0	RW	For Sensor 0 Long Exposure Bit[7:0]: Threshold of un-saturation level for detection of cross-cluster and T-cluster
0x8020621A	SNR0_L_DPC_TTHRE	0x08	RW	For Sensor 0 Long Exposure Bit[7:0]: Threshold to determine a cross-cluster and T-cluster
0x80206220	SNR0_S_DPC_CTRL00	0x18	RW	For Sensor 0 Short Exposure Bit[7]: Tail type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: Saturation type cross cluster correction enable, works only when cross cluster correction is enable 0: Disable 1: Enable Bit[5]: Cross cluster correction enable Bit[4]: Horizontal same color plane couplet correction enable 0: Disable 1: Enable Bit[3]: Horizontal couplet correction enable 0: Disable 1: Enable Bit[2]: Not used Bit[1]: r_bwsnr_en Bit[0]: Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on the analog gain 1: Manual mode in which defect pixel threshold is set manually by register

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table 3-15 DPC registers (sheet 6 of 26)

address	register name	default value	R/W	description
0x80206221	SNR0_S_DPC_CTRL01	0xDF	RW	For Sensor 0 Short Exposure Bit[7]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[6]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable Bit[5]: T-cluster detection 0: Disable 1: Enable Bit[4]: Padding method of edge pixels 00: Pad with 0 01: Pad with 255 10: Pad with (255+1)/2 11: Pad with nearby same channel pixel This option will affect defect pixel detection of boundary pixels. Bit[3]: Vertical black pixel detection 0: Disable 1: Enable Bit[2]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[1:0]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable
0x80206222	SNR0_S_DPC_CTRL02	0xFF	RW	For Sensor 0 Short Exposure Bit[7]: White defect pixel detection 0: Disable 1: Enable Bit[6]: Black defect pixel detection 0: Disable 1: Enable Bit[5:4]: Pixel number threshold for detection of cross-cluster Bit[3:2]: Pixel number threshold for detection of T-cluster Bit[1:0]: Number of vertical connected white pixels removed: 00: Remove the upper one white pixel 01: Remove two vertical white pixels 10: Remove three or less vertical connected white pixel 11: Reserved

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table 3-15 DPC registers (sheet 7 of 26)

address	register name	default value	R/W	description
0x80206223	SNR0_S_DPC_WTHRE	0x08	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold value for detecting white pixel in manual More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x80206224	SNR0_S_DPC_BTHRE	0x20	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold value for detecting black pixel in manual mode More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x80206225	SNR0_S_DPC_THRE1	0x10	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold value used in recovery of defect pixel for long channel The bigger the value, the more details retained, but the less effective of recovering defect
0x80206226	SNR0_S_DPC_THRE2	0x20	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold for registering defect pixel to detect cross cluster for long channel The greater the threshold, the more defect pixels will be removed
0x80206227	SNR0_S_DPC_THRE3	0x10	RW	For Sensor 0 Short Exposure Bit[7:0]: Threshold to determine high frequency area where the DPC will keep the fine details for long channel The greater the threshold, the more details will be removed by DPC
0x80206228	SNR0_S_DPC_THRE4	0x18	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold for detecting horizontal couplet for long channel This threshold should be greater than the threshold for single while/black pixel
0x80206229	SNR0_S_DPC_WTHRE_LIST0	0x08	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 0 in auto mode

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table 3-15 DPC registers (sheet 8 of 26)

address	register name	default value	R/W	description
0x8020622A	SNR0_S_DPC_ WTHRE_LIST1	0x04	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 1 in auto mode
0x8020622B	SNR0_S_DPC_ WTHRE_LIST2	0x02	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 2 in auto mode
0x8020622C	SNR0_S_DPC_ WTHRE_LIST3	0x02	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 3 in auto mode
0x8020622D	SNR0_S_DPC_ BTHRE_LIST0	0x0C	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 0 in auto mode
0x8020622E	SNR0_S_DPC_ BTHRE_LIST1	0x06	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 1 in auto mode
0x8020622F	SNR0_S_DPC_B THRE_LIST2	0x02	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 2 in auto mode
0x80206230	SNR0_S_DPC_ BTHRE_LIST3	0x02	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 3 in auto mode
0x80206231	SNR0_S_DPC_ SAT	0xFF	RW	For Sensor 0 Short Exposure Bit[7:0]: Threshold of the center pixel for saturation type of cross cluster To qualify a saturation type of cross cluster, the center pixel must be greater than this threshold
0x80206232	SNR0_S_DPC_ VB_GAIN_TH1	0x07	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: Vertical black pixel detection threshold 1
0x80206233	SNR0_S_DPC_ VB_GAIN_TH2	0x03	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: Vertical black pixel detection threshold 2
0x80206234	SNR0_S_DPC_ SMOOTH_ GLIST0	0x03	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: Smooth gain list 0
0x80206235	SNR0_S_DPC_ SMOOTH_ GLIST1	0x07	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: Smooth gain list 1
0x80206236	SNR0_S_DPC_ SMOOTH_ GLIST2	0x0F	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: Smooth gain list 2

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table 3-15 DPC registers (sheet 9 of 26)

address	register name	default value	R/W	description
0x80206237	SNR0_S_DPC_SMGAIN_GLIST1	0x07	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC smooth gain threshold 1
0x80206238	SNR0_S_DPC_SMGAIN_GLIST2	0x03	RW	For Sensor 0 Short Exposure Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC smooth gain threshold 2
0x80206239	SNR0_S_DPC_UNSAT	0xF0	RW	For Sensor 0 Short Exposure Bit[7:0]: Threshold of un-saturation level for detection of cross-cluster and T-cluster
0x8020623A	SNR0_S_DPC_TTHRE	0x08	RW	For Sensor 0 Short Exposure Bit[7:0]: Threshold to determine a cross-cluster and T-cluster
0x80206240	SNR0_VS_DPC_CTRL00	0x18	RW	For Sensor 0 Very Short Exposure Bit[7]: Tail type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: Saturation type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[5]: Cross cluster correction enable Bit[4]: Horizontal same color plane couplet correction enable 0: Disable 1: Enable Bit[3]: Horizontal couplet correction enable 0: Disable 1: Enable Bit[2]: Not used Bit[1]: r_bwsnr_en Bit[0]: Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on the analog gain 1: Manual mode in which defect pixel threshold is set manually by register

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table 3-15 DPC registers (sheet 10 of 26)

address	register name	default value	R/W	description
0x80206241	SNR0_VS_DPC_CTRL01	0xDF	RW	For Sensor 0 Very Short Exposure Bit[7]: Manually set threshold for T-cluster Bit[6]: r_comp_en Bit[5]: Vertical black pixel detection 0: Disable 1: Enable Bit[4]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[3]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable Bit[2]: T-cluster detection 0: Disable 1: Enable Bit[1:0]: Padding method of edge pixels 00: Pad with 0 01: Pad with 255 10: Pad with (255+1)/2 11: Pad with nearby same channel pixel This option will affect defect pixel detection of boundary pixels
0x80206242	SNR0_VS_DPC_CTRL02	0xFF	RW	For Sensor 0 Very Short Exposure Bit[7]: White defect pixel detection 0: Disable 1: Enable Bit[6]: Black defect pixel detection 0: Disable 1: Enable Bit[5:4]: Pixel number threshold for detection of cross-cluster Bit[3:2]: Pixel number threshold for detection of T-cluster Bit[1:0]: Number of vertical connected white pixels removed 00: Remove the upper one white pixel 01: Remove two vertical white pixels 10: Remove three or less vertical connected white pixel 11: Reserved

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table 3-15 DPC registers (sheet 11 of 26)

address	register name	default value	R/W	description
0x80206243	SNR0_VS_DPC_WTHREGLIST1	0x08	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold value for detecting white pixel in manual More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x80206244	SNR0_VS_DPC_WTHREGLIST2	0x20	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold value for detecting black pixel in manual mode More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x80206245	SNR0_VS_DPC_THRE1	0x10	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold value used in recovery of defect pixel for long channel The bigger the value, the more details retained, but the less effective of recovering defect
0x80206246	SNR0_VS_DPC_THRE2	0x20	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold for registering defect pixel to detect cross cluster for long channel. The greater the threshold, the more defect pixels will be removed
0x80206247	SNR0_VS_DPC_THRE3	0x10	RW	For Sensor 0 Very Short Exposure Bit[7:0]: Threshold to determine high frequency area where the DPC will keep the fine details for long channel The greater the threshold, the more details will be removed by DPC
0x80206248	SNR0_VS_DPC_THRE4	0x18	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold for detecting horizontal couplet for long channel This threshold should be greater than the threshold for single while/black pixel
0x80206249	SNR0_VS_DPC_WTHRE_LIST0	0x08	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 0 in auto mode

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table 3-15 DPC registers (sheet 12 of 26)

address	register name	default value	R/W	description
0x8020624A	SNR0_VS_DPC_ WTHRE_LIST1	0x04	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 1 in auto mode
0x8020624B	SNR0_VS_DPC_ WTHRE_LIST2	0x02	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 2 in auto mode
0x8020624C	SNR0_VS_DPC_ WTHRE_LIST3	0x02	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 3 in auto mode
0x8020624D	SNR0_VS_DPC_ BTHRE_LIST0	0x0C	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 0 in auto mode
0x8020624E	SNR0_VS_DPC_ BTHRE_LIST1	0x06	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 1 in auto mode
0x8020624F	SNR0_VS_DPC_ BTHRE_LIST2	0x02	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 2 in auto mode
0x80206250	SNR0_VS_DPC_ BTHRE_LIST3	0x02	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 3 in auto mode
0x80206251	SNR0_VS_DPC_ SAT	0xFF	RW	For Sensor 0 Very Short Exposure Bit[7:0]: Threshold of the center pixel for saturation type of cross cluster To qualify a saturation type of cross cluster, the center pixel must be greater than this threshold
0x80206252	SNR0_VS_DPC_ VB_GAIN_TH1	0x07	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Vertical black pixel detection threshold 1
0x80206253	SNR0_VS_DPC_ VB_GAIN_TH2	0x03	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Vertical black pixel detection threshold 2
0x80206254	SNR0_VS_DPC_ SMOOTH_ GLIST0	0x03	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Smooth gain list 0
0x80206255	SNR0_VS_DPC_ SMOOTH_ GLIST1	0x07	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Smooth gain list 1
0x80206256	SNR0_VS_DPC_ SMOOTH_ GLIST2	0x0F	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Smooth gain list 2

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table 3-15 DPC registers (sheet 13 of 26)

address	register name	default value	R/W	description
0x80206257	SNR0_VS_DPC _SMGAIN_TH1	0x07	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC smooth gain threshold 1
0x80206258	SNR0_VS_DPC _SMGAIN_TH2	0x03	RW	For Sensor 0 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC smooth gain threshold 2
0x80206259	SNR0_VS_DPC_ UNSAT	0xF0	RW	For Sensor 0 Very Short Exposure Bit[7:0]: Threshold of un-saturation level for detection of cross-cluster and T-cluster
0x8020625A	SNR0_VS_DPC_ TTHRE	0x08	RW	For Sensor 0 Very Short Exposure Bit[7:0]: Threshold to determine a cross-cluster and T-cluster

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table 3-15 DPC registers (sheet 14 of 26)

address	register name	default value	R/W	description
0x80206280	SNR1_L_DPC_CTRL00	0x18	RW	Sensor 1 Long Exposure DPC Control Bit[7]: m_bEnableTail Tail type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: m_bEnableSaturateCC Saturation type cross cluster correction enable, works only when cross cluster correction is 0: Disable 1: Enable Bit[5]: m_bEnableCrossCluster Cross cluster correction enable Bit[4]: m_bEnableSameChannelConnected Horizontal same color plane couplet correction enable 0: Disable 1: Enable Bit[3]: m_bEnableDiffChannelConnected Horizontal couplet correction enable 0: Disable 1: Enable Bit[2]: m_bEnableSmooth Bit[1]: m_bBWSensorEnable Bit[0]: m_bManualmode Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on the analog gain 1: Manual mode in which defect pixel threshold is set manually by register

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table 3-15 DPC registers (sheet 15 of 26)

address	register name	default value	R/W	description
0x80206281	SNR1_L_DPC_CTRL01	0xDF	RW	Sensor 1 Long Exposure DPC Control Bit[7]: Set threshold for T-cluster 0: Automatically 1: Manually Bit[6]: r_comp_en Bit[5]: Vertical black pixel detection 0: Disable 1: Enable Bit[4]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[3]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable Bit[2]: T-cluster detection 0: Disable 1: Enable Bit[1:0]: Padding method of edge pixels 00: Pad with 0 01: Pad with 255 10: Pad with (255+1)/2 11: Pad with nearby same channel pixel This option will affect defect pixel detection of boundary pixels
0x80206282	SNR0_L_DPC_CTRL02	0xFF	RW	Sensor 1 Long Exposure DPC Control Bit[7]: White defect pixel detection 0: Disable 1: Enable Bit[6]: Black defect pixel detection 0: Disable 1: Enable Bit[5:4]: Pixel number threshold for detection of cross-cluster Bit[3:2]: Pixel number threshold for detection of T-cluster Bit[1:0]: Number of vertical connected white pixels removed 00: Remove the upper one white pixel 01: Remove two vertical white pixels 10: Remove three or less vertical connected white pixel 11: Reserved

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table 3-15 DPC registers (sheet 16 of 26)

address	register name	default value	R/W	description
0x80206283	SNR1_L_DPC_ WTHRE	0x08	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: Threshold value for detecting white pixel in manual More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x80206284	SNR1_L_DPC_ BTHRE	0x20	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: Threshold value for detecting black pixel in manual mode More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x80206285	SNR1_L_DPC_ THRE1	0x10	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: Threshold value used in recovery of defect pixel for long channel The bigger the value, the more details retained, but the less effective of recovering defect
0x80206286	SNR1_L_DPC_ THRE2	0x20	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: Threshold for registering defect pixel to detect cross cluster for long channel The greater the threshold, the more defect pixels will be removed
0x80206287	SNR1_L_DPC_ THRE3	0x10	RW	For Sensor 1 Long Exposure Bit[7:0]: Threshold to determine high frequency area where the DPC will keep the fine details for long channel The greater the threshold, the more details will be removed by DPC
0x80206288	SNR1_L_DPC_ THRE4	0x18	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: Threshold for detecting horizontal couplet for long channel This threshold should be greater than the threshold for single white/black pixel
0x80206289	SNR1_L_DPC_ WTHRE_LIST0	0x08	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 0 in auto mode

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table 3-15 DPC registers (sheet 17 of 26)

address	register name	default value	R/W	description
0x8020628A	SNR1_L_DPC_ WTHRE_LIST1	0x04	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 1 in auto mode
0x8020628B	SNR1_L_DPC_ WTHRE_LIST2	0x02	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 2 in auto mode
0x8020628C	SNR1_L_DPC_ WTHRE_LIST3	0x02	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 3 in auto mode
0x8020628D	SNR1_L_DPC_ BTHRE_LIST0	0x0C	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 0 in auto mode
0x8020628E	SNR1_L_DPC_ BTHRE_LIST1	0x06	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 1 in auto mode
0x8020628F	SNR1_L_DPC_ BTHRE_LIST2	0x02	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 2 in auto mode
0x80206290	SNR1_L_DPC_ BTHRE_LIST3	0x02	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 3 in auto mode
0x80206291	SNR1_L_DPC_ SAT	0xFF	RW	For Sensor 1 Long Exposure Bit[7:0]: Threshold of the center pixel for saturation type of cross cluster To qualify a saturation type of cross cluster, the center pixel must be greater than this threshold
0x80206292	SNR1_L_DPC_ VB_GAIN_TH1	0x07	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: Vertical black pixel detection threshold 1
0x80206293	SNR1_L_DPC_ VB_GAIN_TH2	0x03	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: Vertical black pixel detection threshold 2
0x80206294	SNR1_L_DPC_ SMOOTH_ GLIST0	0x03	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: Smooth gain list 0
0x80206295	SNR1_L_DPC_ SMOOTH_ GLIST1	0x07	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: Smooth gain list 1
0x80206296	SNR1_L_DPC_ SMOOTH_ GLIST2	0x0F	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: Smooth gain list 2

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table 3-15 DPC registers (sheet 18 of 26)

address	register name	default value	R/W	description
0x80206297	SNR1_L_DPC_SMGAIN_TH1	0x07	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC smooth gain threshold 1
0x80206298	SNR1_L_DPC_SMGAIN_TH2	0x03	RW	For Sensor 1 Long Exposure Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC smooth gain threshold 2
0x80206299	SNR1_L_DPC_UNSAT	0xF0	RW	For Sensor 1 Long Exposure Bit[7:0]: Threshold of un-saturation level for detection of cross-cluster and T-cluster
0x8020629A	SNR1_L_DPC_TTHRE	0x08	RW	For Sensor 1 Long Exposure Bit[7:0]: Threshold to determine a cross-cluster and T-cluster
0x802062A0	SNR1_S_DPC_CTRL00	0x18	RW	For Sensor 1 Short Exposure Bit[7]: Tail type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: Saturation type cross cluster correction enable, works only when cross cluster correction is 0: Disable 1: Enable Bit[5]: Cross cluster correction enable Bit[4]: Horizontal same color plane couplet correction enable 0: Disable 1: Enable Bit[3]: Horizontal couplet correction enable 0: Disable 1: Enable Bit[2]: Not used Bit[1]: r_bwsnr_en Bit[0]: Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on the analog gain 1: Manual mode in which defect pixel threshold is set manually by register

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table 3-15 DPC registers (sheet 19 of 26)

address	register name	default value	R/W	description
0x802062A1	SNR1_S_DPC_CTRL01	0xDF	RW	For Sensor 1 Short Exposure Bit[7]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[6]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable Bit[5]: T-cluster detection 0: Disable 1: Enable Bit[4]: Padding method of edge pixels 00: Pad with 0 01: Pad with 255 10: Pad with (255+1)/2 11: Pad with nearby same channel pixel This option will affect defect pixel detection of boundary pixels. Bit[3]: Vertical black pixel detection 0: Disable 1: Enable Bit[2]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[1:0]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable
0x802062A2	SNR1_S_DPC_CTRL02	0xFF	RW	For Sensor 1 Short Exposure Bit[7]: White defect pixel detection 0: Disable 1: Enable Bit[6]: Black defect pixel detection 0: Disable 1: Enable Bit[5:4]: Pixel number threshold for detection of cross-cluster Bit[3:2]: Pixel number threshold for detection of T-cluster Bit[1:0]: Number of vertical connected white pixels removed: 00: Remove the upper one white pixel 01: Remove two vertical white pixels 10: Remove three or less vertical connected white pixel 11: Reserved

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table 3-15 DPC registers (sheet 20 of 26)

address	register name	default value	R/W	description
0x802062A3	SNR1_S_DPC_WTHRE	0x08	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold value for detecting white pixel in manual More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x802062A4	SNR1_S_DPC_BTHRE	0x20	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold value for detecting black pixel in manual mode More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x802062A5	SNR1_S_DPC_THRE1	0x10	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold value used in recovery of defect pixel for long channel The bigger the value, the more details retained, but the less effective of recovering defect
0x802062A6	SNR1_S_DPC_THRE2	0x20	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold for registering defect pixel to detect cross cluster for long channel The greater the threshold, the more defect pixels will be removed
0x802062A7	SNR1_S_DPC_THRE3	0x10	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold to determine high frequency area where the DPC will keep the fine details for long channel The greater the threshold, the more details will be removed by DPC
0x802062A8	SNR1_S_DPC_THRE4	0x18	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold for detecting horizontal couplet for long channel This threshold should be greater than the threshold for single while/black pixel
0x802062A9	SNR1_S_DPC_WTHRE_LIST0	0x08	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 0 in auto mode

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table 3-15 DPC registers (sheet 21 of 26)

address	register name	default value	R/W	description
0x802062AA	SNR1_S_DPC_WTHRE_LIST1	0x04	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 1 in auto mode
0x802062AB	SNR1_S_DPC_WTHRE_LIST2	0x02	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 2 in auto mode
0x802062AC	SNR1_S_DPC_WTHRE_LIST3	0x02	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 3 in auto mode
0x802062AD	SNR1_S_DPC_BTHRE_LIST0	0x0C	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 0 in auto mode
0x802062AE	SNR1_S_DPC_BTHRE_LIST1	0x06	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 1 in auto mode
0x802062AF	SNR1_S_DPC_BTHRE_LIST2	0x02	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 2 in auto mode
0x802062B0	SNR1_S_DPC_BTHRE_LIST3	0x02	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 3 in auto mode
0x802062B1	SNR1_S_DPC_SAT	0xFF	RW	For Sensor 1 Short Exposure Bit[7:0]: Threshold of the center pixel for saturation type of cross cluster To qualify a saturation type of cross cluster, the center pixel must be greater than this threshold
0x802062B2	SNR1_S_DPC_VB_GAIN_TH1	0x07	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: Vertical black pixel detection threshold 1
0x802062B3	SNR1_S_DPC_VB_GAIN_TH2	0x03	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: Vertical black pixel detection threshold 2
0x802062B4	SNR1_S_DPC_SMOOTH_GLIST0	0x03	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: Smooth gain list 0
0x802062B5	SNR1_S_DPC_SMOOTH_GLIST1	0x07	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: Smooth gain list 1
0x802062B6	SNR1_S_DPC_SMOOTH_GLIST2	0x0F	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: Smooth gain list 2

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table 3-15 DPC registers (sheet 22 of 26)

address	register name	default value	R/W	description
0x802062B7	SNR1_S_DPC_ SMGAIN_GLIST1	0x07	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC smooth gain threshold 1
0x802062B8	SNR1_S_DPC_ SMGAIN_GLIST2	0x03	RW	For Sensor 1 Short Exposure Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC smooth gain threshold 2
0x802062B9	SNR1_S_DPC_ UNSAT	0xF0	RW	For Sensor 1 Short Exposure Bit[7:0]: Threshold of un-saturation level for detection of cross-cluster and T-cluster
0x802062BA	SNR1_S_DPC_ TTHRE	0x08	RW	For Sensor 1 Short Exposure Bit[7:0]: Threshold to determine a cross-cluster and T-cluster
0x802062C0	SNR1_VS_DPC_ CTRL00	0x18	RW	For Sensor 1 Very Short Exposure Bit[7]: Tail type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: Saturation type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[5]: Cross cluster correction enable Bit[4]: Horizontal same color plane couplet correction enable 0: Disable 1: Enable Bit[3]: Horizontal couplet correction enable 0: Disable 1: Enable Bit[2]: Not used Bit[1]: r_bwsnr_en Bit[0]: Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on the analog gain 1: Manual mode in which defect pixel threshold is set manually by register

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table 3-15 DPC registers (sheet 23 of 26)

address	register name	default value	R/W	description
0x802062C1	SNR1_VS_DPC_CTRL01	0xDF	RW	For Sensor 1 Very Short Exposure Bit[7]: Manually set threshold for T-cluster Bit[6]: r_comp_en Bit[5]: Vertical black pixel detection 0: Disable 1: Enable Bit[4]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[3]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable Bit[2]: T-cluster detection 0: Disable 1: Enable Bit[1:0]: Padding method of edge pixels 00: Pad with 0 01: Pad with 255 10: Pad with (255+1)/2 11: Pad with nearby same channel pixel This option will affect defect pixel detection of boundary pixels
0x802062C2	SNR1_VS_DPC_CTRL02	0xFF	RW	For Sensor 1 Very Short Exposure Bit[7]: White defect pixel detection 0: Disable 1: Enable Bit[6]: Black defect pixel detection 0: Disable 1: Enable Bit[5:4]: Pixel number threshold for detection of cross-cluster Bit[3:2]: Pixel number threshold for detection of T-cluster Bit[1:0]: Number of vertical connected white pixels removed: 00: Remove the upper one white pixel 01: Remove two vertical white pixels 10: Remove three or less vertical connected white pixel 11: Reserved

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table 3-15 DPC registers (sheet 24 of 26)

address	register name	default value	R/W	description
0x802062C3	SNR1_VS_DPC_WTHREGLIST1	0x08	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold value for detecting white pixel in manual More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x802062C4	SNR1_VS_DPC_WTHREGLIST2	0x20	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold value for detecting black pixel in manual mode More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x802062C5	SNR1_VS_DPC_THRE1	0x10	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold value used in recovery of defect pixel for long channel The bigger the value, the more details retained, but the less effective of recovering defect
0x802062C6	SNR1_VS_DPC_THRE2	0x20	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold for registering defect pixel to detect cross cluster for long channel The greater the threshold, the more defect pixels will be removed
0x802062C7	SNR1_VS_DPC_THRE3	0x10	RW	For Sensor 1 Very Short Exposure Bit[7:0]: Threshold to determine high frequency area where the DPC will keep the fine details for long channel The greater the threshold, the more details will be removed by DPC
0x802062C8	SNR1_VS_DPC_THRE4	0x18	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Threshold for detecting horizontal couplet for long channel This threshold should be greater than the threshold for single while/black pixel
0x802062C9	SNR1_VS_DPC_WTHRE_LIST0	0x08	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 0 in auto mode

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table 3-15 DPC registers (sheet 25 of 26)

address	register name	default value	R/W	description
0x802062CA	SNR1_VS_DPC_WTHRE_LIST1	0x04	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 1 in auto mode
0x802062CB	SNR1_VS_DPC_WTHRE_LIST2	0x02	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 2 in auto mode
0x802062CC	SNR1_VS_DPC_WTHRE_LIST3	0x02	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: White pixel threshold 3 in auto mode
0x802062CD	SNR1_VS_DPC_BTHRE_LIST0	0x0C	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 0 in auto mode
0x802062CE	SNR1_VS_DPC_BTHRE_LIST1	0x06	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 1 in auto mode
0x802062CF	SNR1_VS_DPC_BTHRE_LIST2	0x02	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 2 in auto mode
0x802062D0	SNR1_VS_DPC_BTHRE_LIST3	0x02	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Black pixel threshold 3 in auto mode
0x802062D1	SNR1_VS_DPC_SAT	0xFF	RW	For Sensor 1 Very Short Exposure Bit[7:0]: Threshold of the center pixel for saturation type of cross cluster To qualify a saturation type of cross cluster, the center pixel must be greater than this threshold
0x802062D2	SNR1_VS_DPC_VB_GAIN_TH1	0x07	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Vertical black pixel detection threshold 1
0x802062D3	SNR1_VS_DPC_VB_GAIN_TH2	0x03	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Vertical black pixel detection threshold 2
0x802062D4	SNR1_VS_DPC_SMOOTH_GLIST0	0x03	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Smooth gain list 0
0x802062D5	SNR1_VS_DPC_SMOOTH_GLIST1	0x07	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Smooth gain list 1
0x802062D6	SNR1_VS_DPC_SMOOTH_GLIST2	0x0F	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Smooth gain list 2

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table 3-15 DPC registers (sheet 26 of 26)

address	register name	default value	R/W	description
0x802062D7	SNR1_VS_DPC_SMGAIN_TH1	0x07	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC smooth gain threshold 1
0x802062D8	SNR1_VS_DPC_SMGAIN_TH2	0x03	RW	For Sensor 1 Very Short Exposure Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC smooth gain threshold 2
0x802062D9	SNR1_VS_DPC_UNSAT	0xF0	RW	For Sensor 1 Very Short Exposure Bit[7:0]: Threshold of un-saturation level for detection of cross-cluster and T-cluster
0x802062DA	SNR1_VS_DPC_TTHRE	0x08	RW	For Sensor 1 Very Short Exposure Bit[7:0]: Threshold to determine a cross-cluster and T-cluster

3.11 de-noise (DNS)

In image processing, noise is the most important factor when measuring image quality. There are several steps to reduce noise in the OV490 image pipeline and each de-noise stage is designed to reduce different noise. Based on their stages in the pipeline, they can be classified into two classes: linear domain DNS and after gamma DNS.

RAW DNS is the first step in linear domain DNS. Because the AWB gain often amplifies the noise in R/B channels, the RAW DNS is mainly designed to reduce noise in R/B channel before color interpolation. It can reduce the noise in green channel, but it may remove too much detail and the raw image may lose more sharpness. So, it is not recommended to reduce green channel noise in RAW DNS unless the sensor noise on raw image is very large.

CIP-denoise is the second step in linear domain DNS, which is designed to reduce noise in the green channel during color interpolation. Because CIP is edge adaptive, it can maintain sharp edges better than the RAW DNS function on green channel.

Because the color matrix and gamma curve will amplify noise, which is mainly in low frequency after the linear domain DNS, the gamma DNS modules (UV DNS) is designed to remove low frequency noise in Y and UV channels. UVDNS is the second step DNS after gamma, which is designed to reduce UV noise.

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3.11.1 noise list

Noise levels increase with sensor AGC gain, which makes the DNS module increase the de-noise level when gain changes. All DNS modules have the same logic to auto adjust the de-noise level with sensor AGC gain: an 8-step noise list which defines the de-noise levels that are used when the sensor AGC gain is x1, x2, x4, x8, x16, x32, x64 or x128. If the AGC gain is in between two steps, the real de-noise level will be linearly interpolated between two steps. Each DNS module has its own noise list.

For a further description of RAW DNS and UVDNS, see **section 3.11.2** and **section 3.11.3**. DNS that appears in CIP can be found in **section 3.17.2**.

3.11.2 RAW DNS

Two RAW DNS modules are included in the OV490. One is applied to all three RAW exposure channels before combining (HDR RAW DNS) and the other (OVPB RAW DNS) is used to reduce the noise after combine and tone-mapping.

In HDR RAWDNS, except for the noise list, there are three parameters, which can influence image quality.

- green channel denoising
  There is an option for choosing G position pixels to be involved in denoise, enabled by registers 0x80206308[4], 0x80206312[4], and 0x8020631C[4] for L,S and VS, respectively. Note that enabling the green channel denoising may remove image details and result in a blurry image. Unless the sensor noise level is very high, it is recommended to disable green channel denoising.
- noise Y slop signal
  There is an option to increase the DNS level with the signal level, adjusted by registers 0x80206308[3:0], 0x80206312[3:0], and 0x8020631C[3:0] for L, S and VS, respectively. In the linear domain, shot noise increases with signal level, so for a linear raw image, the dark tone has a lower noise level than mid tone and light tone. A larger value will reduce more noise in light tone.
- maximum edge threshold
  There is an option to preserve color edges in low light conditions, adjusted by registers 0x80206309, 0x80206313, and 0x8020631D for L, S and VS, respectively. A smaller value will preserve color edges, but will also remove less noise in R/B channels.

For HDR raw DNS, it is applied to three exposure channels, separately.

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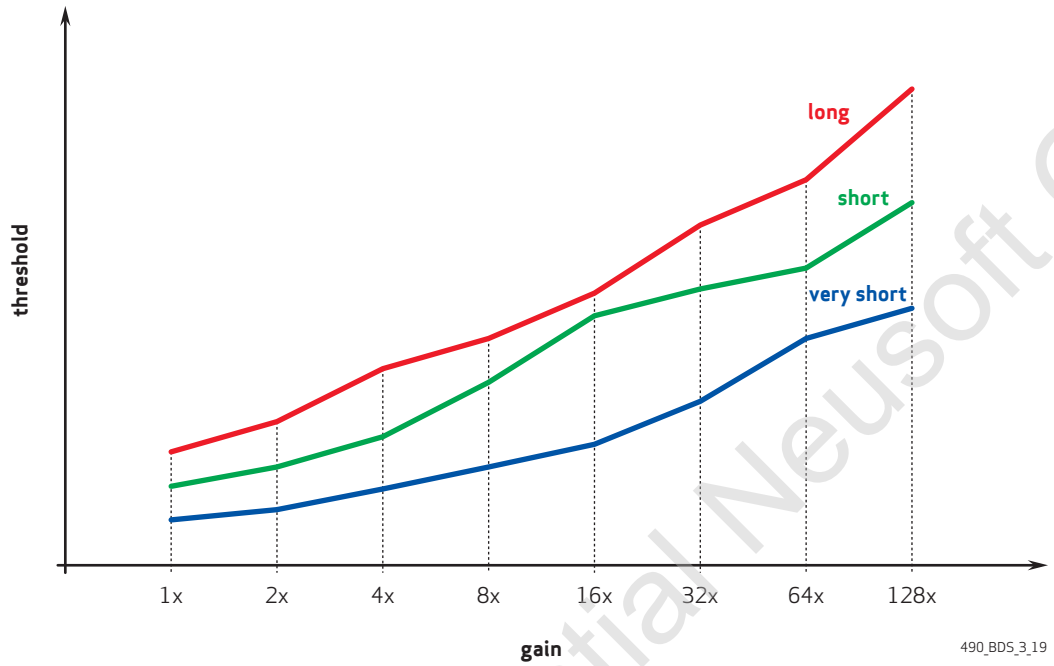
figure 3-19 HDR RAW DNS diagram



HDR RAW DNS noise threshold registers:

- 0x80206300~0x80206307 (0x80206330~0x80206337 for second sensor) for L channel
- 0x8020630A~0x80206311 (0x8020633A~0x80206341 for second sensor) for S channel
- 0x80206314~0x8020631B (0x80206344~0x8020634B for second sensor) for VS channel

The OVPB RAW DNS is applied after combination and uses the same denoise level for all three channels (L, S, VS).

OVPB RAW DNS threshold registers:

- 0x80206381~0x80206388 (0x80206391~0x80206398 for second sensor)

table 3-16 HDR RAW DNS control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x80206010	SNR0_ISP_CTRL_0	0xF7	RW	Bit[6]: Sensor 0 HDR DNS enable 0: HDR RAW DNS disable 1: HDR RAW DNS enable
0x80206030	SNR1_ISP_CTRL_0	0xF7	RW	Bit[6]: Sensor 1 HDR DNS enable 0: HDR RAW DNS disable 1: HDR RAW DNS enable

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table 3-16 HDR RAW DNS control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x80206300	SNR0_DNS_NOISE LIST0_L	0x04	RW	Bit[7:0]: Sensor 0 noise list 0 for long exposure
0x80206301	SNR0_DNS_NOISE LIST1_L	0x08	RW	Bit[7:0]: Sensor 0 noise list 1 for long exposure
0x80206302	SNR0_DNS_NOISE LIST2_L	0x10	RW	Bit[7:0]: Sensor 0 noise list 2 for long exposure
0x80206303	SNR0_DNS_NOISE LIST3_L	0x18	RW	Bit[7:0]: Sensor 0 noise list 3 for long exposure
0x80206304	SNR0_DNS_NOISE LIST4_L	0x20	RW	Bit[7:0]: Sensor 0 noise list 4 for long exposure
0x80206305	SNR0_DNS_NOISE LIST5_L	0x30	RW	Bit[7:0]: Sensor 0 noise list 5 for long exposure
0x80206306	SNR0_DNS_NOISE LIST6_L	0x40	RW	Bit[7:0]: Sensor 0 noise list 6 for long exposure
0x80206307	SNR0_DNS_NOISE LIST7_L	0x40	RW	Bit[7:0]: Sensor 0 noise list 7 for long exposure
0x80206308	SNR0_DNS_CTL_ BITS_L	0x04	RW	Sensor 0 Long Exposure Channel Control Bit[7:5]: Reserved Bit[4]: G point denoise enable (m_bGDNSEnable) Bit[3:0]: NoiseYSlop (m_nNoiseYSlope)
0x80206309	SNR0_DNS_MAX_ EDGE_THRE_L	0x3F	RW	Bit[7:0]: Sensor 0 maximum edge threshold for long exposure
0x8020630A	SNR0_DNS_NOISE LIST0_S	0x04	RW	Bit[7:0]: Sensor 0 noise list 0 for short exposure
0x8020630B	SNR0_DNS_NOISE LIST1_S	0x08	RW	Bit[7:0]: Sensor 0 noise list 1 for short exposure
0x8020630C	SNR0_DNS_NOISE LIST2_S	0x10	RW	Bit[7:0]: Sensor 0 noise list 2 for short exposure
0x8020630D	SNR0_DNS_NOISE LIST3_S	0x18	RW	Bit[7:0]: Sensor 0 noise list 3 for short exposure
0x8020630E	SNR0_DNS_NOISE LIST4_S	0x20	RW	Bit[7:0]: Sensor 0 noise list 4 for short exposure
0x8020630F	SNR0_DNS_NOISE LIST5_S	0x30	RW	Bit[7:0]: Sensor 0 noise list 5 for short exposure
0x80206310	SNR0_DNS_NOISE LIST6_S	0x40	RW	Bit[7:0]: Sensor 0 noise list 6 for short exposure

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table 3-16 HDR RAW DNS control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x80206311	SNR0_DNS_NOISE LIST7_S	0x40	RW	Bit[7:0]: Sensor 0 noise list 7 for short exposure
0x80206312	SNR0_DNS_CTL_ BITS_S	0x04	RW	Sensor 0 Short Exposure Channel Control Bit[7:5]: Reserved Bit[4]: G point denoise enable (m_bGDNSEnable) Bit[3:0]: NoiseYSlop (m_nNoiseYSlope)
0x80206313	SNR0_DNS_MAX_ EDGE_ THRE_S	0x3F	RW	Bit[7:0]: Sensor 0 maximum edge threshold for short exposure
0x80206314	SNR0_DNS_NOISE LIST0_VS	0x04	RW	Bit[7:0]: Sensor 0 noise list 0 for very short exposure
0x80206315	SNR0_DNS_NOISE LIST1_VS	0x08	RW	Bit[7:0]: Sensor 0 noise list 1 for very short exposure
0x80206316	SNR0_DNS_NOISE LIST2_VS	0x10	RW	Bit[7:0]: Sensor 0 noise list 2 for very short exposure
0x80206317	SNR0_DNS_NOISE LIST3_VS	0x18	RW	Bit[7:0]: Sensor 0 noise list 3 for very short exposure
0x80206318	SNR0_DNS_NOISE LIST4_VS	0x20	RW	Bit[7:0]: Sensor 0 noise list 4 for very short exposure
0x80206319	SNR0_DNS_NOISE LIST5_VS	0x30	RW	Bit[7:0]: Sensor 0 noise list 5 for very short exposure
0x8020631A	SNR0_DNS_NOISE LIST6_VS	0x40	RW	Bit[7:0]: Sensor 0 noise list 6 for very short exposure
0x8020631B	SNR0_DNS_NOISE LIST7_VS	0x40	RW	Bit[7:0]: Sensor 0 noise list 7 for very short exposure
0x8020631C	SNR0_DNS_CTL_ BITS_VS	0x04	RW	Sensor 0 Very Short Exposure Channel Control Bit[7:5]: Reserved Bit[4]: G point denoise enable (m_bGDNSEnable) Bit[3:0]: m_nNoiseYSlope
0x8020631D	SNR0_DNS_MAX_ EDGE_THRE_VS	0x3F	RW	Bit[7:0]: Sensor 0 maximum edge threshold for very short exposure
0x80206330	SNR1_DNS_NOISE LIST0_L	0x04	RW	Bit[7:0]: Sensor 1 noise list 0 for long exposure
0x80206331	SNR1_DNS_NOISE LIST1_L	0x08	RW	Bit[7:0]: Sensor 1 noise list 1 for long exposure
0x80206332	SNR1_DNS_NOISE LIST2_L	0x10	RW	Bit[7:0]: Sensor 1 noise list 2 for long exposure

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table 3-16 HDR RAW DNS control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x80206333	SNR1_DNS_NOISE LIST3_L	0x18	RW	Bit[7:0]: Sensor 1 noise list 3 for long exposure
0x80206334	SNR1_DNS_NOISE LIST4_L	0x20	RW	Bit[7:0]: Sensor 1 noise list 4 for long exposure
0x80206335	SNR1_DNS_NOISE LIST5_L	0x30	RW	Bit[7:0]: Sensor 1 noise list 5 for long exposure
0x80206336	SNR1_DNS_NOISE LIST6_L	0x40	RW	Bit[7:0]: Sensor 1 noise list 6 for long exposure
0x80206337	SNR1_DNS_NOISE LIST7_L	0x40	RW	Bit[7:0]: Sensor 1 noise list 7 for long exposure
0x80206338	SNR1_DNS_CTL_ BITS_L	0x04	RW	Sensor 1 Long Exposure Channel Control Bit[7:5]: Reserved Bit[4]: G point denoise enable (m_bGDNSEnable) Bit[3:0]: m_nNoiseYSlope
0x80206339	SNR1_DNS_MAX_ EDGE_THRE_L	0x3F	RW	Bit[7:0]: Sensor 1 maximum edge threshold for long exposure
0x8020633A	SNR1_DNS_NOISE LIST0_S	0x04	RW	Bit[7:0]: Sensor 1 noise list 0 for short exposure
0x8020633B	SNR1_DNS_NOISE LIST1_S	0x08	RW	Bit[7:0]: Sensor 1 noise list 1 for short exposure
0x8020633C	SNR1_DNS_NOISE LIST2_S	0x10	RW	Bit[7:0]: Sensor 1 noise list 2 for short exposure
0x8020633D	SNR1_DNS_NOISE LIST3_S	0x18	RW	Bit[7:0]: Sensor 1 noise list 3 for short exposure
0x8020633E	SNR1_DNS_NOISE LIST4_S	0x20	RW	Bit[7:0]: Sensor 1 noise list 4 for short exposure
0x8020633F	SNR1_DNS_NOISE LIST5_S	0x30	RW	Bit[7:0]: Sensor 1 noise list 5 for short exposure
0x80206340	SNR1_DNS_NOISE LIST6_S	0x40	RW	Bit[7:0]: Sensor 1 noise list 6 for short exposure
0x80206341	SNR1_DNS_NOISE LIST7_S	0x40	RW	Bit[7:0]: Sensor 1 noise list 7 for short exposure
0x80206342	SNR1_DNS_CTRL_ BITS_S	0x04	RW	Sensor 1 Short Exposure Channel Control Bit[7:5]: Reserved Bit[4]: G point denoise enable (m_bGDNSEnable) Bit[3:0]: m_nNoiseYSlope

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table 3-16 HDR RAW DNS control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x80206343	SNR1_DNS_MAX_EDGE_THRE_S	0x3F	RW	Bit[7:0]: Sensor 1 maximum edge threshold for short exposure
0x80206344	SNR1_DNS_NOISE LIST0_VS	0x04	RW	Bit[7:0]: Sensor 1 noise list 0 for very short exposure
0x80206345	SNR1_DNS_NOISE LIST1_VS	0x08	RW	Bit[7:0]: Sensor 1 noise list 1 for very short exposure
0x80206346	SNR1_DNS_NOISE LIST2_VS	0x10	RW	Bit[7:0]: Sensor 1 noise list 2 for very short exposure
0x80206347	SNR1_DNS_NOISE LIST3_VS	0x18	RW	Bit[7:0]: Sensor 1 noise list 3 for very short exposure
0x80206348	SNR1_DNS_NOISE LIST4_VS	0x20	RW	Bit[7:0]: Sensor 1 noise list 4 for very short exposure
0x80206349	SNR1_DNS_NOISE LIST5_VS	0x30	RW	Bit[7:0]: Sensor 1 noise list 5 for very short exposure
0x8020634A	SNR1_DNS_NOISE LIST6_VS	0x40	RW	Bit[7:0]: Sensor 1 noise list 6 for very short exposure
0x8020634B	SNR1_DNS_NOISE LIST7_VS	0x40	RW	Bit[7:0]: Sensor 1 noise list 7 for very short exposure
0x8020634C	SNR1_DNS_CTRL_BITS_VS	0x04	RW	Sensor 1 Very Short Exposure Channel Control Bit[7:5]: Reserved Bit[4]: G point denoise enable (m_bGDNSEnable) Bit[3:0]: m_nNoiseYSlope
0x8020634D	SNR1_DNS_MAX_EDGE_THRE_VS	0x3F	RW	Bit[7:0]: Sensor 1 maximum edge threshold for very short exposure

table 3-17 OVPB RAW DNS registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x80206011	SNR0_ISP_CTRL_1	0xFF	RW	Bit[7]: Reserved Bit[6]: Sensor 0 OVPB RAW DNS enable 0: OVPB RAW DNS disable 1: OVPB RAW DNS enable

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table 3-17 OVPB RAW DNS registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x80206031	SNR1_ISP_CTRL_1	0xFF	RW	Bit[7]: Reserved Bit[6]: Sensor 1 OVPB RAW DNS enable 0: OVPB RAW DNS disable 1: OVPB RAW DNS enable
0x80206380	SNR0_DNS_CTRL0	0x0D	RW	Sensor 0 Control Bit[7:6]: Reserved Bit[5:2]: m_nNoiseYSlope Bit[1]: Manual noise/edge threshold enable Bit[0]: m_bGDNSEnable
0x80206381	SNR0_DNS_NOISE_LIST_0	0x04	RW	Bit[7:0]: Sensor 0 noise list 0
0x80206382	SNR0_DNS_NOISE_LIST_1	0x08	RW	Bit[7:0]: Sensor 0 noise list 1
0x80206383	SNR0_DNS_NOISE_LIST_2	0x10	RW	Bit[7:0]: Sensor 0 noise list 2
0x80206384	SNR0_DNS_NOISE_LIST_3	0x18	RW	Bit[7:0]: Sensor 0 noise list 3
0x80206385	SNR0_DNS_NOISE_LIST_4	0x20	RW	Bit[7:0]: Sensor 0 noise list 4
0x80206386	SNR0_DNS_NOISE_LIST_5	0x30	RW	Bit[7:0]: Sensor 0 noise list 5
0x80206387	SNR0_DNS_NOISE_LIST_6	0x40	RW	Bit[7:0]: Sensor 0 noise list 6
0x80206388	SNR0_DNS_NOISE_LIST_7	0x40	RW	Bit[7:0]: Sensor 0 noise list 7
0x80206389	SNR0_DNS_MAX_EDGE THRE	0xFF	RW	Bit[7:0]: Sensor 0 maximum edge threshold
0x8020638A	SNR0_DNS_NOISE_MAN	0x08	RW	Bit[7:0]: Sensor 0 manual noise level
0x8020638B	SNR0_DNS_EDGETHRE_ MAN	0x18	RW	Bit[7:0]: Sensor 0 manual edge threshold
0x8020638C	SNR0_DNS_NOISE	–	R	Bit[7:0]: Sensor 0 noise
0x8020638D	SNR0_DNS_EDGETHRE	–	R	Bit[7:0]: Sensor 0 edge threshold
0x80206390	SNR1_DNS_CTRL0	0x0D	RW	Sensor 1 Control Bit[7:6]: Reserved Bit[5:2]: m_nNoiseYSlope Bit[1]: Manual noise/edge threshold enable Bit[0]: m_bGDNSEnable
0x80206391	SNR1_DNS_NOISE_LIST_0	0x04	RW	Bit[7:0]: Sensor 1 noise list 0
0x80206392	SNR1_DNS_NOISE_LIST_1	0x08	RW	Bit[7:0]: Sensor 1 noise list 1
0x80206393	SNR1_DNS_NOISE_LIST_2	0x10	RW	Bit[7:0]: Sensor 1 noise list 2

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table 3-17 OVPB RAW DNS registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x80206394	SNR1_DNS_NOISE_LIST_3	0x18	RW	Bit[7:0]: Sensor 1 noise list 3
0x80206395	SNR1_DNS_NOISE_LIST_4	0x20	RW	Bit[7:0]: Sensor 1 noise list 4
0x80206396	SNR1_DNS_NOISE_LIST_5	0x30	RW	Bit[7:0]: Sensor 1 noise list 5
0x80206397	SNR1_DNS_NOISE_LIST_6	0x40	RW	Bit[7:0]: Sensor 1 noise list 6
0x80206398	SNR1_DNS_NOISE_LIST_7	0x40	RW	Bit[7:0]: Sensor 1 noise list 7
0x80206399	SNR1_DNS_MAX_EDGE THRE	0xFF	RW	Bit[7:0]: Sensor 1 maximum edge threshold
0x8020639A	SNR1_DNS_NOISE_MAN	0x08	RW	Bit[7:0]: Sensor 1 manual noise level
0x8020639B	SNR1_DNS_EDGETHRE_ MAN	0x18	RW	Bit[7:0]: Sensor 1 manual edge threshold
0x8020639C	SNR1_DNS_NOISE	–	R	Bit[7:0]: Sensor 1 noise
0x8020639D	SNR1_DNS_EDGETHRE	–	R	Bit[7:0]: Sensor 1 edge threshold

3.11.3 UVDNS

UVDNS is designed to reduce UV noise in the YUV domain. Besides the noise list, the shadow extra noise (0x80207D08[4:0] for first sensor and 0x80207D18[4:0] for the second sensor) is used to increase the de-noise level in dark tones.

When UV DNS auto mode is enabled, that is the 0x80207D08[5] = 0, it will increase the de-noise level by register 0x80207D08[4:0] in the dark zone. The current UV DNS value can be read from register 0x80207D0A.

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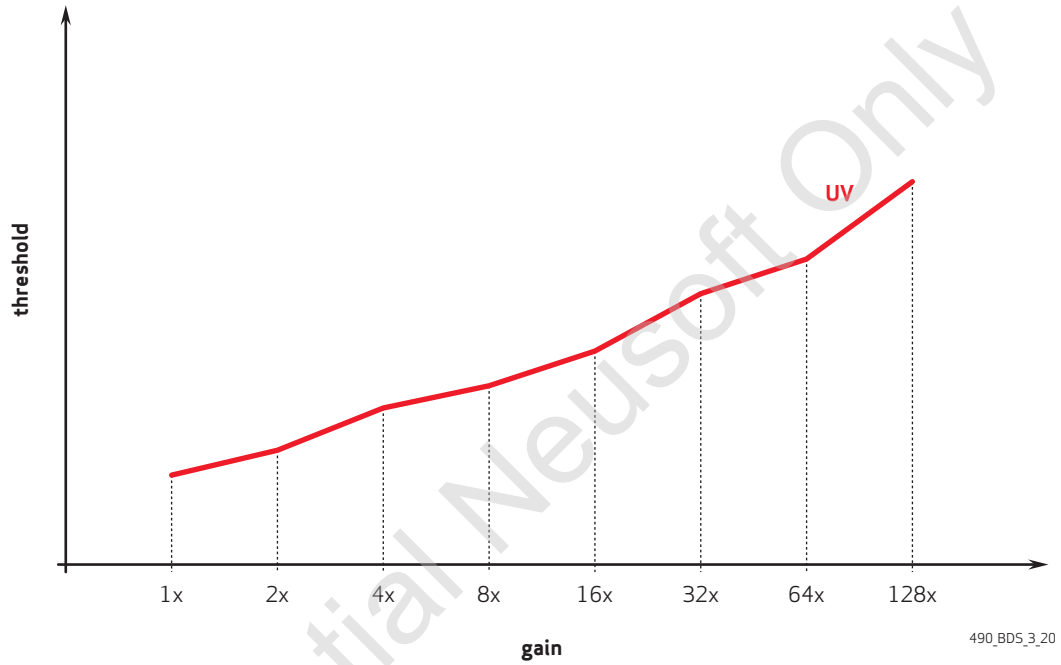
figure 3-20 UV DNS diagram



UV DNS noise threshold list registers are as below: 0x80207D00~0x80207D07 (0x80207D10~0x80207D17 for second sensor).

table 3-18 UV DNS control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x80206012	SNR0_ISP_CTRL_2	0xFF	RW	Bit[5]: Sensor 0 UV DNS enable 0: UV DNS disable 1: UV DNS enable
0x80206032	SNR1_ISP_CTRL_2	0xFF	RW	Bit[5]: Sensor 1 UV DNS enable 0: UV DNS disable 1: UV DNS enable
0x80207D00	SNR0_UVDNS_ NOISE_LIST_0	0x01	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 noise list 0
0x80207D01	SNR0_UVDNS_ NOISE_LIST_1	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 noise list 1
0x80207D02	SNR0_UVDNS_ NOISE_LIST_2	0x04	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 noise list 2
0x80207D03	SNR0_UVDNS_ NOISE_LIST_3	0x08	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 noise list 3

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table 3-18 UV DNS control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x80207D04	SNR0_UVDNS_ NOISE_LIST_4	0x0C	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 noise list 4
0x80207D05	SNR0_UVDNS_ NOISE_LIST_5	0x10	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 noise list 5
0x80207D06	SNR0_UVDNS_ NOISE_LIST_6	0x14	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 noise list 6
0x80207D07	SNR0_UVDNS_ NOISE_LIST_7	0x18	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 noise list 7
0x80207D08	SNR0_UVDNS_CTRL	0x04	RW	Bit[7:6]: Reserved Bit[5]: Manual noise enable Bit[4:0]: Shadow extra noise
0x80207D09	SNR0_UVDNS_MAN_ NOISE	0x0A	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 manual noise
0x80207D0A	SNR0_UVDNS_ NOISE_RO	–	R	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 read out noise
0x80207D10	SNR1_UVDNS_ NOISE_LIST_0	0x01	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 noise list 0
0x80207D11	SNR1_UVDNS_ NOISE_LIST_1	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 noise list 1
0x80207D12	SNR1_UVDNS_ NOISE_LIST_2	0x04	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 noise list 2
0x80207D13	SNR1_UVDNS_ NOISE_LIST_3	0x08	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 noise list 3
0x80207D14	SNR1_UVDNS_ NOISE_LIST_4	0x0C	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 noise list 4
0x80207D15	SNR1_UVDNS_ NOISE_LIST_5	0x10	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 noise list 5
0x80207D16	SNR1_UVDNS_ NOISE_LIST_6	0x14	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 noise list 6
0x80207D17	SNR1_UVDNS_ NOISE_LIST_7	0x18	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 noise list 7
0x80207D18	SNR1_UVDNS_CTRL	0x04	RW	Bit[7:6]: Reserved Bit[5]: Manual noise enable Bit[4:0]: Shadow extra noise
0x80207D19	SNR1_UVDNS_MAN_ NOISE	0x0A	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 manual noise
0x80207D1A	SNR1_UVDNS_ NOISE_RO	–	R	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 read out noise

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3.12 combine

The combine module will combine the L, S and VS channels to a single exposure channel with extended bit depth. It is enabled by default and can be disabled by register 0x80206011[0] (0x80206031[0] for second sensor).

To prepare data for HDR processing, a simple color interpolation procedure (simple CIP) is used. It can recover the R,G,B, and Y information for each point.

Y is calculated from BGR:

Y = (B+G×2+R)>>2.

The combination result gives a combined weighted average of long, short and very short input. To bring the short channel to the same scale as the long channel for combination, the short channel image is multiplied by the exposure ratio of the long channel to the short channel, including the sensitivity ratio.

The combination weights are interpolated from a 2D lookup table based on luminance of long, short and very short channels (see **figure 3-21**).

The grid of long and short channel luminance threshold values are defined by registers 0x80206801~0x80206803.

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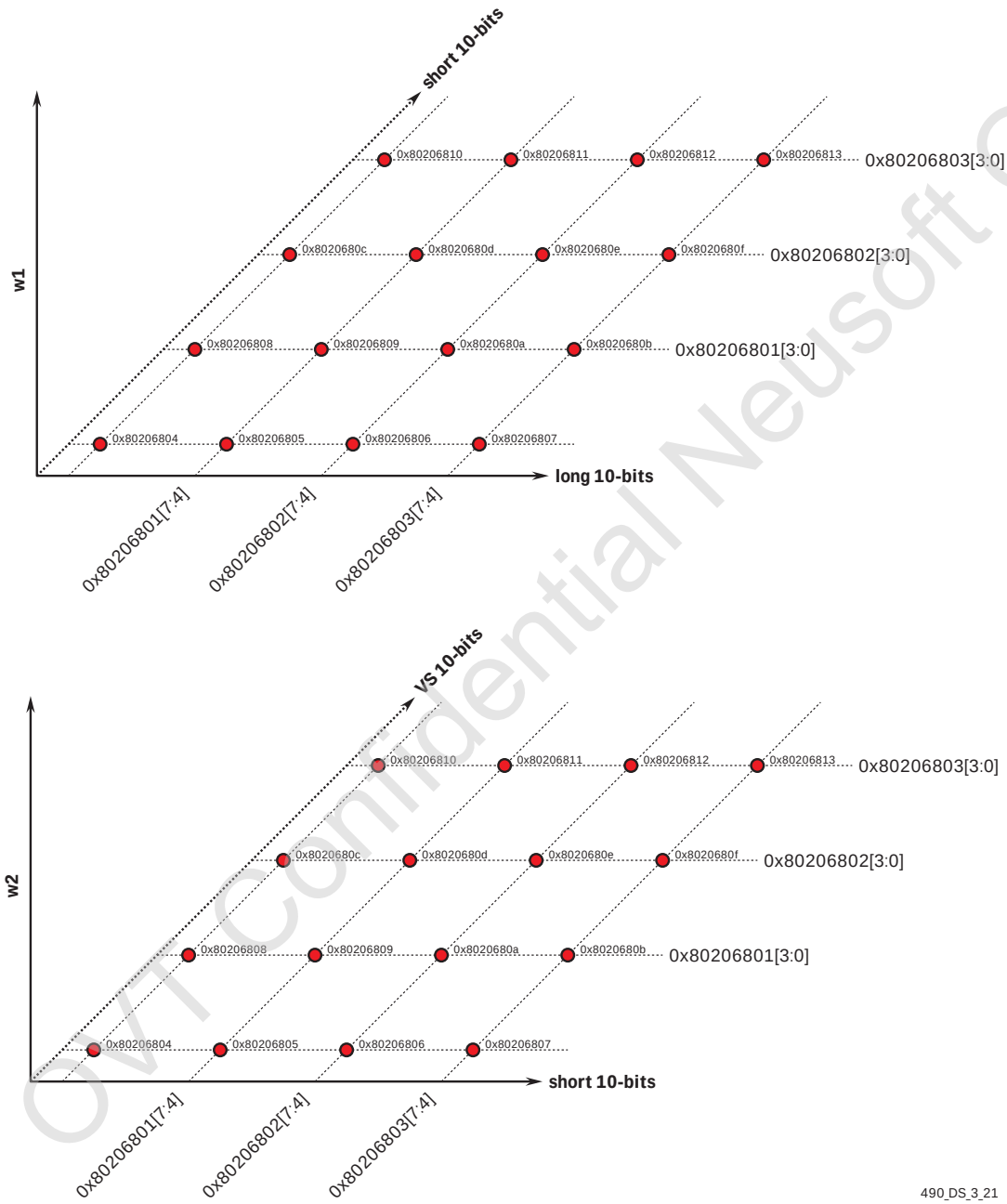
figure 3-21 combination weight graph



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For three exposure mode:

D = DL×W1 + DS×(1-W1)×W2 + DVS×(1-W1)(1-W2)

For LS exposure mode:

D = DL×W1 + DS×(1-W1)

For LVS exposure mode:

D = DL×W1 + DvS×(1-W1)

W1 is the weight between L and S (VS in LVS exposure mode).

W2 is the weight between S and VS (only available in three exposure mode).

D denotes the exposure data.

The weighting varies from pixel to pixel and W1 and W2 is interpolated from a look up table.The two channels with the best SNR are combined for each pixel. So, the combination is either between L and S, or S and VS.

In three exposure mode, there are four different combine modes. This is controlled by register 0x80206800[1:0] (0x80206880[1:0] for the second sensor):

- 0: HDR combine, D=DL×W1 + DS×(1-W1)×W2 + DVS×(1-W1)(1-W2);
- 1: select long, D=DL, W1=1, W2=0
- 2: select short, D=DS, W1=0, W2=1
- 3: select very short, D=DVS, W1=0, W2=0

In order to cancel QE difference between long and short pixel, a color matrix correction may be applied to S channel before combination by setting register 0x80206800[3] =1 (0x80206880[3] for the second sensor).

If current RAW data is blue, then PreCMX will be:

D' = MBB×B + MBG×G+MBR×R;

DSnew = DS - BS + D';

The same process is used for green and red points of short exposure channel.

There are a number of parameters to adjust in the combine and tone mapping processing to get the best image quality for high dynamic range usage. Default values give a good overall HDE performance, but tuning can be done for special cases. Please contact your regional OmniVision FAE for assistance.

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table 3-19 combine control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x80206011	SNR0_ISP_CTRL_1	0xFF	RW	Bit[0]: Sensor 0 combine enable 0: Combine disable 1: Combine
0x80206031	SNR1_ISP_CTRL_1	0xFF	RW	Bit[0]: Sensor 1 combine enable 0: Combine disable 1: Combine
0x80206800	SNR0_COMBINE_CTRL	0x1C	RW	Sensor 0 Combine Control Signals Bit[7:5]: Reserved Bit[4]: Y 2x2 compensate error enable Bit[3]: S channel pre matrix enable Bit[2]: Compensate error enable Bit[1:0]: Combine work mode 00: HDRXCombine 01: HDRLong 10: HDRShort 11: HDRVShort
0x80206801	SNR0_COMBINE_THRE_0	0x95	RW	Bit[7:4]: Sensor 0 combine threshold 0 for long Bit[3:0]: Sensor 0 combine threshold 0 for short
0x80206802	SNR0_COMBINE_THRE_1	0xA8	RW	Bit[7:4]: Sensor 0 combine threshold 1 for long Bit[3:0]: Sensor 0 combine threshold 1 for short
0x80206803	SNR0_COMBINE_THRE_2	0xAA	RW	Bit[7:4]: Sensor 0 combine threshold 2 for long Bit[3:0]: Sensor 0 combine threshold 2 for short
0x80206804	SNR0_COMBINE_WEIGHT_0_0	0x80	RW	Bit[7:0]: Sensor 0 combine weight[0][0]
0x80206805	SNR0_COMBINE_WEIGHT_0_1	0x80	RW	Bit[7:0]: Sensor 0 combine weight[0][1]
0x80206806	SNR0_COMBINE_WEIGHT_0_2	0x60	RW	Bit[7:0]: Sensor 0 combine weight[0][2]
0x80206807	SNR0_COMBINE_WEIGHT_0_3	0x40	RW	Bit[7:0]: Sensor 0 combine weight[0][3]
0x80206808	SNR0_COMBINE_WEIGHT_1_0	0x00	RW	Bit[7:0]: Sensor 0 combine weight[1][0]
0x80206809	SNR0_COMBINE_WEIGHT_1_1	0x80	RW	Bit[7:0]: Sensor 0 combine weight[1][1]

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table 3-19 combine control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x8020680A	SNR0_COMBINE_WEIGHT_1_2	0x40	RW	Bit[7:0]: Sensor 0 combine weight[1][2]
0x8020680B	SNR0_COMBINE_WEIGHT_1_3	0x20	RW	Bit[7:0]: Sensor 0 combine weight[1][3]
0x8020680C	SNR0_COMBINE_WEIGHT_2_0	0x80	RW	Bit[7:0]: Sensor 0 combine weight[2][0]
0x8020680D	SNR0_COMBINE_WEIGHT_2_1	0x60	RW	Bit[7:0]: Sensor 0 combine weight[2][1]
0x8020680E	SNR0_COMBINE_WEIGHT_2_2	0x00	RW	Bit[7:0]: Sensor 0 combine weight[2][2]
0x8020680F	SNR0_COMBINE_WEIGHT_2_3	0x00	RW	Bit[7:0]: Sensor 0 combine weight[2][3]
0x80206810	SNR0_COMBINE_WEIGHT_3_0	0x80	RW	Bit[7:0]: Sensor 0 combine weight[3][0]
0x80206811	SNR0_COMBINE_WEIGHT_3_1	0x80	RW	Bit[7:0]: Sensor 0 combine weight[3][1]
0x80206812	SNR0_COMBINE_WEIGHT_3_2	0x00	RW	Bit[7:0]: Sensor 0 combine weight[3][2]
0x80206813	SNR0_COMBINE_WEIGHT_3_3	0x00	RW	Bit[7:0]: Sensor 0 combine weight[3][3]
0x80206880	SNR1_COMBINE_CTRL	0x1C	RW	Sensor 1 Combine Control Signals Bit[7:5]: Reserved Bit[4]: Y 2x2 compensate error enable Bit[3]: S channel pre matrix enable Bit[2]: Compensate error enable Bit[1:0]: Combine work mode 00: HDRXCombine 01: HDRLong 10: HDRShort 11: HDRVShort
0x80206881	SNR1_COMBINE_THRE_0	0x95	RW	Bit[7:4]: Sensor 1 combine threshold 0 for long Bit[3:0]: Sensor 1 combine threshold 0 for short
0x80206882	SNR1_COMBINE_THRE_1	0xA8	RW	Bit[7:4]: Sensor 1 combine threshold 1 for long Bit[3:0]: Sensor 1 combine threshold 1 for short

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table 3-19 combine control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x80206883	SNR1_COMBINE_THRE_2	0xAA	RW	Bit[7:4]: Sensor 1 combine threshold 2 for long Bit[3:0]: Sensor 1 combine threshold 2 for short
0x80206884	SNR1_COMBINE_WEIGHT_0_0	0x80	RW	Bit[7:0]: Sensor 1 combine weight[0][0]
0x80206885	SNR1_COMBINE_WEIGHT_0_1	0x80	RW	Bit[7:0]: Sensor 1 combine weight[0][1]
0x80206886	SNR1_COMBINE_WEIGHT_0_2	0x60	RW	Bit[7:0]: Sensor 1 combine weight[0][2]
0x80206887	SNR1_COMBINE_WEIGHT_0_3	0x40	RW	Bit[7:0]: Sensor 1 combine weight[0][3]
0x80206888	SNR1_COMBINE_WEIGHT_1_0	0x80	RW	Bit[7:0]: Sensor 1 combine weight[1][0]
0x80206889	SNR1_COMBINE_WEIGHT_1_1	0x80	RW	Bit[7:0]: Sensor 1 combine weight[1][1]
0x8020688A	SNR1_COMBINE_WEIGHT_1_2	0x40	RW	Bit[7:0]: Sensor 1 combine weight[1][2]
0x8020688B	SNR1_COMBINE_WEIGHT_1_3	0x20	RW	Bit[7:0]: Sensor 1 combine weight[1][3]
0x8020688C	SNR1_COMBINE_WEIGHT_2_0	0x80	RW	Bit[7:0]: Sensor 1 combine weight[2][0]
0x8020688D	SNR1_COMBINE_WEIGHT_2_1	0x60	RW	Bit[7:0]: Sensor 1 combine weight[2][1]
0x8020688E	SNR1_COMBINE_WEIGHT_2_2	0x00	RW	Bit[7:0]: Sensor 1 combine weight[2][2]
0x8020688F	SNR1_COMBINE_WEIGHT_2_3	0x00	RW	Bit[7:0]: Sensor 1 combine weight[2][3]
0x80206890	SNR1_COMBINE_WEIGHT_3_0	0x80	RW	Bit[7:0]: Sensor 1 combine weight[3][0]
0x80206891	SNR1_COMBINE_WEIGHT_3_1	0x80	RW	Bit[7:0]: Sensor 1 combine weight[3][1]
0x80206892	SNR1_COMBINE_WEIGHT_3_2	0x00	RW	Bit[7:0]: Sensor 1 combine weight[3][2]
0x80206893	SNR1_COMBINE_WEIGHT_3_3	0x00	RW	Bit[7:0]: Sensor 1 combine weight[3][3]

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table 3-20 pre CMX firmware registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x270	SPRECTLIST_0_H	0x00	RW	Bit[7:0]: B/R for D65 [15:8]
0x271	SPRECTLIST_0_L	0x98	RW	Bit[7:0]: B/R for D65 [7:0]
0x272	SPRECTLIST_1_H	0x00	RW	Bit[7:0]: B/R for CWF [15:8]
0x273	SPRECTLIST_1_L	0xAC	RW	Bit[7:0]: B/R for CWF [7:0]
0x274	SPRECTLIST_2_H	0x01	RW	Bit[7:0]: B/R for A [15:8]
0x275	SPRECTLIST_2_L	0x00	RW	Bit[7:0]: B/R for A [7:0]
0x276	INVMLMS_D_0_0_H	0x01	RW	Bit[7:0]: SPD to LPD D65 matrix 00[15:8]
0x277	INVMLMS_D_0_0_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 00[7:0]
0x278	INVMLMS_D_0_1_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 01[15:8]
0x279	INVMLMS_D_0_1_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 01[7:0]
0x27A	INVMLMS_D_0_2_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 02[15:8]
0x27B	INVMLMS_D_0_2_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 02[7:0]
0x27C	INVMLMS_D_1_0_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 10[15:8]
0x27D	INVMLMS_D_1_0_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 10[7:0]
0x27E	INVMLMS_D_1_1_H	0x01	RW	Bit[7:0]: SPD to LPD D65 matrix 11[15:8]
0x27F	INVMLMS_D_1_1_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 11[7:0]
0x280	INVMLMS_D_1_2_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 12[15:8]
0x281	INVMLMS_D_1_2_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 12[7:0]
0x282	INVMLMS_D_2_0_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 20[15:8]
0x283	INVMLMS_D_2_0_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 20[7:0]
0x284	INVMLMS_D_2_1_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 21[15:8]
0x285	INVMLMS_D_2_1_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 21[7:0]
0x286	INVMLMS_D_2_2_H	0x01	RW	Bit[7:0]: SPD to LPD D65 matrix 22[15:8]
0x287	INVMLMS_D_2_2_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 22[7:0]
0x288	INVMLMS_C_0_0_H	0x01	RW	Bit[7:0]: SPD to LPD CWF matrix 00[15:8]
0x289	INVMLMS_C_0_0_L	0x00	RW	Bit[7:0]: SPD to LPD CWF matrix 00[7:0]
0x28A	INVMLMS_C_0_1_H	0x00	RW	Bit[7:0]: SPD to LPD CWF matrix 01[15:8]
0x28B	INVMLMS_C_0_1_L	0x00	RW	Bit[7:0]: SPD to LPD CWF matrix 01[7:0]
0x28C	INVMLMS_C_0_2_H	0x00	RW	Bit[7:0]: SPD to LPD CWF matrix 02[15:8]
0x28D	INVMLMS_C_0_2_L	0x00	RW	Bit[7:0]: SPD to LPD CWF matrix 02[7:0]

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table 3-20 pre CMX firmware registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x28E	INVMLMS_C_1_0_H	0x00	RW	Bit[7:0]: SPD to LPD CWF matrix 10[15:8]
0x28F	INVMLMS_C_1_0_L	0x00	RW	Bit[7:0]: SPD to LPD CWF matrix 10[7:0]
0x290	INVMLMS_C_1_1_H	0x01	RW	Bit[7:0]: SPD to LPD CWF matrix 11[15:8]
0x291	INVMLMS_C_1_1_L	0x00	RW	Bit[7:0]: SPD to LPD CWF matrix 11[7:0]
0x292	INVMLMS_C_1_2_H	0x00	RW	Bit[7:0]: SPD to LPD CWF matrix 12[15:8]
0x293	INVMLMS_C_1_2_L	0x00	RW	Bit[7:0]: SPD to LPD CWF matrix 12[7:0]
0x294	INVMLMS_C_2_0_H	0x00	RW	Bit[7:0]: SPD to LPD CWF matrix 20[15:8]
0x295	INVMLMS_C_2_0_L	0x00	RW	Bit[7:0]: SPD to LPD CWF matrix 20[7:0]
0x296	INVMLMS_C_2_1_H	0x00	RW	Bit[7:0]: SPD to LPD CWF matrix 21[15:8]
0x297	INVMLMS_C_2_1_L	0x00	RW	Bit[7:0]: SPD to LPD CWF matrix 21[7:0]
0x298	INVMLMS_C_2_2_H	0x01	RW	Bit[7:0]: SPD to LPD CWF matrix 22[15:8]
0x299	INVMLMS_C_2_2_L	0x00	RW	Bit[7:0]: SPD to LPD CWF matrix 22[7:0]
0x29A	INVMLMS_A_0_0_H	0x01	RW	Bit[7:0]: SPD to LPD A matrix 00[15:8]
0x29B	INVMLMS_A_0_0_L	0x00	RW	Bit[7:0]: SPD to LPD A matrix 00[7:0]
0x29C	INVMLMS_A_0_1_H	0x00	RW	Bit[7:0]: SPD to LPD A matrix 01[15:8]
0x29D	INVMLMS_A_0_1_L	0x00	RW	Bit[7:0]: SPD to LPD A matrix 01[7:0]
0x29E	INVMLMS_A_0_2_H	0x00	RW	Bit[7:0]: SPD to LPD A matrix 02[15:8]
0x29F	INVMLMS_A_0_2_L	0x00	RW	Bit[7:0]: SPD to LPD A matrix 02[7:0]
0x2A0	INVMLMS_A_1_0_H	0x00	RW	Bit[7:0]: SPD to LPD A matrix 10[15:8]
0x2A1	INVMLMS_A_1_0_L	0x00	RW	Bit[7:0]: SPD to LPD A matrix 10[7:0]
0x2A2	INVMLMS_A_1_1_H	0x01	RW	Bit[7:0]: SPD to LPD A matrix 11[15:8]
0x2A3	INVMLMS_A_1_1_L	0x00	RW	Bit[7:0]: SPD to LPD A matrix 11[7:0]
0x2A4	INVMLMS_A_1_2_H	0x00	RW	Bit[7:0]: SPD to LPD A matrix 12[15:8]
0x2A5	INVMLMS_A_1_2_L	0x00	RW	Bit[7:0]: SPD to LPD A matrix 12[7:0]
0x2A6	INVMLMS_A_2_0_H	0x00	RW	Bit[7:0]: SPD to LPD A matrix 20[15:8]
0x2A7	INVMLMS_A_2_0_L	0x00	RW	Bit[7:0]: SPD to LPD A matrix 20[7:0]
0x2A8	INVMLMS_A_2_1_H	0x00	RW	Bit[7:0]: SPD to LPD A matrix 21[15:8]
0x2A9	INVMLMS_A_2_1_L	0x00	RW	Bit[7:0]: SPD to LPD A matrix 21[7:0]
0x2AA	INVMLMS_A_2_2_H	0x01	RW	Bit[7:0]: SPD to LPD A matrix 22[15:8]
0x2AB	INVMLMS_A_2_2_L	0x00	RW	Bit[7:0]: SPD to LPD A matrix 22[7:0]

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3.13 HDR gain

After combination, the image brightness may still not reach the target brightness level. In this case, the OV490 can apply a global HDR gain to increase the brightness. However, it is not guaranteed to reach the target brightness level by applying HDR gain, because the maximum HDR gain (firmware register 0x253) and the number of saturated pixels after applying HDR gain is limited by firmware register 0x253.

The frame to frame HDR gain adjustment weight is limited by firmware register 0x1AE, the weight of the new calculated HDR gain is 0x1AE/16.

The HDR gain applied can be read back from registers 0x80207494~0x80207495 (0x80207694~0x80207695 for the second sensor).

table 3-21 HDR gain saturated pixel threshold registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x80206814	SNR0_COMBINE_SATURATE_THRE_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 final saturated pixel num threshold[21:16]
0x80206815	SNR0_COMBINE_SATURATE_THRE_B1	0x01	RW	Bit[7:0]: Sensor 0 final saturated pixel num threshold [15:8]
0x80206816	SNR0_COMBINE_SATURATE_THRE_B0	0x00	RW	Bit[7:0]: Sensor 0 final saturated pixel num threshold [7:0]
0x80206894	SNR1_COMBINE_SATURATE_THRE_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 final saturated pixel num threshold [21:16]
0x80206895	SNR1_COMBINE_SATURATE_THRE_B1	0x01	RW	Bit[7:0]: Sensor 1 final saturated pixel num threshold [15:8]
0x80206896	SNR1_COMBINE_SATURATE_THRE_B0	0x00	RW	Bit[7:0]: Sensor 1 final saturated pixel num threshold [7:0]
0x80207494	SNR0_TMP_LOG_GAIN_B1	–	R	Bit[7]: Reserved Bit[6:0]: Sensor 0 log HDR gain[14:8] Digital gain applied to achieve luminance target log HDR gain=2048 x log2 (HDR gain)
0x80207495	SNR0_TMP_LOG_GAIN_B0	–	R	Bit[7:0]: Sensor 0 log HDR gain[7:0] Digital gain applied to achieve luminance target log HDR gain=2048 x log2 (HDR gain)

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table 3-21 HDR gain saturated pixel threshold registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x80207694	SNR1_TMP_LOG_GAIN_B1	–	R	Bit[7]: Reserved Bit[6:0]: Sensor 1 log HDR gain[14:8] Digital gain applied to achieve luminance target log HDR gain=2048 x log2 (HDR gain)
0x80207695	SNR1_TMP_LOG_GAIN_B0	–	R	Bit[7:0]: Sensor 1 log HDR gain[7:0] Digital gain applied to achieve luminance target log HDR gain=2048 x log2 (HDR gain)

table 3-22 HDR gain firmware registers

address	register name	default value	R/W	description
0x253	MINSATURATELEVEL	0x10	RW	For Max_HDR_Gain Calculation Maximum HDR gain is 256/ MinSaturateLevel
0x1AE	HDRGAINSTEP	0x10	RW	Bit[7:0]: HDRGainStep

3.14 tone mapping

The tone mapping module gets data from the combine module and maps the data to a specified bit-width in order to approximate the appearance of high dynamic range images. The output bit-width can be 16 bits, 18 bits or 20 bits. Default is 16 bits. But for other bit-widths, it is required to manually set as follows:

1. Set register 0x8020740A[5] (register 0x8020760A[5] for the second sensor) to high to enable manually setting raw output bit-width
2. Set register 0x8020740A[4:0] (0x8020760A[4:0] for the second sensor) and the required bit-width number should be 12 to 20

There are several steps in the tone mapping procedure, including global tone mapping, local tone mapping and histogram equalization. The algorithm uses a weighted histogram equalization procedure to automatically generate a tone curve. Global gamma and local gamma are applied on the luminance channel and keep the chrominance unchanged, which compresses the functions data bit depth. The histogram curve is applied to adjust the contrast to equalize the histogram for and improved HDR rendering.

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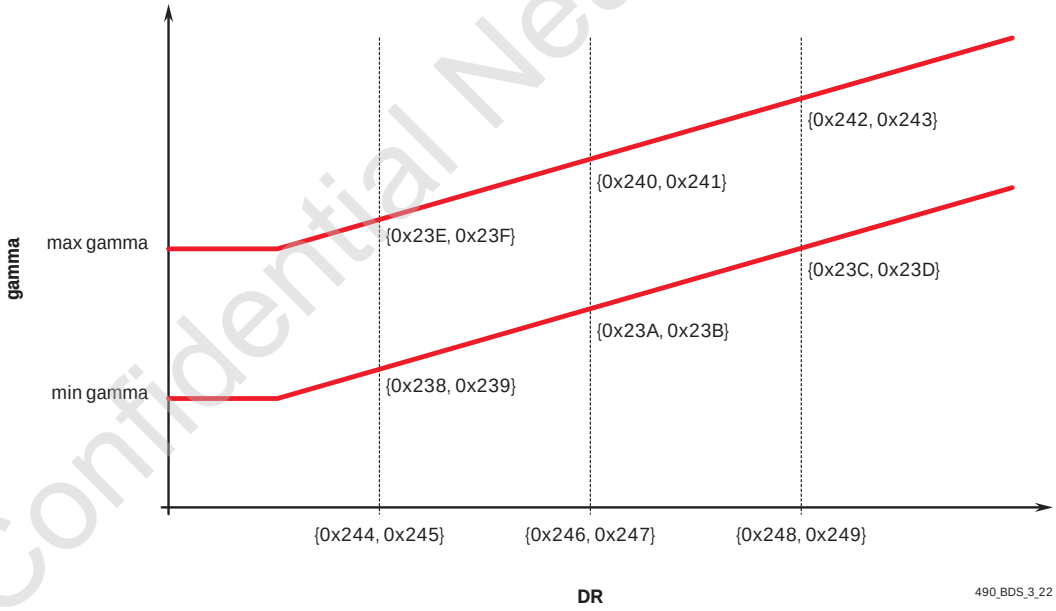
3.14.1 global tone mapping

The OV490 uses global tone mapping to compensate for the nonlinearity of intensity reproduction in a device's display.

Global tone mapping increases with the dynamic range to maintain the same shadow of gray, similar to the display. The OV490 adjusts the gamma curve with the dynamic range based on a user-defined minimum and maximum gamma table as shown in **figure 3-22**.

Registers 0x244~0x249 define the dynamic range at which the gamma should be no lower than 0x238~0x23D, respectively, and no more than 0x23E~0x243, respectively. The minimum and maximum gamma list and dynamic range list registers reside in the firmware registers. The gamma registers specify the inverse of the OV490 gamma or the gamma of the display device. For example, a minimum gamma 2.0 means the correction of max x (x/max)^(1/2.0) for input signal x. See **table 3-23** for further details.

figure 3-22 global gamma curve



The OV490 interpolates the minimum and maximum gamma based on the long/short ratio from the neighboring grids. Most displays require 2.0 or higher gamma correction. The minimum gamma correction should be applied to avoid under correction. The maximum gamma correction must avoid bit loss. Between the minimum and maximum gamma correction, the OV490 calculates the best gamma curve to achieve the brightness target.

The current gamma can be read back from registers {0x80207492, 0x80207493}, ({0x80207692, 0x80207693} for the second sensor). When the dynamic range of the scene changes, the OV490 adjusts the gamma curve. The maximum adjustment step from frame to frame is set by firmware register 0x254. If the step is too high, the image brightness may change rapidly. The gamma curve can be also manually set by firmware registers {0x24A, 0x24B} when firmware register 0x1AB is set to 1.

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table 3-23 global tone mapping firmware registers (sheet 1 of 2)

offset	register name	default value	R/W	description
0x1AB	MANUALGAMMA ENABLE	0x00	RW	Bit[0]: Manual gamma enable 0: Disable 1: Enable
0x238	MINGAMMALIST_0_H	0x01	RW	Bit[7:0]: Min gamma list 1[15:8] Minimum gamma at long short ratio of Gamma_DR_Thre1 Min_Gamma_Thre1 = 256 × gamma
0x239	MINGAMMALIST_0_L	0x00	RW	Bit[7:0]: Min gamma list 1[7:0] Minimum gamma at long short ratio of Gamma_DR_Thre1 Min_Gamma_Thre1 = 256 × gamma
0x23A	MINGAMMALIST_1_H	0x01	RW	Bit[7:0]: Min gamma list 2[15:8] Minimum gamma at long short ratio of Gamma_DR_Thre2 Min_Gamma_Thre1 = 256 × gamma
0x23B	MINGAMMALIST_1_L	0x00	RW	Bit[7:0]: Min gamma list 2[7:0] Minimum gamma at long short ratio of Gamma_DR_Thre2 Min_Gamma_Thre1 = 256 × gamma
0x23C	MINGAMMALIST_2_H	0x01	RW	Bit[7:0]: Min gamma list 3[15:8] Minimum gamma at long short ratio of Gamma_DR_Thre3 Min_Gamma_Thre1 = 256 × gamma
0x23D	MINGAMMALIST_2_L	0x00	RW	Bit[7:0]: Min gamma list 3[7:0] Minimum gamma at long short ratio of Gamma_DR_Thre3 Min_Gamma_Thre1 = 256 × gamma
0x23E	MAXGAMMALIST_0_H	0x01	RW	Bit[7:0]: Max gamma list 1[15:8] Maximum gamma at long short ratio of Gamma_DR_Thre1 Max_Gamma_Thre1 = 256 × gamma
0x23F	MAXGAMMALIST_0_L	0x32	RW	Bit[7:0]: Max gamma list 1[7:0] Maximum gamma at long short ratio of Gamma_DR_Thre1 Max_Gamma_Thre1 = 256 × gamma
0x240	MAXGAMMALIST_1_H	0x01	RW	Bit[7:0]: Max gamma list 2[15:8] Maximum gamma at long short ratio of Gamma_DR_Thre2 Max_Gamma_Thre1 = 256 × gamma
0x241	MAXGAMMALIST_1_L	0xE8	RW	Bit[7:0]: Max gamma list 2[7:0] Maximum gamma at long short ratio of Gamma_DR_Thre2 Max_Gamma_Thre1 = 256 × gamma

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table 3-23 global tone mapping firmware registers (sheet 2 of 2)

offset	register name	default value	R/W	description
0x242	MAXGAMMALIST_2_H	0x02	RW	Bit[7:0]: Max gamma list 3[15:8] Maximum gamma at long short ratio of Gamma_DR_Thre3 Max_Gamma_Thre1 = 256 × gamma
0x243	MAXGAMMALIST_2_L	0x74	RW	Bit[7:0]: Max gamma list 3[7:0] Maximum gamma at long short ratio of Gamma_DR_Thre3 Max_Gamma_Thre1 = 256 × gamma
0x244	DYNAMICRANGELIST _0_H	0x00	RW	Bit[7:0]: Dynamic range list 1[15:8] Long short ratio (DR) threshold 1 Gamma_DR_Thre1 = ratio × 16
0x245	DYNAMICRANGELIST _0_L	0x10	RW	Bit[7:0]: Dynamic range list 1[7:0] Long short ratio (DR) threshold 1 Gamma_DR_Thre1 = ratio × 16
0x246	DYNAMICRANGELIST _1_H	0x00	RW	Bit[7:0]: Dynamic range list 2[15:8] Long short ratio (DR) threshold 2 Gamma_DR_Thre1 = ratio × 16
0x247	DYNAMICRANGELIST _1_L	0x40	RW	Bit[7:0]: Dynamic range list 2[7:0] Long short ratio (DR) threshold 2 Gamma_DR_Thre1 = ratio × 16
0x248	DYNAMICRANGELIST _2_H	0x00	RW	Bit[7:0]: Dynamic range list 3[15:8] Long short ratio (DR) threshold 3 Gamma_DR_Thre1 = ratio × 16
0x249	DYNAMICRANGELIST _2_L	0x80	RW	Bit[7:0]: Dynamic range list 3[7:0] Long short ratio (DR) threshold 3 Gamma_DR_Thre1 = ratio × 16
0x254	GLOBALGAMMASTEP	0x04	RW	Bit[7:0]: Gamma step Frame to frame gamma adjustment step = (tone compression gamma step)/16×100%

table 3-24 global tone mapping control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x80207492	SNR0_TMP_GLOBAL_ GAIN_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 global gamma gain[9:8]
0x80207493	SNR0_TMP_GLOBAL_ GAIN_B0	0xFF	RW	Bit[7:0]: Sensor 0 global gamma gain[7:0]

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table 3-24 global tone mapping control registers (sheet 2 of 2)

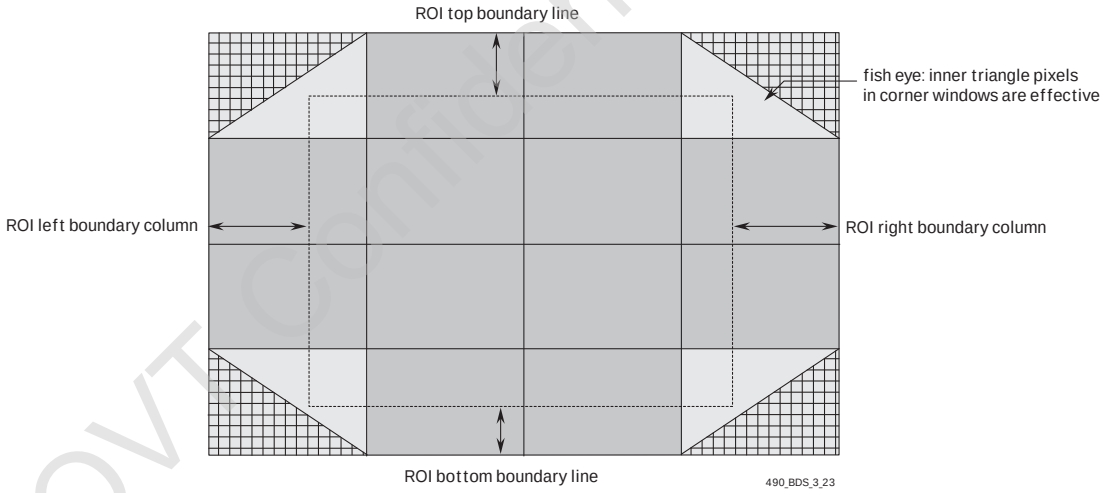
address	register name	default value	R/W	description
0x80207692	SNR1_TMP_GLOBAL_GAIN_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 global gamma gain[9:8]
0x80207693	SNR1_TMP_GLOBAL_GAIN_B0	0xFF	RW	Bit[7:0]: Sensor 1 global gamma gain[7:0]

3.14.2 local tone mapping

The local tone mapping procedure splits the input image into 4×4 fixed blocks. The gamma gain calculation is based on the 4×4 window and then applied to image data. Local mean is calculated as the average value for each window. If fish eye statistics is enabled, special statistics will be done for the 4 corner windows. When it is disabled, the statistics will be the same for each window.

Global mean is calculated based on the total window or ROI window. Tone mapping supports ROI. If ROI is enabled (0x80207400[4]=1), global mean is calculated based on ROI window. The ROI window size is defined by register 0x8020740C ~ 0x80207413.

figure 3-23 tone mapping statistics diagram



Based on local mean and global mean, boost gain for each grid can be calculated and gain for each pixel is interpolated from the neighboring grids. The gain is applied to boost the dark area of a high dynamic range scene. Maximum boost gain is dependent on firmware register 0x261. If the value of register 0x261 is 0x30, then there is no boost gain.

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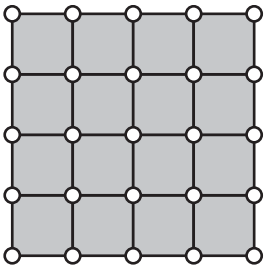
figure 3-24 local tone mapping grid diagram



490_BDS_3_24

Gain is not applied to all pixels but only pixels falling in a luminance range will be boosted. The related register range is firmware registers 0x268~0x26F.

```
brightness = 256/(2^(20 - register value/0x800))
```

Besides boost, some pixels local tone mapping also can suppress the pixels luminance if the gamma suppress function is enabled. The local boost function and gamma suppress function use the same luminance threshold. For local boost function, pixels whose luminance is between YTH1 and YTH2 will be boosted. For gamma suppress function, pixels whose luminance is lower than YTH0 or higher than YTH3 will be suppressed by gamma suppress gain.

Firmware registers {0x268, 0x269} is for YTH0. YTH0=256/(2^(20 - register value /0x800))

Firmware registers {0x26A, 0x26B} is for YTH1. YTH1=256/(2^(20 - register value /0x800))

Firmware registers {0x26C, 0x26D} is for YTH2. YTH2=256/(2^(20 - register value /0x800))

Firmware registers {0x26E, 0x26F} is for YTH3. YTH3=256/(2^(20 - register value /0x800))

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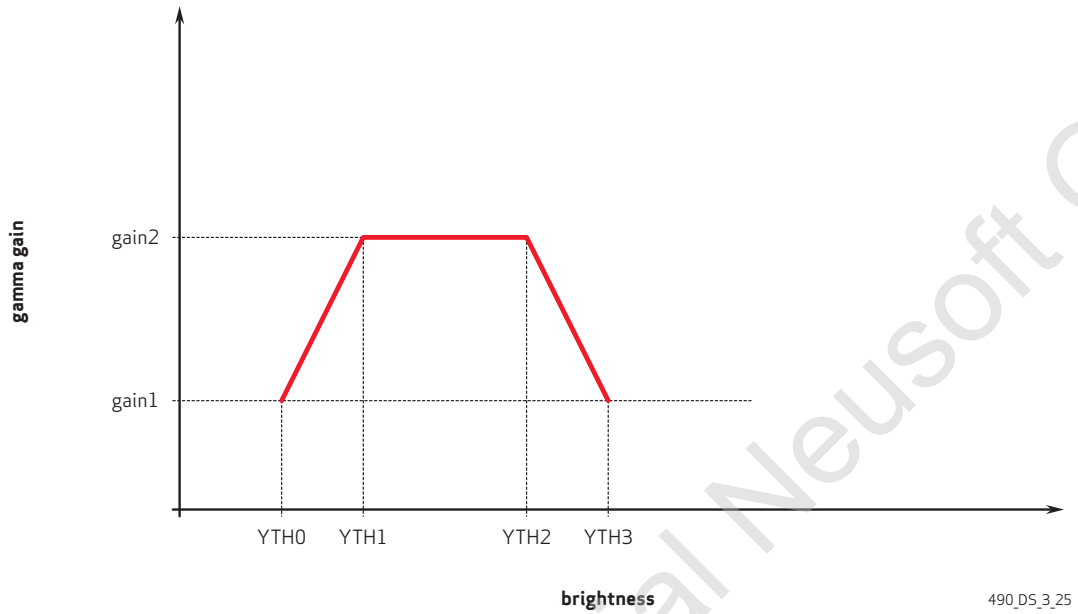
figure 3-25 local tone mapping gamma gain diagram



If the gamma suppress function is enabled (firmware register 0x2B8=1), Gain1 value is Global gamma gain - Gamma suppress gain. The gamma suppress gain is defined in firmware registers {0x2B6, 0x2B7}.

If the gamma suppress function is disabled, then there is no suppression of dark pixels and Gain1 = Global gamma gain.

The Gain2 value is the global gamma gain, *local boost gain. If the value of register 0x621 is 0x20, then there is no boost gain and Gain2 = Global gamma gain.

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table 3-25 tone mapping registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x80207400	SNR0_TMP_CTRL0	0x03	RW	Sensor 0 Tone Mapping Control Bit[7:5]: m_nGlobalMeanStatShift ROI statistic pixel selection 000: All pixels in ROI are used for statistics 001: 1/4 sample in both horizontal and vertical directions 010: 1/16 sample in both horizontal and vertical directions 011: 1/64 sample in both horizontal and vertical directions 100: 1/256 sample in both horizontal and vertical directions Others: Not supported Bit[4]: m_nGlobalMeanStatROI enable 0: Use 4x4 window local statistics results to calculate global mean 1: Use ROI to calculate global mean Bit[3]: m_bLogHDRGainShiftEnable 0: Use log value direct from combine output 1: Plus a shift value to compensate combine output log value Bit[2]: m_nFisheyeStatEnable 0: Statistics all the 4x4 windows with the same method 1: Use special method for statistics of 4 corner windows Bit[1]: m_bContrastBoost Bit[0]: m_bContrastEnable
0x8020740C	SNR0_TMP_ROI_TOP_B1	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 ROI top boundary line[10:8]
0x8020740D	SNR0_TMP_ROI_TOP_B0	0x10	RW	Bit[7:0]: Sensor 0 ROI top boundary line[7:0]
0x8020740E	SNR0_TMP_ROI_BOTTOM_B1	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 ROI bottom boundary line[10:8]
0x8020740F	SNR0_TMP_ROI_BOTTOM_B0	0x10	RW	Bit[7:0]: Sensor 0 ROI bottom boundary line[7:0]

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table 3-25 tone mapping registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x80207410	SNR0_TMP_ROI_ LEFT_B1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 ROI left boundary column[11:8]
0x80207411	SNR0_TMP_ROI_ LEFT_B0	0x10	RW	Bit[7:0]: Sensor 0 ROI left boundary column[7:0]
0x80207412	SNR0_TMP_ROI_ RIGHT_B1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 ROI right boundary column[11:8]
0x80207413	SNR0_TMP_ROI_ RIGHT_B0	0x10	RW	Bit[7:0]: Sensor 0 ROI right boundary column[7:0]
0x80207414	SNR0_TMP_GLOBAL _ST_TH_B2	0x00	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 global mean statistic threshold[22:16]
0x80207415	SNR0_TMP_GLOBAL _ST_TH_B1	0x04	RW	Bit[7:0]: Sensor 0 global mean statistic threshold[15:8]
0x80207416	SNR0_TMP_GLOBAL _ST_TH_B0	0x00	RW	Bit[7:0]: Sensor 0 global mean statistic threshold[7:0]

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table 3-25 tone mapping registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x80207600	SNR1_TMP_CTRL0	0x03	RW	Sensor 1 Tone Mapping Control Bit[7:5]: m_nGlobalMeanStatShift ROI statistic pixel selection 000: All pixels in ROI are used for statistics 001: 1/4 sample in both horizontal and vertical directions 010: 1/16 sample in both horizontal and vertical directions 011: 1/64 sample in both horizontal and vertical directions 100: 1/256 sample in both horizontal and vertical directions Others: Not supported Bit[4]: m_nGlobalMeanStatROI enable 0: Use 4x4 window local statistics results to calculate global mean 1: Use ROI to calculate global mean Bit[3]: m_bLogHDRGainShiftEnable 0: Use log value direct from combine output 1: Plus a shift value to compensate combine output log value Bit[2]: m_nFisheyeStatEnable 0: Statistics all the 4x4 windows with the same method 1: Use special method for statistics of 4 corner windows Bit[1]: m_bContrastBoost Bit[0]: m_bContrastEnable
0x8020760C	SNR1_TMP_ROI_TOP_B1	0x00	RW	Bit[7:2]: Reserved Bit[2:0]: Sensor 1 ROI top boundary line[10:8]
0x8020760D	SNR1_TMP_ROI_TOP_B0	0x10	RW	Bit[7:0]: Sensor 1 ROI top boundary line[7:0]
0x8020760E	SNR1_TMP_ROI_BOTTOM_B1	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 ROI bottom boundary line[10:8]
0x8020760F	SNR1_TMP_ROI_BOTTOM_B0	0x10	RW	Bit[7:0]: Sensor 1 ROI bottom boundary line[7:0]

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table 3-25 tone mapping registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x80207610	SNR1_TMP_ROI_ LEFT_B1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 ROI left boundary column[11:8]
0x80207611	SNR1_TMP_ROI_ LEFT_B0	0x10	RW	Bit[7:0]: Sensor 1 ROI left boundary column[7:0]
0x80207612	SNR1_TMP_ROI_ RIGHT_B1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 ROI right boundary column[11:8]
0x80207613	SNR1_TMP_ROI_ RIGHT_B0	0x10	RW	Bit[7:0]: Sensor 1 ROI right boundary column[7:0]
0x80207614	SNR1_TMP_GLOBAL _ST_TH_B2	0x00	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 global mean statistic threshold[22:16]
0x80207615	SNR1_TMP_GLOBAL _ST_TH_B1	0x04	RW	Bit[7:0]: Sensor 1 global mean statistic threshold[15:8]
0x80207616	SNR1_TMP_GLOBAL _ST_TH_B0	0x00	RW	Bit[7:0]: Sensor 1 global mean statistic threshold[7:0]

table 3-26 tone mapping firmware registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x2B6	MAXSUPPRESSGAIN_H	0x03	RW	Bit[7:0]: Max suppress gain for shadow and highlights[15:8]
0x2B7	MAXSUPPRESSGAIN_L	0x00	RW	Bit[7:0]: Max suppress gain for shadow and highlights[7:0]
0x2B8	MANUALSUPPRESSGAIN	0x01	RW	Bit[7:0]: Manual suppress gain enable
0x261	LOCALENHANCEMENT LEVEL	0x21	RW	Bit[7:0]: Local enhancement level
0x268	YTH0TARGET_0_H	0x78	RW	Bit[7:0]: Dark contrast enhancement Y Th0[15:8]
0x269	YTH0TARGET_0_L	0x00	RW	Bit[7:0]: Dark contrast enhancement Y Th0[7:0]
0x26A	YTH1TARGET_1_H	0x80	RW	Bit[7:0]: Dark contrast enhancement Y Th1[15:8]
0x26B	YTH1TARGET_1_L	0x00	RW	Bit[7:0]: Dark contrast enhancement Y Th1[7:0]

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table 3-26 tone mapping firmware registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x26C	YTH0TARGET_2_H	0x98	RW	Bit[7:0]: Dark contrast enhancement Y Th2[15:8]
0x26D	YTH0TARGET_2_L	0x00	RW	Bit[7:0]: Dark contrast enhancement Y Th2[7:0]
0x26E	YTH1TARGET_3_H	0x9C	RW	Bit[7:0]: Dark contrast enhancement Y Th3[15:8]
0x26F	YTH1TARGET_3_L	0xEC	RW	Bit[7:0]: Dark contrast enhancement Y Th3[7:0]

3.14.3 tone mapping curve

The OV490 estimates a tone mapping curve based on a 16-bin histogram that is achieved from the local tone mapped image. The standard HE mapping curve is weighted by a basic curve using a parameter called ContrastLevel (α)

The tone mapping curve is a weighted average curve between a user defined basic contrast curve and the histogram equalization curve of the image data.

```
tone_mapping_curve = (α × histogram_EQ_curve + (15 - α) × basic contrast_curve)/15,
```

where α is the weight of the histogram equalization curve. Both the contrast curve and histogram equalization curve can be used to improve the contrast of the high dynamic range image. Higher dynamic range usually requires higher contrast, so the weighting of the histogram equalization curve must increase with the dynamic range (see **figure 3-27**).

The ContrastLevel (α) is typically adjusted by dynamic range. The greater the dynamic range is, the greater the possible contrast level. Because high gain usually introduces high noise, which will also be amplified in contrast enhancement, the contrast level will be kept to a low level if the gain is high.

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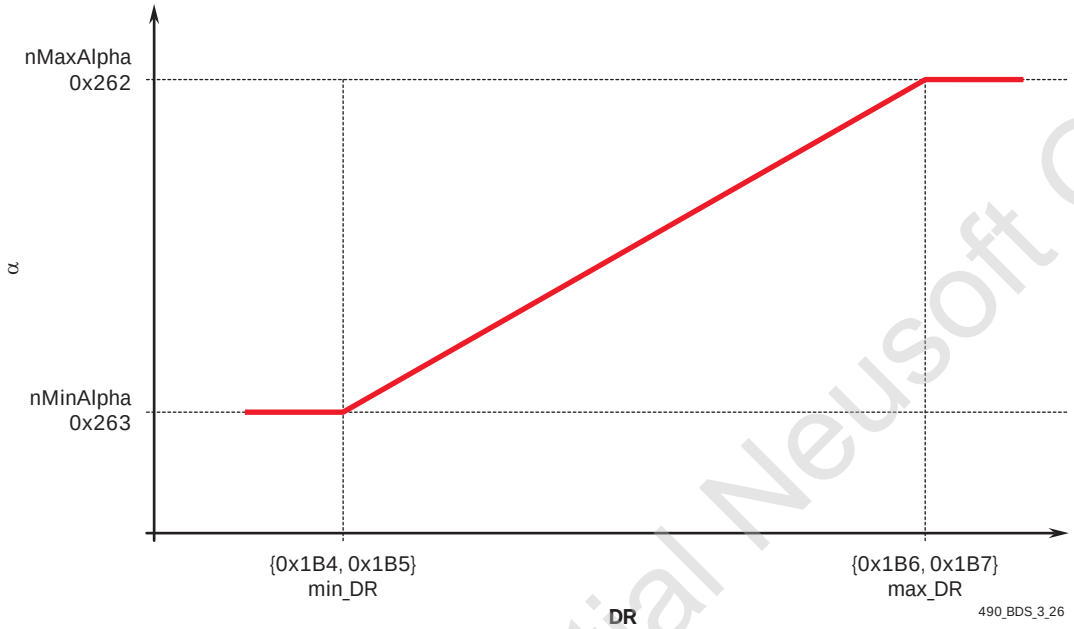
figure 3-26 contrast level threshold



After this curve estimation is done, the tone curve is restricted between two curves (i.e., the dark and light curves to avoid over-enhancement). The contrast curve, light curve and dark curve are shown in **figure 3-27**.

figure 3-27 contrast level restriction

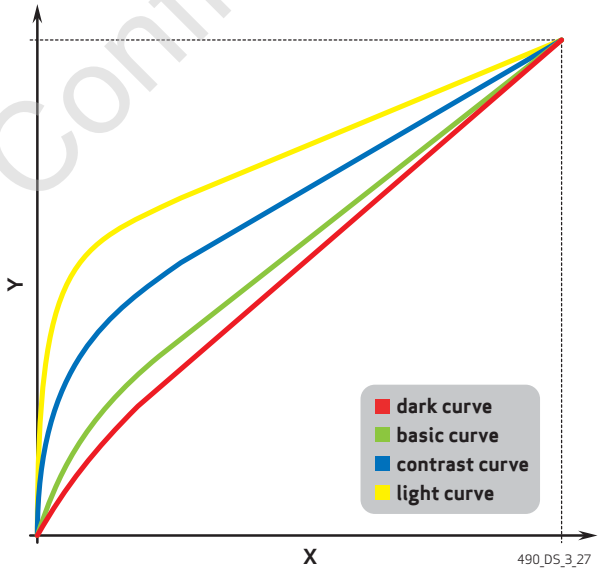


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table 3-27 contrast level restriction firmware registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x1B4	MINDYNAMICRANGE _H	0x00	RW	Bit[7:0]: EQ_α _DR_Thre1[15:8] EQ_ α _DR_Thre1 equals 16 times of long short ratio
0x1B5	MINDYNAMICRANGE _L	0x10	RW	Bit[7:0]: EQ_α _DR_Thre1[7:0] EQ_ α _DR_Thre1 equals 16 times of long short ratio
0x1B6	MAXDYNAMICRANGE _H	0x00	RW	Bit[7:0]: EQ_α _DR_Thre2[15:8] EQ_ α _DR_Thre2 equals 16 times of long short ratio
0x1B7	MAXDYNAMICRANGE _L	0x40	RW	Bit[7:0]: EQ_α _DR_Thre2[7:0] EQ_ α _DR_Thre2 equals 16 times of long short ratio
0x1B8	GAMMALIST_0_H	0x00	RW	Bit[7:0]: Base curve for tone curve P0[15:8]
0x1B9	GAMMALIST_0_L	0x2C	RW	Bit[7:0]: Base curve for tone curve P0[7:0]
0x1BA	GAMMALIST_1_H	0x00	RW	Bit[7:0]: Base curve for tone curve P1[15:8]
0x1BB	GAMMALIST_1_L	0x9B	RW	Bit[7:0]: Base curve for tone curve P1[7:0]
0x1BC	GAMMALIST_2_H	0x00	RW	Bit[7:0]: Base curve for tone curve P2[15:8]
0x1BD	GAMMALIST_2_L	0xD4	RW	Bit[7:0]: Base curve for tone curve P2[7:0]
0x1BE	GAMMALIST_3_H	0x01	RW	Bit[7:0]: Base curve for tone curve P3[15:8]
0x1BF	GAMMALIST_3_L	0x22	RW	Bit[7:0]: Base curve for tone curve P3[7:0]
0x1C0	GAMMALIST_4_H	0x01	RW	Bit[7:0]: Base curve for tone curve P4[15:8]
0x1C1	GAMMALIST_4_L	0x8E	RW	Bit[7:0]: Base curve for tone curve P4[7:0]
0x1C2	GAMMALIST_5_H	0x01	RW	Bit[7:0]: Base curve for tone curve P5[15:8]
0x1C3	GAMMALIST_5_L	0xD2	RW	Bit[7:0]: Base curve for tone curve P5[7:0]
0x1C4	GAMMALIST_6_H	0x02	RW	Bit[7:0]: Base curve for tone curve P6[15:8]
0x1C5	GAMMALIST_6_L	0x21	RW	Bit[7:0]: Base curve for tone curve P6[7:0]
0x1C6	GAMMALIST_7_H	0x02	RW	Bit[7:0]: Base curve for tone curve P7[15:8]
0x1C7	GAMMALIST_7_L	0x4E	RW	Bit[7:0]: Base curve for tone curve P7[7:0]
0x1C8	GAMMALIST_8_H	0x02	RW	Bit[7:0]: Base curve for tone curve P8[15:8]
0x1C9	GAMMALIST_8_L	0x7E	RW	Bit[7:0]: Base curve for tone curve P8[7:0]
0x1CA	GAMMALIST_9_H	0x02	RW	Bit[7:0]: Base curve for tone curve P9[15:8]
0x1CB	GAMMALIST_9_L	0xB3	RW	Bit[7:0]: Base curve for tone curve P9[7:0]
0x1CC	GAMMALIST_10_H	0x02	RW	Bit[7:0]: Base curve for tone curve P10[15:8]

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table 3-27 contrast level restriction firmware registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x1CD	GAMMALIST_10_L	0xEB	RW	Bit[7:0]: Base curve for tone curve P10[7:0]
0x1CE	GAMMALIST_11_H	0x03	RW	Bit[7:0]: Base curve for tone curve P11[15:8]
0x1CF	GAMMALIST_11_L	0x29	RW	Bit[7:0]: Base curve for tone curve P11[7:0]
0x1D0	GAMMALIST_12_H	0x03	RW	Bit[7:0]: Base curve for tone curve P12[15:8]
0x1D1	GAMMALIST_12_L	0x6B	RW	Bit[7:0]: Base curve for tone curve P12[7:0]
0x1D2	GAMMALIST_13_H	0x03	RW	Bit[7:0]: Base curve for tone curve P13[15:8]
0x1D3	GAMMALIST_13_L	0xB2	RW	Bit[7:0]: Base curve for tone curve P13[7:0]
0x1D4	GAMMALIST_14_H	0x03	RW	Bit[7:0]: Base curve for tone curve P14[15:8]
0x1D5	GAMMALIST_14_L	0xD8	RW	Bit[7:0]: Base curve for tone curve P14[7:0]
0x1D6	GAMMALIST_15_H	0x03	RW	Bit[7:0]: Base curve for tone curve P15[15:8]
0x1D7	GAMMALIST_15_L	0xFF	RW	Bit[7:0]: Base curve for tone curve P15[7:0]
0x1D8	LIGHTCURVE_0_H	0x01	RW	Bit[7:0]: High bound of tone curve P0[15:8]
0x1D9	LIGHTCURVE_0_L	0x28	RW	Bit[7:0]: High bound of tone curve P0[7:0]
0x1DA	LIGHTCURVE_1_H	0x01	RW	Bit[7:0]: High bound of tone curve P1[15:8]
0x1DB	LIGHTCURVE_1_L	0x45	RW	Bit[7:0]: High bound of tone curve P1[7:0]
0x1DC	LIGHTCURVE_2_H	0x01	RW	Bit[7:0]: High bound of tone curve P2[15:8]
0x1DD	LIGHTCURVE_2_L	0x88	RW	Bit[7:0]: High bound of tone curve P2[7:0]
0x1DE	LIGHTCURVE_3_H	0x01	RW	Bit[7:0]: High bound of tone curve P3[15:8]
0x1DF	LIGHTCURVE_3_L	0xEE	RW	Bit[7:0]: High bound of tone curve P3[7:0]
0x1E0	LIGHTCURVE_4_H	0x02	RW	Bit[7:0]: High bound of tone curve P4[15:8]
0x1E1	LIGHTCURVE_4_L	0x17	RW	Bit[7:0]: High bound of tone curve P4[7:0]
0x1E2	LIGHTCURVE_5_H	0x02	RW	Bit[7:0]: High bound of tone curve P5[15:8]
0x1E3	LIGHTCURVE_5_L	0x40	RW	Bit[7:0]: High bound of tone curve P5[7:0]
0x1E4	LIGHTCURVE_6_H	0x02	RW	Bit[7:0]: High bound of tone curve P6[15:8]
0x1E5	LIGHTCURVE_6_L	0x6B	RW	Bit[7:0]: High bound of tone curve P6[7:0]
0x1E6	LIGHTCURVE_7_H	0x02	RW	Bit[7:0]: High bound of tone curve P7[15:8]
0x1E7	LIGHTCURVE_7_L	0x98	RW	Bit[7:0]: High bound of tone curve P7[7:0]
0x1E8	LIGHTCURVE_8_H	0x02	RW	Bit[7:0]: High bound of tone curve P8[15:8]
0x1E9	LIGHTCURVE_8_L	0xC2	RW	Bit[7:0]: High bound of tone curve P8[7:0]
0x1EA	LIGHTCURVE_9_H	0x02	RW	Bit[7:0]: High bound of tone curve P9[15:8]

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table 3-27 contrast level restriction firmware registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x1EB	LIGHTCURVE_9_L	0xE7	RW	Bit[7:0]: High bound of tone curve P9[7:0]
0x1EC	LIGHTCURVE_10_H	0x03	RW	Bit[7:0]: High bound of tone curve P10[15:8]
0x1ED	LIGHTCURVE_10_L	0x20	RW	Bit[7:0]: High bound of tone curve P10[7:0]
0x1EE	LIGHTCURVE_11_H	0x03	RW	Bit[7:0]: High bound of tone curve P11[15:8]
0x1EF	LIGHTCURVE_11_L	0x4E	RW	Bit[7:0]: High bound of tone curve P11[7:0]
0x1F0	LIGHTCURVE_12_H	0x03	RW	Bit[7:0]: High bound of tone curve P12[15:8]
0x1F1	LIGHTCURVE_12_L	0x89	RW	Bit[7:0]: High bound of tone curve P12[7:0]
0x1F2	LIGHTCURVE_13_H	0x03	RW	Bit[7:0]: High bound of tone curve P13[15:8]
0x1F3	LIGHTCURVE_13_L	0xBF	RW	Bit[7:0]: High bound of tone curve P13[7:0]
0x1F4	LIGHTCURVE_14_H	0x03	RW	Bit[7:0]: High bound of tone curve P14[15:8]
0x1F5	LIGHTCURVE_14_L	0xE0	RW	Bit[7:0]: High bound of tone curve P14[7:0]
0x1F6	LIGHTCURVE_15_H	0x03	RW	Bit[7:0]: High bound of tone curve P15[15:8]
0x1F7	LIGHTCURVE_15_L	0xFF	RW	Bit[7:0]: High bound of tone curve P15[7:0]
0x1F8	DARKCURVE_0_H	0x00	RW	Bit[7:0]: Low bound of tone curve P0[15:8]
0x1F9	DARKCURVE_0_L	0x11	RW	Bit[7:0]: Low bound of tone curve P0[7:0]
0x1FA	DARKCURVE_1_H	0x00	RW	Bit[7:0]: Low bound of tone curve P1[15:8]
0x1FB	DARKCURVE_1_L	0x28	RW	Bit[7:0]: Low bound of tone curve P1[7:0]
0x1FC	DARKCURVE_2_H	0x00	RW	Bit[7:0]: Low bound of tone curve P2[15:8]
0x1FD	DARKCURVE_2_L	0x5B	RW	Bit[7:0]: Low bound of tone curve P2[7:0]
0x1FE	DARKCURVE_3_H	0x00	RW	Bit[7:0]: Low bound of tone curve P3[15:8]
0x1FF	DARKCURVE_3_L	0xC8	RW	Bit[7:0]: Low bound of tone curve P3[7:0]
0x200	DARKCURVE_4_H	0x01	RW	Bit[7:0]: Low bound of tone curve P4[15:8]
0x201	DARKCURVE_4_L	0x09	RW	Bit[7:0]: Low bound of tone curve P4[7:0]
0x202	DARKCURVE_5_H	0x01	RW	Bit[7:0]: Low bound of tone curve P5[15:8]
0x203	DARKCURVE_5_L	0x57	RW	Bit[7:0]: Low bound of tone curve P5[7:0]
0x204	DARKCURVE_6_H	0x01	RW	Bit[7:0]: Low bound of tone curve P6[15:8]
0x205	DARKCURVE_6_L	0x9B	RW	Bit[7:0]: Low bound of tone curve P6[7:0]
0x206	DARKCURVE_7_H	0x01	RW	Bit[7:0]: Low bound of tone curve P7[15:8]
0x207	DARKCURVE_7_L	0xD4	RW	Bit[7:0]: Low bound of tone curve P7[7:0]
0x208	DARKCURVE_8_H	0x02	RW	Bit[7:0]: Low bound of tone curve P8[15:8]

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table 3-27 contrast level restriction firmware registers (sheet 4 of 8)

address	register name	default value	R/W	description
0x209	DARKCURVE_8_L	0x01	RW	Bit[7:0]: Low bound of tone curve P8[7:0]
0x20A	DARKCURVE_9_H	0x02	RW	Bit[7:0]: Low bound of tone curve P9[15:8]
0x20B	DARKCURVE_9_L	0x25	RW	Bit[7:0]: Low bound of tone curve P9[7:0]
0x20C	DARKCURVE_10_H	0x02	RW	Bit[7:0]: Low bound of tone curve P10[15:8]
0x20D	DARKCURVE_10_L	0x64	RW	Bit[7:0]: Low bound of tone curve P10[7:0]
0x20E	DARKCURVE_11_H	0x02	RW	Bit[7:0]: Low bound of tone curve P11[15:8]
0x20F	DARKCURVE_11_L	0x9B	RW	Bit[7:0]: Low bound of tone curve P11[7:0]
0x210	DARKCURVE_12_H	0x02	RW	Bit[7:0]: Low bound of tone curve P12[15:8]
0x211	DARKCURVE_12_L	0xF9	RW	Bit[7:0]: Low bound of tone curve P12[7:0]
0x212	DARKCURVE_13_H	0x03	RW	Bit[7:0]: Low bound of tone curve P13[15:8]
0x213	DARKCURVE_13_L	0x4E	RW	Bit[7:0]: Low bound of tone curve P13[7:0]
0x214	DARKCURVE_14_H	0x03	RW	Bit[7:0]: Low bound of tone curve P14[15:8]
0x215	DARKCURVE_14_L	0x99	RW	Bit[7:0]: Low bound of tone curve P14[7:0]
0x216	DARKCURVE_15_H	0x03	RW	Bit[7:0]: Low bound of tone curve P15[15:8]
0x217	DARKCURVE_15_L	0xFF	RW	Bit[7:0]: Low bound of tone curve P15[7:0]
0x218	MANUALTONECURVE _0_H	0x00	RW	Bit[7:0]: Manual tone curve P0[15:8]
0x219	MANUALTONECURVE _0_L	0x01	RW	Bit[7:0]: Manual tone curve P0[7:0]
0x21A	MANUALTONECURVE _1_H	0x00	RW	Bit[7:0]: Manual tone curve P1[15:8]
0x21B	MANUALTONECURVE _1_L	0x10	RW	Bit[7:0]: Manual tone curve P1[7:0]
0x21C	MANUALTONECURVE _2_H	0x00	RW	Bit[7:0]: Manual tone curve P2 [15:8]
0x21D	MANUALTONECURVE _2_L	0x20	RW	Bit[7:0]: Manual tone curve P2[7:0]
0x21E	MANUALTONECURVE _3_H	0x00	RW	Bit[7:0]: Manual tone curve P3[15:8]
0x21F	MANUALTONECURVE _3_L	0x40	RW	Bit[7:0]: Manual tone curve P3[7:0]
0x220	MANUALTONECURVE _4_H	0x00	RW	Bit[7:0]: Manual tone curve P4[15:8]

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table 3-27 contrast level restriction firmware registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x221	MANUALTONECURVE _4_L	0x80	RW	Bit[7:0]: Manual tone curve P4 [7:0]
0x222	MANUALTONECURVE _5_H	0x00	RW	Bit[7:0]: Manual tone curve P5[15:8]
0x223	MANUALTONECURVE _5_L	0xB5	RW	Bit[7:0]: Manual tone curve P5[7:0]
0x224	MANUALTONECURVE _6_H	0x01	RW	Bit[7:0]: Manual tone curve P6[15:8]
0x225	MANUALTONECURVE _6_L	0x00	RW	Bit[7:0]: Manual tone curve P6[7:0]
0x226	MANUALTONECURVE _7_H	0x01	RW	Bit[7:0]: Manual tone curve P7[15:8]
0x227	MANUALTONECURVE _7_L	0x30	RW	Bit[7:0]: Manual tone curve P7[7:0]
0x228	MANUALTONECURVE _8_H	0x01	RW	Bit[7:0]: Manual tone curve P8[15:8]
0x229	MANUALTONECURVE _8_L	0x6A	RW	Bit[7:0]: Manual tone curve P8[7:0]
0x22A	MANUALTONECURVE _9_H	0x01	RW	Bit[7:0]: Manual tone curve P9[15:8]
0x22B	MANUALTONECURVE _9_L	0xAF	RW	Bit[7:0]: Manual tone curve P9[7:0]
0x22C	MANUALTONECURVE _10_H	0x02	RW	Bit[7:0]: Manual tone curve P10[15:8]
0x22D	MANUALTONECURVE _10_L	0x00	RW	Bit[7:0]: Manual tone curve P10[7:0]
0x22E	MANUALTONECURVE _11_H	0x02	RW	Bit[7:0]: Manual tone curve P11[15:8]
0x22F	MANUALTONECURVE _11_L	0x61	RW	Bit[7:0]: Manual tone curve P11 [7:0]
0x230	MANUALTONECURVE _12_H	0x02	RW	Bit[7:0]: Manual tone curve P12[15:8]
0x231	MANUALTONECURVE _12_L	0xD4	RW	Bit[7:0]: Manual tone curve P12[7:0]
0x232	MANUALTONECURVE _13_H	0x03	RW	Bit[7:0]: Manual tone curve P13[15:8]
0x233	MANUALTONECURVE _13_L	0x5D	RW	Bit[7:0]: Manual tone curve P13[7:0]

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table 3-27 contrast level restriction firmware registers (sheet 6 of 8)

address	register name	default value	R/W	description
0x234	MANUALTONECURVE_14_H	0x03	RW	Bit[7:0]: Manual tone curve P14[15:8]
0x235	MANUALTONECURVE_14_L	0xAB	RW	Bit[7:0]: Manual tone curve P14[7:0]
0x236	MANUALTONECURVE_15_H	0x03	RW	Bit[7:0]: Manual tone curve P15[15:8]
0x237	MANUALTONECURVE_15_L	0xFF	RW	Bit[7:0]: Manual tone curve P15[7:0]
0x238	MINGAMMALIST_0_H	0x01	RW	Bit[7:0]: Min tone compression gamma list 1[15:8]
0x239	MINGAMMALIST_0_L	0x00	RW	Bit[7:0]: Min tone compression gamma list 1[7:0]
0x23A	MINGAMMALIST_1_H	0x01	RW	Bit[7:0]: Min tone compression gamma list 2[15:8]
0x23B	MINGAMMALIST_1_L	0x00	RW	Bit[7:0]: Min tone compression gamma list 2[7:0]
0x23C	MINGAMMALIST_2_H	0x01	RW	Bit[7:0]: Min tone compression gamma list 3[15:8]
0x23D	MINGAMMALIST_2_L	0x00	RW	Bit[7:0]: Min tone compression gamma list 3[7:0]
0x23E	MAXGAMMALIST_0_H	0x01	RW	Bit[7:0]: Max tone compression gamma list 1[15:8]
0x23F	MAXGAMMALIST_0_L	0x32	RW	Bit[7:0]: Max tone compression gamma list 1[7:0]
0x240	MAXGAMMALIST_1_H	0x01	RW	Bit[7:0]: Max tone compression gamma list 2[15:8]
0x241	MAXGAMMALIST_1_L	0xE8	RW	Bit[7:0]: Max tone compression gamma list 2[7:0]
0x242	MAXGAMMALIST_2_H	0x02	RW	Bit[7:0]: Max tone compression gamma list 3[15:8]
0x243	MAXGAMMALIST_2_L	0x74	RW	Bit[7:0]: Max tone compression gamma list 3[7:0]
0x244	DYNAMICRANGELIST_0_H	0x00	RW	Bit[7:0]: Dynamic range list 1[15:8]
0x245	DYNAMICRANGELIST_0_L	0x10	RW	Bit[7:0]: Dynamic range list 1[7:0]
0x246	DYNAMICRANGELIST_1_H	0x00	RW	Bit[7:0]: Dynamic range list 2[15:8]

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table 3-27 contrast level restriction firmware registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x247	DYNAMICRANGELIST _1_L	0x40	RW	Bit[7:0]: Dynamic range list 2[7:0]
0x248	DYNAMICRANGELIST _2_H	0x00	RW	Bit[7:0]: Dynamic range list 3[15:8]
0x249	DYNAMICRANGELIST _2_L	0x80	RW	Bit[7:0]: Dynamic range list 3[7:0]
0x24A	MANUALGAMMA_H	0x00	RW	Bit[7:0]: Manual tone compression gamma[15:8]
0x24B	MANUALGAMMA_L	0x32	RW	Bit[7:0]: Manual tone compression gamma[7:0]
0x24C	LOGTARGETY_A_H	0x97	RW	Bit[7:0]: Image mean value target for frame A in ABC mode[15:8]
0x24D	LOGTARGETY_A_L	0x00	RW	Bit[7:0]: Image mean value target for frame A in ABC mode[7:0]
0x24E	LOGTARGETY_B_H	0x97	RW	Bit[7:0]: Image mean value target for frame B in ABC mode[15:8]
0x24F	LOGTARGETY_B_L	0x00	RW	Bit[7:0]: Image mean value target for frame B in ABC mode[7:0]
0x250	LOGTARGETY_C_H	0x97	RW	Bit[7:0]: Image mean value target for frame C in ABC mode[15:8]
0x251	LOGTARGETY_C_L	0x00	RW	Bit[7:0]: Image mean value target for frame C in ABC mode[7:0]
0x252	SHAPESMOOTH ENABLE	0x01	RW	Bit[0]: Tone curve smooth enable 0: Disable 1: Enable
0x253	MINSATURATELEVEL	0x10	RW	Bit[7:0]: Minimum saturate level for VS/short
0x254	GLOBALGAMMA STEP	0x04	RW	Bit[7:0]: Tone compression gamma step
0x255	REDUCENOISEINDA RKENABLE	0x00	RW	Bit[7:0]: Reduce noise for dark scenes enable 0: Disable 1: Enable
0x256	REDUCENOISEMAX GAIN_H	0x02	RW	Bit[0]: High gain boundary for reduce noise function[15:8]
0x257	REDUCENOISEMAX GAIN_L	0x00	RW	Bit[7:0]: High gain boundary for reduce noise function[7:0]
0x258	REDUCENOISEMIN GAIN_H	0x00	RW	Bit[7:0]: Low gain boundary for reduce noise function[15:8]
0x259	REDUCENOISEMIN GAIN_L	0xA0	RW	Bit[7:0]: Low gain boundary for reduce noise function[7:0]

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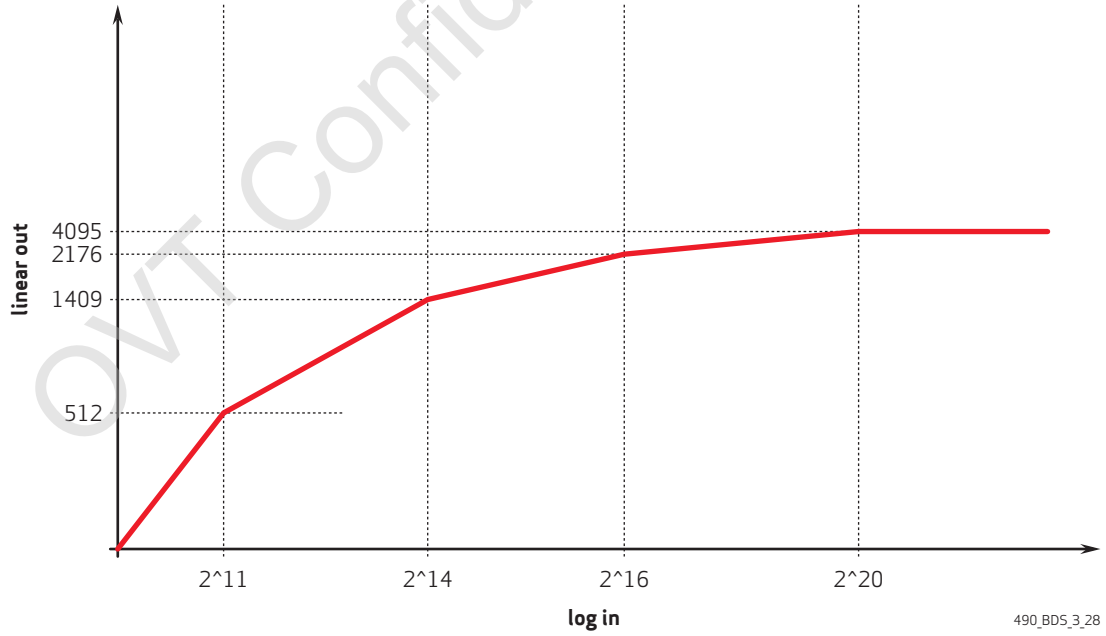
table 3-27 contrast level restriction firmware registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x25A	REDUCENOISESTEP	0x02	RW	Bit[7:0]: Gain step value for reduce noise
0x25B	GLOBALMEANW	0x00	RW	Bit[7:0]: Current global mean value weight to final target
0x25C	GAMMASTEP	0x04	RW	Bit[7:0]: Tone compression gamma change step
0x262	LOWCONTRAST LEVEL	0x01	RW	Bit[7:0]: Min_α Minimum weight of histogram equalization curve when dynamic range is below EQ_α _DR_Thre1
0x263	HIGHCONTRAST LEVEL	0x03	RW	Bit[7:0]: Max_α Maximum weight of histogram equalization curve when dynamic range is above EQ_α _DR_Thre2

3.15 piecewise linear (PWL)

PWL is designed to convert the 20-bit combined linear raw/Y to 12-bit linear raw/Y. A simple piecewise mapping is done based on a compress curve.

figure 3-28 linear out



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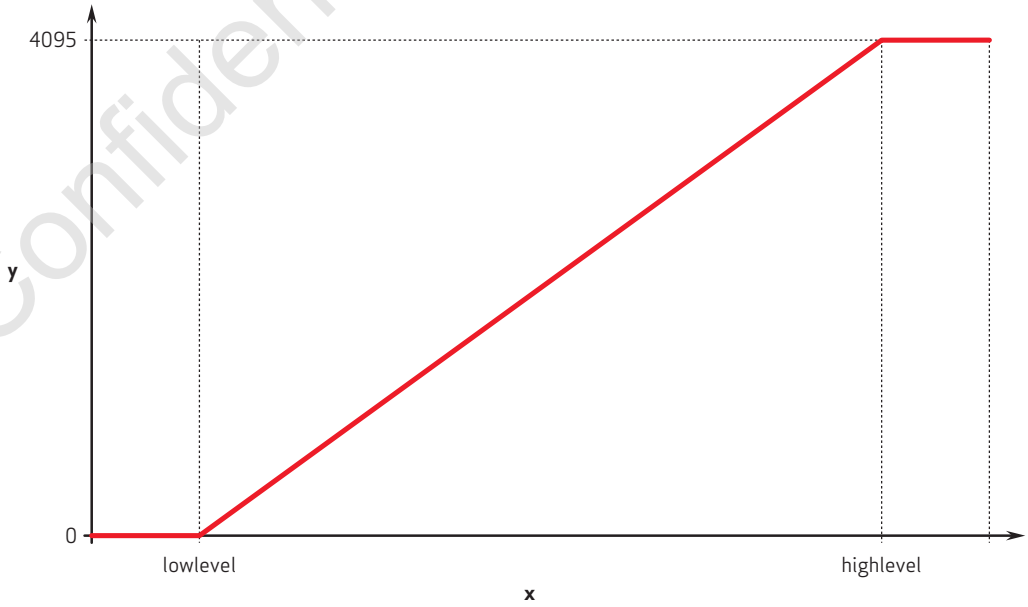
3.16 linear stretch

Linear stretch is designed to automatically enhance the contrast of images. As shown in **figure 3-29**, the input signal between low level and high level will be stretched to [0, 4095]. An input signal below low level will be cut to 0 and an input signal over high level will be saturated to 4095.

By default, high level and low level will be adjusted according to the image content. Two thresholds: threshold1 {0x8020780E, 0x8020780F, 0x80207810} ({0x8020782E, 0x8020782F, 0x80207830} for second sensor) for low level, threshold2 {0x80207811, 0x80207812, 0x80207813} ({0x80207831, 0x80207832, 0x80207833} for second sensor) for high level, and two step value: step1 0x80207804[3:0] (0x80207824[3:0] for second sensor) for low level; step2 0x80207804[7:4] (0x80207804[7:4] for second sensor) for high level, are used for the low/high level adjust: If current low (high) level > threshold1 (2) + minimum_number/2, then new low (high) level = current low (high) level - step1 (2). If current low (high) level < threshold1 (2) - minimum_number/2, then new low (high) level = current low (high) level + step1 (2); else, new low (high) level = current low (high) level.

The minimum_number is selected by 0x80207800[3:2] (0x80207820[3:2] for second sensor), 2'b00: 0x0400; 2'b01: 0x0800; 2'b10: 0x1000; 2'b11: 0x2000. Low level and high level can also be manually set. Setting 0x80207800[1:0] (0x80207820 for second sensor) to 2'b10 will enable the manually set mode. Registers {0x8020780A, 0x8020780B} ({0x8020782A, 0x8020782B} for second sensor) are used as manual low level, registers {0x8020780C, 0x8020780D} ({0x8020782C, 0x8020782D} for second sensor) are used as manual high level.

figure 3-29 stretch graph



$$y = \begin{cases} 0 & \text{if } x \le \text{LowLevel} \\ \dfrac{1023 \times (x - \text{LowLevel})}{(\text{HighLevel} - \text{LowLevel})} & \text{if LowLevel} < x < \text{HighLevel} \\ 1023 & \text{if } x \ge \text{h HighLevel} \end{cases}$$

490_BDS_3_29

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table 3-28 linear stretch registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x80206011	SNR0_ISP_CTRL_1	0xFF	RW	Bit[7]: Sensor 0 OVPB CIP enable Bit[6]: Sensor 0 OVPB RAW DNS enable Bit[5]: Sensor 0 stretch enable Bit[4]: Sensor 0 tone-mapping enable Bit[3]: Sensor 0 HDR statistic enable Bit[2]: Sensor 0 AEC_AGC enable Bit[1]: Sensor 0 curve AWB enable Bit[0]: Sensor 0 combine enable
0x80206031	SNR1_ISP_CTRL_1	0xFF	RW	Bit[7]: Sensor 1 OVPB CIP enable Bit[6]: Sensor 1 OVPB RAW DNS enable Bit[5]: Sensor 1 stretch enable Bit[4]: Sensor 1 tone-mapping enable Bit[3]: Sensor 1 HDR statistic enable Bit[2]: Sensor 1 AEC_AGC enable Bit[1]: Sensor 1 curve AWB enable Bit[0]: Sensor 1 combine enable
0x80207800	SNR0_STRETCH_CTRL_0	0x09	RW	Bit[7:4]: Reserved Bit[3:2]: Sensor 0 stretch minimum number Bit[1:0]: Sensor 0 manual/auto low/high level select 10: Manual set low/high level Others: Auto calculated low/high level
0x80207801	SNR0_STRETCH_CTRL_1	0x06	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 stretch maximum low level
0x80207802	SNR0_STRETCH_CTRL_2	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 stretch minimum low level
0x80207803	SNR0_STRETCH_CTRL_3	0x10	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 stretch minimum high level
0x80207804	SNR0_STRETCH_CTRL_4	0x41	RW	Bit[7:4]: Sensor 0 stretch step2 value Bit[3:0]: Sensor 0 stretch step1 value
0x80207806	SNR0_STRETCH_CTRL_5	0xB0	RW	Bit[7:1]: Reserved Bit[0]: Sensor 0 stretch initial low level[8]
0x80207807	SNR0_STRETCH_CTRL_6	0x40	RW	Bit[7:0]: Sensor 0 stretch initial low level[7:0]
0x80207808	SNR0_STRETCH_CTRL_7	0x0F	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 stretch initial high level[11:8]
0x80207809	SNR0_STRETCH_CTRL_8	0xFC	RW	Bit[7:0]: Sensor 0 stretch initial high level[7:0]
0x8020780A	SNR0_STRETCH_CTRL_9	0x00	RW	Bit[7:1]: Reserved Bit[0]: Sensor 0 stretch manual low level[8]
0x8020780B	SNR0_STRETCH_CTRL_A	0x40	RW	Bit[7:0]: Sensor 0 stretch manual low level[7:0]

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table 3-28 linear stretch registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x8020780C	SNR0_STRETCH _CTRL_B	0x0F	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 stretch manual high level[11:8]
0x8020780D	SNR0_STRETCH _CTRL_C	0xFC	RW	Bit[7:0]: Sensor 0 stretch manual high level[7:0]
0x8020780E	SNR0_STRETCH _CTRL_E	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 stretch threshold 1[20:16]
0x8020780F	SNR0_STRETCH _CTRL_F	0x3B	RW	Bit[7:0]: Sensor 0 stretch threshold 1[15:8]
0x80207810	SNR0_STRETCH _CTRL_10	0xC4	RW	Bit[7:0]: Sensor 0 stretch threshold 1[7:0]
0x80207811	SNR0_STRETCH _CTRL_11	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 stretch threshold 2[20:16]
0x80207812	SNR0_STRETCH _CTRL_12	0x3B	RW	Bit[7:0]: Sensor 0 stretch threshold 2[15:8]
0x80207813	SNR0_STRETCH _CTRL_13	0xC4	RW	Bit[7:0]: Sensor 0 stretch threshold 2[7:0]
0x80207814	SNR0_STRETCH _RO_LLV_H	–	R	Bit[7:1]: Reserved Bit[0]: Sensor 0 stretch current low level[8]
0x80207816	SNR0_STRETCH _RO_LLV_L	–	R	Bit[7:0]: Sensor 0 stretch current low level[7:0]
0x80207817	SNR0_STRETCH _RO_HLV_H	–	R	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 stretch current high level[11:8]
0x80207818	SNR0_STRETCH _RO_HLV_L	–	R	Bit[7:0]: Sensor 0 stretch current high level[7:0]
0x80207819	SNR0_STRETCH _RO_GAIN_H	–	R	Bit[7:1]: Reserved Bit[0]: Sensor 0 stretch gain[8]
0x8020781A	SNR0_STRETCH _RO_GAIN_L	–	R	Bit[7:0]: Sensor 0 stretch gain[7:0]
0x80207820	SNR1_STRETCH _CTRL_0	0x09	RW	Bit[7:4]: Reserved Bit[3:2]: Sensor 1 stretch minimum number Bit[1:0]: Sensor 1 manual/auto low/high level select: 10: Manual set low/high level Others: Auto calculated low/high level
0x80207821	SNR1_STRETCH _CTRL_1	0x06	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 stretch maximum low level
0x80207822	SNR1_STRETCH _CTRL_2	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 stretch minimum low level

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table 3-28 linear stretch registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x80207823	SNR1_STRETCH _CTRL_3	0x10	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 stretch minimum high level
0x80207824	SNR1_STRETCH _CTRL_4	0x41	RW	Bit[7:4]: Sensor 1 stretch step2 value Bit[3:0]: Sensor 1 stretch step1 value
0x80207826	SNR1_STRETCH _CTRL_5	0x00	RW	Bit[7:1]: Reserved Bit[0]: Sensor 1 stretch initial low level[8]
0x80207827	SNR1_STRETCH _CTRL_6	0x40	RW	Bit[7:0]: Sensor 1 stretch initial low level[7:0]
0x80207828	SNR1_STRETCH _CTRL_7	0x0F	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 stretch initial high level[11:8]
0x80207829	SNR1_STRETCH _CTRL_8	0xFC	RW	Bit[7:0]: Sensor 1 stretch initial high level[7:0]
0x8020782A	SNR1_STRETCH _CTRL_9	0x00	RW	Bit[7:1]: Reserved Bit[0]: Sensor 1 stretch manual low level[8]
0x8020782B	SNR1_STRETCH _CTRL_A	0x40	RW	Bit[7:0]: Sensor 1 stretch manual low level[7:0]
0x8020782C	SNR1_STRETCH _CTRL_B	0x0F	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 stretch manual high level[11:8]
0x8020782D	SNR1_STRETCH _CTRL_C	0xFC	RW	Bit[7:0]: Sensor 1 stretch manual high level[7:0]
0x8020782E	SNR1_STRETCH _CTRL_E	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 stretch threshold 1[20:16]
0x8020782F	SNR1_STRETCH _CTRL_F	0x3B	RW	Bit[7:0]: Sensor 1 stretch threshold 1[15:8]
0x80207830	SNR1_STRETCH _CTRL_10	0xC4	RW	Bit[7:0]: Sensor 1 stretch threshold 1[7:0]
0x80207831	SNR1_STRETCH _CTRL_11	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 stretch threshold 2[20:16]
0x80207832	SNR1_STRETCH _CTRL_12	0x3B	RW	Bit[7:0]: Sensor 1 stretch threshold 2[15:8]
0x80207833	SNR1_STRETCH _CTRL_13	0xC4	RW	Bit[7:0]: Sensor 1 stretch threshold 2[7:0]
0x80207834	SNR1_STRETCH _RO_LLV_H	–	R	Bit[7:1]: Reserved Bit[0]: Sensor 1 stretch current low level[8]
0x80207836	SNR1_STRETCH _RO_LLV_L	–	R	Bit[7:0]: Sensor 1 stretch current low level[7:0]

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table 3-28 linear stretch registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x80207837	SNR1_STRETCH _RO_HLV_H	–	R	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 stretch current high level[11:8]
0x80207838	SNR1_STRETCH _RO_HLV_L	–	R	Bit[7:0]: Sensor 1 stretch current high level[7:0]
0x80207839	SNR1_STRETCH _RO_GAIN_H	–	R	Bit[7:1]: Reserved Bit[0]: Sensor 1 stretch gain[8]
0x8020783A	SNR1_STRETCH _RO_GAIN_L	–	R	Bit[7:0]: Sensor 1 stretch gain[7:0]

3.17 color interpolation (CIP)

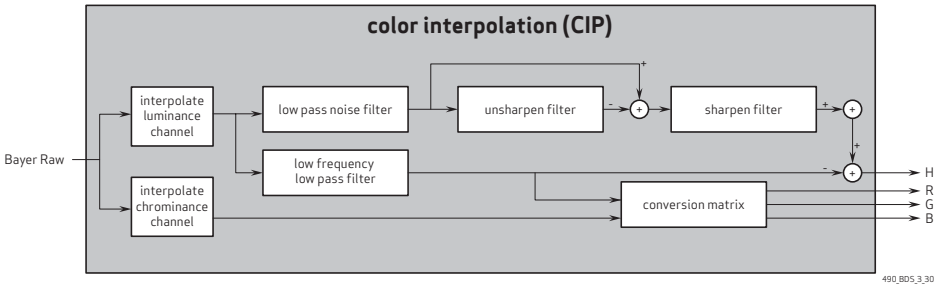
The next step in processing is to convert the Bayer format to an RGB per pixel format. The two missing color values in each pixel are interpolated from the neighboring pixels. CIP also implements other functions such as de-noise, edge sharpening and binning/sub-sampling artifacts correction. The noise filtering and sharpness enhancement is performed in the luminance channel only (see figure 3-30). The input of the CIP block is the Bayer RAW data and the output of the block is R, G and B signals of each pixel, plus a high frequency luminance signal H.

3.17.1 color interpolation

There are two parameters that will change the color aliasing in the high frequency region and green channel interpolation on color edges.

- anti_aliasing (register 0x80207890[6] for first sensor and 0x802078A7[6] for the second sensor): when set to 1, it will help reduce color aliasing in regions with horizontal or vertical high frequency details.
- cip_option (register 0x80207890[4] for first sensor and 0x802078A7[4] for the second sensor): when set to 1, it will help reduce black dot artifacts in diagonal color edges, but it may also introduce color aliasing in regions with high frequency in diagonal directions.

figure 3-30 CIP block diagram



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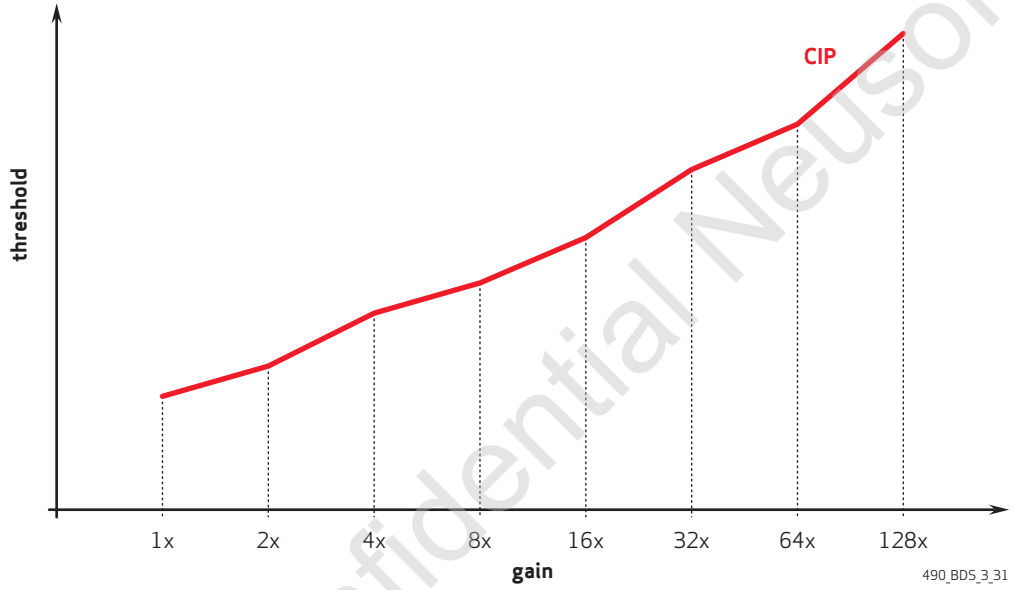
3.17.2 DNS in CIP

Similar to other DNS modules, there is a noise list to control the de-noise level at different AGC gain. Because it is applied in the linear domain, it also has a slope parameter to increase the de-noise level in light tone.

- noise_y_slp (register 0x80207880[7:4] for first sensor and 0x80207897[7:4] for the second sensor): in the linear domain, the shot noise will increase with the signal level, so it will be the same for linear raw image, the dark tone has lower noise level than the mid tone and light tone. This parameter is used to increase the DNS level with the signal level. With a larger value, it will reduce more noise in light tone.

figure 3-31 CIP DNS diagram



The CIP DNS noise threshold list registers are 0x80207882~0x80207889 (0x80207899~0x802078A0 are for the second sensor).

table 3-29 CIP registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x80207880	SNR0_CIP_CTRL_0	0x80	RW	Sensor 0 Control Signals Bit[7:4]: Noise Y slope Bit[3:0]: Local sharpen
0x80207882	SNR0_CIP_NOISE_LIST_0	0x00	RW	Bit[7:0]: Sensor 0 noise list[0]
0x80207883	SNR0_CIP_NOISE_LIST_1	0x00	RW	Bit[7:0]: Sensor 0 noise list[1]
0x80207884	SNR0_CIP_NOISE_LIST_2	0x00	RW	Bit[7:0]: Sensor 0 noise list[2]
0x80207885	SNR0_CIP_NOISE_ LIST_3	0x00	RW	Bit[7:0]: Sensor 0 noise list[3]

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table 3-29 CIP registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x80207886	SNR0_CIP_NOISE_ LIST_4	0x00	RW	Bit[7:0]: Sensor 0 noise list[4]
0x80207887	SNR0_CIP_NOISE_ LIST_5	0x00	RW	Bit[7:0]: Sensor 0 noise list[5]
0x80207888	SNR0_CIP_NOISE_ LIST_6	0x00	RW	Bit[7:0]: Sensor 0 noise list[6]
0x80207889	SNR0_CIP_NOISE_ LIST_7	0x00	RW	Bit[7:0]: Sensor 0 noise list[7]
0x8020788A	SNR0_CIP_MIN_ SHARPEN	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 minimum sharpen
0x8020788B	SNR0_CIP_MAX_ SHARPEN	0x0C	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 maximum sharpen
0x8020788C	SNR0_CIP_MIN_ DETAIL	0x08	RW	Bit[7:0]: Sensor 0 minimum detail
0x8020788D	SNR0_CIP_MAX_ DETAIL	0x0C	RW	Bit[7:0]: Sensor 0 maximum detail
0x8020788E	SNR0_CIP_MIN_ SHARPEN_GAIN	0x02	RW	Bit[7:0]: Sensor 0 minimum sharpen gain
0x8020788F	SNR0_CIP_MAX_ SHARPEN_GAIN	0x10	RW	Bit[7:0]: Sensor 0 maximum sharpen gain
0x80207897	SNR1_CIP_CTRL_0	0x80	RW	Sensor 1 Control Bit[7:4]: Noise Y slope Bit[3:0]: Local sharpen
0x80207899	SNR1_CIP_NOISE_ LIST_0	0x00	RW	Bit[7:0]: Sensor 1 noise list[0]
0x8020789A	SNR1_CIP_NOISE_ LIST_1	0x00	RW	Bit[7:0]: Sensor 1 noise list[1]
0x8020789B	SNR1_CIP_NOISE_ LIST_2	0x00	RW	Bit[7:0]: Sensor 1 noise list[2]
0x8020789C	SNR1_CIP_NOISE_ LIST_3	0x00	RW	Bit[7:0]: Sensor 1 noise list[3]
0x8020789D	SNR1_CIP_NOISE_ LIST_4	0x00	RW	Bit[7:0]: Sensor 1 noise list[4]
0x8020789E	SNR1_CIP_NOISE_ LIST_5	0x00	RW	Bit[7:0]: Sensor 1 noise list[5]
0x8020789F	SNR1_CIP_NOISE_ LIST_6	0x00	RW	Bit[7:0]: Sensor 1 noise list[6]
0x802078A0	SNR1_CIP_NOISE_ LIST_7	0x00	RW	Bit[7:0]: Sensor 1 noise list[7]
0x802078A1	SNR1_CIP_MIN_ SHARPEN	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 minimum sharpen
0x802078A2	SNR1_CIP_MAX_ SHARPEN	0x0C	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 maximum sharpen
0x802078A3	SNR1_CIP_MIN_ DETAIL	0x08	RW	Bit[7:0]: Sensor 1 minimum detail
0x802078A4	SNR1_CIP_MAX_ DETAIL	0x0C	RW	Bit[7:0]: Sensor 1 maximum detail

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table 3-29 CIP registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x802078A5	SNR1_CIP_MIN_ SHARPEN_GAIN	0x02	RW	Bit[7:0]: Sensor 1 minimum sharpen gain
0x802078A6	SNR1_CIP_MAX_ SHARPEN_GAIN	0x10	RW	Bit[7:0]: Sensor 1 maximum sharpen gain

3.17.3 edge sharpening

CIP still includes two edge sharpening methods. The first method is the commonly used un-sharp mask, which is applied equally everywhere in the image. The second method will locally adjust the edge sharpness, which is named local-sharpen.

The basic idea of the un-sharp mask method is to amplify the high frequency component of the image signal and then add it back to enhance the edge. It is controlled by two parameters: one is the sharpening level, which is the gain used to amplify the high frequency and the other is a threshold, which is used to control the small high frequency that will not be amplified. When the sensor gain increases, the noise level will also increase. So the sharpening level and the threshold should adjust with gain to get better image quality. As shown in **figure 3-32**, when the sensor gain is lower than min_sharpen_gain, the sharpening level will be max_sharpen and the threshold will be min_detail. When sensor gain is larger than max_sharpen_gain, the sharpening level will be min_sharpen and the threshold will be max_detail. When the sensor gain is within the range of [min_sharpen_gain, max_sharpen_gain], the sharpening level and the threshold will be linearly interpolated.

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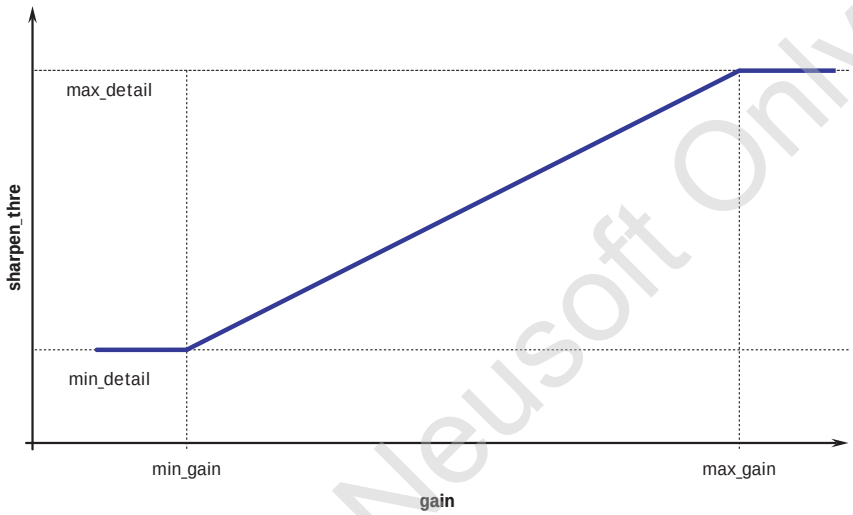
figure 3-32 sharpen curve

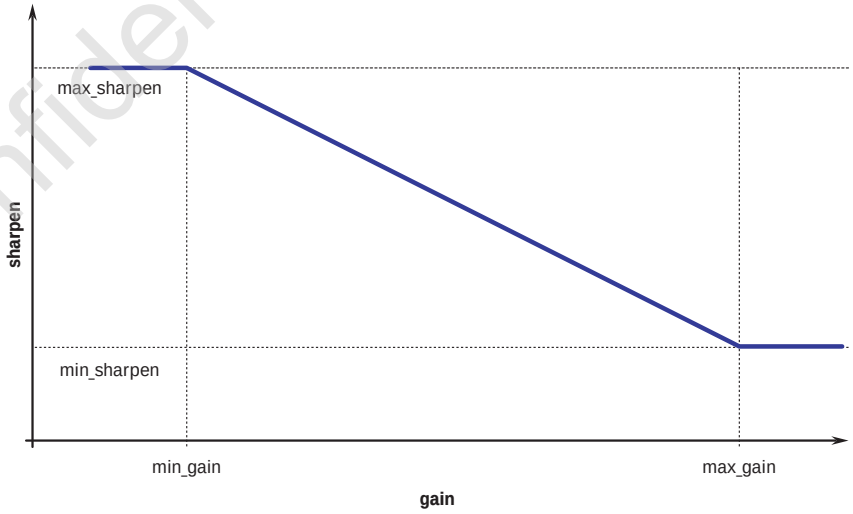


note 1 register settings for max_detail first sensor: 0x8020788D, second sensor: 0x802078A4

note 2 register settings for min_detail first sensor: 0x8020788C, second sensor: 0x802078A3

note 3 register settings for max_gain first sensor: 0x8020788E, second sensor: 0x802078A5

note 4 register settings for max_gain first sensor: 0x8020788F, second sensor: 0x802078A6



note 1 register settings for max_sharpen first sensor: 0x8020788B, second sensor: 0x802078A2

note 2 register settings for min_sharpen first sensor: 0x8020788A, second sensor: 0x802078A1

note 3 register settings for min_gain first sensor: 0x8020788E, second sensor: 0x802078A5

note 4 register settings for max_gain first sensor: 0x8020788F, second sensor: 0x802078A6

490_BDS_3_32

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table 3-30 sharpness registers

address	register name	default value	R/W	description
0x8020788A	SNR0_CIP_MIN_SHARPEN	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 minimum sharpen
0x8020788B	SNR0_CIP_MAX_SHARPEN	0x0C	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 maximum sharpen
0x8020788C	SNR0_CIP_MIN_DETAIL	0x08	RW	Bit[7:0]: Sensor 0 minimum detail
0x8020788D	SNR0_CIP_MAX_DETAIL	0x0C	RW	Bit[7:0]: Sensor 0 maximum detail
0x8020788E	SNR0_CIP_MIN_SHARPEN _GAIN	0x02	RW	Bit[7:0]: Sensor 0 minimum sharpen gain
0x8020788F	SNR0_CIP_MAX_SHARPEN _GAIN	0x10	RW	Bit[7:0]: Sensor 0 maximum sharpen gain
0x802078A1	SNR1_CIP_MIN_SHARPEN	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 minimum sharpen
0x802078A2	SNR1_CIP_MAX_SHARPEN	0x0C	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 maximum sharpen
0x802078A3	SNR1_CIP_MIN_DETAIL	0x08	RW	Bit[7:0]: Sensor 1 minimum detail
0x802078A4	SNR1_CIP_MAX_DETAIL	0x0C	RW	Bit[7:0]: Sensor 1 maximum detail
0x802078A5	SNR1_CIP_MIN_SHARPEN _GAIN	0x02	RW	Bit[7:0]: Sensor 1 minimum sharpen gain
0x802078A6	SNR1_CIP_MAX_SHARPEN _GAIN	0x10	RW	Bit[7:0]: Sensor 1 maximum sharpen gain

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3.18 color matrix (CMX)

Due to spectrum crosstalk, a color correction matrix (CCM) must be applied on the R, G and B values of each pixel to improve the color fidelity. The optimal color correction matrix depends on pixel QE spectrum response and the spectrum of the light source. To optimize for sensor crosstalk, the OV490 can use three color matrices calibrated with three different color temperatures. Alternatively, a single matrix can be used for all color temperatures (0x80207931[1] for first sensor and 0x80207981[1] for the second sensor).

The following equation shows the corrected RGB vector on the left-hand side and the multiplication of a 3x3 matrix and the white-balanced sensor RGB vector on the right-hand side. The matrix should be balanced; otherwise, the white point in sensor RGB space cannot be transformed into the white point in target RGB space. So, one 3x3 matrix only needs six independent parameters (c00, c01, … , c21).

$$\begin{bmatrix} B' \\ G' \\ R' \end{bmatrix} = \frac{1}{1024} \begin{bmatrix} 1024 + C_{00} + C_{01} & -C_{00} & -C_{01} \\ -C_{10} & 1024 + C_{10} + C_{11} & -C_{11} \\ -C_{20} & -C_{21} & 1024 + C_{20} + C_{21} \end{bmatrix} \begin{bmatrix} B \\ G \\ R \end{bmatrix}$$

The current color matrix is automatically estimated based on current CT calculated from the AWB gain. CT is defined as:

CT = (blue channel AWB gain × 128)/(red channel AWB gain)

In daylight, the CT value will be smaller than the CT value under incandescent light. Three thresholds can be defined (ctlist0, ctlist1, ctlist2) in the following equation, which will divide the CT space into three regions. The current matrix can be calculated based on which region the current CT belongs to.

$$M_{3x3} = \begin{cases} D_{3x3}, & ct \le ct_0 \\ D_{3x3} + \dfrac{(C_{3x3} - D_{3x3})(ct - ct_0)}{ct_1 - ct_0}, & ct_0 < ct \le ct_1 \\ C_{3x3} + \dfrac{(A_{3x3} - C_{3x3})(ct - ct_0)}{ct_1 - ct_0}, & ct_1 < ct \le ct_2 \\ A_{3x3}, & ct_2 < ct \end{cases}$$

note 1 D65: 0x80207900-0x8020790B (0x80207950-0x8020795B for the second sensor)

note 2 A: 0x8020790C-0x80207917 (0x8020795B-0x80207967 for the second sensor)

note 3 CWF: 0x80207918-0x80207923 (0x80207968-0x80207973 for the second sensor)

note 4 CTlist0: {0x80207928, 0x80207929} ({0x80207978, 0x80207979} for the second sensor)

note 5 CTlist1: {0x8020792A, 0x8020792B} ({0x8020797A, 0x8020797B} for the second sensor)

note 6 CTlist2: {0x8020792C, 0x8020792D} ({0x8020797C, 0x8020797D} for the second sensor)

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The values in the CCMs are absolute values. The sign for the six parameters given for each CCM are given in registers 0x8020792E (0x8020797E for the second sensor), 0x8020792F (0x8020797F for the second sensor) and 0x80207930 (0x80207980 for the second sensor) for D, A, and CWF light, respectively.

When the sensor gain is high, the OV490 can automatically reduce saturation enabled by register 0x80207931[0] (0x80207981[0] for the second sensor). When the sensor gain is between cmx_min_gain (0x80207934 for first sensor and 0x80207084 for the second sensor) and cmx_max_gain (0x80207935 for first sensor and 0x80207985 for the second sensor), the factor will be linearly interpolated as shown in **figure 3-33**. A factor of 64 means the color saturation will be the same as the original color. A factor smaller than 64 will reduce the color saturation. A factor of 0 will reduce color image to a black/white image.

Manual control of the BR gain is enabled though 0x80207924[4] (0x80207974[4] for the second sensor). The B gain and R gain are 12 bits wide and given by registers {0x80207924[3:0], 0x80207925} ({0x80207974[3:0],0x80207975} for the second sensor) for B gain and registers {0x80207926[3:0],0x80207927} (0x80207976[3:0],0x80207977} for the second sensor) for R gain.

figure 3-33 CMX curve diagram

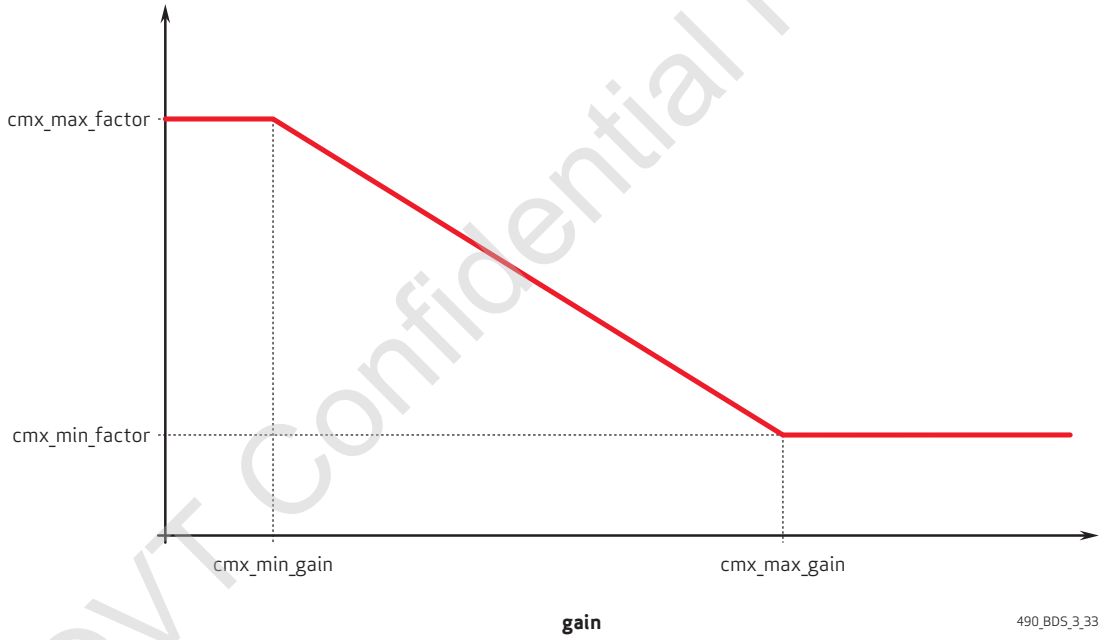

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table 3-31 CMX registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x80207900	SNR0_CMX_CTRL00	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for Day mode C00[11:8]
0x80207901	SNR0_CMX_CTRL01	0x00	RW	Bit[7:0]: Sensor 0 absolute value for Day mode C00[7:0]
0x80207902	SNR0_CMX_CTRL02	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for Day mode C01[11:8]
0x80207903	SNR0_CMX_CTRL03	0x00	RW	Bit[7:0]: Sensor 0 absolute value for Day mode C01[7:0]
0x80207904	SNR0_CMX_CTRL04	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for Day mode C10[11:8]
0x80207905	SNR0_CMX_CTRL05	0x00	RW	Bit[7:0]: Sensor 0 absolute value for Day mode C10[7:0]
0x80207906	SNR0_CMX_CTRL06	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for Day mode C11[11:8]
0x80207907	SNR0_CMX_CTRL07	0x00	RW	Bit[7:0]: Sensor 0 absolute value for Day mode C11[7:0]
0x80207908	SNR0_CMX_CTRL08	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for Day mode C20[11:8]
0x80207909	SNR0_CMX_CTRL09	0x00	RW	Bit[7:0]: Sensor 0 absolute value for Day mode C20[7:0]
0x8020790A	SNR0_CMX_CTRL0A	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for Day mode C21[11:8]
0x8020790B	SNR0_CMX_CTRL0B	0x00	RW	Bit[7:0]: Sensor 0 absolute value for Day mode C21[7:0]
0x8020790C	SNR0_CMX_CTRL0C	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for A mode C00[11:8]
0x8020790D	SNR0_CMX_CTRL0D	0x00	RW	Bit[7:0]: Sensor 0 absolute value for A mode C00[7:0]
0x8020790E	SNR0_CMX_CTRL0E	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for A mode C01[11:8]

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table 3-31 CMX registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x8020790F	SNR0_CMX_CTRL0F	0x00	RW	Bit[7:0]: Sensor 0 absolute value for A mode C01[7:0]
0x80207910	SNR0_CMX_CTRL10	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for A mode C10[11:8]
0x80207911	SNR0_CMX_CTRL11	0x00	RW	Bit[7:0]: Sensor 0 absolute value for A mode C10[7:0]
0x80207912	SNR0_CMX_CTRL12	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for A mode C11[11:8]
0x80207913	SNR0_CMX_CTRL13	0x00	RW	Bit[7:0]: Sensor 0 absolute value for A mode C11[7:0]
0x80207914	SNR0_CMX_CTRL14	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for A mode C20[11:8]
0x80207915	SNR0_CMX_CTRL15	0x00	RW	Bit[7:0]: Sensor 0 absolute value for A mode C20[7:0]
0x80207916	SNR0_CMX_CTRL16	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for A mode C21[11:8]
0x80207917	SNR0_CMX_CTRL17	0x00	RW	Bit[7:0]: Sensor 0 absolute value for A mode C21[7:0]
0x80207918	SNR0_CMX_CTRL18	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for CWF mode C00[11:8]
0x80207919	SNR0_CMX_CTRL19	0x00	RW	Bit[7:0]: Sensor 0 absolute value for CWF mode C00[7:0]
0x8020791A	SNR0_CMX_CTRL1A	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for CWF mode C01[11:8]
0x8020791B	SNR0_CMX_CTRL1B	0x00	RW	Bit[7:0]: Sensor 0 absolute value for CWF mode C01[7:0]
0x8020791C	SNR0_CMX_CTRL1C	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for CWF mode C10[11:8]
0x8020791D	SNR0_CMX_CTRL1D	0x00	RW	Bit[7:0]: Sensor 0 absolute value for CWF mode C10[7:0]
0x8020791E	SNR0_CMX_CTRL1E	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for CWF mode C11[11:8]

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table 3-31 CMX registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x8020791F	SNR0_CMX_CTRL1F	0x00	RW	Bit[7:0]: Sensor 0 absolute value for CWF mode C11[7:0]
0x80207920	SNR0_CMX_CTRL20	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for CWF mode C20[11:8]
0x80207921	SNR0_CMX_CTRL21	0x00	RW	Bit[7:0]: Sensor 0 absolute value for CWF mode C20[7:0]
0x80207922	SNR0_CMX_CTRL22	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for CWF mode C21[11:8]
0x80207923	SNR0_CMX_CTRL23	0x00	RW	Bit[7:0]: Sensor 0 absolute value for CWF mode C21[7:0]
0x80207928	SNR0_CMX_CTRL28	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 color matrix CT list0[9:8]
0x80207929	SNR0_CMX_CTRL29	0x00	RW	Bit[7:0]: Sensor 0 color matrix CT list0[7:0]
0x8020792A	SNR0_CMX_CTRL2A	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 color matrix CT list1[9:8]
0x8020792B	SNR0_CMX_CTRL2B	0x00	RW	Bit[7:0]: Sensor 0 color matrix CT list1[7:0]
0x8020792C	SNR0_CMX_CTRL2C	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 color matrix CT list2[9:8]
0x8020792D	SNR0_CMX_CTRL2D	0x00	RW	Bit[7:0]: Sensor 0 color matrix CT list2[7:0]
0x8020792E	SNR0_CMX_CTRL2E	0x00	RW	Bit[7:6]: Reserved Bit[5]: Sensor 0 sign bits for C00 Day mode Bit[4]: Sensor 0 sign bits for C01 Day mode Bit[3]: Sensor 0 sign bits for C10 Day mode Bit[2]: Sensor 0 sign bits for C11 Day mode Bit[1]: Sensor 0 sign bits for C20 Day mode Bit[0]: Sensor 0 sign bits for C21 Day mode
0x8020792F	SNR0_CMX_CTRL2F	0x00	RW	Bit[7:6]: Reserved Bit[5]: Sensor 0 sign bits for C00 A mode Bit[4]: Sensor 0 sign bits for C01 A mode Bit[3]: Sensor 0 sign bits for C10 A mode Bit[2]: Sensor 0 sign bits for C11 A mode Bit[1]: Sensor 0 sign bits for C20 A mode Bit[0]: Sensor 0 sign bits for C21 A mode

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table 3-31 CMX registers (sheet 4 of 8)

address	register name	default value	R/W	description
0x80207930	SNR0_CMX_CTRL30	0x00	RW	Bit[7:6]: Reserved Bit[5]: Sensor 0 sign bits for C00 CWF mode Bit[4]: Sensor 0 sign bits for C01 CWF mode Bit[3]: Sensor 0 sign bits for C10 CWF mode Bit[2]: Sensor 0 sign bits for C11 CWF mode Bit[1]: Sensor 0 sign bits for C20 CWF mode Bit[0]: Sensor 0 sign bits for C21 CWF mode
0x80207931	SNR0_CMX_CTRL31	0x01	RW	Bit[7:2]: Reserved Bit[1]: Sensor 0 auto CT enable Bit[0]: Sensor 0 auto factor enable
0x80207932	SNR0_CMX_CTRL32	0x40	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 maximum factor value
0x80207933	SNR0_CMX_CTRL33	0x40	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 minimum factor value
0x80207934	SNR0_CMX_CTRL34	0x07	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 minimum gain
0x80207935	SNR0_CMX_CTRL35	0x0F	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 maximum gain
0x80207950	SNR1_CMX_CTRL00	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for Day mode C00[11:8]
0x80207951	SNR1_CMX_CTRL01	0x00	RW	Bit[7:0]: Sensor 1 absolute value for Day mode C00[7:0]
0x80207952	SNR1_CMX_CTRL02	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for Day mode C01[11:8]
0x80207953	SNR1_CMX_CTRL03	0x00	RW	Bit[7:0]: Sensor 1 absolute value for Day mode C01[7:0]
0x80207954	SNR1_CMX_CTRL04	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for Day mode C10[11:8]
0x80207955	SNR1_CMX_CTRL05	0x00	RW	Bit[7:0]: Sensor 1 absolute value for Day mode C10[7:0]
0x80207956	SNR1_CMX_CTRL06	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for Day mode C11[11:8]

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table 3-31 CMX registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x80207957	SNR1_CMX_CTRL07	0x00	RW	Bit[7:0]: Sensor 1 absolute value for Day mode C11[7:0]
0x80207958	SNR1_CMX_CTRL08	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for Day mode C20[11:8]
0x80207959	SNR1_CMX_CTRL09	0x00	RW	Bit[7:0]: Sensor 1 absolute value for Day mode C20[7:0]
0x8020795A	SNR1_CMX_CTRL0A	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for Day mode C21[11:8]
0x8020795B	SNR1_CMX_CTRL0B	0x00	RW	Bit[7:0]: Sensor 1 absolute value for Day mode C21[7:0]
0x8020795C	SNR1_CMX_CTRL0C	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for A mode C00[11:8]
0x8020795D	SNR1_CMX_CTRL0D	0x00	RW	Bit[7:0]: Sensor 1 absolute value for A mode C00[7:0]
0x8020795E	SNR1_CMX_CTRL0E	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for A mode C01[11:8]
0x8020795F	SNR1_CMX_CTRL0F	0x00	RW	Bit[7:0]: Sensor 1 absolute value for A mode C01[7:0]
0x80207960	SNR1_CMX_CTRL10	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for A mode C10[11:8]
0x80207961	SNR1_CMX_CTRL11	0x00	RW	Bit[7:0]: Sensor 1 absolute value for A mode C10[7:0]
0x80207962	SNR1_CMX_CTRL12	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for A mode C11[11:8]
0x80207963	SNR1_CMX_CTRL13	0x00	RW	Bit[7:0]: Sensor 1 absolute value for A mode C11[7:0]
0x80207964	SNR1_CMX_CTRL14	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for A mode C20[11:8]
0x80207965	SNR1_CMX_CTRL15	0x00	RW	Bit[7:0]: Sensor 1 absolute value for A mode C20[7:0]
0x80207966	SNR1_CMX_CTRL16	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for A mode C21[11:8]

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table 3-31 CMX registers (sheet 6 of 8)

address	register name	default value	R/W	description
0x80207967	SNR1_CMX_CTRL17	0x00	RW	Bit[7:0]: Sensor 1 absolute value for A mode C21[7:0]
0x80207968	SNR1_CMX_CTRL18	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for CWF mode C00[11:8]
0x80207969	SNR1_CMX_CTRL19	0x00	RW	Bit[7:0]: Sensor 1 absolute value for CWF mode C00[7:0]
0x8020796A	SNR1_CMX_CTRL1A	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for CWF mode C01[11:8]
0x8020796B	SNR1_CMX_CTRL1B	0x00	RW	Bit[7:0]: Sensor 1 absolute value for CWF mode C01[7:0]
0x8020796C	SNR1_CMX_CTRL1C	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for CWF mode C10[11:8]
0x8020796D	SNR1_CMX_CTRL1D	0x00	RW	Bit[7:0]: Sensor 1 absolute value for CWF mode C10[7:0]
0x8020796E	SNR1_CMX_CTRL1E	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for CWF mode C11[11:8]
0x8020796F	SNR1_CMX_CTRL1F	0x00	RW	Bit[7:0]: Sensor 1 absolute value for CWF mode C11[7:0]
0x80207970	SNR1_CMX_CTRL20	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for CWF mode C20[11:8]
0x80207971	SNR1_CMX_CTRL21	0x00	RW	Bit[7:0]: Sensor 1 absolute value for CWF mode C20[7:0]
0x80207972	SNR1_CMX_CTRL22	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for CWF mode C21[11:8]
0x80207973	SNR1_CMX_CTRL23	0x00	RW	Bit[7:0]: Sensor 1 absolute value for CWF mode C21[7:0]
0x80207978	SNR1_CMX_CTRL28	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 color matrix CT list0[9:8]
0x80207979	SNR1_CMX_CTRL29	0x80	RW	Bit[7:0]: Sensor 1 color matrix CT list0[7:0]
0x8020797A	SNR1_CMX_CTRL2A	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 color matrix CT list1[9:8]
0x8020797B	SNR1_CMX_CTRL2B	0x80	RW	Bit[7:0]: Sensor 1 color matrix CT list1[7:0]

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table 3-31 CMX registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x8020797C	SNR1_CMX_CTRL2C	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 color matrix CT list2[9:8]
0x8020797D	SNR1_CMX_CTRL2D	0x80	RW	Bit[7:0]: Sensor 1 color matrix CT list2[7:0]
0x8020797E	SNR1_CMX_CTRL2E	0x00	RW	Bit[7:6]: Reserved Bit[5]: Sensor 1 sign bits for C00 Day mode Bit[4]: Sensor 1 sign bits for C01 Day mode Bit[3]: Sensor 1 sign bits for C10 Day mode Bit[2]: Sensor 1 sign bits for C11 Day mode Bit[1]: Sensor 1 sign bits for C20 Day mode Bit[0]: Sensor 1 sign bits for C21 Day mode
0x8020797F	SNR1_CMX_CTRL2F	0x00	RW	Bit[7:6]: Reserved Bit[5]: Sensor 1 sign bits for C00 A mode Bit[4]: Sensor 1 sign bits for C01 A mode Bit[3]: Sensor 1 sign bits for C10 A mode Bit[2]: Sensor 1 sign bits for C11 A mode Bit[1]: Sensor 1 sign bits for C20 A mode Bit[0]: Sensor 1 sign bits for C21 A mode
0x80207980	SNR1_CMX_CTRL30	0x00	RW	Bit[7:6]: Reserved Bit[5]: Sensor 1 sign bits for C00 CWF mode Bit[4]: Sensor 1 sign bits for C01 CWF mode Bit[3]: Sensor 1 sign bits for C10 CWF mode Bit[2]: Sensor 1 sign bits for C11 CWF mode Bit[1]: Sensor 1 sign bits for C20 CWF mode Bit[0]: Sensor 1 sign bits for C21 CWF mode
0x80207981	SNR1_CMX_CTRL31	0x01	RW	Bit[7:2]: Reserved Bit[1]: Sensor 1 auto CT enable Bit[0]: Sensor 1 auto factor enable
0x80207982	SNR1_CMX_CTRL32	0x40	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 maximum factor value
0x80207983	SNR1_CMX_CTRL33	0x40	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 minimum factor value
0x80207984	SNR1_CMX_CTRL34	0x07	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 minimum gain
0x80207985	SNR1_CMX_CTRL35	0x0F	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 maximum gain
0x80207990	CMX1_CTRL40	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: snr1_abs_cmx00[11:8]

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table 3-31 CMX registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x80207991	CMX1_CTRL41	0x00	RW	Bit[7:0]: snr1_abs_cmx00[7:0]
0x80207992	CMX1_CTRL42	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: snr1_abs_cmx01[11:8]
0x80207993	CMX1_CTRL43	0x00	RW	Bit[7:0]: snr1_abs_cmx01[7:0]
0x80207994	CMX1_CTRL44	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: snr1_abs_cmx10[11:8]
0x80207995	CMX1_CTRL45	0x00	RW	Bit[7:0]: snr1_abs_cmx10[7:0]
0x80207996	CMX1_CTRL46	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: snr1_abs_cmx11[11:8]
0x80207997	CMX1_CTRL47	0x00	RW	Bit[7:0]: snr1_abs_cmx11[7:0]
0x80207998	CMX1_CTRL48	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: snr1_abs_cmx20[11:8]
0x80207999	CMX1_CTRL49	0x00	RW	Bit[7:0]: snr1_abs_cmx20[7:0]
0x8020799A	CMX1_CTRL4A	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: snr1_abs_cmx21[11:8]
0x8020799B	CMX1_CTRL4B	0x00	RW	Bit[7:0]: snr1_abs_cmx21[7:0]
0x8020799C	CMX1_CTRL4C	0x00	RW	Bit[7:6]: Reserved Bit[5]: sign_snr1_cmx00 Bit[4]: sign_snr1_cmx01 Bit[3]: sign_snr1_cmx10 Bit[2]: sign_snr1_cmx11 Bit[1]: sign_snr1_cmx20 Bit[0]: sign_snr1_cmx21

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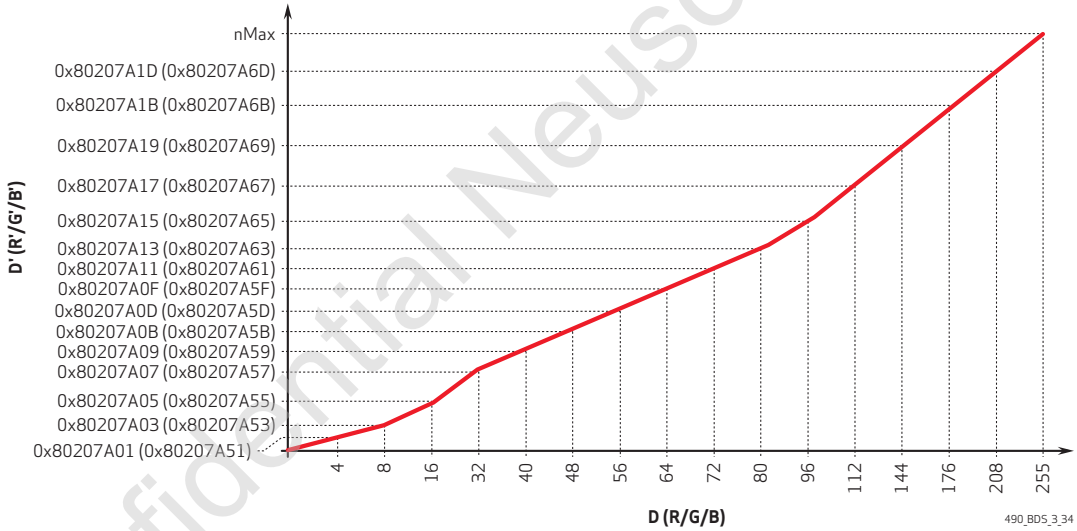
3.19 RGB gamma

Gamma correction is used to compensate for the non-linearity in intensity reproduction of the display device. The gamma correction must increase with dynamic range to maintain the same shadow of gray similar to the display.

A gamma curve is used for R/G/B channel correction. Register 0x80207A01~80207A1D for the curve gamma list (0x80207A51~0x80207A6D for the second sensor). **figure 3-34** shows the gamma curve used for different D.

```
D'=Y[i-1]+((D-X[i-1])×(Y[i] -Y[i-1]))/(X[i]-X[i-1])
```

figure 3-34 gamma curve diagram



For 10-bit or 12-bit YUV output, the applied gamma curve will automatically multiply by 4 or 16 to match the requirement. This means, for 10-bit or 12-bit YUV output, the precision of the gamma curve list may be a bit lower. To resolve this issue, a manual mode is reserved for the user to get a more precise 10-bit or 12-bit curve list. Setting register bit 0x80207A20[0] (0x80207A70[0] for the second sensor) to high will enable the manual curve list. The manual curve list is defined as follows:

```
curve list 0 : {0x80207A26, 0x80207A27}({0x80207A76, 0x80207A77});
curve list 1 : {0x80207A28, 0x80207A29}({0x80207A78, 0x80207A79})
curve list 2 : {0x80207A2A, 0x80207A2B}({0x80207A7A, 0x80207A7B})
curve list 3 : {0x80207A2C, 0x80207A2D}({0x80207A7C, 0x80207A7D})
curve list 4 : {0x80207A2E, 0x80207A2F}({0x80207A7E, 0x80207A7F})
curve list 5 : {0x80207A30, 0x80207A31}({0x80207A80, 0x80207A81})
curve list 6 : {0x80207A32, 0x80207A33}({0x80207A82, 0x80207A83})
```

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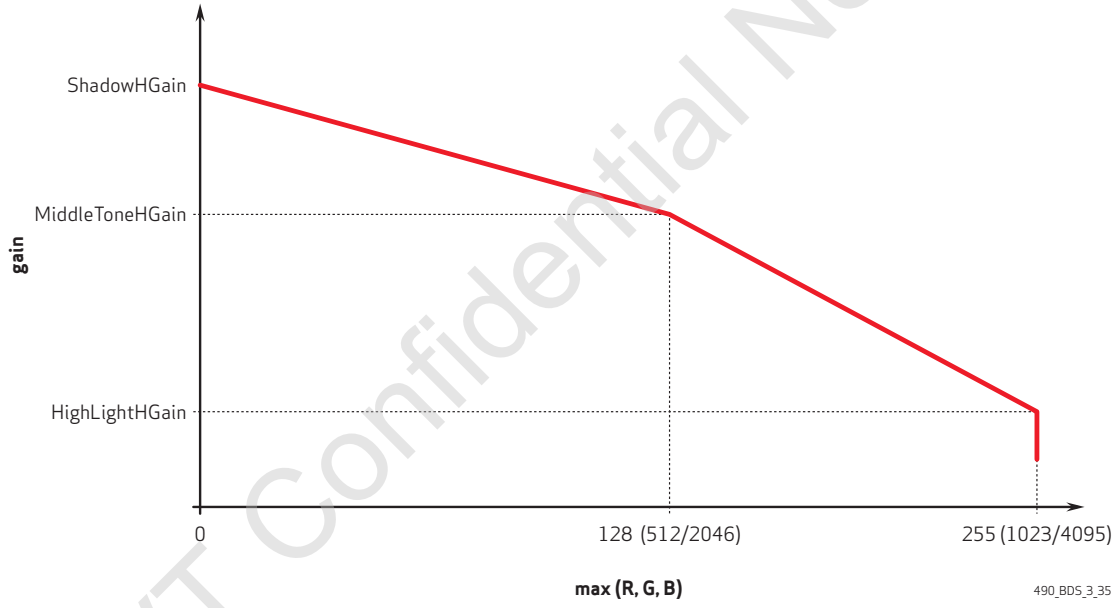
```
curve list 7 : {0x80207A34, 0x80207A35}({0x80207A84, 0x80207A85})
curve list 8 : {0x80207A36, 0x80207A37}({0x80207A86, 0x80207A87})
curve list 9 : {0x80207A38, 0x80207A39}({0x80207A88, 0x80207A89})
curve list 10: {0x80207A3A, 0x80207A3B}({0x80207A8A, 0x80207A8B})
curve list 11: {0x80207A3C, 0x80207A3D}({0x80207A8C, 0x80207A8D})
curve list 12: {0x80207A3E, 0x80207A3F}({0x80207A8E, 0x80207A8F})
curve list 13: {0x80207A40, 0x80207A41}({0x80207A90, 0x80207A91})
curve list 14: {0x80207A42, 0x80207A43}({0x80207A92, 0x80207A93})
```

A gain will be applied to Y channel based on the maximum R, G or B channel data.

figure 3-35 gain of high frequency information



Shadow H gain is calculated based on the real gain and register 0x80207A1F (0x80207A6F for the second sensor) defines the maximum value of shadow H gain. Register 0x80207A22 (0x80207A72 for the second sensor) defines middle tone H gain and 0x80207A24 (0x80207A74 for the second sensor) defines high light, H gain. It provides the user a method to adjust the noise level in shadow, mid-tone, and high light.

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table 3-32 RGB gamma registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x80207A01	SNR0_GAMMA_CTRL_01	0x12	RW	Bit[7:0]: Sensor 0 gamma Y list00 before auto bit-shift
0x80207A03	SNR0_GAMMA_CTRL_03	0x20	RW	Bit[7:0]: Sensor 0 gamma Y list01 before auto bit-shift
0x80207A05	SNR0_GAMMA_CTRL_05	0x3B	RW	Bit[7:0]: Sensor 0 gamma Y list02 before auto bit-shift
0x80207A07	SNR0_GAMMA_CTRL_07	0x5D	RW	Bit[7:0]: Sensor 0 gamma Y list03 before auto bit-shift
0x80207A09	SNR0_GAMMA_CTRL_09	0x6A	RW	Bit[7:0]: Sensor 0 gamma Y list04 before auto bit-shift
0x80207A0B	SNR0_GAMMA_CTRL_0B	0x76	RW	Bit[7:0]: Sensor 0 gamma Y list05 before auto bit-shift
0x80207A0D	SNR0_GAMMA_CTRL_0D	0x81	RW	Bit[7:0]: Sensor 0 gamma Y list06 before auto bit-shift
0x80207A0F	SNR0_GAMMA_CTRL_0F	0x8B	RW	Bit[7:0]: Sensor 0 gamma Y list07 before auto bit-shift
0x80207A11	SNR0_GAMMA_CTRL_11	0x96	RW	Bit[7:0]: Sensor 0 gamma Y list08 before auto bit-shift
0x80207A13	SNR0_GAMMA_CTRL_13	0x9E	RW	Bit[7:0]: Sensor 0 gamma Y list09 before auto bit-shift
0x80207A15	SNR0_GAMMA_CTRL_15	0xAE	RW	Bit[7:0]: Sensor 0 gamma Y list0a before auto bit-shift
0x80207A17	SNR0_GAMMA_CTRL_17	0xBC	RW	Bit[7:0]: Sensor 0 gamma Y list0b before auto bit-shift
0x80207A19	SNR0_GAMMA_CTRL_19	0xCF	RW	Bit[7:0]: Sensor 0 gamma Y list0c before auto bit-shift
0x80207A1B	SNR0_GAMMA_CTRL_1B	0xDE	RW	Bit[7:0]: Sensor 0 gamma Y list0d before auto bit-shift
0x80207A1D	SNR0_GAMMA_CTRL_1D	0xEC	RW	Bit[7:0]: Sensor 0 gamma Y list0e before auto bit-shift
0x80207A1F	SNR0_GAMMA_MAX_SHD_H_GAIN	0xFF	RW	Bit[7:0]: Sensor 0 gamma m_nMaxShadowHGain[7:0]
0x80207A20	SNR0_GAMMA_PARA_MANUAL_EN	0x00	RW	Bit[7:1]: Reserved Bit[0]: Sensor 0 gamma manual control enable
0x80207A22	SNR0_GAMMA_MID_TONE_H_GAIN	0x6E	RW	Bit[7:0]: Sensor 0 gamma m_nMiddleToneHGain[7:0]

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table 3-32 RGB gamma registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x80207A24	SNR0_GAMMA_HIGH_ LIGHT_H_GAIN	0x10	RW	Bit[7:0]: Sensor 0 gamma m_nHighLightHGain[7:0]
0x80207A26	SNR0_GAMMA_26	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list00[11:8]
0x80207A27	SNR0_GAMMA_27	0xE0	RW	Bit[7:0]: Sensor 0 manual gamma Y list00[7:0]
0x80207A28	SNR0_GAMMA_28	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list01[11:8]
0x80207A29	SNR0_GAMMA_29	0xA0	RW	Bit[7:0]: Sensor 0 manual gamma Y list01[7:0]
0x80207A2A	SNR0_GAMMA_2A	0x03	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list02[11:8]
0x80207A2B	SNR0_GAMMA_2B	0x10	RW	Bit[7:0]: Sensor 0 manual gamma Y list02[7:0]
0x80207A2C	SNR0_GAMMA_2C	0x05	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list03[11:8]
0x80207A2D	SNR0_GAMMA_2D	0xA0	RW	Bit[7:0]: Sensor 0 manual gamma Y list03[7:0]
0x80207A2E	SNR0_GAMMA_2E	0x06	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list04[11:8]
0x80207A2F	SNR0_GAMMA_2F	0x90	RW	Bit[7:0]: Sensor 0 manual gamma Y list04[7:0]
0x80207A30	SNR0_GAMMA_30	0x07	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list05[11:8]
0x80207A31	SNR0_GAMMA_31	0x50	RW	Bit[7:0]: Sensor 0 manual gamma Y list05[7:0]
0x80207A32	SNR0_GAMMA_32	0x07	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list06[11:8]
0x80207A33	SNR0_GAMMA_33	0xE0	RW	Bit[7:0]: Sensor 0 manual gamma Y list06[7:0]
0x80207A34	SNR0_GAMMA_34	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list07[11:8]

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table 3-32 RGB gamma registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x80207A35	SNR0_GAMMA_35	0x80	RW	Bit[7:0]: Sensor 0 manual gamma Y list07[7:0]
0x80207A36	SNR0_GAMMA_36	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list08[11:8]
0x80207A37	SNR0_GAMMA_37	0xF0	RW	Bit[7:0]: Sensor 0 manual gamma Y list08[7:0]
0x80207A38	SNR0_GAMMA_38	0x09	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list09[11:8]
0x80207A39	SNR0_GAMMA_39	0x60	RW	Bit[7:0]: Sensor 0 manual gamma Y list09[7:0]
0x80207A3A	SNR0_GAMMA_3A	0x0A	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list0a[11:8]
0x80207A3B	SNR0_GAMMA_3B	0x30	RW	Bit[7:0]: Sensor 0 manual gamma Y list0a[7:0]
0x80207A3C	SNR0_GAMMA_3C	0x0A	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list0b[11:8]
0x80207A3D	SNR0_GAMMA_3D	0xF0	RW	Bit[7:0]: Sensor 0 manual gamma Y list0b[7:0]
0x80207A3E	SNR0_GAMMA_3E	0x0C	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list0c[11:8]
0x80207A3F	SNR0_GAMMA_3F	0x40	RW	Bit[7:0]: Sensor 0 manual gamma Y list0c[7:0]
0x80207A40	SNR0_GAMMA_40	0x0D	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list0d[11:8]
0x80207A41	SNR0_GAMMA_41	0x70	RW	Bit[7:0]: Sensor 0 manual gamma Y list0d[7:0]
0x80207A42	SNR0_GAMMA_42	0x0E	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list0e[11:8]
0x80207A43	SNR0_GAMMA_43	0x80	RW	Bit[7:0]: Sensor 0 manual gamma Y list0e[7:0]
0x80207A51	SNR1_GAMMA_CTRL_01	0x12	RW	Bit[7:0]: Sensor 1 gamma Y list00 before auto bit-shift

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table 3-32 RGB gamma registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x80207A53	SNR1_GAMMA_CTRL_03	0x20	RW	Bit[7:0]: Sensor 1 gamma Y list01 before auto bit-shift
0x80207A55	SNR1_GAMMA_CTRL_05	0x3B	RW	Bit[7:0]: Sensor 1 gamma Y list02 before auto bit-shift
0x80207A57	SNR1_GAMMA_CTRL_07	0x5D	RW	Bit[7:0]: Sensor 1 gamma Y list03 before auto bit-shift
0x80207A59	SNR1_GAMMA_CTRL_09	0x6A	RW	Bit[7:0]: Sensor 1 gamma Y list04 before auto bit-shift
0x80207A5B	SNR1_GAMMA_CTRL_0B	0x76	RW	Bit[7:0]: Sensor 1 gamma Y list05 before auto bit-shift
0x80207A5D	SNR1_GAMMA_CTRL_0D	0x81	RW	Bit[7:0]: Sensor 1 gamma Y list06 before auto bit-shift
0x80207A5F	SNR1_GAMMA_CTRL_0F	0x8B	RW	Bit[7:0]: Sensor 1 gamma Y list07 before auto bit-shift
0x80207A61	SNR1_GAMMA_CTRL_11	0x96	RW	Bit[7:0]: Sensor 1 gamma Y list08 before auto bit-shift
0x80207A63	SNR1_GAMMA_CTRL_13	0x9E	RW	Bit[7:0]: Sensor 1 gamma Y list09 before auto bit-shift
0x80207A65	SNR1_GAMMA_CTRL_15	0xAE	RW	Bit[7:0]: Sensor 1 gamma Y list0a before auto bit-shift
0x80207A67	SNR1_GAMMA_CTRL_17	0xBC	RW	Bit[7:0]: Sensor 1 gamma Y list0b before auto bit-shift
0x80207A69	SNR1_GAMMA_CTRL_19	0xCF	RW	Bit[7:0]: Sensor 1 gamma Y list0c before auto bit-shift
0x80207A6B	SNR1_GAMMA_CTRL_1B	0xDE	RW	Bit[7:0]: Sensor 1 gamma Y list0d before auto bit-shift
0x80207A6D	SNR1_GAMMA_CTRL_1D	0xEC	RW	Bit[7:0]: Sensor 1 gamma Y list0e before auto bit-shift
0x80207A6F	SNR1_GAMMA_MAX_SHD_H_GAIN	0xFF	RW	Bit[7:0]: Sensor 1 gamma m_nMaxShadowHGain[7:0]
0x80207A70	SNR1_GAMMA_PARA_MANUAL_EN	0x00	RW	Bit[7:1]: Reserved Bit[0]: Sensor 1 gamma manual control enable
0x80207A72	SNR1_GAMMA_MID_TONE_H_GAIN	0x6E	RW	Bit[7:0]: Sensor 1 gamma m_nMiddleToneHGain[7:0]
0x80207A74	SNR1_GAMMA_HIGH_LIGHT_H_GAIN	0x10	RW	Bit[7:0]: Sensor 1 gamma m_nHighLightHGain[7:0]

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table 3-32 RGB gamma registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x80207A76	SNR1_GAMMA_26	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list00[11:8]
0x80207A77	SNR1_GAMMA_27	0xE0	RW	Bit[7:0]: Sensor 1 manual gamma Y list00[7:0]
0x80207A78	SNR1_GAMMA_28	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list01[11:8]
0x80207A79	SNR1_GAMMA_29	0xA0	RW	Bit[7:0]: Sensor 1 manual gamma Y list01[7:0]
0x80207A7A	SNR1_GAMMA_2A	0x03	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list02[11:8]
0x80207A7B	SNR1_GAMMA_2B	0x10	RW	Bit[7:0]: Sensor 1 manual gamma Y list02[7:0]
0x80207A7C	SNR1_GAMMA_2C	0x05	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list03[11:8]
0x80207A7D	SNR1_GAMMA_2D	0xA0	RW	Bit[7:0]: Sensor 1 manual gamma Y list03[7:0]
0x80207A7E	SNR1_GAMMA_2E	0x06	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list04[11:8]
0x80207A7F	SNR1_GAMMA_2F	0x90	RW	Bit[7:0]: Sensor 1 manual gamma Y list04[7:0]
0x80207A80	SNR1_GAMMA_30	0x07	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list05[11:8]
0x80207A81	SNR1_GAMMA_31	0x50	RW	Bit[7:0]: Sensor 1 manual gamma Y list05[7:0]
0x80207A82	SNR1_GAMMA_32	0x07	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list06[11:8]
0x80207A83	SNR1_GAMMA_33	0xE0	RW	Bit[7:0]: Sensor 1 manual gamma Y list06[7:0]
0x80207A84	SNR1_GAMMA_34	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list07[11:8]
0x80207A85	SNR1_GAMMA_35	0x80	RW	Bit[7:0]: Sensor 1 manual gamma Y list07[7:0]

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table 3-32 RGB gamma registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x80207A86	SNR1_GAMMA_36	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list08[11:8]
0x80207A87	SNR1_GAMMA_37	0xF0	RW	Bit[7:0]: Sensor 1 manual gamma Y list08[7:0]
0x80207A88	SNR1_GAMMA_38	0x09	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list09[11:8]
0x80207A89	SNR1_GAMMA_39	0x60	RW	Bit[7:0]: Sensor 1 manual gamma Y list09[7:0]
0x80207A8A	SNR1_GAMMA_3A	0x0A	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list0a[11:8]
0x80207A8B	SNR1_GAMMA_3B	0x30	RW	Bit[7:0]: Sensor 1 manual gamma Y list0a[7:0]
0x80207A8C	SNR1_GAMMA_3C	0x0A	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list0b[11:8]
0x80207A8D	SNR1_GAMMA_3D	0xF0	RW	Bit[7:0]: Sensor 1 manual gamma Y list0b[7:0]
0x80207A8E	SNR1_GAMMA_3E	0x0C	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list0c[11:8]
0x80207A8F	SNR1_GAMMA_3F	0x40	RW	Bit[7:0]: Sensor 1 manual gamma Y list0c[7:0]
0x80207A90	SNR1_GAMMA_40	0x0D	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list0d[11:8]
0x80207A91	SNR1_GAMMA_41	0x70	RW	Bit[7:0]: Sensor 1 manual gamma Y list0d[7:0]
0x80207A92	SNR1_GAMMA_42	0x0E	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list0e[11:8]
0x80207A93	SNR1_GAMMA_43	0x80	RW	Bit[7:0]: Sensor 1 manual gamma Y list0e[7:0]

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3.20 RGB2YUV

One of the last modules in the ISP pipeline is to convert data from RGB to YUV data path. The RGB data is noise filtered before conversion and the YUV data is filtered after conversion.

$$\begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} = M \times \begin{bmatrix} B \\ G \\ R \end{bmatrix} + \begin{bmatrix} 0 \\ H \\ H \end{bmatrix}$$

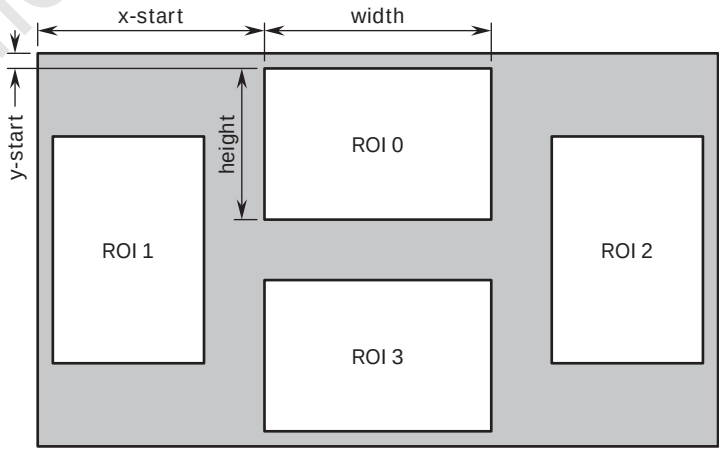
$$M = \begin{bmatrix} 29 & 150 & 77 \\ 128 & -85 & -43 \\ -21 & -107 & 128 \end{bmatrix} /256$$

note H=128 for 8-bit YUV or 512 for 10-bit YUV

3.21 YUV ROI statistics

In total, four ROI statistic windows are available. In the case of dual sensor mode, only two ROIs per input source are available. The ROI window size can be set individually, maximum size can be equal to the input image size, and the ROI area can be overlapped. A sample rate is applied to both x and y directions for each sensor. Statistic results include 16 bins Y histogram (linear partition) and average of Y, U, and V channels separately for each ROI window.

figure 3-36 YUV ROI diagram



490_BDS_3_36

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3.22 window

The output window from ISP can be manually controlled and supports both RAW path and YUV path (RAW path and YUV path share the same size/start-point information). The output window x-offset, y-offset, width and height values are controlled by IDC by default, but can be manually set as follows:

```
x-offset {0x80206023[3:0], 0x80206021} ({0x80206043[3:0], 0x80206041} for second sensor)

y-offset {0x80206023[6:4], 0x80206022} ({0x80206043[6:4], 0x80206042} for second sensor)

width {0x80206026[3:0], 0x80206024} ({0x80206046[3:0], 0x80206044} for second sensor)

height {0x80206026[6:4], 0x80206025} ({0x80206046[3:0], 0x80206045} for second sensor)
```

The manual options are enabled through register 0x80206023[7] (0x80206043[7] for the second sensor).

3.23 AEC/AGC

In the OV490, the auto exposure and gain statistics are used to determine the exposure and gain values in the next frames. There are three different exposure channels in the OV490. L channel is for long exposure, S channel is for short exposure and VS channel is for very short exposure. For the three exposure working mode, L and S use the same algorithm to compute the next frame exposure based on the weighted average of current exposure. But the difference is the L channel can change freely in range, but the S channel is limited by the new dynamic range and new L exposure value. The VS channel keeps a fixed ratio to S channel.

The long channel is used to see details in dark areas. By increasing the weight for dark pixels, AEC/AGC will tend to increase the exposure for shadows and result in more details in shadow area.

The short channel is used to see details in bright areas. By increasing the weight for high light pixels, AEC/AGC will tend to decrease the exposure for saturated areas and result in more details in bright areas.

In HDR mode, the dynamic range extension is dependent on the L, S, and VS channel exposure ratio. By default, the L/S ratio is automatically adjusted according to the dynamic range and the target stable range. S/VS ratio is fixed which is controlled by the firmware registers {0x31E/ 0x31F}. The OV490 also has a fixed exposure ratio, which is enabled by firmware register 0x2E1=0x1. The fixed ratio value is controlled by the firmware register 0x2FC. The exposure ratio here is not only the ratio of exposure time, but also includes the sensitivity ratio which is calibrated by firmware registers {0x31C, 0x31D}.

The exposure/gain control is designed to adjust the weighted frame average to a user defined range. It is important to calculate the current frame weight. The statistics for AEC/AGC is calculated as a weighted average of the user defined range. The weight of each pixel includes three parts: position weight (Wp), combination weight (Wc) and luminance weight (WY).

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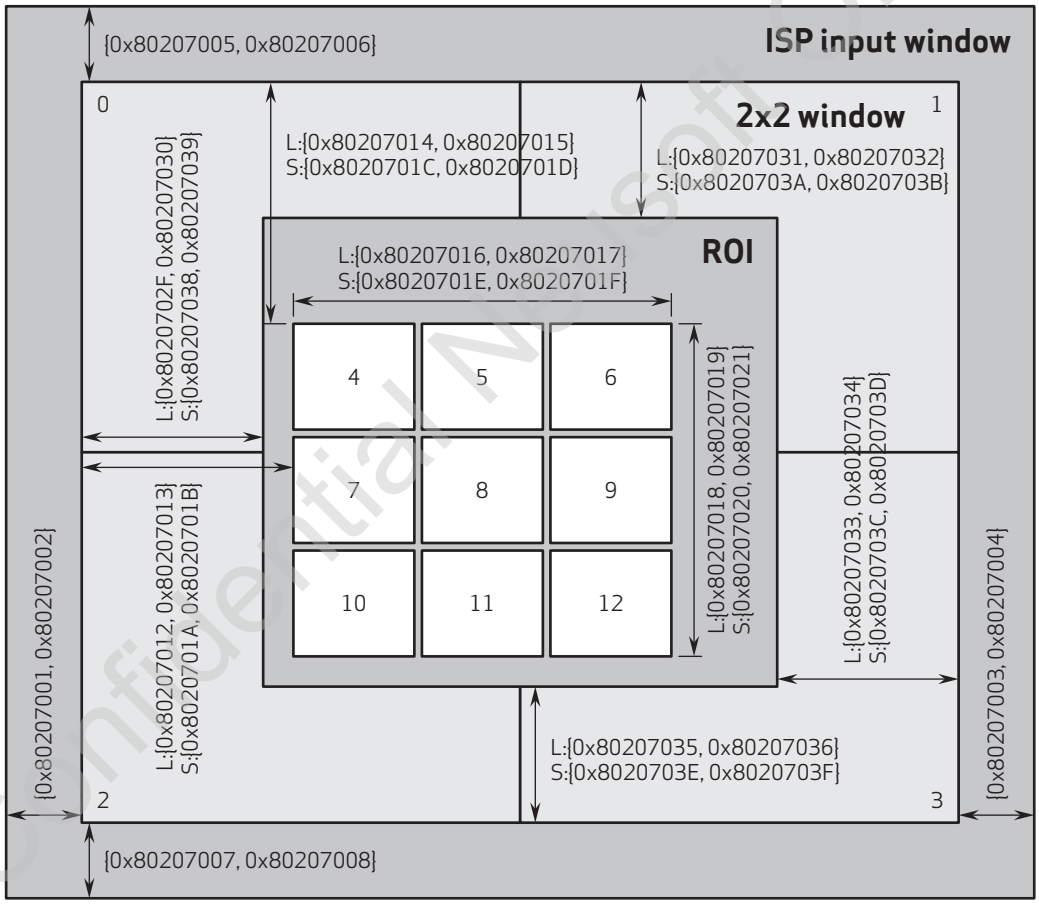
3.23.1 position weight

To measure the brightness of the current frame, the position weight is determined by the position of the pixel which also includes two independent parts: windowing weight and region of interest (ROI) weight.

figure 3-37 position window diagram



490_DS_3_37

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Instead of using the whole frame, the statistic window can be defined manually with the left offset {0x80207001[3:0], 0x80207002[7:0]}, right offset {0x80207003[3:0], 0x80207004[7:0]}, top offset {0x80207005[2:0], 0x80207006[7:0]}, and bottom offset {0x80207007[2:0], 0x80207008[7:0]} (Note:{0x80207071[3:0], 0x80207072[7:0]}, {0x80207073[3:0], 0x80207074[7:0]}, {0x80207075[2:0], 0x80207076[7:0]}, {0x80207077[2:0], 0x80207078[7:0]} is for the second sensor). The L/S/VS exposure channel uses the same statistic window size. The pixels outside of the window will not be included in the weighted average.

Respectively inside this area, a user-defined small window area (3×3 window) with left {0x80207012[3:0], 0x80207013[7:0]} ({0x8020701A[3:0], 0x8020701B[7:0]} is for short exposure), top {0x80207014[2:0], 0x80207015[7:0]} ({0x8020701C[2:0], 0x8020701D[7:0]} is for short exposure), width {0x80207016[3:0], 0x80207017[7:0]} ({0x8020701E[3:0], 0x8020701F[7:0]} is for short exposure) and height {0x80207018[2:0], 0x80207019[7:0]} ({0x80207020[2:0], 0x80207021[7:0]} is for short exposure) are divided into 9 smaller areas, 13 weights total are used for these different areas as shown in **figure 3-41**. Registers 0x80207022~0x8020702E are used for these 13 weight values (bit[7:4] is for long exposure, bit[3:0] is for short exposure). The summation of the pixel value multiplied by the zone weight will be divided by the 13 weights, so the weight is just a relative value.

Besides, a ROI weight is defined to further differentiate the weight of inner and outer pixels. Register {0x8020702F[3:0], 0x80207030[7:0]} ({0x80207038[3:0], 0x80207039[7:0]} for short exposure), {0x80207031[2:0], 0x80207032[7:0]} ({0x8020703A[2:0], 0x8020703B[7:0]} for short exposure), {0x80207033[3:0], 0x80207034[7:0]} ({0x8020703C[3:0], 0x8020703D[7:0]} for short exposure) and {0x80207035[2:0], 0x80207036[7:0]} ({0x8020703E[2:0], 0x8020703F[7:0]} for short exposure) defines left, top, right and bottom offsets of ROI area in the statistics window. Register 0x80207037[7:4] (0x80207040[7:4] for short exposure) defines ROI weight value and register 0x80207037[3:0] (0x80207040[3:0] for short exposure) defines non-ROI weight values.

There are statistics window, ROI window, 3x3 window for AE statistics window. Note these windows use offsets to determine window position. Refer to **figure 3-40** for the offset details.

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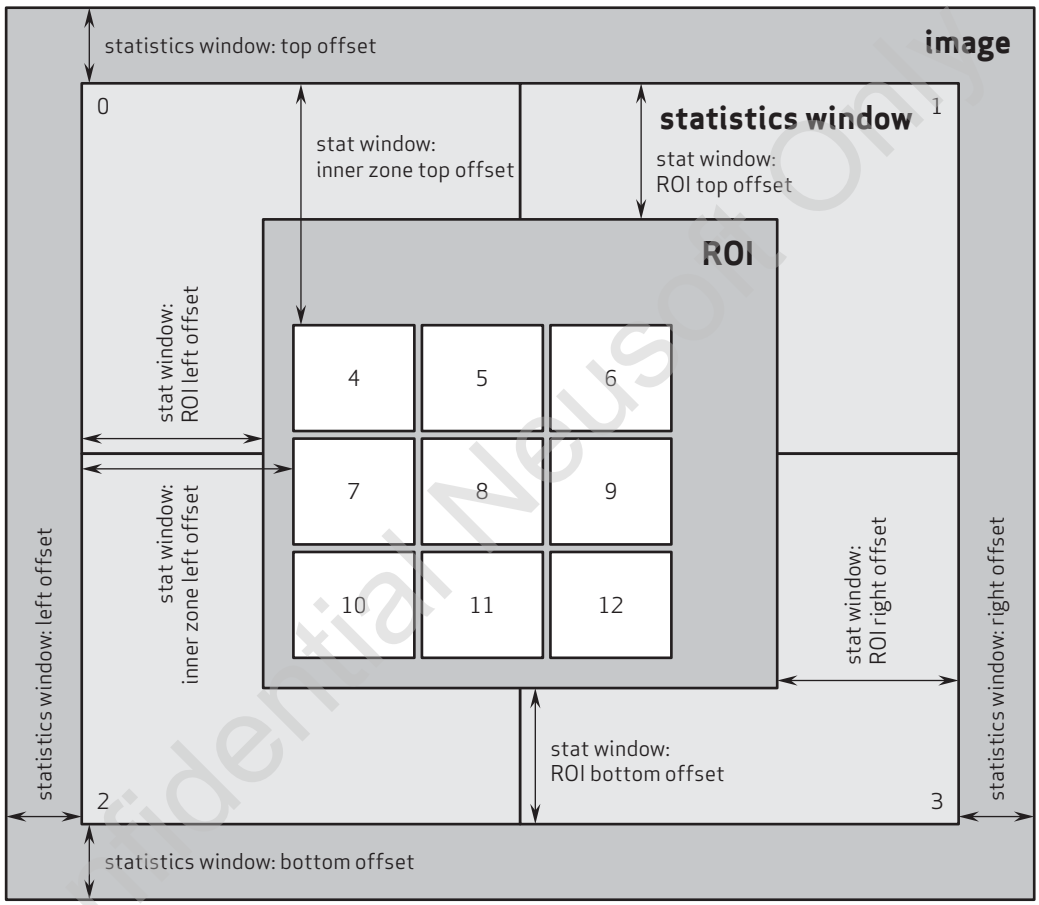
figure 3-38 statistics window diagram



490_DS_3_38

The position weight will be calculated by the statistics window weight and ROI weight. Refer to the following formula for details:

$$W_{pos} = W_{win}(x, y) * W_{ROI}(x, y)$$

$$W_{win}(x, y) = W_i \text{ if } (x, y) \in \text{ window}, 0 \le i \le 12$$

$$W_{ROI} = \begin{cases} W_i \text{ if } (x, y) \in ROI \\ W_{out} \text{ if } (x, y) \notin ROI \end{cases}$$

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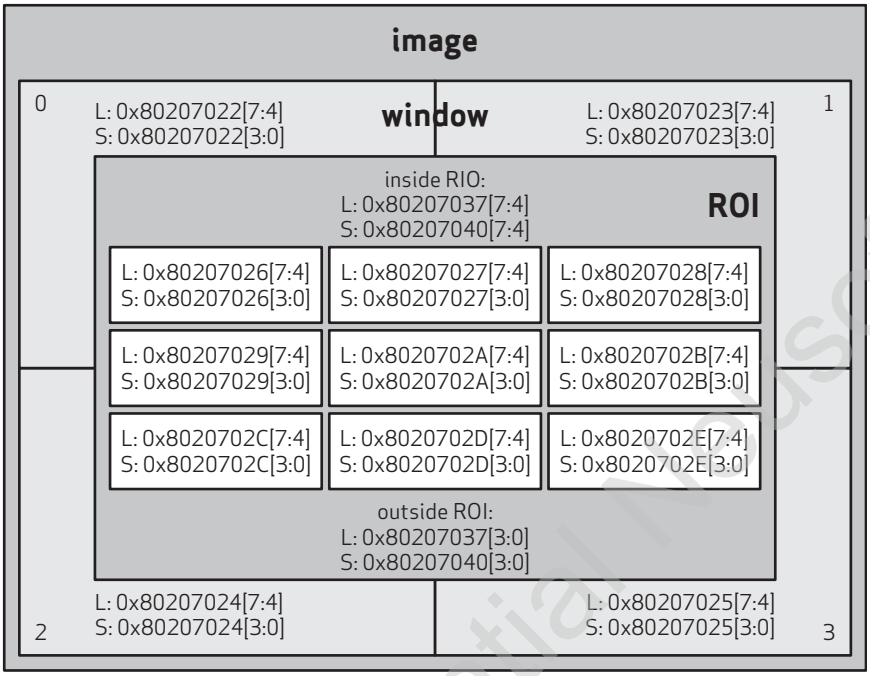
figure 3-39 position weight diagram



490_DS_3_39

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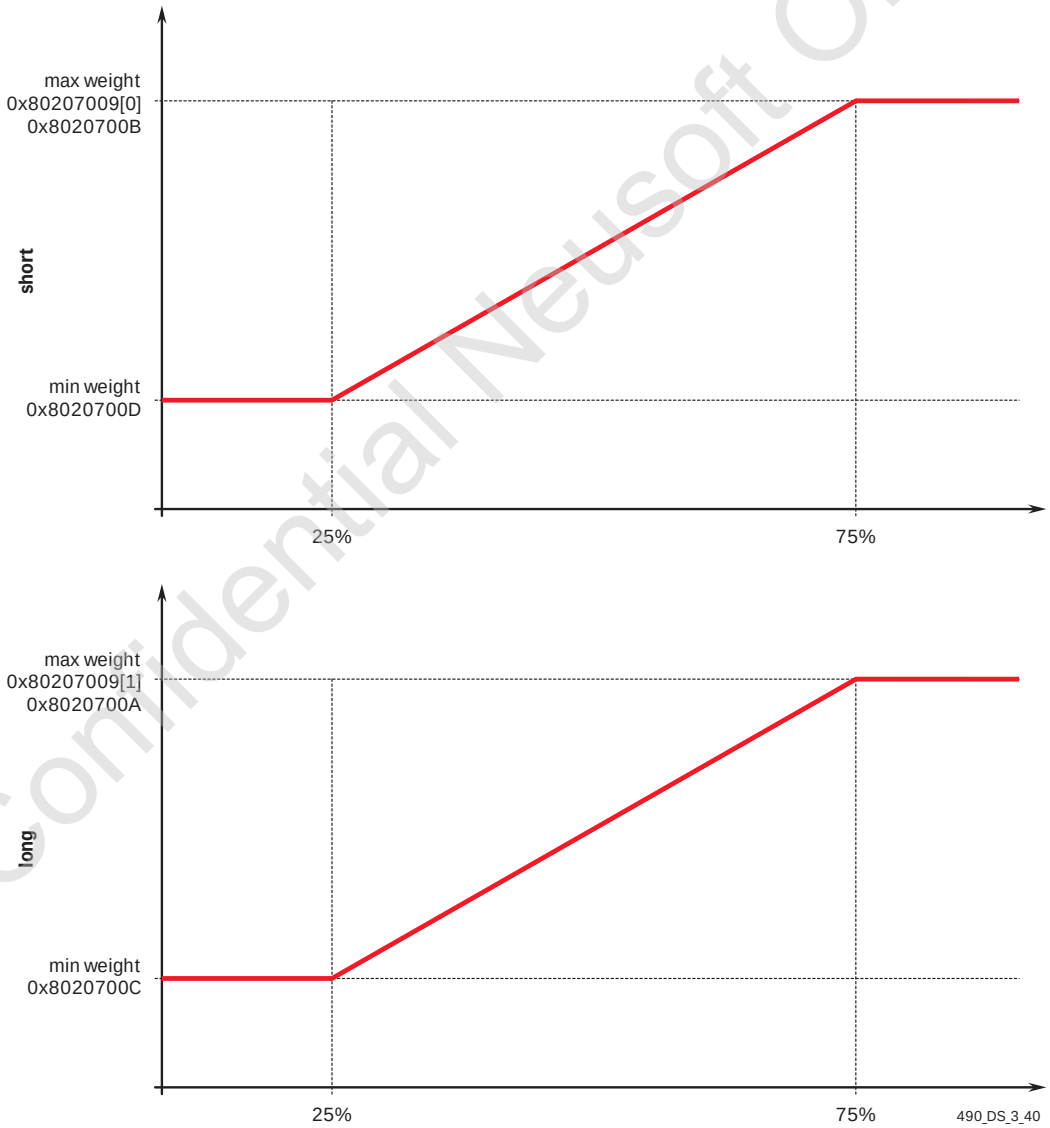
3.23.2 combination weight

The AEC/AGC weighs each pixel by wc (x,y) to calculate the average of long and short exposure image according to the combination weight wc (x,y), where c means long channel or short channel.

figure 3-40 combination weight diagram



- Wmin: Register 0x8020700C for long channel, and register 0x8020700D for short channel
- Wmax: Register {0x80207009[1], 0x8020700A[7:0]} for long channel and registers {0x80207009[0], 0x8020700B[7:0]} for short channel

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3.23.3 luminance weight

After the processing of position weight and combine weight, the last position weight will be: $W_{pos} = W_{win} \times W_{ROI}$

Then, weight for each pixel will be: $W_{pix} = W_c \times W_{pos}$

A weighted luminance summary and weight summary will be:

$$SumM = \sum (Y * W)$$

$$SumW = \sum W$$

Here, Y is the luminance of each pixel and W is former calculated pixel weight (multiplication of combine weight and position weight).

According the pixel luminance based on combine weight and position weight, it will be divided by all pixels to 3 ranges: black (low light), middle tone and high light. Register 0x80207010 defines low light threshold and register 0x80207011 defines high light threshold for luminance range divided. Each pixel will get a luminance weight based on current image's pixel luminance range. For low light (black) and high light (saturate) range, weights are calculated as shown in **figure 3-41**.

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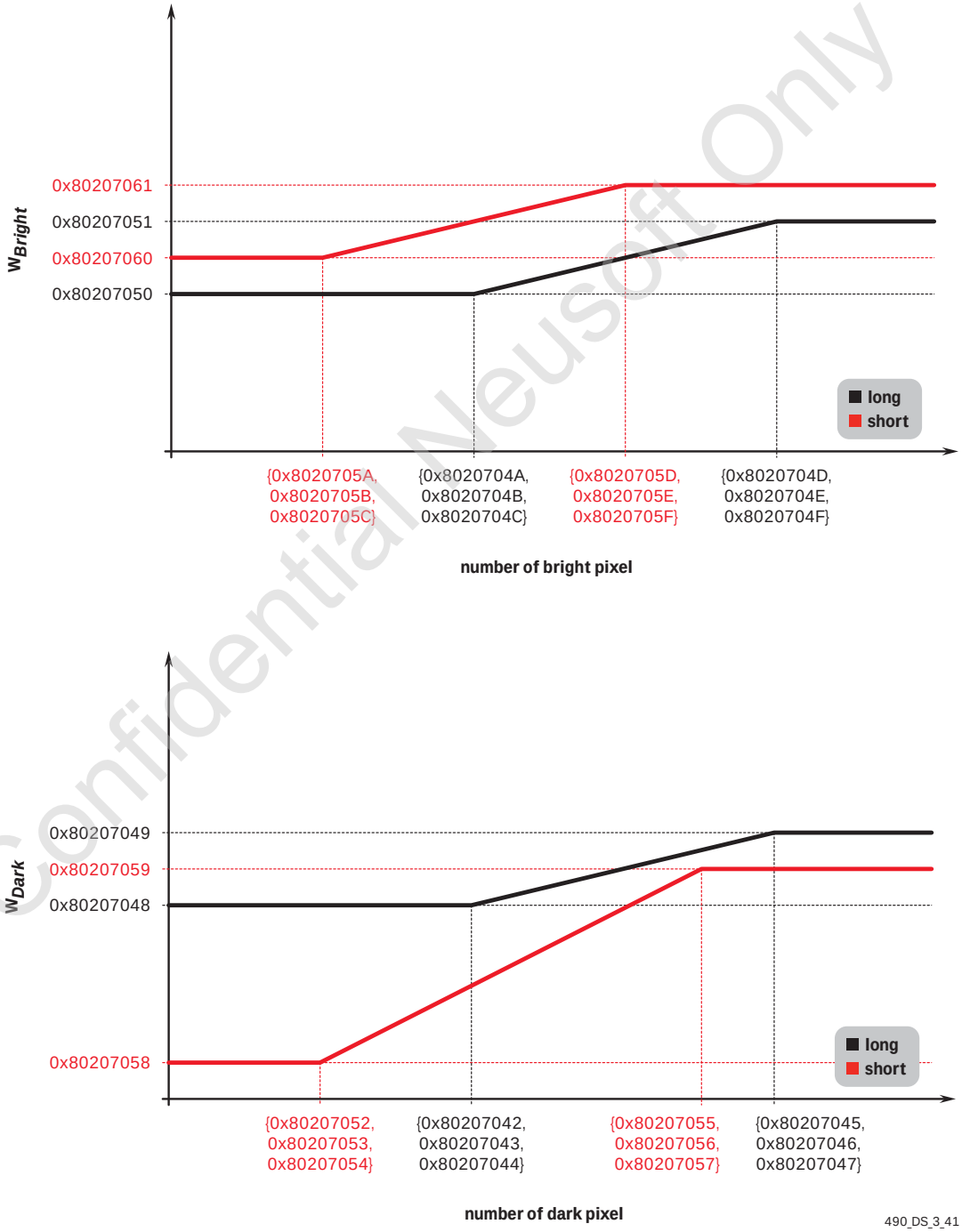
figure 3-41 luminance threshold curve



490_DS_3_41

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For middle tone range, luminance weight will always be 1.

The latest weighted luminance average will be:

MeanY = ((SMB×WLB) + SMM + (SMH×WLH)) / ((SWB×WLB) +SWM + (SWH×WLH))

Here, MeanY is the latest statistics result, SMB, WLB and SWB are the identifiers for weight luminance summary, luminance weight and weight summary of black (low light) range pixels, SMM and SWM are the identifiers for weight luminance summary and weight summary of middle tone range pixel, SMH, WLH and SWH are the identifiers for weight luminance summary luminance weight and weight summary of high light (saturate) range pixels.

note
The AEC/AGC registers for the second sensor start from 0x80207070 and the function is the same as the first sensor.

table 3-33 AEC window and weight control registers (sheet 1 of 12)

address	register name	default value	R/W	description
0x80207000	SNR0_AEC_AGC_STAT_TYPE	1'b0	RW	Bit[0]: Sensor 0 AECAGC statistic type 0: Mean value of R, G, B 1: Max value of R, G, B
0x80207001	SNR0_AEC_STAT_WIN_LEFT_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 statistic window left offset[11:8]
0x80207002	SNR0_AEC_STAT_WIN_LEFT_L	0x00	RW	Bit[7:0]: Sensor 0 statistic window left offset[7:0]
0x80207003	SNR0_AEC_STAT_WIN_RIGHT_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 statistic window right offset[11:8]
0x80207004	SNR0_AEC_STAT_WIN_RIGHT_L	0x00	RW	Bit[7:0]: Sensor 0 statistic window right offset[7:0]
0x80207005	SNR0_AEC_STAT_WIN_TOP_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 statistic window top offset[10:8]
0x80207006	SNR0_AEC_STAT_WIN_TOP_L	0x00	RW	Bit[7:0]: Sensor 0 statistic window top offset[7:0]
0x80207007	SNR0_AEC_STAT_WIN_BOTTOM_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 statistic window bottom offset[10:8]
0x80207008	SNR0_AEC_STAT_WIN_BOTTOM_L	0x14	RW	Bit[7:0]: Sensor 0 statistic window bottom offset[7:0]
0x80207009	SNR0_AEC_MAX_W_H	0x01	RW	Bit[7:2]: Reserved Bit[1]: Sensor 0 MaxW[0] high byte Bit[0]: Sensor 0 MaxW[1] high byte
0x8020700A	SNR0_AEC_MAX_W_0_L	0x20	RW	Bit[7:0]: Sensor 0 MaxW[0] low byte
0x8020700B	SNR0_AEC_MAX_W_1_L	0x00	RW	Bit[7:0]: Sensor 0 MaxW[1] low byte

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table 3-33 AEC window and weight control registers (sheet 2 of 12)

address	register name	default value	R/W	description
0x8020700C	SNR0_AEC_MIN_W_0	0x01	RW	Bit[7:0]: Sensor 0 MinW[0]
0x8020700D	SNR0_AEC_MIN_W_1	0x01	RW	Bit[7:0]: Sensor 0 MinW[1]
0x8020700E	SNR0_AEC_STAT_DS_RATE	0x04	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 statistic sample rate
0x8020700F	SNR0_AEC_POS_W_SHIFT	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 position weight shift
0x80207010	SNR0_AEC_LOW_LIGHT_THRE	0x00	RW	Bit[7:0]: Sensor 0 low light threshold
0x80207011	SNR0_AEC_HIGH_LIGHT_THRE	0xF0	RW	Bit[7:0]: Sensor 0 high light threshold
0x80207012	SNR0_AEC_WIN_LEFT_0_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 win left[0] high byte
0x80207013	SNR0_AEC_WIN_LEFT_0_L	0x78	RW	Bit[7:0]: Sensor 0 win left[0] low byte
0x80207014	SNR0_AEC_WIN_TOP_0_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 win top[0] high byte
0x80207015	SNR0_AEC_WIN_TOP_0_L	0x04	RW	Bit[7:0]: Sensor 0 win top[0] low byte
0x80207016	SNR0_AEC_STAT_WIN_WIDTH_0_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 statistic window width[0] high byte
0x80207017	SNR0_AEC_STAT_WIN_WIDTH_0_L	0x78	RW	Bit[7:0]: Sensor 0 statistic window width[0] low byte
0x80207018	SNR0_AEC_STAT_WIN_HEIGHT_0_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 statistic window height[0] high byte
0x80207019	SNR0_AEC_STAT_WIN_HEIGHT_0_L	0x04	RW	Bit[7:0]: Sensor 0 statistic window height[0] low byte
0x8020701A	SNR0_AEC_WIN_LEFT_1_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 window left[1] high byte
0x8020701B	SNR0_AEC_WIN_LEFT_1_L	0x78	RW	Bit[7:0]: Sensor 0 window left[1] low byte
0x8020701C	SNR0_AEC_WIN_TOP_1_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 window top[1] high byte
0x8020701D	SNR0_AEC_WIN_TOP_1_L	0x04	RW	Bit[7:0]: Sensor 0 window top[1] low byte

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table 3-33 AEC window and weight control registers (sheet 3 of 12)

address	register name	default value	R/W	description
0x8020701E	SNR0_AEC_STAT_WIN_WIDTH_1_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 statistic window width[1] high byte
0x8020701F	SNR0_AEC_STAT_WIN_WIDTH_1_L	0x78	RW	Bit[7:0]: Sensor 0 statistic window width[1] low byte
0x80207020	SNR0_AEC_STAT_WIN_HEIGHT_1_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 statistic window height[1] high byte
0x80207021	SNR0_AEC_STAT_WIN_HEIGHT_1_L	0x04	RW	Bit[7:0]: Sensor 0 statistic window height[1] low byte
0x80207022	SNR0_AEC_WEIGHTS_0	0x11	RW	Bit[7:4]: Sensor 0 weights[0][0] Bit[3:0]: Sensor 0 weights[1][0]
0x80207023	SNR0_AEC_WEIGHTS_1	0x11	RW	Bit[7:4]: Sensor 0 weights[0][1] Bit[3:0]: Sensor 0 weights[1][1]
0x80207024	SNR0_AEC_WEIGHTS_2	0x11	RW	Bit[7:4]: Sensor 0 weights[0][2] Bit[3:0]: Sensor 0 weights[1][2]
0x80207025	SNR0_AEC_WEIGHTS_3	0x11	RW	Bit[7:4]: Sensor 0 weights[0][3] Bit[3:0]: Sensor 0 weights[1][3]
0x80207026	SNR0_AEC_WEIGHTS_4	0x11	RW	Bit[7:4]: Sensor 0 weights[0][4] Bit[3:0]: Sensor 0 weights[1][4]
0x80207027	SNR0_AEC_WEIGHTS_5	0x11	RW	Bit[7:4]: Sensor 0 weights[0][5] Bit[3:0]: Sensor 0 weights[1][5]
0x80207028	SNR0_AEC_WEIGHTS_6	0x11	RW	Bit[7:4]: Sensor 0 weights[0][6] Bit[3:0]: Sensor 0 weights[1][6]
0x80207029	SNR0_AEC_WEIGHTS_7	0x11	RW	Bit[7:4]: Sensor 0 weights[0][7] Bit[3:0]: Sensor 0 weights[1][7]
0x8020702A	SNR0_AEC_WEIGHTS_8	0x11	RW	Bit[7:4]: Sensor 0 weights[0][8] Bit[3:0]: Sensor 0 weights[1][8]
0x8020702B	SNR0_AEC_WEIGHTS_9	0x11	RW	Bit[7:4]: Sensor 0 weights[0][9] Bit[3:0]: Sensor 0 weights[1][9]
0x8020702C	SNR0_AEC_WEIGHTS_10	0x11	RW	Bit[7:4]: Sensor 0 weights[0][10] Bit[3:0]: Sensor 0 weights[1][10]
0x8020702D	SNR0_AEC_WEIGHTS_11	0x11	RW	Bit[7:4]: Sensor 0 weights[0][11] Bit[3:0]: Sensor 0 weights[1][11]
0x8020702E	SNR0_AEC_WEIGHTS_12	0x11	RW	Bit[7:4]: Sensor 0 weights[0][12] Bit[3:0]: Sensor 0 weights[1][12]
0x8020702F	SNR0_AEC_ROI_LEFT_0_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 ROI left[0] high byte

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table 3-33 AEC window and weight control registers (sheet 4 of 12)

address	register name	default value	R/W	description
0x80207030	SNR0_AEC_ROI_LEFT _0_L	0x00	RW	Bit[7:0]: Sensor 0 ROI left[0] low byte
0x80207031	SNR0_AEC_ROI_TOP _0_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 ROI top[0] high byte
0x80207032	SNR0_AEC_ROI_TOP _0_L	0x00	RW	Bit[7:0]: Sensor 0 ROI top[0] low byte
0x80207033	SNR0_AEC_ROI_RIGHT _0_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 ROI right[0] high byte
0x80207034	SNR0_AEC_ROI_RIGHT _0_L	0x00	RW	Bit[7:0]: Sensor 0 ROI right[0] low byte
0x80207035	SNR0_AEC_ROI_ BOTTOM_0_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 ROI bottom[0] high byte
0x80207036	SNR0_AEC_ROI_ BOTTOM_0_L	0x00	RW	Bit[7:0]: Sensor 0 ROI bottom[0] low byte
0x80207037	SNR0_AEC_ROI_ WEIGHTS_0	0x11	RW	Bit[7:4]: Sensor 0 ROI weights[0][0] Bit[3:0]: Sensor 0 ROI weights[0][1]
0x80207038	SNR0_AEC_ROI_LEFT _1_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 ROI left[1] high byte
0x80207039	SNR0_AEC_ROI_LEFT _1_L	0x00	RW	Bit[7:0]: Sensor 0 ROI left[1] low byte
0x8020703A	SNR0_AEC_ROI_TOP _1_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 ROI top[1] high byte
0x8020703B	SNR0_AEC_ROI_TOP _1_L	0x00	RW	Bit[7:0]: Sensor 0 ROI top[1] low byte
0x8020703C	SNR0_AEC_ROI_RIGHT _1_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 ROI right[1] high byte
0x8020703D	SNR0_AEC_ROI_RIGHT _1_L	0x00	RW	Bit[7:0]: Sensor 0 ROI right[1] low byte
0x8020703E	SNR0_AEC_ROI_ BOTTOM_1_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 ROI bottom[1] high byte
0x8020703F	SNR0_AEC_ROI_ BOTTOM_1_L	0x00	RW	Bit[7:0]: Sensor 0 ROI bottom[1] low byte
0x80207040	SNR0_AEC_ROI_ WEIGHTS_1	0x11	RW	Bit[7:4]: Sensor 0 ROI weights[1][0] Bit[3:0]: Sensor 0 ROI weights[1][1]

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table 3-33 AEC window and weight control registers (sheet 5 of 12)

address	register name	default value	R/W	description
0x80207041	SNR0_AEC_ROI_SHIFT	0x00	RW	Bit[7:4]: Reserved Bit[3:2]: Sensor 0 ROI shift[0] Bit[1:0]: Sensor 0 ROI shift[1]
0x80207042	SNR0_AEC_BLACK_ THRE1_0_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 black threshold1[0] high byte
0x80207043	SNR0_AEC_BLACK_ THRE1_0_B1	0x04	RW	Bit[7:0]: Sensor 0 black threshold1[0] middle byte
0x80207044	SNR0_AEC_BLACK_ THRE1_0_B0	0x00	RW	Bit[7:0]: Sensor 0 black threshold1[0] low byte
0x80207045	SNR0_AEC_BLACK_ THRE2_0_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 black threshold2[0] high byte
0x80207046	SNR0_AEC_BLACK_ THRE2_0_B1	0x20	RW	Bit[7:0]: Sensor 0 black threshold2[0] middle byte
0x80207047	SNR0_AEC_BLACK_ THRE2_0_B0	0x00	RW	Bit[7:0]: Sensor 0 black threshold2[0] low byte
0x80207048	SNR0_AEC_BLACK_ WEIGHT1_0	0x10	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 black weight1[0]
0x80207049	SNR0_AEC_BLACK_ WEIGHT2_0	0x14	RW	Bit[7:6]: Reserved Bit[6:0]: Sensor 0 black weight2[0]
0x8020704A	SNR0_AEC_SATURATE_ THRE1_0_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 saturate threshold1[0] high byte
0x8020704B	SNR0_AEC_SATURATE_ THRE1_0_B1	0x08	RW	Bit[7:0]: Sensor 0 saturate threshold1[0] middle byte
0x8020704C	SNR0_AEC_SATURATE_ THRE1_0_B0	0x00	RW	Bit[7:0]: Sensor 0 saturate threshold1[0] low byte
0x8020704D	SNR0_AEC_SATURATE_ THRE2_0_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 saturate threshold2[0] high byte
0x8020704E	SNR0_AEC_SATURATE_ THRE2_0_B1	0x10	RW	Bit[7:0]: Sensor 0 saturate threshold2[0] middle byte
0x8020704F	SNR0_AEC_SATURATE_ THRE2_0_B0	0x00	RW	Bit[7:0]: Sensor 0 saturate threshold2[0] low byte
0x80207050	SNR0_AEC_SATURATE_ WEIGHT1_0	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 saturate weight1[0]
0x80207051	SNR0_AEC_SATURATE_ WEIGHT2_0	0x12	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 saturate weight2[0]

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table 3-33 AEC window and weight control registers (sheet 6 of 12)

address	register name	default value	R/W	description
0x80207052	SNR0_AEC_BLACK_THRE1_1_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 black threshold1[1] high byte
0x80207053	SNR0_AEC_BLACK_THRE1_1_B1	0x10	RW	Bit[7:0]: Sensor 0 black threshold1[1] middle byte
0x80207054	SNR0_AEC_BLACK_THRE1_1_B0	0x00	RW	Bit[7:0]: Sensor 0 black threshold1[1] low byte
0x80207055	SNR0_AEC_BLACK_THRE2_1_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 black threshold2[1] high byte
0x80207056	SNR0_AEC_BLACK_THRE2_1_B1	0x40	RW	Bit[7:0]: Sensor 0 black threshold2[1] middle byte
0x80207057	SNR0_AEC_BLACK_THRE2_1_B0	0x00	RW	Bit[7:0]: Sensor 0 black threshold2[1] low byte
0x80207058	SNR0_AEC_BLACK_WEIGHT1_1	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 black weight1[1]
0x80207059	SNR0_AEC_BLACK_WEIGHT2_1	0x12	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 black weight2[1]
0x8020705A	SNR0_AEC_SATURATE_THRE1_1_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 saturate threshold1[1] high byte
0x8020705B	SNR0_AEC_SATURATE_THRE1_1_B1	0x04	RW	Bit[7:0]: Sensor 0 saturate threshold1[1] middle byte
0x8020705C	SNR0_AEC_SATURATE_THRE1_1_B0	0x00	RW	Bit[7:0]: Sensor 0 saturate threshold1[1] low byte
0x8020705D	SNR0_AEC_SATURATE_THRE2_1_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 saturate threshold2[1] high byte
0x8020705E	SNR0_AEC_SATURATE_THRE2_1_B1	0x20	RW	Bit[7:0]: Sensor 0 saturate threshold2[1] middle byte
0x8020705F	SNR0_AEC_SATURATE_THRE2_1_B0	0x00	RW	Bit[7:0]: Sensor 0 saturate threshold2[1] low byte
0x80207060	SNR0_AEC_SATURATE_WEIGHT1_1	0x10	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 saturate weight1[1]
0x80207061	SNR0_AEC_SATURATE_WEIGHT2_1	0x14	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 saturate weight2[1]
0x80207062	SNR0_AEC_MEAN_Y_0_B1	–	R	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 mean Y[0] high byte

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table 3-33 AEC window and weight control registers (sheet 7 of 12)

address	register name	default value	R/W	description
0x80207063	SNR0_AEC_MEAN_Y_0_B0	–	R	Bit[7:0]: Sensor 0 mean Y[0] low byte
0x80207064	SNR0_AEC_MEAN_Y_1_B1	–	R	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 mean Y[1] high byte
0x80207065	SNR0_AEC_MEAN_Y_1_B0	–	R	Bit[7:0]: Sensor 0 mean Y[1] low byte
0x80207066	SNR0_AEC_CNV_GAIN_RATIO	0x00	RW	Bit[7:0]: Sensor 0 conversion gain ratio (firmware use only)
0x80207070	SNR1_AEC_AGC_STAT_TYPE	1'b0	RW	Bit[0]: Sensor 1 AECAGC statistic type 0: Mean value of R, G, B 1: Max value of R, G, B
0x80207071	SNR1_AEC_STAT_WIN_LEFT_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 statistic window left offset[11:8]
0x80207072	SNR1_AEC_STAT_WIN_LEFT_L	0x00	RW	Bit[7:0]: Sensor 1 statistic window left offset[7:0]
0x80207073	SNR1_AEC_STAT_WIN_RIGHT_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 statistic window right offset[11:8]
0x80207074	SNR1_AEC_STAT_WIN_RIGHT_L	0x00	RW	Bit[7:0]: Sensor 1 statistic window right offset[7:0]
0x80207075	SNR1_AEC_STAT_WIN_TOP_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 statistic window top offset[10:8]
0x80207076	SNR1_AEC_STAT_WIN_TOP_L	0x00	RW	Bit[7:0]: Sensor 1 statistic window top offset[7:0]
0x80207077	SNR1_AEC_STAT_WIN_BOTTOM_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 statistic window bottom offset[10:8]
0x80207078	SNR1_AEC_STAT_WIN_BOTTOM_L	0x14	RW	Bit[7:0]: Sensor 1 statistic window bottom offset[7:0]
0x80207079	SNR1_AEC_MAX_W_H	0x01	RW	Bit[7:2]: Reserved Bit[1]: Sensor 1 MaxW[0] high byte Bit[0]: Sensor 1 MaxW[1] high byte
0x8020707A	SNR1_AEC_MAX_W_0_L	0x20	RW	Bit[7:0]: Sensor 1 MaxW[0] low byte
0x8020707B	SNR1_AEC_MAX_W_1_L	0x00	RW	Bit[7:0]: Sensor 1 MaxW[1] low byte
0x8020707C	SNR1_AEC_MIN_W_0	0x01	RW	Bit[7:0]: Sensor 1 MinW[0]

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table 3-33 AEC window and weight control registers (sheet 8 of 12)

address	register name	default value	R/W	description
0x8020707D	SNR1_AEC_MIN_W_1	0x01	RW	Bit[7:0]: Sensor 1 MinW[1]
0x8020707E	SNR1_AEC_STAT_DS_RATE	0x04	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 statistic sample rate
0x8020707F	SNR1_AEC_POS_W_SHIFT	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 position weight shift
0x80207080	SNR1_AEC_LOW_LIGHT_THRE	0x00	RW	Bit[7:0]: Sensor 1 low light threshold
0x80207081	SNR1_AEC_HIGH_LIGHT_THRE	0xF0	RW	Bit[7:0]: Sensor 1 high light threshold
0x80207082	SNR1_AEC_WIN_LEFT_0_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 win left[0] high byte
0x80207083	SNR1_AEC_WIN_LEFT_0_L	0x78	RW	Bit[7:0]: Sensor 1 win left[0] low byte
0x80207084	SNR1_AEC_WIN_TOP_0_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 win top[0] high byte
0x80207085	SNR1_AEC_WIN_TOP_0_L	0x04	RW	Bit[7:0]: Sensor 1 win top[0] low byte
0x80207086	SNR1_AEC_STAT_WIN_WIDTH_0_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 statistic window width[0] high byte
0x80207087	SNR1_AEC_STAT_WIN_WIDTH_0_L	0x78	RW	Bit[7:0]: Sensor 1 statistic window width[0] low byte
0x80207088	SNR1_AEC_STAT_WIN_HEIGHT_0_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 statistic window height[0] high byte
0x80207089	SNR1_AEC_STAT_WIN_HEIGHT_0_L	0x04	RW	Bit[7:0]: Sensor 1 statistic window height[0] low byte
0x8020708A	SNR1_AEC_WIN_LEFT_1_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 window left[1] high byte
0x8020708B	SNR1_AEC_WIN_LEFT_1_L	0x78	RW	Bit[7:0]: Sensor 1 window left[1] low byte
0x8020708C	SNR1_AEC_WIN_TOP_1_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 window top[1] high byte
0x8020708D	SNR1_AEC_WIN_TOP_1_L	0x04	RW	Bit[7:0]: Sensor 1 window top[1] low byte

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table 3-33 AEC window and weight control registers (sheet 9 of 12)

address	register name	default value	R/W	description
0x8020708E	SNR1_AEC_STAT_WIN_WIDTH_1_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 statistic window width[1] high byte
0x8020708F	SNR1_AEC_STAT_WIN_WIDTH_1_L	0x78	RW	Bit[7:0]: Sensor 1 statistic window width[1] low byte
0x80207090	SNR1_AEC_STAT_WIN_HEIGHT_1_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 statistic window height[1] high byte
0x80207091	SNR1_AEC_STAT_WIN_HEIGHT_1_L	0x04	RW	Bit[7:0]: Sensor 1 statistic window height[1] low byte
0x80207092	SNR1_AEC_WEIGHTS_0	0x11	RW	Bit[7:4]: Sensor 1 weights[0][0] Bit[3:0]: Sensor 1 weights[1][0]
0x80207093	SNR1_AEC_WEIGHTS_1	0x11	RW	Bit[7:4]: Sensor 1 weights[0][1] Bit[3:0]: Sensor 1 weights[1][1]
0x80207094	SNR1_AEC_WEIGHTS_2	0x11	RW	Bit[7:4]: Sensor 1 weights[0][2] Bit[3:0]: Sensor 1 weights[1][2]
0x80207095	SNR1_AEC_WEIGHTS_3	0x11	RW	Bit[7:4]: Sensor 1 weights[0][3] Bit[3:0]: Sensor 1 weights[1][3]
0x80207096	SNR1_AEC_WEIGHTS_4	0x11	RW	Bit[7:4]: Sensor 1 weights[0][4] Bit[3:0]: Sensor 1 weights[1][4]
0x80207097	SNR1_AEC_WEIGHTS_5	0x11	RW	Bit[7:4]: Sensor 1 weights[0][5] Bit[3:0]: Sensor 1 weights[1][5]
0x80207098	SNR1_AEC_WEIGHTS_6	0x11	RW	Bit[7:4]: Sensor 1 weights[0][6] Bit[3:0]: Sensor 1 weights[1][6]
0x80207099	SNR1_AEC_WEIGHTS_7	0x11	RW	Bit[7:4]: Sensor 1 weights[0][7] Bit[3:0]: Sensor 1 weights[1][7]
0x8020709A	SNR1_AEC_WEIGHTS_8	0x11	RW	Bit[7:4]: Sensor 1 weights[0][8] Bit[3:0]: Sensor 1 weights[1][8]
0x8020709B	SNR1_AEC_WEIGHTS_9	0x11	RW	Bit[7:4]: Sensor 1 weights[0][9] Bit[3:0]: Sensor 1 weights[1][9]
0x8020709C	SNR1_AEC_WEIGHTS_10	0x11	RW	Bit[7:4]: Sensor 1 weights[0][10] Bit[3:0]: Sensor 1 weights[1][10]
0x8020709D	SNR1_AEC_WEIGHTS_11	0x11	RW	Bit[7:4]: Sensor 1 weights[0][11] Bit[3:0]: Sensor 1 weights[1][11]
0x8020709E	SNR1_AEC_WEIGHTS_12	0x11	RW	Bit[7:4]: Sensor 1 weights[0][12] Bit[3:0]: Sensor 1 weights[1][12]
0x8020709F	SNR1_AEC_ROI_LEFT_0_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 ROI left[0] high byte

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table 3-33 AEC window and weight control registers (sheet 10 of 12)

address	register name	default value	R/W	description
0x802070A0	SNR1_AEC_ROI_LEFT _0_L	0x00	RW	Bit[7:0]: Sensor 1 ROI left[0] low byte
0x802070A1	SNR1_AEC_ROI_TOP _0_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 ROI top[0] high byte
0x802070A2	SNR1_AEC_ROI_TOP _0_L	0x00	RW	Bit[7:0]: Sensor 1 ROI top[0] low byte
0x802070A3	SNR1_AEC_ROI_RIGHT _0_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 ROI right[0] high byte
0x802070A4	SNR1_AEC_ROI_RIGHT _0_L	0x00	RW	Bit[7:0]: Sensor 1 ROI right[0] low byte
0x802070A5	SNR1_AEC_ROI_ BOTTOM_0_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 ROI bottom[0] high byte
0x802070A6	SNR1_AEC_ROI_ BOTTOM_0_L	0x00	RW	Bit[7:0]: Sensor 1 ROI bottom[0] low byte
0x802070A7	SNR1_AEC_ROI_ WEIGHTS_0	0x11	RW	Bit[7:4]: Sensor 1 ROI weights[0][0] Bit[3:0]: Sensor 1 ROI weights[0][1]
0x802070A8	SNR1_AEC_ROI_LEFT _1_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 ROI left[1] high byte
0x802070A9	SNR1_AEC_ROI_LEFT _1_L	0x00	RW	Bit[7:0]: Sensor 1 ROI left[1] low byte
0x802070AA	SNR1_AEC_ROI_TOP _1_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 ROI top[1] high byte
0x802070AB	SNR1_AEC_ROI_TOP _1_L	0x00	RW	Bit[7:0]: Sensor 1 ROI top[1] low byte
0x802070AC	SNR1_AEC_ROI_RIGHT _1_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 ROI right[1] high byte
0x802070AD	SNR1_AEC_ROI_RIGHT _1_L	0x00	RW	Bit[7:0]: Sensor 1 ROI right[1] low byte
0x802070AE	SNR1_AEC_ROI_ BOTTOM_1_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 ROI bottom[1] high byte
0x802070AF	SNR1_AEC_ROI_ BOTTOM_1_L	0x00	RW	Bit[7:0]: Sensor 1 ROI bottom[1] low byte
0x802070B0	SNR1_AEC_ROI_ WEIGHTS_1	0x11	RW	Bit[7:4]: Sensor 1 ROI weights[1][0] Bit[3:0]: Sensor 1 ROI weights[1][1]

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table 3-33 AEC window and weight control registers (sheet 11 of 12)

address	register name	default value	R/W	description
0x802070B1	SNR1_AEC_ROI_SHIFT	0x00	RW	Bit[7:4]: Reserved Bit[3:2]: Sensor 1 ROI shift[0] Bit[1:0]: Sensor 1 ROI shift[1]
0x802070B2	SNR1_AEC_BLACK_ THRE1_0_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 black threshold1[0] high byte
0x802070B3	SNR1_AEC_BLACK_ THRE1_0_B1	0x04	RW	Bit[7:0]: Sensor 1 black threshold1[0] middle byte
0x802070B4	SNR1_AEC_BLACK_ THRE1_0_B0	0x00	RW	Bit[7:0]: Sensor 1 black threshold1[0] low byte
0x802070B5	SNR1_AEC_BLACK_ THRE2_0_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 black threshold2[0] high byte
0x802070B6	SNR1_AEC_BLACK_ THRE2_0_B1	0x20	RW	Bit[7:0]: Sensor 1 black threshold2[0] middle byte
0x802070B7	SNR1_AEC_BLACK_ THRE2_0_B0	0x00	RW	Bit[7:0]: Sensor 1 black threshold2[0] low byte
0x802070B8	SNR1_AEC_BLACK_ WEIGHT1_0	0x10	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 black weight1[0]
0x802070B9	SNR1_AEC_BLACK_ WEIGHT2_0	0x14	RW	Bit[7:6]: Reserved Bit[6:0]: Sensor 1 black weight2[0]
0x802070BA	SNR1_AEC_SATURATE_ THRE1_0_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 saturate threshold1[0] high byte
0x802070BB	SNR1_AEC_SATURATE_ THRE1_0_B1	0x08	RW	Bit[7:0]: Sensor 1 saturate threshold1[0] bottom byte
0x802070BC	SNR1_AEC_SATURATE_ THRE1_0_B0	0x00	RW	Bit[7:0]: Sensor 1 saturate threshold1[0] low byte
0x802070BD	SNR1_AEC_SATURATE_ THRE2_0_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 saturate threshold2[0] high byte
0x802070BE	SNR1_AEC_SATURATE_ THRE2_0_B1	0x10	RW	Bit[7:0]: Sensor 1 saturate threshold2[0] middle byte
0x802070BF	SNR1_AEC_SATURATE_ THRE2_0_B0	0x00	RW	Bit[7:0]: Sensor 1 saturate threshold2[0] low byte
0x802070C0	SNR1_AEC_SATURATE_ WEIGHT1_0	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 saturate weight1[0]
0x802070C1	SNR1_AEC_SATURATE_ WEIGHT2_0	0x12	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 saturate weight2[0]

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table 3-33 AEC window and weight control registers (sheet 12 of 12)

address	register name	default value	R/W	description
0x802070C2	SNR1_AEC_BLACK_THRE1_1_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 black threshold1[1] high byte
0x802070C3	SNR1_AEC_BLACK_THRE1_1_B1	0x10	RW	Bit[7:0]: Sensor 1 black threshold1[1] middle byte
0x802070C4	SNR1_AEC_BLACK_THRE1_1_B0	0x00	RW	Bit[7:0]: Sensor 1 black threshold1[1] low byte
0x802070C5	SNR1_AEC_BLACK_THRE2_1_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 black threshold2[1] high byte
0x802070C6	SNR1_AEC_BLACK_THRE2_1_B1	0x40	RW	Bit[7:0]: Sensor 1 black threshold2[1] middle byte
0x802070C7	SNR1_AEC_BLACK_THRE2_1_B0	0x00	RW	Bit[7:0]: Sensor 1 black threshold2[1] low byte
0x802070C8	SNR1_AEC_BLACK_WEIGHT1_1	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 black weight1[1]
0x802070C9	SNR1_AEC_BLACK_WEIGHT2_1	0x12	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 black weight2[1]
0x802070CA	SNR1_AEC_SATURATE_THRE1_1_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 saturate threshold1[1] high byte
0x802070CB	SNR1_AEC_SATURATE_THRE1_1_B1	0x04	RW	Bit[7:0]: Sensor 1 saturate threshold1[1] middle byte
0x802070CC	SNR1_AEC_SATURATE_THRE1_1_B0	0x00	RW	Bit[7:0]: Sensor 1 saturate threshold1[1] low byte
0x802070CD	SNR1_AEC_SATURATE_THRE2_1_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 saturate threshold2[1] high byte
0x802070CE	SNR1_AEC_SATURATE_THRE2_1_B1	0x20	RW	Bit[7:0]: Sensor 1 saturate threshold2[1] middle byte
0x802070CF	SNR1_AEC_SATURATE_THRE2_1_B0	0x00	RW	Bit[7:0]: Sensor 1 saturate threshold2[1] low byte
0x802070D0	SNR1_AEC_SATURATE_WEIGHT1_1	0x10	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 saturate weight1[1]
0x802070D1	SNR1_AEC_SATURATE_WEIGHT2_1	0x14	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 saturate weight2[1]

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3.23.4 exposure/gain control

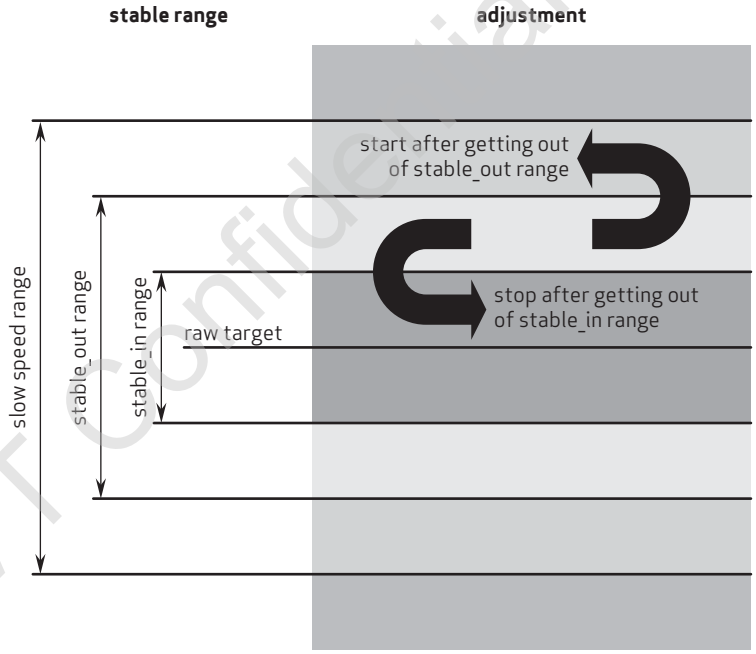
AEC target determines the target raw brightness. Basically, AEC/AGC has two states, stable and un-stable. The AEC/AGC range from unstable to stable determines the range within which the image brightness is considered to be reaching the target. AEC/AGC range from stable to unstable determines when AEC/AGC starts to adjust the exposure/gain and the image brightness is considered to be off the target.

Maximum camera gain is used for low light conditions. Some sensors use high gain to boost AEC/AGC to the desired brightness level. However, as gain goes up, noise becomes more visible. It is a compromise to decide which noise level is accepted with the acceptable level of brightness. Minimum camera gain is used for high light conditions.

Maximum exposure is mostly determined by the sensor frame rate. Minimum exposure time is useful for outdoor scenarios, where the exposure time needs to be short enough; otherwise, the image will be all saturated.

Considering the non-linearity of the weighted average, there are three regions based on the distance between current weighted average and the target: fast range, slow range and stable range. When the current weighted average changes within the stable range, the exposure will remain stable. The difference between slow range and fast range is the exposure changing speed. In slow range, the exposure is limited to changing in small steps.

figure 3-42 automatic adjustment step mode diagram



490_DS_3_42

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The AEC/AGC adjustment step is calculated by the distance between the current average value and the target. When the current weighted average is far from the stable range, a large adjustment step is applied to quickly bring the average value to stable range. Register 0x2F6 defines the percentage of the adjustment with respect to the distance to the target value. The exposure adjustment is further limited by the ratio to the exposure time of the previous frame. The maximum current-to-previous-frame exposure ratio range is limited to the range of (16/0x2FA, 0x2FA/16).

When the current weighted average is close to the stable range, a small adjustment step is applied to avoid overshoot or undershoot. Register 0x2FB defines the percentage of the adjustment with respect to the distance to the target value. The exposure adjustment is further limited by the ratio to the exposure time of the previous frame. The maximum current-to-previous-frame exposure ratio range is limited to the range of (1 - 0x2FB/16, 1 + 0x2FB/16).

Besides, down sample statistics is supported in the OV490. A down scale rate can be set by register 0x8020700E[2:0]. Statistic type is also selectable between Y channel and the maximum data of R/G/B by register 0x80207000[0] (0: Y, 1: MAX (R, G, B)).

The OV490 supports three different AEC/AGC stable range modes, AA, AB and ABC mode. Generally, the OV490 default is AA mode. It uses a command set for the AB/ABC mode switch. In AA mode, all frames have the same AEC/AGC stable range. In AB mode, the AEC/AGC stable range of even and odd frames can be set to different values. ABC mode is the same as AB except that the frames split into three subsets and there are three different AEC/AGC targets. The exposure and gain of A, B and C frames are adjusted separately when register 0x2E2 is set to 0. They can settle down to a slightly different value even with the same stable range. When register 0x2E2 is set to 1, the exposure/gain of frames B and C is proportional to the exposure/gain of frame A. The exposure ratio between frame B and frame A is set by register 0x2FE and the exposure ratio between frames C and A is set by firmware register 0x2FF. For these three modes, the OV490 supports auto and manual exposure/gain control.

table 3-34 exposure time and gain (sheet 1 of 2)

parameter	frame A	frame B	frame C
Raw target for long channel	0x2EC	0x2ED	0x2EE
Raw target for short channel	0x2EF	0x2F0	0x2F1
YUV target in log domain	{0x24C,0x24D}	{0x24E, 0x24F}	{0x250, 0x251}
stable_in range	(Raw target - register 0x2F4, Raw target + register 0x2F4)		
stable_out range	(Raw target - register 0x2F5, Raw target + register 0x2F5)		
slow speed range for long channel	(Raw target for long channel - register 0x2F2, Raw target for long channel + register 0x2F2)		
slow speed range for short channel	(Raw target for short channel - register 0x2F3, Raw target for short channel + register 0x2F3)		
fast adjustment step for long channel	(register 0x2F6/16)×(current_level - target_level)		
fast adjustment step for short channel	(register 0x2F7/16)×(current_level - target_level)		
slow adjustment step for long channel	(register 0x2F8/16)*(current_level - target_level)		
slow adjustment step for short channel	(register 0x2F9/16)*(current_level - target_level)		

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table 3-34 exposure time and gain (sheet 2 of 2)

parameter	frame A	frame B	frame C
max fast current-to-previous-frame exposure ratio range	(16/register 0x2FA, register 0x2FA/16)		
max slow current-to-previous frame exposure ratio range	(1-register 0x2FB/16, 1+register 0x2FB/16)		

In the OV490, exposure time and gain changes every two frames. At the end of the first frame, the new exposure time and gain will be estimated and the exposure time registers will be updated afterward. The gain registers will be updated at the end of the second frame. So, the third frame will be the result of new exposure and gain. The same algorithm is employed to adjust the exposure and gain for frames A, B and C in AB or ABC mode. The control register sets are separated for frames A, B and C.

The user can also specify the target brightness of the final image output. The brightness target, however, does not affect AEC/AGC. The OV490 adjusts the gamma curve and HDR gain to achieve the brightness target, but it is not guaranteed to reach the target value. Tone mapping will change the image brightness afterwards.

In extremely dark situations, night mode is activated (0x2E3), allowing the sensor to extend the frame period and thus, the exposure time. The frame period can be extended a maximum of 3 times the original frame period (0x327). So for L channel, maximum exposure time can be up to 4 times the original frame period. For S and VS channels, there are other controls which limit the maximum exposure time. Registers 0x350 ~ 0x361 show the maximum gain multiplied by the maximum exposure for each channel.

To avoid image banding under a flickering light source, the exposure time can be adjusted in steps of integer multiples of the light flickering period, enabled by registers 0x2E5, 0x2E6 and 0x2E7 for L, S and VS channels. The light source flicker frequency (50/60 Hz) is selected by register 0x2EB.

3.23.5 manual exposure/gain control

The manual AEC/AGC control register is firmware register 0xAD8=1.

A backend processor can fully control the exposure/gain for both long and short exposure using the following sequence.

For AA mode:

1. Disable auto exposure 0xAD8=1
2. Choose manual AEC AA mode 0x00 = 0
3. Set exposure/gain using 0x32C~0x34F

Manual mode for AB and ABC mode is enabled by register 0x00. The manual exposure time for L, S and VS channels for frames A, B and C is set by registers 0x32C ~ 0x33D. Gain is set by registers 0x33E ~ 0x34F.

The OV490 uses cmdset to utilize the manual exposure/gain control for AA/AB/ABC mode. Please refer to the *OV490 Application Note* or contact your local OmniVision FAE for details.

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table 3-35 AEC control firmware registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x00	TARGETNUM	0x01	RW	Bit[7:2]: Reserved Bit[1:0]: ABC target number
0x2FE	GPMODERATIO_0	0x20	RW	B/A Ratio in GP Mode
0x2FF	GPMODERATIO_1	0x08	RW	C/A Ratio in GP Mode
0x300	EXPRATIOSTEP	0x20	RW	L/S Ratio Change Step
0x301	NONHDRSTEP	0x08	RW	L/S Change Step in Non-HDR Mode
0x304	MAXCAMERAGAIN_0_H	0x02	RW	Bit[1:0]: Max gain for long[9:8]
0x305	MAXCAMERAGAIN_0_L	0x00	RW	Bit[7:0]: Max gain for long[7:0]
0x306	MAXCAMERAGAIN_1_H	0x02	RW	Bit[1:0]: Max gain for short[9:8]
0x307	MAXCAMERAGAIN_1_L	0x00	RW	Bit[7:0]: Max gain for short[7:0]
0x308	MAXCAMERAGAIN_2_H	0x02	RW	Bit[1:0]: Max gain for VS[9:8]
0x309	MAXCAMERAGAIN_2_L	0x00	RW	Bit[7:0]: Max gain for VS[7:0]
0x30A	MINCAMERAGAIN_0_H	0x00	RW	Bit[1:0]: Min gain for long[9:8]
0x30B	MINCAMERAGAIN_0_L	0x20	RW	Bit[7:0]: Min gain for long[7:0]
0x30C	MINCAMERAGAIN_1_H	0x00	RW	Bit[1:0]: Min gain for short[9:8]
0x30D	MINCAMERAGAIN_1_L	0x20	RW	Bit[7:0]: Min gain for short[7:0]
0x30E	MINCAMERAGAIN_2_H	0x00	RW	Bit[1:0]: Min gain for VS[9:8]
0x30F	MINCAMERAGAIN_2_L	0x20	RW	Bit[7:0]: Min gain for VS[7:0]
0x310	MAXEXPOSURE_0_H	0x02	RW	Bit[7:0]: Max exposure for long[15:8]
0x311	MAXEXPOSURE_0_L	0x08	RW	Bit[7:0]: Max exposure for long[7:0]
0x312	MAXEXPOSURE_1_H	0x02	RW	Bit[7:0]: Max exposure for short[15:8]
0x313	MAXEXPOSURE_1_L	0x08	RW	Bit[7:0]: Max exposure for short[7:0]
0x314	MAXEXPOSURE_2_H	0x00	RW	Bit[7:0]: Max exposure for VS[15:8]
0x315	MAXEXPOSURE_2_L	0x78	RW	Bit[7:0]: Max exposure for VS[7:0]
0x316	MINEXPOSURE_0_H	0x00	RW	Bit[7:0]: Min exposure for long[15:8]
0x317	MINEXPOSURE_0_L	0x01	RW	Bit[7:0]: Min exposure for long[7:0]
0x318	MINEXPOSURE_1_H	0x00	RW	Bit[7:0]: Min exposure for short[15:8]
0x319	MINEXPOSURE_1_L	0x01	RW	Bit[7:0]: Min exposure for short[7:0]
0x31A	MINEXPOSURE_2_H	0x00	RW	Bit[7:0]: Min exposure for VS[15:8]
0x31B	MINEXPOSURE_2_L	0x01	RW	Bit[7:0]: Min exposure for VS[7:0]

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table 3-35 AEC control firmware registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x31C	LSSENSITIVITYRATIO_H	0x08	RW	Bit[7:0]: L/S sensitivity ratio[15:8]
0x31D	LSSENSITIVITYRATIO_L	0x00	RW	Bit[7:0]: L/S sensitivity ratio[7:0]
0x31E	SVSFIXEDRATIO_H	0x00	RW	Bit[7:0]: S/VS exposure ratio[15:8]
0x31F	SVSFIXEDRATIO_L	0x80	RW	Bit[7:0]: S/VS exposure ratio[7:0]
0x320	BANDVALUE60HZ_H	0x20	RW	Bit[7:0]: Band filter value for 60Hz[15:8]
0x321	BANDVALUE60HZ_L	0xD0	RW	Bit[7:0]: Band filter value for 60Hz[7:0]
0x322	BANDVALUE50HZ_H	0x27	RW	Bit[7:0]: Band filter value for 50Hz[15:8]
0x323	BANDVALUE50HZ_L	0x60	RW	Bit[7:0]: Band filter value for 50Hz[7:0]
0x324	MAXRATIO_H	0x00	RW	Bit[7:0]: Max L/S ratio[15:8]
0x325	MAXRATIO_L	0x20	RW	Bit[7:0]: Max L/S ratio[7:0]
0x326	MINRATIO	0x02	RW	Minimum L/S Ratio
0x327	MAXINSERTFRAME	0x03	RW	Maximum Insert Frames in Night Mode
0x328	VTSWRITEMODE	0x01	RW	VTS Write Mode 0: Write with exposure 1: Write with gain
0x350	MAXTOTALEXP_L_BYTE0	0x00	RW	Bit[7:0]: Max total exposure for long[31:24]
0x351	MAXTOTALEXP_L_BYTE1	0x0A	RW	Bit[7:0]: Max total exposure for long[23:16]
0x352	MAXTOTALEXP_L_BYTE2	0x28	RW	Bit[7:0]: Max total exposure for long[15:8]
0x353	MAXTOTALEXP_L_BYTE3	0x00	RW	Bit[7:0]: Max total exposure for long[7:0]
0x354	MAXTOTALEXP_S_BYTE0	0x00	RW	Bit[7:0]: Max total exposure for short[31:24]
0x355	MAXTOTALEXP_S_BYTE1	0x04	RW	Bit[7:0]: Max total exposure for short[23:16]
0x356	MAXTOTALEXP_S_BYTE2	0x10	RW	Bit[7:0]: Max total exposure for short[15:8]
0x357	MAXTOTALEXP_S_BYTE3	0x00	RW	Bit[7:0]: Max total exposure for short[7:0]
0x358	MAXTOTALEXP_VS_BYTE0	0x00	RW	Bit[7:0]: Max total exposure for VS[31:24]
0x359	MAXTOTALEXP_VS_BYTE1	0x02	RW	Bit[7:0]: Max total exposure for VS[23:16]
0x35A	MAXTOTALEXP_VS_BYTE2	0x60	RW	Bit[7:0]: Max total exposure for VS[15:8]
0x35B	MAXTOTALEXP_VS_BYTE3	0x00	RW	Bit[7:0]: Max total exposure for VS[7:0]
0x35C	MINTOTALEXP_L_H	0x00	RW	Bit[7:0]: Min total exposure for long[15:8]

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table 3-35 AEC control firmware registers (sheet 3 of 3)

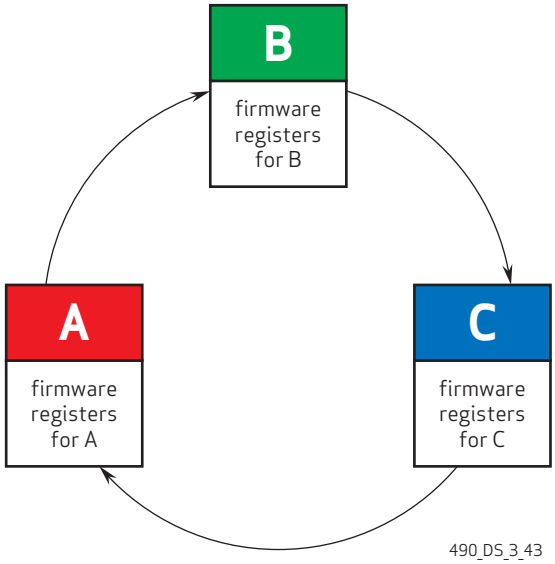
address	register name	default value	R/W	description
0x35D	MINTOTALEXP_L_L	0x20	RW	Bit[7:0]: Min total exposure for long[7:0]
0x35E	MINTOTALEXP_S_H	0x00	RW	Bit[7:0]: Min total exposure for short[15:8]
0x35F	MINTOTALEXP_S_L	0x20	RW	Bit[7:0]: Min total exposure for short[7:0]
0x360	MINTOTALEXP_VS_H	0x00	RW	Bit[7:0]: Min total exposure for VS[15:8]
0x361	MINTOTALEXP_VS_L	0x20	RW	Bit[7:0]: Min total exposure for VS[7:0]
0xAD8	MANUALAECENABLE	0x00	RW	Manual AEC Enable 0: Disable 1: Enable

3.23.6 ABC context switch

AB/ABC context switch is used in more and more applications. In AB mode for example, A frame and B frame are configured with different exposure/gain. A frame is used for lane detection and B frame is used for high beam assistant or traffic light detection.

The OV490 firmware supports AA..., ABAB..., ABCABC... mode. In AB or ABC mode, the AEC/AGC target range, manual exposure, and gain can be automatically switched among frames A, B and C. Some firmware registers set up the specific context for frames A, B and C.

figure 3-43 ABC mode diagram



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The context of frames A, B and C are stored in corresponding firmware registers. Regarding at the specific AB context switch host command, please refer to the *OV490 Application Note* document.

table 3-36 context switch control firmware registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x24C	LOGTARGETY_A_H	0x97	RW	Bit[7:0]: Image mean value target for frame A in ABC mode[15:8]
0x24D	LOGTARGETY_A_L	0x00	RW	Bit[7:0]: Image mean value target for frame A in ABC mode[7:0]
0x24E	LOGTARGETY_B_H	0x97	RW	Bit[7:0]: Image mean value target for frame B in ABC mode[15:8]
0x24F	LOGTARGETY_B_L	0x00	RW	Bit[7:0]: Image mean value target for frame B in ABC mode[7:0]
0x250	LOGTARGETY_C_H	0x97	RW	Bit[7:0]: Image mean value target for frame C in ABC mode[15:8]
0x251	LOGTARGETY_C_L	0x00	RW	Bit[7:0]: Image mean value target for frame C in ABC mode[7:0]
0x2EC	TARGETY_L_A	0x40	RW	Bit[7:0]: Target of raw data for long channel for frame A in ABC mode
0x2ED	TARGETY_L_B	0x40	RW	Bit[7:0]: Target of raw data for long channel for frame B in ABC mode
0x2EE	TARGETY_L_C	0x40	RW	Bit[7:0]: Target of raw data for long channel for frame C in ABC mode
0x2EF	TARGETY_S_A	0x80	RW	Bit[7:0]: Target of raw data for short channel for frame A in ABC mode
0x2F0	TARGETY_S_B	0x80	RW	Bit[7:0]: Target of raw data for short channel for frame B in ABC mode
0x2F1	TARGETY_S_C	0x80	RW	Bit[7:0]: Target of raw data for short channel for frame C in ABC mode
0x329	AECMANUALMODE	0x07	RW	Bit[2]: Frame C manual exposure/gain enable 0: Disable 1: Enable Bit[1]: Frame B manual exposure/gain enable 0: Disable 1: Enable Bit[0]: Frame A manual exposure/gain enable 0: Disable 1: Enable

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table 3-36 context switch control firmware registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x32A	AECMANUALDONE	0x02	RW	Manual AEC Start Mode 00: Inactive 01: Active 10: Always active 11: Not allowed
0x32C	AECMANUALEXP_L_A_H	0x00	RW	Bit[7:0]: Manual exposure for long[15:8] for frame A in ABC mode
0x32D	AECMANUALEXP_L_A_L	0x40	RW	Bit[7:0]: Manual exposure for long[7:0] for frame A in ABC mode
0x32E	AECMANUALEXP_L_B_H	0x00	RW	Bit[7:0]: Manual exposure for long[15:8] for frame B in ABC mode
0x32F	AECMANUALEXP_L_B_L	0x40	RW	Bit[7:0]: Manual exposure for long[7:0] for frame B in ABC mode
0x330	AECMANUALEXP_L_C_H	0x00	RW	Bit[7:0]: Manual exposure for long[15:8] for frame C in ABC mode
0x331	AECMANUALEXP_L_C_L	0x40	RW	Bit[7:0]: Manual exposure for long[7:0] for frame C in ABC mode
0x332	AECMANUALEXP_S_A_H	0x00	RW	Bit[7:0]: Manual exposure for short[15:8] for frame A in ABC mode
0x333	AECMANUALEXP_S_A_L	0x10	RW	Bit[7:0]: Manual exposure for short[7:0] for frame A in ABC mode
0x334	ECMANUALEXP_S_B_H	0x00	RW	Bit[7:0]: Manual exposure for short[15:8] for frame B in ABC mode
0x335	AECMANUALEXP_S_B_L	0x10	RW	Bit[7:0]: Manual exposure for short[7:0] for frame B in ABC mode
0x336	AECMANUALEXP_S_C_H	0x00	RW	Bit[7:0]: Manual exposure for short[15:8] for frame C in ABC mode
0x337	AECMANUALEXP_S_C_L	0x10	RW	Bit[7:0]: Manual exposure for short[7:0] for frame C in ABC mode
0x338	AECMANUALEXP_VS_A_H	0x00	RW	Bit[7:0]: Manual exposure for VS[15:8] for frame A in ABC mode
0x339	AECMANUALEXP_VS_A_L	0x20	RW	Bit[7:0]: Manual exposure for VS[7:0] for frame A in ABC mode
0x33A	AECMANUALEXP_VS_B_H	0x00	RW	Bit[7:0]: Manual exposure for VS[15:8] for frame B in ABC mode
0x33B	AECMANUALEXP_VS_B_L	0x20	RW	Bit[7:0]: Manual exposure for VS[7:0] for frame B in ABC mode
0x33C	AECMANUALEXP_VS_C_H	0x00	RW	Bit[7:0]: Manual exposure for VS[15:8] for frame C in ABC mode
0x33D	AECMANUALEXP_VS_C_L	0x20	RW	Bit[7:0]: Manual exposure for VS[7:0] for frame C in ABC mode

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table 3-36 context switch control firmware registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x33E	AECMANUALGAIN_L_A_H	0x00	RW	Bit[7:0]: Manual gain for long[15:8] for frame A in ABC mode
0x33F	AECMANUALGAIN_L_A_L	0x20	RW	Bit[7:0]: Manual gain for long[7:0] for frame A in ABC mode
0x340	AECMANUALGAIN_L_B_H	0x00	RW	Bit[7:0]: Manual gain for long[15:8] for frame B in ABC mode
0x341	AECMANUALGAIN_L_B_L	0x20	RW	Bit[7:0]: Manual gain for long[7:0] for frame B in ABC mode
0x342	AECMANUALGAIN_L_C_H	0x00	RW	Bit[7:0]: Manual gain for long[15:8] for frame C in ABC mode
0x343	AECMANUALGAIN_L_C_L	0x20	RW	Bit[7:0]: Manual gain for long[7:0] for frame C in ABC mode
0x344	AECMANUALGAIN_S_A_H	0x00	RW	Bit[7:0]: Manual gain for short[15:8] for frame A in ABC mode
0x345	AECMANUALGAIN_S_A_L	0x20	RW	Bit[7:0]: Manual gain for short[7:0] for frame A in ABC mode
0x346	AECMANUALGAIN_S_B_H	0x00	RW	Bit[7:0]: Manual gain for short[15:8] for frame B in ABC mode
0x347	AECMANUALGAIN_S_B_L	0x20	RW	Bit[7:0]: Manual gain for short[7:0] for frame B in ABC mode
0x348	AECMANUALGAIN_S_C_H	0x00	RW	Bit[7:0]: Manual gain for short[15:8] for frame C in ABC mode
0x349	AECMANUALGAIN_S_C_L	0x20	RW	Bit[7:0]: Manual gain for short[7:0] for frame C in ABC mode
0x34A	AECMANUALGAIN_VS_A_H	0x00	RW	Bit[7:0]: Manual gain for VS[15:8] for frame A in ABC mode
0x34B	AECMANUALGAIN_VS_A_L	0x20	RW	Bit[7:0]: Manual gain for VS[7:0] for frame A in ABC mode
0x34C	AECMANUALGAIN_VS_B_H	0x00	RW	Bit[7:0]: Manual gain for VS[15:8] for frame B in ABC mode
0x34D	AECMANUALGAIN_VS_B_L	0x20	RW	Bit[7:0]: Manual gain for VS[7:0] for frame B in ABC mode
0x34E	AECMANUALGAIN_VS_C_H	0x00	RW	Bit[7:0]: Manual gain for VS[15:8] for frame C in ABC mode
0x34F	AECMANUALGAIN_VS_C_L	0x20	RW	Bit[7:0]: Manual gain for VS[7:0] for frame C in ABC mode
0xAD8	MANUALAECENABLE	0x00	RW	Manual AEC Enable 0: Disable 1: Enable

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3.24 high temperature control

When the surrounding temperature increases above 100°C, the sensor's temperature increases. An increase in temperature causes the image to display more noise, color in the image will not be well-distributed and there may be some color shift. The OV490 uses high temperature (HT) control to maintain good image performance.

The HT control focuses on noise reduction and color balance. For noise reduction, the OV490 uses HDR gain control, LENC control and gamma gain. For color balance, the OV490 uses color saturation control and BLC target.

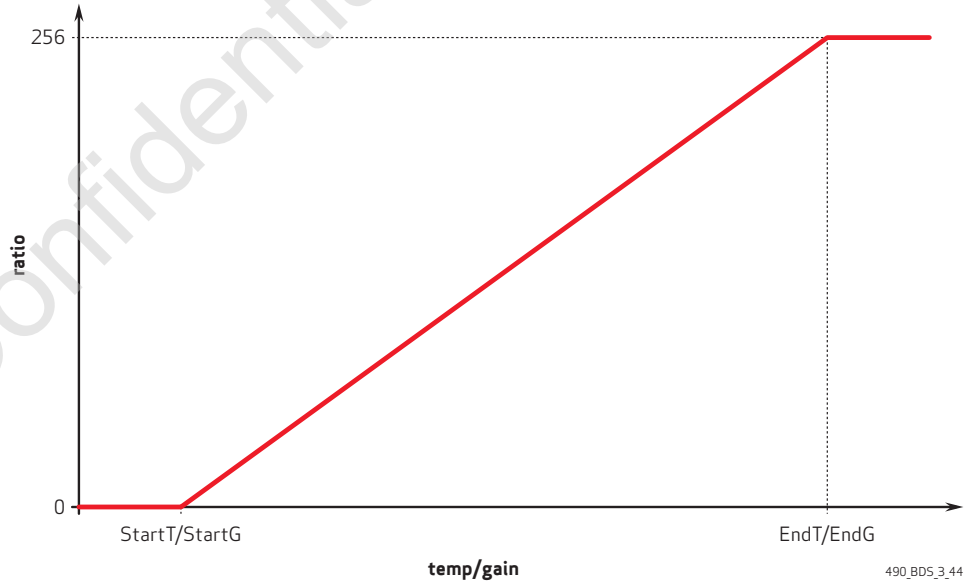
For HT control enable, the temperature range firmware register is {0x36D, 0x36E} and {0x86E, 0x86F} high temperature start and end values are 0x86E and 0x86F, respectively. In other scenes, the temperature is high but the exposure gain maintains a low level. The denoise function is based on the exposure gain level. So, the exposure gain range should be defined for the HT scene. In the HT scene, compute the ratio for the temperature and exposure gain. When the sensor temperature value (sensor register 0x304C) is higher than the HT limit temperature start, the HT control will go into effect.

For HT control, there are two types of ratios for temperature and exposure gain.

3.24.1 type 0 ratio

When type=0, it is used on the HT BLC offset function.

figure 3-44 type 0 ratio



If current gain < StartG {0x370, 0x371} or current temperature < StartT (0x36D), ratio = 0

If current gain > EndG {0x372, 0x373} and current temperature > EndT (0x36E), ratio = 256

If StartG {0x370, 0x371} < current gain < EndG {0x372, 0x373} and StartT (0x36D) < current temperature < EndT (0x36E), ratio=256×((temp-StartT)×(gain-StartG))/((EndT-StartT)×(EndG-StartG))

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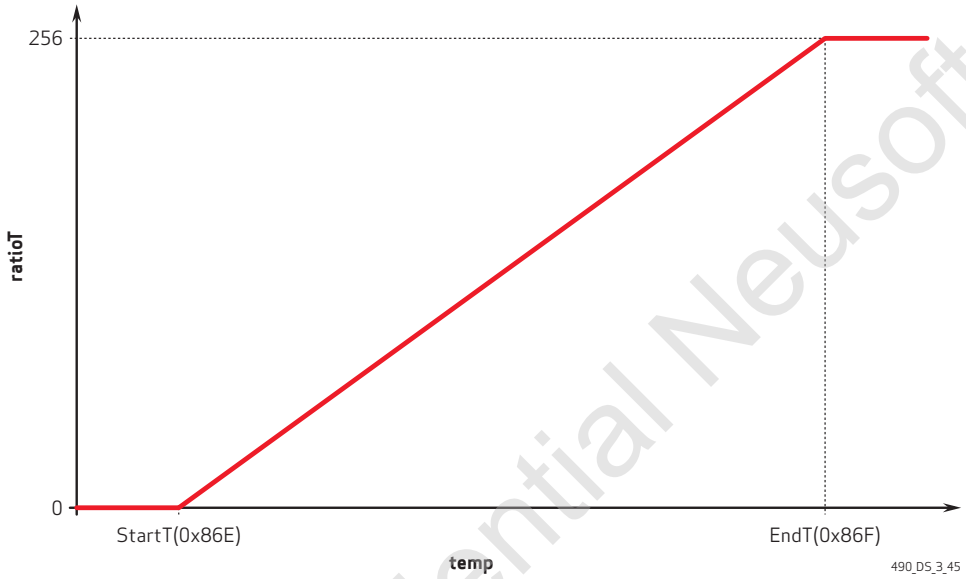
3.24.2 type 1 ratio

This is used on the HDR gain, saturation, LENC and RGB gamma functions.

In this type, it has weight control (0x86D) on exposure and temperature. For temperature, ratioT, see **figure 3-45**.

figure 3-45 type 1 ratioT



If current gain < StartG {0x870, 0x871} or current temperature < StartT (0x86E), ratioT = 0

If current gain > EndG {0x872, 0x873} and current temperature > EndT (0x86F), ratioT = 256

If StartG {0x870, 0x871} < current gain < EndG {0x872, 0x873} and StartT (0x86E) < current temperature < EndT (0x86F), ratioT = 256×((temp-StartT)×(gain-StartG))/((EndT-StartT)×(EndG-StartG))

For gain, ratioG, see **figure 3-46**.

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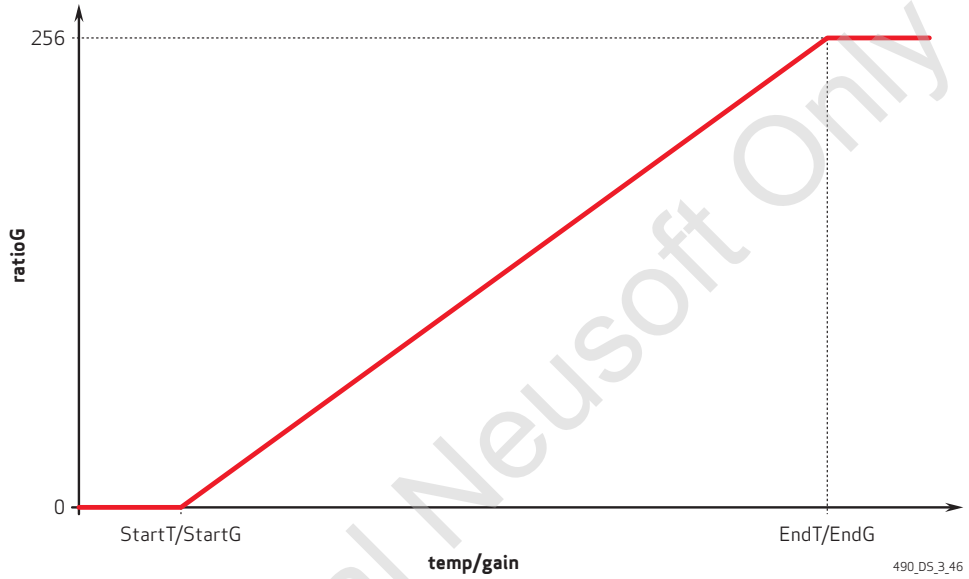
figure 3-46 type 1 ratioG



If the current gain < StartG {0x870, 0x871} or the current temperature < StartT (0x86E), ratioG = 0

If the current gain > EndG {0x872, 0x873} and the current temperature > EndT (0x86F), ratioG = 256

If StartG {0x870, 0x871} < current gain < EndG {0x872, 0x873} and StartT (0x86E) < the current temperature < EndT (0x86F), ratioG = 256×((temp-StartT)×(gain-StartG))/((EndT-StartT)×(EndG-StartG))

So, the last ratio is expressed as the following computational formula: Ratio = (ratioT×weightT + ratioG×(16-weightT))/16.

WeightT value is defined as the HT control weight between temperature and exposure gain.

If weightT = 8, it means gain, ratioG, and temperature, ratioT, have the same weight on the ratio.

If weightT > 8, it means temperature, ratioT, has more effect on the ratio.

If weightT < 8, it means gain, ratioG, has more effect on the ratio.

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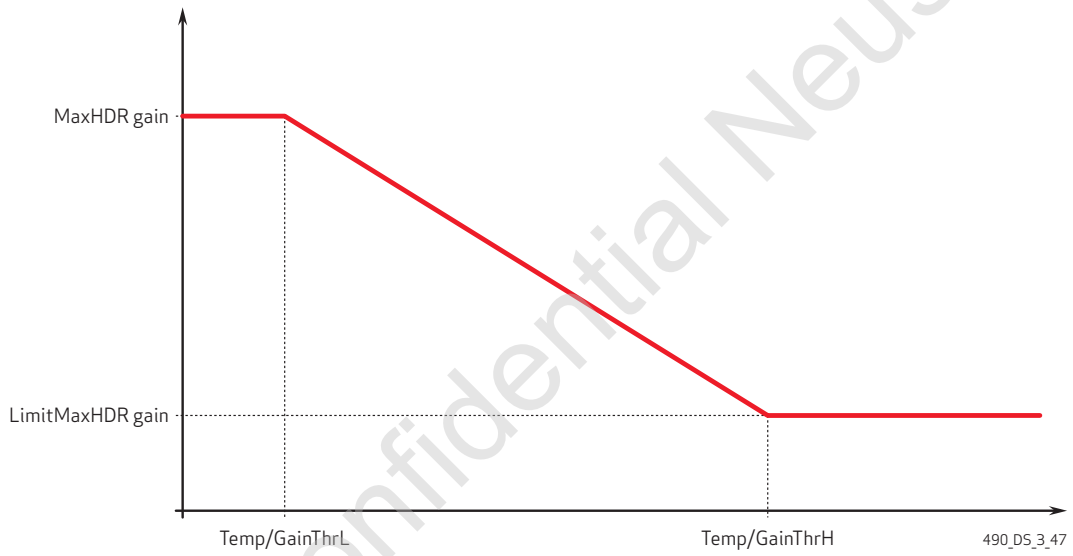
3.24.3 HDR gain control

To reach the target brightness, HDR gain can be applied to all pixels to increase brightness. For HT mode, noise levels increase and HDR gain in normal mode does not work. The HDR GainTarget {0x876, 0x877} plays a role on reducing noise level when it is in HT mode.

HDR gain control uses the second type ratio. The OV490 HDR target is:

- When gain < StartG or temperature < StartT, HDR gain target automatically runs in normal mode.
- When gain > EndG and temperature > EndT, HDR gain target value is the HDR gain target
- When StartG < gain < EndG and StartT< temperature < EndT, the HDR gain target is Max HDR gain target - ratio×(max HDR gain target - HT HDR gain target)/256

figure 3-47 HDR gain control



In HT mode, the HT HDR gain target value {0x876, 0x877} is bigger, the HDR gain applied on the pixel is bigger, so the image is brighter and has more noise. When the HT HDR gain target value is smaller and the HDR gain is smaller, the image is darker and noise is reduced in the image. In the HT mode, the right weightT can be selected depending on the noise source. If the noise comes from high temperature increasing, a bigger value for weighT can be selected. If the noise comes from gain increasing, the weightT is smaller.

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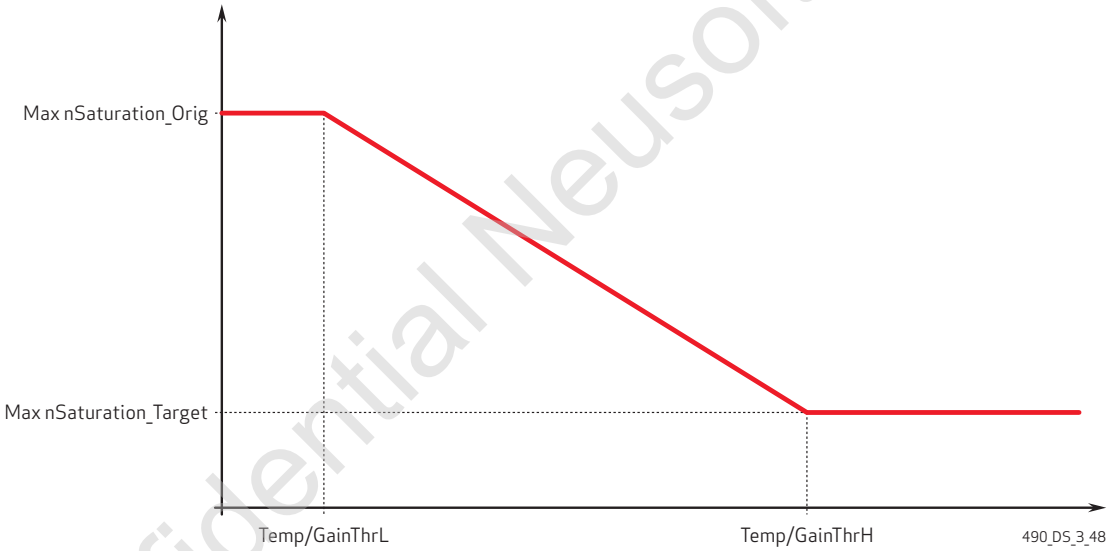
3.24.4 saturation control

In a common scene, the color matrix uses two factors to control saturation when gain is increasing. Its purpose is to limit color saturation from getting too high when gain is high. When temperature is high, BLC distributes unevenly and color in the image is not as accurate as in normal mode. The HT saturation control is used to maintain color accuracy.

In this mode, the ratio for temperature and gain will choose the second type of calculation. If register 0x89C is set to 1, the saturation function for HT mode will enabled.

figure 3-48 saturation factor control



When gain < HT StartG or temperature < HT StartT, color saturation will automatically run in normal mode based on the normal saturation target, Saturation_Orig {0x89D, 0x89E}.

When gain is > HT EndG and temperature > HT EndT, color saturation factor value is the HT saturation target {0x89F, 0x8A0}.

When HT StartG < gain< HT EndG and HT StartT < temperature < HT EndT, color saturation factor is Saturation_Orig - ratio×(Saturation_Orig - HTSaturationTarget)/256.

Saturation, defined by registers 0x89D and 0x89E, is a function in normal mode of the OV490. If values for registers 0x89D and 0x89E change, then the saturation in normal mode is influenced.

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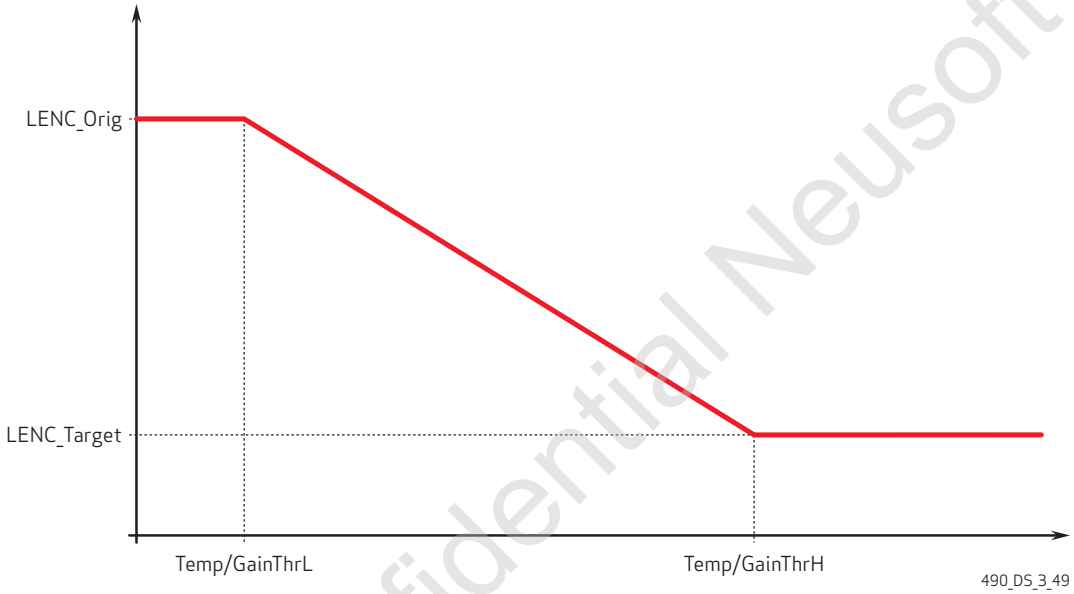
3.24.5 LENC control

The OV490 can automatically adjust gain for the pixel to adapt to sensor gain. In high temperature, the OV490 has more noise than under normal conditions. The LENC control function can suppress LENC gain to reduce the amount of noise. In LENC mode, the ratio for temperature and gain selects the second type of calculation.

If register 0x8A2 is set to 1, LENC control function for HT mode will be enabled.

figure 3-49 LENC factor control



When gain < StartG or temperature < StartT, LENC factor automatically runs in normal mode based on the LENC original value {0x8A3, 0x8A4}.

When gain is > EndG and temperature > EndT, LENC is in high temperature mode and its LENC factor is defined by LENC target {0x8A5, 0x8A6}.

When StartG < gain < EndG and StartT < temperature < EndT, color saturation factor is LENC original target - ratio×(LENC original target - LENC target)/256.

In this function, LENC original values {0x8A3, 0x8A4} also control the LENC factor in normal mode. OmniVision recommends to not change these values.

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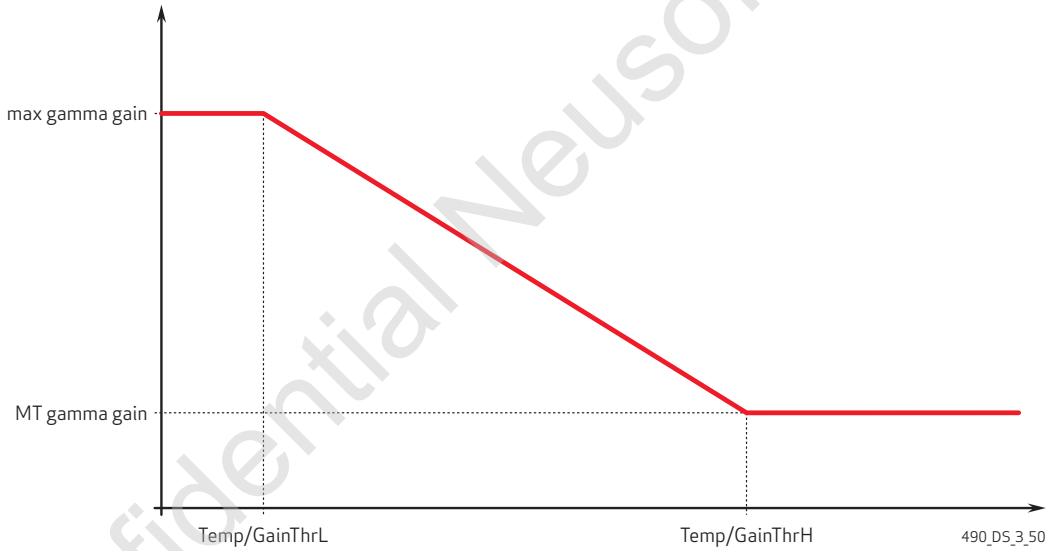
3.24.6 gamma control

In high temperature mode, the image has more noise than normal. High gamma gain can diminish the noise level. The HT gamma gain function is used to limit gamma corresponding to temperature changes in order to lessen noise brought on by image temperature.

In this mode, ratio for temperature and gain will select the second type of calculation.

If register 0x378 is set to 1, gamma gain control function for HT mode is enabled.

figure 3-50 gamma control



- When gain < StartG or temperature < StartT, LENC factor automatically runs in normal mode based on gamma gain {0x80207492, 0x80207493}
- When gain is > EndG and temperature > EndT, LENC is in high temperature mode and its gamma gain is defined by HT limit gamma threshold {0x379, 0x37A}
- When StartG < gain < EndG and StartT < temperature < EndT, color saturation factor is Gamma gain - ratio×(Gamma gain - HT Limit Gamma Threshold)/256

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3.24.7 BLC control

When the temperature reaches a high level, some sensors' BLC may be uneven and some images will display color issues. The OV490 supports the sensor BLC target function, which can add a BLC offset value automatically based on temperature to improve this issue.

The OV490 supports two methods to implement this function. Firmware register 0x374=0 means this function is disabled.

When firmware register 0x374=1, the OV490 adds the BLC value based on the current temperature and the OV490 real gain. When firmware register is 0x374=2, the OV490 adds a BLC value based on the sensor black value, Y, which changes based on temperature. This setting is used primarily with the OV10640.

The BLC base {0x38C, 0x38D}, {0x2D1, 0x2D2}, {0x2D8, 0x2D9} is for the BLC target value in normal temperature mode, which should be equal to the sensor BLC target value. For method 1, the OV490 uses firmware registers 0x375~0x377 to control the max BLC target value in temperature mode. For the second method, firmware registers 0x375~0x377. When the slope between black Y and the added BLC offset is increased in value, it causes an increase in the final BLC target value.

table 3-37 high temperature control firmware registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x2D1	BLCBASES_H	0x00	RW	Bit[7:0]: BLC target value[15:8] For S channel in normal temperature
0x2D2	BLCBASES_L	0x88	RW	Bit[7:0]: BLC target value[7:0] For S channel in normal temperature
0x2D8	BLCBASEVS_H	0x00	RW	Bit[7:0]: BLC target value[15:8] For VS channel in normal temperature
0x2D9	BLCBASEVS_L	0x88	RW	Bit[7:0]: BLC target value[7:0] For VS channel in normal temperature
0x38C	BLCBASEL_H	0x00	RW	Bit[7:0]: BLC target value[15:8] For L channel in normal temperature
0x38D	BLCBASEL_L	0x80	RW	Bit[7:0]: BLC target value[7:0] For L channel in normal temperature
0x36D	HTLIMITSTARTT	0x46	RW	Temperature Start Threshold in High Temperature BLC Function
0x36E	HTLIMITENDT	0x64	RW	Temperature End Threshold in High Temperature BLC Function

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table 3-37 high temperature control firmware registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x370	HTLIMITSTARTG_H	0x00	RW	Bit[7:0]: Analog gain start threshold[15:8] in high temperature BLC function
0x371	HTLIMITSTARTG_L	0xC0	RW	Bit[7:0]: Analog gain start threshold[7:0] in high temperature BLC function
0x372	HTLIMITENDG_H	0x01	RW	Bit[7:0]: Analog gain end threshold[15:8] in high temperature BLC function
0x373	HTLIMITENDG_L	0x80	RW	Bit[7:0]: Analog gain end threshold[7:0] in high temperature BLC function
0x374	ADDBLCOFFSETENABLE	0x02	RW	High Temperature BLC Target Offset Enable
0x375	HTLIMITBLCTHREL	0x30	RW	BLC Offset for L Exposure in High Temperature BLC Function
0x376	HTLIMITBLCTHRES	0x30	RW	BLC Offset for S Exposure in High Temperature BLC Function
0x377	HTLIMITBLCTHREVS	0x30	RW	BLC Offset for VS Exposure in High Temperature BLC Function
0x378	HTLIMITGAMMAENABLE	0x01	RW	High Temperature BLC Limit Gamma Function Enable
0x379	HTLIMITMINGAMMATHRE	0x04	RW	High Temperature BLC Limit Minimum Gamma Threshold
0x37A	HTLIMITMAXGAMMATHRE	0x08	RW	High Temperature BLC Limit Maximum Gamma Threshold
0x86C	BHTLIMITHDRGAINEN	0x01	RW	Bit[7:1]: Reserved Bit[0]: HTLimitHDRGainEn
0x86D	WEIGHTT	0x0C	RW	Bit[3:0]: Weight temp[3:0]
0x86E	NHTLIMITHDR_STARTTEMP	0x46	RW	Bit[7:0]: High temperature start
0x86F	HTLIMITHDR_ENDTEMP	0x64	RW	Bit[7:0]: High temperature end
0x870	HTLIMITHDR_STARTG HIGH	0x00	RW	Bit[7:0]: High temp HDR gain start value[15:8]
0x871	HTLIMITHDR_STARTG LOW	0x20	RW	Bit[7:0]: High temp HDR gain start value[7:0]
0x872	HTLIMITHDR_ENDG HIGH	0x01	RW	Bit[7:0]: High temp HDR gain end value[15:8]

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table 3-37 high temperature control firmware registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x873	HTLIMITHDR_ENDG LOW	0x00	RW	Bit[7:0]: High temp HDR gain end value[7:0]
0x876	HTHDRGAINTARGET	0x03	RW	Bit[7:0]: High temp HDR gain target value[15:8]
0x877	HTHDRGAINTARGET	0x00	RW	Bit[7:0]: High temp HDR gain target value[7:0]
0x89C	HTLIMITSATURATIONEN	0x01	RW	Bit[7:1]: Reserved Bit[0]: HTLimitSaturationEn
0x89D	SATURATION_ORIGHIGH	0x38	RW	Bit[7:0]: Normal CMX maximum factor
0x89E	SATURATION_ORIGLOW	0x18	RW	Bit[7:0]: Normal CMX minimum factor
0x89F	SATURATION_TARGET HIGH	0x18	RW	Bit[7:0]: High temperature CMX maximum factor
0x8A0	SATURATION_TARGET LOW	0x10	RW	Bit[7:0]: High temp CMX minimum factor
0x8A2	HTLIMITLENCEN	0x01	RW	Bit[7:1]: Reserved Bit[0]: bHTLimitLencEn
0x8A3	LENC_ORIGHIGH	0x38	RW	Bit[7:0]: Normal lens maximum factor
0x8A4	LENC_ORIGLOW	0x28	RW	Bit[7:0]: Normal lens minimum factor
0x8A5	LENC_TARGETHIGH	0x00	RW	Bit[7:0]: High temp maximum factor
0x8A6	LENC_TARGETLOW	0x00	RW	Bit[7:0]: High temp minimum factor

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4 register tables

4.1 chip address and memory allocation

table 4-1 AHB bus address allocation (sheet 1 of 2)

module name	address range	notes
32K ROM	0x00100000 ~ 0x00107FFF	
128K PRAM	0x00180000 ~ 0x0019FFFF	It is also mapped to the following addresses: 0~32K: 0x001A0000 ~ 0x001A7FFF 32K~64K: 0x001B0000 ~ 0x001B7FFF 64K~96K: 0x001C0000 ~ 0x001C7FFF 96K~128K:0x001D0000 ~ 0x001D7FFF
SC REG	0x80800000 ~ 0x80800FFF	
IDC REG	0x80820000 ~ 0x80827FFF	
VSGEN REG	0x80850000 ~ 0x8085FFFF	
ISP REG	0x80200000 ~ 0x8020FFFF	
SPI REG	0x80250000 ~ 0x8025FFFF	
TPM REG	0x80260000 ~ 0x8026FFFF	
UART0 REG	0x80284000 ~ 0x80285FFF	
DVP REG	0x80286000 ~ 0x80287FFF	
DMA0 REG	0x8028C000 ~ 0x8028CFFF	
DMA1 REG	0x8028D000 ~ 0x8028DFFF	
OTP REG	0x8028E000 ~ 0x8028EFFF	
MIPI RX REG	0x80290000 ~ 0x80291FFF	
MIPI TX REG	0x80292000 ~ 0x80293FFF	
CIF REG	0x80294000 ~ 0x80295FFF	
VFIFO REG	0x80296000 ~ 0x80297FFF	
COLORBAR0 REG	0x80298000 ~ 0x802980FF	
COLORBAR1 REG	0x80298100 ~ 0x802981FF	
COLORBAR FTX REG	0x80298200 ~ 0x802982FF	
ROMCV REG	0x8029A000 ~ 0x8029BFFF	
ODS REG	0x8029D000 ~ 0x8029DFFF	
EMB LINE REG	0x8029E000 ~ 0x8029FFFF	
UART1 REG	0x802A0000 ~ 0x802A1FFF	

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table 4-1 AHB bus address allocation (sheet 2 of 2)

module name	address range	notes
UART2 REG	0x802A2000 ~ 0x802A3FFF	
UART3 REG	0x802A4000 ~ 0x802A5FFF	
SCCB S REG	0x802A6000 ~ 0x802A7FFF	
SCCB MS0 REG	0x80900000 ~ 0x8090FFFF	
SCCB MS1 REG	0x80910000 ~ 0x8091FFFF	
IDC RAM	0x80828000 ~ 0x8082FFFF	for BIST only
VFIFO RAM	0x80220000 ~ 0x8022FFFF	
EMB LINE RAM	0x80830000 ~ 0x8083FFFF	for BIST only
RISC IC TAG RAM	0x80230000 ~ 0x80233FFF	for BIST only
RISC IC DAT RAM	0x80234000 ~ 0x80237FFF	for BIST only
RISC DC TAG RAM	0x80238000 ~ 0x8023BFFF	
RISC DC DAT RAM	0x8023C000 ~ 0x8023FFFF	
ISP RAM	0x80240000 ~ 0x8024FFFF	
ISP AWB RAM	0x80840000 ~ 0x8084FFFF	

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4.2 CPU interrupt

table 4-2 group 1 interrupts (sheet 1 of 2)

level trigger	interrupt	notes
31	RSVD	
30	MTX_FS_DONE	
29	MTX_LAST_LINE	
28	EMBL_CRC_ERR	
27	EMBL_EOF	
26	EMBL_SOF	
25	ODS_EOF	
24	VFIFO_SOF	
23	VFIFO_STATUS (UNDERFLOW, OVERFLOW)	
22	FSIN1	
21	FSIN0	
20	FSYNC	
19	VSGEN_INT	
18	DVP_VSYNC	
17	DMAS_DONE	
16	DMA_DONE	
15	TPM_INT	
14	ISP_YUV_STAT_DONE	
13	ODS_SOF	
12	HOST_CMD	
11	GPIO_GLOBAL	
10	SUSPEND/SLEEP	
9	GPIO RSVD	
8	SUSPEND RSVD	
edge trigger		
7	ISP_AWB2_DONE	
6	ISP_AWB1_DONE	
5	ISP_AEC2_DONE	

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table 4-2 group 1 interrupts (sheet 2 of 2)

level trigger	interrupt	notes
4	ISP_AEC1_DONE	
3	ISP_HDR_STAT2_DONE	
2	ISP_HDR_STAT1_DONE	
1	ISP_EOF	
0	ISP_SOF	

table 4-3 group 2 interrupts (sheet 1 of 2)

level trigger	interrupt	notes
31	IDC_VSYNC	
30	CIF_CNT_INT	
29	CIF_EOF	
28	CIF_SOF	
27	EMBL_RD_DONE	
26	EMBL_WR_DONE	
25	MRX_S1_EOF_V0	
24	MRX_S1_SOF_V0	
23	MRX_S0/1_EOF_V1	
22	MRX_S0/1_SOF_V1	
21	MRX_S0_EOF_V0	
20	MRX_S0_SOF_V0	
19	UART3_INT	
18	UART2_INT	
17	UART1_INT	
16	UART0_INT	
15	MRX_S0/1_DET_ERR	
14	SSCCB_FIFO_INT	
13	SCCB_MS1_INT	
12	SCCB_MS0_INT	
11	SPI_M_TX_FINISH	

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table 4-3 group 2 interrupts (sheet 2 of 2)

level trigger	interrupt	notes
10	SPI_M_RX_FINISH	
9	SPI_TX_INT	
8	SPI_RX_INT	
edge trigger		
7	IDC_EOF	
6	IDC_SOF	
5	ISP_EOF2	
4	ISP_EOF1	
3	ISP_YUV_STAT2_DONE	
2	ISP_YUV_STAT1_DONE	
1	ISP_LINE_INT2	
0	ISP_LINE_INT1	

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4.3 embedded line control

base address: 0x8029E000

SRAM base address: 0x80830000

- SEI_sram1: 0x80830000 ~ 0x8083050F
- SEI_sram2: 0x80830800 ~ 0x80830D0F
- SEI_sram3: 0x80831000 ~ 0x8083150F
- SEI_sram4: 0x80831800 ~ 0x80831D0F
- OVI_sram1: 0x80832000 ~ 0x8083250F
- OVI_sram2: 0x80832800 ~ 0x80832D0F

table 4-4 embedded line control registers (sheet 1 of 13)

address	register name	default value	R/W	description
0x8029E000	EMBEDLINE CTRL	0x00	RW	Embedline Control Bit[7:6]: Debug mode Bit[5]: OVI single address 0: For normal, CPU access OVI SRAM by AHB bus 1: For OVI SRAM AHB address is a single address, when the OVI line is inserted, DMA moves data from ISP to embline only in single address mode, one write action takes 1 byte. Bit[4]: Single sensor 0: Input image is dual sensor 1: Input image is single sensor Bit[3]: OVI first 0: SEI line before OVI line (recommended) 1: OVI line before SEI line Bit[2]: Auto insertion 0: Manual mode, use manual setting to insert lines 1: Auto mode, use detected setting to insert lines, detected setting is from the previous frame. Bit[1]: Enable embedline in YUV 1: Select YUV data to insert embedline Bit[0]: Enable embedline in raw 1: Select RAW data to insert embedline Note: SEI is related to sensor information lines and OVI is related to OV490 information lines.

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table 4-4 embedded line control registers (sheet 2 of 13)

address	register name	default value	R/W	description
0x8029E001	IMAGE WIDTH1 LOW	0x00	RW	Bit[7:0]: image_width1[7:0]
0x8029E002	IMAGE WIDTH1 HIGH	0x00	RW	Bit[7:0]: image_width1[15:8]
0x8029E003	IMAGE HEIGHT1 LOW	0x00	RW	Bit[7:0]: image_height1[7:0]
0x8029E004	IMAGE HEIGHT1 HIGH	0x00	RW	Bit[7:0]: image_height1[15:8]
0x8029E005	IMAGE WIDTH2 LOW	0x00	RW	Bit[7:0]: image_width2[7:0]
0x8029E006	IMAGE WIDTH2 HIGH	0x00	RW	Bit[7:0]: image_width2[15:8]
0x8029E007	IMAGE HEIGHT2 LOW	0x00	RW	Bit[7:0]: image_height2[7:0]
0x8029E008	IMAGE HEIGHT2 HIGH	0x00	RW	Bit[7:0]: image_height2[15:8]
0x8029E009	SEI LINE NUM IN	0x00	RW	Bit[7]: Only left SEI Only left sensor has SEI 0: When single sensor and the sensor is right, or when there are 2 sensors, this bit is set to low 1: When there is a single sensor and the sensor is left, this bit is set to high Bit[6:4]: Number of sensor information lines input at the end of the image 000: Reserved 001: 1 line 010: 2 lines 011 3 lines 100: 4 lines Others: Reserved Bit[3]: Only right SEI Only right sensor has SEI 0: When single sensor and the sensor is left, or when 2 sensors, this bit is set to low 1: When single sensor and the sensor is right, this bit is set to high Bit[2:0]: Number of sensor information lines input at the beginning of the image 000: Reserved 001: 1 line 010: 2 lines 011: 3 lines 100: 4 lines Others: Reserved

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table 4-4 embedded line control registers (sheet 3 of 13)

address	register name	default value	R/W	description
0x8029E00A	INSERT SENSOR INFORMATION LINE NUMBER	0x00	RW	Bit[7]: Do not used Bit[6:4]: Insert sensor information line number at the end of frame 000: 0 line 001: 1 line (1 line after image frame) 010: 2 lines (2 lines after image frame) 011: 3 lines (3 lines after image frame) 100: 4 lines (4 lines after image frame) Others: Reserved Bit[3]: SEI_empty_en Bit[2:0]: Insert sensor information line number before frame 000: 0 line 001: 1 line (1 line before image frame) 010: 2 lines (2 lines before image frame) 011: 3 lines (3 lines before image frame) 100: 4 lines (4 lines before image frame) Others: Reserved

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table 4-4 embedded line control registers (sheet 4 of 13)

address	register name	default value	R/W	description
0x8029E00B	INSERT OV490 INFORMATION LINE NUMBER	0x00	RW	Bit[7]: Reserved Bit[6:4]: Insert OV490 information line number after frame 000: 0 line 001: 1 line (1 line after image frame) 010: 2 lines (2 lines after image frame) 011: 3 lines (3 lines after image frame) 100: 4 lines (4 lines after image frame) Others: Reserved Bit[3]: OVI empty enable 0: When OVI SRAM is empty, still read SRAM as output timing 1: When OVI SRAM is empty, do not read SRAM Bit[2:0]: Insert OV490 information line number before frame 000: 0 line 001: 1 line (1 line before image frame) 010: 2 lines (2 lines before image frame) 011: 3 lines (3 lines before image frame) 100: 4 lines (4 lines before image frame) Others: Reserved
0x8029E00C	INTERRUPT EN	0x00	RW	Bit[7]: right_sensor 0: For left sensor 1: For right sensor Bit[6]: crc_order 0: Input CRC 4 byte order is LSB 1: Input CRC 4 byte order is MSB Bit[5]: rx_ck_sum_inv 1: Invert 32b of CRC to check Bit[4]: int_ovi_sram_tx_end enable Bit[3]: int_ovi_sram_rx_end enable Bit[2]: int_SEI_sram_tx_end enable Bit[1]: int_SEI_sram_rx_end enable Bit[0]: int_crc_err enable

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table 4-4 embedded line control registers (sheet 5 of 13)

address	register name	default value	R/W	description
0x8029E00D	TIM GEN CONTROL	0x00	RW	Bit[7]: Do not used Bit[6]: Transmit check sum value invert 0: Not allowed 1: Invert 32b of CRC to output Bit[5:4]: Output byte rate Output byte per cycle in insert lines 00: Reserved 01: 1 byte per cycle 10: 2 bytes per cycle 11: 3 bytes per cycle Bit[3:2]: Reserved Bit[1]: OVI data MSB output select 0: For OVI data LSB output 1: For OVI data MSB output Bit[0]: Output EOF select 0: Output EOF generated by FSM 1: Output EOF by EMB self counted (recommended)

0x8029E00E	BYTE LEFT	0x00	RW	To handle the remainder of 3, because the output of raw is in 3 bytes per cycle
				Only when RD[5:4] = 2'b11, set these bits.
				Bit[7:6]: r_total_lft2
				r_total_lft2 = (total_byte2-4) mod 3 in OVI line
				//r_valid_lft is in raw data, r_valid_lft = (valid_byte - 4) mod 3
				//r_total_lft is in raw data, r_total_lft = (total_byte - 4) mod 3
				Bit[5:4]: r_total_lft1
				r_total_lft1 = (total_byte1-4) mod 3 in SEI line
				Bit[3:2]: r_valid_lft2
				r_valid_lft2 = (valid_byte2-4) mod 3 in OVI line
				Bit[1:0]: r_valid_lft1
				r_valid_lft1 = (valid_byte1-4) mod 3 in SEI line

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table 4-4 embedded line control registers (sheet 6 of 13)

address	register name	default value	R/W	description
0x8029E00F	IO BYTE ORDER	0x00	RW	Bit[7:6]: Reserved Bit[5]: Check CRC mode 0: Check CRC in each line 1: Check CRC in the last line Bit[4]: ovi_crc_wrong_en 0: Doing nothing 1: Output CRC as 0x55AA55AA if buffer underflow Bit[3]: SEI_crc_wrong_en 0: Doing nothing 1: Output CRC as 0x55AA55AA if sensor CRC input is wrong Bit[2:1]: r_take_byte For sensor, input is tag+data+tag+data 00: Take all data 01: Take one byte per two bytes 10: Take one byte per four bytes 11: Take one byte per six bytes Bit[0]: SEI_byte_order 0: SEI_data_i[31:0] 1: {SEI_data_i[7:0], SEI_data_i[15:8], SEI_data_i[23:16], SEI_data_i[31:24]}
0x8029E010	HORIZONTAL LINE CYCLE NUMBER LOW	–	R	Bit[7:0]: Line cycle num[7:0] Hline in cycles low byte
0x8029E011	HORIZONTAL LINE CYCLE NUMBER HIGH	–	R	Bit[7:0]: Line cycle num[15:8] Hline in cycles high byte
0x8029E012	HORIZONTAL BLANKING CYCLE NUMBER LOW	–	R	Bit[7:0]: Line blanking cycle num[7:0] Hblanking in cycles low byte
0x8029E013	HORIZONTAL BLANKING CYCLE NUMBER HIGH	–	R	Bit[7:0]: Line blanking cycle num[15:8] Hblanking in cycles high byte
0x8029E014	VERTICAL BLANKING CYCLE NUMBER LOW	–	R	Bit[7:0]: Vblanking cycle num[7:0] Vblanking in cycles low byte
0x8029E015	VERTICAL BLANKING CYCLE NUMBER MID	–	R	Bit[7:0]: Vblanking cycle num[15:8] Vblanking in cycles middle byte
0x8029E016	VERTICAL BLANKING CYCLE NUMBER HIGH	–	R	Bit[7:0]: Vblanking cycle num[23:16] Vblanking in cycles high byte

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table 4-4 embedded line control registers (sheet 7 of 13)

address	register name	default value	R/W	description
0x8029E017	LATENCY CYCLE NUMBER LOW	–	R	Bit[7:0]: Latency cycle num[7:0] Latency in cycles low byte There must be latency > R05[2:0] × hline + hblanking, so R05[2:0] insert line number relies on it.
0x8029E018	LATENCY CYCLE NUMBER MID	–	R	Bit[7:0]: Latency cycle num[15:8] Latency in cycles middle byte (high byte in register 0x8029E02F)
0x8029E019	ERROR	–	R	Bit[7]: Reserved Bit[6]: SEI rd but empty, SEI SRAM underflow This bit indicates underflow (e.g., when reading SRAM but it is empty). The solution is try to write SRAM earlier, or read buffer later. Bit[5]: OVI rd but empty, OVI SRAM underflow This bit indicates underflow (e.g., when reading SRAM, but it is empty). The solution is try to write SRAM earlier or read buffer later. Bit[4]: SEI empty, combine logic signal, internal use Bit[3]: OVI empty, combine logic signal, internal use Bit[2]: Overlap error Embedline and image line overlapped Bit[1]: latency_error2 Timing intervals is not enough to insert OVI data before image (if OVI data follows SEI data) Bit[0]: latency error1 vblanking < hline Timing interval is not enough to insert SEI and OVI data before image
0x8029E01A	INPUT IMAGE WIDTH LOW	–	R	Bit[7:0]: input_image_width[7:0]
0x8029E01B	INPUT IMAGE WIDTH HIGH	–	R	Bit[7:0]: input_image_width[15:8] Left and right sensor, respectively
0x8029E01C	INPUT IMAGE HEIGHT LOW	–	R	Bit[7:0]: input_image_height[7:0]
0x8029E01D	INPUT IMAGE HEIGHT HIGH	–	R	Bit[7:0]: input_image_height[15:8] Left and right sensor totally

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table 4-4 embedded line control registers (sheet 8 of 13)

address	register name	default value	R/W	description
0x8029E01E	SEI_LINE_NUM CUR_ST	–	R	For Debug, Status of State Machine Bit[7:6]: Reserved Bit[5:3]: SEI_line num 000: No SEI line 001: First SEI line 100: Fourth SEI line Bit[2:0]: cur_st If SEI goes first: 0000: For IDLE 0001: For VBLANK 0010: For SEI_B4 0011: For OVI B4 0100: For IMAGE 0101: For SEI AF 0110: For OVI AF 0111: For ERROR If OVI goes first: 0000: For IDLE 0001: For VBLANK 0010: For OVI B4 0011: For SEI_B4 0100: For IMAGE 0101: For OVI AF 0110: For SEI AF 0111: For ERROR

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table 4-4 embedded line control registers (sheet 9 of 13)

address	register name	default value	R/W	description
0x8029E01F	OVI_LINE_NUM CUR_ST	–	R	For debug, the status of state machine Bit[7:6]: Reserved Bit[5:3]: ovi_line num 000: No OVI line 001: First OVI line 010: Second OVI line 011: Third OVI line 100: Fourth OVI line Bit[2:0]: cur_st If SEI goes first: 0000: For IDLE 0001: For VBLANK 0010: For SEI_B4 0011: For OVI B4 0100: For IMAGE 0101: For SEI AF 0110: For OVI AF 0111: For ERROR If OVI goes first: 0000: For IDLE 0001: For VBLANK 0010: For OVI B4 0011: For SEI_B4 0100: For IMAGE 0101: For OVI AF 0110: For SEI AF 0111: For ERROR
0x8029E020	MANUAL HORIZONTAL LINE CYCLE NUMBER LOW	0x00	RW	Bit[7:0]: Line cycle num[7:0] hline_man in cycles
0x8029E021	MANUAL HORIZONTAL LINE CYCLE NUMBER HIGH	0x00	RW	Bit[7:0]: Line cycle num[15:8] hline_man in cycles
0x8029E022	MANUAL HORIZONTAL BLANKING CYCLE NUMBER LOW	0x00	RW	Bit[7:0]: Line blanking cycle num[7:0] Hblanking_man in cycles
0x8029E023	MANUAL HORIZONTAL BLANKING CYCLE NUMBER HIGH	0x00	RW	Bit[7:0]: Line blanking cycle num[15:8] Hblanking_man in cycles
0x8029E024	MANUAL VERTICAL BLANKING CYCLE NUMBER LOW	0x00	RW	Bit[7:0]: Vblanking cycle num[7:0] Vblanking_man in cycles

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table 4-4 embedded line control registers (sheet 10 of 13)

address	register name	default value	R/W	description
0x8029E025	MANUAL VERTICAL BLANKING CYCLE NUMBER MID	0x00	RW	Bit[7:0]: Vblanking cycle num[15:8] Vblanking_man in cycles
0x8029E026	MANUAL VERTICAL BLANKING CYCLE NUMBER	0x00	RW	Bit[7:0]: Vblanking cycle num[23:16] Vblanking_man in cycles
0x8029E027	VALID BYTES1 LOW	0x00	RW	Bit[7:0]: SEI valid bytes first line[7:0] Must be in multiples of four
0x8029E028	VALID BYTES1 HIGH	0x00	RW	Bit[7:0]: SEI valid bytes first line[15:8] Must be in multiples of four
0x8029E029	VALID_BYTES2 LOW	0x00	RW	Bit[7:0]: OVI valid bytes in line before image[7:0] Must be in multiples of four
0x8029E02A	VALID_BYTES2 HIGH	0x00	RW	Bit[7:0]: OVI valid bytes in line before image[15:8] Must be in multiples of four
0x8029E02B	TOTAL_BYTES1 LOW	0x00	RW	Bit[7:0]: SEI total bytes per line[7:0]
0x8029E02C	TOTAL_BYTES1 HIGH	0x00	RW	Bit[7:0]: SEI total bytes per line[15:8]
0x8029E02D	TOTAL_BYTES2 LOW	0x00	RW	Bit[7:0]: OVI total bytes per line[7:0]
0x8029E02E	TOTAL_BYTES2 HIGH	0x00	RW	Bit[7:0]: OVI total bytes per line[15:8]
0x8029E02F	LATENCY CYCLE NUMBER HIGH	–	R	Bit[7:0]: Latency cycle num[23:16] Latency in cycles high byte (low byte in register 0x8029E018)

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table 4-4 embedded line control registers (sheet 11 of 13)

address	register name	default value	R/W	description
0x8029E030	R_BYTE_ORDER	0x00	RW	Bit[7:6]: Not used Bit[5]: OVI raw swap 0: {data2, data1, data0} 1: {data0, data1, data2} Bit[4]: OVI YUV swap 0: {data1, data0} 1: {data0, data1} Bit[3]: SEI raw swap 0: {data2, data1, data0} 1: {data0, data1, data2} Bit[2]: SEI YUV swap 0: {data1, data0} 1: {data0, data1} Bit[1:0]: r_byte_order 00: Put byte at low location {4'b0,data[7:0]} 01: Put byte at mid location {2'b0,data[7:0],2'b0} 10: Put byte at high location {data[7:0],4'b0} 11: Not allowed
0x8029E031	OVI SVLD LOW	0x00	RW	In OVI Output Lines, When in Separate Line Mode, OVI Line Byte Num Per Line Low Byte
0x8029E032	OVI SVLD HIGH	0x00	RW	In OVI Output Lines, When in Separate Line Mode, OVI Line Byte Num Per Line High Byte
0x8029E033	SEI DELAY	0x00	RW	SEI Line Output Delay, Unit Is 4 Cycles
0x8029E034	OVI DELAY	0x00	RW	OVI Line Output Delay, Unit Is 4 Cycles
0x8029E035	LINE DELAY LOW	0x00	RW	Bit[7:0]: Line delay[7:0] After image insert lines can be delayed unit is line
0x8029E036	SEI HEADER LENGTH	0x00	RW	Bit[7:4]: Line delay[11:8] Bit[3:0]: header_length Unit is 8B, to add header at the beginning of SEI line, CPU must write SEI SRAM to fill the first several bytes, header will be added before the SEI data
0x8029E037	BYTE LEFT2	0x00	RW	Usage (see register 0x8029E00E) Bit[7:6]: OVI valid2 left Bit[5:4]: SEI valid4 left Bit[3:2]: SEI valid3 left Bit[1:0]: SEI valid2 left
0x8029E038	VALID_WORD_CNT_REG	--	R	Bit[7:0]: valid_word_cnt_reg[7:0] SEI input valid word number

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table 4-4 embedded line control registers (sheet 12 of 13)

address	register name	default value	R/W	description
0x8029E039	VALID_WORD_CNT_REG	–	R	Bit[7:6]: Reserved Bit[5:0]: valid_word_cnt_reg[13:8] SEI input valid word number
0x8029E03A	RO_TOTAL_BYTE1 LOW	–	R	Bit[7:0]: Output total byte1[7:0]
0x8029E03B	RO_TOTAL_BYTE1 HIGH	–	R	Bit[7:0]: Output total byte1[15:8]
0x8029E03C	RO_TOTAL_BYTE2 LOW	–	R	Bit[7:0]: Output total byte2[7:0]
0x8029E03D	RO_TOTAL_BYTE2 HIGH	–	R	Bit[7:0]: Output total byte2[15:8]
0x8029E03E	RO_TOTAL_HEIGHT LOW	–	R	Bit[7:0]: Output total height[7:0]
0x8029E03F	RO_TOTAL_HEIGHT HIGH	–	R	Bit[7:0]: Output total height[15:8]
0x8029E040	SEI_VALID_BYTE2 LOW	0x00	RW	Bit[7:0]: SEI valid byte2[7:0] SEI line2 valid byte Must be in multiples of four
0x8029E041	SEI_VALID_BYTE2 HIGH	0x00	RW	Bit[7:0]: SEI valid byte2[15:8] SEI line2 valid byte Must be in multiples of four
0x8029E042	SEI_VALID_BYTE3 LOW	0x00	RW	Bit[7:0]: SEI valid byte3[7:0] SEI line3 valid byte Must be in multiples of four
0x8029E043	SEI_VALID_BYTE3 HIGH	0x00	RW	Bit[7:0]: SEI valid byte3[15:8] SEI line3 valid byte Must be in multiples of four
0x8029E044	SEI_VALID_BYTE4 LOW	0x00	RW	Bit[7:0]: SEI valid byte4[7:0] SEI line4 valid byte Must be in multiples of four
0x8029E045	SEI_VALID_BYTE4 HIGH	0x00	RW	Bit[7:0]: SEI valid byte4[15:8] SEI line4 valid byte Must be in multiples of four

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table 4-4 embedded line control registers (sheet 13 of 13)

address	register name	default value	R/W	description
0x8029E046	INT CLR	0x00	RW	To Clear Status Bit, Write 1. Then Write 0 to the Cleared Bit to Reset Bit[7:4]: Reserved Bit[3]: OVI_rd_end clear bit Bit[2]: OVI_wr_end clear bit Bit[1]: SEI_rd_end clear bit Bit[0]: SEI_wr_end clear bit When interrupt arises, set these bits to clear them. After interrupts clear, these clear bits,
0x8029E047	RSVD	–	–	Reserved
0x8029E048	ADD EMBL FLAG EN	0x00	RW	Bit[7:2]: Reserved Bit[1]: YUV add embline flag enable 0: Not allowed 1: Put embline flag on YUV image lines Bit[0]: RAW add embline flag enable 0: Not allowed 1: Put embline flag on RAW image lines
0x8029E049	OVI_VALID_BYTE2 LOW	0x00	RW	Bit[7:0]: OVI valid byte2[7:0] OVI line2 valid byte must be in multiples of four
0x8029E04A	OVI_VALID_BYTE2 HIGH	0x00	RW	Bit[7:0]: OVI valid byte2[15:8] OVI line2 valid byte must be in multiples of four

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4.4 color bar 0/1/2 control

4.4.1 color bar 0 (pre)

base address: 0x80298000 colorbar0

table 4-5 color bar 0 pre registers

address	register name	default value	R/W	description
0x80298000	CB_CTRL	0x00	RW	Bit[7:6]: Image data width select 00: 12 bits 01: 10 bits 1x: 8 bits Bit[5:4]: px_rate 00: For 1cpp, one valid data per cycle 01: For 2cpp, one valid data every 2 cycles 10: For 4cpp, one valid data every 4 cycles 11: For 8cpp, one valid data every 8 cycles Bit[3]: RAW color bar select 0: Output YUV422 image 1: Output raw image Bit[2]: Color bar roll enable 0: Normal color bar 1: Rolling color bar enable Bit[1]: Color bar 75 select 0: Color bar-100 format 1: Color bar-75 format Bit[0]: Color bar enable 0: Disable 1: Enable
0x80298001	HSIZE LOW	0x80	RW	Bit[7:0]: Image horizontal size[7:0]
0x80298002	HSIZE HIGH	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: Image horizontal size[12:8]
0x80298003	VSIZE LOW	0xE0	RW	Bit[7:0]: Image vertical size[7:0]
0x80298004	VSIZE HIGH	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Image vertical size[11:8]
0x80298005	VDELAY	0x10	RW	Bit[7:0]: Lines number between VSYNC and first HREF
0x80298006	VDMY	0x10	RW	Bit[7:0]: Lines number between last HREF and EOF
0x80298007	VBLANK	0x10	RW	Bit[7:0]: Lines between EOF and next VSYNC
0x80298008	HBLANK	0x14	RW	Bit[7:0]: Reference horizontal blank Real horizontal blank is 8*pixel_rate*value

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4.4.2 color bar 1 (pre)

base address: 0x80298100 colorbar1

table 4-6 color bar 1 pre registers

address	register name	default value	R/W	description
0x80298100	CB_CTRL	0x00	RW	Bit[7:6]: Image data width select 00: 12 bits 01: 10 bits 1x: 8 bits Bit[5:4]: pixel rate 00: For 1cpp, one valid data per cycle 01: For 2cpp, one valid data every 2 cycles 10: For 4cpp, one valid data every 4 cycles 11: For 8cpp, one valid data every 8 cycles Bit[3]: RAW color bar select 0: Output YUV422 image 1: Output raw image Bit[2]: Color bar roll enable 0: Normal color bar 1: Rolling color bar enable Bit[1]: Color bar 75 select 0: Color bar-100 format 1: Color bar-75 format Bit[0]: Color bar enable 0: Disable 1: Enable
0x80298101	HSIZE LOW	0x80	RW	Bit[7:0]: Image horizontal size[7:0]
0x80298102	HSIZE HIGH	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: Image horizontal size[12:8]
0x80298103	VSIZE LOW	0xE0	RW	Bit[7:0]: Image vertical size[7:0]
0x80298104	VSIZE HIGH	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Image vertical size[11:8]
0x80298105	VDELAY	0x10	RW	Bit[7:0]: Lines number between VSYNC and first HREF
0x80298106	VDMY	0x10	RW	Bit[7:0]: Lines number between last HREF and EOF
0x80298107	VBLANK	0x10	RW	Bit[7:0]: Lines between EOF and next VSYNC
0x80298108	HBLANK	0x14	RW	Bit[7:0]: Reference horizontal blank Real horizontal blank is 8*pixel_rate*value

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4.4.3 color bar 2 (post)

base address: 0x80298200 colorbar2

table 4-7 color bar2 post registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x80298200	CB_CTRL	0x00	RW	Bit[7:6]: Image data width select 00: 12 bits 01: 10 bits 10: 8 bits 11: Reserved Bit[5:4]: Pixel rate 00: For 1cpp, one valid data per cycle 01: For 2cpp, one valid data every 2 cycles 10: For 4cpp, one valid data every 4 cycles 11: For 8cpp, one valid data every 8 cycles Bit[3]: RAW color bar select 0: Output YUV422 image 1: Output raw image Bit[2]: Color bar roll enable 0: Normal color bar 1: Rolling color bar enable Bit[1]: Color bar 75 select 0: Color bar-100 format 1: Color bar-75 format Bit[0]: Color bar enable 0: Disable 1: Enable
0x80298201	HSIZE LOW	0x80	RW	Bit[7:0]: Image horizontal size[7:0]
0x80298202	HSIZE HIGH	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: Image horizontal size[12:8]
0x80298203	VSIZE LOW	0xE0	RW	Bit[7:0]: Image vertical size[7:0]
0x80298204	VSIZE HIGH	0x01	RW	Bit[7:5]: Reserved Bit[3:0]: Image vertical size[11:8]
0x80298205	VDELAY	0x10	RW	Bit[7:0]: Lines number between VSYNC and first HREF
0x80298206	VDMY	0x10	RW	Bit[7]: DVP color bar (YUV) enable 0: 24-bits output 1: 12-bits output Bit[6]: mipi_tx color bar YUYV format 0: YUYV 1: UYVY Bit[5:0]: Lines number between last HREF and EOF

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table 4-7 color bar2 post registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x80298207	VBLANK	0x10	RW	Bit[7:0]: Lines between EOF next VSYNC
0x80298208	HBLANK LOW	0x14	RW	Bit[7:0]: Reference horizontal blank[7:0] Real horizontal blank is 8*pixel_rate*value
0x80298209	HBLANK HIGH	0x00	RW	Bit[7:0]: Reference horizontal blank[15:8] Real horizontal blank is 8*pixel_rate*value

4.5 CIF control

base address: 0x80294000

table 4-8 CIF registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x80294000	CIF_CTRL0	0x00	RW	Bit[7:6]: Image data width select 00: 12 bits 01: 10 bits 1x: 8 bits Bit[5]: HSYNC/HREF mode 0: HREF mode (normal) 1: HSYNC mode (shared HREF pin) Bit[3]: VSYNC polarity select 0: Positive edge 1: Negative edge Bit[2]: SOF mode 0: VSYNC negative edge 1: VSYNC positive edge Bit[1]: Not used Bit[0]: CIF enable 0: Disable 1: Enable
0x80294001	CIF_CTRL1	0x00	RW	Bit[7:5]: Reserved Bit[4]: Image format select 0: RAW 1: YUV422 Bit[3:0]: Reserved
0x80294002	CIF_CTRL2	0x00	RW	Bit[7]: Reserved Bit[6]: Image data (raw) output position 0: Image data output from high 8/10 bits 1: Image data output from low 8/10 bits Bit[5:0]: Reserved

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table 4-8 CIF registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x80294004	HSIZE LOW	0x80	RW	Bit[7:0]: Image horizontal size[7:0]
0x80294005	HSIZE HIGH	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: Image horizontal size[12:8]
0x80294006	VSIZE LOW	0xE0	RW	Bit[7:0]: Image vertical size[7:0]
0x80294007	VSIZE HIGH	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Image vertical size[11:8]
0x80294008	HSTART LOW	0x00	RW	Bit[7:0]: Image horizontal start position[7:0]
0x80294009	HSTART HIGH	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Image horizontal start position[11:8]
0x8029400A	VSTART LOW	0x00	RW	Bit[7:0]: Image vertical start position[7:0]
0x8029400B	VSTART HIGH	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Image vertical start poistion[11:8]
0x8029400C	CIF_CTRL3	0x00	RW	Bit[7]: HREF polarity select 0: Positive edge 1: Negative edge Bit[6:4]: Reserved Bit[3]: Frame control enable 0: Disable 1: Enable Bit[2:0]: Reserved
0x8029400D	FRAME ON NUM	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Frame on number
0x8029400E	FRAME OFF NUM	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Frame off number
0x80294013	IRQ HCNT LOW	0x00	RW	Bit[7:0]: Horizontal size count of Irq[7:0]
0x80294014	IRQ HCNT HIGH	0x00	RW	Bit[7]: Reserved Bit[6]: Interrupt mask 0: Unmask 1: Mask Bit[5:0]: Horizontal size count of Irq[13:8]
0x80294015	IRQ VCNT LOW	0x00	RW	Bit[7:0]: Vertical size count of Irq[7:0]
0x80294016	IRQ VCNT HIGH	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Vertical size count of Irq[12:8]

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table 4-8 CIF registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x80294017	EMB LINE	0x00	RW	Bit[7]: Embedded lines (pre) enable 1: Enable, output related embedded line timing 0: Disable Bit[6:4]: Embedded lines (pre) number Bit[3]: Embedded lines (post) enable 0: Disable 1: Enable, output related embedded line timing Bit[2:0]: Embedded lines (post) number

4.6 DVP control

base address: 0x80286000

table 4-9 DVP registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x80286000	DVP CTRL0	0x04	RW	Bit[7:4]: Reserved Bit[3]: ccir656_v_select This bit is used to select which package is the first package of one frame in CCIR656 mode start of active video package or end of active video package 0: Send SAV at the start of one frame in CCIR656 mode 1: Send EAV at the start of one frame in CCIR656 mode Bit[2]: ccir656_f_value This bit is used to indicate the current frame is odd field or even field in CCIR656 odd/even mode 0: Indicates this field is field 1 1: Indicates this field is field 2 Bit[1]: CCIR656 mode enable 0: Disable CCIR656 mode 1: Enable CCIR656 mode Bit[0]: HSYNC mode enable 0: Disable HSYNC mode 1: Enable HSYNC mode

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table 4-9 DVP registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x80286001	VSYNC WIDTH CNT0	0x00	RW	Bit[7:0]: VSYNC width line counter Width of VSYNC signal is defined by the sum of line based length and pixel based length. Line based length is set by VSYNC width cnt0.
0x80286002	VSYNC WIDTH CNT1	0x00	RW	Bit[7:0]: VSYNC width pixel count[15:8] Pixel based VSYNC width is set by VSYNC width cnt1 and VSYNC width cnt2
0x80286003	VSYNC WIDTH CNT2	0x10	RW	Bit[7:0]: VSYNC width pixel count[7:0] Pixel based VSYNC width is set by VSYNC width cnt1 and VSYNC width cnt2
0x80286004	DVP CTRL1	0x00	RW	Bit[7:4]: Reserved Bit[3:2]: VSYNC output select VSYNC output signal can be produced in the module or can be bypassed from the input signals 00: Generate VSYNC signal in the module 01: Bypass gpio_vsync_i to be VSYNC output signal 10: Bypass tc_hsync_i to be VSYNC output signal 11: Bypass eof_i to be VSYNC output signal Bit[1:0]: vsync_mod When generating the VSYNC signal, the VSYNC signal form can be selected 00: Mode 1, SOF signal trigger the VSYNC signal 01: Mode 2, EOF signal trigger the VSYNC signal 10: Mode 3, the end of the VSYNC signal will be determined by the relationship with the first_l_i signal 11: Not allowed
0x80286005	VSYNC DELAY CNT 2	0x00	RW	Bit[7:0]: EOF/SOF to VSYNC delay[23:16] Start position of the VSYNC signal can be determined by the VSYNC delay counter
0x80286006	VSYNC DELAY CNT 1	0x01	RW	Bit[7:0]: EOF/SOF to VSYNC delay[15:8] Start position of the VSYNC signal can be determined by the VSYNC delay counter

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table 4-9 DVP registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x80286007	VSYNC DELAY CNT 0	0x00	RW	Bit[7:0]: EOF/SOF to VSYNC delay[7:0] Start position of the VSYNC signal can be determined by the VSYNC delay counter
0x80286008	DVP CTRL2	0x01	RW	Bit[7]: Reserved Bit[6]: Output HSYNC polarity 0: Retain input polarity 1: Invert input polarity Bit[5:3]: Reserved Bit[2]: Output HREF polarity 0: Retain input polarity 1: Invert input polarity Bit[1]: Output VSYNC polarity 0: Retain selected output VSYNC signal polarity 1: Invert selected output VSYNC signal polarity Bit[0]: Output PCLK polarity 0: Retain input polarity 1: Invert input polarity

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table 4-9 DVP registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x80286009	DVP CTRL3	0x00	RW	Bit[7]: Reserved Bit[6:4]: Data bit swap Sequence of output bits can be arranged 0000: [11:0] 0001: [0:11] 0010: [2:11], [1:0] 0011: [4:11], [3:0] 0100: [9:0], [11:10] 0101: [7:0], [11:8] 0110: [10:0], [11] 0111: [1:11], [0] Bit[3]: Bit test mode In mode0, every data lasting one clock cycles In mode1, every data lasting two clock cycles 0: 0, 1, 2, 4, 8, 16... 1: 0, 0, 1, 1, 2, 2, 4, 4, 8, 8... Bit[2]: Bit test 10-bit mode Max test data is 1023 0: Disable 1: Enable Bit[1]: Bit test 8-bit mode Max test data is 255 0: Disable 1: Enable Bit[0]: Bit test enable Enable walking one test 0: Disable 1: Enable
0x8028600A	DVP CTRL4	0x00	RW	Bit[7:5]: Reserved Bit[4]: HREF input select Select source of HREF input signal 0: tc_hsync_i 1: gpo_href_i Bit[3:0]: Reserved

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4.7 UART control

4.7.1 UART0 control

base address: 0x80284000 UART0

table 4-10 UART0 control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x80284000	UART CTRL0	0x3C	RW	Bit[7:6]: Reserved Bit[5]: Transmit enable When this bit is set, system can start transmitting data through UART0 0: Disable UART transmit 1: Enable UART transmit Bit[4]: Receive enable When this bit is set, system can receive data through UART0 0: Disable UART receive 1: Enable UART receive Bit[3]: Transmit parity enable Enable transmitting parity check bit 0: Disable 1: Enable Bit[2]: Receive parity enable Enable receiving parity check bit 0: Disable 1: Enable Bit[1]: Clear receive Clear receiving FIFO 0: Do not clear receiving FIFO 1: Clear receiving FIFO Bit[0]: Clear transmit Clear transmitting FIFO 0: Do not clear transmitting FIFO 1: Clear transmitting FIFO
0x80284001	RX THRESHOLD	0x01	RW	Bit[7:4]: RX FIFO almost empty threshold Receiving FIFO almost empty counter Bit[3:0]: RX FIFO almost full threshold Receiving FIFO almost full counter
0x80284002	TX THRESHOLD	0x01	RW	Bit[7:4]: TX FIFO almost empty threshold Transmitting FIFO almost empty counter Bit[3:0]: TX FIFO almost full threshold Transmitting FIFO almost full counter

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table 4-10 UART0 control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x80284003	RX CLOCK DIVIDER0	0x1F	RW	Bit[7:0]: RX clock divider coefficients[7:0] (high byte in register 0x8028400A)
0x80284004	TX CLOCK DIVIDER0	0x1F	RW	Bit[7:0]: TX clock divider coefficients[7:0] (high byte in register 0x8028400B)
0x80284005	UART CTRL1	0x00	RW	Bit[7:6]: Receive parity select 00: Receiving parity bit is the one received from the host 01: Receiving parity bit is the one from the host and is inverted 10: Receiving parity bit is 1'b0 11: Receiving parity bit is 1'b1 Bit[5:4]: Transmit parity select 00: Transmitted parity bit is the calculated one 01: Transmitted parity bit is the calculated one and is inverted 10: Transmitted parity bit is 1'b1 11: Transmitted parity bit is 1'b0 Bit[3]: Transmit break enable Enable transmit break 0: Disable 1: Enable Bit[2]: Address match auto check Enable automatic address check 0: Disable 1: Enable Bit[1]: Transmit address bit enable When this bit is set, one bit address bit will be transmitted 0: Disable 1: Enable Bit[0]: Receive address bit enable When this bit is set, one bit address bit will be received 0: Disable 1: Enable
0x80284006	UART RECEIVING ADDRESS	0x01	RW	Bit[7:0]: UART receiving address Address of host
0x80284007	UART BROADCAST ADDRESS	0xFF	RW	Bit[7:0]: UART broadcast address Address to broadcast
0x80284008	DATA BIT WIDTH	0x3F	RW	Bit[7:6]: Reserved Bit[5:3]: Receive data bit width Bit number is from 5 to 8 Bit[2:0]: Transmit data bit width Bit number is from 5 to 8

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table 4-10 UART0 control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x80284009	STOP BIT WIDTH	0x00	RW	Bit[7:4]: Reserved Bit[3:2]: Receive stop bit width Bit[1:0]: Transmit data bit width
0x8028400A	RX CLOCK DIVIDER1	0x00	RW	Bit[7:0]: RX clock divider coefficients[15:8] (low byte in register 0x80284003)
0x8028400B	TX CLOCK DIVIDER1	0x00	RW	Bit[7:0]: TX clock divider coefficients[15:8] (low byte in register 0x80284004)
0x8028400C~ 0x8028400F	RSVD	–	–	Reserved
0x80284010	TRANSMIT DATA	0x00	RW	Bit[7:0]: Transmit data
0x80284011	UART CTRL2	0x00	RW	Bit[7:1]: Reserved Bit[0]: Transmit address bit
0x80284012~ 0x8028401F	RSVD	–	–	Reserved
0x80284020	RECEIVE DATA	–	R	Bit[7:0]: Receive data bits
0x80284021	UART STATUS0	–	R	Bit[7:4]: Reserved Bit[3]: Receive address bit or data bit 0: Receiving data bit 1: Receiving address bit Bit[2]: Receive break error Break error is when zero status lasts for more than one frame 0: There is no a break error in receiving part 1: There is a break error in receiving part Bit[1]: Receive parity error Parity error is when parity check fails 0: There is no parity check error in receiving part 1: There is a parity check error in receiving part Bit[0]: Receive frame error Frame error is when there is no valid frame end bit in one frame 0: There is no frame error in receiving part 1: There is a frame error in receiving part

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table 4-10 UART0 control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x80284022	UART STATUS1	–	R	Bit[7]: Receive FIFO not empty Bit[6]: Receive FIFO full Bit[5]: Receive FIFO almost full Bit[4]: Receive FIFO almost empty Bit[3]: Transmit FIFO not empty Bit[2]: Transmit FIFO full Bit[1]: Transmit FIFO almost full Bit[0]: Transmit FIFO almost empty
0x80284023~ 0x8028402F	RSVD	–	–	Reserved
0x80284030	ERROR INT EN	0x00	RW	Bit[7:3]: Reserved Bit[2]: Break error interrupt enable When this bit is set, break error interrupt is enabled 0: Disable 1: Enable Bit[1]: Parity error interrupt enable When this bit is set, parity error interrupt is enabled 0: Disable 1: Enable Bit[0]: Frame error interrupt enable When this bit is set, frame error interrupt is enabled 0: Disable 1: Enable

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table 4-10 UART0 control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x80284031	FIFO INT EN	0x00	RW	Bit[7]: Transmit FIFO not empty interrupt enable 0: Disable 1: Enable Bit[6]: Transmit FIFO full interrupt enable 0: Disable 1: Enable Bit[5]: Transmit FIFO almost full interrupt enable 0: Disable 1: Enable Bit[4]: Transmit FIFO almost empty interrupt enable 0: Disable 1: Enable Bit[3]: Receive FIFO not empty interrupt enable 0: Disable 1: Enable Bit[2]: Receive FIFO full interrupt enable 0: Disable 1: Enable Bit[1]: Receive FIFO almost full interrupt enable 0: Disable 1: Enable Bit[0]: Receive FIFO almost empty interrupt enable 0: Disable 1: Enable
0x80284032	ERROR INT CLEAR	0x00	RW	Bit[7:3]: Reserved Bit[2]: Break error interrupt status and clear Break error interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[1]: Parity error interrupt status and clear Parity error interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[0]: Frame error interrupt status and clear Frame error interrupt status can be read out and the interrupt will be cleared when this bit is written

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table 4-10 UART0 control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x80284033	FIFO INT CLEAR	0x00	RW	Bit[7]: Transmit FIFO not empty interrupt status and clear Transmit FIFO not empty interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[6]: Transmit FIFO full interrupt status and clear Transmit FIFO full interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[5]: Transmit FIFO almost full interrupt status and clear Transmit FIFO almost full interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[4]: Transmit FIFO almost empty interrupt status and clear Transmit FIFO almost empty interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[3]: Receive FIFO not empty interrupt status and clear Receive FIFO not empty interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[2]: Receive FIFO full interrupt status and clear Receive FIFO full interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[1]: Receive FIFO almost full interrupt status and clear Receive FIFO almost full interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[0]: Receive FIFO almost empty interrupt status and clear Receive FIFO almost empty interrupt status can be read out and the interrupt will be cleared when this bit is written

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4.7.2 UART1 control

base address: 0x802A0000 UART1

table 4-11 UART1 control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x802A0000	UART CTRL0	0x3C	RW	Bit[7:6]: Reserved Bit[5]: Transmit enable When this bit is set, system can start transmit data though UART1 0: Disable UART transmit 1: Enable UART transmit Bit[4]: Receive enable When this bit is set, system can receive data though UART1 0: Disable UART receive 1: Enable UART receive Bit[3]: Transmit parity enable Enable transmitting parity check 0: Disable 1: Enable Bit[2]: Receive parity enable Enable receiving parity check bit 0: Disable 1: Enable Bit[1]: Clear receive Clear receiving FIFO 0: Do not clear receiving FIFO 1: Clear receiving FIFO Bit[0]: Clear transmit Clear transmitting FIFO 0: Do not clear transmitting FIFO 1: Clear transmitting FIFO
0x802A0001	RX THRESHOLD	0x1F	RW	Bit[7:4]: RX FIFO almost empty threshold Receiving FIFO almost empty counter Bit[3:0]: RX FIFO almost full threshold Receiving FIFO almost full counter
0x802A0002	TX THRESHOLD	0x1F	RW	Bit[7:4]: TX FIFO almost empty threshold Transmitting FIFO almost empty counter Bit[3:0]: TX FIFO almost full threshold Transmitting FIFO almost full counter
0x802A0003	RX CLOCK DIVIDER0	0x0F	RW	Bit[7:0]: RX clock divider coefficients[7:0] (high byte in register 0x802A000A)

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table 4-11 UART1 control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x802A0004	TX CLOCK DIVIDER0	0x0F	RW	Bit[7:0]: TX clock divider coefficients[7:0] (high byte in register 0x802A000B)
0x802A0005	UART CTRL1	0x00	RW	Bit[7:6]: Receive parity select 00: Receiving parity bit is the one received from the host 01: Receiving parity bit is the one received from the host and is inverted 10: Receiving parity bit is 1'b0 11: Receiving parity bit is 1'b1 Bit[5:4]: Transmit parity select 00: Transmitted parity bit is the calculated one 01: Transmitted parity bit is the calculated one and is inverted 10: Transmitted parity bit is 1'b1 11: Transmitted parity bit is 1'b0 Bit[3]: Transmit break enable Enable transmit break 0: Disable 1: Enable Bit[2]: Address match auto check Enable automatic address check 0: Disable 1: Enable Bit[1]: Transmit address bit enable When this bit is set, one bit address bit will be transmitted 0: Disable 1: Enable Bit[0]: Receive address bit enable When this bit is set, one bit address bit will be received 0: Disable 1: Enable
0x802A0006	UART RECEIVING ADDRESS	0x01	RW	Bit[7:0]: UART receiving address Address of host
0x802A0007	UART BROADCAST ADDRESS	0xFF	RW	Bit[7:0]: UART broadcast address Address to broadcast
0x802A0008	DATA BIT WIDTH	0x3F	RW	Bit[7:6]: Reserved Bit[5:3]: Receive data bit width Bit number is from 5 to 8 Bit[2:0]: Transmit data bit width Bit number is from 5 to 8

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table 4-11 UART1 control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x802A0009	STOP BIT WIDTH	0x00	RW	Bit[7:4]: Reserved Bit[3:2]: Receive stop bit width Bit[1:0]: Transmit stop bit width (low byte in register 0x802A0003)
0x802A000A	RX CLOCK DIVIDER1	0x00	RW	Bit[7:0]: RX clock divider coefficients[15:8] (low byte in register 0x802A0004)
0x802A000B	TX CLOCK DIVIDER1	0x00	RW	Bit[7:0]: TX clock divider coefficients[15:8]
0x802A000C~ 0x802A000F	RSVD	–	–	Reserved
0x802A0010	TRANSMIT DATA	0x00	RW	Bit[7:0]: Transmit data bits
0x802A0011	UART CTRL2	0x00	RW	Bit[7:1]: Reserved Bit[0]: Transmit address bit
0x802A0012~ 0x802A001F	RSVD	–	–	Reserved
0x802A0020	RECEIVE DATA	–	R	Bit[7:0]: Receive data bits
0x802A0021	UART STATUS0	–	R	Bit[7:4]: Reserved Bit[3]: Receive address bit or data bit 0: Receiving data bit 1: Receiving address bit Bit[2]: Receive break error Break error is when zero status lasts for more than one frame 0: There is no break error in receiving part 1: There is a break error in receiving part Bit[1]: Receive parity error Parity error is when parity check fails 0: There is no parity check error in receiving part 1: There is a parity check error in receiving part Bit[0]: Receive frame error Frame error is when there is no valid frame end bit in one frame 0: There is no frame error in receiving part 1: There is a frame error in receiving part

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table 4-11 UART1 control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x802A0022	UART STATUS1	–	R	Bit[7]: Receive FIFO not empty Bit[6]: Receive FIFO full Bit[5]: Receive FIFO almost full Bit[4]: Receive FIFO almost empty Bit[3]: Transmit FIFO not empty Bit[2]: Transmit FIFO full Bit[1]: Transmit FIFO almost full Bit[0]: Transmit FIFO almost empty
0x802A0023~ 0x802A002F	RSVD	–	–	Reserved
0x802A0030	ERROR INT EN	0x00	RW	Bit[7:3]: Reserved Bit[2]: Break error interrupt enable When this bit is set, break error interrupt is enabled 0: Disable 1: Enable Bit[1]: Parity error interrupt enable When this bit is set, parity error interrupt is enabled 0: Disable 1: Enable Bit[0]: Frame error interrupt enable When this bit is set, frame error interrupt is enabled 0: Disable 1: Enable

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table 4-11 UART1 control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x802A0031	FIFO INT EN	0x00	RW	Bit[7]: Transmit FIFO not empty interrupt enable 0: Disable 1: Enable Bit[6]: Transmit FIFO full interrupt enable 0: Disable 1: Enable Bit[5]: Transmit FIFO almost full interrupt enable 0: Disable 1: Enable Bit[4]: Transmit FIFO almost empty interrupt enable 0: Disable 1: Enable Bit[3]: Receive FIFO not empty interrupt enable 0: Disable 1: Enable Bit[2]: Receive FIFO full interrupt enable 0: Disable 1: Enable Bit[1]: Receive FIFO almost full interrupt enable 0: Disable 1: Enable Bit[0]: Receive FIFO almost empty interrupt enable 0: Disable 1: Enable
0x802A0032	ERROR INT CLEAR	0x00	RW	Bit[7:3]: Reserved Bit[2]: Break error interrupt status and clear Break error interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[1]: Parity error interrupt status and clear Parity error interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[0]: Frame error interrupt status and clear Frame error interrupt status can be read out and the interrupt will be cleared when this bit is written

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table 4-11 UART1 control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x802A0033	FIFO INT CLEAR	0x00	RW	Bit[7]: Transmit FIFO not empty interrupt status and clear Transmit FIFO not empty interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[6]: Transmit FIFO full interrupt status and clear Transmit FIFO full interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[5]: Transmit FIFO almost full interrupt status and clear Transmit FIFO almost full interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[4]: Transmit FIFO almost empty interrupt status and clear Transmit FIFO almost empty interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[3]: Receive FIFO not empty interrupt status and clear Receive FIFO not empty interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[2]: Receive FIFO full interrupt status and clear Receive FIFO full interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[1]: Receive FIFO almost full interrupt status and clear Receive FIFO almost full interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[0]: Receive FIFO almost empty interrupt status and clear Receive FIFO almost empty interrupt status can be read out and the interrupt will be cleared when this bit is written

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4.7.3 UART2 control

base address: 0x802A2000 UART2

table 4-12 UART2 control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x802A2000	UART CTRL0	0x3C	RW	Bit[7:6]: Reserved Bit[5]: Transmit enable When this bit is set, system can start transmit data through UART2 0: Disable UART transmit 1: Enable UART transmit Bit[4]: Receive enable When this bit is set, system can receive data through UART2 0: Disable UART receive 1: Enable UART receive Bit[3]: Transmit parity enable Enable transmitting parity check 0: Disable 1: Enable Bit[2]: Receive parity enable Enable receiving parity check bit 0: Disable 1: Enable Bit[1]: Clear receive Clear receiving FIFO 0: Do not clear receiving FIFO 1: Clear receiving FIFO [0]: Clear transmit Clear transmitting FIFO 0: Do not clear transmitting FIFO 1: Clear transmitting FIFO
0x802A2001	RX THRESHOLD	0x1F	RW	Bit[7:4]: RX FIFO almost empty threshold Receiving FIFO almost empty counter Bit[3:0]: RX FIFO almost full threshold Receiving FIFO almost full counter.
0x802A2002	TX THRESHOLD	0x1F	RW	Bit[7:4]: TX FIFO almost empty threshold Transmitting FIFO almost empty counter Bit[3:0]: TX FIFO almost full threshold Transmitting FIFO almost full counter
0x802A2003	RX CLOCK DIVIDER0	0x0F	RW	Bit[7:0]: RX clock divider coefficients[7:0] (high byte in register 0x802A000A)

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table 4-12 UART2 control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x802A2004	TX CLOCK DIVIDER0	0x0F	RW	Bit[7:0]: TX clock divider coefficients[7:0] (high byte in register 0x802A000B)
0x802A2005	UART CTRL1	0x00	RW	Bit[7:6]: Receive parity select 00: Receiving parity bit is the one received from the host 01: Receiving parity bit is the one received from the host and is inverted 10: Receiving parity bit is 1'b0 11: Receiving parity bit is 1'b1 Bit[5:4]: Transmit parity select 00: Transmitted parity bit is the calculated one 01: Transmitted parity bit is the calculated one and is inverted 10: Transmitted parity bit is 1'b1 11: Transmitted parity bit is 1'b0 Bit[3]: Transmit break enable Enable transmit break 0: Disable 1: Enable Bit[2]: Address match auto check Enable automatic address check 0: Disable 1: Enable Bit[1]: Transmit address bit enable When this bit is set, one bit address bit will be transmitted 0: Disable 1: Enable Bit[0]: Receive address bit enable When this bit is set, one bit address bit will be received 0: Disable 1: Enable
0x802A2006	UART RECEIVING ADDRESS	0x01	RW	Bit[7:0]: UART receiving address Address of host
0x802A2007	UART BROADCAST ADDRESS	0xFF	RW	Bit[7:0]: UART broadcast address Address to broadcast
0x802A2008	DATA BIT WIDTH	0x3F	RW	Bit[7:6]: Reserved Bit[5:3]: Receive data bit width Bit number is from 5 to 8 Bit[2:0]: Transmit data bit width Bit number is from 5 to 8

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table 4-12 UART2 control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x802A2009	STOP BIT WIDTH	0x00	RW	Bit[7:4]: Reserved Bit[3:2]: Receive stop bit width Bit[1:0]: Transmit stop bit width
0x802A200A	RX CLOCK DIVIDER1	0x00	RW	Bit[7:0]: RX clock divider coefficients[15:8] (low byte in register 0x802A0003)
0x802A200B	TX CLOCK DIVIDER1	0x00	RW	Bit[7:0]: TX clock divider coefficients[15:8] (low byte in register 0x802A0004)
0x802A200C~ 0x802A200F	RSVD	–	–	Reserved
0x802A2010	TRANSMIT DATA	0x00	RW	Bit[7:0]: Transmit data bits
0x802A2011	UART CTRL2	0x00	RW	Bit[7:1]: Reserved Bit[0]: Transmit address bit
0x802A2012~ 0x802A201F	RSVD	–	–	Reserved
0x802A2020	RECEIVE DATA	–	R	Bit[7:0]: Receive data bits
0x802A2021	UART STATUS0	–	R	Bit[7:4]: Reserved Bit[3]: Receive address bit or data bit 0: Receiving data bit 1: Receiving address bit Bit[2]: Receive break error Break error is when zero status lasts for more than one frame 0: There is no break error in receiving part 1: There is a break error in receiving part Bit[1]: Receive parity error Parity error is when parity check fails 0: There is no parity check error in receiving part 1: There is a parity check error in receiving part Bit[0]: Receive frame error Frame error is when there is no valid frame end bit in one frame 0: There is no frame error in receiving part 1: There is a frame error in receiving part

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table 4-12 UART2 control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x802A2022	UART STATUS1	–	R	Bit[7]: Receive FIFO not empty Bit[6]: Receive FIFO full Bit[5]: Receive FIFO almost full Bit[4]: Receive FIFO almost empty Bit[3]: Transmit FIFO not empty Bit[2]: Transmit FIFO full Bit[1]: Transmit FIFO almost full Bit[0]: Transmit FIFO almost empty
0x802A2023~ 0x802A202F	RSVD	–	–	Reserved
0x802A2030	ERROR INT EN	0x00	RW	Bit[7:3]: Reserved Bit[2]: Break error interrupt enable When this bit is set, break error interrupt is enabled 0: Disable 1: Enable Bit[1]: Parity error interrupt enable When this bit is set, parity error interrupt is enabled 0: Disable 1: Enable [0]: Frame error interrupt enable When this bit is set, frame error interrupt is enabled 0: Disable 1: Enable

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table 4-12 UART2 control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x802A2031	FIFO INT EN	0x00	RW	Bit[7]: Transmit FIFO not empty interrupt enable 0: Disable 1: Enable Bit[6]: Transmit FIFO full interrupt enable 0: Disable 1: Enable Bit[5]: Transmit FIFO almost full interrupt enable 0: Disable 1: Enable Bit[4]: Transmit FIFO almost empty interrupt enable 0: Disable 1: Enable Bit[3]: Receive FIFO not empty interrupt enable 0: Disable 1: Enable Bit[2]: Receive FIFO full interrupt enable 0: Disable 1: Enable Bit[1]: Receive FIFO almost full interrupt enable 0: Disable 1: Enable Bit[0]: Receive FIFO almost empty interrupt enable 0: Disable 1: Enable
0x802A2032	ERROR INT CLEAR	0x00	RW	Bit[7:3]: Reserved Bit[2]: Break error interrupt status and clear Break error interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[1]: Parity error interrupt status and clear Parity error interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[0]: Frame error interrupt status and clear Frame error interrupt status can be read out and the interrupt will be cleared when this bit is written

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table 4-12 UART2 control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x802A2033	FIFO INT CLEAR	0x00	RW	Bit[7]: Transmit FIFO not empty interrupt status and clear Transmit FIFO not empty interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[6]: Transmit FIFO full interrupt status and clear Transmit FIFO full interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[5]: Transmit FIFO almost full interrupt status and clear Transmit FIFO almost full interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[4]: Transmit FIFO almost empty interrupt status and clear Transmit FIFO almost empty interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[3]: Receive FIFO not empty interrupt status and clear Receive FIFO not empty interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[2]: Receive FIFO full interrupt status and clear Receive FIFO full interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[1]: Receive FIFO almost full interrupt status and clear Receive FIFO almost full interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[0]: Receive FIFO almost empty interrupt status and clear Receive FIFO almost empty interrupt status can be read out and the interrupt will be cleared when this bit is written

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4.7.4 UART3 control

base address: 0x802A4000 UART3

table 4-13 UART3 control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x802A4000	UART CTRL0	0x3C	RW	Bit[7:6]: Reserved Bit[5]: Transmit enable When this bit is set, system can start transmit data through UART3 0: Disable UART transmit 1: Enable UART transmit Bit[4]: Receive enable When this bit is set, system can receive data through UART3 0: Disable UART receive 1: Enable UART receive Bit[3]: Transmit parity enable Enable transmitting parity check 0: Disable 1: Enable Bit[2]: Receive parity enable Enable receiving parity check bit 0: Disable 1: Enable Bit[1]: Clear receive Clear receiving FIFO 0: Do not clear receiving FIFO 1: Clear receiving FIFO Bit[0]: Clear transmit Clear transmitting FIFO 0: Do not clear transmitting FIFO 1: Clear transmitting FIFO
0x802A4001	RX THRESHOLD	0x1F	RW	Bit[7:4]: RX FIFO almost empty threshold Receiving FIFO almost empty counter Bit[3:0]: RX FIFO almost full threshold Receiving FIFO almost full counter
0x802A4002	TX THRESHOLD	0x1F	RW	Bit[7:4]: TX FIFO almost empty threshold Transmitting FIFO almost empty counter Bit[3:0]: TX FIFO almost full threshold Transmitting FIFO almost full counter
0x802A4003	RX CLOCK DIVIDER0	0x0F	RW	Bit[7:0]: RX clock divider coefficients[7:0] (high byte in register 0x802A400A)

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table 4-13 UART3 control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x802A4004	TX CLOCK DIVIDER0	0x0F	RW	Bit[7:0]: TX clock divider coefficients[7:0] (high byte in register 0x802A400B)
0x802A4005	UART CTRL1	0x00	RW	Bit[7:6]: Receive parity select 00: Receiving parity bit is the one received one from the host 01: Receiving parity bit is the one received from the host and is inverted 10: Receiving parity bit is 1'b0 11: Receiving parity bit is 1'b1 Bit[5:4]: Transmit parity select 00: Transmitted parity bit is the calculated one 01: Transmitted parity bit is the calculated one and is inverted 10: Transmitted parity bit is 1'b1 11: Transmitted parity bit is 1'b0 Bit[3]: Transmit break enable Enable transmit break 0: Disable 1: Enable Bit[2]: Address match auto check Enable automatic address check 0: Disable 1: Enable Bit[1]: Transmit address bit enable When this bit is set, one bit address bit will be transmitted 0: Disable 1: Enable Bit[0]: Receive address bit enable When this bit is set, one bit address bit will be received 0: Disable 1: Enable
0x802A4006	UART RECEIVING ADDRESS	0x01	RW	Bit[7:0]: UART receiving address Address of host
0x802A4007	UART BROADCAST ADDRESS	0xFF	RW	Bit[7:0]: UART broadcast address Address to broadcast
0x802A4008	DATA BIT WIDTH	0x3F	RW	Bit[7:6]: Reserved Bit[5:3]: Receive data bit width Bit number is from 5 to 8 Bit[2:0]: Transmit data bit width Bit number is from 5 to 8

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table 4-13 UART3 control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x802A4009	STOP BIT WIDTH	0x00	RW	Bit[7:4]: Reserved Bit[3:2]: Receive stop bit width Bit[1:0]: Transmit stop bit width
0x802A400A	RX CLOCK DIVIDER1	0x00	RW	Bit[7:0]: RX clock divider coefficients[15:8] (low byte in register 0x802A4003)
0x802A400B	TX CLOCK DIVIDER1	0x00	RW	Bit[7:0]: TX clock divider coefficients[7:0] (low byte in register 0x802A4004)
0x802A400C~ 0x802A400F	RSVD	–	–	Reserved
0x802A4010	TRANSMIT DATA	0x00	RW	Bit[7:0]: Transmit data bits
0x802A4011	UART CTRL2	0x00	RW	Bit[7:1]: Reserved Bit[0]: Transmit address bit
0x802A4012~ 0x802A401F	RSVD	–	–	Reserved
0x802A4020	RECEIVE DATA	–	R	Bit[7:0]: Receive data bits
0x802A4021	UART STATUS0	–	R	Bit[7:4]: Reserved Bit[3]: Receive address bit or data bit 0: Receiving data bit 1: Receiving address bit Bit[2]: Receive break error Break error is when zero status lasts for more than one frame 0: There is no break error in receiving part 1: There is a break error in receiving part Bit[1]: Receive parity error Parity error is when parity check fails 0: There is no parity check error in receiving part 1: There is a parity check error in receiving part Bit[0]: Receive frame error Frame error is when there is no valid end bit in one frame 0: There is no frame error in receiving part 1: There is a frame error in receiving part

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table 4-13 UART3 control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x802A4022	UART STATUS1	–	R	Bit[7]: Receive FIFO not empty Bit[6]: Receive FIFO full Bit[5]: Receive FIFO almost full Bit[4]: Receive FIFO almost empty Bit[3]: Transmit FIFO not empty Bit[2]: Transmit FIFO full Bit[1]: Transmit FIFO almost full Bit[0]: Transmit FIFO almost empty
0x802A4023~ 0x802A402F	RSVD	–	–	Reserved
0x802A4030	ERROR INT EN	0x00	RW	Bit[7:3]: Reserved Bit[2]: Break error interrupt enable When this bit is set, break error interrupt is enabled 0: Disable 1: Enable Bit[1]: Parity error interrupt enable When this bit is set, parity error interrupt is enabled 0: Disable 1: Enable Bit[0]: Frame error interrupt enable When this bit is set, frame error interrupt is enabled 0: Disable 1: Enable

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table 4-13 UART3 control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x802A4031	FIFO INT EN	0x00	RW	Bit[7]: Transmit FIFO not empty interrupt enable 0: Disable 1: Enable Bit[6]: Transmit FIFO full interrupt enable 0: Disable 1: Enable Bit[5]: Transmit FIFO almost full interrupt enable 0: Disable 1: Enable Bit[4]: Transmit FIFO almost empty interrupt enable 0: Disable 1: Enable Bit[3]: Receive FIFO not empty interrupt enable 0: Disable 1: Enable Bit[2]: Receive FIFO full interrupt enable 0: Disable 1: Enable Bit[1]: Receive FIFO almost full interrupt enable 0: Disable 1: Enable Bit[0]: Receive FIFO almost empty interrupt enable 0: Disable 1: Enable
0x802A4032	ERROR INT CLEAR	0x00	RW	Bit[7:3]: Reserved Bit[2]: Break error interrupt status and clear Break error interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[1]: Parity error interrupt status and clear Parity error interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[0]: Frame error interrupt status and clear Frame error interrupt status can be read out and the interrupt will be cleared when this bit is written

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table 4-13 UART3 control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x802A4033	FIFO INT CLEAR	0x00	RW	BIt[7]: Transmit FIFO not empty interrupt status and clear Transmit FIFO not empty interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[6]: Transmit FIFO full interrupt status and clear Transmit FIFO full interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[5]: Transmit FIFO almost full interrupt status and clear Transmit FIFO almost full interrupt status can be read out and the interrupt will be cleared when this bit is written BIt[4]: Transmit FIFO almost empty interrupt status and clear Transmit FIFO almost empty interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[3]: Receive FIFO not empty interrupt status and clear Receive FIFO not empty interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[2]: Receive FIFO full interrupt status and clear Receive FIFO full interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[1]: Receive FIFO almost full interrupt status and clear Receive FIFO almost full interrupt status can be read out and the interrupt will be cleared when this bit is written Bit[0]: Receive FIFO almost empty interrupt status and clear Receive FIFO almost empty interrupt status can be read out and the interrupt will be cleared when this bit is written

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4.8 MIPI RX control

4.8.1 MIPI RX0 control

base address: 0x80290000 MIPI_RX0_BASE

table 4-14 MIPI RX0 registers (sheet 1 of 12)

address	register name	default value	R/W	description
0x80290000	MIPI RX CTRL0	0x20	RW	Bit[7]: Four lane select When this bit is set, four lane input mode will be enabled 0: Four lane input mode disable 1: Four lane input mode enable Bit[6]: Bypass ECC 0: Enable ECC check function 1: Bypass ECC check function Bit[5]: Two lane select When this bit is set, two lane input mode will be enabled 0: Two lane input mode disable 1: Two lane input mode enable Bit[4]: Packet header bit order 0: Retain receiving header data in sequence 1: Reverse receiving header data in sequence Bit[3:2]: Packet header byte order 00: {byte_id, byte_number[7:0], byte_number[15:8]} 01: {byte_id, byte_number} 10: {byte_number[7:0], byte_number[15:8], byte_id} 11: {byte_number, byte id} Bit[1]: HREF select for virtual channel1 0: HREF signal of virtual channel 1 generated by aligning valid data package 1: HREF signal of virtual channel 1 generated by line start and Line end packages Bit[0]: HREF select for virtual channel0 0: HREF signal of virtual channel 0 generated by aligning valid data package 1: HREF signal of virtual channel 0 generated by line start and Line end packages
0x80290001	START SIZE V0	0x04	RW	Bit[7:0]: Read FIFO start size for virtual channel0

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table 4-14 MIPI RX0 registers (sheet 2 of 12)

address	register name	default value	R/W	description
0x80290002	MIPI RX CTRL1	0x80	RW	Bit[7]: SOT 1 bit wrong match enable Bit[6]: Data type select for virtual channel0 0: Data type of virtual channel 0 set by receiving data 1: Data type of virtual channel 0 set by register Bit[5:0]: Data type set by registers for virtual channel0
0x80290003	VSYNC COUNTER1 V0	0x04	RW	Bit[7:0]: Counter for asserting VSYNC signal after frame end packet in virtual channel0
0x80290004	VSYNC COUNTER2 V0	0x04	RW	Bit[7:0]: Counter for de-asserting VSYNC signal after frame start packet in virtual channel0
0x80290005	START SIZE V1	0x04	RW	Bit[7:0]: Read FIFO start size for virtual channel1
0x80290006	MIPI RX CTRL2	0x00	RW	Bit[7]: Reserved Bit[6]: Data type select for virtual channel1 0: Data type of virtual channel 1 set by receiving data 1: Data type of virtual channel 1 set by register Bit[5:0]: Data type set by registers for virtual channel1
0x80290007	VSYNC COUNTER1 V1	0x04	RW	Bit[7:0]: Counter for asserting VSYNC signal after frame end packet in virtual channel1
0x80290008	VSYNC COUNTER2 V1	0x04	RW	Bit[7:0]: Counter for de-asserting VSYNC signal after frame start packet in virtual channel1
0x80290009	VIRTUAL CHANNEL NUMBER	0x04	RW	Bit[7:4]: Reserved Bit[3:2]: Virtual channel1 number Bit[1:0]: Virtual channel0 number
0x8029000A~ 0x8029000F	RSVD	–	–	Reserved

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table 4-14 MIPI RX0 registers (sheet 3 of 12)

address	register name	default value	R/W	description
0x80290010	MIPI RX CTRL3	0x0F	RW	Bit[7:6]: Reserved Bit[5]: Disable VSYNC control for HREF and valid in virtual channel1 0: Do not disable VSYNC control in virtual channel1 1: Disable VSYNC control in virtual channel1 Bit[4]: Disable VSYNC control for HREF and valid in virtual channel0 0: Do not disable VSYNC control in virtual channel0 1: Disable VSYNC control in virtual channel0 Bit[3]: Enable VSYNC positive edge reset in virtual channel1 asynchronous FIFO 0: Disable VSYNC positive edge reset in virtual channel1 1: Enable VSYNC positive edge reset in virtual channel1 Bit[2]: Enable VSYNC negative edge reset in virtual channel1 asynchronous FIFO 0: Disable VSYNC negative edge reset in virtual channel1 1: Enable VSYNC negative edge reset in virtual channel1 Bit[1]: Enable VSYNC positive edge reset in virtual channel0 asynchronous FIFO 0: Disable VSYNC positive edge reset in virtual channel0 1: Enable VSYNC positive edge reset in virtual channel0 Bit[0]: Enable VSYNC negative edge reset in virtual channel0 asynchronous FIFO 0: Disable VSYNC negative edge reset in virtual channel0 1: Enable VSYNC negative edge reset in virtual channel0

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table 4-14 MIPI RX0 registers (sheet 4 of 12)

address	register name	default value	R/W	description
0x80290011	LANE SWAP	0xE4	RW	Bit[7:6]: Lane swap control for lane 3 00: Lane3 at the position 0 01: Lane3 at the position 1 10: Lane3 at the position 2 11: Lane3 at the position 3 Bit[5:4]: Lane swap control for lane 2 00: Lane2 at the position 0 01: Lane2 at the position 1 10: Lane2 at the position 2 11: Lane2 at the position 3 Bit[3:2]: Lane swap control for lane 1 00: Lane1 at the position 0 01: Lane1 at the position 1 10: Lane1 at the position 2 11: Lane1 at the position 3 Bit[1:0]: Lane swap control for lane 0 00: Lane0 at the position 0 01: Lane0 at the position 1 10: Lane0 at the position 2 11: Lane0 at the position 3

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table 4-14 MIPI RX0 registers (sheet 5 of 12)

address	register name	default value	R/W	description
0x80290012	OUTPUT CONTROL	0x00	RW	Bit[7:6]: Reserved Bit[5]: Output swap control for virtual channel 1 Reverse the output data byte order of virtual channel 1 Bit[4]: Output swap control for virtual channel 0 Reverse the output data byte order of virtual channel 0 Bit[3]: Four word output control for virtual channel1 0: Disable four word output mode for virtual channel1 1: Enable four word output mode for virtual channel1 Bit[2]: Four word output control for virtual channel0 0: Disable four word output mode for virtual channel0 1: Enable four word output mode for virtual channel0 Bit[1]: Two word output control for virtual channel1 0: Disable two word output mode for virtual channel1 1: Enable two word output mode for virtual channel1 Bit[0]: Two word output control for virtual channel0 0: Disable two word output mode for virtual channel0 1: Enable two word output mode for virtual channel0
0x80290013	SHIFT CONTROL	0x00	RW	Bit[7:4]: Reserved Bit[3]: Shift 4 bits for virtual channel 1 Right shift output data 4 bits in virtual channel1 Bit[2]: Shift 4 bits for virtual channel 0 Right shift output data 4 bits in virtual channe0 Bit[1]: Shift 2 bits for virtual channel 1 Right shift output data 2 bits in virtual channel1 Bit[0]: Shift 2 bits for virtual channel 0 Right shift output data 2 bits in virtual channel0
0x80290014~ 0x8029001F	RSVD	–	–	Reserved

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table 4-14 MIPI RX0 registers (sheet 6 of 12)

address	register name	default value	R/W	description
0x80290020	PRBS CONTROL	0x00	RW	Bit[7:3]: Reserved Bit[2]: PRBS error clear 0: Do not clear PRBS error 1: Clear PRBS error Bit[1]: PRBS in select 0: PRBS input is not valid 1: PRBS input is valid Bit[0]: PRBS enable 0: Disable PRBS 1: Enable PRBS
0x80290021	CLEAR ERROR STATUS0	0x00	RW	Bit[7]: SOT error more than 1 bit in lane1 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[6]: SOT error more than 1 bit in lane0 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[5]: One bit error in SOT of lane 1 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[4]: One bit error in SOT of lane 0 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[3]: Receiving byte number not match interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[2]: CRC check error interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[1]: ECC error more than 1 bit interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[0]: ECC single bit error interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt

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table 4-14 MIPI RX0 registers (sheet 7 of 12)

address	register name	default value	R/W	description
0x80290022	CLEAR ERROR STATUS1	0x00	RW	Bit[7]: Receiving FIFO for virtual channel 1 empty interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[6]: Receiving FIFO for virtual channel 0 empty interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[5]: PRBS error in lane0 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[4]: PRBS error in lane1 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[3]: Receiving FIFO for virtual channel 1 overflow interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[2]: Receiving FIFO for virtual channel 1 full interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[1]: Receiving FIFO for virtual channel 0 overflow interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[0]: Receiving FIFO for virtual channel 0 full interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt
0x80290023	PRBS TEST COUNTER0	0x00	RW	Bit[7:0]: PRBS test counter[7:0]
0x80290024	PRBS TEST COUNTER1	0x00	RW	Bit[7:0]: PRBS test counter[15:8]
0x80290025	PRBS TEST COUNTER2	0x40	RW	Bit[7:0]: PRBS test counter[23:16]
0x80290026	PRBS ERROR COUNTER	0x10	RW	Bit[7:0]: PRBS error counter

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table 4-14 MIPI RX0 registers (sheet 8 of 12)

address	register name	default value	R/W	description
0x80290027	ERROR INTERRUPT ENABLE0	0x00	RW	Bit[7]: SOT error more than 1 bit in lane1 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[6]: SOT error more than 1 bit in lane0 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[5]: One bit error in SOT of lane 1 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[4]: One bit error in SOT of lane 0 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[3]: Receiving byte number not match interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[2]: CRC check error interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[1]: ECC error more than 1 bit interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[0]: ECC single bit error interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt

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table 4-14 MIPI RX0 registers (sheet 9 of 12)

address	register name	default value	R/W	description
0x80290028	ERROR INTERRUPT ENABLE1	0x00	RW	Bit[7]: Receiving FIFO for virtual channel 1 empty interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[6]: Receiving FIFO for virtual channel 0 empty interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[5]: PRBS error in lane0 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[4]: PRBS error in lane1 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[3]: Receiving FIFO for virtual channel 1 overflow interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[2]: Receiving FIFO for virtual channel 1 full interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[1]: Receiving FIFO for virtual channel 0 overflow interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[0]: Receiving FIFO for virtual channel 0 full interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt

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table 4-14 MIPI RX0 registers (sheet 10 of 12)

address	register name	default value	R/W	description
0x80290029	CLEAR ERROR STATUS2	0x00	RW	Bit[7:6]: Reserved Bit[5]: SOT error more than 1 bit in lane3 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[4]: SOT error more than 1 bit in lane2 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[3]: One bit error in SOT of lane 3 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[2]: One bit error in SOT of lane 2 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[1:0]: Reserved
0x8029002A	ERROR INTERRUPT ENABLE2	0x00	RW	Bit[7:6]: Reserved Bit[5]: SOT error more than 1 bit in lane3 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[4]: SOT error more than 1 bit in lane2 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[3]: One bit error in SOT of lane 3 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[2]: One bit error in SOT of lane 2 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[1:0]: Reserved
0x8029002B	CLEAR ERROR STATUS3	0x00	RW	Bit[7:2]: Reserved Bit[1]: PRBS error in lane2 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[0]: PRBS error in lane3 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt

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table 4-14 MIPI RX0 registers (sheet 11 of 12)

address	register name	default value	R/W	description
0x8029002C	MIPI RX CTRL4	0x48	RW	BIt[7:2]: Embedded ID for virtual channel 1 Embedded ID is used to identify the embedded line data Bit[1]: PRBS error in lane2 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[0]: PRBS error in lane3 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt
0x8029002D	EMBED LINE CTRL0	0x12	RW	Bit[7]: Channel 0 embedded line enable 0: Disable channel 0 embedded line 1: Enable channel 0 embedded line Bit[6]: Channel 1 embedded line enable 0: Disable channel 1 embedded line 1: Enable channel 1 embedded line Bit[5:0]: Embedded ID for virtual channel 0 Embedded ID is used to identify embedded line data
0x8029002E	EMBED LINE CTRL1	0x2C	RW	Bit[7:6]: Reserved Bit[5:0]: Embedded data type of channel 0 Embedded data type is used to decode the correct data from long package
0x8029002F	EMBED LINE CTRL2	0x2C	RW	Bit[7:6]: Reserved BIt[5:0]: Embedded data type of channel 1 Embedded data type is used to decode the correct data from long package
0x80290030	ERROR STATUS0	–	R	Bit[7]: SOT error more than 1 bit in lane1 Bit[6]: SOT error more than 1 bit in lane0 Bit[5]: One bit error in SOT of lane 1 Bit[4]: One bit error in SOT of lane 0 Bit[3]: Receiving byte number not match Bit[2]: CRC check error Bit[1]: ECC error more than 1 bit Bit[0]: ECC single bit error
0x80290031	ERROR STATUS1	–	R	Bit[7]: Receiving FIFO for virtual channel 1 empty Bit[6]: Receiving FIFO for virtual channel 0 empty Bit[5]: PRBS error in lane0 Bit[4]: PRBS error in lane1 Bit[3]: Receiving FIFO for virtual channel 1 overflow Bit[2]: Receiving FIFO for virtual channel 1 full Bit[1]: Receiving FIFO for virtual channel 0 overflow Bit[0]: Receiving FIFO for virtual channel 0 full

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table 4-14 MIPI RX0 registers (sheet 12 of 12)

address	register name	default value	R/W	description
0x80290032	ERROR STATUS2	–	R	Bit[7:6]: Reserved Bit[5]: SOT error more than 1 bit in lane3 Bit[4]: SOT error more than 1 bit in lane2 Bit[3]: One bit error in SOT of lane 3 Bit[2]: One bit error in SOT of lane 2 Bit[1:0]: Reserved
0x80290033	PRBS STATUS	–	R	Bit[7]: PRBS fail in lane0 Bit[6]: PRBS fail in lane1 Bit[5]: PRBS fail in lane2 Bit[4]: PRBS fail in lane3 Bit[3]: PRBS succeed in lane0 Bit[2]: PRBS succeed in lane1 Bit[1]: PRBS succeed in lane2 Bit[0]: PRBS succeed in lane3
0x80290034	ERROR STATUS3	–	R	Bit[7:2]: Reserved Bit[1]: PRBS error in lane2 Bit[0]: PRBS error in lane3
0x80290035~ 0x80290037	RSVD	–	–	Reserved
0x80290038	PIXEL NUM LOW0	–	R	Bit[7:0]: Pixel number in one line for virtual channel 0[7:0]
0x80290039	PIXEL NUM HIGH0	–	R	Bit[7:0]: Pixel number in one line for virtual channel 0[15:8]
0x8029003A	LINE NUM LOW0	–	R	Bit[7:0]: Line number in one frame for virtual channel 0[7:0]
0x8029003B	LINE NUM HIGH0	–	R	Bit[7:0]: Line number in one frame for virtual channel 0[15:8]
0x8029003C	PIXEL NUM LOW1	–	R	Bit[7:0]: Pixel number in one line for virtual channel 1[7:0]
0x8029003D	PIXEL NUM HIGH1	–	R	Bit[7:0]: Pixel number in one line for virtual channel 1[15:8]
0x8029003E	LINE NUM LOW1	–	R	Bit[7:0]: Line number in one frame for virtual channel 1[7:0]
0x8029003F	LINE NUM HIGH1	–	R	Bit[7:0]: Line number in one frame for virtual channel 1[15:8]

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4.8.2 MIPI RX1 control

base address: 0x80290080 MIPI_RX1_BASE

table 4-15 MIPI RX1 registers (sheet 1 of 12)

address	register name	default value	R/W	description
0x80290080	MIPI RX CTRL0	0x20	RW	Bit[7]: Four lane select When this bit is set, four lane input mode will be enabled 0: Four lane input mode disable 1: Four lane input mode enable Bit[6]: Bypass ECC 0: Enable ECC check function 1: Bypass ECC check function Bit[5]: Two lane select When this bit is set, two lane input mode will be enabled 0: Two lane input mode disable 1: Two lane input mode enable Bit[4]: Packet header bit order 0: Retain receiving header data in sequence 1: Reverse receiving header data in sequence Bit[3:2]: Packet header byte order 00: {byte_id byte_number[7:0], byte_number[15:8]} 01: {byte_id, byte_number} 10: {byte_number[7:0], byte_number[15:8], byte_id} 11: {byte_number, byte id} Bit[1]: HREF select for virtual channel1 0: HREF signal of virtual channel 1 generated by aligning valid data package 1: HREF signal of virtual channel 1 generated by line start and line end packages Bit[0]: HREF select for virtual channel0 0: HREF signal of virtual channel 0 generated by aligning valid data package 1: HREF signal of virtual channel 0generated by line start and line end packages
0x80290081	START SIZE V0	0x04	RW	Bit[7:0]: Read FIFO start size for virtual channel0

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table 4-15 MIPI RX1 registers (sheet 2 of 12)

address	register name	default value	R/W	description
0x80290082	MIPI RX CTRL1	0x80	RW	Bit[7]: SOT 1 bit wrong match enable Bit[6]: Data type select for virtual channel0 0: Data type of virtual channel 0 set by receiving data 1: Data type of virtual channel 0 set by register Bit[5:0]: Data type set by registers for virtual channel0
0x80290083	VSYNC COUNTER1 V0	0x04	RW	Bit[7:0]: Counter for asserting VSYNC signal after frame end packet in virtual channel0
0x80290084	VSYNC COUNTER2 V0	0x04	RW	Bit[7:0]: Counter for de-asserting VSYNC signal after frame start packet in virtual channel0
0x80290085	START SIZE V1	0x04	RW	Bit[7:0]: Read FIFO start size for virtual channel1
0x80290086	MIPI RX CTRL2	0x00	RW	Bit[7]: Reserved Bit[6]: Data type select for virtual channel1 0: Data type of virtual channel 1 set by receiving data 1: Data type of virtual channel 1 set by register Bit[5:0]: Data type set by registers for virtual channel1
0x80290087	VSYNC COUNTER1 V1	0x04	RW	Bit[7:0]: Counter for asserting VSYNC signal after frame end packet in virtual channel1
0x80290088	VSYNC COUNTER2 V1	0x04	RW	Bit[7:0]: Counter for de-asserting VSYNC signal after frame start packet in virtual channel1
0x80290089	VIRTUAL CHANNEL NUMBER	0x04	RW	Bit[7:4]: Reserved Bit[3:2]: Virtual channel1 number Bit[1:0]: Virtual channel0 number
0x8029008A~ 0x8029008F	RSVD	–	–	Reserved

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table 4-15 MIPI RX1 registers (sheet 3 of 12)

address	register name	default value	R/W	description
0x80290090	MIPI RX CTRL3	0x0F	RW	Bit[7:6]: Reserved Bit[5]: Disable VSYNC control for HREF and valid in virtual channel1 0: Do not disable VSYNC control in virtual channel1 1: Disable VSYNC control in virtual channel1 Bit[4]: Disable VSYNC control for HREF and valid in virtual channel0 0: Do not disable VSYNC control in virtual channel0 1: Disable VSYNC control in virtual channel0 Bit[3]: Enable VSYNC postive edge reset in virtual channel1 asynchronous FIFO 0: Disable VSYNC postive edge reset in virtual channel1 1: Enable VSYNC postive edge reset in virtual channel1 Bit[2]: Enable VSYNC negative edge reset in virtual channel1 asynchronous FIFO 0: Disable VSYNC negative edge reset in virtual channel1 1: Enable VSYNC negative edge reset in virtual channel1 Bit[1]: Enable VSYNC postive edge reset in virtual channel0 asynchronous FIFO 0: Disable VSYNC postive edge reset in virtual channel0 1: Enable VSYNC postive edge reset in virtual channel0 Bit[0]: Enable VSYNC negative edge reset in virtual channel0 asynchronous FIFO 0: Disable VSYNC negative edge reset in virtual channel0 1: Enable VSYNC negative edge reset in virtual channel0

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table 4-15 MIPI RX1 registers (sheet 4 of 12)

address	register name	default value	R/W	description
0x80290091	LANE SWAP	0xE4	RW	Bit[7:6]: Lane swap control for lane 3 00: Lane3 at the position 0 01: Lane3 at the position 1 10: Lane3 at the position 2 11: Lane3 at the position 3 Bit[5:4]: Lane swap control for lane 2 00: Lane2 at the position 0 01: Lane2 at the position 1 10: Lane2 at the position 2 11: Lane2 at the position 3 Bit[3:2]: Lane swap control for lane 1 00: Lane1 at the position 0 01: Lane1 at the position 1 10: Lane1 at the position 2 11: Lane1 at the position 3 Bit[1:0]: Lane swap control for lane 0 00: Lane0 at the position 0 01: Lane0 at the position 1 10: Lane0 at the position 2 11: Lane0 at the position 3

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table 4-15 MIPI RX1 registers (sheet 5 of 12)

address	register name	default value	R/W	description
0x80290092	OUTPUT CONTROL	0x00	RW	Bit[7:6]: Reserved Bit[5]: Output swap control for virtual channel 1 Reverse the output data byte order of virtual channel 1 Bit[4]: Output swap control for virtual channel 0 Reverse the output data byte order of virtual channel 0 Bit[3]: Four word output control for virtual channel1 0: Disable four word output mode for virtual channel1 1: Enable four word output mode for virtual channel1 Bit[2]: Four word output control for virtual channel0 0: Disable four word output mode for virtual channel0 1: Enable four word output mode for virtual channel0 Bit[1]: Two word output control for virtual channel1 0: Disable two word output mode for virtual channel1 1: Enable two word output mode for virtual channel1 Bit[0]: Two word output control for virtual channel0 0: Disable two word output mode for virtual channel0 1: Enable two word output mode for virtual channel0
0x80290093	SHIFT CONTROL	0x00	RW	Bit[7:4]: Reserved Bit[3]: Shift 4 bits for virtual channel 1 Right shift output data 4 bits in virtual channel1 Bit[2]: Shift 4 bits for virtual channel 0 Right shift output data 4 bits in virtual channe0 Bit[1]: Shift 2 bits for virtual channel 1 Right shift output data 2 bits in virtual channel1 Bit[0]: Shift 2 bits for virtual channel 0 Right shift output data 2 bits in virtual channel0
0x80290094~ 0x8029009F	RSVD	–	–	Reserved

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table 4-15 MIPI RX1 registers (sheet 6 of 12)

address	register name	default value	R/W	description
0x802900A0	PRBS CONTROL	0x00	RW	Bit[7:3]: Reserved Bit[2]: PRBS error clear 0: Do not clear PRBS error 1: Clear PRBS error Bit[1]: PRBS in select 0: PRBS input is not valid 1: PRBS input is valid Bit[0]: PRBS enable 0: Disable PRBS 1: Enable PRBS
0x802900A1	CLEAR ERROR STATUS0	0x00	RW	Bit[7]: SOT error more than 1 bit in lane1 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[6]: SOT error more than 1 bit in lane0 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[5]: One bit error in SOT of lane 1 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[4]: One bit error in SOT of lane 0 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[3]: Receiving byte number not match interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[2]: CRC check error interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[1]: ECC error more than 1 bit interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[0]: ECC single bit error interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt

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table 4-15 MIPI RX1 registers (sheet 7 of 12)

address	register name	default value	R/W	description
0x802900A2	CLEAR ERROR STATUS1	0x00	RW	Bit[7]: Receiving FIFO for virtual channel 1 empty interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[6]: Receiving FIFO for virtual channel 0 empty interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[5]: PRBS error in lane0 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[4]: PRBS error in lane1 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[3]: Receiving FIFO for virtual channel 1 overflow interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[2]: Receiving FIFO for virtual channel 1 full interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[1]: Receiving FIFO for virtual channel 0 overflow interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[0]: Receiving FIFO for virtual channel 0 full interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt
0x802900A3	PRBS TEST COUNTER0	0x00	RW	Bit[7:0]: PRBS test counter[7:0]
0x802900A4	PRBS TEST COUNTER1	0x00	RW	Bit[7:0]: PRBS test counter[15:8]
0x802900A5	PRBS TEST COUNTER2	0x40	RW	Bit[7:0]: PRBS test counter[23:16]
0x802900A6	PRBS ERROR COUNTER	0x10	RW	Bit[7:0]: PRBS error counter

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table 4-15 MIPI RX1 registers (sheet 8 of 12)

address	register name	default value	R/W	description
0x802900A7	ERROR INTERRUPT ENABLE0	0x00	RW	Bit[7]: SOT error more than 1 bit in lane1 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[6]: SOT error more than 1 bit in lane0 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[5]: One bit error in SOT of lane 1 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[4]: One bit error in SOT of lane 0 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[3]: Receiving byte number not match interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[2]: CRC check error interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[1]: ECC error more than 1 bit interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[0]: ECC single bit error interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt

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table 4-15 MIPI RX1 registers (sheet 9 of 12)

address	register name	default value	R/W	description
0x802900A8	ERROR INTERRUPT ENABLE1	0x00	RW	Bit[7]: Receiving FIFO for virtual channel 1 empty interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[6]: Receiving FIFO for virtual channel 0 empty interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[5]: PRBS error in lane0 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[4]: PRBS error in lane1 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[3]: Receiving FIFO for virtual channel 1 overflow interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[2]: Receiving FIFO for virtual channel 1 full interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[1]: Receiving FIFO for virtual channel 0 overflow interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[0]: Receiving FIFO for virtual channel 0 full interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt

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table 4-15 MIPI RX1 registers (sheet 10 of 12)

address	register name	default value	R/W	description
0x802900A9	CLEAR ERROR STATUS2	0x00	RW	Bit[7:6]: Reserved Bit[5]: SOT error more than 1 bit in lane3 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[4]: SOT error more than 1 bit in lane2 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[3]: One bit error in SOT of lane 3 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[2]: One bit error in SOT of lane 2 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[1:0]: Reserved
0x802900AA	ERROR INTERRUPT ENABLE2	0x00	RW	Bit[7:6]: Reserved Bit[5]: SOT error more than 1 bit in lane3 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[4]: SOT error more than 1 bit in lane2 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[3]: One bit error in SOT of lane 3 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[2]: One bit error in SOT of lane 2 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[1:0]: Reserved
0x802900AB	CLEAR ERROR STATUS3	0x00	RW	Bit[7:2]: Reserved Bit[1]: PRBS error in lane2 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt Bit[0]: PRBS error in lane3 interrupt clear 0: Do not clear error status and interrupt 1: Clear error status and interrupt

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table 4-15 MIPI RX1 registers (sheet 11 of 12)

address	register name	default value	R/W	description
0x802900AC	MIPI RX CTRL4	0x48	RW	Bit[7:2]: Embedded ID for virtual channel 1 Embedded ID is used to identify embedded line data Bit[1]: PRBS error in lane2 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt Bit[0]: PRBS error in lane3 interrupt enable 0: Disable error status and interrupt 1: Enable error status and interrupt
0x802900AD	EMBED LINE CTRL0	0x12	RW	Bit[7]: Channel 0 embedded line enable 0: Disable channel 0 embedded line 1: Enable channel 0 embedded line Bit[6]: Channel 1 embedded line enable 0: Disable channel 1 embedded line 1: Enable channel 1 embedded line Bit[5:0]: Embedded ID for virtual channel 0 Embedded ID is used to identify the embedded line data
0x802900AE	EMBED LINE CTRL1	0x2C	RW	Bit[7:6]: Reserved Bit[5:0]: Embedded data type of channel 0 Embedded data type is used to decode the correct data from the long package
0x802900AF	EMBED LINE CTRL2	0x2C	RW	Bit[7:6]: Reserved Bit[5:0]: Embedded data type of channel 1 Embedded data type is used to decode the correct data from long package
0x802900B0	ERROR STATUS0	–	R	Bit[7]: SOT error more than 1 bit in lane1 Bit[6]: SOT error more than 1 bit in lane0 Bit[5]: One bit error in SOT of lane 1 Bit[4]: One bit error in SOT of lane 0 Bit[3]: Receiving byte number not match Bit[2]: CRC check error Bit[1]: ECC error more than 1 bit Bit[0]: ECC single bit error
0x802900B1	ERROR STATUS1	–	R	Bit[7]: Receiving FIFO for virtual channel 1 empty Bit[6]: Receiving FIFO for virtual channel 0 empty Bit[5]: PRBS error in lane0 Bit[4]: PRBS error in lane1 Bit[3]: Receiving FIFO for virtual channel 1 overflow Bit[2]: Receiving FIFO for virtual channel 1 full Bit[1]: Receiving FIFO for virtual channel 0 overflow Bit[0]: Receiving FIFO for virtual channel 0 full

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table 4-15 MIPI RX1 registers (sheet 12 of 12)

address	register name	default value	R/W	description
0x802900B2	ERROR STATUS2	–	R	Bit[7:6]: Reserved Bit[5]: SOT error more than 1 bit in lane3 Bit[4]: SOT error more than 1 bit in lane2 Bit[3]: One bit error in SOT of lane 3 Bit[2]: One bit error in SOT of lane 2 Bit[1:0]: Reserved
0x802900B3	PRBS STATUS	–	R	Bit[7]: PRBS fail in lane0 Bit[6]: PRBS fail in lane1 Bit[5]: PRBS fail in lane2 Bit[4]: PRBS fail in lane3 Bit[3]: PRBS succeed in lane0 Bit[2]: PRBS succeed in lane1 Bit[1]: PRBS succeed in lane2 Bit[0]: PRBS succeed in lane3
0x802900B4	ERROR STATUS3	–	R	Bit[7:2]: Reserved Bit[1]: PRBS error in lane2 Bit[0]: PRBS error in lane3
0x802900B5~ 0x802900B7	RSVD	–	–	Reserved
0x802900B8	PIXEL NUM LOW0	–	R	Bit[7:0]: Pixel number in one line for virtual channel 0[7:0]
0x802900B9	PIXEL NUM HIGH0	–	R	Bit[7:0]: Pixel number in one line for virtual channel 0[15:8]
0x802900BA	LINE NUM LOW0	–	R	Bit[7:0]: Line number in one frame for virtual channel 0[7:0]
0x802900BB	LINE NUM HIGH0	–	R	Bit[7:0]: Line number in one frame for virtual channel 0[15:8]
0x802900BC	PIXEL NUM LOW1	–	R	Bit[7:0]: Pixel number in one line for virtual channel 1[7:0]
0x802900BD	PIXEL NUM HIGH1	–	R	Bit[7:0]: Pixel number in one line for virtual channel 1[15:8]
0x802900BE	LINE NUM LOW1	–	R	Bit[7:0]: Line number in one frame for virtual channel 1[7:0]
0x802900BF	LINE NUM HIGH1	–	R	Bit[7:0]: Line number in one frame for virtual channel 1[15:8]

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4.9 MIPI TX control

base address: 0x80292000

table 4-16 MIPI TX registers (sheet 1 of 10)

address	register name	default value	R/W	description
0x80292000	CLK_POST_ CONST_MIN	0x41	RW	Bit[7:0]: T(clk_post) constant minimum value
0x80292001	CLK_POST_UI_ MIN	0x34	RW	Bit[7:6]: Reserved Bit[5:0]: T(clk_post) UI minimum value
0x80292002	CLK_TRAIL_ CONST_MIN	0x41	RW	Bit[7:0]: T(clk_trail) constant minimum value
0x80292003	CLK_TRAIL_UI _MIN	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: T(clk_trail) UI minimum value
0x80292004	CLK_PREPARE _ CONST_MIN	0x32	RW	Bit[7:0]: T(clk_prepare) constant minimum value
0x80292005	CLK_PREPARE _UI_ MIN	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: T(clk_prepare) UI minimum value
0x80292006	CLK_ZERO_ CONST_MIN1	0x01	RW	Bit[7:2]: Reserved Bit[1:0]: T(clk_zero) constant minimum value[9:8]
0x80292007	CLK_ZERO_ CONST_MIN2	0x2C	RW	Bit[7:0]: T(clk_zero) constant minimum value[7:0]
0x80292008	CLK_ZERO_UI _MIN	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: T(clk_zero) UI minimum value
0x80292009	HS_EXIT_ CONST_ MIN	0x6E	RW	Bit[7:0]: T(hs_exit) constant minimum value
0x8029200A	HS_EXIT_UI_ MIN	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: T(hs_exit) UI minimum value
0x8029200B	HS_PREPARE_ CONST_MIN	0x37	RW	Bit[7:0]: T(hs_prepare) constant minimum value
0x8029200C	HS_PREPARE_ UI_ MIN	0x04	RW	Bit[7:6]: Reserved Bit[5:0]: T(hs_prepare) UI minimum value
0x8029200D	HS_ZERO_ CONST_ MIN	0x6E	RW	Bit[7:0]: T(hs_zero) constant minimum value
0x8029200E	HS_ZERO_UI_ MIN	0x06	RW	Bit[7:6]: Reserved Bit[5:0]: T(hs_zero) UI minimum value
0x8029200F	HS_TRAIL_ CONST_MIN	0x41	RW	Bit[7:0]: T(hs_trail) constant minimum value

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table 4-16 MIPI TX registers (sheet 2 of 10)

address	register name	default value	R/W	description
0x80292010	HS_TRAIL_UI_MIN	0x04	RW	Bit[7:6]: Reserved Bit[5:0]: T(hs_trail) UI minimum value
0x80292011	LPX_CONST_MIN	0x37	RW	Bit[7:0]: T(lpx) constant minimum value
0x80292012	LPX_UI_MIN	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: T(lpx) UI minimum value
0x80292013	MIPI_CLK_PERIOD1	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Clock period of mipi_clk[9:8] Used to calculate timing parameters of MIPI TX Update this register when mipi_clk clock cycle is changed. mipi_clk default is 100MHz
0x80292014	MIPI_CLK_PERIOD2	0x28	RW	Bit[7:0]: Clock period of mipi_clk[7:0] Used to calculate timing parameters of MIPI TX Update this register when the mipi_clk clock cycle is changed mipi_clk default is 100MHz

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table 4-16 MIPI TX registers (sheet 3 of 10)

address	register name	default value	R/W	description
0x80292015	MIPI_LANE_CTRL0	0x92	RW	Bit[7]: Finish lane transfer long packet data exactly 0: Maybe send any dummy data in data lane when image line byte number (add 2 CRC byte) cannot be divided by lane number, meaning there will be one dummy byte in some data lanes 1: Do not send any dummy data in data lane, meaning trail data will be behind image data in each data lane Bit[6]: Clock lane data change 2'b01 → 2'b10 0: Clock lane output sequence is {bit[1][0]} 1: Clock lane output sequence is changed to {bit[0][1]} Bit[5]: dis_clk_lane (active high) Disable clock lane 0: Enable clock lane 1: Disable clock lane Bit[4]: line_sync_en Insert LS/LE in the MIPI TX stream if this bit is set 0: MIPI TX not send any line start (LS) packet or any line end (LE) packet 1: MIPI TX send line start (LS) packet and line end (LE) packet Bit[3]: frame_cnt_zero_c1 MIPI TX channel 1 will keep frame counter zero if this bit is set 0: Virtual channel 1 frame count not kept at zero 1: Virtual channel 1 frame count not kept at zero Bit[2]: frame_cnt_zero_c0 MIPI TX channel 0 will keep frame counter zero if this bit is set 0: Virtual channel 0 frame count not kept at zero 1: Virtual channel 0 frame count kept at zero

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table 4-16 MIPI TX registers (sheet 4 of 10)

address	register name	default value	R/W	description
0x80292015				Bit[1]: gate_clk_en2 (active high) Gate clock about clock lane when frame blanking time 0: Do not gate clock lane when frame blanking 1: Gate clock lane when frame blanking Bit[0]: gate_clk_en1 (active high) Gate clock about clock lane when line/frame blanking time 0: Do not gate clock lane when line/frame blanking 1: Gate clock lane when line/frame blanking
0x80292016	MIPI_LPKT_MAN	0x00	RW	Bit[7]: Reserved Bit[6]: lpkt_man_en (active high) Long packet manual input mode enable 0: Disable long packet manual input mode 1: Enable long packet manual input mode Bit[5:0]: Manual data type
0x80292017	MIPI_DI0	0x1E	RW	Bit[7:6]: Virtual channel ID for data path 0 Bit[5:0]: Data type for data path 0
0x80292018	MIPI_DI1	0x5E	RW	Bit[7:6]: Virtual channel ID for data path 1 Bit[5:0]: Data type for data path 1
0x80292019	MIPI_DI2	0xAA	RW	Bit[7:6]: Virtual channel ID for data path 2 Bit[5:0]: Data type for data path 2
0x8029201A	MIPI_DI3	0xEA	RW	Bit[7:6]: Virtual channel ID for data path 3 Bit[5:0]: Data type for data path 3
0x8029201B	MIPI_IMG_WIDTHH0	0x02	RW	Bit[7:0]: img_width[15:8] Channel 0 image width
0x8029201C	MIPI_IMG_WIDTHL0	0x80	RW	Bit[7:0]: img_width[7:0] Channel 0 image width
0x8029201D	MIPI_IMG_HEIGHTH0	0x01	RW	Bit[7:0]: img_height[15:8] Channel 0 image height
0x8029201E	MIPI_IMG_HEIGHTL0	0xE0	RW	Bit[7:0]: img_height[7:0] Channel 0 image height
0x8029201F	MIPI_IMG_WIDTHH1	0x02	RW	Bit[7:0]: img_width[15:8] Channel 1 image width
0x80292020	MIPI_IMG_WIDTHL1	0x80	RW	Bit[7:0]: img_width[7:0] Channel 1 image width

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table 4-16 MIPI TX registers (sheet 5 of 10)

address	register name	default value	R/W	description
0x80292021	MIPI_IMG_ HEIGHTH1	0x01	RW	Bit[7:0]: img_height[15:8] Channel 1 image height
0x80292022	MIPI_IMG_ HEIGHTL1	0xE0	RW	Bit[7:0]: img_height[7:0] Channel 1 image height
0x80292023	MIPI_IMG_ WIDTHH2	0x02	RW	Bit[7:0]: img_width[15:8] Channel 2 image width
0x80292024	MIPI_IMG_ WIDTHL2	0x80	RW	Bit[7:0]: img_width[7:0] Channel 2 image width
0x80292025	MIPI_IMG_ HEIGHTH2	0x01	RW	Bit[7:0]: img_height[15:8] Channel 2 image height
0x80292026	MIPI_IMG_ HEIGHTL2	0xE0	RW	Bit[7:0]: img_height[7:0] Channel 2 image height
0x80292027	MIPI_IMG_ WIDTHH3	0x02	RW	Bit[7:0]: img_width[15:8] Channel 3 image width
0x80292028	MIPI_IMG_ WIDTHL3	0x80	RW	Bit[7:0]: img_width[7:0] Channel 3 image width
0x80292029	MIPI_IMG_ HEIGHTH3	0x01	RW	Bit[7:0]: img_height[15:8] Channel 3 image height
0x8029202A	MIPI_IMG_ HEIGHTL3	0xE0	RW	Bit[7:0]: img_height[7:0] Channel 3 image height
0x8029202B	MIPI_STATUS	–	R	Bit[7:2]: Reserved Bit[1]: mipi_ph_done MIPI has transferred Long packet header data Bit[0]: mipi_busy MIPI is transmitting data if this bit is asserted

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table 4-16 MIPI TX registers (sheet 6 of 10)

address	register name	default value	R/W	description
0x8029202C	MIPI_LANE_CTRL1	0x0B	RW	Bit[7]: Embedded line enable 0: Disable MIPI TX transmit embedded line 1: Enable MIPI TX transmit embedded line Bit[6]: Send frame start packet (FS) packet after MIPI received SOF 0: Send "FS" packet when VFIFO data is ready 1: Send "FS" packet when MIPI received SOF Bit[5]: Long packet CRC chksum byte exchange enable 0: Chksum output sequence is CRC[15:0] 1: Chksum output sequence is changed to {CRC[7:0], CRC[15:8]} Bit[4]: Reserved Bit[3]: Low power state when data lane is idle 0: Low power signal for each data lane controlled by "lane_en" 1: lp_p or lp_n will stay "1" if current data lane is not active Bit[2]: pclk_inv_en (active high) PCLK inverse enable (PCLK: parallel clock, output to TX PHY) 0: PCLK does not inverse when output 1: PCLK inverse when output Bit[1]: gen_fe1_en Force to generate frame end (FE) short packet in channel 1 when MIPI TX has transmitted one line but VFIFO of this channel is overflow/underflow 0: Do not force to generate FE in channel 1 when MIPI TX has transmitted one line but VFIFO of this channel is overflow/underflow 1: Force to generate FE in channel 1 when MIPI TX has transmitted one line but VFIFO of this channel is overflow/underflow

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table 4-16 MIPI TX registers (sheet 7 of 10)

address	register name	default value	R/W	description
0x8029202C				Bit[0]: gen_fe0_en Force to generate frame end (FE) short packet in channel 0 when MIPI TX has transmitted one line if VFIFO of this channel is overflow/underflow 0: Do not force to generate FE in channel 0 when MIPI TX has transmitted one line but VFIFO of this channel is overflow/underflow 1: Force to generate FE in channel 0 when MIPI TX has transmitted one line but VFIFO of this channel is overflow/underflow
0x8029202D	MIPI_LANE_CTRL2	0x00	RW	Bit[7]: Data lane 4 inverse enable 0: Data output from lane 4 not inversed 1: Data output from lane 4 inversed Bit[6]: Data lane 3 inverse enable 0: Data output from lane 3 not inversed 1: Data output from lane 3 inversed Bit[5]: Data lane 2 inverse enable 0: Data output from lane 2 not inversed 1: Data output from lane 2 inversed Bit[4]: Data lane 1 inverse enable 0: Data output from lane 1 not inversed 1: Data output from lane 1 inversed Bit[3]: lane4_en Data lane 4 enable 0: Disable data lane 4, keep LP11 1: Enable data lane 4 to transmit data Bit[2]: lane3_en Data lane 3 enable 0: Disable data lane 3, keep LP11 1: Enable data lane 3 to transmit data Bit[1]: lane2_en Data lane 2 enable 0: Disable data lane 2, keep LP11 1: Enable data lane 2 to transmit data Bit[0]: lane1_en Data lane 1 enable 0: Disable data lane 1, keep LP11 1: Enable data lane 1 to transmit data

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table 4-16 MIPI TX registers (sheet 8 of 10)

address	register name	default value	R/W	description
0x8029202E	MIPI_LANE_ CTRL3	0x03	RW	Bit[7:4]: Reserved Bit[3]: frame_cnt_zero_c3 MIPI TX channel 3 will keep frame counter zero if this bit is set Bit[2]: frame_cnt_zero_c2 MIPI TX channel 2 will keep frame counter zero if this bit is set Bit[1]: gen_fe3_en Force to generate frame end short packet in channel 3 when MIPI TX has transmitted one line if VFIFO of this channel is overflow/underflow Bit[0]: gen_fe2_en Force to generate frame end short packet in channel 2 when MIPI TX has transmitted one line if VFIFO of this channel is overflow/underflow
0x8029202F	MIPI_TEST	0x00	RW	Bit[7:6]: Reserved Bit[5]: lp_n_man_data Output manual lower power data in MIPI test mode Bit[4]: lp_p_man_data Output manual lower power data in MIPI test mode Bit[3]: lp_man_en Output manual low power data enable in low power test mode and de-assert high speed signal (hs_en or valid) 0: Disable output manual low power data 1: Enable output manual low power data Bit[2]: hs_man_en Manual test data will output to PHY when this bit is set and MIPI TX in high speed test mode (register 0x80292030 must be set in this case) 0: Disable high speed manual test 1: Enable high speed manual test Bit[1]: MIPI TX test_mode 0: Test start point sync by "mipi_test" 1: Test start point sync by MIPI RX output "prbs_en" Bit[0]: mipi_test (active high) Test MIPI TX and RX PHY 0: Disable MIPI TX test 1: Enable MIPI TX test
0x80292030	MAN_DATA	0xFF	RW	Bit[7:0]: Manual test data for MIPI PHY

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table 4-16 MIPI TX registers (sheet 9 of 10)

address	register name	default value	R/W	description
0x80292031	MAX_FCNT_HC0	0xFF	RW	Bit[7:0]: Max frame counter of channel 0[15:8]
0x80292032	MAX_FCNT_LC0	0xFF	RW	Bit[7:0]: Max frame counter of channel 0[7:0]
0x80292033	MAX_FCNT_HC1	0xFF	RW	Bit[7:0]: Max frame counter of channel 1[15:8]
0x80292034	MAX_FCNT_LC1	0xFF	RW	Bit[7:0]: Max frame counter of channel 1[7:0]
0x80292035	MAX_FCNT_HC2	0xFF	RW	Bit[7:0]: Max frame counter of channel 2[15:8]
0x80292036	MAX_FCNT_LC2	0xFF	RW	Bit[7:0]: Max frame counter of channel 2[7:0]
0x80292037	MAX_FCNT_HC3	0xFF	RW	Bit[7:0]: Maxm frame counter of channel 3[15:8]
0x80292038	MAX_FCNT_LC3	0xFF	RW	Bit[7:0]: Max frame counter of channel 3[7:0]
0x80292039	MIPI_EMB_DI0	0x3A	RW	Bit[7:6]: Reserved Bit[5:0]: Data type of embedded line for data path 0
0x8029203A	MIPI_EMB_DI1	0x3A	RW	Bit[7:6]: Reserved Bit[5:0]: Data type of embedded line for data path 1
0x8029203B	MIPI_EMB_DI2	0x3F	RW	Bit[7:6]: Reserved Bit[5:0]: Data type of embedded line for data path 2
0x8029203C	MIPI_EMB_DI3	0x3F	RW	Bit[7:6]: Reserved Bit[5:0]: Data type of embedded line for data path 3
0x8029203D	MIPI_EMB_LINE_WIDTHH0	0x02	RW	Bit[7:0]: img_width[15:8] Channel 0 embedded line width
0x8029203E	MIPI_EMB_LINE_WIDTHL0	0x80	RW	Bit[7:0]: img_width[7:0] Channel 0 embedded line width
0x8029203F	MIPI_EMB_LINE_WIDTHH1	0x02	RW	Bit[7:0]: img_width[15:8] Channel 1 embedded line width
0x80292040	MIPI_EMB_LINE_WIDTHL1	0x80	RW	Bit[7:0]: img_width[7:0] Channel 1 embedded line width
0x80292041	MIPI_EMB_LINE_WIDTHH2	0x02	RW	Bit[7:0]: img_width[15:8] Channel 2 embedded line width

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table 4-16 MIPI TX registers (sheet 10 of 10)

address	register name	default value	R/W	description
0x80292042	MIPI_EMB_ LINE_WIDTHL2	0x80	RW	Bit[7:0]: img_width[7:0] Channel 2 embedded line width
0x80292043	MIPI_EMB_ LINE_WIDTHH3	0x02	RW	Bit[7:0]: img_width[15:8] Channel 3 embedded line width
0x80292044	MIPI_EMB_ LINE_WIDTHL3	0x80	RW	Bit[7:0]: img_width[7:0] Channel 3 embedded line width

4.10 4-wire serial interface control

In the OV490, there is one 4-wire serial interface_M_S module which can be selected as a 4-wire serial interface master or as a 4-wire serial interface slave. By configuring register 0x8080016D, Bit[5]: 4-wire serial interface mode select (0: slave, 1: master (default)); Bit[4]: 4-wire serial interface function enable (0: disable (default), 1: enable). The 4-wire serial interface_M_S can be selected as a master or a slave (default is master).

4.10.1 4-wire serial interface master

base address: 0x80250000

table 4-17 4-wire serial interface master registers (sheet 1 of 11)

address	register name	default value	R/W	description
0x80250000	4-WIRE SERIAL INTERFACE_ CTRL	0x18	RW	Bit[7:5]: Reserved Bit[4]: 4-wire serial interface RX LSB first 0: 4-wire serial interface receive data MSB first 1: 4-wire serial interface receive data LSB first Bit[3]: 4-wire serial interface TX LSB first 4-wire serial interface 0: 4-wire serial interface transmit data MSB first 1: 4-wire serial interface transmit data LSB first Bit[2]: 4-wire serial interface clock phase (CPHA) select This bit is used to select the 4-wire serial interface clock format. In master mode, a change of this bit will abort a transmission in progress and force the 4-wire serial interface system into idle state. 0: Sampling of data occurs at odd edges (1,3,5,...,15) of the SCK clock 1: Sampling of data occurs at even edges (2,4,6,...,16) of the SCK clock

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table 4-17 4-wire serial interface master registers (sheet 2 of 11)

address	register name	default value	R/W	description
0x80250000				Bit[1]: 4-wire serial interface clock polarity (CPOL) This bit selects an inverted or non~ inverted 4-wire serial interface clock. To transmit data between 4-wire serial interface modules, the 4-wire serial interface modules must have identical CPOL values. In master mode, a change of this bit will abort a transmission in progress and force the 4-wire serial interface system into idle state. 0: Active high clocks selected. In idle state, SCK is low. 1: Active low clocks selected. In idle state, SCK is high. Bit[0]: 4-wire serial interface function enable 0: Disable 4-wire serial interface_M_S module 4-wire serial interface function, whatever select as a 4-wire serial interface master or a 4-wire serial interface slave 1: Enable 4-wire serial interface_M_S module 4-wire serial interface function
0x80250001	4-WIRE SERIAL INTERFACE_ START_CTRL	0x01	RW	Bit[7]: dma_access_en 0: Use RISC for 4-wire serial interface master transmit and receive 1: Use DMA for 4-wire serial interface master transmit and receive Bit[6:3]: Reserved Bit[2]: 4-wire serial interface start 0: Do not start 4-wire serial interface transmit or receive data process 1: Start 4-wire serial interface transmit or receive data process Bit[1]: CS control in block 0: 4-wire serial interface CS is allowed to keep low during one block 1: 4-wire serial interface CS is not allowed to keep low during one block when TX FIFO empty or RX FIFO full Bit[0]: CS control between block 0: 4-wire serial interface CS is allowed to keep low between blocks 1: 4-wire serial interface CS is not allowed to keep low between blocks when TX FIFO empty or RX FIFO full

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table 4-17 4-wire serial interface master registers (sheet 3 of 11)

address	register name	default value	R/W	description
0x80250002	4-WIRE SERIAL INTERFACE_ TX_SIZE_LOW	0x00	RW	Bit[7:0]: 4-wire serial interface TX size in one block[7:0] (high byte in register 0x80250009)
0x80250003	4-WIRE SERIAL INTERFACE_ TXSTART_ SIZE_LOW	0x00	RW	Bit[7:0]: 4-wire serial interface TX start size in one block[7:0] (high byte in register 0x8025000A)
0x80250004	4-WIRE SERIAL INTERFACE_ RX_SIZE_LOW	0x00	RW	Bit[7:0]: 4-wire serial interface RX size in one block[7:0] (high byte in register 0x8025000B)
0x80250005	4-WIRE SERIAL INTERFACE_ RXSTART_ SIZE_LOW	0x00	RW	Bit[7:0]: 4-wire serial interface RX start size in one block[7:0] (high byte in register 0x8025000C)
0x80250006	4-WIRE SERIAL INTERFACE_ DIV_RATE	0x00	RW	Bit[7:0]: 4-wire serial interface clock dividing rate base on spi_clk_i Dividing from spi_clk_i/2 - > spi_clk_i/4 - > spi_clk_i/6 … 00: Frequency of SCK is frequency of spi_clk_i / 2 01: Frequency of SCK is frequency of spi_clk_i / 4 10: Frequency of SCK is frequency of spi_clk_i / 6 11: Frequency of SCK is frequency of spi_clk_i / 8 …..255, frequency of SCK is frequency of spi_clk_i / 512

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table 4-17 4-wire serial interface master registers (sheet 4 of 11)

address	register name	default value	R/W	description
0x80250007	4-WIRE SERIAL INTERFACE_ CS_COUNTER	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: 4-wire serial interface CS counter, counting from half of one cycle → one cycle → one and half cycle … 0000: Before start transmit/receive data, count 4-wire serial interface CS active low for half of one SCK cycle 0001: Before start transmit/receive data, count 4-wire serial interface CS low active for one SCK cycle 0010: Before start transmit/receive data, count 4-wire serial interface CS low active for one and half SCK cycles 0011: Before start transmit/receive data, count 4-wire serial interface CS low active for two cycles 0100: Before start transmit/receive data, count 4-wire serial interface CS active low for two and half SCK cycles 0101: Before start transmit/receive data, count 4-wire serial interface CS low active for three SCK cycles 0110: Before start transmit/receive data, count 4-wire serial interface CS low active for three and half SCK cycles 0111: Before start transmit/receive data, count 4-wire serial interface CS low active for four SCK cycles 1000: Before start transmit/receive data, count 4-wire serial interface CS active low for four and half SCK cycles 1001: Before start transmit/receive data, count 4-wire serial interface CS active low for five SCK cycles 1010: Before start transmit/receive data, count 4-wire serial interface CS active low for five and half SCK cycles 1011: Before start transmit/receive data, count 4-wire serial interface CS active low for six SCK cycles 1100: Before start transmit/receive data, count 4-wire serial interface CS active low for six and half SCK cycles

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table 4-17 4-wire serial interface master registers (sheet 5 of 11)

address	register name	default value	R/W	description
0x80250007				1101: Before start transmit/receive data, count 4-wire serial interface CS active low for seven SCK cycles 1110: Before start transmit/receive data, count 4-wire serial interface CS active low for seven and half SCK cycles 1111: Before start transmit/receive data, count 4-wire serial interface CS active low for eight SCK cycles
0x80250008	4-WIRE SERIAL INTERFACE_ SLAVE_SEL	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: 4-wire serial interface slave selection
0x80250009	4-WIRE SERIAL INTERFACE_ TX_SIZE_ HIGH	0x00	RW	Bit[7:0]: 4-wire serial interface TX size in one block[15:8] (low byte in register 0x80250002)
0x8025000A	4-WIRE SERIAL INTERFACE_ TXSTART SIZE_HIGH	0x00	RW	Bit[7:0]: 4-wire serial interface TX start size in one block[15:8] (low byte in register 0x80250003)
0x8025000B	4-WIRE SERIAL INTERFACE_ RX_SIZE_ HIGH	0x00	RW	Bit[7:0]: 4-wire serial interface RX size in one block[15:8] (low byte in register 0x80250004)
0x8025000C	4-WIRE SERIAL INTERFACE_ RXSTART SIZE_HIGH	0x00	RW	Bit[7:0]: 4-wire serial interface RX start size in one block[15:8] (low byte in register 0x80250005)
0x80250010	4-WIRE SERIAL INTERFACE_ TX WDATA	0x00	RW	Bit[7:0]: 4-wire serial interface TX FIFO write data
0x80250011	4-WIRE SERIAL INTERFACE_ RX RDATA	–	R	Bit[7:0]: 4-wire serial interface RX FIFO read data

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table 4-17 4-wire serial interface master registers (sheet 6 of 11)

address	register name	default value	R/W	description
0x80250012	4-WIRE SERIAL INTERFACE_ FIFOSTATUS	–	R	Bit[7:6]: Reserved Bit[5]: RX FIFO is almost full state Bit[4]: TX FIFO is almost empty state Bit[3]: RX FIFO is full state Bit[2]: RX FIFO is not empty state Bit[1]: TX FIFO is full state Bit[0]: TX FIFO is not empty state
0x80250013~ 0x8025001F	RSVD	–	–	Reserved
0x80250020	4-WIRE SERIAL INTERFACE_ ERR_INT_EN	0x00	RW	Bit[7]: 4-wire serial interface RX FIFO almost full interrupt enable 0: Do not output interrupt when 4-wire serial interface RX FIFO is almost full 1: Output interrupt when 4-wire serial interface RX FIFO is almost full Bit[6]: 4-wire serial interface TX FIFO almost empty interrupt enable 0: Do not output interrupt when 4-wire serial interface TX FIFO is almost empty 1: Output interrupt when 4-wire serial interface TX FIFO is almost empty Bit[5]: 4-wire serial interface TX finish interrupt enable 0: Do not output interrupt when 4-wire serial interface transmit data process is finish 1: Output interrupt when 4-wire serial interface transmit data process is finish Bit[4]: 4-wire serial interface RX finish interrupt enable 0: Do not output interrupt when 4-wire serial interface receive data process is finished 1: Output interrupt when 4-wire serial interface receive data process is finish Bit[3]: 4-wire serial interface RX FIFO full interrupt enable 0: Do not output interrupt when 4-wire serial interface RX FIFO is full 1: Output interrupt when 4-wire serial interface RX FIFO is full

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table 4-17 4-wire serial interface master registers (sheet 7 of 11)

address	register name	default value	R/W	description
0x80250020				Bit[2]: 4-wire serial interface RX FIFO not empty interrupt enable 0: Do not output interrupt when 4-wire serial interface RX FIFO is not empty 1: Output interrupt when 4-wire serial interface RX FIFO is not empty Bit[1]: 4-wire serial interface TX FIFO full interrupt enable 0: Do not output interrupt when 4-wire serial interface TX FIFO is full 1: Output interrupt when 4-wire serial interface TX FIFO is full Bit[0]: 4-wire serial interface TX FIFO not empty interrupt enable 0: Do not output interrupt when 4-wire serial interface TX FIFO is not empty 1: Output interrupt when 4-wire serial interface TX FIFO is not empty

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table 4-17 4-wire serial interface master registers (sheet 8 of 11)

address	register name	default value	R/W	description
0x80250021	4-WIRE SERIAL INTERFACE_ ERR_INT_ST	–	R	Bit[7]: 4-wire serial interface interrupt flag for RX FIFO almost full state 0: Indicates there does not exist a 4-wire serial interface RX FIFO almost full interrupt in 4-wire serial interface receive data process 1: Indicates there exists a 4-wire serial interface RX FIFO almost full interrupt in 4-wire serial interface receive data process Bit[6]: 4-wire serial interface interrupt flag for 4-wire serial interface TX FIFO almost empty state 0: Indicates there does not exist a 4-wire serial interface TX FIFO almost empty interrupt in 4-wire serial interface transmit data process 1: Indicates there exists 4-wire serial interface TX FIFO almost full interrupt in 4-wire serial interface transmit data process Bit[5]: 4-wire serial interface interrupt flag for 4-wire serial interface transmit data process finish state 0: Indicates there does not exist a 4-wire serial interface transmit data process finish state interrupt in 4-wire serial interface transmit data process 1: Indicates there exists 4-wire serial interface transmit data process finish state interrupt in 4-wire serial interface transmit data process Bit[4]: 4-wire serial interface interrupt flag for 4-wire serial interface receive data process finish state 0: Indicates there does not a exist 4-wire serial interface receive data process finish state interrupt in 4-wire serial interface transmit data process 1: Indicates there exists a 4-wire serial interface receive data process finish state interrupt in 4-wire serial interface transmit data process X FIFO full interrupt in 4-wire serial interface transmit data process

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table 4-17 4-wire serial interface master registers (sheet 9 of 11)

address	register name	default value	R/W	description
0x80250021				Bit[3]: 4-wire serial interface interrupt flag for 4-wire serial interface RX FIFO full state 0: Indicates there does not exist a 4-wire serial interface RX FIFO full interrupt in 4-wire serial interface receive data process 1: Indicates there exists a 4-wire serial interface RX FIFO full interrupt in 4-wire serial interface receive data process Bit[2]: 4-wire serial interface interrupt flag for 4-wire serial interface RX FIFO not empty state 0: Indicates there does not exist a 4-wire serial interface RX FIFO not empty interrupt in 4-wire serial interface receive data process 1: Indicates there exists a 4-wire serial interface RX FIFO not empty interrupt in 4-wire serial interface receive data process Bit[1]: 4-wire serial interface interrupt flag for 4-wire serial interface TX FIFO full state 0: Indicates there does not exist a 4-wire serial interface TX FIFO full interrupt in 4-wire serial interface transmit data process 1: Indicates there exists a 4-wire serial interface TX FIFO full interrupt in 4-wire serial interface transmit process Bit[0]: 4-wire serial interface interrupt flag for 4-wire serial interface TX FIFO not empty state 0: Indicates there does not exist a 4-wire serial interface TX FIFO not empty interrupt in 4-wire serial interface transmit data process 1: Indicates there exists a 4-wire serial interface TX FIFO not empty interrupt in 4-wire serial interface transmit data process
0x80250022	4-WIRE SERIAL INTERFACE_ TX_FIFO_ CNT	–	R	Bit[7:6]: Reserved Bit[5:0]: Number of bytes that exist in TX FIFO

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table 4-17 4-wire serial interface master registers (sheet 10 of 11)

address	register name	default value	R/W	description
0x80250023	4-WIRE SERIAL INTERFACE_ RX_FIFO_ CNT	–	R	Bit[7:6]: Reserved Bit[5:0]: Number of bytes that exist in RX FIFO
0x80250024	4-WIRE SERIAL INTERFACE_ INTR_CLEAR	–	W	Bit[7]: Clear enable of 4-wire serial interface interrupt flag for 4-wire serial interface RX FIFO almost full state 0: Do not clear 4-wire serial interface interrupt flag for 4-wire serial interface RX FIFO almost full state 1: Clear 4-wire serial interface interrupt flag for 4-wire serial interface RX FIFO almost full state Bit[6]: Clear enable of 4-wire serial interface interrupt flag for 4-wire serial interface TX FIFO almost empty state 0: Do not clear 4-wire serial interface interrupt flag for 4-wire serial interface TX FIFO almost empty state 1: Clear 4-wire serial interface interrupt flag for 4-wire serial interface TX FIFO almost empty state Bit[5]: Clear enable of 4-wire serial interface interrupt flag for 4-wire serial interface transmit data process finish state 0: Do not clear 4-wire serial interface interrupt flag for 4-wire serial interface transmit data process finish state 1: Clear 4-wire serial interface interrupt flag for 4-wire serial interface transmit data process finish state Bit[4]: Clear enable of 4-wire serial interface interrupt flag for 4-wire serial interface receive data process finish state 0: Do not clear 4-wire serial interface interrupt flag for 4-wire serial interface receive data process finish state 1: Clear 4-wire serial interface interrupt flag for 4-wire serial interface receive data process finish state

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table 4-17 4-wire serial interface master registers (sheet 11 of 11)

address	register name	default value	R/W	description
				Bit[3]: Clear enable of 4-wire serial interface interrupt for 4-wire serial interface RX FIFO full state 0: Do not clear 4-wire serial interface interrupt flag for 4-wire serial interface RX FIFO full state 1: Clear 4-wire serial interface interrupt flag for 4-wire serial interface RX FIFO full state Bit[2]: Clear enable of 4-wire serial interface interrupt flag for 4-wire serial interface RX FIFO not empty state 0: Do not clear 4-wire serial interface interrupt flag for 4-wire serial interface RX FIFO not empty state 1: Clear 4-wire serial interface interrupt flag for 4-wire serial interface RX FIFO not empty state Bit[1]: Clear enable of 4-wire serial interface interrupt flag for 4-wire serial interface TX FIFO full state 0: Do not clear 4-wire serial interface interrupt flag for 4-wire serial interface TX FIFO full state 1: Clear 4-wire serial interface interrupt flag for 4-wire serial interface TX FIFO full state Bit[0]: Clear enable of 4-wire serial interface interrupt flag for 4-wire serial interface TX FIFO not empty state
0x80250025~ 0x8025002F	RSVD	–	–	Reserved
0x80250030	4-WIRE SERIAL INTERFACE_ MST_TX_FIFO _THRE	0x10	RW	Bit[7:0]: 4-wire serial interface master TX FIFO threshold for requesting DMA write
0x80250031	4-WIRE SERIAL INTERFACE_ SLV_RX_FIFO _THRE	0x10	RW	Bit[7:0]: 4-wire serial interface master RX FIFO threshold for requesting DMA read

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4.10.2 4-wire serial interface slave

base address: 0x80250000

table 4-18 4-wire serial interface slave registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x80250000	SPI_CTRL_R0	0x00	RW	Bit[7]: 4-wire serial interface clock phase (CPHA) select This bit is used to select the 4-wire serial interface clock format. In master mode, a change of this bit will abort a transmission in progress and force the 4-wire serial interface system into idle state. 0: Sampling of data occurs at odd edges (1,3,5,...,15) of the SCK clock 1: Sampling of data occurs at even edges (2,4,6,...,16) of the SCK clock Bit[6]: 4-wire serial interface clock polarity (CPOL) This bit selects an inverted or non-inverted 4-wire serial interface clock. To transmit data between 4-wire serial interface modules, the 4-wire serial interface modules must have identical CPOL values. In master mode, a change of this bit will abort a transmission in progress and force the 4-wire serial interface system into idle state. 0: Active high clocks selected. In idle state, SCK is low 1: Active low clocks selected. In idle state, SCK is high. Bit[5]: 4-wire serial interface RX enable 0: Disable 4-wire serial interface slave receive data process 1: Enable 4-wire serial interface slave receive data process Bit[4]: 4-wire serial interface TX enable 0: Disable 4-wire serial interface slave transmit data process 1: Enable 4-wire serial interface slave transmit data process Bit[3]: 4-wire serial interface LSB first 0: 4-wire serial interface slave transmit/receive data MSB first 1: 4-wire serial interface slave transmit/receive data LSB first

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table 4-18 4-wire serial interface slave registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x80250000				Bit[2]: 4-wire serial interface RX FIFO empty interrupt enable 0: Do not output interrupt when 4-wire serial interface RX FIFO is empty 1: Output interrupt when 4-wire serial interface RX FIFO is empty Bit[1]: 4-wire serial interface TX FIFO full interrupt enable 0: Do not output interrupt when 4-wire serial interface TX FIFO is full 1: Output interrupt when 4-wire serial interface TX FIFO is full Bit[0]: 4-wire serial interface SLAVE reset select 0: 4-wire serial interface reset by system reset 1: 4-wire serial interface reset by system reset and 4-wire serial interface CS

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table 4-18 4-wire serial interface slave registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x80250001	SPI_CTRL_R1	0x00	RW	Bit[7]: dma_access_en 0: Use RISC for 4-wire serial interface transmit and receive data move 1: Use DMA for 4-wire serial interface transmit and receive data move Bit[6:5]: Reserved Bit[4]: 4-wire serial interface slave RX FIFO write clear 0: Do not enable 4-wire serial interface slave asynchronous RX FIFO write clear 1: Enable 4-wire serial interface slave asynchronous RX FIFO write clear Bit[3]: 4-wire serial interface slave RX FIFO read clear 0: Do not enable 4-wire serial interface slave asynchronous RX FIFO read clear 1: Enable 4-wire serial interface slave asynchronous RX FIFO read clear Bit[2]: 4-wire serial interface slave TX FIFO write clear 0: Do not enable 4-wire serial interface slave asynchronous TX FIFO write clear 1: Enable 4-wire serial interface slave asynchronous TX FIFO write clear Bit[1]: 4-wire serial interface slave TX FIFO read clear 0: Do not enable 4-wire serial interface slave asynchronous TX FIFO read clear 1: Enable 4-wire serial interface slave asynchronous TX FIFO read clear Bit[0]: 4-wire serial interface slave enable

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table 4-18 4-wire serial interface slave registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x80250003	SPI_STAT_R3	–	R	Bit[7]: 4-wire serial interface interrupt flag for 4-wire serial interface RX FIFO not empty state 0: Indicates there does not exist a 4-wire serial interface RX FIFO not empty interrupt in 4-wire serial interface receive data process 1: Indicates there exists a 4-wire serial interface RX FIFO not empty interrupt in 4-wire serial interface receive data process Bit[6]: 4-wire serial interface interrupt flag for 4-wire serial interface RX FIFO full state 0: Indicates there does not exist a 4-wire serial interface RX FIFO full interrupt in 4-wire serial interface receive data process 1: Indicates there exists a 4-wire serial interface RX FIFO full interrupt in 4-wire serial interface receive data process Bit[5]: 4-wire serial interface interrupt flag for 4-wire serial interface TX FIFO not empty state 0: Indicates there does not exist a 4-wire serial interface TX FIFO not empty interrupt in 4-wire serial interface transmit data process 1: Indicates there exists a 4-wire serial interface TX FIFO not empty interrupt in 4-wire serial interface transmit data process Bit[1]: 4-wire serial interface interrupt flag for 4-wire serial interface TX FIFO full state 0: Indicates there does not exist a 4-wire serial interface TX FIFO full interrupt in 4-wire serial interface transmit data process 1: Indicates there exists a 4-wire serial interface TX FIFO full interrupt in 4-wire serial interface transmit data process Bit[3]: 4-wire serial interface TX FIFO not empty state 0: 4-wire serial interface TX FIFO is in empty state 1: 4-wire serial interface TX FIFO is not in empty state

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table 4-18 4-wire serial interface slave registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x80250003				Bit[2]: 4-wire serial interface TX FIFO full state 0: 4-wire serial interface TX FIFO is not in full state 1: 4-wire serial interface TX FIFO is in full state Bit[1]: 4-wire serial interface RX FIFO not empty state 0: 4-wire serial interface RX FIFO is in empty state 1: 4-wire serial interface RX FIFO is not in empty state Bit[0]: 4-wire serial interface RX FIFO full state 0: 4-wire serial interface RX FIFO is not in full state 1: 4-wire serial interface RX FIFO is in full state
0x80250004	SPI_TXD_R4	0x00	RW	Bit[7:0]: 4-wire serial interface TX FIFO write data
0x80250005	SPI_RXD_R5	–	R	Bit[7:0]: 4-wire serial interface RX FIFO read data
0x80250006	SPI_SLV_TX_FIFO_THRE	0x10	RW	Bit[7:0]: 4-wire serial interface slave TX FIFO threshold for requesting DMA write
0x80250007	SPI_SLV_RX_FIFO_THRE	0x10	RW	Bit[7:0]: 4-wire serial interface slave RX FIFO threshold for requesting DMA read

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table 4-18 4-wire serial interface slave registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x80250008	SPI_SLV_ ALMOST_ STATUS	–	R	Bit[7:4]: Reserved Bit[3]: 4-wire serial interface interrupt flag for RX FIFO almost full state 0: Indicates there does not exist a 4-wire serial interface RX FIFO almost full interrupt in 4-wire serial interface receive data process 1: Indicates there exists a 4-wire serial interface RX FIFO almost full interrupt in 4-wire serial interface receive data process Bit[2]: 4-wire serial interface interrupt flag for 4-wire serial interface TX FIFO almost empty state 0: Indicates there does not exist a 4-wire serial interface TX FIFO almost empty interrupt in 4-wire serial interface transmit data process 1: Indicates there exists a 4-wire serial interface TX FIFO almost full interrupt in 4-wire serial interface transmit data process Bit[1]: 4-wire serial interface RX FIFO almost full state 0: 4-wire serial interface RX FIFO is not in almost full state 1: 4-wire serial interface RX FIFO is in almost full state Bit[0]: 4-wire serial interface TX FIFO almost empty state 0: 4-wire serial interface TX FIFO is not in almost empty state 1: 4-wire serial interface TX FIFO is in almost empty state

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4.11 DMA control

DMA control has two main registers whose address is dma_start_addr and dma_start_addr + 4. For dma_start_addr, Bit[31:23] is DMA size. For mode 0 and not 4-wire serial interface mode, one DMA size is equal to 4 bytes. Maximum is 255, which is equal to 255x4 bytes. For others, one DMA size is equal to 1 bytes. Maximum is 511 bytes. Bit[22:20]: DMA type. 3'b000: normal access. DMA mode various transfer types:

- internal 32r 32w
- internal 32r 8w
- internal 8r 32w
- internal 8r 8w

To enable handshake with 4-wire serial interface into 1'b1:

- with 4-wire serial interface, 8r of 4-wire serial interface, 8w - read 4-wire serial interface enable, should set EMA_SEL
- with 4-wire serial interface, 8r of 4-wire serial interface, 32w - read 4-wire serial interface enable, 32-bit 4-wire serial interface mode, should set EMA_SEL
- with 4-wire serial interface, 8w of 4-wire serial interface, 8r - write 4-wire serial interface enable
- with 4-wire serial interface 8w of 4-wire serial interface, 32r - write 4-wire serial interface enable, 32 bit 4-wire serial interface mode

```
3'b001: special uncontinuous register address mode for 16bit address
3'b010: a/b frame write mode for 16bit address
3'b011: special uncontinuous register address mode for 32-bit address
3'b100: a/b frame write mode for 32-bit address

Bit[19]: dma read address 32 bit enable

Bit[18]: dma write address 32 bit enable

Bit[15:8]: ord address[24:16]

Bit[7:0]: ord address[15:8]

For (dma_start_addr + 4)

Bit[31:24]: ord address[7:0]

Bit[23:0]: des address[23:0]
```

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base address: 0x8028C000

table 4-19 DMA control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x8028C000	DMA START ADDRESS BYTE0	0x00	RW	Bit[7:0]: Address from which DMA first takes information of configuration such as the size and type of data transferred by DMA start address[31:24]
0x8028C001	DMA START ADDRESS BYTE1	0x00	RW	Bit[7:0]: Address from which DMA first takes information of configuration such as the size and type of data transferred by DMA start address[23:16]
0x8028C002	DMA START ADDRESS BYTE2	0x00	RW	Bit[7:0]: Address from which DMA first takes information of configuration such as the size and type of data transferred by DMA start address[15:8]
0x8028C003	DMA START ADDRESS BYTE3	0x00	RW	Bit[7:0]: Address from which DMA first takes information of configuration such as the size and type of data transferred by DMA start address[7:0]
0x8028C004~ 0x8028C007	RSVD	–	–	Reserved
0x8028C008	EMB ADDRESS BYTE0	0x00	RW	Bit[7:0]: Target address[31:24] of SRAM of embedded line or FIFO of 4-wire serial interface in mode 1 or mode 3
0x8028C009	EMB ADDRESS BYTE1	0x06	RW	Bit[7:0]: Target address[23:16] of SRAM of embedded line or FIFO of 4-wire serial interface in mode 1 or mode 3
0x8028C00A	EMB ADDRESS BYTE2	0x68	RW	Bit[7:0]: Target address[15:8] of SRAM of embedded line or FIFO of 4-wire serial interface in mode 1 or mode 3
0x8028C00B	EMB ADDRESS BYTE3	0x10	RW	Bit[7:0]: Target address[7:0] of SRAM of embedded line or FIFO of 4-wire serial interface in mode 1 or mode 3

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table 4-19 DMA control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x8028C00C	EMB SEL	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Embedded line address select for 8 bit access of SRAM of embedded line or FIFO of 4-wire serial interface
0x8028C00D	EMA HI ADDR BYTE0	0x00	RW	Bit[7:0]: Base address[15:8] of the target address for embedded line registers in mode 1 or mode 2
0x8028C00E	EMA HI ADDR BYTE1	0x06	RW	Bit[7:0]: Base address[7:0] of the target address for embedded line registers in mode 1 or mode 2
0x8028C00F~ 0x8028C010	RSVD	–	–	Reserved
0x8028C011	CONTROL REGISTER	0x00	RW	Bit[7:5]: Reserved Bit[4]: Enable access of SRAM in 32-bit mode in 4-wire serial interface mode 0: Disable mode 1: Enable mode Bit[3]: Enable action of writing unfixed address for embedded line access 0: Disable action 1: Enable action Bit[2]: Read or write 4-wire serial interface module 0: Write 4-wire serial interface 1: Read 4-wire serial interface Bit[1]: Enable hardware handshake with 4-wire serial interface module 0: Disable handshake with 4-wire serial interface 1: Enable handshake with 4-wire serial interface Bit[0]: Enable A/B frame mode 0: Disable A/B frame mode 1: Enable A/B frame mode

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base address: 0x8028D000

table 4-20 DMA control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x8028D000	DMA START ADDRESS BYTE0	0x00	RW	Bit[7:0]: Address from which DMA first takes information of configuration such as the size and type of data transferred by DMA start address[31:24]
0x8028D001	DMA START ADDRESS BYTE1	0x00	RW	Bit[7:0]: Address from which DMA first takes information of configuration such as the size and type of data transferred by DMA start address[23:16]
0x8028D002	DMA START ADDRESS BYTE2	0x00	RW	Bit[7:0]: Address from which DMA first takes information of configuration such as the size and type of data transferred by DMA start address[15:8]
0x8028D003	DMA START ADDRESS BYTE3	0x00	RW	Bit[7:0]: Address from which DMA first takes information of configuration such as the size and type of data transferred by DMA start address[7:0]
0x8028D004~ 0x8028D007	RSVD	–	–	Reserved
0x8028D008	EMB ADDRESS BYTE0	0x00	RW	Bit[7:0]: Target address[31:24] of SRAM of embedded line or FIFO of 4-wire serial interface in mode 1 or mode 3
0x8028D009	EMB ADDRESS BYTE1	0x06	RW	Bit[7:0]: Target address[23:16] of SRAM of embedded line or FIFO of 4-wire serial interface in mode 1 or mode 3
0x8028D00A	EMB ADDRESS BYTE2	0x68	RW	Bit[7:0]: Target address[15:8] of SRAM of embedded line or FIFO of 4-wire serial interface in mode 1 or mode 3
0x8028D00B	EMB ADDRESS BYTE3	0x10	RW	Bit[7:0]: Target address[7:0] of SRAM of embedded line or FIFO of 4-wire serial interface in mode 1 or mode 3

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table 4-20 DMA control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x8028D00C	EMB SEL	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Embedded line address select for 8 bit access of SRAM of embedded line or FIFO of 4-wire serial interface
0x8028D00D	EMA HI ADDR BYTE0	0x00	RW	Bit[7:0]: Base address[15:8] of target address for embedded line registers in mode 1 or mode 2
0x8028D00E	EMA HI ADDR BYTE1	0x06	RW	Bit[7:0]: Base address[7:0] of target address for embedded line registers in mode 1 or mode 2
0x8028D00F~ 0x8028D010	RSVD	–	–	Reserved
0x8028D011	CONTROL REGISTER	0x00	RW	Bit[7:5]: Reserved Bit[4]: Enable access of SRAM in 32-bit mode in 4-wire serial interface mode 0: Disable mode 1: Enable mode Bit[3]: Enable action of writing unfixed address for embedded line access 0: Disable action 1: Enable action Bit[2]: Read or write 4-wire serial interface module 0: Write 4-wire serial interface 1: Read 4-wire serial interface Bit[1]: Enable hardware handshake with 4-wire serial interface module 0: Disable handshake with 4-wire serial interface 1: Enable handshake with 4-wire serial interface Bit[0]: Enable A/B frame mode 0: Disable A/B frame mode 1: Enable A/B frame mode

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4.12 VFIFO control

base address: 0x80296000

table 4-21 VFIFO registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x80296000~ 0x80296003	RSVD	–	–	Reserved
0x80296004	CHANNEL ENABLE REG	0x00	RW	Bit[7:4]: Reserved Bit[3]: Channel 4 enable 0: Disable channel 4 1: Enable channel 4 Bit[2]: Channel 3 enable 0: Disable channel 3 1: Enable channel 3 Bit[1]: Channel 2 enable 0: Disable channel 2 1: Enable channel 2 Bit[0]: Channel 1 enable 0: Disable channel 1 1: Enable channel 1
0x80296005~ 0x8029600A	RSVD	–	–	Reserved
0x8029600B	MIPI INTERFACE REG	0x80	RW	Bit[7:4]: Reserved Bit[3]: mipi_lp_dir2_o Bit[2]: mipi_lp_dir1_o Bit[1]: mipi_lp_ck_sel_o Bit[0]: mipi_lp_da_sel_o
0x8029600C	RSVD	–	–	Reserved
0x8029600E	CTRL REGISTER0	0x00	RW	Bit[7:2]: Reserved Bit[1]: Embedded line mode enable 0: Disable embedded line mode 1: Enable embedded line mode Bit[0]: Enable mode of directly selecting long/short/vshort pixels 0: Disable mode 1: Enable mode
0x8029600F	CHANNEL ID REGISTER	0xE4	RW	Bit[7:6]: Channel ID4 Bit[5:4]: Channel ID3 Bit[3:2]: Channel ID2 Bit[1:0]: Channel ID1

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table 4-21 VFIFO registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x80296010	IMAGE CONTROL REGISTER	0x01	RW	Bit[7]: Reserved Bit[6]: Image of side-by-side delay mode enable 0: Disable mode 1: Enable mode Bit[5]: Enable merging of two line for side-by-side mode 0: Disable mode 1: Enable mode Bit[4]: Enable swapping of Y and UV 0: Enable swapping 1: Disable swapping Bit[3]: Reserved Bit[2:1]: Image format and mode 00: Single image one format 01: Single image two format 10: Dual image single format 11: Dual image dual format Bit[0]: Priority for lanes when data of two lanes arrives 0: Lane3 or lane4 first 1: Lane1 or lane2 first
0x80296011~ 0x80296028	RSVD	–	–	Reserved
0x80296029	LANE1 H SIZE BYTE0	0x0A	RW	Bit[7:5]: Reserved Bit[4:0]: Horizontal size[12:8] of lane 1
0x8029602A	LANE1 H SIZE BYTE1	0x00	RW	Bit[7:0]: Horizontal size[7:0] of lane 1
0x8029602B	LANE1 V SIZE BYTE0	0x04	RW	Bit[7:4]: Reserved Bit[3:0]: Vertical size[11:8] of lane 1
0x8029602C	LANE1 V SIZE BYTE1	0x38	RW	Bit[7:0]: Horizontal size[7:0] of lane 1
0x8029602D	LANE2 H SIZE BYTE0	0x05	RW	Bit[7:5]: Reserved Bit[4:0]: Horizontal size[12:8] of lane 2
0x8029602E	LANE2 H SIZE BYTE1	0x00	RW	Bit[7:0]: Horizontal size[7:0] of lane 2
0x8029602F	LANE2 V SIZE BYTE0	0x04	RW	Bit[7:4]: Reserved Bit[3:0]: Vertical size[11:8] of lane 2
0x80296030	LANE2 V SIZE BYTE1	0x38	RW	Bit[7:0]: Horizontal size[7:0] of lane 2
0x80296031	FORMAT SELECT REG	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Format selection for L/S/VS bypass mode

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table 4-21 VFIFO registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x80296032~ 0x80296040	RSVD	–	–	Reserved
0x80296041	DVP CTRL0 FOR LANE1	0x17		Bit[7:4]: Line pixel counter control of DVP for lane1 Bit[3]: Line pixel counter control free of DVP for lane1 Bit[2]: Read start point select of DVP for lane1 0: Read start point defined by subtraction of line length register sub read start register 1: Read start point defined by read start register Bit[1]: Reserved Bit[0]: Read start signal select of DVP for lane1 0: Select fifo_rd_i as read start signal 1: Select moment when line pixel counter is equal to read start
0x80296042~ 0x80296044	RSVD	–	–	Reserved
0x80296045	DVP CTRL1 FOR LANE1	0x04		Bit[7:4]: Reserved Bit[3]: Automatic set start size of DVP for lane1 Bit[2]: Line length select of DVP for lane1 0: Auto calculate line length 1: Line length is set by register Bit[1]: Reserved Bit[0]: First line signal select of DVP for lane1 0: First line signal will be generated when line counter is equal to one 1: First line signal will be generated when the first valid data is inputted
0x80296046	DVP LINE LENGTH BYTE0 FOR LANE1	0x00	RW	Bit[7:0]: Line length[15:8] for DVP for lane1
0x80296047	DVP LINE LENGTH BYTE1 FOR LANE1	0x00	RW	Bit[7:0]: Line length[7:0] for DVP for lane1
0x80296048	READ START BYTE0 FOR LANE1	0x05	RW0	Bit[7:0]: Read start[15:8] for lane1

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table 4-21 VFIFO registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x80296049	READ START BYTE1 FOR LANE1	0x00	RW	Bit[7:0]: Read start[7:0] for lane1
0x8029604A	HSYNC START BYTE0 FOR LANE1	0x00	RW	Bit[7:0]: HSYNC start position[15:8] for lane1 HSYNC start position defines first HSYNC position at Vblanking time
0x8029604B	HSYNC START BYTE1 FOR LANE1	0xBF	RW	Bit[7:0]: HSYNC start position[7:0] for lane1 HSYNC start position defines first HSYNC position at Vblanking time
0x8029604C	HSYNC CTRL FOR LANE1	0x00	RW	Bit[7:4]: HSYNC header[11:8] for lane1 HSYNC header defines blanking cycles between end of valid data and start of the HSYNC signal (see register 0x80296053 for low byte) Bit[3:0]: HSYNC trail[11:8] for lane1 HSYNC trail register defines the blanking cycles between end of HSYNC signal and start of valid data (see register 0x80296054 for low byte)
0x8029604D~ 0x8029604F	RSVD	–	–	Reserved
0x80296050	DVP CTRL2 FOR LANE1	0x01	RW	Bit[7:3]: Reserved Bit[2]: HSYNC polarity for lane1 0: Active high for HSYNC signal 1: Active low for HSYNC signal Bit[1]: dvp_swp_en for lane1 Bit[0]: Reserved
0x80296051	EMB READ START BYTE0 FOR LANE1	0x00	RW	Bit[7:0]: Read start[15:8] for embedded line for lane1
0x80296052	EMB READ START BYTE1 FOR LANE1	0x00	RW	Bit[7:0]: Read start[7:0] for embedded line for lane1
0x80296053	HSYNC HEADER FOR LANE1	0x05	RW	Bit[7:0]: HSYNC header[7:0] for lane1 HSYNC header register defines blanking cycles between end of valid data and start of the HSYNC signal (see register bits 0x8029604[7:4] for high byte)
0x80296054	HSYNC TRAIL FOR LANE1	0x00	RW	Bit[7:0]: HSYNC trail[7:0] for lane1 HSYNC trail register defines blanking cycles between end of HSYNC signal and start of valid data (see register bits 0x8029604[3:0] for high byte)

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table 4-21 VFIFO registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x80296055~ 0x80296080	RSVD	–	–	Reserved
0x80296081	DVP CTRL0 FOR LANE2	0x17	RW	Bit[7:4]: Line pixel counter control of DVP for lane2 Bit[3]: Line pixel counter control free of DVP for lane2 Bit[2]: Read start point select of DVP for lane2 0: Read start point defined by subtraction of line length register sub read start register 1: Read start point defined by read start register Bit[1]: Reserved Bit[0]: Read start signal select of DVP for lane2 0: Select fifo_rd_i as read start signal 1: Select moment when line pixel counter is equal to read start
0x80296082~ 0x80296084	RSVD	–	–	Reserved
0x80296085	DVP CTRL1 FOR LANE2	0x04	RW	Bit[7:4]: Reserved Bit[3]: Automatic set start size of DVP for lane2 Bit[2]: Line length select of DVP for lane2 0: Auto calculate line length 1: Line length is set by register Bit[1]: Reserved Bit[0]: First line signal select of DVP for lane2 0: First line signal will be generated when line counter is equal to one 1: First line signal will be generated when first valid data is inputted
0x80296086	DVP LINE LENGTH BYTE0 FOR LANE2	0x00	RW	Bit[7:0]: Line length[15:8] for DVP for lane2
0x80296087	DVP LINE LENGTH BYTE1 FOR LANE2	0x00	RW	Bit[7:0]: Line length[7:0] for DVP for lane2
0x80296088	READ START BYTE0 FOR LANE2	0x05	RW0	Bit[7:0]: Read start[15:8] for lane2

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table 4-21 VFIFO registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x80296089	READ START BYTE1 FOR LANE2	0x00	RW	Bit[7:0]: Read start[7:0] for lane2
0x8029608A	HSYNC START BYTE0 FOR LANE2	0x00	RW	Bit[7:0]: HSYNC start position[15:8] for lane2 HSYNC start position defines first HSYNC position at Vblanking time
0x8029608B	HSYNC START BYTE1 FOR LANE2	0xBF	RW	Bit[7:0]: HSYNC start position[7:0] for lane2 HSYNC start position defines first HSYNC position at Vblanking time
0x8029608C	HSYNC CTRL FOR LANE2	0x00	RW	Bit[7:4]: HSYNC header[11:8] for lane1 HSYNC header register defines blanking cycles between end of valid data and start of HSYNC signal (see register 0x8029693 for low byte) Bit[3:0]: HSYNC trail[11:8] for lane1 HSYNC trail defines blanking cycles between end of HSYNC signal and start of valid data (see register 0x8029694 for low byte)
0x8029608D~ 0x80296089	RSVD	–	–	Reserved
0x80296090	DVP CTRL2 FOR LANE2	0x01	RW	Bit[7:3]: Reserved Bit[2]: HSYNC polarity for lane1 0: Active high for HSYNC signal 1: Active low for HSYNC signal Bit[1]: dvp_swp_en for lane1 Bit[0]: Reserved
0x80296091	EMB READ START BYTE0 FOR LANE2	0x00	RW	Bit[7:0]: Read start[15:8] for embedded line for lane2
0x80296092	EMB READ START BYTE1 FOR LANE2	0x00	RW	Bit[7:0]: Read start[7:0] for embedded line for lane2
0x80296093	SYNC HEADER FOR LANE2	0x05	RW	Bit[7:0]: HSYNC header[7:0] for lane1 HSYNC header defines blanking cycles between end of valid data and start of HSYNC signal (see register bits 0x8029608C[7:4] for high byte)
0x80296094	HSYNC TRAIL FOR LANE2	0x00	RW	Bit[7:0]: HSYNC trail[7:0] for lane1 HSYNC trail defines blanking cycles between end of HSYNC signal and start of valid data (see register bits 0x8029608C[3:0] for high byte)

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4.13 SCCB slave control

base address: 0x802A6000

table 4-22 SCCB slave registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x802A6000	SCCB_CTRL	0x00	RW	Bit[7]: rd_clear enable 0: Do not enable asynchronous FIFO read clear 1: Enable asynchronous FIFO read clear Bit[6]: wr_clear enable 0: Do not enable asynchronous FIFO write clear 1: Enable asynchronous FIFO write clear Bit[5]: Clear enable of interrupt flag for asynchronous FIFO full state 0: Do not clear interrupt flag for asynchronous FIFO full state 1: Clear interrupt flag for asynchronous FIFO full state Bit[4]: Clear enable of interrupt flag for asynchronous FIFO not empty state 0: Do not clear interrupt flag for asynchronous FIFO not empty state 1: Clear interrupt flag for asynchronous FIFO not empty state Bit[3]: Asynchronous FIFO full interrupt enable 0: Do not output interrupt when asynchronous FIFO is full 1: Output interrupt when asynchronous FIFO is full Bit[2]: Asynchronous FIFO not empty interrupt enable 0: Do not output interrupt when asynchronous FIFO is not empty 1: Output interrupt when asynchronous FIFO is not empty Bit[1]: Reserved Bit[0]: Enable address increment for burst transmission 0: Do not enable slave address increment mode for burst transmission 1: Enable slave address increment mode for burst transmission

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table 4-22 SCCB slave registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x802A6001	SCCB_SLV_ID1	0x48	RW	Bit[7:0]: Indicates ID1 when SCCB at slave mode
0x802A6002~ 0x802A6008	RSVD	–	–	Reserved
0x802A6009	SCCB_SLV_ID2	0x46	RW	Bit[7:0]: Indicates ID2 when SCCB at slave mode
0x802A600A	SCCB_ MAILBOX_CTRL	0x00	RW	Bit[7]: SCCB hardware mailbox function enable 0: Disable SCCB hardware mailbox function 1: Enable SCCB hardware mailbox function Bit[6]: SCCB hardware mailbox work mode 0: Use SCCB hardware mailbox function when SCCB slave ID matches 1: Use SCCB hardware mailbox function when SCCB slave ID does not match Bit[5:4]: SCCB handshake mode with host 00: SCCB slave handshake with host by using full status of asynchronous FIFO 01: SCCB slave handshake with host by using empty status of asynchronous FIFO 10: SCCB slave handshake with host by using almost full status of asynchronous FIFO 11: SCCB slave handshake with host by using almost empty status of asynchronous FIFO Bit[3]: Clear enable of interrupt flag for asynchronous FIFO almost empty state 0: Do not clear interrupt flag for asynchronous FIFO almost empty state 1: Clear interrupt flag for asynchronous FIFO almost empty state Bit[2]: Clear enable of interrupt flag for asynchronous FIFO almost full state 0: Do not clear interrupt flag for asynchronous FIFO almost full state 1: Clear interrupt flag for asynchronous FIFO almost full state

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table 4-22 SCCB slave registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x802A600A				Bit[1]: Asynchronous FIFO almost empty interrupt enable 0: Do not output interrupt when asynchronous FIFO is almost empty 1: Output interrupt when asynchronous FIFO is almost empty Bit[0]: Asynchronous FIFO almost full interrupt enable 0: Do not output interrupt when asynchronous FIFO is almost full 1: Output interrupt when asynchronous FIFO is almost full
0x802A600B	FIFO_WR_ THRESHOLD	0x02	RW	Bit[7:0]: Threshold value for indicating asynchronous FIFO is almost empty When word count value is smaller than this threshold, asynchronous FIFO has almost empty status and host can write to SCCB slave
0x802A600C	FIFO_RD_ THRESHOLD	0x02	RW	Bit[7:0]: Threshold value for indicating asynchronous FIFO is almost full When word count value is larger than this threshold, asynchronous FIFO has almost full status and host cannot continue to write to SCCB slave
0x802A600D	FIFO_STATUS	–	R	Bit[7]: SCCB asynchronous FIFO almost empty interrupt flag Bit[6]: SCCB asynchronous FIFO almost full interrupt flag Bit[5]: SCCB asynchronous FIFO full interrupt flag Bit[4]: SCCB asynchronous FIFO not empty interrupt flag Bit[3]: SCCB asynchronous FIFO almost empty status Bit[2]: SCCB asynchronous FIFO almost full status Bit[1]: SCCB asynchronous FIFO full status Bit[0]: SCCB asynchronous FIFO not empty status
0x802A600E	FIFO_WR_ POINTER	–	R	Bit[7:3]: Reserved Bit[2:0]: Asynchronous FIFO write pointer
0x802A600F	FIFO_RD_ POINTER	–	R	Bit[7:3]: Reserved Bit[2:0]: Asynchronous FIFO read pointer

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table 4-22 SCCB slave registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x802A6010~ 0x802A601F	RSVD	–	–	Reserved
0x802A6020	SCCB_SLV_ID3	0x4A	RW	Bit[7:0]: Indicates the ID3 when SCCB is in slave mode
0x802A6021	SCCB_SLV_ID4	0x4C	RW	Bit[7:0]: Indicates the ID4 when SCCB is in slave mode

4.14 SCCB master control

base address: 0x80900000 SCCB_MS0

table 4-23 SCCB master0 registers[abc] (sheet 1 of 5)

address	register name	default value	R/W	description
0x80900000	SCCB CTRL 0	0x41	RW	Bit[7:6]: SCCB slave's internal address width 00: 8-bit 01: 16-bit 10: 24-bit 11: 32-bit Bit[5:4]: SCCB slave's internal data width 00: 8-bit 01: 16-bit 10: 24-bit 11: 32-bit Bit[3]: SCCB slave's ID width 0: 7-bit 1: 10-bit Bit[2]: SCCB slave stretch SCL low enable 0: Disable 1: Enable Bit[1]: SCCB slave stretch SCL low mode 0: Hardware 1: Software Bit[0]: Software control bit for stretch SCL low (hardware clear, software set) 0: Hold SCL low 1: Release SCL high

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table 4-23 SCCB master0 registers[abc] (sheet 2 of 5)

address	register name	default value	R/W	description
0x80900001	SCCB CTRL 1	0x03	RW	Bit[7:2]: Reserved Bit[1]: SCCB stop condition arbitration enable 0: Disable 1: Enable Bit[0]: SCCB data bit and ACK bit arbitration enable 0: Disable 1: Enable
0x80900002	SCCB CTRL 2	0x00	RW	Bit[7]: SCCB master re-transmit pulse Bit[6:4]: Reserved Bit[3]: RCV buffer clear pulse Bit[2]: TRN buffer's read pointer clear pulse Bit[1]: TRN buffer clear pulse Bit[0]: SCCB master abort pulse
0x80900003	SCCB CTRL 3	0xA0	RW	Bit[7]: SCCB enable 0: Disable 1: Enable Bit[6]: SCCB mode 0: Slave 1: Master Bit[5:3]: RCV buffer depth 000: 0 byte 001: 4 bytes 010: 8 bytes 011: 12 bytes 100: 16 bytes 101: 20 bytes 110: 24 bytes 111: 28 bytes Bit[2]: SCCB slave command decode mode 0: Hardware 1: Software Bit[1:0]: RCV buffer read byte 00: 3 bytes 01: 1 bytes 10: 2 bytes 11: 3 bytes
0x80900004	SCCB STAT0	–	R	Bit[7:6]: Reserved Bit[5]: TRN buffer empty Bit[4]: RCV buffer full Bit[3]: TRN buffer full Bit[2]: RCV buffer empty Bit[1]: TRN buffer almost full Bit[0]: SCCB transmission direction 0: From master to slave 1: From slave to master

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table 4-23 SCCB master0 registers[abc] (sheet 3 of 5)

address	register name	default value	R/W	description
0x80900005	SCCB STAT1	–	R	Bit[7]: SCCB slave ID match Bit[6:0]: Reserved
0x80900006	SCCB STAT2	–	R	Bit[7:2]: Reserved Bit[1]: SCCB master busy Bit[0]: Arbitration lost Software clear
0x80900007	SCCB STAT3	–	R	Bit[7]: SCCB bus busy Bit[6]: ACK stat 0: ACK received 1: NACK received Bit[5:0]: Reserved
0x80900008	SCCB ID LOW	0x20 (MS0) 0x24 (MS1)	RW	Bit[7:0]: SCCB slave ID[7:0]
0x80900009	SCCB ID HIGH	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: SCCB slave ID[9:8]
0x8090000A~ 0x8090000B	RSVD	–	–	Reserved
0x8090000C	SCCB BRTL	0xFF	RW	Bit[7:0]: Base value for SCCB master's baud rate counter[7:0]
0x8090000D	SCCB BRTH	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Base value of SCCB master's baud rate counter[11:8]
0x8090000E	SCCB DCA	0x00	RW	Bit[7:0]: SCCB master's SCL duty cycle adjustment SCL duty cycle decreases when this value increases
0x8090000F	RSVD	–	–	Reserved
0x80900010	SCCB RCVLV	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Threshold for RCV buffer's level interrupt
0x80900011	RSVD	–	–	Reserved
0x80900012	SCCB TRNLV	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Threshold for TRN buffer's level interrupt
0x80900013	RSVD	–	–	Reserved
0x80900014	SCCB WTC	0xFF	RW	Bit[7:0]: Threshold for wait out interrupt This value must not be set to 0
0x80900015~ 0x80900017	RSVD	–	–	Reserved

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table 4-23 SCCB master0 registers[abc] (sheet 4 of 5)

address	register name	default value	R/W	description
0x80900018	SCCB INTERRUPT ENABLE	0x00	RW	Bit[7]: TRN buffer level interrupt enable Bit[6]: RCV buffer level interrupt enable Bit[5]: Slave's NACK received interrupt enable Bit[4]: Slave's read request When received ID+R and match interrupt enable Bit[3]: Master's ACK received interrupt enable Bit[2]: Master's wait out interrupt enable Bit[1]: Master's arbitration interrupt enable Bit[0]: Reserved
0x80900019	RSVD	–	–	Reserved
0x8090001A	SCCB INTERRUPT STATUS	0x00	RW	Bit[7]: TRN buffer level interrupt flag Bit[6]: RCV buffer level interrupt flag Bit[5]: Slave's NACK received interrupt flag Bit[4]: Slave's read request interrupt flag Bit[3]: Master's ACK received interrupt flag Bit[2]: Master's wait out interrupt flag Bit[1]: Master's arbitration interrupt flag Bit[0]: Master's NACK received interrupt flag All flag bit is set by hardware and clear by software
0x8090001B	RSVD	–	–	Reserved
0x8090001C	ACK ID LOW	–	R	Bit[7:0]: Latest ACK slave ID[7:0]
0x8090001D	ACK ID HIGH	–	R	Bit[7:0]: Latest ACK slave ID[15:8]
0x8090001E~ 0x8090001F	RSVD	–	–	Reserved
0x80900020	RCV USEDW	–	R	Bit[7:0]: Number of used unit in RCV buffer
0x80900021	RSVD	–	–	Reserved
0x80900022	TRN USEDW	–	R	Bit[7:0]: Number of used unit in TRN buffer
0x80900023	TRN UNUSE	–	R	Bit[7:0]: Number of unused unit in TRN buffer
0x80900024	LAST ID LOW	–	R	Bit[7:0]: Last slave ID transmitted by SCCB master[7:0]
0x80900025	LAST ID HIGH	–	R	Bit[7:0]: Last slave ID transmitted by SCCB master[15:8]
0x80900026~ 0x80900027	RSVD	–	–	Reserved

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table 4-23 SCCB master0 registers[abc] (sheet 5 of 5)

address	register name	default value	R/W	description
0x80900028	LAST ADDR0	–	R	Bit[7:0]: Last byte of address transmitted by SCCB master
0x80900029	LAST ADDR1	–	R	Bit[7:0]: Address byte transmitted by SCCB master before last addr0
0x8090002A	LAST ADDR2	–	R	Bit[7:0]: Address byte transmitted by SCCB master before last addr1
0x8090002B	LAST ADDR3	–	R	Bit[7:0]: Address byte transmitted by SCCB master before last addr2
0x8090002C	LAST DATA	–	R	Bit[7:0]: Last byte of data transmitted by SCCB master
0x8090002D~ 0x8090002F	RSVD	–	–	Reserved
0x80900030	CMD STAT	–	R	Bit[7:4]: SCCB master transmission stage 0000: Idle 1000: ID transmission 0100: ADDR transmission 0010: DATA transmission 0001: Read from slave Bit[3:0]: Burst offset[11:8]
0x80900031	CMD STAT	–	R	Bit[7:0]: Burst offset[7:0]
0x80900032~ 0x80900033	SDA DELAY SEL	0x02	RW	Bit[7:6]: Reserved Bit[5:0]: Delay cycle of SDA input
0x80900034	HD TIME	0x01	RW	Bit[7:0]: Hold time of SCCB master SDA's data bit
0x80900035	SCL DELAY SEL	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Delay cycle of SCL input
0x80900036	STR LEN	0x04	RW	Bit[7:0]: Length of SCCB slave stretch SCL low

a. writing to reserved addresses or bits will induce unpredictable results, so do not change their values

b. reading reserved addresses or bits will get uncertain values

c. all registers can be accessed by both 32-bit mode and 8-bit mode

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base address: 0x80910000 SCCB_MS1

table 4-24 SCCB master1 registers[abc] (sheet 1 of 5)

address	register name	default value	R/W	description
0x80910000	SCCB CTRL 0	0x41	RW	Bit[7:6]: SCCB slave's internal address width 00: 8-bit 01: 16-bit 10: 24-bit 11: 32-bit Bit[5:4]: SCCB slave's internal data width 00: 8-bit 01: 16-bit 10: 24-bit 11: 32-bit Bit[3]: SCCB slave's ID width 0: 7-bit 1: 10-bit Bit[2]: SCCB slave stretch SCL low enable 0: Disable 1: Enable Bit[1]: SCCB slave stretch SCL low mode 0: Hardware 1: Software Bit[0]: Software control bit for stretch SCL low Hardware clear, software set 0: Hold SCL low 1: Release SCL high
0x80910001	SCCB CTRL 1	0x03	RW	Bit[7:2]: Reserved Bit[1]: SCCB STOP condition arbitration enable 0: Disable 1: Enable Bit[0]: SCCB data bit and ACK bit arbitration enable 0: Disable 1: Enable
0x80910002	SCCB CTRL 2	0x00	RW	Bit[7]: SCCB master re-transmit pulse Bit[6:4]: Reserved Bit[3]: RCV buffer clear pulse Bit[2]: TRN buffer's read pointer clear pulse Bit[1]: TRN buffer clear pulse Bit[0]: SCCB master abort pulse

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table 4-24 SCCB master1 registers[abc] (sheet 2 of 5)

address	register name	default value	R/W	description
0x80910003	SCCB CTRL 3	0xA0	RW	Bit[7]: SCCB enable 0: Disable 1: Enable Bit[6]: SCCB mode 0: Slave 1: Master Bit[5:3]: RCV buffer depth 000: 0 byte 001: 4 bytes 010: 8 bytes 011: 12 bytes 100: 16 bytes 101: 20 bytes 110: 24 bytes 111: 28 bytes Bit[2]: SCCB slave command decode mode 0: Hardware 1: Software Bit[1:0]: RCV buffer read byte 00: 3 bytes 01: 1 bytes 10: 2 bytes 11: 3 bytes
0x80910004	SCCB STAT0	–	R	Bit[7:6]: Reserved Bit[5]: TRN buffer empty Bit[4]: RCV buffer full Bit[3]: TRN buffer full Bit[2]: RCV buffer empty Bit[1]: TRN buffer almost full Bit[0]: SCCB transmission direction 0: From master to slave 1: From slave to master
0x80910005	SCCB STAT1	–	R	Bit[7]: SCCB slave ID match Bit[6:0]: Reserved
0x80910006	SCCB STAT2	–	R	Bit[7:2]: Reserved Bit[1]: SCCB master busy Bit[0]: Arbitration lost Software clear
0x80910007	SCCB STAT3	–	R	Bit[7]: SCCB bus busy Bit[6]: ACK stat 0: ACK received 1: NACK received Bit[5:0]: Reserved
0x80910008	SCCB ID LOW	0x20 (MS0) 0x24 (MS1)	RW	Bit[7:0]: SCCB slave ID[7:0]

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table 4-24 SCCB master1 registers[abc] (sheet 3 of 5)

address	register name	default value	R/W	description
0x80910009	SCCB ID HIGH	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: SCCB slave ID[9:8]
0x8091000A~ 0x8091000B	RSVD	–	–	Reserved
0x8091000C	SCCB BRTL	0xFF	RW	Bit[7:0]: Base value for SCCB master's baud rate counter[7:0]
0x8091000D	SCCB BRTH	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Base value for SCCB master's baud rate counter[15:8]
0x8091000E	SCCB DCA	0x00	RW	Bit[7:0]: SCCB master's SCL duty cycle adjustment SCL duty cycle decreases when this value increases
0x8091000F	RSVD	–	–	Reserved
0x80910010	SCCB RCVLV	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Threshold for RCV buffer's level interrupt
0x80910011	RSVD	–	–	Reserved
0x80910012	SCCB TRNLV	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Threshold for TRN buffer's level interrupt
0x80910013	RSVD	–	–	Reserved
0x80910014	SCCB WTC	0xFF	RW	Bit[7:0]: Threshold for wait out interrupt This value must not be set to 0
0x80910015~ 0x80910017	RSVD	–	–	Reserved
0x80910018	SCCB INTERRUPT ENABLE	0x00	RW	Bit[7]: TRN buffer level interrupt enable Bit[6]: RCV buffer level interrupt enable Bit[5]: Slave's NACK received interrupt enable Bit[4]: Slave's read request When received ID+R and match interrupt enable Bit[3]: Master's ACK received interrupt enable Bit[2]: Master's wait out interrupt enable Bit[1]: Master's arbitration interrupt enable Bit[0]: Reserved
0x80910019	RSVD	–	–	Reserved

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table 4-24 SCCB master1 registers[abc] (sheet 4 of 5)

address	register name	default value	R/W	description
0x8091001A	SCCB INTERRUPT STATUS	0x00	RW	Bit[7]: TRN buffer level interrupt flag Bit[6]: RCV buffer level interrupt flag Bit[5]: Slave's NACK received interrupt flag Bit[4]: Slave's read request interrupt flag Bit[3]: Master's ACK received interrupt flag Bit[2]: Master's wait out interrupt flag Bit[1]: Master's arbitration interrupt flag Bit[0]: Master's NACK received interrupt flag All flag bit is set by hardware and clear by software
0x8091001B	RSVD	–	–	Reserved
0x8091001C	ACK ID LOW	–	R	Bit[7:0]: Latest ACK slave ID[7:0]
0x8091001D	ACK ID HIGH	–	R	Bit[7:0]: Latest ACK slave ID[15:8]
0x8091001E~ 0x8091001F	RSVD	–	–	Reserved
0x80910020	RCV USEDW	–	R	Bit[7:0]: Number of used unit in RCV buffer
0x80910021	RSVD	–	–	Reserved
0x80910022	TRN USEDW	–	R	Bit[7:0]: Number of used unit in TRN buffer
0x80910023	TRN UNUSE	–	R	Bit[7:0]: Number of un used unit in TRN buffer
0x80910024	LAST ID LOW	–	R	Bit[7:0]: Last slave's ID transmitted by SCCB master[7:0]
0x80910025	LAST ID HIGH	–	R	Bit[7:0]: Last slave ID transmitted by SCCB master[15:8]
0x80910026~ 0x80910027	RSVD	–	–	Reserved
0x80910028	LAST ADDR0	–	R	Bit[7:0]: Last byte of address transmitted by SCCB master
0x80910029	LAST ADDR1	–	R	Bit[7:0]: Address byte transmitted by SCCB master before last addr0
0x8091002A	LAST ADDR2	–	R	Bit[7:0]: Address byte transmitted by SCCB master before last addr1
0x8091002B	LAST ADDR3	–	R	Bit[7:0]: Address byte transmitted by SCCB master before last addr2
0x8091002C	LAST DATA	–	R	Bit[7:0]: Last byte of data transmitted by SCCB master

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table 4-24 SCCB master1 registers[abc] (sheet 5 of 5)

address	register name	default value	R/W	description
0x8091002D~ 0x8091002F	RSVD	–	–	Reserved
0x80910030	CMD STAT	–	R	Bit[7:4]: SCCB master transmission stage 0000: Idle 1000: ID transmission 0100: ADDR transmission 0010: DATA transmission 0001: Read from slave Bit[3:0]: Burst offset[11:8]
0x80910031	CMD STAT	–	R	Bit[7:0]: Burst offset[7:0]
0x80910032~ 0x80910033	SDA DELAY SEL	0x02	RW	Bit[7:6]: Reserved Bit[5:0]: Delay cycle of SDA input
0x80910034	HD TIME	0x01	RW	Bit[7:0]: Hold time of SCCB master SDA's data bit
0x80910035	SCL DELAY SEL	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Delay cycle of SCL input
0x80910036	STR LEN	0x04	RW	Bit[7:0]: Length of SCCB slave stretch SCL low

a. writing to reserved addresses or bits will induce unpredictable results, so do not change their values

b. reading reserved addresses or bits will get uncertain values

c. all registers can be accessed by both 32-bit mode and 8-bit mode

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4.15 IDC control

base address: 0x80820000

table 4-25 IDC registers[abc] (sheet 1 of 16)

address	register name	default value	R/W	description
0x80820000	IDC CTRL 0	0x10	RW	Bit[7:6]: Reserved Bit[5]: Combine line buffer enable 0: Two independent line buffer for 2 image 1: Combine line buffers for one large image Bit[4]: Line buffer enable Enable bit for line buffer in IDC For dual image cases, this bit should be set 0: Disable line buffer 1: Enable line buffer Bit[3]: Output enable Used by full frame mode only 0: Frame output disabled 1: Frame output enabled Bit[2]: Full frame mode enable When this bit is set frame output of IDC at start of each frame can be started or stopped 0: Disabled 1: Enabled Bit[1]: Crop enable Enable bit for crop/window function in IDC 0: Disabled 1: Enabled Bit[0]: IDC enable Enable bit for input data merge and conversion function 0: Disabled 1: Enabled

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table 4-25 IDC registers[abc] (sheet 2 of 16)

address	register name	default value	R/W	description
0x80820001	IDC CTRL 1	0x00	RW	Bit[7]: Disable output embedded line flag When set this bit, output embedded line flag will be 0. Discard received and internal embedded line flag. But internal path handles embedded line flag according to the other setting. Bit[6]: Embedded line input byte invert Invert embedded line byte sequence before this data be fed into line buffer Bit[5:4]: Embedded line byte alignment select Select valid embedded data bit position in a word larger than 8 bits 00: MSB alignment 01: LSB alignment 10: Second MSB alignment 11: Reserved Bit[3]: SRAM overflow status clear Bit[2]: This bit can be set to enable in/out FIFO when at line buffer is in disabled mode. When line buffer is in disabled and needs to convert embedded line byte alignment to 32-bits, this bit should be set. Bit[1]: Embedded line as image mode enable When this bit is set, embedded line data will be treated as image data. But embedded line flag will be generated. Bit[0]: Disable input/internal embedded line flag When this bit is set, input embedded line flag will be ignored and all embedded line data will be treated as image data.

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table 4-25 IDC registers[abc] (sheet 3 of 16)

address	register name	default value	R/W	description
0x80820002	IDC CTRL 2	0x00	RW	Bit[7]: Read start independent mode enable When this bit is set, read start operation of each image will only be determined by start condition of itself. If this bit is 0, read operation will only be started when the start conditions of both image are met Bit[6:4]: Reserved Bit[3:2]: Output end of frame (EOF) source select 00: From image0 EOF 01: From image1 EOF 10: From internally generated source 0 11: From internally generated source 1 Bit[1:0]: Output SOF source select 00: From image0 SOF 01: From image1 SOF 10: From internal generated source 0 11: From internal generated source 1
0x80820003	IDC CTRL 3	0x80	RW	Bit[7]: IDC bypass enable When this bit is set, IDC internal function will be bypassed. Data will be output without processing. Only one piece of image data can be output when in bypass mode 0: Go through internal processing path 1: Bypass IDC Bit[6]: Embedded line enable If there is embedded line data at current image frame, this bit must be set Bit[5]: Swap L/VS flag Swap flag for 2x11 bits RAW Bit[4]: 2x11 bits data alignment select Select the alignment method for 2x11 bits RAW 0: LSB alignment 1: MSB alignment Bit[3]: L/VS position select for 2x11 bits RAW 0: L/VS at first word 1: L/VS at second word Bit[2:0]: Reserved
0x80820004~ 0x80820007	RSVD	–	–	Reserved

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table 4-25 IDC registers[abc] (sheet 4 of 16)

address	register name	default value	R/W	description
0x80820008	IMAGE0 CTRL0	0x00	RW	Bit[7:4]: Image0 source select Select the data input source of image0 0x0: MRX0 VC0 12-bit channel 0x1: MRX0 VC0 24-bit channel 0x2: MRX0 VC0 48-bit channel 0x3: MRX0 VC1 12-bit channel 0x4: MRX0 VC1 24-bit channel 0x5: MRX0 VC1 48-bit channel 0x6: MRX1 VC0 12-bit channel 0x7: MRX1 VC0 24-bit channel 0x8: MRX1 VC0 48-bit channel 0x9: MRX1 VC1 12-bit channel 0xA: MRX1 VC1 24-bit channel 0xB: MRX1 VC1 48-bit channel 0xC: CIF 0xD: Color bar0 0xE: Color bar1 0xF: Reserved Bit[3:2]: Reserved Bit[1]: Image0 read start enable When this bit is 0, read start condition of image0 will be ignored Bit[0]: Image0 enable Enable bit for image 0 processing path 0: Disabled 1: Enabled
0x80820009	IMAGE0 CTRL1	0x00	RW	Bit[7:6]: Reserved Bit[5:4]: Image0 embedded line data sequence select Select output byte sequence of embedded line data Bit[3:0]: Image0 input data format select 0x0: Normal/pure RAW12 0x1: 12-bit YUV422 0x2: 3x12 bits RAW 0x3: 2x12 bits RAW 0x4: 20-bit combined RAW 0x5: 16-bit compressed/tone mapped RAW 0x6: 12-bit compressed/tone mapped RAW 0x7: 2x11 bits selected/ compressed RAW 0x8~0xF: Reserved

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table 4-25 IDC registers[abc] (sheet 5 of 16)

address	register name	default value	R/W	description
0x8082000A	IMAGE0 CTRL2	0x00	RW	Bit[7]: Image0 byte invert Change input byte sequence for IDC Bit[6:4]: Image0 byte sequence select based on different format Bit[3:0]: Image0 output data format select 0x0: Normal/pure RAW12 0x1: Reserved 0x2: 3x12 bits RAW 0x3: 2x12 bits RAW 0x4: 20-bit combined RAW 0x5: 16-bit compressed/ tone-mapped RAW 0x6: 12-bit compressed/ tone-mapped RAW 0x7: 2x11 bits selected/compressed RAW 0x8~0xE: Reserved 0xF: 12-bit YUV422
0x8082000B	IMAGE0 CTRL3	0x00	RW	Bit[7]: Reserved Bit[6:4]: Image0 output 3-byte sequence select Select output data sequence of 36-bit data Bit[3:0]: Reserved
0x8082000C	IMAGE1 CTRL0	0x00	RW	Bit[7:4]: Image1 source select Select data input source of image1 0x0: MRX0 VC0 12 bit channel 0x1: MRX0 VC0 24 bit channel 0x2: MRX0 VC0 48 bit channel 0x3: MRX0 VC1 12 bit channel 0x4: MRX0 VC1 24 bit channel 0x5: MRX0 VC1 48 bit channel 0x6: MRX1 VC0 12 bit channel 0x7: MRX1 VC0 24 bit channel 0x8: MRX1 VC0 48 bit channel 0x9: MRX1 VC1 12 bit channel 0xA: MRX1 VC1 24 bit channel 0xB: MRX1 VC1 48 bit channel 0xC: CIF 0xD: Color bar0 0xE: Color bar1 0xF: Reserved Bit[3:2]: Reserved Bit[1]: Image1 read start enable When this bit is 0, read start condition of image1 will be ignored Bit[0]: Image1 enable Enable bit for image 1 processing path 0: Disabled 1: Enabled

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table 4-25 IDC registers[abc] (sheet 6 of 16)

address	register name	default value	R/W	description
0x8082000D	IMAGE1 CTRL1	0x00	RW	Bit[7:6]: Reserved Bit[5:4]: Image1 embedded line data sequence select Select the output byte sequence of embedded line data Bit[3:0]: Image1 input data format select 0x0: Normal/pure RAW12 0x1: 12-bit YUV422 0x2: 3x12 bits RAW 0x3: 2x12 bits RAW 0x4: 20-bit combined RAW 0x5: 16-bit compressed/ tone-mapped RAW 0x6: 12-bit compressed/ tone-mapped RAW 0x7: 2x11 bits selected/ compressed RAW 0x8~0xF: Reserved
0x8082000E	IMAGE1 CTRL2	0x00	RW	Bit[7]: Image1 byte invert Change input byte sequence for IDC Bit[6:4]: Image1 byte sequence select based on different format Bit[3:0]: Image1 output data format select 0x0: Normal/pure RAW12 0x1: Reserved 0x2: 3x12 bits RAW 0x3: 2x12 bits RAW 0x4: 20-bit combined RAW 0x5: 16-bit compressed/ tone-mapped RAW 0x6: 12-bit compressed/ tone-mapped RAW 0x7: 2x11 bits selected/ compressed RAW 0x8~0xE: Reserved 0xF: 12-bit YUV422
0x8082000F	IMAGE1 CTRL3	0x00	RW	Bit[7]: Reserved Bit[6:4]: Image1 output 3-byte sequence select Select output data sequence of 36-bit data Bit[3:0]: Reserved
0x80820010	IMAGE0 IHSIZE0	0x80	RW	Bit[7:0]: Image0 input horizontal size[7:0]
0x80820011	IMAGE0 IHSIZE1	0x02	RW	Bit[7:4]: Reserved Bit[3:0]: Image0 input horizontal size[11:8]
0x80820012	IMAGE0 IVSIZE0	0xE0	RW	Bit[7:0]: Image0 input vertical size[7:0]

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table 4-25 IDC registers[abc] (sheet 7 of 16)

address	register name	default value	R/W	description
0x80820013	IMAGE0 IVSIZE1	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Image0 input vertical size[10:8]
0x80820014	IMAGE1 IHSIZE0	0x80	RW	Bit[7:0]: Image1 input horizontal size[7:0]
0x80820015	IMAGE1 IHSIZE1	0x02	RW	Bit[7:4]: Reserved Bit[3:0]: Image1 input horizontal size[11:8]
0x80820016	IMAGE1 IVSIZE0	0xE0	RW	Bit[7:0]: Image1 input vertical size[7:0]
0x80820017	IMAGE1 IVSIZE1	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Image1 input vertical size[10:8]
0x80820018	IMAGE0 STARTB0	0x40	RW	Bit[7:0]: Image0 read start byte (pixel) number[7:0]
0x80820019	IMAGE0 STARTB1	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Image0 read start byte (pixel) number[10:8]
0x8082001A	IMAGE0 HBLANK0	0x80	RW	Bit[7:0]: Image0 horizontal blank cycle number[7:0]
0x8082001B	IMAGE0 HBLANK1	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Image0 horizontal blank cycle number[12:8]
0x8082001C	IMAGE1 STARTB0	0x40	RW	Bit[7:0]: Image1 read start byte (pixel) number[7:0]
0x8082001D	IMAGE1 STARTB1	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Image1 read start byte (pixel) number[10:8]
0x8082001E	IMAGE1 HBLANK0	0x80	RW	Bit[7:0]: Image1 horizontal blank cycle number[7:0]
0x8082001F	IMAGE1 HBLANK1	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Image1 horizontal blank cycle number[12:8]
0x80820020	IMAGE0 OHSIZE0	0x80	RW	Bit[7:0]: Image0 output horizontal size[7:0] This register will be used by crop/window function in IDC
0x80820021	IMAGE0 OHSIZE1	0x02	RW	Bit[7:4]: Reserved Bit[3:0]: Image0 output horizontal size[11:8] This register will be used by crop/window function in IDC
0x80820022	IMAGE0 OVSIZE0	0xE0	RW	Bit[7:0]: Image0 output vertical size[7:0] This register will be used by crop/window function in IDC

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table 4-25 IDC registers[abc] (sheet 8 of 16)

address	register name	default value	R/W	description
0x80820023	IMAGE0 OVSIZE1	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Image0 output vertical size[10:8] This register will be used by crop/window function in IDC
0x80820024	IMAGE1 OHSIZE0	0x80	RW	Bit[7:0]: Image1 output horizontal size[7:0] This register will be used by crop/window function in IDC
0x80820025	IMAGE1 OHSIZE1	0x02	RW	Bit[7:4]: Reserved Bit[3:0]: Image1 output horizontal size[11:8] This register will be used by crop/window function in IDC
0x80820026	IMAGE1 OVSIZE0	0xE0	RW	Bit[7:0]: Image1 output vertical size[7:0] This register will be used by crop/window function in IDC
0x80820027	IMAGE1 OVSIZE1	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Image1 output vertical size[10:8] This register will be used by crop/window function in IDC
0x80820028	IMAGE0 HSTART0	0x00	RW	Bit[7:0]: Image0 crop horizontal start[7:0] This register will be used by crop/window function in IDC
0x80820029	IMAGE0 HSTART1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Image0 crop horizontal start[11:8] This register will be used by crop/window function in IDC
0x8082002A	IMAGE0 VSTART0	0x00	RW	Bit[7:0]: Image0 crop vertical start[7:0] This register will be used by crop/window function in IDC
0x8082002B	IMAGE0 VSTART1	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Image0 crop vertical start[10:8] This register will be used by crop/window function in IDC
0x8082002C	IMAGE1 HSTART0	0x00	RW	Bit[7:0]: Image1 crop horizontal start[7:0] This register will be used by crop/window function in IDC
0x8082002D	IMAGE1 HSTART1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Image1 crop horizontal start[11:8] This register will be used by crop/window function in IDC
0x8082002E	IMAGE1 VSTART0	0x00	RW	Bit[7:0]: Image1 crop vertical start[7:0] This register will be used by crop/window function in IDC

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table 4-25 IDC registers[abc] (sheet 9 of 16)

address	register name	default value	R/W	description
0x8082002F	IMAGE1 VSTART1	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Image1 crop vertical start[10:8] This register will be used by crop/window function in IDC
0x80820030~ 0x8082003B	RSVD	–	–	Reserved
0x8082003C	EOF DELAY0	0x00	RW	Bit[7:0]: EOF output delay cycle control[7:0] Used to add an extra delay on output EOF signal
0x8082003D	EOF DELAY1	0x00	RW	Bit[7:0]: EOF output delay cycle control[15:8] Used to add an extra delay on output EOF signal
0x8082003E~ 0x8082003F	RSVD	–	–	Reserved
0x80820040	IMAGE0 BLC VALUE0	0x00	RW	Bit[7:0]: Image0 BLC value[7:0] Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x80820041	IMAGE0 BLC VALUE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Image0 BLC value[11:8] Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x80820042	IMAGE1 BLC VALUE0	0x00	RW	Bit[7:0]: Image1 BLC value[7:0] Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x80820043	IMAGE1 BLC VALUE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Image1 BLC value[11:8] Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x80820044	IMAGE0 LS RATIO0	0x00	RW	Bit[7:0]: Image0 LS ratio[7:0] Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x80820045	IMAGE0 LS RATIO1	0x00	RW	Bit[7:0]: Image0 LS ratio[15:8] Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x80820046	IMAGE1 LS RATIO0	0x00	RW	Bit[7:0]: Image1 LS ratio[7:0] Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x80820047	IMAGE1 LS RATIO1	0x00	RW	Bit[7:0]: Image1 LS ratio[15:8] Used by 2x11 bit RAW to 3x12 bit RAW recovery logic

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table 4-25 IDC registers[abc] (sheet 10 of 16)

address	register name	default value	R/W	description
0x80820048	IMAGE0 SVS RATIO0	0x00	RW	Bit[7:0]: Image0 SVS ratio[7:0] Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x80820049	IMAGE0 SVS RATIO1	0x00	RW	Bit[7:0]: Image0 SVS ratio[15:8] Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x8082004A	IMAGE1 SVS RATIO0	0x00	RW	Bit[7:0]: Image1 SVS ratio[7:0] Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x8082004B	IMAGE1 SVS RATIO1	0x00	RW	Bit[7:0]: Image1 SVS ratio[15:8] Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x8082004C	IMAGE0 LVS RATIO0	0x00	RW	Bit[7:0]: Image0 LVS ratio[7:0] Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x8082004D	IMAGE0 LVS RATIO1	0x00	RW	Bit[7:0]: Image0 LVS ratio[15:8] Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x8082004E	IMAGE0 LVS RATIO2	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Image0 LVS ratio[17:16] Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x8082004F	RSVD	–	–	Reserved
0x80820050	IMAGE0 INV LS RATIO0	0x00	RW	Bit[7:0]: Image0 inverted LS ratio[7:0] There is a reciprocal relationship between LS ratio and inverted LS ratio. Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x80820051	IMAGE0 INV LS RATIO1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Image0 inverted LS ratio[11:8] This is a reciprocal relationship between LS ratio and inverted LS ratio. Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x80820052	IMAGE1 INV LS RATIO0	0x00	RW	Bit[7:0]: Image1 inverted LS ratio[7:0] This is a reciprocal relationship between LS ratio and inverted LS ratio. Used by 2x11 bit RAW to 3x12 bit RAW recovery logic

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table 4-25 IDC registers[abc] (sheet 11 of 16)

address	register name	default value	R/W	description
0x80820053	IMAGE1 INV LS RATIO1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Image1 inverted LS ratio[11:8] This is a reciprocal relationship between LS ratio and inverted LS ratio. Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x80820054	IMAGE0 INV SVS RATIO0	0x00	RW	Bit[7:0]: Image0 inverted SVS ratio[7:0] This is a reciprocal relationship between SVS ratio and inverted SVS ratio. Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x80820055	IMAGE0 INV SVS RATIO1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Image0 inverted SVS ratio[11:8] This is a reciprocal relationship between SVS ratio and inverted SVS ratio. Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x80820056	IMAGE1 INV SVS RATIO0	0x00	RW	Bit[7:0]: Image1 inverted SVS ratio[7:0] This is a reciprocal relationship between SVS ratio and inverted SVS ratio. Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x80820057	IMAGE1 INV SVS RATIO1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Image1 inverted SVS ratio[11:8] This is a reciprocal relationship between SVS ratio and inverted SVS ratio. Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x80820058	IMAGE0 INV LVS RATIO0	0x00	RW	Bit[7:0]: Image0 inverted LVS ratio[7:0] This is a reciprocal relationship between LVS ratio and inverted LVS ratio. Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x80820059	IMAGE0 INV LVS RATIO1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Image0 inverted LVS ratio[11:8] This is a reciprocal relationship between LVS ratio and inverted LVS ratio. Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x8082005A	IMAGE1 INV LVS RATIO0	0x00	RW	Bit[7:0]: Image1 inverted LVS ratio[7:0] This is a reciprocal relationship between LVS ratio and inverted LVS ratio. Used by 2x11 bit RAW to 3x12 bit RAW recovery logic

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table 4-25 IDC registers[abc] (sheet 12 of 16)

address	register name	default value	R/W	description
0x8082005B	IMAGE1 INV LVS RATIO1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Image1 inverted LVS ratio[11:8] This is a reciprocal relationship between LVS ratio and inverted LVS ratio. Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x8082005C	IMAGE1 LVS RATIO0	0x00	RW	Bit[7:0]: Image1 LVS ratio[7:0] Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x8082005D	IMAGE1 LVS RATIO1	0x00	RW	Bit[7:0]: Image1 LVS ratio[15:8] Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x8082005E	IMAGE1 LVS RATIO2	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Image1 LVS ratio[17:16] Used by 2x11 bit RAW to 3x12 bit RAW recovery logic
0x8082005F	RSVD	–	–	Reserved
0x80820060	ISP IMAGE0 OHSIZE0	0x80	RW	Bit[7:0]: ISP image0 output horizontal size[7:0] Used by crop/window function in ISP module
0x80820061	ISP IMAGE0 OHSIZE1	0x02	RW	Bit[7:4]: Reserved Bit[3:0]: ISP image0 output horizontal size[11:8] Used by crop/window function in ISP module
0x80820062	ISP IMAGE0 OVSIZE0	0xE0	RW	Bit[7:0]: ISP image0 output vertical size[7:0] Used by crop/window function in ISP module
0x80820063	ISP IMAGE0 OVSIZE1	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: ISP image0 output vertical size[10:8] Used by crop/window function in ISP module
0x80820064	ISP IMAGE1 OHSIZE0	0x80	RW	Bit[7:0]: ISP image1 output horizontal size[7:0] Used by crop/window function in ISP module
0x80820065	ISP IMAGE1 OHSIZE1	0x02	RW	Bit[7:4]: Reserved Bit[3:0]: ISP image1 output horizontal size[11:8]
0x80820066	ISP IMAGE1 OVSIZE0	0xE0	RW	Bit[7:0]: ISP image1 output vertical size[7:0] Used by crop/window function in ISP module

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table 4-25 IDC registers[abc] (sheet 13 of 16)

address	register name	default value	R/W	description
0x80820067	ISP IMAGE1 OVSIZE1	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: ISP image1 output vertical size[10:8] Used by crop/window function in ISP module
0x80820068	ISP IMAGE0 HSTART0	0x00	RW	Bit[7:0]: ISP image0 crop horizontal start[7:0] Used by crop/window function in ISP module
0x80820069	ISP IMAGE0 HSTART1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: ISP image0 crop horizontal start[11:8] Used by crop/window function in ISP module
0x8082006A	ISP IMAGE0 VSTART0	0x00	RW	Bit[7:0]: ISP mage0 crop vertical start[7:0] Used by crop/window function in ISP module
0x8082006B	ISP IMAGE0 VSTART1	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: ISP image0 crop vertical start[10:8] Used by crop/window function in ISP module
0x8082006C	ISP IMAGE1 HSTART0	0x00	RW	Bit[7:0]: ISP image1 crop horizontal start[7:0] Used by crop/window function in ISP module
0x8082006D	ISP IMAGE1 HSTART1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: ISP image1 crop horizontal start[11:8] Used by crop/window function in ISP module
0x8082006E	ISP IMAGE1 VSTART0	0x00	RW	Bit[7:0]: ISP image1 crop vertical start[7:0] Used by crop/window function in ISP module
0x8082006F	ISP IMAGE1 VSTART1	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: ISP image1 crop vertical start[10:8] Used by crop/window function in ISP module

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table 4-25 IDC registers[abc] (sheet 14 of 16)

address	register name	default value	R/W	description
0x80820070	ISP IMAGE0 FORMAT0	0x00	RW	Bit[7:4]: ISP image0 output tone-mapped format These bits indicate format of ISP output tone-mapped data for ODS module 0x0: 12 bit tone-mapped RAW 0x1: 16 bit tone-mapped RAW 0x2: 20 bit tone-mapped RAW 0x3~0xF: Reserved Bit[3:0]: ISP image0 input data format This is intended for ISP module using the format definition listed as follows: 0x0: Three exposure mode 0x1: LS exposure mode 0x2: LVS exposure mode 0x3: L exposure mode 0x4: Traffic exposure mode 0x5~0xF: Reserved

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table 4-25 IDC registers[abc] (sheet 15 of 16)

address	register name	default value	R/W	description
0x80820071	ISP IMAGE0 FORMAT1	0x00	RW	Bit[7:4]: ISP image0 output YUV format These bits are used in ISP module, and indicate data format of ISP YUV output channel 0x0: No output 0x1: 8-bit YUV422 0x2: 10-bit YUV422 0x3: 12-bit YUV422 0x4~0x5: RGB888 with simple bit clamp operation 0x6~0x7: RGB888 with transform directly from YUV data 0x8~0xF: Reserved Bit[3:0]: ISP image0 and image1 output RAW format These bits are used in ISP module and indicate data format of ISP RAW output channel 0x0: Image0 and image1 no output 0x1: Image0 output in 3x12 bits RAW (non-combined) format and image1 no output 0x2: Image0 no output, image1 output in 3x12 bits RAW (non-combined) format 0x3: Image0 and image1 output in 3x12 bit RAW (non-combined) format 0x4: No output 0x5: Image0 output in 12-bit/20-bit tone-mapped RAW format and image1 no output 0x6: Image0 no output, image1 output in 12-bit/20-bit tone-mapped RAW format 0x7: Image0 and image1 output in 12-bit/20-bit tone-mapped RAW format 0x8: No output 0x9: Image0 output in linear RAW12 format and image1 no output 0xA: Image0 no output, image1 output in linear RAW12 format 0xB: Image0 and image1 output in linear RAW12 format 0xC: No output 0xD: Image0 output in Y format and image1 no output

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table 4-25 IDC registers[abc] (sheet 16 of 16)

address	register name	default value	R/W	description
0x80820071				0xE: Image0 no output, image1 output in Y format 0xF: Image0 and image1 output in Y format
0x80820072~ 0x80820073	RSVD	–	–	Reserved
0x80820074	ISP IMAGE1 FORMAT0	0x00	RW	Bit[7:4]: ISP image1 output tone-mapped format These bits indicate format of ISP output tone-mapped data for ODS module 0x0: 12-bit tone-mapped RAW 0x1: 16-bit tone-mapped RAW 0x2: 20-bit tone-mapped RAW 0x3~0xF: Reserved Bit[3:0]: ISP image1 input data format These bits are intended for ISP module using the format definition listed as follows: 0x0: 3-exposure mode 0x1: LS exposure mode 0x2: LVS exposure mode 0x3: L exposure mode 0x4: Traffic exposure mode 0x5~0xF: Reserved
0x80820075	ISP IMAGE1 FORMAT1	0x00	RW	Bit[7:4]: ISP image1 output YUV format These bits are for ISP module use and indicate data format of ISP YUV output channel 0x0: No output 0x1: 8-bit YUV422 0x2: 10-bit YUV422 0x3: 12-bit YUV422 0x4~0x5: RGB888 with simple bit clamp operation 0x6~0x7: RGB888 with transform directly from YUV data 0x8~0xF: Reserved Bit[3:0]: Reserved
0x80820076~ 0x808200FF	RSVD	–	–	Reserved

a. writing to reserved addresses or bits will induce unpredictable result, so do not change their values

b. reading reserved addresses or bits will get uncertain values

c. all registers can be accessed by both 32-bit mode and 8-bit mode

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4.16 temperature sensor control

base address: 0x80260000

table 4-26 temperature sensor registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x80260000	R_TPM_SLOPE_H	0x4D	RW	Bit[7:0]: Slope(A)[15:8] Temperature = A × average + B
0x80260001	R_TPM_SLOPE_L	0x8F	RW	Bit[7:0]: Slope(A)[7:0]
0x80260002	R_TPM_OFFSET_3	0xBA	RW	Bit[7:0]: Offset(B)[31:24]
0x80260003	R_TPM_OFFSET_2	0x4C	RW	Bit[7:0]: Offset(B)[23:16]
0x80260004	R_TPM_OFFSET_1	0x00	RW	Bit[7:0]: Offset(B)[15:8]
0x80260005	R_TPM_OFFSET_0	0x00	RW	Bit[7:0]: Offset(B)[7:0]
0x80260006	R_DIV	0x0C	RW	Bit[7:0]: This byte indicates clock dividing maximum counter Clock counter based on input system clock and generates a clock to analog temperature sensor which will give out a temperature value according this clock. Default value is based on the crystal clock (24MHz)
0x80260007	R_CNT_BIT	0x07	RW	Bit[7:0]: Option to adjust sampling time 000: 256 output clock periods 001: 512 output clock periods 010: 1024 output clock periods 011: 2048 output clock periods 100: 4096 output clock periods 101: 8192 output clock periods 110: 16384 output clock periods 111: 32768 output clock periods
0x80260008	R_CLK_RE	0x00	RW	Bit[7:0]: Reverse output clock to analog part select 0: No reverse 1: Reverse
0x80260009	R_STALL	0x00	RW	Bit[7:0]: Stall option When set to 1 enabled, whole calculation process will be stalled

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table 4-26 temperature sensor registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x8026000A	R_OTP_CTRL_EN	0x00	RW	Bit[7:0]: There are 2 options to load slope (A) and offset (B) Default option (0) is to load the registers from internal modules When set to 1, can be changed to external inputs from OTP 0: Load from internal registers 1: Load from OTP registers
0x8026000B	R_SOF_UPDATE_EN	0x00	RW	Bit[7:0]: Temperature read out value be updated for every input frame When set to 1, read out temperature value will be updated every frame
0x8026000C	R_SHIFT_BIT	0x01	RW	Bit[4:0]: In offset bits, there are 1 signed bit, 9 integer bits, and rest of bits are the decimal part If more space is needed for integer part, integer part can be shifted to decimal part. If this byte is 0, then no bit will be shifted. Default value indicates 10-bit integer part.
0x8026000D	R_PD_TPM_SNR	0x00	RW	Bit[7:0]: Option to power down temperature sensor 0: Do not power down 1: Power down
0x80260012	R_TPM_F_EN	0x00	RW	Bit[7:0]: When bit r_sof_update_en is not set, this bit will be used to manually update read out temperature value
0x80260013	R_TPM_INT_RDOUT	–	R	Bit[7:0]: Read out integer part of output temperature at any time
0x80260014	R_TPM_DEC_RDOUT	–	R	Bit[7:0]: Read out decimal part of output temperature at any time
0x80260015	R_TPM_INT	–	R	Bit[7:0]: Internal update of temperature, integer part at the start of every frame
0x80260016	R_TPM_DEC	–	R	Bit[7:0]: Internal update of temperature, decimal part at the start of every frame

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4.17 ODS control

The ODS is a MUX to select video stream from the ISP or IDC directly.

base address: 0x8029D000

table 4-27 ODS registers[ab] (sheet 1 of 3)

address	register name	default value	R/W	description
0x8029D000	ODS CTRL 0 RW	0x00	RW	Bit[7:6]: EOF select Select end-of-frame (EOF) source for downstream data path module 00: According to bypass enable, bypass0 or bypass1 is enabled and it will be from IDC; else, from ISP 01: From ISP EOF 10: From IDC EOF 11: Reserved Bit[5:4]: SOF select Select start-of-frame (SOF) source for downstream data path module 00: According to bypass enable, bypass0 or bypass1 is enabled and it will be from IDC; else, from ISP 01: From ISP SOF 10: From IDC SOF 11: Reserved Bit[3]: Full frame mode output enable 0: Frame output disabled 1: Frame output enabled Bit[2]: Full frame mode enable When this bit is set, output frame of ODS will be in whole frame mode 0: Normal output mode without control 1: Full frame output mode Bit[1]: Bypass1 Bypass IDC data to YUV channel 0: Disabled 1: Enabled Bit[0]: Bypass0 Bypass IDC data to RAW channel 0: Disabled 1: Enabled

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table 4-27 ODS registers[ab] (sheet 2 of 3)

address	register name	default value	R/W	description
0x8029D001	ODS CTRL 1	0x00	RW	Bit[7:2]: Reserved Bit[1]: Clamp enable Used to clamp output value of image data 0: Disabled 1: Enabled Bit[0]: RGB565 enable When set, RGB888 data will be converted to RGB565 for downstream use
0x8029D002	RAW MAX V0 LOW	0x00	RW	Bit[7:0]: Max value of output RAW data[7:0] For data clamp function use
0x8029D003	RAW MAX V0 HIGH	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Max value of output RAW data[11:8] For data clamp function use
0x8029D004	RAW MAX V1 LOW	0x00	RW	Bit[7:0]: Max value of output RAW data[19:12] For data clamp function use
0x8029D005	RAW MAX V1 HIGH	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Max value of output RAW data[23:20] For data clamp function use
0x8029D006	RAW MAX V2 LOW	0x00	RW	Bit[7:0]: Max value of output RAW data[31:24] For data clamp function use
0x8029D007	RAW MAX V2 HIGH	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Max value of output RAW data[35:32] For data clamp function use
0x8029D008	RAW MIN V0 LOW	0x00	RW	Bit[7:0]: Min value of output RAW data[7:0] For data clamp function use
0x8029D009	RAW MIN V0 HIGH	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Min value of output RAW data[11:8] For data clamp function use
0x8029D00A	RAW MIN V1 LOW	0x00	RW	Bit[7:0]: Min value of output RAW data[19:12] For data clamp function use
0x8029D00B	RAW MIN V1 HIGH	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Min value of output RAW data[23:20] For data clamp function use
0x8029D00C	RAW MIN V2 LOW	0x00	RW	Bit[7:0]: Min value of output RAW data[31:24] For data clamp function use
0x8029D00D	RAW MIN V2 HIGH	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Min value of output RAW data[35:32] For data clamp function use

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table 4-27 ODS registers[ab] (sheet 3 of 3)

address	register name	default value	R/W	description
0x8029D00E~ 0x8029D00F	RSVD	–	–	Reserved
0x8029D010	YUV MAX V0 LOW	0x00	RW	Bit[7:0]: Max value of output YUV data[7:0] For data clamp function use
0x8029D011	YUV MAX V0 HIGH	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Max value of output YUV data[11:8] For data clamp function use
0x8029D012	YUV MAX V1 LOW	0x00	RW	Bit[7:0]: Max value of output YUV data[19:12] For data clamp function use
0x8029D013	YUV MAX V1 HIGH	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Max value of output YUV data[23:20] For data clamp function use
0x8029D014	YUV MIN V0 LOW	0x00	RW	Bit[7:0]: Min value of output YUV data[7:0] For data clamp function use
0x8029D015	YUV MIN V0 HIGH	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Min value of output YUV data[11:8] For data clamp function use
0x8029D016	YUV MIN V1 LOW	0x00	RW	Bit[7:0]: Min value of output YUV data[19:12] For data clamp function use
0x8029D017	YUV MIN V1 HIGH	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Min value of output YUV data[23:20] For data clamp function use

a. writing to reserved addresses or bits will induce unpredictable result, so do not change their values

b. reading reserved address or bits will get uncertain values

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4.18 system control (SC) control

base address: 0x80800000

table 4-28 SC registers[abc] (sheet 1 of 31)

address	register name	default value	R/W	description
0x80800000~ 0x8080000F	RSVD	–	–	Reserved
0x80800010	SC RESET0	0x00	RW	Bit[7]: ROM software reset (active high) Bit[6]: SRAM software reset (active high) Bit[5]: SCCB master1 software reset (active high) Bit[4]: SCCB master0 software reset (active high) Bit[3]: Reserved (do not write 0x01 to this bit) Bit[2]: RISC software reset (active high) Bit[1:0]: Reserved (do not write 0x01 to these bits)
0x80800011	SC RESET1	0x00	RW	Bit[7]: MIPI TX software reset (active high) Bit[6]: MIPI RX1 out software reset (active high) Bit[5]: MIPI RX0 out software reset (active high) Bit[4]: DMA software reset (active high) Bit[3]: GPIO software reset (active high) Bit[2]: SCCB software reset (active high) Bit[1]: MBIST software reset (active high) Bit[0]: JTAG software reset (active high)
0x80800012	SC RESET2	0xB0	RW	Bit[7]: VFIFO pclk domain software reset (active high) Bit[6]: 4-wire serial interface software reset (active high) Bit[5]: MRX1 PHY software reset (active high) Bit[4]: MRX0 PHY software reset (active high) Bit[3]: VFIFO sclk domain software reset (active high) Bit[2]: ISP software reset (active high) Bit[1]: DVP software reset (active high) Bit[0]: CIF software reset (active high)
0x80800013	SC RESET3	0xF7	RW	Bit[7]: Image path software reset (active high) Bit[6]: MRX1 PCLK domain software reset (active high) Bit[5]: MRX0 PCLK domain software reset (active high) Bit[4]: IDC software reset (active high) Bit[3]: OTP software reset (active high) Bit[2]: Reserved Bit[1]: Color bar software reset (active high) Bit[0]: MTX PHY software reset (active high)

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table 4-28 SC registers[abc] (sheet 2 of 31)

address	register name	default value	R/W	description
0x80800014	SC RESET4	0x7E	RW	Bit[7]: TPM software reset (active high) Bit[6]: VSGEN software reset (active high) Bit[5]: EMBL software reset (active high) Bit[4]: ODS software reset (active high) Bit[3]: UART2 software reset (active high) Bit[2]: UART1 software reset (active high) Bit[1]: UART0 software reset (active high) Bit[0]: UART software reset (active high)
0x80800015	SC RESET5	0x01	RW	Bit[7:1]: Debug mode Bit[0]: DMAS software reset (active high) Used by crop/window function in ISP module
0x80800016	SC RESET6	0x00	RW	Bit[7]: Peripheral register reset2 (active high) Bit[6]: Peripheral register reset1 (active high) Bit[5]: Peripheral register reset0 (active high) Bit[4]: IDC register reset (active high) Bit[3]: Image path register reset2 (active high) Bit[2]: Image path register reset1 (active high) Bit[1]: Image path register reset0 (active high) Bit[0]: ISP register reset (active high)
0x80800017	SC RESET7	0x00	RW	Bit[7]: Reserved Bit[6]: Watch dog reset system enable 0: Watch dog reset RISC only 1: Watch dog reset whole system Bit[5]: PLL2 reset (active high) Bit[4]: PLL1 reset (active high) Bit[3]: MRX and BO bias reset (active high) Bit[2]: DVP SYNC reset (active high) Bit[1]: Debug mode Bit[0]: Peripheral register reset3 (active high)
0x80800018	SC CLOCK0	0xFE	RW	Bit[7]: Clock enable bit for ROM 0: Clock off 1: Clock on Bit[6]: Clock enable bit for PRAM 0: Clock off 1: Clock on Bit[5]: Clock enable bit for SCCB master1 0: Clock off 1: Clock on Bit[4]: Clock enable bit for SCCB master0 0: Clock off 1: Clock on Bit[3]: Reserved (do not write 0x00 to this bit) Bit[2]: Clock enable bit for RISC 0: Clock off 1: Clock on Bit[1:0]: Reserved (do not write 0x00 to these bits)

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table 4-28 SC registers[abc] (sheet 3 of 31)

address	register name	default value	R/W	description
0x80800019	SC CLOCK1	0x0F	RW	Bit[7]: Clock enable bit for MTX pixel clock 0: Clock off 1: Clock on Bit[6]: Clock enable bit for MRX0 system clock 0: Clock off 1: Clock on Bit[5]: Clock enable bit for MRX1 system clock 0: Clock off 1: Clock on Bit[4]: Clock enable bit for DMA 0: Clock off 1: Clock on Bit[3]: Clock enable bit for GPIO 0: Clock off 1: Clock on Bit[2]: Clock enable bit for SCCB slave 0: Clock off 1: Clock on Bit[1]: Clock enable bit for MBIST 0: Clock off 1: Clock on Bit[0]: Clock enable bit for JTAG 0: Clock off 1: Clock on
0x8080001A	SC CLOCK2	0x40	RW	Bit[7]: Clock enable bit for VFIFO pclk 0: Clock off 1: Clock on Bit[6]: Clock enable bit for 4-wire serial interface 0: Clock off 1: Clock on Bit[5]: Clock enable bit for MRX1 pclk 0: Clock off 1: Clock on Bit[4]: Clock enable bit for MRX0 pclk 0: Clock off 1: Clock on Bit[3]: Clock enable bit for VFIFO sclk 0: Clock off 1: Clock on Bit[2]: Clock enable bit for ISP 0: Clock off 1: Clock on Bit[1]: Clock enable bit for DVP 0: Clock off 1: Clock on Bit[0]: Clock enable bit for CIF 0: Clock off 1: Clock on

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table 4-28 SC registers[abc] (sheet 4 of 31)

address	register name	default value	R/W	description
0x8080001B	SC CLOCK3	0x08	RW	Bit[7]: Clock enable bit for image path 0: Clock off 1: Clock on Bit[6]: Clock enable bit for CCLK1 0: Clock off 1: Clock on Bit[5]: Clock enable bit for CCLK0 0: Clock off 1: Clock on Bit[4]: Clock enable bit for IDC 0: Clock off 1: Clock on Bit[3]: Clock enable bit for OTP 0: Clock off 1: Clock on Bit[2]: Debug mode Bit[1]: Clock enable bit for color bar0 and 1 0: Clock off 1: Clock on Bit[0]: Clock enable bit for color bar FTX 0: Clock off 1: Clock on
0x8080001C	SC CLOCK4	0x81	RW	Bit[7]: Clock enable bit for TPM 0: Clock off 1: Clock on Bit[6]: Clock enable bit for VSGEN 0: Clock off 1: Clock on Bit[5]: Clock enable bit for EMBL 0: Clock off 1: Clock on Bit[4]: Clock enable bit for ODS 0: Clock off 1: Clock on Bit[3]: Clock enable bit for UART2 0: Clock off 1: Clock on Bit[2]: Clock enable bit for UART1 0: Clock off 1: Clock on Bit[1]: Clock enable bit for UART0 0: Clock off 1: Clock on Bit[0]: Clock enable bit for UART 0: Clock off 1: Clock on

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table 4-28 SC registers[abc] (sheet 5 of 31)

address	register name	default value	R/W	description
0x8080001D	SC CLOCK5	0x02	RW	Bit[7:1]: Debug mode Bit[0]: Clock enable bit for DMAS 0: Clock off 1: Clock on
0x8080001E	RSVD	–	–	Reserved
0x8080001F	SC CLOCK7	0x00	RW	Bit[7]: MRX1 pixel clock invert 0: Normal phase 1: Inverted phase Bit[6]: MRX0 pixel clock invert 0: Normal phase 1: Inverted phase Bit[5]: MRX1 pixel clock source 0: From MRX PHY1 1: From MRX PHY0 Bit[4]: MRX0 pixel clock source 0: From MRX PHY0 1: From MRX PHY1 Bit[3:2]: Debug mode Bit[1]: CCLK1 output enable 0: Do not output on CCLK1 pad 1: Output CCLK1 on CCLK1 pad Bit[0]: CCLK0 output enable 0: Do not output on CCLK0 pad 1: Output CCLK1 on CCLK0 pad
0x80800020	SC CLOCK 8	0x04	RW	Bit[7:0]: Divider ratio for system clock divider
0x80800021	SC CLOCK 9	0x00	RW	Bit[7:5]: Debug mode Bit[4]: System clock change set Only when this bit is set, setting changing on system clock is valid; otherwise, no change on system clock Bit[3:2]: System clock source select 00: From pad clock 01: From system clock divider 10: From pad clock 11: From RDS divider Bit[1:0]: System clock divider source select 00: From pad clock 01: From pad clock 10: From PLL1 clock0 11: From PLL1 clock1
0x80800022	SC CLOCK A	0x04	RW	Bit[7:0]: Divider ratio for ISP clock divider

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table 4-28 SC registers[abc] (sheet 6 of 31)

address	register name	default value	R/W	description
0x80800023	SC CLOCK B	0x00	RW	Bit[7]: Debug mode Bit[6]: DVP/VFIFO pclk select 0: From MTX clock 1: From ISP clock Bit[5:3]: Debug mode Bit[2]: ISP clock source select 0: From pad clock 1: From ISP clock divider Bit[1:0]: ISP clock divider source select 00: From pad clock 01: From pad clock 10: From PLL1 clock0 11: From PLL1 clock1
0x80800024	SC CLOCK C	0x02	RW	Bit[7:0]: Divider ratio for CCLK0 clock divider
0x80800025	SC CLOCK D	0x00	RW	Bit[7:5]: Debug mode Bit[4]: CCLK0 clock change set (reserved) Bit[3]: CCLK0 divider source select2 PLL select 0: From PLL1 1: From PLL2 clock1 Bit[2]: CCLK0 source select 0: From pad clock 1: From CCLK0 clock divider Bit[1]: CCLK0 divider source select1 0: From pad clock 1: From PLL1 or PLL2 clock Bit[0]: CCLK0 divider source select0 PLL1 clock select 0: From pad clock 1: From PLL1 or PLL2 clock
0x80800026	SC CLOCK E	0x02	RW	Bit[7:0]: Divider ratio for CCLK1 clock divider
0x80800027	SC CLOCK F	0x00	RW	Bit[7:4]: Debug mode Bit[3]: CCLK1 divider source select2 PLL select 0: From PLL1 1: From PLL2 clock1 Bit[2]: CCLK1 source select 0: From pad clock 1: From CCLK0 clock divider Bit[1]: CCLK1 divider source select1 0: From pad clock 1: From PLL1 or PLL2 clock Bit[0]: CCLK1 divider source select0 PLL1 clock select 0: From PLL1 clock0 1: From PLL1 clock1
0x80800028	SC CLOCK 10	0x04	RW	Bit[7:0]: Divider ratio for MIPI TX clock divider

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table 4-28 SC registers[abc] (sheet 7 of 31)

address	register name	default value	R/W	description
0x80800029	SC CLOCK 11	0x00	RW	Bit[7:3]: Debug mode Bit[2]: MTX clock source select 0: From pad clock 1: From MTX clock divider Bit[1]: MTX clock divider source select 0: From pad clock 1: From PLL2 clock1 Bit[0]: Debug mode
0x8080002A	SC CLOCK 12	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Divider ratio for RDS clock divider 00: /1 01: /2 10: /4 11: Debug mode
0x8080002B	SC CLOCK 13	0x00	RW	Bit[7:5]: Debug mode Bit[4]: RISC clock change set Only when this bit is set, setting changing on RISC clock is valid; otherwise, no change on RISC clock Bit[3]: Debug mode Bit[2]: RISC clock source select 0: From system clock divider 1: From RDS clock divider Bit[1:0]: Debug mode
0x8080002C~ 0x8080002F	DEBUG	–	–	Debug Mode

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table 4-28 SC registers[abc] (sheet 8 of 31)

address	register name	default value	R/W	description
0x80800030	SC POWER 0	0x00	RW	Bit[7]: Analog power down mode When this bit is set, analog module will be controlled by hardware suspend sequence. When this bit is 0, analog module can only power down by register. Bit[6]: Reserved Bit[5]: Power down enable If this bit is set, auto suspend sequence will generate power down signal for PD regulator and analog module Bit[4]: Disable OSC enable If this bit is set, auto suspend sequence will generate disable OSC control signal Bit[3]: Software suspend enable If this bit is set, suspend sequence will just generate a suspend interrupt and real suspend operation needs a trigger pulse or write manual software suspend registers. If auto hardware suspend mode is desired, set to 0 Bit[2]: Suspend clear enable If this bit is set, all registers including special boot registers will be cleared when resume 0: Normal suspend mode. Some special registers' values will be maintained during suspend mode RISC boot from SRAM or ROM can be selected 1: Special suspend mode. All registers' values will be cleared the restart sequence is similar to power on Bit[1]: Suspend enable PWDN pin signal will only be valid for internal suspend logic when this bit is set Bit[0]: Idle mode enable When this bit is set, only bus clock will be enabled

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table 4-28 SC registers[abc] (sheet 9 of 31)

address	register name	default value	R/W	description
0x80800031	SC POWER1	0x00	RW	The following bits can be used to control the power down function manually. Since there is a strict sequence requirement for these operations, please do not use the following bits for normal use case Bit[7:4]: Reserved Bit[3]: Manual software isolation enable 0: ISO disabled 1: ISO enabled Bit[2]: Manual software regulator switch disable 0: Switch enabled 1: Switch disabled Bit[1]: Manual software power down 0: Power ON 1: Power down Bit[0]: Manual software disable OSC 0: OSC input enabled 1: OSC input disabled
0x80800032	SC POWER2	0x00	RW	Bit[7:2]: Reserved Bit[1]: Clear bit for suspend individual/reserved interrupt Reserved for backup interrupt only. Do not use this in normal use case Bit[0]: Enable bit for suspend individual/ reserved interrupt Reserved for backup interrupt only. Do not use this in normal case
0x80800033	RSVD	–	–	Reserved
0x80800034	SC POWER4	0x00	RW	Bit[7:1]: Reserved Bit[0]: Auto software suspend start bit Writing 1 to this bit will generate a suspend start pulse for auto software suspend mode. Suspend sequence will be executed after writing to this bit. This bit should be set only after RISC response finishes
0x80800035~ 0x8080003F	RSVD	–	–	Reserved

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table 4-28 SC registers[abc] (sheet 10 of 31)

address	register name	default value	R/W	description
0x80800040	SC BOOT0	0x00	RW	Bit[7:2]: Reserved Bit[1]: Manual load bit for RISC boot setting bits When loading RISC boot address select option without RISC reset is needed, this bit can be used This is intended for special use case. Bit[0]: RISC pulse reset When writing 1 to this bit, a reset pulse will be generated for RISC and boot settings will be reloaded at the same time. This bit is intended for normal reboot operation which is controlled by firmware.
0x80800041~ 0x80800043	RSVD	–	–	Reserved
0x80800044	SC BOOT S0	0x06	RW	Bit[7:6]: Boot select pins read value Bit[5:4]: Dummy bits for firmware use Bit[3:1]: Reserved Bit[0]: Select RISC boot memory This bit will be only valid when RISC reset or using load manually 0: ROM 1: SRAM
0x80800045	SC BOOT S1	0x00	RW	Bit[7:6]: Reserved Bit[5:4]: Read value for SCCBID1 and SCCBID0 Bit[3:0]: Reserved
0x80800046	SC BOOT S2	0x00	RW	Bit[7:0]: Dummy bits for firmware use

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table 4-28 SC registers[abc] (sheet 11 of 31)

address	register name	default value	R/W	description
0x80800047	SC BOOT S3	0x00	RW	Bit[7]: System maintain PD modules configuration registers when resume Available when PD is in power down mode 0: Reset PD register values 1: Retain PD register values Bit[6]: System maintains PK module's configuration registers when resume 0: Reset PK/SC register values 1: Retain PK/SC register values Bit[5]: System maintains GPIO module's configuration registers when resume 0: Reset GPIO register values 1: Retain GPIO register values Bit[4]: Reserved Bit[3]: System maintains PD module's logic status or not when resume Not available when PD is in power down mode 0: Reset PD logic status 1: Retain PD logic status Bit[2]: System keep PK/SC module's logic status when resume 0: Reset PK/SC logic status 1: Retain PK/SC logic status Bit[1:0]: Reserved
0x80800048~ 0x8080004F	RSVD	–	–	Reserved

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table 4-28 SC registers[abc] (sheet 12 of 31)

address	register name	default value	R/W	description
0x80800050	GPIO SEL0	0x00	RW	Bit[7:6]: Reserved for SCCBID pad GPIO function Bit[5]: GPIO select for pad GPIO5 Enable bit for pad GPIO5 GPIO function 0: Normal function 1: Pad controlled by GPIO Bit[4]: GPIO select for pad GPIO4 Enable bit for pad GPIO4 GPIO function 0: Normal function 1: Pad controlled by GPIO Bit[3]: GPIO select for pad GPIO3 Enable bit for pad GPIO3 GPIO function 0: Normal function 1: Pad controlled by GPIO Bit[2]: GPIO select for pad GPIO2 Enable bit for pad GPIO2 GPIO function 0: Normal function 1: Pad controlled by GPIO Bit[1]: GPIO select for pad GPIO1 Enable bit for pad GPIO1 GPIO function 0: Normal function 1: Pad controlled by GPIO Bit[0]: GPIO select for pad GPIO0 Enable bit for pad GPIO0 GPIO function 0: Normal function 1: Pad controlled by GPIO
0x80800051	GPIO SEL1	0x00	RW	Bit[7:2]: Debug mode Bit[1]: GPIO select for pad SPWDN1 Enable bit for pad SPWDN1 GPIO function 0: Debug mode 1: Pad controlled by GPIO Bit[0]: GPIO select for pad SPWDN0 Enable bit for pad SPWDN0 GPIO function 0: Debug mode 1: Pad controlled by GPIO
0x80800052~ 0x80800053	RSVD	–	–	Reserved

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table 4-28 SC registers[abc] (sheet 13 of 31)

address	register name	default value	R/W	description
0x80800054	GPIO DIRECTION0	0x00	RW	Bit[7:6]: Reserved for SCCBID pad GPIO function Bit[5]: Direction select bit for pad GPIO5 GPIO function 0: Input 1: Output Bit[4]: Direction select bit for pad GPIO4 GPIO function 0: Input 1: Output Bit[3]: Direction select bit for pad GPIO3 GPIO function 0: Input 1: Output Bit[2]: Direction select bit for pad GPIO2 GPIO function 0: Input 1: Output Bit[1]: Direction select bit for pad GPIO1 GPIO function 0: Input 1: Output Bit[0]: Direction select bit for pad GPIO0 GPIO function 0: Input 1: Output
0x80800055	GPIO DIRECTION1	0x00	RW	Bit[7:2]: Debug mode Bit[1]: Direction select bit for pad SPWDN1 GPIO function 0: Input 1: Output Bit[0]: Direction select bit for pad SPWDN0 GPIO function 0: Input 1: Output
0x80800056~ 0x80800057	RSVD	–	–	Reserved

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table 4-28 SC registers[abc] (sheet 14 of 31)

address	register name	default value	R/W	description
0x80800058	GPIO OUTPUT VALUE0	0x00	RW	Bit[7:6]: Reserved for SCCBID pad GPIO function Bit[5]: Output value for pad GPIO5 GPIO output function Bit[4]: Output value for pad GPIO4 GPIO output function Bit[3]: Output value for pad GPIO3 GPIO output function Bit[2]: Output value for pad GPIO2 GPIO output function Bit[1]: Output value for pad GPIO1 GPIO output function Bit[0]: Output value for pad GPIO0 GPIO output function
0x80800059	GPIO OUTPUT VALUE1	0x00	RW	Bit[7:2]: Reserved Bit[1]: Output value for pad SPWDN1 GPIO output function Bit[0]: Output value for pad SPWDN0 GPIO output function
0x8080005A~ 0x8080005B	RSVD	–	–	Reserved
0x8080005C	GPIO INPUT VALUE0	–	R	Bit[7:6]: Reserved for SCCBID pad GPIO function Bit[5]: Input value for pad GPIO5 GPIO input function Bit[4]: Input value for pad GPIO4 GPIO input function Bit[3]: Input value for pad GPIO3 GPIO input function Bit[2]: Input value for pad GPIO2 GPIO input function Bit[1]: Input value for pad GPIO1 GPIO input function Bit[0]: Input value for pad GPIO0 GPIO input function
0x8080005D	GPIO INPUT VALUE1	–	R	Bit[7:2]: Debug mode Bit[1]: Input value for pad SPWDN1 GPIO input function Bit[0]: Input value for pad SPWDN0 GPIO input function
0x8080005E~ 0x8080005F	RSVD	–	–	Reserved

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table 4-28 SC registers[abc] (sheet 15 of 31)

address	register name	default value	R/W	description
0x80800060	GPIO CTRL0	0xFF	RW	Bit[7:6]: Reserved for SCCBID GPIO pad function Bit[5]: Enable GPIO input debounce function for GPIO5 pad Bit[4]: Enable GPIO input debounce function for GPIO4 pad Bit[3]: Enable GPIO input debounce function for GPIO3 pad Bit[2]: Enable GPIO input debounce function for GPIO2 pad Bit[1]: Enable GPIO input debounce function for GPIO1 pad Bit[0]: Enable GPIO input debounce function for GPIO0 pad
0x80800061~ 0x80800063	RSVD	–	–	Reserved
0x80800064	GPIO DEBOUNCE COUNTER0	0xFF	RW	Bit[7:0]: Debounce counter0 value[7:0] These bits indicate cycle number which an input signal should keep for treated as a valid input signal. Used by GPIO0, GPIO2 and GPIO4.
0x80800065	GPIO DEBOUNCE COUNTER1	0xFF	RW	Bit[7:0]: Debounce counter0 value[15:8] These bits indicate cycle number which an input signal should keep for treated as a valid input signal. Used by GPIO0, GPIO2 and GPIO4.
0x80800066	GPIO DEBOUNCE COUNTER2	0x00	RW	Bit[7:0]: Debounce counter0 value[23:16] These bits indicate cycle number which an input signal should keep for treated as a valid input signal. Used by GPIO0, GPIO2 and GPIO4.
0x80800067	RSVD	–	–	Reserved
0x80800068	GPIO DEBOUNCE COUNTER4	0xFF	RW	Bit[7:0]: Debounce counter1 value[7:0] These bits indicate cycle number which an input signal should keep for treated as a valid input signal. Used by GPIO1, GPIO3 and GPIO5.
0x80800069	GPIO DEBOUNCE COUNTER5	0xFF	RW	Bit[7:0]: Debounce counter1 value[15:8] These bits indicate cycle number which an input signal should keep for treated as a valid input signal. Used by GPIO1, GPIO3 and GPIO5.

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table 4-28 SC registers[abc] (sheet 16 of 31)

address	register name	default value	R/W	description
0x8080006A	GPIO DEBOUNCE COUNTER6	0x00	RW	Bit[7:0]: Debounce counter1 value[23:16] These bits indicate cycle number which an input signal should keep for treated as a valid input signal. Used by GPIO1, GPIO3 and GPIO5.
0x8080006B	RSVD	–	–	Reserved
0x8080006C	GPIO INTERRUPT0	0x00	RW	Bit[7:6]: Reserved for SCCBID PAD GPIO function Bit[5:0]: Enable bits for GPIO input individual/ reserved interrupt These bits also need to be set when use system GPIO interrupt
0x8080006D~ 0x8080006F	RSVD	–	–	Reserved
0x80800070	GPIO INTERRUPT1	0x00	RW	Bit[7:6]: Reserved for SCCBID PAD GPIO function Bit[5:0]: Interrupt flag bits for GPIO input individual/ reserved interrupt Use this bit to determine which GPIO interrupt is generated
0x80800071~ 0x80800073	RSVD	–	–	Reserved

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table 4-28 SC registers[abc] (sheet 17 of 31)

address	register name	default value	R/W	description
0x80800074	GPIO INTERRUPT2	0xFF	RW	Bit[7:6]: Reserved for SCCBID GPIO pad function Bit[5]: Select the level or edge type to generate an interrupt for GPIO5 0: Low level or negative edge trigger interrupt 1: High level or postive edge trigger interrupt Bit[4]: Select the level or edge type to generate an interrupt for GPIO4 0: Low level or negative edge trigger interrupt 1: High level or postive edge trigger interrupt Bit[3]: Select the level or edge type to generate an interrupt for GPIO3 0: Low level or negative edge trigger interrupt 1: High level or postive edge trigger interrupt Bit[2]: Select the level or edge type to generate an interrupt for GPIO2 0: Low level or negative edge trigger interrupt 1: High level or postive edge trigger interrupt Bit[1]: Select the level or edge type to generate an interrupt for GPIO1 0: Low level or negative edge trigger interrupt 1: High level or postive edge trigger interrupt Bit[0]: Select the level or edge type to generate an interrupt for GPIO0 0: Low level or negative edge trigger interrupt 1: High level or postive edge trigger interrupt
0x80800075~ 0x80800077	RSVD	–	–	Reserved

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table 4-28 SC registers[abc] (sheet 18 of 31)

address	register name	default value	R/W	description
0x80800078	GPIO INTERRUPT3	0x00	RW	Bit[7:6]: Reserved for SCCBID GPIO pad function Bit[5]: Select the signal type to generate an interrupt for GPIO5 0: Level trigger 1: Edge trigger Bit[4]: Select the signal type to generate an interrupt for GPIO4 0: Level trigger 1: Edge trigger Bit[3]: Select the signal type to generate an interrupt for GPIO3 0: Level trigger 1: Edge trigger Bit[2]: Select the signal type to generate an interrupt for GPIO2 0: Level trigger 1: Edge trigger Bit[1]: Select the signal type to generate an interrupt for GPIO1 0: Level trigger 1: Edge trigger Bit[0]: Select the signal type to generate an interrupt for GPIO0 0: Level trigger 1: Edge trigger
0x80800079~ 0x8080007B	RSVD	–	–	Reserved
0x8080007C	GPIO INTERRUPT4	0x00	RW	Bit[7:6]: Reserved for SCCBID GPIO pad function Bit[5]: Enable both edge trigger functions for GPIO5 (only valid when in edge trigger mode) Bit[4]: Enable both edge trigger functions for GPIO4 (only valid when in edge trigger mode) Bit[3]: Enable both edge trigger functions for GPIO3 (only valid when in edge trigger mode) Bit[2]: Enable both edge trigger functions for GPIO2 (only valid when in edge trigger mode) Bit[1]: Enable both edge trigger functiosn for GPIO1 (only valid when in edge trigger mode) Bit[0]: Enable both edge trigger functions for GPIO0 (only valid when in edge trigger mode)
0x8080007D~ 0x8080008F	RSVD	–	–	Reserved

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table 4-28 SC registers[abc] (sheet 19 of 31)

address	register name	default value	R/W	description
0x80800090	IMAGE PATH CONTROL0	0x05	RW	Bit[7]: MIPI digital loop enable bit 0: Normal data path 1: MIPI RX receive data from MIPI TX Bit[6]: Select the data source for MTX 0: From VFIFO 1: From color bar FTX Bit[5:0]: Debug mode
0x80800091	IMAGE PATH CONTROL1	0x00	RW	Bit[7:1]: Debug mode Bit[0]: Select the data source for DVP 0: From VFIFO 1: From color bar FTX
0x80800092~ 0x8080009F	RSVD	–	–	Reserved
0x808000A0	PLL1 CONTROL0	0x1D	RW	Bit[7:0]: PLL1 loopdiv_p Vloopdiv_p = loopdiv_p For integer mode: fvco = (f_{OSC}/Vprediv)×(2×Vloopdivp+8+Vsdiv) fclk0 = fvco/Vdiv_hs fclk1 = fvco/Vdiv_ls For fractional mode: fvco = (f_{OSC}/Vprediv)× (2×Vloopdivp+8+Vsdiv+Vdsm[19:0]/ (2^20)) For SSCG mode: fvco = [(f_{OSC}/Vprediv)× (2×Vloopdivp+8+Vsdiv+Vdsm[9:0]/(2^9)), (f_{OSC}/Vprediv)×(2×Vloopdivp+8+Vsdiv+ Vdsm[19:10]/(2^9))] fssc = f_{OSC}/(2×(8-Vcntck[2:0])×(Vdsm[19:10]- Vdsm[9:0]))

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table 4-28 SC registers[abc] (sheet 20 of 31)

address	register name	default value	R/W	description
0x808000A1	PLL1 CONTROL1	0xAF	RW	Bit[7]: PLL1 high frequency select This bit should be set when fvco > 600MHz Bit[6:4]: PLL1 pre_div PLL1 pre-divider ratio 0x0: Vprediv = 1 0x1: Vprediv = 1.5 0x2: Vprediv = 2 0x3: Vprediv = 2.5 0x4: Vprediv = 3 0x5: Vprediv = 4 0x6: Vprediv = 6 0x7: Vprediv = 6 Bit[3]: PLL1 sdiv 0: Vsdiv = 0 1: Vsdiv = 1 Bit[2:0]: PLL1 cntck Control bits for adjustment on period triangular waveform in SSCG Vcntck = cntck
0x808000A2	PLL1 CONTROL2	0x77	RW	Bit[7:4]: PLL1 div_ls Post divider for PLL1 clock1 output 0x0: Vdiv_ls = 1 0x1: Vdiv_ls = 2 0x2: Vdiv_ls = 3 0x3: Vdiv_ls = 4 0x4: Vdiv_ls = 5 0x5: Vdiv_ls = 6 0x6: Vdiv_ls = 7 0x7: Vdiv_ls = 8 0x8: Vdiv_ls = 9 0x9: Vdiv_ls = 10 0xA: Vdiv_ls = 1.5 0xB~0xF: Debug mode Bit[3:0]: PLL1 div_hs Post divider for PLL1 clock0 output 0x0: Vdiv_ls = 1 0x1: Vdiv_ls = 2 0x2: Vdiv_ls = 3 0x3: Vdiv_ls = 4 0x4: Vdiv_ls = 5 0x5: Vdiv_ls = 6 0x6: Vdiv_ls = 7 0x7: Vdiv_ls = 8 0x8: Vdiv_ls = 9 0x9: Vdiv_ls = 10 0xA: Vdiv_ls = 1.5 0xB~0xF: Debug mode

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table 4-28 SC registers[abc] (sheet 21 of 31)

address	register name	default value	R/W	description
0x808000A3	PLL1 CONTROL3	0x29	RW	Bit[7:6]: Debug mode Bit[5:4]: PLL1 LPF Control bits for LPF resistor value adjustment Bit[3]: PLL1 integer enable Enable PLL1 integer-N mode Bit[2:0]: PLL1 cp Control bits for charge pump current I = 2.5×(8-cp)
0x808000A4	PLL2 CONTROL0	0x1D	RW	Bit[7:0]: PLL2 loopdiv_p Vloopdiv_p = loopdiv_p For integer mode: fvco = (f_{OSC}/Vprediv)×(2×Vloopdivp+8+Vsdiv). fclk0 = fvco/Vdiv_hs fclk1 = fvco/Vdiv_ls For fractional mode: fvco = (f_{OSC}/Vprediv)×(2×Vloopdivp+8+Vsdiv+Vdsm[19:0]/(2^20)) For SSCG mode: fvco = [(f_{OSC}/Vprediv)×(2×Vloopdivp+8+Vsdiv + Vdsm[9:0]/(2^9)), (f_{OSC}/Vprediv)×(2×Vloopdivp+8+Vsdiv+Vdsm[19:10]/(2^9))] fssc = f_{OSC}/(2*(8-Vcntck[2:0])×(Vdsm[19:10]-Vdsm[9:0]))
0x808000A5	PLL2 CONTROL1	0xAF	RW	Bit[7]: PLL2 high frequency select This bit should be set when fvco > 600MHz Bit[6:4]: PLL2 pre_div PLL2 pre-divider ratio 0x0: Vprediv = 1 0x1: Vprediv = 1.5 0x2: Vprediv = 2 0x3: Vprediv = 2.5 0x4: Vprediv = 3 0x5: Vprediv = 4 0x6: Vprediv = 6 0x7: Vprediv = 6 Bit[3]: PLL2 sdiv 0: Vsdiv = 0 1: Vsdiv = 1 Bit[2:0]: PLL2 cntck Control bits for adjustment on period triangular waveform in SSCG Vcntck = cntck

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table 4-28 SC registers[abc] (sheet 22 of 31)

address	register name	default value	R/W	description
0x808000A6	PLL2 CONTROL2	0x70	RW	Bit[7:4]: PLL2 div_ls Post divider for PLL2 clock1 output 0x0: Vdiv_ls = 1 0x1: Vdiv_ls = 2 0x2: Vdiv_ls = 3 0x3: Vdiv_ls = 4 0x4: Vdiv_ls = 5 0x5: Vdiv_ls = 6 0x6: Vdiv_ls = 7 0x7: Vdiv_ls = 8 0x8: Vdiv_ls = 9 0x9: Vdiv_ls = 10 0xA: Vdiv_ls = 1.5 0xB~0xF: Debug mode Bit[3:0]: PLL2 div_hs Post divider for PLL2 clock0 output PLL2 clock0 is intended for MIPI TX PHY 0x0: Vdiv_ls = 1 0x1: Vdiv_ls = 2 0x2: Vdiv_ls = 3 0x3: Vdiv_ls = 4 0x4: Vdiv_ls = 5 0x5: Vdiv_ls = 6 0x6: Vdiv_ls = 7 0x7: Vdiv_ls = 8 0x8: Vdiv_ls = 9 0x9: Vdiv_ls = 10 0xA: Vdiv_ls = 1.5 0xB~0xF: Debug mode
0x808000A7	PLL2 CONTROL3	0x29	RW	Bit[7:6]: Debug mode Bit[5:4]: PLL2 LPF Control bits for LPF resistor value adjustment Bit[3]: PLL2 integer enable Enable PLL2 integer-N mode Bit[2:0]: PLL2 cp Control bits for charge pump current I = 2.5×(8-cp)
0x808000A8	PLL1 CONTROL4	0x00	RW	Bit[7:0]: PLL1 DSM[7:0]
0x808000A9	PLL1 CONTROL5	0x00	RW	Bit[7:0]: PLL1 DSM[15:8]

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table 4-28 SC registers[abc] (sheet 23 of 31)

address	register name	default value	R/W	description
0x808000AA	PLL1 CONTROL6	0x00	RW	Bit[7]: PLL1 SSCG mode enable 0: Disabled 1: Enabled Bit[6]: PLL1 dither enable 0: Disabled 1: Enabled Bit[5:4]: Debug mode Bit[3:0]: PLL1 DSM[19:16]
0x808000AB~ 0x808000AC	RSVD	–	–	Reserved
0x808000AD	MIPI CONTROL1	0x00	RW	Bit[7]: pd_mipi_tx Bit[6:4]: slew_rate Bit[3]: pd_dvp Bit[2:0]: Reserved
0x808000AE	RSVD	–	–	Reserved
0x808000AF	MIPI CONTROL3	0x0F	RW	Bit[7]: pd_ivref_tx_pll 0: Normal 1: Power down Bit[6:0]: Debug mode
0x808000B0	MIPI CONTROL4	0x00	RW	Bit[7:4]: Reserved Bit[3]: pd_lprx0 Power down low power of RX0 0: Normal 1: Power down Bit[2]: pd_hsrx0 Power down high speed of RX0 0: Normal 1: Power down Bit[1:0]: enable_d_lane_r0 Enable data lane of RX0 00: Lane0 and lane1 disabled 01: Lane0 enabled, lane1 disabled 10: Lane1 enabled, lan0 disabled 11: Lane0 and lane1 enabled
0x808000B1~ 0x808000B3	RSVD	–	–	Reserved

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table 4-28 SC registers[abc] (sheet 24 of 31)

address	register name	default value	R/W	description
0x808000B4	MIPI CONTROL8	0x00	RW	BIt[7:4]: Reserved Bit[3]: pd_lprx1 Power down low power of RX1 0: Normal 1: Power down Bit[2]: pd_hsrx1 Power down high speed of RX1 0: Normal 1: Power down Bit[1:0]: enable_d_lane_r1 Enable data lane of RX1 00: Lane0 and lane1 disabled 01: Lane0 enabled, lane1 disabled 10: Lane1 enabled, lan0 disabled 11: Lane0 and lane1 enabled
0x808000B5~ 0x808000B7	RSVD	–	–	Reserved
0x808000B8	MIPI CONTROL C	0x00	RW	Bit[7]: Disable TX D1 lane 0: Enabled 1: Disabled Bit[6:4]: Reserved Bit[3]: Disable TX D0 lane Enable bit for MIPI TX data lane0 0: Enabled 1: Disabled Bit[2:0]: Reserved
0x808000B9	MIPI CONTROL D	0x00	RW	Bit[7]: Disable TX D3 lane 0: Enabled 1: Disabled Bit[6:4]: Reserved Bit[3]: Disable TX D2 lane Enable bit for MIPI TX data lane2 0: Enabled 1: Disabled Bit[2:0]: Reserved
0x808000BA	MIPI CONTROL E	0x20	RW	Bit[7:4]: Reserved Bit[3]: Disable TX clock lane Enable bit for MIPI TX clock lane 0: Enabled 1: Disabled Bit[2:0]: Reserved

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table 4-28 SC registers[abc] (sheet 25 of 31)

address	register name	default value	R/W	description
0x808000BB	MIPI CONTROL F	0x1D	RW	Bit[7]: Reserved Bit[3]: Bypass DVP sync Bypass DVP sync 0: DVP output from DVP sync module 1: DVP output from digital interface directly Bit[2:0]: Reserved
0x808000BC~ 0x808000BF	RSVD	–	–	Reserved
0x808000C0	HOST COMMAND	0x00	RW	Host Command Bits Writing to these bits will trigger host command interrupt. Firmware can read these bits to determine what command host had sent in when an interrupt was detected.
0x808000C1~ 0x808000C4	RSVD	–	–	Reserved
0x808000C5	INTERRUPT1 ENABLE1	0x00	RW	Bit[7:2]: Enable bits for system interrupt group1[15:10] Bit[1:0]: Reserved
0x808000C6	INTERRUPT1 ENABLE2	0x00	RW	Bit[7:0]: Enable bits for system interrupt group1[23:16]
0x808000C7	INTERRUPT1 ENABLE3	0x00	RW	Bit[7:0]: Enable bit for system interrupt group1[31:26]
0x808000C8	RSVD	–	–	Reserved
0x808000C9	INTERRUPT1 FLAG1	0x00	RW	Bit[7:2]: System interrupt group1 flag[15:10] Writing '1' to these bits will clear the flag Bit[1:0]: Reserved
0x808000CA	INTERRUPT1 FLAG2	0x00	RW	Bit[7:0]: System interrupt group1 flag[23:16] Writing '1' to these bits will clear the flag
0x808000CB	INTERRUPT1 FLAG3	0x00	RW	Bit[7:2]: System interrupt group1 flag[31:24] Writing '1' to these bits will clear the flag Bit[1:0]: Reserved
0x808000CC~ 0x808000F7	RSVD	–	–	Reserved
0x808000F8	ANALOG MISC0	0x1F	RW	Bit[7]: pd_ts Power down temperature sensor 0: Normal 1: Power down Bit[6:0]: Debug mode

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table 4-28 SC registers[abc] (sheet 26 of 31)

address	register name	default value	R/W	description
0x808000F9	ANALOG MISC1	0x00	RW	Bit[7:3]: Debug mode Bit[2:0]: reg_vrbg LDO bandgap adjustment
0x808000FA	RSVD	–	–	Reserved
0x808000FB	ANALOG MISC3	0x00	RW	Bit[7]: PD brown-out Power down brown-out 0: Normal 1: Power down Bit[6:0]: Reserved
0x808000FC	PLL2 CONTROL4	0x00	RW	Bit[7:0]: PLL2 DSM[7:0] For fractional and SSCG mode use
0x808000FD	PLL2 CONTROL5	0x00	RW	Bit[7:0]: PLL2 DSM[15:8] For fractional and SSCG mode use
0x808000FE	PLL2 CONTROL6	0x00	RW	Bit[7]: PLL2 SSCG mode enable 0: Enabled 1: Disabled Bit[6]: PLL2 dither enable 0: Enabled 1: Disabled Bit[5:4]: Debug mode Bit[3:0]: PLL2 DSM[19:16] For fractional and SSCG mode use
0x808000FF~ 0x8080014F	RSVD	–	–	Reserved
0x80800150	WATCHDOG CONTROL0	0xFF	RW	Bit[7:0]: Watchdog reset counter full threshold[7:0]
0x80800151	WATCHDOG CONTROL1	0xFF	RW	Bit[7:0]: Watchdog reset counter full threshold[15:8]
0x80800152	WATCHDOG CONTROL2	0xFF	RW	Bit[7:0]: Watchdog reset counter full threshold[23:16]
0x80800153	WATCHDOG CONTROL2	0x3F	RW	Bit[7]: Watchdog enable 0: Enabled 1: Disabled Bit[6]: Watchdog clear Writing 1 to this bit will clear watchdog counter Bit[5:0]: Watchdog reset counter full threshold[29:24]
0x80800154~ 0x8080015F	RSVD	–	–	Reserved

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table 4-28 SC registers[abc] (sheet 27 of 31)

address	register name	default value	R/W	description
0x80800160	PAD CONTROL0	0x00	RW	Bit[7]: Output driving strength select for FSIN1 pad Bit[6]: Output driving strength select for FSIN0 pad Bit[5]: Output driving strength select for SPWDN1 pad Bit[4]: Output driving strength select for SPWDN0 pad Bit[3]: Output driving strength select for SSDA pad Bit[2]: Output driving strength select for SSCK pad Bit[1]: Output driving strength select for CCLK1 pad Bit[0]: Output driving strength select for CCLK0 pad
0x80800161	PAD CONTROL1	0x00	RW	Bit[7]: Output driving strength select for TXD pad Bit[6]: Output driving strength select for RXD Bit[5:0]: Reserved
0x80800162	PAD CONTROL2	0x00	RW	Bit[7]: Output driving strength select for SDA1 pad Bit[6]: Output driving strength select for SCK1 pad Bit[5]: Output driving strength select for SDA0 pad Bit[4]: Output driving strength select for SCK0 pad Bit[3]: Output driving strength select for YO pad Bit[2]: Output driving strength select for PCLKO pad Bit[1]: Output driving strength select for HREFO pad Bit[0]: Output driving strength select for VSYNCO pad
0x80800163	PAD CONTROL3	0x00	RW	Bit[7:6]: Reserved Bit[5]: Output driving strength select for GPIO5 pad Bit[4]: Output driving strength select for GPIO4 pad Bit[3]: Output driving strength select for GPO3 pad Bit[2]: Output driving strength select for GPIO2 pad Bit[1]: Output driving strength select for GPIO1 pad Bit[0]: Output driving strength select for GPIO0 pad

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table 4-28 SC registers[abc] (sheet 28 of 31)

address	register name	default value	R/W	description
0x80800164	PAD CONTROL4	0x00	RW	Bit[7]: Pull down enable for FSIN1 pad Bit[6]: Pull down enable for FSIN0 pad Bit[5]: Pull down enable for SPWDN1 pad Bit[4]: Pull down enable for SPWDN0 pad Bit[3]: Pull down enable for SSDA pad Bit[2]: Pull down enable for SSCK pad Bit[1]: Pull down enable for CCLK1 pad Bit[0]: Pull down enable for CCLK0 pad
0x80800165	PAD CONTROL5	0x00	RW	Bit[7]: Pull up enable for TXD pad Bit[6]: Pull up enable for RXD pad Bit[5:0]: Reserved
0x80800166	PAD CONTROL6	0x00	RW	Bit[7]: Pull down enable for SDA1 pad Bit[6]: Pull down enable for SCK1 pad Bit[5]: Pull down enable for SDA0 pad Bit[4]: Pull down enable for SCK0 pad Bit[3:0]: Reserved
0x80800167	PAD CONTROL7	0x00	RW	Bit[7:6]: Reserved Bit[5]: Pull up enable for GPIO5 pad Bit[4]: Pull up enable for GPIO4 pad Bit[3]: Pull down enable for GPIO3 pad Bit[2]: Pull down enable for GPIO2 pad Bit[1]: Pull down enable for GPIO1 pad Bit[0]: Pull down enable for GPIO0 pad
0x80800168	PAD CONTROL8	0xFC	RW	Bit[7]: Input enable bit for FSIN1 pad Bit[6]: Input enable bit for FSIN0 pad Bit[5]: Input enable bit for SPWDN1 pad Bit[4]: Input enable bit for SPWDN0 pad Bit[3]: Input enable bit for SSDA pad Bit[2]: Input enable bit for SSCK pad Bit[1]: Input enable bit for CCLK1 pad Bit[0]: Input enable bit for CCLK0 pad
0x80800169	PAD CONTROL9	0xEE	RW	Bit[7]: Input enable bit for TXD pad Bit[6]: Input enable bit for RXD pad Bit[5:0]: Reserved
0x8080016A	PAD CONTROL A	0xFF	RW	Bit[7]: Input enable bit for SDA1 pad Bit[6]: Input enable bit for SCK1 pad Bit[5]: Input enable bit for SDA0 pad Bit[4]: Input enable bit for SCK0 pad Bit[3:0]: Reserved

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table 4-28 SC registers[abc] (sheet 29 of 31)

address	register name	default value	R/W	description
0x8080016B	PAD CONTROL B	0xFF	RW	Bit[7:6]: Reserved Bit[5]: Input enable bit for GPIO5 pad Bit[4]: Input enable bit for GPIO4 pad Bit[3]: Input enable bit for GPIO3 pad Bit[2]: Input enable bit for GPIO2 pad Bit[1]: Input enable bit for GPIO1 pad Bit[0]: Input enable bit for GPIO0 pad
0x8080016C	PAD MUX CONTROL0	0x32	RW	Bit[7]: Debug mode Bit[6]: SCCBS master mode enable Bit[5]: SCCB MS1 pads master mode enable 0: Disable 1: Enable Bit[4]: SCCB MS0 pads master mode enable 0: Disable 1: Enable Bit[3]: Debug mode Bit[2]: Input enable for pads group1 Bit[1]: Input enable for pads group0 Bit[0]: Reserved
0x8080016D	PAD MUX CONTROL1	0x00	RW	Bit[7]: DVP output interface enable 0: Disable 1: Enable Bit[6]: DVP input interface enable 0: Disable 1: Enable Bit[5]: 4-wire serial interface master/slave mode select 0: Disable 1: Enable Bit[4]: 4-wire serial interface enable 0: Disable 1: Enable Bit[3:0]: Debug mode
0x8080016E	PAD MUX CONTROL2	0x00	RW	Bit[7]: Debug mode Bit[6]: FSYNC mode 0: Input 1: Output Bit[5:1]: Debug mode Bit[0]: 4-wire serial interface SSN2 enable When this bit is set, SSN2 signal can be output through GPIO4
0x8080016F	PAD MUX CONTROL3	0x00	RW	Bit[7:4]: Reserved Bit[3]: BON flag output enable 0: Disable output 1: Enable output Bit[2:0]: Reserved

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table 4-28 SC registers[abc] (sheet 30 of 31)

address	register name	default value	R/W	description
0x80800170	PAD CONTROL C	0x00	RW	Bit[7]: Output driving strength select for TDI pad Bit[6]: Output driving strength select for TDO pad Bit[5]: Output driving strength select for SCCBID pad Bit[4]: Output driving strength select for FSYNC pad Bit[3]: Output driving strength select for MISO pad Bit[2]: Output driving strength select for MOSI pad Bit[1]: Output driving strength select for SSN pad Bit[0]: Output driving strength select for SICK pad
0x80800171	PAD CONTROL D	0x00	RW	Bit[7]: Output driving strength select for BON pad Bit[6]: Output driving strength select for TXD1 pad Bit[5]: Output driving strength select for RXD1 pad Bit[4]: Output driving strength select for TXD0 pad Bit[3]: Output driving strength select for RXD0 pad Bit[2]: Output driving strength select for TRST pad Bit[1]: Output driving strength select for TCK pad Bit[0]: Output driving strength select for TMS pad
0x80800172	PAD CONTROL E	0x00	RW	Bit[7:1]: Debug mode Bit[0]: Output driving strength select for SCCBID1
0x80800173	RSVD	–	–	Reserved
0x80800174	PAD CONTROL 10	0x00	RW	Bit[7]: Pull down enable for TDI pad Bit[6]: Pull down enable for TDO pad Bit[5]: Pull down enable for SCCBID pad Bit[4]: Pull down enable for FSYNC pad Bit[3]: Pull down enable for MISO pad Bit[2]: Pull down enable for MOSI pad Bit[1]: Pull up enable for SSN pad Bit[0]: Pull down enable for SICK pad
0x80800175	PAD CONTROL 11	0x00	RW	Bit[7]: Pull up enable for BON pad Bit[6]: Pull up enable for TXD1 pad Bit[5]: Pull up enable for RXD1 pad Bit[4]: Pull up enable for TXD0 pad Bit[3]: Pull up enable for RXD0 pad Bit[2]: Pull down enable for TRST pad Bit[1]: Pull down enable for TCK pad Bit[0]: Pull down enable for TMS pad
0x80800176	PAD CONTROL 12	0x00	RW	Bit[7:1]: Debug mode Bit[0]: Pull down enable for pad SCCBID1
0x80800177	RSVD	–	–	Reserved

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table 4-28 SC registers[abc] (sheet 31 of 31)

address	register name	default value	R/W	description
0x80800178	PAD CONTROL 13	0xBF	RW	Bit[7]: Input enable bit for TDI pad Bit[6]: Input enable bit for TDO pad Bit[5]: Input enable bit for SCCBID pad Bit[4]: Input enable bit for FSYNC pad Bit[3]: Input enable bit for MISO pad Bit[2]: Input enable bit for MOSI pad Bit[1]: Input enable bit for SSN pad Bit[0]: Input enable bit for SICK pad
0x80800179	PAD CONTROL 14	0x7F	RW	Bit[7]: Input enable bit for BON pad Bit[6]: Input enable bit for TXD1 pad Bit[5]: Input enable bit for RXD1 pad Bit[4]: Input enable bit for TXD0 pad Bit[3]: Input enable bit for RXD0 pad Bit[2]: Input enable bit for TRST pad Bit[1]: Input enable bit for TCK pad Bit[0]: Input enable bit for TMS pad
0x8080017A	PAD CONTROL 15	0x01	RW	Bit[7:1]: Debug mode Bit[0]: Input enable bit for PAD SCCBID1
0x808017B~ 0x80801C4	RSVD	–	–	Reserved
0x808001C5	INTERRUPT2 ENABLE1	0x00	RW	Bit[7:0]: Enable bits for system interrupt group2[15:8]
0x808001C6	INTERRUPT2 ENABLE2	0x00	RW	Bit[7:0]: Enable bits for system interrupt group2[23:16]
0x808001C7	INTERRUPT2 ENABLE3	0x00	RW	Bit[7:0]: Enable bits for system interrupt group2[31:24]
0x808001C8	RSVD	–	–	Reserved
0x808001C9	INTERRUPT2 FLAG1	0x00	RW	Bit[7:0]: System interrupt group2 flag[15:8] Writing '1' to these bits will clear the flag
0x808001CA	INTERRUPT2 FLAG2	0x00	RW	Bit[7:0]: System interrupt group2 flag[23:16] Writing '1' to these bits will clear the flag
0x808001CB	INTERRUPT2 FLAG3	0x00	RW	Bit[7:0]: System interrupt group2 flag[31:24] Writing '1' to these bits will clear the flag

a. writing to reserved addresses or bits will induce unpredictable result, so do not change their values

b. reading reserved addresses or bits will get uncertain values

c. all registers can be accessed by both 32-bit mode and 8-bit mode

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4.19 OTP control

base address: 0x8028E000

table 4-29 OTP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x8028E000	BANK REG0	0x00	RW	For 128 x 8 bits OTP, there are 8 banks, each of which is 16 bytes. If one needs to write to one of these banks. First, write the expected values to be burned into OTP into bank registers one by one. Then, start the write action into OTP. If one needs to read one of the banks. First start the load function. After the loading has been finished, read the banks out, and verify the values are what are expected. These are the mirror registers for each bank of OTP Bit[7:0]: Byte0 mirror register
0x8028E001	BANK REG1	0x00	RW	Bit[7:0]: Byte1 mirror register
0x8028E002	BANK REG2	0x00	RW	Bit[7:0]: Byte2 mirror register
0x8028E003	BANK REG3	0x00	RW	Bit[7:0]: Byte3 mirror register
0x8028E004	BANK REG4	0x00	RW	Bit[7:0]: Byte4 mirror register
0x8028E005	BANK REG5	0x00	RW	Bit[7:0]: Byte5 mirror register
0x8028E006	BANK REG6	0x00	RW	Bit[7:0]: Byte6 mirror register
0x8028E007	BANK REG7	0x00	RW	Bit[7:0]: Byte7 mirror register
0x8028E008	BANK REG8	0x00	RW	Bit[7:0]: Byte8 mirror register
0x8028E009	BANK REG9	0x00	RW	Bit[7:0]: Byte9 mirror register
0x8028E00A	BANK REG10	0x00	RW	Bit[7:0]: Byte10 mirror register
0x8028E00B	BANK REG11	0x00	RW	Bit[7:0]: Byte11 mirror register
0x8028E00C	BANK REG12	0x00	RW	Bit[7:0]: Byte12 mirror register
0x8028E00D	BANK REG13	0x00	RW	Bit[7:0]: Byte13 mirror register
0x8028E00E	BANK REG14	0x00	RW	Bit[7:0]: Byte14 mirror register
0x8028E00F	BANK REG15	0x00	RW	Bit[7:0]: Byte15 mirror register
0x8028E080	OTP PROGRAM	0x00	RW	Bit[7]: Status of programming or not (read only) Bit[6:1]: Reserved Bit[0]: Start program (write only) Once written to bit[1], programming into OTP begins

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table 4-29 OTP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x8028E081	OTP READ	0x00	RW	Bit[7]: Status of loading or not (read only) Bit[6:1]: Reserved Bit[0]: Start loading (write only) Once written to bit[1], loading from OTP begins
0x8028E082	PROGRAM CONTROL	0x0F	RW	Bit[7:0]: Width of program strobe pulse control Actual width of pulse is (pqm_ctrl*8+6)*clock
0x8028E083	READ CONTROL	0x01	RW	Bit[7:0]: Control width of load strobe pulse Actual width of pulse is (read_ctrl+6)*clock
0x8028E084	MODE CONTROL	0x00	RW	Bit[7]: Enable OTP programming 0: Enable the OTP programming 1: Disable the OTP programming Bit[6]: Manual or auto mode of programming 0: Enable auto mode for programming and loading 1: Enable manual mode for programming and loading Bit[5:3]: Reserved Bit[2:0]: Bank number of OTP for manual mode select
0x8028E085	START ADDRESS	0x00	RW	Bit[7:0]: Start address of bank register for certain bank in manual mode
0x8028E086	END ADDRESS	0x0F	RW	Bit[7:0]: End address of bank register for certain bank in manual mode
0x8028E088	PS2CS	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Value of PS to CS[9:8]
0x8028E089	PS2CS	0x96	RW	Bit[7:0]: Value of PS to CS[7:0]
0x8028E08A	PS2VDDQ	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Value of PS to VDDQ[9:8]
0x8028E08B	PS2VDDQ	0x01	RW	Bit[7:0]: Value of PS to VDDQ[7:0]
0x8028E08C	VDDQ2PGN	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Value of VDDQ to PGN[9:8]
0x8028E08D	VDDQ2PGN	0x96	RW	Bit[7:0]: Value of VDDQ to PGN[7:0]

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4.20 ISP sub-module base address summary

table 4-30 ISP sub-module base address summary

module name	function	base address
OV490/ISP/ISP CTRL	ISP top control	0x80206000
OV490/ISP/pre ISP	pre-ISP process	0x80206080
OV490/ISP/AWB gain	auto white balance gain apply	0x80206100
OV490/ISP/DPC	defect pixels correction	0x80206200
OV490/ISP/HDR RAW DNS	HDR path RAW de-noise	0x80206300
OV490/ISP/OVPB RAW DNS	OVPB path RAW de-noise	0x80206380
OV490/ISP/LENC	lens correction	0x80206400
OV490/ISP/combine	HDR combine	0x80206800
OV490/ISP/curve AWB	curve based auto white balance	0x80206C00
OV490/ISP/AEC AGC	auto exposure / gain control	0x80207000
OV490/ISP/tone-mapping	tone-mapping	0x80207400
OV490/ISP/stretch	RAW stretch	0x80207800
OV490/ISP/CIP	color interpolation	0x80207880
OV490/ISP/CMX	color matrix	0x80207900
OV490/ISP/RGB gamma	RGB gamma	0x80207A00
OV490/ISP/RGB DNS	RGBH de-noise	0x80207B00
OV490/ISP/SDE	special digital effect	0x80207B80
OV490/ISP/YUV statistic	YUV statistic	0x80207C00
OV490/ISP/UV DNS	UV de-noise	0x80207D00
OV490/ISP/AEC PK	auto exposure control power keep	0x80207D80

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4.21 auto exposure/gain correction (AEC/AGC)

table 4-31 AEC/AGC registers (sheet 1 of 13)

address	register name	default value	R/W	description
0x80207000	SNR0_AEC_AGC_STAT_TYPE	0x00	RW	Bit[7:1]: Reserved Bit[0]: Sensor 0 AECAGC statistic type 0: Mean value of R, G, B 1: Max value of R, G, B
0x80207001	SNR0_AEC_STAT_WIN_LEFT_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 statistic window left offset[11:8]
0x80207002	SNR0_AEC_STAT_WIN_LEFT_L	0x00	RW	Bit[7:0]: Sensor 0 statistic window left offset[7:0]
0x80207003	SNR0_AEC_STAT_WIN_RIGHT_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 statistic window right offset[11:8]
0x80207004	SNR0_AEC_STAT_WIN_RIGHT_L	0x00	RW	Bit[7:0]: Sensor 0 statistic window right offset[7:0]
0x80207005	SNR0_AEC_STAT_WIN_TOP_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 statistic window top offset[10:8]
0x80207006	SNR0_AEC_STAT_WIN_TOP_L	0x00	RW	Bit[7:0]: Sensor 0 statistic window top offset[7:0]
0x80207007	SNR0_AEC_STAT_WIN_BOTTOM_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 statistic window bottom offset[10:8]
0x80207008	SNR0_AEC_STAT_WIN_BOTTOM_L	0x14	RW	Bit[7:0]: Sensor 0 statistic window bottom offset[7:0]
0x80207009	SNR0_AEC_MAX_W_H	0x01	RW	Bit[7:2]: Reserved Bit[1]: Sensor 0 MaxW[0] high byte Bit[0]: Sensor 0 MaxW[1] low byte
0x8020700A	SNR0_AEC_MAX_W_0_L	0x20	RW	Bit[7:0]: Sensor 0 MaxW[0] low byte
0x8020700B	SNR0_AEC_MAX_W_1_L	0x00	RW	Bit[7:0]: Sensor 0 MaxW[1] low byte
0x8020700C	SNR0_AEC_MIN_W_0	0x01	RW	Bit[7:0]: Sensor 0 MinW[0]
0x8020700D	SNR0_AEC_MIN_W_1	0x01	RW	Bit[7:0]: Sensor 0 MinW[1]
0x8020700E	SNR0_AEC_STAT_DS_RATE	0x04	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 statistic sample rate

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table 4-31 AEC/AGC registers (sheet 2 of 13)

address	register name	default value	R/W	description
0x8020700F	SNR0_AEC_POS_W_SHIFT	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 position weight shift
0x80207010	SNR0_AEC_LOW_LIGHT_THRE	0x00	RW	Bit[7:0]: Sensor 0 low light threshold
0x80207011	SNR0_AEC_HIGH_LIGHT_THRE	0xF0	RW	Bit[7:0]: Sensor 0 high light threshold
0x80207012	SNR0_AEC_WIN_LEFT_0_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 win left[0] high byte
0x80207013	SNR0_AEC_WIN_LEFT_0_L	0x78	RW	Bit[7:0]: Sensor 0 win left[0] low byte
0x80207014	SNR0_AEC_WIN_TOP_0_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 win top[0] high byte
0x80207015	SNR0_AEC_WIN_TOP_0_L	0x04	RW	Bit[7:0]: Sensor 0 win top[0] low byte
0x80207016	SNR0_AEC_STAT_WIN_WIDTH_0_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 statistic window width[0] high byte
0x80207017	SNR0_AEC_STAT_WIN_WIDTH_0_L	0x78	RW	Bit[7:0]: Sensor 0 statistic window width[0] low byte
0x80207018	SNR0_AEC_STAT_WIN_HEIGHT_0_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 statistic window height[0] high byte
0x80207019	SNR0_AEC_STAT_WIN_HEIGHT_0_L	0x04	RW	Bit[7:0]: Sensor 0 statistic window height[0] low byte
0x8020701A	SNR0_AEC_WIN_LEFT_1_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 window left[1] high byte
0x8020701B	SNR0_AEC_WIN_LEFT_1_L	0x78	RW	Bit[7:0]: Sensor 0 window left[1] low byte
0x8020701C	SNR0_AEC_WIN_TOP_1_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 window top[1] high byte
0x8020701D	SNR0_AEC_WIN_TOP_1_L	0x04	RW	Bit[7:0]: Sensor 0 window top[1] low byte
0x8020701E	SNR0_AEC_STAT_WIN_WIDTH_1_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 statistic window width[1] high byte
0x8020701F	SNR0_AEC_STAT_WIN_WIDTH_1_L	0x78	RW	Bit[7:0]: Sensor 0 statistic window width[1] low byte

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table 4-31 AEC/AGC registers (sheet 3 of 13)

address	register name	default value	R/W	description
0x80207020	SNR0_AEC_STAT_WIN_HEIGHT_1_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 statistic window height[1] high byte
0x80207021	SNR0_AEC_STAT_WIN_HEIGHT_1_L	0x04	RW	Bit[7:0]: Sensor 0 statistic window height[1] low byte
0x80207022	SNR0_AEC_WEIGHTS_0	0x11	RW	Bit[7:4]: Sensor 0 weights[0][0] Bit[3:0]: Sensor 0 weights[1][0]
0x80207023	SNR0_AEC_WEIGHTS_1	0x11	RW	Bit[7:4]: Sensor 0 weights[0][1] Bit[3:0]: Sensor 0 weights[1][1]
0x80207024	SNR0_AEC_WEIGHTS_2	0x11	RW	Bit[7:4]: Sensor 0 weights[0][2] Bit[3:0]: Sensor 0 weights[1][2]
0x80207025	SNR0_AEC_WEIGHTS_3	0x11	RW	Bit[7:4]: Sensor 0 weights[0][3] Bit[3:0]: Sensor 0 weights[1][3]
0x80207026	SNR0_AEC_WEIGHTS_4	0x11	RW	Bit[7:4]: Sensor 0 weights[0][4] Bit[3:0]: Sensor 0 weights[1][4]
0x80207027	SNR0_AEC_WEIGHTS_5	0x11	RW	Bit[7:4]: Sensor 0 weights[0][5] Bit[3:0]: Sensor 0 weights[1][5]
0x80207028	SNR0_AEC_WEIGHTS_6	0x11	RW	Bit[7:4]: Sensor 0 weights[0][6] Bit[3:0]: Sensor 0 weights[1][6]
0x80207029	SNR0_AEC_WEIGHTS_7	0x11	RW	Bit[7:4]: Sensor 0 weights[0][7] Bit[3:0]: Sensor 0 weights[1][7]
0x8020702A	SNR0_AEC_WEIGHTS_8	0x11	RW	Bit[7:4]: Sensor 0 weights[0][8] Bit[3:0]: Sensor 0 weights[1][8]
0x8020702B	SNR0_AEC_WEIGHTS_9	0x11	RW	Bit[7:4]: Sensor 0 weights[0][9] Bit[3:0]: Sensor 0 weights[1][9]
0x8020702C	SNR0_AEC_WEIGHTS_10	0x11	RW	Bit[7:4]: Sensor 0 weights[0][10] Bit[3:0]: Sensor 0 weights[1][10]
0x8020702D	SNR0_AEC_WEIGHTS_11	0x11	RW	Bit[7:4]: Sensor 0 weights[0][11] Bit[3:0]: Sensor 0 weights[1][11]
0x8020702E	SNR0_AEC_WEIGHTS_12	0x11	RW	Bit[7:4]: Sensor 0 weights[0][12] Bit[3:0]: Sensor 0 weights[1][12]
0x8020702F	SNR0_AEC_ROI_LEFT_0_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 ROI left[0] high byte
0x80207030	SNR0_AEC_ROI_LEFT_0_L	0x00	RW	Bit[7:0]: Sensor 0 ROI left[0] low byte
0x80207031	SNR0_AEC_ROI_TOP_0_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 ROI top[0] high byte

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table 4-31 AEC/AGC registers (sheet 4 of 13)

address	register name	default value	R/W	description
0x80207032	SNR0_AEC_ROI_TOP_0_L	0x00	RW	Bit[7:0]: Sensor 0 ROI top[0] low byte
0x80207033	SNR0_AEC_ROI_RIGHT_0_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 ROI right[0] high byte
0x80207034	SNR0_AEC_ROI_RIGHT_0_L	0x00	RW	Bit[7:0]: Sensor 0 ROI right[0] low byte
0x80207035	SNR0_AEC_ROI_BOTTOM_0_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 ROI bottom[0] high byte
0x80207036	SNR0_AEC_ROI_BOTTOM_0_L	0x00	RW	Bit[7:0]: Sensor 0 ROI bottom[0] low byte
0x80207037	SNR0_AEC_ROI_WEIGHTS_0	0x11	RW	Bit[7:4]: Sensor 0 ROI weights[0][0] Bit[3:0]: Sensor 0 ROI weights[0][1]
0x80207038	SNR0_AEC_ROI_LEFT_1_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 ROI left[1] high byte
0x80207039	SNR0_AEC_ROI_LEFT_1_L	0x00	RW	Bit[7:0]: Sensor 0 ROI left[1] low byte
0x8020703A	SNR0_AEC_ROI_TOP_1_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 ROI top[1] high byte
0x8020703B	SNR0_AEC_ROI_TOP_1_L	0x00	RW	Bit[7:0]: Sensor 0 ROI top[1] low byte
0x8020703C	SNR0_AEC_ROI_RIGHT_1_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 ROI right[1] high byte
0x8020703D	SNR0_AEC_ROI_RIGHT_1_L	0x00	RW	Bit[7:0]: Sensor 0 ROI right[1] low byte
0x8020703E	SNR0_AEC_ROI_BOTTOM_1_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 ROI bottom[1] high byte
0x8020703F	SNR0_AEC_ROI_BOTTOM_1_L	0x00	RW	Bit[7:0]: Sensor 0 ROI bottom[1] low byte
0x80207040	SNR0_AEC_ROI_WEIGHTS_1	0x11	RW	Bit[7:4]: Sensor 0 ROI weights[1][0] Bit[3:0]: Sensor 0 ROI weights[1][1]
0x80207041	SNR0_AEC_ROI_SHIFT	0x00	RW	Bit[7:4]: Reserved Bit[3:2]: Sensor 0 ROI shift[0] Bit[1:0]: Sensor 0 ROI shift[1]
0x80207042	SNR0_AEC_BLACK_THRE1_0_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 black threshold1[0] high byte

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table 4-31 AEC/AGC registers (sheet 5 of 13)

address	register name	default value	R/W	description
0x80207043	SNR0_AEC_BLACK_THRE1_0_B1	0x04	RW	Bit[7:0]: Sensor 0 black threshold1[0] middle byte
0x80207044	SNR0_AEC_BLACK_THRE1_0_B0	0x00	RW	Bit[7:0]: Sensor 0 black threshold1[0] low byte
0x80207045	SNR0_AEC_BLACK_THRE2_0_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 black threshold2[0] high byte
0x80207046	SNR0_AEC_BLACK_THRE2_0_B1	0x20	RW	Bit[7:0]: Sensor 0 black threshold2[0] middle byte
0x80207047	SNR0_AEC_BLACK_THRE2_0_B0	0x00	RW	Bit[7:0]: Sensor 0 black threshold2[0] low byte
0x80207048	SNR0_AEC_BLACK_WEIGHT1_0	0x10	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 black weight1[0]
0x80207049	SNR0_AEC_BLACK_WEIGHT2_0	0x14	RW	Bit[7:6]: Reserved Bit[6:0]: Sensor 0 black weight2[0]
0x8020704A	SNR0_AEC_SATURATE_THRE1_0_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 saturate threshold1[0] high byte
0x8020704B	SNR0_AEC_SATURATE_THRE1_0_B1	0x08	RW	Bit[7:0]: Sensor 0 saturate threshold1[0] middle byte
0x8020704C	SNR0_AEC_SATURATE_THRE1_0_B0	0x00	RW	Bit[7:0]: Sensor 0 saturate threshold1[0] low byte
0x8020704D	SNR0_AEC_SATURATE_THRE2_0_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 saturate threshold2[0] high byte
0x8020704E	SNR0_AEC_SATURATE_THRE2_0_B1	0x10	RW	Bit[7:0]: Sensor 0 saturate threshold2[0] middle byte
0x8020704F	SNR0_AEC_SATURATE_THRE2_0_B0	0x00	RW	Bit[7:0]: Sensor 0 saturate threshold2[0] low byte
0x80207050	SNR0_AEC_SATURATE_WEIGHT1_0	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 saturate weight1[0]
0x80207051	SNR0_AEC_SATURATE_WEIGHT2_0	0x12	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 saturate weight2[0]
0x80207052	SNR0_AEC_BLACK_THRE1_1_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 black threshold1[1] high byte
0x80207053	SNR0_AEC_BLACK_THRE1_1_B1	0x10	RW	Bit[7:0]: Sensor 0 black threshold1[1] middle byte

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table 4-31 AEC/AGC registers (sheet 6 of 13)

address	register name	default value	R/W	description
0x80207054	SNR0_AEC_BLACK_THRE1_1_B0	0x00	RW	Bit[7:0]: Sensor 0 black threshold1[1] low byte
0x80207055	SNR0_AEC_BLACK_THRE2_1_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 black threshold2[1] high byte
0x80207056	SNR0_AEC_BLACK_THRE2_1_B1	0x40	RW	Bit[7:0]: Sensor 0 black threshold2[1] middle byte
0x80207057	SNR0_AEC_BLACK_THRE2_1_B0	0x00	RW	Bit[7:0]: Sensor 0 black threshold2[1] low byte
0x80207058	SNR0_AEC_BLACK_WEIGHT1_1	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 black weight1[1]
0x80207059	SNR0_AEC_BLACK_WEIGHT2_1	0x12	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 black weight2[1]
0x8020705A	SNR0_AEC_SATURATE_THRE1_1_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 saturate threshold1[1] high byte
0x8020705B	SNR0_AEC_SATURATE_THRE1_1_B1	0x04	RW	Bit[7:0]: Sensor 0 saturate threshold1[1] middle byte
0x8020705C	SNR0_AEC_SATURATE_THRE1_1_B0	0x00	RW	Bit[7:0]: Sensor 0 saturate threshold1[1] low byte
0x8020705D	SNR0_AEC_SATURATE_THRE2_1_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 saturate threshold2[1] high byte
0x8020705E	SNR0_AEC_SATURATE_THRE2_1_B1	0x20	RW	Bit[7:0]: Sensor 0 saturate threshold2[1] middle byte
0x8020705F	SNR0_AEC_SATURATE_THRE2_1_B0	0x00	RW	Bit[7:0]: Sensor 0 saturate threshold2[1] low byte
0x80207060	SNR0_AEC_SATURATE_WEIGHT1_1	0x10	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 saturate weight1[1]
0x80207061	SNR0_AEC_SATURATE_WEIGHT2_1	0x14	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 saturate weight2[1]
0x80207062	SNR0_AEC_MEAN_Y_0_B1	–	R	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 mean Y[0] high byte
0x80207063	SNR0_AEC_MEAN_Y_0_B0	–	R	Bit[7:0]: Sensor 0 mean Y[0] low byte
0x80207064	SNR0_AEC_MEAN_Y_1_B1	–	R	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 mean Y[1] low byte

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table 4-31 AEC/AGC registers (sheet 7 of 13)

address	register name	default value	R/W	description
0x80207065	SNR0_AEC_MEAN_Y_1_B0	–	R	Bit[7:0]: Sensor 0 mean Y[1] low byte
0x80207066	SNR0_AEC_CNV_GAIN_RATIO	0x00	RW	Bit[7:0]: Sensor 0 conversion gain ratio (firmware use only)
0x80207070	SNR1_AEC_AGC_STAT_TYPE	1'b0	RW	Bit[7:1]: Reserved Bit[0]: Sensor 1 AECAGC statistic type 0: Mean value of R, G, B 1: Max value of R, G, B
0x80207071	SNR1_AEC_STAT_WIN_LEFT_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 statistic window left offset[11:8]
0x80207072	SNR1_AEC_STAT_WIN_LEFT_L	0x00	RW	Bit[7:0]: Sensor 1 statistic window left offset[7:0]
0x80207073	SNR1_AEC_STAT_WIN_RIGHT_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 statistic window right offset[11:8]
0x80207074	SNR1_AEC_STAT_WIN_RIGHT_L	0x00	RW	Bit[7:0]: Sensor 1 statistic window right offset[7:0]
0x80207075	SNR1_AEC_STAT_WIN_TOP_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 statistic window top offset[10:8]
0x80207076	SNR1_AEC_STAT_WIN_TOP_L	0x00	RW	Bit[7:0]: Sensor 1 statistic window top offset[7:0]
0x80207077	SNR1_AEC_STAT_WIN_BOTTOM_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 statistic window bottom offset[10:8]
0x80207078	SNR1_AEC_STAT_WIN_BOTTOM_L	0x14	RW	Bit[7:0]: Sensor 1 statistic window bottom offset[7:0]
0x80207079	SNR1_AEC_MAX_W_H	0x01	RW	Bit[7:2]: Reserved Bit[1]: Sensor 1 MaxW[0] high byte Bit[0]: Sensor 1 MaxW[1] high byte
0x8020707A	SNR1_AEC_MAX_W_0_L	0x20	RW	Bit[7:0]: Sensor 1 MaxW[0] low byte
0x8020707B	SNR1_AEC_MAX_W_1_L	0x00	RW	Bit[7:0]: Sensor 1 MaxW[1] low byte
0x8020707C	SNR1_AEC_MIN_W_0	0x01	RW	Bit[7:0]: Sensor 1 MinW[0]
0x8020707D	SNR1_AEC_MIN_W_1	0x01	RW	Bit[7:0]: Sensor 1 MinW[1]
0x8020707E	SNR1_AEC_STAT_DS_RATE	0x04	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 statistic sample rate

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table 4-31 AEC/AGC registers (sheet 8 of 13)

address	register name	default value	R/W	description
0x8020707F	SNR1_AEC_POS_W_SHIFT	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 position weight shift
0x80207080	SNR1_AEC_LOW_LIGHT_THRE	0x00	RW	Bit[7:0]: Sensor 1 low light threshold
0x80207081	SNR1_AEC_HIGH_LIGHT_THRE	0xF0	RW	Bit[7:0]: Sensor 1 high light threshold
0x80207082	SNR1_AEC_WIN_LEFT_0_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 win left[0] high byte
0x80207083	SNR1_AEC_WIN_LEFT_0_L	0x78	RW	Bit[7:0]: Sensor 1 win left[0] low byte
0x80207084	SNR1_AEC_WIN_TOP_0_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: sensor 1 win top[0] high byte
0x80207085	SNR1_AEC_WIN_TOP_0_L	0x04	RW	Bit[7:0]: Sensor 1 win top[0] low byte
0x80207086	SNR1_AEC_STAT_WIN_WIDTH_0_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 statistic window width[0] high byte
0x80207087	SNR1_AEC_STAT_WIN_WIDTH_0_L	0x78	RW	Bit[7:0]: Sensor 1 statistic window width[0] low byte
0x80207088	SNR1_AEC_STAT_WIN_HEIGHT_0_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 statistic window height[0] high byte
0x80207089	SNR1_AEC_STAT_WIN_HEIGHT_0_L	0x04	RW	Bit[7:0]: Sensor 1 statistic window height[0] low byte
0x8020708A	SNR1_AEC_WIN_LEFT_1_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 window left[1] high byte
0x8020708B	SNR1_AEC_WIN_LEFT_1_L	0x78	RW	Bit[7:0]: Sensor 1 window left[1] low byte
0x8020708C	SNR1_AEC_WIN_TOP_1_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 window top[1] high byte
0x8020708D	SNR1_AEC_WIN_TOP_1_L	0x04	RW	Bit[7:0]: Sensor 1 window top[1] low byte
0x8020708E	SNR1_AEC_STAT_WIN_WIDTH_1_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 statistic window width[1] high byte
0x8020708F	SNR1_AEC_STAT_WIN_WIDTH_1_L	0x78	RW	Bit[7:0]: Sensor 1 statistic window width[1] low byte

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table 4-31 AEC/AGC registers (sheet 9 of 13)

address	register name	default value	R/W	description
0x80207090	SNR1_AEC_STAT_WIN_HEIGHT_1_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 statistic window height[1] high byte
0x80207091	SNR1_AEC_STAT_WIN_HEIGHT_1_L	0x04	RW	Bit[7:0]: Sensor 1 statistic window height[1] low byte
0x80207092	SNR1_AEC_WEIGHTS_0	0x11	RW	Bit[7:4]: Sensor 1 weights[0][0] Bit[3:0]: Sensor 1 weights[1][0]
0x80207093	SNR1_AEC_WEIGHTS_1	0x11	RW	Bit[7:4]: Sensor 1 weights[0][1] Bit[3:0]: Sensor 1 weights[1][1]
0x80207094	SNR1_AEC_WEIGHTS_2	0x11	RW	Bit[7:4]: Sensor 1 weights[0][2] Bit[3:0]: Sensor 1 weights[1][2]
0x80207095	SNR1_AEC_WEIGHTS_3	0x11	RW	Bit[7:4]: Sensor 1 weights[0][3] Bit[3:0]: Sensor 1 weights[1][3]
0x80207096	SNR1_AEC_WEIGHTS_4	0x11	RW	Bit[7:4]: Sensor 1 weights[0][4] Bit[3:0]: Sensor 1 weights[1][4]
0x80207097	SNR1_AEC_WEIGHTS_5	0x11	RW	Bit[7:4]: Sensor 1 weights[0][5] Bit[3:0]: Sensor 1 weights[1][5]
0x80207098	SNR1_AEC_WEIGHTS_6	0x11	RW	Bit[7:4]: Sensor 1 weights[0][6] Bit[3:0]: Sensor 1 weights[1][6]
0x80207099	SNR1_AEC_WEIGHTS_7	0x11	RW	Bit[7:4]: Sensor 1 weights[0][7] Bit[3:0]: Sensor 1 weights[1][7]
0x8020709A	SNR1_AEC_WEIGHTS_8	0x11	RW	Bit[7:4]: Sensor 1 weights[0][8] Bit[3:0]: Sensor 1 weights[1][8]
0x8020709B	SNR1_AEC_WEIGHTS_9	0x11	RW	Bit[7:4]: Sensor 1 weights[0][9] Bit[3:0]: Sensor 1 weights[1][9]
0x8020709C	SNR1_AEC_WEIGHTS_10	0x11	RW	Bit[7:4]: Sensor 1 weights[0][10] Bit[3:0]: Sensor 1 weights[1][10]
0x8020709D	SNR1_AEC_WEIGHTS_11	0x11	RW	Bit[7:4]: Sensor 1 weights[0][11] Bit[3:0]: Sensor 1 weights[1][11]
0x8020709E	SNR1_AEC_WEIGHTS_12	0x11	RW	Bit[7:4]: Sensor 1 weights[0][12] Bit[3:0]: Sensor 1 weights[1][12]
0x8020709F	SNR1_AEC_ROI_LEFT_0_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 ROI left[0] high byte
0x802070A0	SNR1_AEC_ROI_LEFT_0_L	0x00	RW	Bit[7:0]: Sensor 1 ROI left[0] low byte
0x802070A1	SNR1_AEC_ROI_TOP_0_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 ROI top[0] high byte

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table 4-31 AEC/AGC registers (sheet 10 of 13)

address	register name	default value	R/W	description
0x802070A2	SNR1_AEC_ROI_TOP_0_L	0x00	RW	Bit[7:0]: Sensor 1 ROI top[0] low byte
0x802070A3	SNR1_AEC_ROI_RIGHT_0_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 ROI right[0] high byte
0x802070A4	SNR1_AEC_ROI_RIGHT_0_L	0x00	RW	Bit[7:0]: Sensor 1 ROI right[0] low byte
0x802070A5	SNR1_AEC_ROI_BOTTOM_0_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 ROI bottom[0] high byte
0x802070A6	SNR1_AEC_ROI_BOTTOM_0_L	0x00	RW	Bit[7:0]: Sensor 1 ROI bottom[0] low byte
0x802070A7	SNR1_AEC_ROI_WEIGHTS_0	0x11	RW	Bit[7:4]: Sensor 1 ROI weights[0][0] Bit[3:0]: Sensor 1 ROI weights[0][1]
0x802070A8	SNR1_AEC_ROI_LEFT_1_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 ROI left[1] high byte
0x802070A9	SNR1_AEC_ROI_LEFT_1_L	0x00	RW	Bit[7:0]: Sensor 1 ROI left[1] low byte
0x802070AA	SNR1_AEC_ROI_TOP_1_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 ROI top[1] high byte
0x802070AB	SNR1_AEC_ROI_TOP_1_L	0x00	RW	Bit[7:0]: Sensor 1 ROI top[1] low byte
0x802070AC	SNR1_AEC_ROI_RIGHT_1_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 ROI right[1] high byte
0x802070AD	SNR1_AEC_ROI_RIGHT_1_L	0x00	RW	Bit[7:0]: Sensor 1 ROI right[1] low byte
0x802070AE	SNR1_AEC_ROI_BOTTOM_1_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 ROI bottom[1] high byte
0x802070AF	SNR1_AEC_ROI_BOTTOM_1_L	0x00	RW	Bit[7:0]: Sensor 1 ROI bottom[1] low byte
0x802070B0	SNR1_AEC_ROI_WEIGHTS_1	0x11	RW	Bit[7:4]: Sensor 1 ROI weights[1][0] Bit[3:0]: Sensor 1 ROI weights[1][1]
0x802070B1	SNR1_AEC_ROI_SHIFT	0x00	RW	Bit[7:4]: Reserved Bit[3:2]: Sensor 1 ROI shift[0] Bit[1:0]: Sensor 1 ROI shift[1]
0x802070B2	SNR1_AEC_BLACK_THRE1_0_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 black threshold1[0] high byte

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table 4-31 AEC/AGC registers (sheet 11 of 13)

address	register name	default value	R/W	description
0x802070B3	SNR1_AEC_BLACK_THRE1_0_B1	0x04	RW	Bit[7:0]: Sensor 1 black threshold1[0] middle byte
0x802070B4	SNR1_AEC_BLACK_THRE1_0_B0	0x00	RW	Bit[7:0]: Sensor 1 black threshold1[0] low byte
0x802070B5	SNR1_AEC_BLACK_THRE2_0_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 black threshold2[0] high byte
0x802070B6	SNR1_AEC_BLACK_THRE2_0_B1	0x20	RW	Bit[7:0]: Sensor 1 black threshold2[0] middle byte
0x802070B7	SNR1_AEC_BLACK_THRE2_0_B0	0x00	RW	Bit[7:0]: Sensor 1 black threshold2[0] low byte
0x802070B8	SNR1_AEC_BLACK_WEIGHT1_0	0x10	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 black weight1[0]
0x802070B9	SNR1_AEC_BLACK_WEIGHT2_0	0x14	RW	Bit[7:6]: Reserved Bit[6:0]: Sensor 1 black weight2[0]
0x802070BA	SNR1_AEC_SATURATE_THRE1_0_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 saturate threshold1[0] high byte
0x802070BB	SNR1_AEC_SATURATE_THRE1_0_B1	0x08	RW	Bit[7:0]: Sensor 1 saturate threshold1[0] middle byte
0x802070BC	SNR1_AEC_SATURATE_THRE1_0_B0	0x00	RW	Bit[7:0]: Sensor 1 saturate threshold1[0] low byte
0x802070BD	SNR1_AEC_SATURATE_THRE2_0_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 saturate threshold2[0] high byte
0x802070BE	SNR1_AEC_SATURATE_THRE2_0_B1	0x10	RW	Bit[7:0]: Sensor 1 saturate threshold2[0] middle byte
0x802070BF	SNR1_AEC_SATURATE_THRE2_0_B0	0x00	RW	Bit[7:0]: Sensor 1 saturate threshold2[0] low byte
0x802070C0	SNR1_AEC_SATURATE_WEIGHT1_0	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 saturate weight1[0]
0x802070C1	SNR1_AEC_SATURATE_WEIGHT2_0	0x12	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 saturate weight2[0]
0x802070C2	SNR1_AEC_BLACK_THRE1_1_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 black threshold1[1] high byte
0x802070C3	SNR1_AEC_BLACK_THRE1_1_B1	0x10	RW	Bit[7:0]: Sensor 1 black threshold1[1] middle byte

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table 4-31 AEC/AGC registers (sheet 12 of 13)

address	register name	default value	R/W	description
0x802070C4	SNR1_AEC_BLACK_THRE1_1_B0	0x00	RW	Bit[7:0]: Sensor 1 black threshold1[1] low byte
0x802070C5	SNR1_AEC_BLACK_THRE2_1_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 black threshold2[1] high byte
0x802070C6	SNR1_AEC_BLACK_THRE2_1_B1	0x40	RW	Bit[7:0]: Sensor 1 black threshold2[1] middle byte
0x802070C7	SNR1_AEC_BLACK_THRE2_1_B0	0x00	RW	Bit[7:0]: Sensor 1 black threshold2[1] low byte
0x802070C8	SNR1_AEC_BLACK_WEIGHT1_1	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 black weight1[1]
0x802070C9	SNR1_AEC_BLACK_WEIGHT2_1	0x12	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 black weight2[1]
0x802070CA	SNR1_AEC_SATURATE_THRE1_1_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 saturate threshold1[1] high byte
0x802070CB	SNR1_AEC_SATURATE_THRE1_1_B1	0x04	RW	Bit[7:0]: Sensor 1 saturate threshold1[1] middle byte
0x802070CC	SNR1_AEC_SATURATE_THRE1_1_B0	0x00	RW	Bit[7:0]: Sensor 1 saturate threshold1[1] low byte
0x802070CD	SNR1_AEC_SATURATE_THRE2_1_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 saturate threshold2[1] high byte
0x802070CE	SNR1_AEC_SATURATE_THRE2_1_B1	0x20	RW	Bit[7:0]: Sensor 1 saturate threshold2[1] middle byte
0x802070CF	SNR1_AEC_SATURATE_THRE2_1_B0	0x00	RW	Bit[7:0]: Sensor 1 saturate threshold2[1] low byte
0x802070D0	SNR1_AEC_SATURATE_WEIGHT1_1	0x10	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 saturate weight1[1]
0x802070D1	SNR1_AEC_SATURATE_WEIGHT2_1	0x14	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 saturate weight2[1]
0x802070D2	SNR1_AEC_MEAN_Y_0_B1	–	R	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 mean Y[0] high byte
0x802070D3	SNR1_AEC_MEAN_Y_0_B0	–	R	Bit[7:0]: Sensor 1 mean Y[0] low byte
0x802070D4	SNR1_AEC_MEAN_Y_1_B1	–	R	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 mean Y[1] high byte

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table 4-31 AEC/AGC registers (sheet 13 of 13)

address	register name	default value	R/W	description
0x802070D5	SNR1_AEC_MEAN_Y_1_B0	–	R	Bit[7:0]: Sensor 1 mean Y[1] low byte
0x802070D6	SNR1_AEC_CNV_GAIN_RATIO	0x00	RW	Bit[7:0]: Sensor 1 conversion gain ratio (firmware use only)

4.22 AEC PK control

table 4-32 AEC PK control registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x80207D80	SNR0_PK_EXP_L_H	0x00	RW	Bit[7:0]: Sensor 0 long exposure value[15:8]
0x80207D81	SNR0_PK_EXP_L_L	0x80	RW	Bit[7:0]: Sensor 0 long exposure value[7:0]
0x80207D82	SNR0_PK_EXP_S_H	0x00	RW	Bit[7:0]: Sensor 0 short exposure value[15:8]
0x80207D83	SNR0_PK_EXP_S_L	0x50	RW	Bit[7:0]: Sensor 0 short exposure value[7:0]
0x80207D84	SNR0_PK_EXP_VS	0x2A	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure value
0x80207D86	SNR0_PK_REAL_GAIN_L_H	0x01	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure real gain[11:5]
0x80207D87	SNR0_PK_REAL_GAIN_L_L	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 long exposure real gain[4:0]
0x80207D88	SNR0_PK_REAL_GAIN_S_H	0x01	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure real gain[11:5]
0x80207D89	SNR0_PK_REAL_GAIN_S_L	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 short exposure real gain[4:0]
0x80207D8A	SNR0_PK_REAL_GAIN_VS_H	0x01	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure real gain[11:5]

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table 4-32 AEC PK control registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x80207D8B	SNR0_PK_REAL_GAIN_VS_L	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 very short exposure real gain[4:0]
0x80207D8C	SNR0_PK_DIG_GAIN_L_H	0x02	RW	Bit[7:0]: Sensor 0 long exposure digital gain[15:8]
0x80207D8D	SNR0_PK_DIG_GAIN_L_L	0x00	RW	Bit[7:0]: Sensor 0 long exposure digital gain[7:0]
0x80207D8E	SNR0_PK_DIG_GAIN_S_H	0x02	RW	Bit[7:0]: Sensor 0 short exposure digital gain[15:8]
0x80207D8F	SNR0_PK_DIG_GAIN_S_L	0x00	RW	Bit[7:0]: Sensor 0 short exposure digital gain[7:0]
0x80207D90	SNR0_PK_DIG_GAIN_VS_H	0x02	RW	Bit[7:0]: Sensor 0 very short exposure digital gain[15:8]
0x80207D91	SNR0_PK_DIG_GAIN_VS_L	0x00	RW	Bit[7:0]: Sensor 0 very short exposure digital gain[7:0]
0x80207D92	SNR0_PK_BLC_L_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 target BLC of long exposure for sensor core[11:8]
0x80207D93	SNR0_PK_BLC_L_L	0x10	RW	Bit[7:0]: Sensor 0 target BLC of long exposure for sensor core[7:0]
0x80207D94	SNR0_PK_BLC_S_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 target BLC of short exposure for sensor core[11:8]
0x80207D95	SNR0_PK_BLC_S_L	0x10	RW	Bit[7:0]: Sensor 0 target BLC of short exposure for sensor core[7:0]
0x80207D96	SNR0_PK_BLC_VS_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 target BLC of very short exposure for sensor core[11:8]
0x80207D97	SNR0_PK_BLC_VS_L	0x10	RW	Bit[7:0]: Sensor 0 target BLC of very short exposure for sensor core[7:0]
0x80207D98	SNR0_HDR_BLC_L_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 BLC of long exposure for HDR process[11:8]

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table 4-32 AEC PK control registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x80207D99	SNR0_HDR_BLC_L_L	0x00	RW	Bit[7:0]: Sensor 0 BLC of long exposure for HDR process[7:0]
0x80207D9A	SNR0_HDR_BLC_S_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 BLC of short exposure for HDR process[11:8]
0x80207D9B	SNR0_HDR_BLC_S_L	0x00	RW	Bit[7:0]: Sensor 0 short exposure for HDR process[7:0]
0x80207D9C	SNR0_HDR_BLC_VS_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 BLC of very short exposure for HDR process[11:8]
0x80207D9D	SNR0_HDR_BLC_VS_L	0x00	RW	Bit[7:0]: Sensor 0 BLC of very short exposure for HDR process[7:0]
0x80207D9E	SNR0_PK_DAC_OFFSET_L	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 use this value for long exposure when dac_offset_corr is disabled
0x80207D9F	SNR0_PK_DAC_OFFSET_S	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 use this value for short exposure when dac_offset_corr is disabled
0x80207DA0	SNR0_PK_DAC_OFFSET_VS	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 use this value for very short exposure when dac_offset_corr is disabled
0x80207DA1	SNR0_PK_DAC_OFFSET_ STEP	0x0D	RW	Bit[7:0]: Sensor 0 DAC offset step
0x80207DA2	SNR0_PK_DARK_CURRENT_ L_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 measured dark current for long exposure[9:8] Filter mode (1/4 new, 3/4 old). Re-trigger overrides filter

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table 4-32 AEC PK control registers (sheet 4 of 8)

address	register name	default value	R/W	description
0x80207DA3	SNR0_PK_DARK_CURRENT_L_L	0x00	RW	Bit[7:0]: Sensor 0 measured dark current for long exposure[7:0] Filter mode (1/4 new, 3/4 old). Re-trigger overrides filter
0x80207DA4	SNR0_PK_DARK_CURRENT_S_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 measured dark current for short exposure[9:8] Filter mode (1/4 new, 3/4 old). Re-trigger overrides filter
0x80207DA5	SNR0_PK_DARK_CURRENT_S_L	0x00	RW	Bit[7:0]: Sensor 0 measured dark current for short exposure[7:0] Filter mode (1/4 new, 3/4 old). Re-trigger overrides filter
0x80207DA6	SNR0_PK_DARK_CURRENT_VS_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 measured dark current for very short exposure[9:8] Filter mode(1/4 new, 3/4 old). Re-trigger overrides filter
0x80207DA7	SNR0_PK_DARK_CURRENT_VS_L	0x00	RW	Bit[7:0]: Sensor 0 measured dark current for very short exposure[7:0] Filter mode(1/4 new, 3/4 old). Re-trigger overrides filter
0x80207DB0	SNR1_PK_EXP_L_H	0x00	RW	Bit[7:0]: Sensor 1 long exposure value[15:8]
0x80207DB1	SNR1_PK_EXP_L_L	0x80	RW	Bit[7:0]: Sensor 1 long exposure value[7:0]
0x80207DB2	SNR1_PK_EXP_S_H	0x00	RW	Bit[7:0]: Sensor 1 short exposure value[15:8]
0x80207DB3	SNR1_PK_EXP_S_L	0x50	RW	Bit[7:0]: Sensor 1 short exposure value[7:0]
0x80207DB4	SNR1_PK_EXP_VS	0x2A	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure value

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table 4-32 AEC PK control registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x80207DB6	SNR1_PK_REAL_GAIN_L_H	0x01	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure real gain[11:5]
0x80207DB7	SNR1_PK_REAL_GAIN_L_L	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 long exposure real gain[4:0]
0x80207DB8	SNR1_PK_REAL_GAIN_S_H	0x01	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure real gain[11:5]
0x80207DB9	SNR1_PK_REAL_GAIN_S_L	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 short exposure real gain[4:0]
0x80207DBA	SNR1_PK_REAL_GAIN_VS_H	0x01	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure real gain[11:5]
0x80207DBB	SNR1_PK_REAL_GAIN_VS_L	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 very short exposure real gain[4:0]
0x80207DBC	SNR1_PK_DIG_GAIN_L_H	0x02	RW	Bit[7:0]: Sensor 1 long exposure digital gain[15:8]
0x80207DBD	SNR1_PK_DIG_GAIN_L_L	0x00	RW	Bit[7:0]: Sensor 1 long exposure digital gain[7:0]
0x80207DBE	SNR1_PK_DIG_GAIN_S_H	0x02	RW	Bit[7:0]: Sensor 1 short exposure digital gain[15:8]
0x80207DBF	SNR1_PK_DIG_GAIN_S_L	0x00	RW	Bit[7:0]: Sensor 1 short exposure digital gain[7:0]
0x80207DC0	SNR1_PK_DIG_GAIN_VS_H	0x02	RW	Bit[7:0]: Sensor 1 very short exposure digital gain[15:8]
0x80207DC1	SNR1_PK_DIG_GAIN_VS_L	0x00	RW	Bit[7:0]: Sensor 1 very short exposure digital gain[7:0]
0x80207DC2	SNR1_PK_BLC_L_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 target BLC of long exposure for sensor core[11:8]
0x80207DC3	SNR1_PK_BLC_L_L	0x10	RW	Bit[7:0]: Sensor 1 target BLC of long exposure for sensor core[7:0]

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table 4-32 AEC PK control registers (sheet 6 of 8)

address	register name	default value	R/W	description
0x80207DC4	SNR1_PK_BLC_S_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 target BLC of short exposure for sensor core[11:8]
0x80207DC5	SNR1_PK_BLC_S_L	0x10	RW	Bit[7:0]: Sensor 1 target BLC of short exposure for sensor core[7:0]
0x80207DC6	SNR1_PK_BLC_VS_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 target BLC of very short exposure for sensor core[11:8]
0x80207DC7	SNR1_PK_BLC_VS_L	0x10	RW	Bit[7:0]: Sensor 1 target BLC of very short exposure for sensor core[7:0]
0x80207DC8	SNR0_HDR_BLC_L_	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 BLC of long exposure for HDR process[11:8]
0x80207DC9	SNR0_HDR_BLC_L_L	0x00	RW	Bit[7:0]: Sensor 0 BLC of long exposure for HDR process[7:0]
0x80207DCA	SNR0_HDR_BLC_S_H	0x00	RW	Bit[7:0]: Reserved Bit[3:0]: Sensor 0 BLC of short exposure for HDR process[11:8]
0x80207DCB	SNR0_HDR_BLC_S_L	0x00	RW	Bit[7:0]: Sensor 0 BLC of short exposure for HDR process[7:0]
0x80207DCC	SNR0_HDR_BLC_VS_H	0x00	RW	Bit[7:0]: Reserved Bit[3:0]: Sensor 0 BLC of very short exposure for HDR process[11:8]
0x80207DCD	SNR0_HDR_BLC_VS_L	0x00	RW	Bit[7:0]: Sensor 0 BLC of very short exposure for HDR process[7:0]
0x80207DCE	SNR1_PK_DAC_OFFSET_L	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 uses this value for long exposure when dac_offset_corr is disabled

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table 4-32 AEC PK control registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x80207DCF	SNR1_PK_DAC_OFFSET_S	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 uses this value for short exposure when dac_offset_corr is disabled
0x80207DD0	SNR1_PK_DAC_OFFSET_VS	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 uses this value for very short exposure when dac_offset_corr is disabled
0x80207DD1	SNR1_PK_DAC_OFFSET_STEP	0x0D	RW	Bit[7:0]: Sensor 1 DAC offset step
0x80207DD2	SNR1_PK_DARK_CURRENT_L_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 measured dark current for long exposure[9:8] Filter mode (1/4 new, 3/4 old). Re-trigger overrides filter
0x80207DD3	SNR1_PK_DARK_CURRENT_L_L	0x00	RW	Bit[7:0]: Sensor 1 measured dark current for long exposure[7:0] Filter mode (1/4 new, 3/4 old). Re-trigger overrides filter
0x80207DD4	SNR1_PK_DARK_CURRENT_S_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 measured dark current for short exposure[9:8] Filter mode (1/4 new, 3/4 old). Re-trigger overrides filter
0x80207DD5	SNR1_PK_DARK_CURRENT_S_L	0x00	RW	Bit[7:0]: Sensor 1 measured dark current for short exposure[7:0] Filter mode (1/4 new, 3/4 old). Re-trigger overrides filter
0x80207DD6	SNR1_PK_DARK_CURRENT_VS_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 measured dark current for very short exposure[9:8] Filter mode (1/4 new, 3/4 old). Re-trigger overrides filter

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table 4-32 AEC PK control registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x80207DD7	SNR1_PK_DARK_CURRENT_VS_L	0x00	RW	Bit[7:0]: Sensor 1 measured dark current for very short exposure[7:0] Filter mode (1/4 new, 3/4 old). Re-trigger overrides filter

4.23 auto white balance gain (AWBG) control

table 4-33 AWBG control registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x80206100	SNR0_AWBG_R_GAIN_L_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 R gain[11:8] for long exposure
0x80206101	SNR0_AWBG_R_GAIN_L_L	0x00	RW	Bit[7:0]: Sensor 0 R gain[7:0] for long exposure
0x80206102	SNR0_AWBG_GR_GAIN_L_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 Gr gain[11:8] for long exposure
0x80206103	SNR0_AWBG_GR_GAIN_L_L	0x00	RW	Bit[7:0]: Sensor 0 Gr gain[7:0] for long exposure
0x80206104	SNR0_AWBG_GB_GAIN_L_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 Gb gain[11:8] for long exposure
0x80206105	SNR0_AWBG_GB_GAIN_L_L	0x00	RW	Bit[7:0]: Sensor 0 Gb gain[7:0] for long exposure
0x80206106	SNR0_AWBG_B_GAIN_L_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 B gain[11:8] for long exposure
0x80206107	SNR0_AWBG_B_GAIN_L_L	0x00	RW	Bit[7:0]: Sensor 0 B gain[7:0] for long exposure
0x80206108	SNR0_AWBG_R_GAIN_S_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 R gain[11:8] for short exposure
0x80206109	SNR0_AWBG_R_GAIN_S_L	0x00	RW	Bit[7:0]: Sensor 0 R gain[7:0] for short exposure

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table 4-33 AWBG control registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x8020610A	SNR0_AWBG_GR_GAIN _S_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 Gr gain[11:8] for short exposure
0x8020610B	SNR0_AWBG_GR_GAIN _S_L	0x00	RW	Bit[7:0]: Sensor 0 Gr gain[7:0] for short exposure
0x8020610C	SNR0_AWBG_GB_GAIN _S_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 Gb gain[11:8] for short exposure
0x8020610D	SNR0_AWBG_GB_GAIN _S_L	0x00	RW	Bit[7:0]: Sensor 0 Gb gain[7:0] for short exposure
0x8020610E	SNR0_AWBG_B_GAIN _S_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 B gain[11:8] for short exposure
0x8020610F	SNR0_AWBG_B_GAIN _S_L	0x00	RW	Bit[7:0]: Sensor 0 B gain[7:0] for short exposure
0x80206110	SNR0_AWBG_R_GAIN _V_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 R gain[11:8] for very short exposure
0x80206111	SNR0_AWBG_R_GAIN _V_L	0x00	RW	Bit[7:0]: Sensor 0 R gain[7:0] for very short exposure
0x80206112	SNR0_AWBG_GR_GAIN _V_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 Gr gain[11:8] for very short exposure
0x80206113	SNR0_AWBG_GR_GAIN _V_L	0x00	RW	Bit[7:0]: Sensor 0 Gr gain[7:0] for very short exposure
0x80206114	SNR0_AWBG_GB_GAIN _V_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 Gb gain[11:8] for very short exposure
0x80206115	SNR0_AWBG_GB_GAIN _V_L	0x00	RW	Bit[7:0]: Sensor 0 Gb gain[7:0] for very short exposure
0x80206116	SNR0_AWBG_B_GAIN _V_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 B gain[11:8] for very short exposure
0x80206117	SNR0_AWBG_B_GAIN _V_L	0x00	RW	Bit[7:0]: Sensor 0 B gain[7:0] for very short exposure
0x80206119	SNR0_AWBG_R_ OFFSET_L_H	0x00	RW	Bit[7:0]: Sensor 0 R offset[23:16] for long exposure
0x8020611A	SNR0_AWBG_R_ OFFSET_L_M	0x00	RW	Bit[7:0]: Sensor 0 R offset[15:8] for long exposure

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table 4-33 AWBG control registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x8020611B	SNR0_AWBG_R_OFFSET_L_L	0x00	RW	Bit[7:0]: Sensor 0 R offset[7:0] for long exposure
0x8020611D	SNR0_AWBG_GR_OFFSET_L_H	0x00	RW	Bit[7:0]: Sensor 0 Gr offset[23:16] for long exposure
0x8020611E	SNR0_AWBG_GR_OFFSET_L_M	0x00	RW	Bit[7:0]: Sensor 0 Gr offset[15:8] for long exposure
0x8020611F	SNR0_AWBG_GR_OFFSET_L_L	0x00	RW	Bit[7:0]: Sensor 0 Gr offset[7:0] for long exposure
0x80206121	SNR0_AWBG_GB_OFFSET_L_H	0x00	RW	Bit[7:0]: Sensor 0 Gb offset[23:16] for long exposure
0x80206122	SNR0_AWBG_GB_OFFSET_L_M	0x00	RW	Bit[7:0]: Sensor 0 Gb offset[15:8] for long exposure
0x80206123	SNR0_AWBG_GB_OFFSET_L_L	0x00	RW	Bit[7:0]: Sensor 0 Gb offset[7:0] for long exposure
0x80206125	SNR0_AWBG_B_OFFSET_L_H	0x00	RW	Bit[7:0]: Sensor 0 B offset[23:16] for long exposure
0x80206126	SNR0_AWBG_B_OFFSET_L_M	0x00	RW	Bit[7:0]: Sensor 0 R offset[15:8] for long exposure
0x80206127	SNR0_AWBG_B_OFFSET_L_L	0x00	RW	Bit[7:0]: Sensor 0 R offset[7:0] for long exposure
0x80206129	SNR0_AWBG_R_OFFSET_S_H	0x00	RW	Bit[7:0]: Sensor 0 R offset[23:16] for short exposure
0x8020612A	SNR0_AWBG_R_OFFSET_S_M	0x00	RW	Bit[7:0]: Sensor 0 R offset[15:8] for short exposure
0x8020612B	SNR0_AWBG_R_OFFSET_S_L	0x00	RW	Bit[7:0]: Sensor 0 R offset[7:0] for short exposure
0x8020612D	SNR0_AWBG_GR_OFFSET_S_H	0x00	RW	Bit[7:0]: Sensor 0 Gr offset[23:16] for short exposure
0x8020612E	SNR0_AWBG_GR_OFFSET_S_M	0x00	RW	Bit[7:0]: Sensor 0 Gr offset[15:8] for short exposure
0x8020612F	SNR0_AWBG_GR_OFFSET_S_L	0x00	RW	Bit[7:0]: Sensor 0 Gr offset[7:0] for short exposure
0x80206131	SNR0_AWBG_GB_OFFSET_S_H	0x00	RW	Bit[7:0]: Sensor 0 Gb offset[23:16] for short exposure
0x80206132	SNR0_AWBG_GB_OFFSET_S_M	0x00	RW	Bit[7:0]: Sensor 0 Gb offset[15:8] for short exposure
0x80206133	SNR0_AWBG_GB_OFFSET_S_L	0x00	RW	Bit[7:0]: Sensor 0 Gb offset[7:0] for short exposure

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table 4-33 AWBG control registers (sheet 4 of 8)

address	register name	default value	R/W	description
0x80206135	SNR0_AWBG_B_ OFFSET_S_H	0x00	RW	Bit[7:0]: Sensor 0 B offset[23:16] for short exposure
0x80206136	SNR0_AWBG_B_ OFFSET_S_M	0x00	RW	Bit[7:0]: Sensor 0 R offset[15:8] for short exposure
0x80206137	SNR0_AWBG_B_ OFFSET_S_L	0x00	RW	Bit[7:0]: Sensor 0 R offset[7:0] for short exposure
0x80206139	SNR0_AWBG_R_ OFFSET_V_H	0x00	RW	Bit[7:0]: Sensor 0 R offset[23:16] for very short exposure
0x8020613A	SNR0_AWBG_R_ OFFSET_V_M	0x00	RW	Bit[7:0]: Sensor 0 R offset[15:8] for very short exposure
0x8020613B	SNR0_AWBG_R_ OFFSET_V_L	0x00	RW	Bit[7:0]: Sensor 0 R offset[7:0] for very short exposure
0x8020613D	SNR0_AWBG_GR_ OFFSET_V_H	0x00	RW	Bit[7:0]: Sensor 0 Gr offset[23:16] for very short exposure
0x8020613E	SNR0_AWBG_GR_ OFFSET_V_M	0x00	RW	Bit[7:0]: Sensor 0 Gr offset[15:8] for very short exposure
0x8020613F	SNR0_AWBG_GR_ OFFSET_V_L	0x00	RW	Bit[7:0]: Sensor 0 Gr offset[7:0] for very short exposure
0x80206141	SNR0_AWBG_GB_ OFFSET_V_H	0x00	RW	Bit[7:0]: Sensor 0 Gb offset[23:16] for very short exposure
0x80206142	SNR0_AWBG_GB_ OFFSET_V_M	0x00	RW	Bit[7:0]: Sensor 0 Gb offset[15:8] for very short exposure
0x80206143	SNR0_AWBG_GB_ OFFSET_V_L	0x00	RW	Bit[7:0]: Sensor 0 Gb offset[7:0] for very short exposure
0x80206145	SNR0_AWBG_B_ OFFSET_V_H	0x00	RW	Bit[7:0]: Sensor 0 B offset[23:16] for very short exposure
0x80206146	SNR0_AWBG_B_ OFFSET_V_M	0x00	RW	Bit[7:0]: Sensor 0 R offset[15:8] for very short exposure
0x80206147	SNR0_AWBG_B_ OFFSET_V_L	0x00	RW	Bit[7:0]: Sensor 0 R offset[7:0] for very short exposure
0x80206150	SNR1_AWBG_R_GAIN _L_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 R gain[11:8] for long exposure
0x80206151	SNR1_AWBG_R_GAIN _L_L	0x00	RW	Bit[7:0]: Sensor 1 R gain[7:0] for long exposure
0x80206152	SNR1_AWBG_GR_GAIN _L_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 Gr gain[11:8] for long exposure

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table 4-33 AWBG control registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x80206153	SNR1_AWBG_GR_GAIN _L_L	0x00	RW	Bit[7:0]: Sensor 1 Gr gain[7:0] for long exposure
0x80206154	SNR1_AWBG_GB_GAIN _L_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 Gb gain[11:8] for long exposure
0x80206155	SNR1_AWBG_GB_GAIN _L_L	0x00	RW	Bit[7:0]: Sensor 1 Gb gain[7:0] for long exposure
0x80206156	SNR1_AWBG_B_GAIN _L_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 B gain[11:8] for long exposure
0x80206157	SNR1_AWBG_B_GAIN _L_L	0x00	RW	Bit[7:0]: Sensor 1 B gain[7:0] for long exposure
0x80206158	SNR1_AWBG_R_GAIN _S_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 R gain[11:8] for short exposure
0x80206159	SNR1_AWBG_R_GAIN _S _L	0x00	RW	Bit[7:0]: Sensor 1 R gain[7:0] for short exposure
0x8020615A	SNR1_AWBG_GR_GAIN _S_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 Gr gain[11:8] for short exposure
0x8020615B	SNR1_AWBG_GR_GAIN _S _L	0x00	RW	Bit[7:0]: Sensor 1 Gr gain[7:0] for short exposure
0x8020615C	SNR1_AWBG_GB_GAIN _S_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 Gb gain[11:8] for short exposure
0x8020615D	SNR1_AWBG_GB_GAIN _S _L	0x00	RW	Bit[7:0]: Sensor 1 Gb gain[7:0] for short exposure
0x8020615E	SNR1_AWBG_B_GAIN _S_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 B gain[11:8] for short exposure
0x8020615F	SNR1_AWBG_B_GAIN _S _L	0x00	RW	Bit[7:0]: Sensor 1 B gain[7:0] for short exposure
0x80206160	SNR1_AWBG_R_GAIN _V_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 R gain[11:8] for very short exposure
0x80206161	SNR1_AWBG_R_GAIN _V _L	0x00	RW	Bit[7:0]: Sensor 1 R gain[7:0] for very short exposure
0x80206162	SNR1_AWBG_GR_GAIN _V_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 Gr gain[11:8] for very short exposure

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table 4-33 AWBG control registers (sheet 6 of 8)

address	register name	default value	R/W	description
0x80206163	SNR1_AWBG_GR_GAIN _V _L	0x00	RW	Bit[7:0]: Sensor 1 Gr gain[7:0] for very short exposure
0x80206164	SNR1_AWBG_GB_GAIN _V_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 Gb gain[11:8] for very short exposure
0x80206165	SNR1_AWBG_GB_GAIN _V _L	0x00	RW	Bit[7:0]: Sensor 1 Gb gain[7:0] for very short exposure
0x80206166	SNR1_AWBG_B_GAIN _V_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 B gain[11:8] for very short exposure
0x80206167	SNR1_AWBG_B_GAIN _V _L	0x00	RW	Bit[7:0]: Sensor 1 B gain[7:0] for very short exposure
0x80206169	SNR1_AWBG_R_ OFFSET_L_H	0x00	RW	Bit[7:0]: Sensor 1 R offset[23:16] for long exposure
0x8020616A	SNR1_AWBG_R_ OFFSET_L_M	0x00	RW	Bit[7:0]: Sensor 1 R offset[15:8] for long exposure
0x8020616B	SNR1_AWBG_R_ OFFSET_L_L	0x00	RW	Bit[7:0]: Sensor 1 R offset[7:0] for long exposure
0x8020616D	SNR1_AWBG_GR_ OFFSET_L_H	0x00	RW	Bit[7:0]: Sensor 1 Gr offset[23:16] for long exposure
0x8020616E	SNR1_AWBG_GR_ OFFSET_L_M	0x00	RW	Bit[7:0]: Sensor 1 Gr offset[15:8] for long exposure
0x8020616F	SNR1_AWBG_GR_ OFFSET_L_L	0x00	RW	Bit[7:0]: Sensor 1 Gr offset[7:0] for long exposure
0x80206171	SNR1_AWBG_GB_ OFFSET_L_H	0x00	RW	Bit[7:0]: Sensor 1 Gb offset[23:16] for long exposure
0x80206172	SNR1_AWBG_GB_ OFFSET_L_M	0x00	RW	Bit[7:0]: Sensor 1 Gb offset[15:8] for long exposure
0x80206173	SNR1_AWBG_GB_ OFFSET_L_L	0x00	RW	Bit[7:0]: Sensor 1 Gb offset[7:0] for long exposure
0x80206175	SNR1_AWBG_B_ OFFSET_L_H	0x00	RW	Bit[7:0]: Sensor 1 B offset[23:16] for long exposure
0x80206176	SNR1_AWBG_B_ OFFSET_L_M	0x00	RW	Bit[7:0]: Sensor 1 R offset[15:8] for long exposure
0x80206177	SNR1_AWBG_B_ OFFSET_L_L	0x00	RW	Bit[7:0]: Sensor 1 R offset[7:0] for long exposure
0x80206179	SNR1_AWBG_R_ OFFSET_S_H	0x00	RW	Bit[7:0]: Sensor 1 R offset[23:16] for short exposure

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table 4-33 AWBG control registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x8020617A	SNR1_AWBG_R_ OFFSET_S_M	0x00	RW	Bit[7:0]: Sensor 1 R offset[15:8] for short exposure
0x8020617B	SNR1_AWBG_R_ OFFSET_S_L	0x00	RW	Bit[7:0]: Sensor 1 R offset[7:0] for short exposure
0x8020617D	SNR1_AWBG_GR_ OFFSET_S_H	0x00	RW	Bit[7:0]: Sensor 1 Gr offset[23:16] for short exposure
0x8020617E	SNR1_AWBG_GR_ OFFSET_S_M	0x00	RW	Bit[7:0]: Sensor 1 Gr offset[15:8] for short exposure
0x8020617F	SNR1_AWBG_GR_ OFFSET_S_L	0x00	RW	Bit[7:0]: Sensor 1 Gr offset[7:0] for short exposure
0x80206181	SNR1_AWBG_GB_ OFFSET_S_H	0x00	RW	Bit[7:0]: Sensor 1 Gb offset[23:16] for short exposure
0x80206182	SNR1_AWBG_GB_ OFFSET_S_M	0x00	RW	Bit[7:0]: Sensor 1 Gb offset[15:8] for short exposure
0x80206183	SNR1_AWBG_GB_ OFFSET_S_L	0x00	RW	Bit[7:0]: Sensor 1 Gb offset[7:0] for short exposure
0x80206185	SNR1_AWBG_B_ OFFSET_S_H	0x00	RW	Bit[7:0]: Sensor 1 B offset[23:16] for short exposure
0x80206186	SNR1_AWBG_B_ OFFSET_S_M	0x00	RW	Bit[7:0]: Sensor 1 R offset[15:8] for short exposure
0x80206187	SNR1_AWBG_B_ OFFSET_S_L	0x00	RW	Bit[7:0]: Sensor 1 R offset[7:0] for short exposure
0x80206189	SNR1_AWBG_R_ OFFSET_V_H	0x00	RW	Bit[7:0]: Sensor 1 R offset[23:16] for very short exposure
0x8020618A	SNR1_AWBG_R_ OFFSET_V_M	0x00	RW	Bit[7:0]: Sensor 1 R offset[15:8] for very short exposure
0x8020618B	SNR1_AWBG_R_ OFFSET_V_L	0x00	RW	Bit[7:0]: Sensor 1 R offset[7:0] for very short exposure
0x8020618D	SNR1_AWBG_GR_ OFFSET_V_H	0x00	RW	Bit[7:0]: Sensor 1 Gr offset[23:16] for very short exposure
0x8020618E	SNR1_AWBG_GR_ OFFSET_V_M	0x00	RW	Bit[7:0]: Sensor 1 Gr offset[15:8] for very short exposure
0x8020618F	SNR1_AWBG_GR_ OFFSET_V_L	0x00	RW	Bit[7:0]: Sensor 1 Gr offset[7:0] for very short exposure
0x80206191	SNR1_AWBG_GB_ OFFSET_V_H	0x00	RW	Bit[7:0]: Sensor 1 Gb offset[23:16] for very short exposure
0x80206192	SNR1_AWBG_GB_ OFFSET_V_M	0x00	RW	Bit[7:0]: Sensor 1 Gb offset[15:8] for very short exposure

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table 4-33 AWBG control registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x80206193	SNR1_AWBG_GB_ OFFSET_V_L	0x00	RW	Bit[7:0]: Sensor 1 Gb offset[7:0] for very short exposure
0x80206195	SNR1_AWBG_B_ OFFSET_V_H	0x00	RW	Bit[7:0]: Sensor 1 B offset[23:16] for very short exposure
0x80206196	SNR1_AWBG_B_ OFFSET_V_M	0x00	RW	Bit[7:0]: Sensor 1 R offset[15:8] for very short exposure
0x80206197	SNR1_AWBG_B_ OFFSET_V_L	0x00	RW	Bit[7:0]: Sensor 1 R offset[7:0] for very short exposure

4.24 color interpolation (CIP) control

table 4-34 CIP registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x80207880	SNR0_CIP_CTRL_0	0x80	RW	Sensor 0 Control Bit[7:4]: Noise Y slope Bit[3:0]: Local sharpen
0x80207881	SNR0_CIP_CTRL_1	0x00	RW	Sensor 0 Control Bit[7:5]: Reserved Bit[4:1]: GbGr shift Bit[0]: GbGr remove enable
0x80207882	SNR0_CIP_NOISE_LIST_0	0x00	RW	Bit[7:0]: Sensor 0 noise list[0]
0x80207883	SNR0_CIP_NOISE_LIST_1	0x00	RW	Bit[7:0]: Sensor 0 noise list[1]
0x80207884	SNR0_CIP_NOISE_LIST_2	0x00	RW	Bit[7:0]: Sensor 0 noise list[2]
0x80207885	SNR0_CIP_NOISE_LIST_3	0x00	RW	Bit[7:0]: Sensor 0 noise list[3]
0x80207886	SNR0_CIP_NOISE_LIST_4	0x00	RW	Bit[7:0]: Sensor 0 noise list[4]
0x80207887	SNR0_CIP_NOISE_LIST_5	0x00	RW	Bit[7:0]: Sensor 0 noise list[5]
0x80207888	SNR0_CIP_NOISE_LIST_6	0x00	RW	Bit[7:0]: Sensor 0 noise list[6]
0x80207889	SNR0_CIP_NOISE_LIST_7	0x00	RW	Bit[7:0]: Sensor 0 noise list[7]
0x8020788A	SNR0_CIP_MIN_SHARPEN	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 minimum sharpen
0x8020788B	SNR0_CIP_MAX_SHARPEN	0x0C	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 maximum sharpen

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table 4-34 CIP registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x8020788C	SNR0_CIP_MIN_DETAIL	0x08	RW	Bit[7:0]: Sensor 0 minimum detail
0x8020788D	SNR0_CIP_MAX_DETAIL	0x0C	RW	Bit[7:0]: Sensor 0 maximum detail
0x8020788E	SNR0_CIP_MIN_SHARPEN _GAIN	0x02	RW	Bit[7:0]: Sensor 0 minimum sharpen gain
0x8020788F	SNR0_CIP_MAX_SHARPEN _GAIN	0x10	RW	Bit[7:0]: Sensor 0 maximum sharpen gain
0x80207890	SNR0_CIP_CTRL_2	0x60	RW	Sensor 0 Control Bit[7]: Reserved Bit[6]: Anti aliasing Bit[5]: FixH binning enable Bit[4]: CIP option Bit[3:2]: Binning pattern Bit[1:0]: Reserved
0x80207891	SNR0_CIP_EOF_DELAY	0x28	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 number of EOF signal delay cycles
0x80207892~ 0x80207895	RSVD	–	–	Reserved
0x80207896	SNR0_CIP_CTRL_3	0x10	RW	Sensor 0 Control Bit[7]: Anti-flickering enable Bit[6:5]: Reserved Bit[4:0]: Sharpen V coefficient
0x80207897	SNR1_CIP_CTRL_0	0x80	RW	Sensor 1 Control Bit[7:4]: Noise Y slope Bit[3:0]: Local sharpen
0x80207898	SNR1_CIP_CTRL_1	0x00	RW	Sensor 1 Control Bit[7:5]: Reserved Bit[4:1]: GbGr shift Bit[0]: GbGr remove enable
0x80207899	SNR1_CIP_NOISE_LIST_0	0x00	RW	Bit[7:0]: Sensor 1 noise list[0]
0x8020789A	SNR1_CIP_NOISE_LIST_1	0x00	RW	Bit[7:0]: Sensor 1 noise list[1]
0x8020789B	SNR1_CIP_NOISE_LIST_2	0x00	RW	Bit[7:0]: Sensor 1 noise list[2]
0x8020789C	SNR1_CIP_NOISE_LIST_3	0x00	RW	Bit[7:0]: Sensor 1 noise list[3]
0x8020789D	SNR1_CIP_NOISE_LIST_4	0x00	RW	Bit[7:0]: Sensor 1 noise list[4]
0x8020789E	SNR1_CIP_NOISE_LIST_5	0x00	RW	Bit[7:0]: Sensor 1 noise list[5]
0x8020789F	SNR1_CIP_NOISE_LIST_6	0x00	RW	Bit[7:0]: Sensor 1 noise list[6]
0x802078A0	SNR1_CIP_NOISE_LIST_7	0x00	RW	Bit[7:0]: Sensor 1 noise list[7]

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table 4-34 CIP registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x802078A1	SNR1_CIP_MIN_SHARPEN	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 minimum sharpen
0x802078A2	SNR1_CIP_MAX_SHARPEN	0x0C	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 maximum sharpen
0x802078A3	SNR1_CIP_MIN_DETAIL	0x08	RW	Bit[7:0]: Sensor 1 minimum detail
0x802078A4	SNR1_CIP_MAX_DETAIL	0x0C	RW	Bit[7:0]: Sensor 1 maximum detail
0x802078A5	SNR1_CIP_MIN_SHARPEN _GAIN	0x02	RW	Bit[7:0]: Sensor 1 minimum sharpen gain
0x802078A6	SNR1_CIP_MAX_SHARPEN _GAIN	0x10	RW	Bit[7:0]: Sensor 1 maximum sharpen gain
0x802078A7	SNR1_CIP_CTRL_2	0x60	RW	Sensor 1 Control Bit[6]: Anti aliasing Bit[5]: Fix H binning enable Bit[4]: CIP option Bit[3:2]: Binning pattern Bit[1:0]: Binning mode
0x802078A8	SNR1_CIP_EOF_DELAY	0x28	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 number of EOF signal delay cycles
0x802078A9	SNR1_CIP_AF_FILTER_ COEF_0	0x00	RW	Bit[7:0]: Sensor 1 AF filter coefficient[0]
0x802078AA	SNR1_CIP_AF_FILTER_ COEF_1	0x00	RW	Bit[7:0]: Sensor 1 AF filter coefficient[1]
0x802078AB	SNR1_CIP_AF_FILTER_ COEF_2	0x00	RW	Bit[7:0]: Sensor 1 AF filter coefficient[2]
0x802078AC	SNR1_CIP_AF_FILTER_ COEF_3	0x00	RW	Bit[7:0]: Sensor 1 AF filter coefficient[3]
0x802078AD	SNR1_CIP_CTRL_3	0x10	RW	Sensor 1 Control Bit[7]: Anti-flickering enable Bit[6:5]: Reserved Bit[4:0]: Sharpen V coefficient

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4.25 color correction matrix (CMX) control

table 4-35 CMX registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x80207900	SNR0_CMX_CTRL00	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for Day mode C00[11:8]
0x80207901	SNR0_CMX_CTRL01	0x00	RW	Bit[7:0]: Sensor 0 absolute value for Day mode C00[7:0]
0x80207902	SNR0_CMX_CTRL02	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for Day mode C01[11:8]
0x80207903	SNR0_CMX_CTRL03	0x00	RW	Bit[7:0]: Sensor 0 absolute value for Day mode C01[7:0]
0x80207904	SNR0_CMX_CTRL04	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for Day mode C10[11:8]
0x80207905	SNR0_CMX_CTRL05	0x00	RW	Bit[7:0]: Sensor 0 absolute value for Day mode C10[7:0]
0x80207906	SNR0_CMX_CTRL06	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for Day mode C11[11:8]
0x80207907	SNR0_CMX_CTRL07	0x00	RW	Bit[7:0]: Sensor 0 absolute value for Day mode C11[7:0]
0x80207908	SNR0_CMX_CTRL08	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for Day mode C20[11:8]
0x80207909	SNR0_CMX_CTRL09	0x00	RW	Bit[7:0]: Sensor 0 absolute value for Day mode C20[7:0]
0x8020790A	SNR0_CMX_CTRL0A	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for Day mode C21[11:8]
0x8020790B	SNR0_CMX_CTRL0B	0x00	RW	Bit[7:0]: Sensor 0 absolute value for Day mode C21[7:0]
0x8020790C	SNR0_CMX_CTRL0C	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for A mode C00[11:8]
0x8020790D	SNR0_CMX_CTRL0D	0x00	RW	Bit[7:0]: Sensor 0 absolute value for A mode C00[7:0]

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table 4-35 CMX registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x8020790E	SNR0_CMX_CTRL0E	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for A mode C01[11:8]
0x8020790F	SNR0_CMX_CTRL0F	0x00	RW	Bit[7:0]: Sensor 0 absolute value for A mode C01[7:0]
0x80207910	SNR0_CMX_CTRL10	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for A mode C10[11:8]
0x80207911	SNR0_CMX_CTRL11	0x00	RW	Bit[7:0]: Sensor 0 absolute value for A mode C10[7:0]
0x80207912	SNR0_CMX_CTRL12	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for A mode C11[11:8]
0x80207913	SNR0_CMX_CTRL13	0x00	RW	Bit[7:0]: Sensor 0 absolute value for A mode C11[7:0]
0x80207914	SNR0_CMX_CTRL14	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for A mode C20[11:8]
0x80207915	SNR0_CMX_CTRL15	0x00	RW	Bit[7:0]: Sensor 0 absolute value for A mode C20[7:0]
0x80207916	SNR0_CMX_CTRL16	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for A mode C21[11:8]
0x80207917	SNR0_CMX_CTRL17	0x00	RW	Bit[7:0]: Sensor 0 absolute value for A mode C21[7:0]
0x80207918	SNR0_CMX_CTRL18	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for CWF mode C00[11:8]
0x80207919	SNR0_CMX_CTRL19	0x00	RW	Bit[7:0]: Sensor 0 absolute value for CWF mode C00[7:0]
0x8020791A	SNR0_CMX_CTRL1A	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for CWF mode C01[11:8]
0x8020791B	SNR0_CMX_CTRL1B	0x00	RW	Bit[7:0]: Sensor 0 absolute value for CWF mode C01[7:0]
0x8020791C	SNR0_CMX_CTRL1C	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for CWF mode C10[11:8]
0x8020791D	SNR0_CMX_CTRL1D	0x00	RW	Bit[7:0]: Sensor 0 absolute value for CWF mode C10[7:0]

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table 4-35 CMX registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x8020791E	SNR0_CMX_CTRL1E	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for CWF mode C11[11:8]
0x8020791F	SNR0_CMX_CTRL1F	0x00	RW	Bit[7:0]: Sensor 0 absolute value for CWF mode C11[7:0]
0x80207920	SNR0_CMX_CTRL20	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for CWF mode C20[11:8]
0x80207921	SNR0_CMX_CTRL21	0x00	RW	Bit[7:0]: Sensor 0 absolute value for CWF mode C20[7:0]
0x80207922	SNR0_CMX_CTRL22	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 absolute value for CWF mode C21[11:8]
0x80207923	SNR0_CMX_CTRL23	0x00	RW	Bit[7:0]: Sensor 0 absolute value for CWF mode C21[7:0]
0x80207928	SNR0_CMX_CTRL28	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 color matrix CT list0[9:8]
0x80207929	SNR0_CMX_CTRL29	0x00	RW	Bit[7:0]: Sensor 0 color matrix CT list0[7:0]
0x8020792A	SNR0_CMX_CTRL2A	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 color matrix CT list1[9:8]
0x8020792B	SNR0_CMX_CTRL2B	0x00	RW	Bit[7:0]: Sensor 0 color matrix CT list1[7:0]
0x8020792C	SNR0_CMX_CTRL2C	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 color matrix CT list2[9:8]
0x8020792D	SNR0_CMX_CTRL2D	0x00	RW	Bit[7:0]: Sensor 0 color matrix CT list2[7:0]
0x8020792E	SNR0_CMX_CTRL2E	0x00	RW	Bit[7:6]: Reserved Bit[5]: Sensor 0 sign bits for C00 Day mode Bit[4]: Sensor 0 sign bits for C01 Day mode Bit[3]: Sensor 0 sign bits for C10 Day mode Bit[2]: Sensor 0 sign bits for C11 Day mode Bit[1]: Sensor 0 sign bits for C20 Day mode Bit[0]: Sensor 0 sign bits for C21 Day mode

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table 4-35 CMX registers (sheet 4 of 8)

address	register name	default value	R/W	description
0x8020792F	SNR0_CMX_CTRL2F	0x00	RW	Bit[7:6]: Reserved Bit[5]: Sensor 0 sign bits for C00 A mode Bit[4]: Sensor 0 sign bits for C01 A mode Bit[3]: Sensor 0 sign bits for C10 A mode Bit[2]: Sensor 0 sign bits for C11 A mode Bit[1]: Sensor 0 sign bits for C20 A mode Bit[0]: Sensor 0 sign bits for C21 A mode
0x80207930	SNR0_CMX_CTRL30	0x00	RW	Bit[7:6]: Reserved Bit[5]: Sensor 0 sign bits for C00 CWF mode Bit[4]: Sensor 0 sign bits for C01 CWF mode Bit[3]: Sensor 0 sign bits for C10 CWF mode Bit[2]: Sensor 0 sign bits for C11 CWF mode Bit[1]: Sensor 0 sign bits for C20 CWF mode Bit[0]: Sensor 0 sign bits for C21 CWF mode
0x80207931	SNR0_CMX_CTRL31	0x01	RW	Bit[7:2]: Reserved Bit[1]: Sensor 0 auto CT enable Bit[0]: Sensor 0 auto factor enable
0x80207932	SNR0_CMX_CTRL32	0x40	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 maximum factor value
0x80207933	SNR0_CMX_CTRL33	0x40	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 minimum factor value
0x80207934	SNR0_CMX_CTRL34	0x07	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 minimum gain
0x80207935	SNR0_CMX_CTRL35	0x0F	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 maximum gain
0x80207950	SNR1_CMX_CTRL00	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for Day mode C00[11:8]
0x80207951	SNR1_CMX_CTRL01	0x00	RW	Bit[7:0]: Sensor 1 absolute value for Day mode C00[7:0]
0x80207952	SNR1_CMX_CTRL02	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for Day mode C01[11:8]
0x80207953	SNR1_CMX_CTRL03	0x00	RW	Bit[7:0]: Sensor 1 absolute value for Day mode C01[7:0]

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table 4-35 CMX registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x80207954	SNR1_CMX_CTRL04	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for Day mode C10[11:8]
0x80207955	SNR1_CMX_CTRL05	0x00	RW	Bit[7:0]: Sensor 1 absolute value for Day mode C10[7:0]
0x80207956	SNR1_CMX_CTRL06	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for Day mode C11[11:8]
0x80207957	SNR1_CMX_CTRL07	0x00	RW	Bit[7:0]: Sensor 1 absolute value for Day mode C11[7:0]
0x80207958	SNR1_CMX_CTRL08	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for Day mode C20[11:8]
0x80207959	SNR1_CMX_CTRL09	0x00	RW	Bit[7:0]: Sensor 1 absolute value for Day mode C20[7:0]
0x8020795A	SNR1_CMX_CTRL0A	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for Day mode C21[11:8]
0x8020795B	SNR1_CMX_CTRL0B	0x00	RW	Bit[7:0]: Sensor 1 absolute value for Day mode C21[7:0]
0x8020795C	SNR1_CMX_CTRL0C	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for A mode C00[11:8]
0x8020795D	SNR1_CMX_CTRL0D	0x00	RW	Bit[7:0]: Sensor 1 absolute value for A mode C00[7:0]
0x8020795E	SNR1_CMX_CTRL0E	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for A mode C01[11:8]
0x8020795F	SNR1_CMX_CTRL0F	0x00	RW	Bit[7:0]: Sensor 1 absolute value for A mode C01[7:0]
0x80207960	SNR1_CMX_CTRL10	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for A mode C10[11:8]
0x80207961	SNR1_CMX_CTRL11	0x00	RW	Bit[7:0]: Sensor 1 absolute value for A mode C10[7:0]
0x80207962	SNR1_CMX_CTRL12	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for A mode C11[11:8]
0x80207963	SNR1_CMX_CTRL13	0x00	RW	Bit[7:0]: Sensor 1 absolute value for A mode C11[7:0]

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table 4-35 CMX registers (sheet 6 of 8)

address	register name	default value	R/W	description
0x80207964	SNR1_CMX_CTRL14	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for A mode C20[11:8]
0x80207965	SNR1_CMX_CTRL15	0x00	RW	Bit[7:0]: Sensor 1 absolute value for A mode C20[7:0]
0x80207966	SNR1_CMX_CTRL16	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for A mode C21[11:8]
0x80207967	SNR1_CMX_CTRL17	0x00	RW	Bit[7:0]: Sensor 1 absolute value for A mode C21[7:0]
0x80207968	SNR1_CMX_CTRL18	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for CWF mode C00[11:8]
0x80207969	SNR1_CMX_CTRL19	0x00	RW	Bit[7:0]: Sensor 1 absolute value for CWF mode C00[7:0]
0x8020796A	SNR1_CMX_CTRL1A	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for CWF mode C01[11:8]
0x8020796B	SNR1_CMX_CTRL1B	0x00	RW	Bit[7:0]: Sensor 1 absolute value for CWF mode C01[7:0]
0x8020796C	SNR1_CMX_CTRL1C	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for CWF mode C10[11:8]
0x8020796D	SNR1_CMX_CTRL1D	0x00	RW	Bit[7:0]: Sensor 1 absolute value for CWF mode C10[7:0]
0x8020796E	SNR1_CMX_CTRL1E	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for CWF mode C11[11:8]
0x8020796F	SNR1_CMX_CTRL1F	0x00	RW	Bit[7:0]: Sensor 1 absolute value for CWF mode C11[7:0]
0x80207970	SNR1_CMX_CTRL20	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for CWF mode C20[11:8]
0x80207971	SNR1_CMX_CTRL21	0x00	RW	Bit[7:0]: Sensor 1 absolute value for CWF mode C20[7:0]
0x80207972	SNR1_CMX_CTRL22	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 absolute value for CWF mode C21[11:8]
0x80207973	SNR1_CMX_CTRL23	0x00	RW	Bit[7:0]: Sensor 1 absolute value for CWF mode C21[7:0]

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table 4-35 CMX registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x80207978	SNR1_CMX_CTRL28	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 color matrix CT list0[9:8]
0x80207979	SNR1_CMX_CTRL29	0x80	RW	Bit[7:0]: Sensor 1 color matrix CT list0[7:0]
0x8020797A	SNR1_CMX_CTRL2A	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 color matrix CT list1[9:8]
0x8020797B	SNR1_CMX_CTRL2B	0x80	RW	Bit[7:0]: Sensor 1 color matrix CT list1[7:0]
0x8020797C	SNR1_CMX_CTRL2C	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 color matrix CT list2[9:8]
0x8020797D	SNR1_CMX_CTRL2D	0x80	RW	Bit[7:0]: Sensor 1 color matrix CT list2[7:0]
0x8020797E	SNR1_CMX_CTRL2E	0x00	RW	Bit[7:6]: Reserved Bit[5]: Sensor 1 sign bits for C00 Day mode Bit[4]: Sensor 1 sign bits for C01 Day mode Bit[3]: Sensor 1 sign bits for C10 Day mode Bit[2]: Sensor 1 sign bits for C11 Day mode Bit[1]: Sensor 1 sign bits for C20 Day mode Bit[0]: Sensor 1 sign bits for C21 Day mode
0x8020797F	SNR1_CMX_CTRL2F	0x00	RW	Bit[7:6]: Reserved Bit[5]: Sensor 1 sign bits for C00 A mode Bit[4]: Sensor 1 sign bits for C01 A mode Bit[3]: Sensor 1 sign bits for C10 A mode Bit[2]: Sensor 1 sign bits for C11 A mode Bit[1]: Sensor 1 sign bits for C20 A mode Bit[0]: Sensor 1 sign bits for C21 A mode
0x80207980	SNR1_CMX_CTRL30	0x00	RW	Bit[7:6]: Reserved Bit[5]: Sensor 1 sign bits for C00 CWF mode Bit[4]: Sensor 1 sign bits for C01 CWF mode Bit[3]: Sensor 1 sign bits for C10 CWF mode Bit[2]: Sensor 1 sign bits for C11 CWF mode Bit[1]: Sensor 1 sign bits for C20 CWF mode Bit[0]: Sensor 1 sign bits for C21 CWF mode

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table 4-35 CMX registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x80207981	SNR1_CMX_CTRL31	0x01	RW	Bit[7:2]: Reserved Bit[1]: Sensor 1 auto CT enable Bit[0]: Sensor 1 auto factor enable
0x80207982	SNR1_CMX_CTRL32	0x40	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 maximum factor value
0x80207983	SNR1_CMX_CTRL33	0x40	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 minimum factor value
0x80207984	SNR1_CMX_CTRL34	0x07	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 minimum gain
0x80207985	SNR1_CMX_CTRL35	0x0F	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 maximum gain

4.26 combine control

table 4-36 combine registers (sheet 1 of 9)

address	register name	default value	R/W	description
0x80206800	SNR0_COMBINE _CTRL	0x1C	RW	Sensor 0 Combine Control Bit[7:5]: Reserved Bit[4]: Y 2x2 compensate error enable Bit[3]: S channel pre matrix enable Bit[2]: Compensate error enable Bit[1:0]: Combine work mode 00: HDRXCombine 01: HDRLong 10: HDRShor 11: HDRVShort
0x80206801	SNR0_COMBINE _THRE_0	0x95	RW	Bit[7:4]: Sensor 0 combine threshold 0 for long Bit[3:0]: Sensor 0 combine threshold 0 for short
0x80206802	SNR0_COMBINE _THRE_1	0xA8	RW	Bit[7:4]: Sensor 0 combine threshold 1 for long Bit[3:0]: Sensor 0 combine threshold 1 for short
0x80206803	SNR0_COMBINE _THRE_2	0xAA	RW	Bit[7:4]: Sensor 0 combine threshold 2 for long Bit[3:0]: Sensor 0 combine threshold 2 for short
0x80206804	SNR0_COMBINE _WEIGHT_0_0	0x80	RW	Bit[7:0]: Sensor 0 combine weight[0][0]
0x80206805	SNR0_COMBINE _WEIGHT_0_1	0x80	RW	Bit[7:0]: Sensor 0 combine weight[0][1]

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table 4-36 combine registers (sheet 2 of 9)

address	register name	default value	R/W	description
0x80206806	SNR0_COMBINE _WEIGHT_0_2	0x60	RW	Bit[7:0]: Sensor 0 combine weight[0][2]
0x80206807	SNR0_COMBINE _WEIGHT_0_3	0x40	RW	Bit[7:0]: Sensor 0 combine weight[0][3]
0x80206808	SNR0_COMBINE _WEIGHT_1_0	0x00	RW	Bit[7:0]: Sensor 0 combine weight[1][0]
0x80206809	SNR0_COMBINE _WEIGHT_1_1	0x80	RW	Bit[7:0]: Sensor 0 combine weight[1][1]
0x8020680A	SNR0_COMBINE _WEIGHT_1_2	0x40	RW	Bit[7:0]: Sensor 0 combine weight[1][2]
0x8020680B	SNR0_COMBINE _WEIGHT_1_3	0x20	RW	Bit[7:0]: Sensor 0 combine weight[1][3]
0x8020680C	SNR0_COMBINE _WEIGHT_2_0	0x80	RW	Bit[7:0]: Sensor 0 combine weight[2][0]
0x8020680D	SNR0_COMBINE _WEIGHT_2_1	0x60	RW	Bit[7:0]: Sensor 0 combine weight[2][1]
0x8020680E	SNR0_COMBINE _WEIGHT_2_2	0x00	RW	Bit[7:0]: Sensor 0 combine weight[2][2]
0x8020680F	SNR0_COMBINE _WEIGHT_2_3	0x00	RW	Bit[7:0]: Sensor 0 combine weight[2][3]
0x80206810	SNR0_COMBINE _WEIGHT_3_0	0x80	RW	Bit[7:0]: Sensor 0 combine weight[3][0]
0x80206811	SNR0_COMBINE _WEIGHT_3_1	0x80	RW	Bit[7:0]: Sensor 0 combine weight[3][1]
0x80206812	SNR0_COMBINE _WEIGHT_3_2	0x00	RW	Bit[7:0]: Sensor 0 combine weight[3][2]
0x80206813	SNR0_COMBINE _WEIGHT_3_3	0x00	RW	Bit[7:0]: Sensor 0 combine weight[3][3]
0x80206814	SNR0_COMBINE _SATURATE_ THRE_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 final saturate threshold[21:16]
0x80206815	SNR0_COMBINE _SATURATE_ THRE_B1	0x01	RW	Bit[7:0]: Sensor 0 final saturate threshold[15:8]
0x80206816	SNR0_COMBINE _SATURATE_ THRE_B0	0x00	RW	Bit[7:0]: Sensor 0 final saturate threshold[7:0]

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table 4-36 combine registers (sheet 3 of 9)

address	register name	default value	R/W	description
0x80206817	SNR0_COMBINE_TRAFFIC_S_TH_H	0x28	RW	Bit[7:0]: Sensor 0 traffic S threshold[15:8]
0x80206818	SNR0_COMBINE_TRAFFIC_S_TH_L	0x00	RW	Bit[7:0]: Sensor 0 traffic S threshold[7:0]
0x80206819	SNR0_COMBINE_TH_S_0_H	0x08	RW	Bit[7:0]: Sensor 0 m_nThS[0] high byte
0x8020681A	SNR0_COMBINE_TH_S_0_L	0x00	RW	Bit[7:0]: Sensor 0 m_nThS[0] low byte
0x8020681B	SNR0_COMBINE_TH_S_1_H	0x10	RW	Bit[7:0]: Sensor 0 m_nThS[1] high byte
0x8020681C	SNR0_COMBINE_TH_S_1_L	0x00	RW	Bit[7:0]: Sensor 0 m_nThS[1] low byte
0x8020681D	SNR0_COMBINE_THS_DINV	0x20	RW	Bit[7:0]: Sensor 0 m_nThSDinv Equal to (2^16)/(m_nThS[1]-m_nThS[0])
0x80206840	SNR0_COMBINE_GLOBAL_LOG_RATIO_0_H	0x10	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 global log ratio[0] (unsigned) high byte
0x80206841	SNR0_COMBINE_GLOBAL_LOG_RATIO_0_L	0x00	RW	Bit[7:0]: Sensor 0 global log ratio[0] (unsigned) low byte
0x80206842	SNR0_COMBINE_GLOBAL_LOG_RATIO_1_H	0x18	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 global log ratio[1] (unsigned) high byte
0x80206843	SNR0_COMBINE_GLOBAL_LOG_RATIO_1_L	0x00	RW	Bit[7:0]: Sensor 0 global log ratio[1] (unsigned) low byte
0x80206844	SNR0_COMBINE_LOG_E_0_H	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 LogE[0] (signed) high byte
0x80206845	SNR0_COMBINE_LOG_E_0_L	0x00	RW	Bit[7:0]: Sensor 0 LogE[0] (signed) low byte
0x80206846	SNR0_COMBINE_LOG_E_1_H	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 LogE[1] (signed) high byte
0x80206847	SNR0_COMBINE_LOG_E_1_L	0x00	RW	Bit[7:0]: Sensor 0 LogE[1] (signed) low byte
0x80206848	SNR0_COMBINE_INV_MLMS_APPLY_00_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 m_nInvMLMSApply[0][0] high byte

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table 4-36 combine registers (sheet 4 of 9)

address	register name	default value	R/W	description
0x80206849	SNR0_COMBINE_INV_MLMS_APPLY_00_L	0xDA	RW	Bit[7:0]: Sensor 0 m_nInvMLMSApply[0][0] low byte
0x8020684A	SNR0_COMBINE_INV_MLMS_APPLY_01_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 m_nInvMLMSApply[0][1] high byte
0x8020684B	SNR0_COMBINE_INV_MLMS_APPLY_01_L	0x1F	RW	Bit[7:0]: Sensor 0 m_nInvMLMSApply[0][1] low byte
0x8020684C	SNR0_COMBINE_INV_MLMS_APPLY_02_H	0x0	RW	Bit[7:2]: Reserved Bit[7:0]: Sensor 0 m_nInvMLMSApply[0][2] high byte
0x8020684D	SNR0_COMBINE_INV_MLMS_APPLY_02_L	0x07	RW	Bit[7:0]: Sensor 0 m_nInvMLMSApply[0][2] low byte
0x8020684E	SNR0_COMBINE_INV_MLMS_APPLY_10_H	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 m_nInvMLMSApply[1][0] high byte
0x8020684F	SNR0_COMBINE_INV_MLMS_APPLY_10_L	0xEB	RW	Bit[7:0]: Sensor 0 m_nInvMLMSApply[1][0] low byte
0x80206850	SNR0_COMBINE_INV_MLMS_APPLY_11_H	0x01	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 m_nInvMLMSApply[1][1] high byte
0x80206851	SNR0_COMBINE_INV_MLMS_APPLY_11_L	0x07	RW	Bit[7:0]: Sensor 0 m_nInvMLMSApply[1][1] low byte
0x80206852	SNR0_COMBINE_INV_MLMS_APPLY_12_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 m_nInvMLMSApply[1][2] high byte
0x80206853	SNR0_COMBINE_INV_MLMS_APPLY_12_L	0x0E	RW	Bit[7:0]: Sensor 0 m_nInvMLMSApply[1][2] low byte
0x80206854	SNR0_COMBINE_INV_MLMS_APPLY_20_H	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 m_nInvMLMSApply[2][0] high byte
0x80206855	SNR0_COMBINE_INV_MLMS_APPLY_20_L	0xF2	RW	Bit[7:0]: Sensor 0 m_nInvMLMSApply[2][0] low byte

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table 4-36 combine registers (sheet 5 of 9)

address	register name	default value	R/W	description
0x80206856	SNR0_COMBINE _INV_MLMS_ APPLY_21_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 m_nInvMLMSApply[2][1] high byte
0x80206857	SNR0_COMBINE _INV_MLMS_ APPLY_21_L	0x07	RW	Bit[7:0]: Sensor 0 m_nInvMLMSApply[2][1] low byte
0x80206858	SNR0_COMBINE _INV_MLMS_ APPLY_22_H	0x01	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 m_nInvMLMSApply[2][2] high byte
0x80206859	SNR0_COMBINE _INV_MLMS_ APPLY_22_L	0x07	RW	Bit[7:0]: Sensor 0 m_nInvMLMSApply[2][2] low byte
0x80206860	SNR0_COMBINE _E_0_H	–	R	Bit[7:0]: Sensor 0 E[0] (E[0], signed) high byte
0x80206861	SNR0_COMBINE _E_0_L	–	R	Bit[7:0]: Sensor 0 E[0] (E[0], signed) low byte
0x80206862	SNR0_COMBINE _E_1_H	–	R	Bit[7:0]: Sensor 0 E[1] (E[1], signed) high byte
0x80206863	SNR0_COMBINE _E_1_L	–	R	Bit[7:0]: Sensor 0 E[1] (E[1], signed) low byte
0x80206864	SNR0_COMBINE _SATURATE_ LEVEL	–	R	Bit[7:0]: Sensor 0 estimate saturate level
0x80206880	SNR1_COMBINE _CTRL	0x1C	RW	Sensor 1 Combine Control Signals Bit[7:5]: Reserved Bit[4]: Y 2x2 compensate error enable Bit[3]: S channel pre matrix enable Bit[2]: Compensate error enable Bit[1:0]: Combine work mode 00: HDRXCombine 01: HDRLong 10: HDRShor 11: HDRVShort
0x80206881	SNR1_COMBINE _THRE_0	0x95	RW	Bit[7:4]: Sensor 1 combine threshold 0 for long Bit[3:0]: Sensor 1 combine threshold 0 for short
0x80206882	SNR1_COMBINE _THRE_1	0xA8	RW	Bit[7:4]: Sensor 1 combine threshold 1 for long Bit[3:0]: Sensor 1 combine threshold 1 for short
0x80206883	SNR1_COMBINE _THRE_2	0xAA	RW	Bit[7:4]: Sensor 1 combine threshold 2 for long Bit[3:0]: Sensor 1 combine threshold 2 for short
0x80206884	SNR1_COMBINE _WEIGHT_0_0	0x80	RW	Bit[7:0]: Sensor 1 combine weight[0][0]

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table 4-36 combine registers (sheet 6 of 9)

address	register name	default value	R/W	description
0x80206885	SNR1_COMBINE _WEIGHT_0_1	0x80	RW	Bit[7:0]: Sensor 1 combine weight[0][1]
0x80206886	SNR1_COMBINE _WEIGHT_0_2	0x60	RW	Bit[7:0]: Sensor 1 combine weight[0][2]
0x80206887	SNR1_COMBINE _WEIGHT_0_3	0x40	RW	Bit[7:0]: Sensor 1 combine weight[0][3]
0x80206888	SNR1_COMBINE _WEIGHT_1_0	0x80	RW	Bit[7:0]: Sensor 1 combine weight[1][0]
0x80206889	SNR1_COMBINE _WEIGHT_1_1	0x80	RW	Bit[7:0]: Sensor 1 combine weight[1][1]
0x8020688A	SNR1_COMBINE _WEIGHT_1_2	0x40	RW	Bit[7:0]: Sensor 1 combine weight[1][2]
0x8020688B	SNR1_COMBINE _WEIGHT_1_3	0x20	RW	Bit[7:0]: Sensor 1 combine weight[1][3]
0x8020688C	SNR1_COMBINE _WEIGHT_2_0	0x80	RW	Bit[7:0]: Sensor 1 combine weight[2][0]
0x8020688D	SNR1_COMBINE _WEIGHT_2_1	0x60	RW	Bit[7:0]: Sensor 1 combine weight[2][1]
0x8020688E	SNR1_COMBINE _WEIGHT_2_2	0x00	RW	Bit[7:0]: Sensor 1 combine weight[2][2]
0x8020688F	SNR1_COMBINE _WEIGHT_2_3	0x00	RW	Bit[7:0]: Sensor 1 combine weight[2][3]
0x80206890	SNR1_COMBINE _WEIGHT_3_0	0x80	RW	Bit[7:0]: Sensor 1 combine weight[3][0]
0x80206891	SNR1_COMBINE _WEIGHT_3_1	0x80	RW	Bit[7:0]: Sensor 1 combine weight[3][1]
0x80206892	SNR1_COMBINE _WEIGHT_3_2	0x00	RW	Bit[7:0]: Sensor 1 combine weight[3][2]
0x80206893	SNR1_COMBINE _WEIGHT_3_3	0x00	RW	Bit[7:0]: Sensor 1 combine weight[3][3]
0x80206894	SNR1_COMBINE _SATURATE_ THRE_B2	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 final saturate threshold[21:16]
0x80206895	SNR1_COMBINE _SATURATE_ THRE_B1	0x01	RW	Bit[7:0]: Sensor 1 final saturate threshold[15:8]

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table 4-36 combine registers (sheet 7 of 9)

address	register name	default value	R/W	description
0x80206896	SNR1_COMBINE _SATURATE_ THRE_B0	0x00	RW	Bit[7:0]: Sensor 1 final saturate threshold[7:0]
0x80206897	SNR1_COMBINE _TRAFFIC_S_ TH_H	0x28	RW	Bit[7:0]: Sensor 1 traffic S threshold[15:8]
0x80206898	SNR1_COMBINE _TRAFFIC_S_ TH_L	0x00	RW	Bit[7:0]: Sensor 1 traffic S threshold[7:0]
0x80206899	SNR1_COMBINE _TH_S_0_H	0x08	RW	Bit[7:0]: Sensor 1 m_nThS[0] high byte
0x8020689A	SNR1_COMBINE _TH_S_0_L	0x00	RW	Bit[7:0]: Sensor 1 m_nThS[0] low byte
0x8020689B	SNR1_COMBINE _TH_S_1_H	0x10	RW	Bit[7:0]: Sensor 1 m_nThS[1] high byte
0x8020689C	SNR1_COMBINE _TH_S_1_L	0x00	RW	Bit[7:0]: Sensor 1 m_nThS[1] low byte
0x8020689D	SNR1_COMBINE _THS_DINV	0x20	RW	Bit[7:0]: Sensor 1 m_nThSDinv Equal to (2^16)/ (m_nThS[1]-m_nThS[0])
0x802068C0	SNR1_COMBINE _GLOBAL_LOG_ RATIO_0_H	0x10	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 global log ratio[0] (unsigned) high byte
0x802068C1	SNR1_COMBINE _GLOBAL_LOG_ RATIO_0_L	0x00	RW	Bit[7:0]: Sensor 1 global log ratio[0] (unsigned) low byte
0x802068C2	SNR1_COMBINE _GLOBAL_LOG_ RATIO_1_H	0x18	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 global log ratio[1] (unsigned) high byte
0x802068C3	SNR1_COMBINE _GLOBAL_LOG_ RATIO_1_L	0x00	RW	Bit[7:0]: Sensor 1 global log ratio[1] (unsigned) low byte
0x802068C4	SNR1_COMBINE _LOG_E_0_H	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 LogE[0] (signed) high byte
0x802068C5	SNR1_COMBINE _LOG_E_0_L	0x00	RW	Bit[7:0]: Sensor 1 LogE[0] (signed) low byte
0x802068C6	SNR1_COMBINE _LOG_E_1_H	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 LogE[1] (signed) high byte
0x802068C7	SNR1_COMBINE _LOG_E_1_L	0x00	RW	Bit[7:0]: Sensor 1 LogE[1] (signed) low byte

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table 4-36 combine registers (sheet 8 of 9)

address	register name	default value	R/W	description
0x802068C8	SNR1_COMBINE_INV_MLMS_APPLY_00_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 m_nInvMLMSApply[0][0] high byte
0x802068C9	SNR1_COMBINE_INV_MLMS_APPLY_00_L	0xDA	RW	Bit[7:0]: Sensor 1 m_nInvMLMSApply[0][0] low byte
0x802068CA	SNR1_COMBINE_INV_MLMS_APPLY_01_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 m_nInvMLMSApply[0][1] high byte
0x802068CB	SNR1_COMBINE_INV_MLMS_APPLY_01_L	0x1F	RW	Bit[7:0]: Sensor 1 m_nInvMLMSApply[0][1] low byte
0x802068CC	SNR1_COMBINE_INV_MLMS_APPLY_02_H	0x00	RW	Bit[7:2]: Reserved Bit[7:0]: Sensor 1 m_nInvMLMSApply[0][2] high byte
0x802068CD	SNR1_COMBINE_INV_MLMS_APPLY_02_L	0x07	RW	Bit[7:0]: Sensor 1 m_nInvMLMSApply[0][2] low byte
0x802068CE	SNR1_COMBINE_INV_MLMS_APPLY_10_H	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 m_nInvMLMSApply[1][0] high byte
0x802068CF	SNR1_COMBINE_INV_MLMS_APPLY_10_L	0xEB	RW	Bit[7:0]: Sensor 1 m_nInvMLMSApply[1][0] low byte
0x802068D0	SNR1_COMBINE_INV_MLMS_APPLY_11_H	0x01	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 m_nInvMLMSApply[1][1] high byte
0x802068D1	SNR1_COMBINE_INV_MLMS_APPLY_11_L	0x07	RW	Bit[7:0]: Sensor 1 m_nInvMLMSApply[1][1] low byte
0x802068D2	SNR1_COMBINE_INV_MLMS_APPLY_12_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 m_nInvMLMSApply[1][2] high byte
0x802068D3	SNR1_COMBINE_INV_MLMS_APPLY_12_L	0x0E	RW	Bit[7:0]: Sensor 1 m_nInvMLMSApply[1][2] low byte
0x802068D4	SNR1_COMBINE_INV_MLMS_APPLY_20_H	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 m_nInvMLMSApply[2][0] high byte

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table 4-36 combine registers (sheet 9 of 9)

address	register name	default value	R/W	description
0x802068D5	SNR1_COMBINE_INV_MLMS_APPLY_20_L	0xF2	RW	Bit[7:0]: Sensor 1 m_nInvMLMSApply[2][0] low byte
0x802068D6	SNR1_COMBINE_INV_MLMS_APPLY_21_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 m_nInvMLMSApply[2][1] high byte
0x802068D7	SNR1_COMBINE_INV_MLMS_APPLY_21_L	0x07	RW	Bit[7:0]: Sensor 1 m_nInvMLMSApply[2][1] low byte
0x802068D8	SNR1_COMBINE_INV_MLMS_APPLY_22_H	0x01	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 m_nInvMLMSApply[2][2] high byte
0x802068D9	SNR1_COMBINE_INV_MLMS_APPLY_22_L	0x07	RW	Bit[7:0]: Sensor 1 m_nInvMLMSApply[2][2] low byte
0x802068E0	SNR1_COMBINE_E_0_H	–	R	Bit[7:0]: Sensor 1 E[0] (E[0], signed) high byte
0x802068E1	SNR1_COMBINE_E_0_L	–	R	Bit[7:0]: Sensor 1 E[0] (E[0], signed) low byte
0x802068E2	SNR1_COMBINE_E_1_H	–	R	Bit[7:0]: Sensor 1 E[1] (E[1], signed) high byte
0x802068E3	SNR1_COMBINE_E_1_L	–	R	Bit[7:0]: Sensor 1 E[1] (E[1], signed) low byte
0x802068E4	SNR1_COMBINE_SATURATE_LEVEL	–	R	Bit[7:0]: Sensor 1 estimate saturate level

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4.27 curve AWB control

table 4-37 curve AWB registers (sheet 1 of 17)

address	register name	default value	R/W	description
0x80206C00	SNR0_CURVE_AWB_CTRL	0x00	RW	Sensor 0 Curve AWB Control Bit[7:5]: Reserved Bit[4:3]: Statistic exposure select 00: Long 01: Short 1x: Very short Bit[2]: Simple enable 1: Simple mode enable Bit[1]: statistic rectangle enable 0: Statistic all 1: Statistic rectangle Bit[0]: InterP mode enable (m_bInterpModeEnable)
0x80206C01	SNR0_AWB_STAT_RECT_LEFT_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 statistic rectangle left coordinate[11:8]
0x80206C02	SNR0_AWB_STAT_RECT_LEFT_L	0x00	RW	Bit[7:0]: Sensor 0 statistic rectangle left coordinate[7:0]
0x80206C03	SNR0_AWB_STAT_RECT_TOP_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 statistic rectangle top coordinate[10:8]
0x80206C04	SNR0_AWB_STAT_RECT_TOP_L	0x00	RW	Bit[7:0]: Sensor 0 statistic rectangle top coordinate[7:0]
0x80206C05	SNR0_AWB_STAT_RECT_RIGHT_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 statistic rectangle right coordinate[11:8]
0x80206C06	SNR0_AWB_STAT_RECT_RIGHT_L	0x00	RW	Bit[7:0]: Sensor 0 statistic rectangle right coordinate[7:0]
0x80206C07	SNR0_AWB_STAT_RECT_BOTTOM_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 statistic rectangle bottom coordinate[10:8]
0x80206C08	SNR0_AWB_STAT_RECT_BOTTOM_L	0x00	RW	Bit[7:0]: Sensor 0 statistic rectangle bottom coordinate[7:0]
0x80206C09	SNR0_AWB_STATISTIC_RATE	0x44	RW	Bit[7:4]: Sensor 0 X statistic sample rate Bit[3:0]: Sensor 0 Y statistic sample rate
0x80206C0A	SNR0_AWB_MAX_VALUE_H	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 statistic maximum value[9:8]

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table 4-37 curve AWB registers (sheet 2 of 17)

address	register name	default value	R/W	description
0x80206C0B	SNR0_AWB_MAX_VALUE_L	0xE0	RW	Bit[7:0]: Sensor 0 statistic maximum value[7:0]
0x80206C0C	SNR0_AWB_MIN_VALUE_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 statistic minimum value[9:8]
0x80206C0D	SNR0_AWB_MIN_VALUE_L	0x0E	RW	Bit[7:0]: Sensor 0 statistic minimum value[7:0]
0x80206C0E	SNR0_AWB_XOFFSET_H	0xFE	RW	Bit[7:0]: Sensor 0 X offset[15:8] (signed)
0x80206C0F	SNR0_AWB_XOFFSET_L	0x3D	RW	Bit[7:0]: Sensor 0 X offset[7:0] (signed)
0x80206C10	SNR0_AWB_YOFFSET_H	0xFE	RW	Bit[7:0]: Sensor 0 Y offset[15:8] (signed)
0x80206C11	SNR0_AWB_YOFFSET_L	0x42	RW	Bit[7:0]: Sensor 0 Y offset[7:0] (signed)
0x80206C12	SNR0_AWB_SCALE_BITS	0x0A	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 scale bits (can be 0x8 or 0xA only)
0x80206C13	SNR0_AWB_WEIGHT_TH	0x00	RW	Bit[7:0]: Sensor 0 weight threshold
0x80206C14	SNR0_AWB_REG0_X_H	0x00	RW	Bit[7:0]: Sensor 0 reg0 x[15:8] (m_nreg0_x, signed)
0x80206C15	SNR0_AWB_REG0_X_L	0x16	RW	Bit[7:0]: Sensor 0 reg0 x[7:0] (m_nreg0_x, signed)
0x80206C16	SNR0_AWB_REG0_Y_H	0x00	RW	Bit[7:0]: Sensor 0 reg0 y[15:8] (m_nreg0_y, signed)
0x80206C17	SNR0_AWB_REG0_Y_L	0x24	RW	Bit[7:0]: Sensor 0 reg0 y[7:0] (m_nreg0_y, signed)
0x80206C18	SNR0_AWB_REG0_W	0x18	RW	Bit[7:0]: Sensor 0 reg0 w (m_nreg0_w)
0x80206C19	SNR0_AWB_REG0_H	0x1C	RW	Bit[7:0]: Sensor 0 reg0 h (m_nreg0_h)
0x80206C1A	SNR0_AWB_REG1_X_H	0x00	RW	Bit[7:0]: Sensor 0 reg1 x[15:8] (m_nreg1_x, signed)
0x80206C1B	SNR0_AWB_REG1_X_L	0x08	RW	Bit[7:0]: Sensor 0 reg1 x[7:0] (m_nreg1_x, signed)
0x80206C1C	SNR0_AWB_REG1_Y_H	0x00	RW	Bit[7:0]: Sensor 0 reg1 y[15:8] (m_nreg1_y, signed)

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table 4-37 curve AWB registers (sheet 3 of 17)

address	register name	default value	R/W	description
0x80206C1D	SNR0_AWB_REG1_Y_L	0x18	RW	Bit[7:0]: Sensor 0 reg1 y[7:0] (m_nreg1_y, signed)
0x80206C1E	SNR0_AWB_REG1_W	0x0C	RW	Bit[7:0]: Sensor 0 reg1 w (m_nreg1_w)
0x80206C1F	SNR0_AWB_REG1_H	0x0E	RW	Bit[7:0]: Sensor 0 reg1 h (m_nreg1_h)
0x80206C20	SNR0_AWB_REG2_X_H	0x00	RW	Bit[7:0]: Sensor 0 reg2 x[15:8] (m_nreg2_x, signed)
0x80206C21	SNR0_AWB_REG2_X_L	0x16	RW	Bit[7:0]: Sensor 0 reg2 x[7:0] (m_nreg2_x, signed)
0x80206C22	SNR0_AWB_REG2_Y_H	0x00	RW	Bit[7:0]: Sensor 0 reg2 y[15:8] (m_nreg2_y, signed)
0x80206C23	SNR0_AWB_REG2_Y_L	0x02	RW	Bit[7:0]: Sensor 0 reg2 y[7:0] (m_nreg2_y, signed)
0x80206C24	SNR0_AWB_REG2_W	0x18	RW	Bit[7:0]: Sensor 0 reg2 w (m_nreg2_w)
0x80206C25	SNR0_AWB_REG2_H	0x14	RW	Bit[7:0]: Sensor 0 reg2 h (m_nreg2_h)
0x80206C26	SNR0_AWB_REG3_X_H	0x00	RW	Bit[7:0]: Sensor 0 reg3 x[15:8] (m_nreg3_x, signed)
0x80206C27	SNR0_AWB_REG3_X_L	0x00	RW	Bit[7:0]: Sensor 0 reg3 x[7:0] (m_nreg3_x, signed)
0x80206C28	SNR0_AWB_REG3_Y_H	0x00	RW	Bit[7:0]: Sensor 0 reg3 y[15:8] (m_nreg3_y, signed)
0x80206C29	SNR0_AWB_REG3_Y_L	0x00	RW	Bit[7:0]: Sensor 0 reg3 y[7:0] (m_nreg3_y, signed)
0x80206C2A	SNR0_AWB_REG3_W	0x40	RW	Bit[7:0]: Sensor 0 reg3 w (m_nreg3_w)
0x80206C2B	SNR0_AWB_REG3_H	0x40	RW	Bit[7:0]: Sensor 0 reg3 h (m_nreg3_h)
0x80206C2C	SNR0_AWB_ROW0_WIN_EN	0x1F	RW	Sensor 0 Sub-windows [0][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 00 enable Bit[3]: Sub-window 01 enable Bit[2]: Sub-window 02 enable Bit[1]: Sub-window 03 enable Bit[0]: Sub-window 04 enable

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table 4-37 curve AWB registers (sheet 4 of 17)

address	register name	default value	R/W	description
0x80206C2D	SNR0_AWB_ROW1_WIN_EN	0x1F	RW	Sensor 0 Sub-windows [1][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 10 enable Bit[3]: Sub-window 11 enable Bit[2]: Sub-window 12 enable Bit[1]: Sub-window 13 enable Bit[0]: Sub-window 14 enable
0x80206C2E	SNR0_AWB_ROW2_WIN_EN	0x1F	RW	Sensor 0 Sub-windows [2][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 20 enable Bit[3]: Sub-window 21 enable Bit[2]: Sub-window 22 enable Bit[1]: Sub-window 23 enable Bit[0]: Sub-window 24 enable
0x80206C2F	SNR0_AWB_ROW3_WIN_EN	0x1F	RW	Sensor 0 Sub-windows [3][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 30 enable Bit[3]: Sub-window 31 enable Bit[2]: Sub-window 32 enable Bit[1]: Sub-window 33 enable Bit[0]: Sub-window 34 enable
0x80206C30	SNR0_AWB_ROW4_WIN_EN	0x1F	RW	Sensor 0 Sub-windows [4][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 40 enable Bit[3]: Sub-window 41 enable Bit[2]: Sub-window 42 enable Bit[1]: Sub-window 43 enable Bit[0]: Sub-window 44 enable
0x80206C31	SNR0_AWB_SUB_WIN_WIDTH_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 sub-window width[9:8]
0x80206C32	SNR0_AWB_SUB_WIN_WIDTH_L	0x96	RW	Bit[7:0]: Sensor 0 sub-window width[7:0]
0x80206C33	SNR0_AWB_SUB_WIN_HEIGHT_H	0x00	RW	Bit[7:1]: Reserved Bit[0]: Sensor 0 sub-window height[8]
0x80206C34	SNR0_AWB_SUB_WIN_HEIGHT_L	0x68	RW	Bit[7:0]: Sensor 0 sub-window height[7:0]
0x80206C3A	AHB_TIME_OUT_CTRL_0	0x84	RW	AHB Bus Time Out Control 0 (both sensors) Bit[7]: Time out control enable Bit[6:0]: Time out number[14:0]
0x80206C3B	AHB_TIME_OUT_CTRL_1	0x00	RW	AHB Bus Time Out Control 1 (both sensors) Bit[7:0]: Time out number[7:0]
0x80206C40	RSVD	–	–	Reserved

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table 4-37 curve AWB registers (sheet 5 of 17)

address	register name	default value	R/W	description
0x80206C41	SNR0_AWB_KX	0x00	RW	Bit[7:0]: Sensor 0 Kx (unsigned short)
0x80206C42	RSVD	–	–	Reserved
0x80206C43	SNR0_AWB_KY	0x00	RW	Bit[7:0]: Sensor 0 Ky (unsigned short)
0x80206C44	SNR0_AWB_ INVERSE_GAIN_0_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 inverse gain[0] (signed)[11:8]
0x80206C45	SNR0_AWB_ INVERSE_GAIN_0_L	0x00	RW	Bit[7:0]: Sensor 0 inverse gain[0] (signed)[7:0]
0x80206C46	SNR0_AWB_ INVERSE_GAIN_1_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 inverse gain[1] (signed)[11:8]
0x80206C47	SNR0_AWB_ INVERSE_GAIN_1_L	0x00	RW	Bit[7:0]: Sensor 0 inverse gain[1] (signed)[7:0]
0x80206C50	SNR0_AWB_SUM_B_ BYTE3	–	R	Bit[7:0]: Sensor 0 sum BGR[0], B channel[31:24]
0x80206C51	SNR0_AWB_SUM_B_ BYTE2	–	R	Bit[7:0]: Sensor 0 sum BGR[0], B channel[23:16]
0x80206C52	SNR0_AWB_SUM_B_ BYTE1	–	R	Bit[7:0]: Sensor 0 sum BGR[0], B channel[15:8]
0x80206C53	SNR0_AWB_SUM_B_ BYTE0	–	R	Bit[7:0]: Sensor 0 sum BGR[0], B channel[7:0]
0x80206C54	SNR0_AWB_SUM_G_ BYTE3	–	R	Bit[7:0]: Sensor 0 sum BGR[1], G channel[31:24]
0x80206C55	SNR0_AWB_SUM_G_ BYTE2	–	R	Bit[7:0]: Sensor 0 sum BGR[1], G channel[23:16]
0x80206C56	SNR0_AWB_SUM_G_ BYTE1	–	R	Bit[7:0]: Sensor 0 sum BGR[1], G channel[15:8]
0x80206C57	SNR0_AWB_SUM_G_ BYTE0	–	R	Bit[7:0]: Sensor 0 sum BGR[1], G channel[7:0]
0x80206C58	SNR0_AWB_SUM_R_ BYTE3	–	R	Bit[7:0]: Sensor 0 sum BGR[0], R channel[31:24]
0x80206C59	SNR0_AWB_SUM_R_ BYTE2	–	R	Bit[7:0]: Sensor 0 sum BGR[0], R channel[23:16]
0x80206C5A	SNR0_AWB_SUM_R_ BYTE1	–	R	Bit[7:0]: Sensor 0 sum BGR[0], R channel[15:8]
0x80206C5B	SNR0_AWB_SUM_R_ BYTE0	–	R	Bit[7:0]: Sensor 0 sum BGR[0], R channel[7:0]

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table 4-37 curve AWB registers (sheet 6 of 17)

address	register name	default value	R/W	description
0x80206C5C	SNR0_AWB_CNT_BYTE3	–	R	Bit[7:0]: Sensor 0 sum count[31:24]
0x80206C5D	SNR0_AWB_CNT_BYTE2	–	R	Bit[7:0]: Sensor 0 sum count[23:16]
0x80206C5E	SNR0_AWB_CNT_BYTE1	–	R	Bit[7:0]: Sensor 0 sum count[15:8]
0x80206C5F	SNR0_AWB_CNT_BYTE0	–	R	Bit[7:0]: Sensor 0 sum count[7:0]
0x80206C60	SNR0_AWB_SUM_REG0_B_BYTE3	–	R	Bit[7:0]: Sensor 0 sum BGR[0] reg0, B channel[31:24]
0x80206C61	SNR0_AWB_SUM_REG0_B_BYTE2	–	R	Bit[7:0]: Sensor 0 sum BGR[0] reg0, B channel[23:16]
0x80206C62	SNR0_AWB_SUM_REG0_B_BYTE1	–	R	Bit[7:0]: Sensor 0 sum BGR[0] reg0, B channel[15:8]
0x80206C63	SNR0_AWB_SUM_REG0_B_BYTE0	–	R	Bit[7:0]: Sensor 0 sum BGR[0] reg0, B channel[7:0]
0x80206C64	SNR0_AWB_SUM_REG0_G_BYTE3	–	R	Bit[7:0]: Sensor 0 sum BGR[1] reg0, G channel[31:24]
0x80206C65	SNR0_AWB_SUM_REG0_G_BYTE2	–	R	Bit[7:0]: Sensor 0 sum BGR[1] reg0, G channel[23:16]
0x80206C66	SNR0_AWB_SUM_REG0_G_BYTE1	–	R	Bit[7:0]: Sensor 0 sum BGR[1] reg0, G channel[15:8]
0x80206C67	SNR0_AWB_SUM_REG0_G_BYTE0	–	R	Bit[7:0]: Sensor 0 sum BGR[1] reg0, G channel[7:0]
0x80206C68	SNR0_AWB_SUM_REG0_R_BYTE3	–	R	Bit[7:0]: Sensor 0 sum BGR[2] reg0, R channel[31:24]
0x80206C69	SNR0_AWB_SUM_REG0_R_BYTE2	–	R	Bit[7:0]: Sensor 0 sum BGR[2] reg0, R channel[23:16]
0x80206C6A	SNR0_AWB_SUM_REG0_R_BYTE1	–	R	Bit[7:0]: Sensor 0 sum BGR[2] reg0, R channel[15:8]
0x80206C6B	SNR0_AWB_SUM_REG0_R_BYTE0	–	R	Bit[7:0]: Sensor 0 sum BGR[2] reg0, R channel[7:0]
0x80206C6C	SNR0_AWB_CNT_REG0_BYTE3	–	R	Bit[7:0]: Sensor 0 sum count reg0[31:24]
0x80206C6D	SNR0_AWB_CNT_REG0_BYTE2	–	R	Bit[7:0]: Sensor 0 sum count reg0[23:16]
0x80206C6E	SNR0_AWB_CNT_REG0_BYTE1	–	R	Bit[7:0]: Sensor 0 sum count reg0[15:8]

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table 4-37 curve AWB registers (sheet 7 of 17)

address	register name	default value	R/W	description
0x80206C6F	SNR0_AWB_CNT_REG0_BYTE0	–	R	Bit[7:0]: Sensor 0 sum count reg0[7:0]
0x80206C70	SNR0_AWB_SUM_REG1_B_BYTE3	–	R	Bit[7:0]: Sensor 0 sum BGR[0] reg1, B channel[31:24]
0x80206C71	SNR0_AWB_SUM_REG1_B_BYTE2	–	R	Bit[7:0]: Sensor 0 sum BGR[0] reg1, B channel[23:16]
0x80206C72	SNR0_AWB_SUM_REG1_B_BYTE1	–	R	Bit[7:0]: Sensor 0 sum BGR[0] reg1, B channel[15:8]
0x80206C73	SNR0_AWB_SUM_REG1_B_BYTE0	–	R	Bit[7:0]: Sensor 0 sum BGR[0] reg1, B channel[7:0]
0x80206C74	SNR0_AWB_SUM_REG1_G_BYTE3	–	R	Bit[7:0]: Sensor 0 sum BGR[1] reg1, G channel[31:24]
0x80206C75	SNR0_AWB_SUM_REG1_G_BYTE2	–	R	Bit[7:0]: Sensor 0 sum BGR[1] reg1, G channel[23:16]
0x80206C76	SNR0_AWB_SUM_REG1_G_BYTE1	–	R	Bit[7:0]: Sensor 0 sum BGR[1] reg1, G channel[15:8]
0x80206C77	SNR0_AWB_SUM_REG1_G_BYTE0	–	R	Bit[7:0]: Sensor 0 sum BGR[1] reg1, G channel[7:0]
0x80206C78	SNR0_AWB_SUM_REG1_R_BYTE3	–	R	Bit[7:0]: Sensor 0 sum BGR[2] reg1, R channel[31:24]
0x80206C79	SNR0_AWB_SUM_REG1_R_BYTE2	–	R	Bit[7:0]: Sensor 0 sum BGR[2] reg1, R channel[23:16]
0x80206C7A	SNR0_AWB_SUM_REG1_R_BYTE1	–	R	Bit[7:0]: Sensor 0 sum BGR[2] reg1, R channel[15:8]
0x80206C7B	SNR0_AWB_SUM_REG1_R_BYTE0	–	R	Bit[7:0]: Sensor 0 sum BGR[2] reg1, R channel[7:0]
0x80206C7C	SNR0_AWB_CNT_REG1_BYTE3	–	R	Bit[7:0]: Sensor 0 sum count reg1[31:24]
0x80206C7D	SNR0_AWB_CNT_REG1_BYTE2	–	R	Bit[7:0]: Sensor 0 sum count reg1[23:16]
0x80206C7E	SNR0_AWB_CNT_REG1_BYTE1	–	R	Bit[7:0]: Sensor 0 sum count reg1[15:8]
0x80206C7F	SNR0_AWB_CNT_REG1_BYTE0	–	R	Bit[7:0]: Sensor 0 sum count reg1[7:0]
0x80206C80	SNR0_AWB_SUM_REG2_B_BYTE3	–	R	Bit[7:0]: Sensor 0 sum BGR[0] reg2, B channel[31:24]
0x80206C81	SNR0_AWB_SUM_REG2_B_BYTE2	–	R	Bit[7:0]: Sensor 0 sum BGR[0] reg2, B channel[23:16]

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table 4-37 curve AWB registers (sheet 8 of 17)

address	register name	default value	R/W	description
0x80206C82	SNR0_AWB_SUM_REG2_B_BYTE1	–	R	Bit[7:0]: Sensor 0 sum BGR[0] reg2, B channel[15:8]
0x80206C83	SNR0_AWB_SUM_REG2_B_BYTE0	–	R	Bit[7:0]: Sensor 0 sum BGR[0] reg2, B channel[7:0]
0x80206C84	SNR0_AWB_SUM_REG2_G_BYTE3	–	R	Bit[7:0]: Sensor 0 sum BGR[1] reg2, G channel[31:24]
0x80206C85	SNR0_AWB_SUM_REG2_G_BYTE2	–	R	Bit[7:0]: Sensor 0 sum BGR[1] reg2, G channel[23:16]
0x80206C86	SNR0_AWB_SUM_REG2_G_BYTE1	–	R	Bit[7:0]: Sensor 0 sum BGR[1] reg2, G channel[15:8]
0x80206C87	SNR0_AWB_SUM_REG2_G_BYTE0	–	R	Bit[7:0]: Sensor 0 sum BGR[1] reg2, G channel[7:0]
0x80206C88	SNR0_AWB_SUM_REG2_R_BYTE3	–	R	Bit[7:0]: Sensor 0 sum BGR[2] reg2, R channel[31:24]
0x80206C89	SNR0_AWB_SUM_REG2_R_BYTE2	–	R	Bit[7:0]: Sensor 0 sum BGR[2] reg2, R channel[23:16]
0x80206C8A	SNR0_AWB_SUM_REG2_R_BYTE1	–	R	Bit[7:0]: Sensor 0 sum BGR[2] reg2, R channel[15:8]
0x80206C8B	SNR0_AWB_SUM_REG2_R_BYTE0	–	R	Bit[7:0]: Sensor 0 sum BGR[2] reg2, R channel[7:0]
0x80206C8C	SNR0_AWB_CNT_REG2_BYTE3	–	R	Bit[7:0]: Sensor 0 sum count reg2[31:24]
0x80206C8D	SNR0_AWB_CNT_REG2_BYTE2	–	R	Bit[7:0]: Sensor 0 sum count reg2[23:16]
0x80206C8E	SNR0_AWB_CNT_REG2_BYTE1	–	R	Bit[7:0]: Sensor 0 sum count reg2[15:8]
0x80206C8F	SNR0_AWB_CNT_REG2_BYTE0	–	R	Bit[7:0]: Sensor 0 sum count reg2[7:0]
0x80206C90	SNR0_AWB_SUM_REG3_B_BYTE3	–	R	Bit[7:0]: Sensor 0 sum BGR[0] reg3, B channel[31:24]
0x80206C91	SNR0_AWB_SUM_REG3_B_BYTE2	–	R	Bit[7:0]: Sensor 0 sum BGR[0] reg3, B channel[23:16]
0x80206C92	SNR0_AWB_SUM_REG3_B_BYTE1	–	R	Bit[7:0]: Sensor 0 sum BGR[0] reg3, B channel[15:8]
0x80206C93	SNR0_AWB_SUM_REG3_B_BYTE0	–	R	Bit[7:0]: Sensor 0 sum BGR[0] reg3, B channel[7:0]
0x80206C94	SNR0_AWB_SUM_REG3_G_BYTE3	–	R	Bit[7:0]: Sensor 0 sum BGR[1] reg3, G channel[31:24]

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table 4-37 curve AWB registers (sheet 9 of 17)

address	register name	default value	R/W	description
0x80206C95	SNR0_AWB_SUM_REG3_G_BYTE2	–	R	Bit[7:0]: Sensor 0 sum BGR[1] reg3, G channel[23:16]
0x80206C96	SNR0_AWB_SUM_REG3_G_BYTE1	–	R	Bit[7:0]: Sensor 0 sum BGR[1] reg3, G channel[15:8]
0x80206C97	SNR0_AWB_SUM_REG3_G_BYTE0	–	R	Bit[7:0]: Sensor 0 sum BGR[1] reg3, G channel[7:0]
0x80206C98	SNR0_AWB_SUM_REG3_R_BYTE3	–	R	Bit[7:0]: Sensor 0 sum BGR[2] reg3, R channel[31:24]
0x80206C99	SNR0_AWB_SUM_REG3_R_BYTE2	–	R	Bit[7:0]: Sensor 0 sum BGR[2] reg3, R channel[23:16]
0x80206C9A	SNR0_AWB_SUM_REG3_R_BYTE1	–	R	Bit[7:0]: Sensor 0 sum BGR[2] reg3, R channel[15:8]
0x80206C9B	SNR0_AWB_SUM_REG3_R_BYTE0	–	R	Bit[7:0]: Sensor 0 sum BGR[2] reg3, R channel[7:0]
0x80206C9C	SNR0_AWB_CNT_REG3_BYTE3	–	R	Bit[7:0]: Sensor 0 sum count reg3[31:24]
0x80206C9D	SNR0_AWB_CNT_REG3_BYTE2	–	R	Bit[7:0]: Sensor 0 sum count reg3[23:16]
0x80206C9E	SNR0_AWB_CNT_REG3_BYTE1	–	R	Bit[7:0]: Sensor 0 sum count reg3[15:8]
0x80206C9F	SNR0_AWB_CNT_REG3_BYTE0	–	R	Bit[7:0]: Sensor 0 sum count reg3[7:0]
0x80206CA0	SNR1_CURVE_AWB_CTRL	0x00	RW	Sensor 1 Curve AWB Control Bit[7:5]: Reserved Bit[4:3]: Statistic exposure select 00: Long 01: Short 1x: Very short Bit[2]: Simple enable 1: Simple mode enable Bit[1]: Statistic rectangle enable 0: Statistic all 1: Statistic rectangle Bit[0]: InterP mode enable (m_bInterpModeEnable)
0x80206CA1	SNR1_AWB_STAT_RECT_LEFT_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 statistic rectangle left coordinate[11:8]
0x80206CA2	SNR1_AWB_STAT_RECT_LEFT_L	0x00	RW	Bit[7:0]: Sensor 1 statistic rectangle left coordinate[7:0]

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table 4-37 curve AWB registers (sheet 10 of 17)

address	register name	default value	R/W	description
0x80206CA3	SNR1_AWB_STAT_ RECT_TOP_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 statistic rectangle top coordinate[10:8]
0x80206CA4	SNR1_AWB_STAT_ RECT_TOP_L	0x00	RW	Bit[7:0]: Sensor 1 statistic rectangle top coordinate[7:0]
0x80206CA5	SNR1_AWB_STAT_ RECT_RIGHT_H	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 statistic rectangle right coordinate[11:8]
0x80206CA6	SNR1_AWB_STAT_ RECT_RIGHT_L	0x00	RW	Bit[7:0]: Sensor 1 statistic rectangle right coordinate[7:0]
0x80206CA7	SNR1_AWB_STAT_ RECT_BOTTOM_H	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 statistic rectangle bottom coordinate[10:8]
0x80206CA8	SNR1_AWB_STAT_ RECT_BOTTOM_L	0x00	RW	Bit[7:0]: Sensor 1 statistic rectangle bottom coordinate [7:0]
0x80206CA9	SNR1_AWB_ STATISTIC_RATE	0x44	RW	Bit[7:4]: Sensor 1 X statistic sample rate Bit[3:0]: Sensor 1 Y statistic sample rate
0x80206CAA	SNR1_AWB_MAX_ VALUE_H	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 statistic maximum value[9:8]
0x80206CAB	SNR1_AWB_MAX_ VALUE_L	0xE0	RW	Bit[7:0]: Sensor 1 statistic maximum value[7:0]
0x80206CAC	SNR1_AWB_MIN_ VALUE_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 statistic minimum value[9:8]
0x80206CAD	SNR1_AWB_MIN_ VALUE_L	0x0E	RW	Bit[7:0]: Sensor 1 statistic minimum value[7:0]
0x80206CAE	SNR1_AWB_ XOFFSET_H	0xFE	RW	Bit[7:0]: Sensor 1 X offset[15:8] (signed)
0x80206CAF	SNR1_AWB_ XOFFSET_L	0x3D	RW	Bit[7:0]: Sensor 1 X offset[7:0] (signed)
0x80206CB0	SNR1_AWB_ YOFFSET_H	0xFE	RW	Bit[7:0]: Sensor 1 Y offset[15:8] (signed)
0x80206CB1	SNR1_AWB_ YOFFSET_L	0x42	RW	Bit[7:0]: Sensor 1 Y offset[7:0] (signed)
0x80206CB2	SNR1_AWB_ SCALE_BITS	0x0A	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 scale bits (can be 0x8 or 0xA only)

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table 4-37 curve AWB registers (sheet 11 of 17)

address	register name	default value	R/W	description
0x80206CB3	SNR1_AWB_WEIGHT_TH	0x00	RW	Bit[7:0]: Sensor 1 weight threshold
0x80206CB4	SNR1_AWB_REG0_X_H	0x00	RW	Bit[7:0]: Sensor 1 reg0 x[15:8] (m_nreg0_x, signed)
0x80206CB5	SNR1_AWB_REG0_X_L	0x16	RW	Bit[7:0]: Sensor 1 reg0 x[7:0] (m_nreg0_x, signed)
0x80206CB6	SNR1_AWB_REG0_Y_H	0x00	RW	Bit[7:0]: Sensor 1 reg0 y[15:8] (m_nreg0_y, signed)
0x80206CB7	SNR1_AWB_REG0_Y_L	0x24	RW	Bit[7:0]: Sensor 1 reg0 y[7:0] (m_nreg0_y, signed)
0x80206CB8	SNR1_AWB_REG0_W	0x18	RW	Bit[7:0]: Sensor 1 reg0 w (m_nreg0_w)
0x80206CB9	SNR1_AWB_REG0_H	0x1C	RW	Bit[7:0]: Sensor 1 reg0 h (m_nreg0_h)
0x80206CBA	SNR1_AWB_REG1_X_H	0x00	RW	Bit[7:0]: Sensor 1 reg1 x[15:8] (m_nreg1_x, signed)
0x80206CBB	SNR1_AWB_REG1_X_L	0x08	RW	Bit[7:0]: Sensor 1 reg1 x[7:0] (m_nreg1_x, signed)
0x80206CBC	SNR1_AWB_REG1_Y_H	0x00	RW	Bit[7:0]: Sensor 1 reg1 y[15:8] (m_nreg1_y, signed)
0x80206CBD	SNR1_AWB_REG1_Y_L	0x18	RW	Bit[7:0]: Sensor 1 reg1 y[7:0] (m_nreg1_y, signed)
0x80206CBE	SNR1_AWB_REG1_W	0x0C	RW	Bit[7:0]: Sensor 1 reg1 w (m_nreg1_w)
0x80206CBF	SNR1_AWB_REG1_H	0x0E	RW	Bit[7:0]: Sensor 1 reg1 h (m_nreg1_h)
0x80206CC0	SNR1_AWB_REG2_X_H	0x00	RW	Bit[7:0]: Sensor 1 reg2 x[15:8] (m_nreg2_x, signed)
0x80206CC1	SNR1_AWB_REG2_X_L	0x16	RW	Bit[7:0]: Sensor 1 reg2 x[7:0] (m_nreg2_x, signed)
0x80206CC2	SNR1_AWB_REG2_Y_H	0x00	RW	Bit[7:0]: Sensor 1 reg2 y[15:8] (m_nreg2_y, signed)
0x80206CC3	SNR1_AWB_REG2_Y_L	0x02	RW	Bit[7:0]: Sensor 1 reg2 y[7:0] (m_nreg2_y, signed)
0x80206CC4	SNR1_AWB_REG2_W	0x18	RW	Bit[7:0]: Sensor 1 reg2 w (m_nreg2_w)
0x80206CC5	SNR1_AWB_REG2_H	0x14	RW	Bit[7:0]: Sensor 1 reg2 h (m_nreg2_h)

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table 4-37 curve AWB registers (sheet 12 of 17)

address	register name	default value	R/W	description
0x80206CC6	SNR1_AWB_REG3_X_H	0x00	RW	Bit[7:0]: Sensor 1 reg3 x[15:8] (m_nreg3_x, signed)
0x80206CC7	SNR1_AWB_REG3_X_L	0x00	RW	Bit[7:0]: Sensor 1 reg3 x[7:0] (m_nreg3_x, signed)
0x80206CC8	SNR1_AWB_REG3_Y_H	0x00	RW	Bit[7:0]: Sensor 1 reg3 y[15:8] (m_nreg3_y, signed)
0x80206CC9	SNR1_AWB_REG3_Y_L	0x00	RW	Bit[7:0]: Sensor 1 reg3 y[7:0] (m_nreg3_y, signed)
0x80206CCA	SNR1_AWB_REG3_W	0x40	RW	Bit[7:0]: Sensor 1 reg3 w (m_nreg3_w)
0x80206CCB	SNR1_AWB_REG3_H	0x00	RW	Bit[7:0]: Sensor 1 reg3 h (m_nreg3_h)
0x80206CCC	SNR1_AWB_ROW0_WIN_EN	0x1F	RW	Sensor 1 Sub-windows [0][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 00 enable Bit[3]: Sub-window 01 enable Bit[2]: Sub-window 02 enable Bit[1]: Sub-window 03 enable Bit[0]: Sub-window 04 enable
0x80206CCD	SNR1_AWB_ROW1_WIN_EN	0x1F	RW	Sensor 1 Sub-windows [1][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 10 enable Bit[3]: Sub-window 11 enable Bit[2]: Sub-window 12 enable Bit[1]: Sub-window 13 enable Bit[0]: Sub-window 14 enable
0x80206CCE	SNR1_AWB_ROW2_WIN_EN	0x1F	RW	Sensor 1 Sub-windows [2][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 20 enable Bit[3]: Sub-window 21 enable Bit[2]: Sub-window 22 enable Bit[1]: Sub-window 23 enable Bit[0]: Sub-window 24 enable
0x80206CCF	SNR1_AWB_ROW3_WIN_EN	0x1F	RW	Sensor 1 Sub-windows [3][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 30 enable Bit[3]: Sub-window 31 enable Bit[2]: Sub-window 32 enable Bit[1]: Sub-window 33 enable Bit[0]: Sub-window 34 enable

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table 4-37 curve AWB registers (sheet 13 of 17)

address	register name	default value	R/W	description
0x80206CD0	SNR1_AWB_ROW4_WIN_EN	0x1F	RW	Sensor 1 Sub-windows [4][x] Enable Bit[7:5]: Reserved Bit[4]: Sub-window 40 enable Bit[3]: Sub-window 41 enable Bit[2]: Sub-window 42 enable Bit[1]: Sub-window 43 enable Bit[0]: Sub-window 44 enable
0x80206CD1	SNR1_AWB_SUB_WIN_WIDTH_H	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 sub-window width[9:8]
0x80206CD2	SNR1_AWB_SUB_WIN_WIDTH_L	0x96	RW	Bit[7:0]: Sensor 1 sub-window width[7:0]
0x80206CD3	SNR1_AWB_SUB_WIN_HEIGHT_H	0x00	RW	Bit[7:1]: Reserved Bit[0]: Sensor 1 sub-window height[8]
0x80206CD4	SNR1_AWB_SUB_WIN_HEIGHT_L	0x68	RW	Bit[7:0]: Sensor 1 sub-window height[7:0]
0x80206CE0	RSVD	–	–	Reserved
0x80206CE1	SNR1_AWB_KX	0x00	RW	Bit[7:0]: Sensor 1 Kx (unsigned short)
0x80206CE2	RSVD	–	–	Reserved
0x80206CE3	SNR1_AWB_KY	0x00	RW	Bit[7:0]: Sensor 1 Ky (unsigned short)
0x80206CE4	SNR1_AWB_INVERSE_GAIN_0_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 inverse gain[0] (signed)[11:8]
0x80206CE5	SNR1_AWB_INVERSE_GAIN_0_L	0x00	RW	Bit[7:0]: Sensor 1 inverse gain[0] (signed)[7:0]
0x80206CE6	SNR1_AWB_INVERSE_GAIN_1_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 inverse gain[1] (signed)[11:8]
0x80206CE7	SNR1_AWB_INVERSE_GAIN_1_L	0x00	RW	Bit[7:0]: Sensor 1 inverse gain[1] (signed)[7:0]
0x80206CF0	SNR1_AWB_SUM_B_BYTE3	–	R	Bit[7:0]: Sensor 1 sum BGR[0], B channel[31:24]
0x80206CF1	SNR1_AWB_SUM_B_BYTE2	–	R	Bit[7:0]: Sensor 1 sum BGR[0], B channel[23:16]
0x80206CF2	SNR1_AWB_SUM_B_BYTE1	–	R	Bit[7:0]: Sensor 1 sum BGR[0], B channel[15:8]
0x80206CF3	SNR1_AWB_SUM_B_BYTE0	–	R	Bit[7:0]: Sensor 1 sum BGR[0], B channel[7:0]

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table 4-37 curve AWB registers (sheet 14 of 17)

address	register name	default value	R/W	description
0x80206CF4	SNR1_AWB_SUM_G_BYTE3	–	R	Bit[7:0]: Sensor 1 sum BGR[1] G channel[31:24]
0x80206CF5	SNR1_AWB_SUM_G_BYTE2	–	R	Bit[7:0]: Sensor 1 sum BGR[1] G channel[23:16]
0x80206CF6	SNR1_AWB_SUM_G_BYTE1	–	R	Bit[7:0]: Sensor 1 sum BGR[1] G channel[15:8]
0x80206CF7	SNR1_AWB_SUM_G_BYTE0	–	R	Bit[7:0]: Sensor 1 sum BGR[1] G channel[7:0]
0x80206CF8	SNR1_AWB_SUM_R_BYTE3	–	R	Bit[7:0]: Sensor 1 sum BGR[0] R channel[31:24]
0x80206CF9	SNR1_AWB_SUM_R_BYTE2	–	R	Bit[7:0]: Sensor 1 sum BGR[0] R channel[23:16]
0x80206CFA	SNR1_AWB_SUM_R_BYTE1	–	R	Bit[7:0]: Sensor 1 sum BGR[0] R channel[15:8]
0x80206CFB	SNR1_AWB_SUM_R_BYTE0	–	R	Bit[7:0]: Sensor 1 sum BGR[0] R channel[7:0]
0x80206CFC	SNR1_AWB_CNT_BYTE3	–	R	Bit[7:0]: Sensor 1 sum count[31:24]
0x80206CFD	SNR1_AWB_CNT_BYTE2	–	R	Bit[7:0]: Sensor 1 sum count[23:16]
0x80206CFE	SNR1_AWB_CNT_BYTE1	–	R	Bit[7:0]: Sensor 1 sum count[15:8]
0x80206CFF	SNR1_AWB_CNT_BYTE0	–	R	Bit[7:0]: Sensor 1 sum count[7:0]
0x80206D00	SNR1_AWB_SUM_REG0_B_BYTE3	–	R	Bit[7:0]: Sensor 1 sum BGR[0] reg0 B channel[31:24]
0x80206D01	SNR1_AWB_SUM_REG0_B_BYTE2	–	R	Bit[7:0]: Sensor 1 sum BGR[0] reg0 B channel[23:16]
0x80206D02	SNR1_AWB_SUM_REG0_B_BYTE1	–	R	Bit[7:0]: Sensor 1 sum BGR[0] reg0 B channel[15:8]
0x80206D03	SNR1_AWB_SUM_REG0_B_BYTE0	–	R	Bit[7:0]: Sensor 1 sum BGR[0] reg0 B channel[7:0]
0x80206D04	SNR1_AWB_SUM_REG0_G_BYTE3	–	R	Bit[7:0]: Sensor 1 sum BGR[1] reg0 G channel[31:24]
0x80206D05	SNR1_AWB_SUM_REG0_G_BYTE2	–	R	Bit[7:0]: Sensor 1 sum BGR[1] reg0 G channel[23:16]
0x80206D06	SNR1_AWB_SUM_REG0_G_BYTE1	–	R	Bit[7:0]: Sensor 1 sum BGR[1] reg0 G channel[15:8]

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table 4-37 curve AWB registers (sheet 15 of 17)

address	register name	default value	R/W	description
0x80206D07	SNR1_AWB_SUM_REG0_G_BYTE0	–	R	Bit[7:0]: Sensor 1 sum BGR[1] reg0 G channel[7:0]
0x80206D08	SNR1_AWB_SUM_REG0_R_BYTE3	–	R	Bit[7:0]: Sensor 1 sum BGR[2] reg0 R channel[31:24]
0x80206D09	SNR1_AWB_SUM_REG0_R_BYTE2	–	R	Bit[7:0]: Sensor 1 sum BGR[2] reg0 R channel[23:16]
0x80206D0A	SNR1_AWB_SUM_REG0_R_BYTE1	–	R	Bit[7:0]: Sensor 1 sum BGR[2] reg0 R channel[15:8]
0x80206D0B	SNR1_AWB_SUM_REG0_R_BYTE0	–	R	Bit[7:0]: Sensor 1 sum BGR[2] reg0 R channel[7:0]
0x80206D0C	SNR1_AWB_CNT_REG0_BYTE3	–	R	Bit[7:0]: Sensor 1 sum count reg0[31:24]
0x80206D0D	SNR1_AWB_CNT_REG0_BYTE2	–	R	Bit[7:0]: Sensor 1 sum count reg0[23:16]
0x80206D0E	SNR1_AWB_CNT_REG0_BYTE1	–	R	Bit[7:0]: Sensor 1 sum count reg0[15:8]
0x80206D0F	SNR1_AWB_CNT_REG0_BYTE0	–	R	Bit[7:0]: Sensor 1 sum count reg0[7:0]
0x80206D10	SNR1_AWB_SUM_REG1_B_BYTE3	–	R	Bit[7:0]: Sensor 1 sum BGR[0] reg1 B channel[31:24]
0x80206D11	SNR1_AWB_SUM_REG1_B_BYTE2	–	R	Bit[7:0]: Sensor 1 sum BGR[0] reg1 B channel[23:16]
0x80206D12	SNR1_AWB_SUM_REG1_B_BYTE1	–	R	Bit[7:0]: Sensor 1 sum BGR[0] reg1 B channel[15:8]
0x80206D13	SNR1_AWB_SUM_REG1_B_BYTE0	–	R	Bit[7:0]: Sensor 1 sum BGR[0] reg1 B channel[7:0]
0x80206D14	SNR1_AWB_SUM_REG1_G_BYTE3	–	R	Bit[7:0]: Sensor 1 sum BGR[1] reg1 G channel[31:24]
0x80206D15	SNR1_AWB_SUM_REG1_G_BYTE2	–	R	Bit[7:0]: Sensor 1 sum BGR[1] reg1 G channel[23:16]
0x80206D16	SNR1_AWB_SUM_REG1_G_BYTE1	–	R	Bit[7:0]: Sensor 1 sum BGR[1] reg1 G channel[15:8]
0x80206D17	SNR1_AWB_SUM_REG1_G_BYTE0	–	R	Bit[7:0]: Sensor 1 sum BGR[1] reg1 G channel[7:0]
0x80206D18	SNR1_AWB_SUM_REG1_R_BYTE3	–	R	Bit[7:0]: Sensor 1 sum BGR[2] reg1 R channel[31:24]
0x80206D19	SNR1_AWB_SUM_REG1_R_BYTE2	–	R	Bit[7:0]: Sensor 1 sum BGR[2] reg1 R channel[23:16]

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table 4-37 curve AWB registers (sheet 16 of 17)

address	register name	default value	R/W	description
0x80206D1A	SNR1_AWB_SUM_REG1_R_BYTE1	–	R	Bit[7:0]: Sensor 1 sum BGR[2] reg1 R channel[15:8]
0x80206D1B	SNR1_AWB_SUM_REG1_R_BYTE0	–	R	Bit[7:0]: Sensor 1 sum BGR[2] reg1 R channel[7:0]
0x80206D1C	SNR1_AWB_CNT_REG1_BYTE3	–	R	Bit[7:0]: Sensor 1 sum count reg1[31:24]
0x80206D1D	SNR1_AWB_CNT_REG1_BYTE2	–	R	Bit[7:0]: Sensor 1 sum count reg1[23:16]
0x80206D1E	SNR1_AWB_CNT_REG1_BYTE1	–	R	Bit[7:0]: Sensor 1 sum count reg1[15:8]
0x80206D1F	SNR1_AWB_CNT_REG1_BYTE0	–	R	Bit[7:0]: Sensor 1 sum count reg1[7:0]
0x80206D20	SNR1_AWB_SUM_REG2_B_BYTE3	–	R	Bit[7:0]: Sensor 1 sum BGR[0] reg2 B channel[31:24]
0x80206D21	SNR1_AWB_SUM_REG2_B_BYTE2	–	R	Bit[7:0]: Sensor 1 sum BGR[0] reg2 B channel[23:16]
0x80206D22	SNR1_AWB_SUM_REG2_B_BYTE1	–	R	Bit[7:0]: Sensor 1 sum BGR[0] reg2 B channel[15:8]
0x80206D23	SNR1_AWB_SUM_REG2_B_BYTE0	–	R	Bit[7:0]: Sensor 1 sum BGR[0] reg2 B channel[7:0]
0x80206D24	SNR1_AWB_SUM_REG2_G_BYTE3	–	R	Bit[7:0]: Sensor 1 sum BGR[1] reg2 G channel[31:24]
0x80206D25	SNR1_AWB_SUM_REG2_G_BYTE2	–	R	Bit[7:0]: Sensor 1 sum BGR[1] reg2 G channel[23:16]
0x80206D26	SNR1_AWB_SUM_REG2_G_BYTE1	–	R	Bit[7:0]: Sensor 1 sum BGR[1] reg2 G channel[15:8]
0x80206D27	SNR1_AWB_SUM_REG2_G_BYTE0	–	R	Bit[7:0]: Sensor 1 sum BGR[1] reg2 G channel[7:0]
0x80206D28	SNR1_AWB_SUM_REG2_R_BYTE3	–	R	Bit[7:0]: Sensor 1 sum BGR[2] reg2 R channel[31:24]
0x80206D29	SNR1_AWB_SUM_REG2_R_BYTE2	–	R	Bit[7:0]: Sensor 1 sum BGR[2] reg2 R channel[23:16]
0x80206D2A	SNR1_AWB_SUM_REG2_R_BYTE1	–	R	Bit[7:0]: Sensor 1 sum BGR[2] reg2 R channel[15:8]
0x80206D2B	SNR1_AWB_SUM_REG2_R_BYTE0	–	R	Bit[7:0]: Sensor 1 sum BGR[2] reg2 R channel[7:0]
0x80206D2C	SNR1_AWB_CNT_REG2_BYTE3	–	R	Bit[7:0]: Sensor 1 sum count reg2[31:24]

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table 4-37 curve AWB registers (sheet 17 of 17)

address	register name	default value	R/W	description
0x80206D2D	SNR1_AWB_CNT_REG2_BYTE2	–	R	Bit[7:0]: Sensor 1 sum count reg2[23:16]
0x80206D2E	SNR1_AWB_CNT_REG2_BYTE1	–	R	Bit[7:0]: Sensor 1 sum count reg2[15:8]
0x80206D2F	SNR1_AWB_CNT_REG2_BYTE0	–	R	Bit[7:0]: Sensor 1 sum count reg2[7:0]
0x80206D30	SNR1_AWB_SUM_REG3_B_BYTE3	–	R	Bit[7:0]: Sensor 1 sum BGR[0] reg3 B channel[31:24]
0x80206D31	SNR1_AWB_SUM_REG3_B_BYTE2	–	R	Bit[7:0]: Sensor 1 sum BGR[0] reg3 B channel[23:16]
0x80206D32	SNR1_AWB_SUM_REG3_B_BYTE1	–	R	Bit[7:0]: Sensor 1 sum BGR[0] reg3 B channel[15:8]
0x80206D33	SNR1_AWB_SUM_REG3_B_BYTE0	–	R	Bit[7:0]: Sensor 1 sum BGR[0] reg3 B channel[7:0]
0x80206D34	SNR1_AWB_SUM_REG3_G_BYTE3	–	R	Bit[7:0]: Sensor 1 sum BGR[1] reg3 G channel[31:24]
0x80206D35	SNR1_AWB_SUM_REG3_G_BYTE2	–	R	Bit[7:0]: Sensor 1 sum BGR[1] reg3 G channel[23:16]
0x80206D36	SNR1_SUM_REG3_G_BYTE1	–	R	Bit[7:0]: Sensor 1 sum BGR[1] reg3 G channel[15:8]
0x80206D37	SNR1_SUM_REG3_G_BYTE0	–	R	Bit[7:0]: Sensor 1 sum BGR[1] reg3 G channel[7:0]
0x80206D38	SNR1_SUM_REG3_R_BYTE3	–	R	Bit[7:0]: Sensor 1 sum BGR[2] reg3 R channel[31:24]
0x80206D39	SNR1_SUM_REG3_R_BYTE2	–	R	Bit[7:0]: Sensor 1 sum BGR[2] reg3 R channel[23:16]
0x80206D3A	SNR1_SUM_REG3_R_BYTE1	–	R	Bit[7:0]: Sensor 1 sum BGR[2] reg3 R channel[15:8]
0x80206D3B	SNR1_SUM_REG3_R_BYTE0	–	R	Bit[7:0]: Sensor 1 sum BGR[2] reg3 R channel[7:0]
0x80206D3C	SNR1_CNT_REG3_BYTE3	–	R	Bit[7:0]: Sensor 1 sum count reg3[31:24]
0x80206D3D	SNR1_CNT_REG3_BYTE2	–	R	Bit[7:0]: Sensor 1 sum count reg3[23:16]
0x80206D3E	SNR1_CNT_REG3_BYTE1	–	R	Bit[7:0]: Sensor 1 sum count reg3[15:8]
0x80206D3F	SNR1_CNT_REG3_BYTE0	–	R	Bit[7:0]: Sensor 1 sum count reg3[7:0]

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4.28 defect pixel correction (DPC) control

table 4-38 DPC registers (sheet 1 of 14)

address	register name	default value	R/W	description
0x80206200	SNR0_L_DPC_CTRL00	0x18	RW	Sensor 0 Long Exposure DPC Control Bit[7]: m_bEnableTail Bit[6]: m_bEnableSaturateCC Bit[5]: m_bEnableCrossCluster Bit[4]: m_bEnableSameChannelConnected Bit[3]: m_bEnableDiffChannelConnected Bit[2]: m_bEnableSmooth Bit[1]: m_bBWSensorEnable Bit[0]: m_bManualmode
0x80206201	SNR0_L_DPC_CTRL01	0xDF	RW	Sensor 0 Long Exposure DPC Control Bit[7]: Manual set m_nTClusterThres enable Bit[6]: m_bEnableComp Bit[5]: m_bVBP_en Bit[4]: m_bEnableColorLine_man Bit[3]: m_bCrossNew_man Bit[2]: m_bTCluster_man Bit[1:0]: m_nEdgeOption
0x80206202	SNR0_L_DPC_CTRL02	0xFF	RW	Sensor 0 Long Exposure DPC Control Bit[7]: Remove white pixel enable (m_bWhitePixel) Bit[6]: Remove black pixel enable (m_bBlackPixel) Bit[5:4]: m_nUnSatNumCross Bit[3:2]: m_nUnSatNum Bit[1:0]: m_nVerticalNum
0x80206203	SNR0_L_DPC_WTHRE	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC manual white threshold (m_nWThre_man)
0x80206204	SNR0_L_DPC_BTHRE	0x20	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC manual black threshold (m_nBThre_man)
0x80206205	SNR0_L_DPC_THRE1	0x10	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC threshold 1 for calculation (m_nPatternThre1)
0x80206206	SNR0_L_DPC_THRE2	0x20	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC threshold 2 for calculation (m_nRegThre)
0x80206207	SNR0_L_DPC_THRE3	0x10	RW	Bit[7:0]: Sensor 0 long exposure DPC threshold 3 for calculation (m_nPatternThre2)

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table 4-38 DPC registers (sheet 2 of 14)

address	register name	default value	R/W	description
0x80206208	SNR0_L_DPC_ THRE4	0x18	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC threshold 4 for calculation (m_nHCThre)
0x80206209	SNR0_L_DPC_ WTHRE_LIST0	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC white threshold list0 (m_nWThresList[0])
0x8020620A	SNR0_L_DPC_ WTHRE_LIST1	0x04	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC white threshold list1 (m_nWThresList[1])
0x8020620B	SNR0_L_DPC_ WTHRE_LIST2	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC white threshold list2 (m_nWThresList[2])
0x8020620C	SNR0_L_DPC_ WTHRE_LIST3	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC white threshold list3 (m_nWThresList[3])
0x8020620D	SNR0_L_DPC_ BTHRE_LIST0	0x0C	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC black threshold list0 (m_nBThresList[0])
0x8020620E	SNR0_L_DPC_ BTHRE_LIST1	0x06	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC black threshold list1 (m_nBThresList[1])
0x8020620F	SNR0_L_DPC_ BTHRE_LIST2	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC black threshold list2 (m_nBThresList[2])
0x80206210	SNR0_L_DPC_ BTHRE_LIST3	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC black threshold list3 (m_nBThresList[3])
0x80206211	SNR0_L_DPC_ SAT	0xFF	RW	Bit[7:0]: Sensor 0 long exposure DPC saturate level (m_nSaturate)
0x80206212	SNR0_L_DPC_ VB_GAIN_TH1	0x07	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC m_nVB_gain_th1
0x80206213	SNR0_L_DPC_ VB_GAIN_TH2	0x03	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC m_nVB_gain_th2
0x80206214	SNR0_L_DPC_ SMOOTH_ GLIST0	0x03	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC smooth gain list 0 (m_nGainListSmooth[0])
0x80206215	SNR0_L_DPC_ SMOOTH_ GLIST1	0x07	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC smooth gain list 1 (m_nGainListSmooth[1])

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table 4-38 DPC registers (sheet 3 of 14)

address	register name	default value	R/W	description
0x80206216	SNR0_L_DPC_SMOOTH_GLIST2	0x0F	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC smooth gain list 2 (m_nGainListSmooth[2])
0x80206217	SNR0_L_DPC_SMGAIN_TH1	0x07	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC smooth gain threshold 1 (m_nSmooth_gain_th1)
0x80206218	SNR0_L_DPC_SMGAIN_TH2	0x03	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 long exposure DPC smooth gain threshold 2 (m_nSmooth_gain_th2)
0x80206219	SNR0_L_DPC_UNSAT	0xF0	RW	Bit[7:0]: Sensor 0 Long exposure DPC unsaturate level (m_nUnSaturate)
0x8020621A	SNR0_L_DPC_TTHRE	0x08	RW	Bit[7:0]: Sensor 0 Long exposure DPC T cluster threshold (m_nTClusterThres)
0x80206220	SNR0_S_DPC_CTRL00	0x18	RW	Sensor 0 Short Exposure DPC Control Bit[7]: m_bEnableTail Bit[6]: m_bEnableSaturateCC Bit[5]: m_bEnableCrossCluster Bit[4]: m_bEnableSameChannelConnected Bit[3]: m_bEnableDiffChannelConnected Bit[2]: m_bEnableSmooth Bit[1]: m_bBWSensorEnable Bit[0]: m_bManualmode
0x80206221	SNR0_S_DPC_CTRL01	0xDF	RW	Sensor 0 Short Exposure DPC Control Bit[7]: Manual set m_nTClusterThres enable Bit[6]: m_bEnableComp Bit[5]: m_bVBP_en Bit[4]: m_bEnableColorLine_man Bit[3]: m_bCrossNew_man Bit[2]: m_bTCluster_man Bit[1:0]: m_nEdgeOption
0x80206222	SNR0_S_DPC_CTRL02	0xFF	RW	Sensor 0 Short Exposure DPC Control Bit[7]: Remove white pixel enable (m_bWhitePixel) Bit[6]: Remove black pixel enable (m_bBlackPixel) Bit[5:4]: m_nUnSatNumCross Bit[3:2]: m_nUnSatNum Bit[1:0]: m_nVerticalNum
0x80206223	SNR0_S_DPC_WTHRE	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC manual white threshold (m_nWThre_man)
0x80206224	SNR0_S_DPC_BTHRE	0x20	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC manual black threshold (m_nBThre_man)

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table 4-38 DPC registers (sheet 4 of 14)

address	register name	default value	R/W	description
0x80206225	SNR0_S_DPC_THRE1	0x10	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC threshold 1 for calculation (m_nPatternThre1)
0x80206226	SNR0_S_DPC_THRE2	0x20	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC threshold 2 for calculation (m_nRegThre)
0x80206227	SNR0_S_DPC_THRE3	0x10	RW	Bit[7:0]: Sensor 0 short exposure DPC threshold 3 for calculation (m_nPatternThre2)
0x80206228	SNR0_S_DPC_THRE4	0x18	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC threshold 4 for calculation (m_nHCThre)
0x80206229	SNR0_S_DPC_WTHRE_LIST0	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC white threshold list0 (m_nWThresList[0])
0x8020622A	SNR0_S_DPC_WTHRE_LIST1	0x04	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC white threshold list1 (m_nWThresList[1])
0x8020622B	SNR0_S_DPC_WTHRE_LIST2	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC white threshold list2 (m_nWThresList[2])
0x8020622C	SNR0_S_DPC_WTHRE_LIST3	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC white threshold list3 (m_nWThresList[3])
0x8020622D	SNR0_S_DPC_BTHRE_LIST0	0x0C	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC black threshold list0 (m_nBThresList[0])
0x8020622E	SNR0_S_DPC_BTHRE_LIST1	0x06	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC black threshold list1 (m_nBThresList[1])
0x8020622F	SNR0_S_DPC_BTHRE_LIST2	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC black threshold list2 (m_nBThresList[2])
0x80206230	SNR0_S_DPC_BTHRE_LIST3	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC black threshold list3 (m_nBThresList[3])
0x80206231	SNR0_S_DPC_SAT	0xFF	RW	Bit[7:0]: Sensor 0 short exposure DPC saturate level (m_nSaturate)
0x80206232	SNR0_S_DPC_VB_GAIN_TH1	0x07	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC m_nVB_gain_th1

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table 4-38 DPC registers (sheet 5 of 14)

address	register name	default value	R/W	description
0x80206233	SNR0_S_DPC_ VB_GAIN_TH2	0x03	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC m_nVB_gain_th2
0x80206234	SNR0_S_DPC_ SMOOTH_ GLIST0	0x03	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC smooth gain list 0 (m_nGainListSmooth[0])
0x80206235	SNR0_S_DPC_ SMOOTH_ GLIST1	0x07	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC smooth gain list 1 (m_nGainListSmooth[1])
0x80206236	SNR0_S_DPC_ SMOOTH_ GLIST2	0x0F	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC smooth gain list 2 (m_nGainListSmooth[2])
0x80206237	SNR0_S_DPC_ SMGAIN_TH1	0x07	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC smooth gain threshold 1 (m_nSmooth_gain_th1)
0x80206238	SNR0_S_DPC_ SMGAIN_TH2	0x03	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 short exposure DPC smooth gain threshold 2 (m_nSmooth_gain_th2)
0x80206239	SNR0_S_DPC_ UNSAT	0xF0	RW	Bit[7:0]: Sensor 0 short exposure DPC unsaturate level (m_nUnSaturate)
0x8020623A	SNR0_S_DPC_ TTHRE	0x08	RW	Bit[7:0]: Sensor 0 short exposure DPC T cluster threshold (m_nTClusterThres)
0x80206240	SNR0_VS_DPC _CTRL00	0x18	RW	Sensor 0 Very Short Exposure DPC Control Bit[7]: m_bEnableTail Bit[6]: m_bEnableSaturateCC Bit[5]: m_bEnableCrossCluster Bit[4]: m_bEnableSameChannelConnected Bit[3]: m_bEnableDiffChannelConnected Bit[2]: m_bEnableSmooth Bit[1]: m_bBWSensorEnable Bit[0]: m_bManualmode
0x80206241	SNR0_VS_DPC _CTRL01	0xDF	RW	Sensor 0 Very Short Exposure DPC Control Bit[7]: Manual set m_nTClusterThres enable Bit[6]: m_bEnableComp Bit[5]: m_bVBP_en Bit[4]: m_bEnableColorLine_man Bit[3]: m_bCrossNew_man Bit[2]: m_bTCluster_man Bit[1:0]: m_nEdgeOption

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table 4-38 DPC registers (sheet 6 of 14)

address	register name	default value	R/W	description
0x80206242	SNR0_VS_DPC _CTRL02	0xFF	RW	Sensor 0 Very Short Exposure DPC Control Bit[7]: Remove white pixel enable (m_bWhitePixel) Bit[6]: Remove black pixel enable (m_bBlackPixel) Bit[5:4]: m_nUnSatNumCross Bit[3:2]: m_nUnSatNum Bit[1:0]: m_nVerticalNum
0x80206243	SNR0_VS_DPC _WTHRE	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC manual white threshold (m_nWThre_man)
0x80206244	SNR0_VS_DPC _BTHRE	0x20	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC manual black threshold (m_nBThre_man)
0x80206245	SNR0_VS_DPC _THRE1	0x10	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC threshold 1 for calculation (m_nPatternThre1)
0x80206246	SNR0_VS_DPC _THRE2	0x20	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC threshold 2 for calculation (m_nRegThre)
0x80206247	SNR0_VS_DPC _THRE3	0x10	RW	Bit[7:0]: Sensor 0 very short exposure DPC threshold 3 for calculation (m_nPatternThre2)
0x80206248	SNR0_VS_DPC _THRE4	0x18	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC threshold 4 for calculation (m_nHCThre)
0x80206249	SNR0_VS_DPC _WTHRE_LIST0	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC white threshold list0 (m_nWThresList[0])
0x8020624A	SNR0_VS_DPC _WTHRE_LIST1	0x04	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC white threshold list1 (m_nWThresList[1])
0x8020624B	SNR0_VS_DPC _WTHRE_LIST2	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC white threshold list2 (m_nWThresList[2])
0x8020624C	SNR0_VS_DPC _WTHRE_LIST3	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC white threshold list3 (m_nWThresList[3])

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table 4-38 DPC registers (sheet 7 of 14)

address	register name	default value	R/W	description
0x8020624D	SNR0_VS_DPC _BTHRE_LIST0	0x0C	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC black threshold list0 (m_nBThresList[0])
0x8020624E	SNR0_VS_DPC _BTHRE_LIST1	0x06	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC black threshold list1 (m_nBThresList[1])
0x8020624F	SNR0_VS_DPC _BTHRE_LIST2	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC black threshold list2 (m_nBThresList[2])
0x80206250	SNR0_VS_DPC _BTHRE_LIST3	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC black threshold list3 (m_nBThresList[3])
0x80206251	SNR0_VS_DPC _SAT	0xFF	RW	Bit[7:0]: Sensor 0 very short exposure DPC saturate level (m_nSaturate)
0x80206252	SNR0_VS_DPC _VB_GAIN_TH1	0x07	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC m_nVB_gain_th1
0x80206253	SNR0_VS_DPC _VB_GAIN_TH2	0x03	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC m_nVB_gain_th2
0x80206254	SNR0_VS_DPC _SMOOTH_GLI ST0	0x03	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC smooth gain list 0 (m_nGainListSmooth[0])
0x80206255	SNR0_VS_DPC _SMOOTH_GLI ST1	0x07	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC smooth gain list 1 (m_nGainListSmooth[1])
0x80206256	SNR0_VS_DPC _SMOOTH_GLI ST2	0x0F	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC smooth gain list 2 (m_nGainListSmooth[2])
0x80206257	SNR0_VS_DPC _SMGAIN_TH1	0x07	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC smooth gain threshold 1 (m_nSmooth_gain_th1)
0x80206258	SNR0_VS_DPC _SMGAIN_TH2	0x03	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 very short exposure DPC smooth gain threshold 2 (m_nSmooth_gain_th2)
0x80206259	SNR0_VS_DPC _UNSAT	0xF0	RW	Bit[7:0]: Sensor 0 very short exposure DPC unsaturate level (m_nUnSaturate)

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table 4-38 DPC registers (sheet 8 of 14)

address	register name	default value	R/W	description
0x8020625A	SNR0_VS_DPC _TTHRE	0x08	RW	Bit[7:0]: Sensor 0 very short exposure DPC T cluster threshold (m_nTClusterThres)
0x80206280	SNR1_L_DPC_ CTRL00	0x18	RW	Sensor 1 Long Exposure DPC Control Bit[7]: m_bEnableTail Bit[6]: m_bEnableSaturateCC Bit[5]: m_bEnableCrossCluster Bit[4]: m_bEnableSameChannelConnected Bit[3]: m_bEnableDiffChannelConnected Bit[2]: m_bEnableSmooth Bit[1]: m_bBWSensorEnable Bit[0]: m_bManualmode
0x80206281	SNR1_L_DPC_ CTRL01	0xDF	RW	Sensor 1 Long Exposure DPC Control Bit[7]: Manual set m_nTClusterThres enable Bit[6]: m_bEnableComp Bit[5]: m_bVBP_en Bit[4]: m_bEnableColorLine_man Bit[3]: m_bCrossNew_man Bit[2]: m_bTCluster_man Bit[1:0]: m_nEdgeOption
0x80206282	SNR1_L_DPC_ CTRL02	0xFF	RW	Sensor 1 Long Exposure DPC Control Bit[7]: Remove white pixel enable (m_bWhitePixel) Bit[6]: Remove black pixel enable (m_bBlackPixel) Bit[5:4]: m_nUnSatNumCross Bit[3:2]: m_nUnSatNum Bit[1:0]: m_nVerticalNum
0x80206283	SNR1_L_DPC_ WTHRE	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC manual white threshold (m_nWThre_man)
0x80206284	SNR1_L_DPC_ BTHRE	0x20	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC manual black threshold (m_nBThre_man)
0x80206285	SNR1_L_DPC_ THRE1	0x10	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC threshold 1 for calculation (m_nPatternThre1)
0x80206286	SNR1_L_DPC_ THRE2	0x20	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC threshold 2 for calculation (m_nRegThre)
0x80206287	SNR1_L_DPC_ THRE3	0x10	RW	Bit[7:0]: Sensor 1 long exposure DPC threshold 3 for calculation (m_nPatternThre2)
0x80206288	SNR1_L_DPC_ THRE4	0x18	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC threshold 4 for calculation (m_nHCThre)

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table 4-38 DPC registers (sheet 9 of 14)

address	register name	default value	R/W	description
0x80206289	SNR1_L_DPC_ WTHRE_LIST0	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC white threshold list0 (m_nWThresList[0])
0x8020628A	SNR1_L_DPC_ WTHRE_LIST1	0x04	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC white threshold list1 (m_nWThresList[1])
0x8020628B	SNR1_L_DPC_ WTHRE_LIST2	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC white threshold list2 (m_nWThresList[2])
0x8020628C	SNR1_L_DPC_ WTHRE_LIST3	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC white threshold list3 (m_nWThresList[3])
0x8020628D	SNR1_L_DPC_ BTHRE_LIST0	0x0C	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC black threshold list0 (m_nBThresList[0])
0x8020628E	SNR1_L_DPC_ BTHRE_LIST1	0x06	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC black threshold list1 (m_nBThresList[1])
0x8020628F	SNR1_L_DPC_ BTHRE_LIST2	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC black threshold list2 (m_nBThresList[2])
0x80206290	SNR1_L_DPC_ BTHRE_LIST3	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC black threshold list3 (m_nBThresList[3])
0x80206291	SNR1_L_DPC_ SAT	0xFF	RW	Bit[7:0]: Sensor 1 long exposure DPC saturate level (m_nSaturate)
0x80206292	SNR1_L_DPC_ VB_GAIN_TH1	0x07	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC m_nVB_gain_th1
0x80206293	SNR1_L_DPC_ VB_GAIN_TH2	0x03	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC m_nVB_gain_th2
0x80206294	SNR1_L_DPC_ SMOOTH_ GLIST0	0x03	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC smooth gain list 0 (m_nGainListSmooth[0])
0x80206295	SNR1_L_DPC_ SMOOTH_ GLIST1	0x07	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC smooth gain list 1 (m_nGainListSmooth[1])
0x80206296	SNR1_L_DPC_ SMOOTH_ GLIST2	0x0F	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC smooth gain list 2 (m_nGainListSmooth[2])

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table 4-38 DPC registers (sheet 10 of 14)

address	register name	default value	R/W	description
0x80206297	SNR1_L_DPC_SMGAIN_TH1	0x07	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC smooth gain threshold 1 (m_nSmooth_gain_th1)
0x80206298	SNR1_L_DPC_SMGAIN_TH2	0x03	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 long exposure DPC smooth gain threshold 2 (m_nSmooth_gain_th2)
0x80206299	SNR1_L_DPC_UNSAT	0xF0	RW	Bit[7:0]: Sensor 1 long exposure DPC unsaturate level (m_nUnSaturate)
0x8020629A	SNR1_L_DPC_TTHRE	0x08	RW	Bit[7:0]: Sensor 1 long exposure DPC T cluster threshold (m_nTClusterThres)
0x802062A0	SNR1_S_DPC_CTRL00	0x18	RW	Sensor 1 Short Exposure DPC Control Bit[7]: m_bEnableTail Bit[6]: m_bEnableSaturateCC Bit[5]: m_bEnableCrossCluster Bit[4]: m_bEnableSameChannelConnected Bit[3]: m_bEnableDiffChannelConnected Bit[2]: m_bEnableSmooth Bit[1]: m_bBWSensorEnable Bit[0]: m_bManualmode
0x802062A1	SNR1_S_DPC_CTRL01	0xDF	RW	Sensor 1 Short Exposure DPC Control Bit[7]: Manual set m_nTClusterThres enable Bit[6]: m_bEnableComp Bit[5]: m_bVBP_en Bit[4]: m_bEnableColorLine_man Bit[3]: m_bCrossNew_man Bit[2]: m_bTCluster_man Bit[1:0]: m_nEdgeOption
0x802062A2	SNR1_S_DPC_CTRL02	0xFF	RW	Sensor 1 Short Exposure DPC Control Bit[7]: Remove white pixel enable (m_bWhitePixel) Bit[6]: Remove black pixel enable (m_bBlackPixel) Bit[5:4]: m_nUnSatNumCross Bit[3:2]: m_nUnSatNum Bit[1:0]: m_nVerticalNum
0x802062A3	SNR1_S_DPC_WTHRE	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC manual white threshold (m_nWThre_man)
0x802062A4	SNR1_S_DPC_BTHRE	0x20	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC manual black threshold (m_nBThre_man)
0x802062A5	SNR1_S_DPC_THRE1	0x10	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC threshold 1 for calculation (m_nPatternThre1)

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table 4-38 DPC registers (sheet 11 of 14)

address	register name	default value	R/W	description
0x802062A6	SNR1_S_DPC_THRE2	0x20	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC threshold 2 for calculation (m_nRegThre)
0x802062A7	SNR1_S_DPC_THRE3	0x10	RW	Bit[7:0]: Sensor 1 short exposure DPC threshold 3 for calculation (m_nPatternThre2)
0x802062A8	SNR1_S_DPC_THRE4	0x18	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC threshold 4 for calculation (m_nHCThre)
0x802062A9	SNR1_S_DPC_WTHRE_LIST0	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC white threshold list0 (m_nWThresList[0])
0x802062AA	SNR1_S_DPC_WTHRE_LIST1	0x04	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC white threshold list1 (m_nWThresList[1])
0x802062AB	SNR1_S_DPC_WTHRE_LIST2	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC white threshold list2 (m_nWThresList[2])
0x802062AC	SNR1_S_DPC_WTHRE_LIST3	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC white threshold list3 (m_nWThresList[3])
0x802062AD	SNR1_S_DPC_BTHRE_LIST0	0x0C	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC black threshold list0 (m_nBThresList[0])
0x802062AE	SNR1_S_DPC_BTHRE_LIST1	0x06	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC black threshold list1 (m_nBThresList[1])
0x802062AF	SNR1_S_DPC_BTHRE_LIST2	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC black threshold list2 (m_nBThresList[2])
0x802062B0	SNR1_S_DPC_BTHRE_LIST3	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC black threshold list3 (m_nBThresList[3])
0x802062B1	SNR1_S_DPC_SAT	0xFF	RW	Bit[7:0]: Sensor 1 short exposure DPC saturate level (m_nSaturate)
0x802062B2	SNR1_S_DPC_VB_GAIN_TH1	0x07	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC m_nVB_gain_th1
0x802062B3	SNR1_S_DPC_VB_GAIN_TH2	0x03	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC m_nVB_gain_th2

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table 4-38 DPC registers (sheet 12 of 14)

address	register name	default value	R/W	description
0x802062B4	SNR1_S_DPC_SMOOTH_GLIST0	0x03	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC smooth gain list 0 (m_nGainListSmooth[0])
0x802062B5	SNR1_S_DPC_SMOOTH_GLIST1	0x07	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC smooth gain list 1 (m_nGainListSmooth[1])
0x802062B6	SNR1_S_DPC_SMOOTH_GLIST2	0x0F	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC smooth gain list 2 (m_nGainListSmooth[2])
0x802062B7	SNR1_S_DPC_SMGAIN_TH1	0x07	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC smooth gain threshold 1 (m_nSmooth_gain_th1)
0x802062B8	SNR1_S_DPC_SMGAIN_TH2	0x03	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 short exposure DPC smooth gain threshold 2 (m_nSmooth_gain_th2)
0x802062B9	SNR1_S_DPC_UNSAT	0xF0	RW	Bit[7:0]: Sensor 1 short exposure DPC unsaturate level (m_nUnSaturate)
0x802062BA	SNR1_S_DPC_TTHRE	0x08	RW	Bit[7:0]: Sensor 1 short exposure DPC T cluster threshold (m_nTClusterThres)
0x802062C0	SNR1_VS_DPC_CTRL00	0x18	RW	Sensor 1 Very Short Exposure DPC Control Bit[7]: m_bEnableTail Bit[6]: m_bEnableSaturateCC Bit[5]: m_bEnableCrossCluster Bit[4]: m_bEnableSameChannelConnected Bit[3]: m_bEnableDiffChannelConnected Bit[2]: m_bEnableSmooth Bit[1]: m_bBWSensorEnable Bit[0]: m_bManualmode
0x802062C1	SNR1_VS_DPC_CTRL01	0xDF	RW	Sensor 1 Very Short Exposure DPC Control Bit[7]: Manual set m_nTClusterThres enable Bit[6]: m_bEnableComp Bit[5]: m_bVBP_en Bit[4]: m_bEnableColorLine_man Bit[3]: m_bCrossNew_man Bit[2]: m_bTCluster_man Bit[1:0]: m_nEdgeOption
0x802062C2	SNR1_VS_DPC_CTRL02	0xFF	RW	Sensor 1 Very Short Exposure DPC Control Bit[7]: Remove white pixel enable (m_bWhitePixel) Bit[6]: Remove black pixel enable (m_bBlackPixel) Bit[5:4]: m_nUnSatNumCross Bit[3:2]: m_nUnSatNum Bit[1:0]: m_nVerticalNum

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table 4-38 DPC registers (sheet 13 of 14)

address	register name	default value	R/W	description
0x802062C3	SNR1_VS_DPC _WTHRE	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC manual white threshold (m_nWThre_man)
0x802062C4	SNR1_VS_DPC _BTHREG	0x20	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC manual black threshold (m_nBThre_man)
0x802062C5	SNR1_VS_DPC _THRE1	0x10	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC threshold 1 for calculation (m_nPatternThre1)
0x802062C6	SNR1_VS_DPC _THRE2	0x20	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC threshold 2 for calculation (m_nRegThre)
0x802062C7	SNR1_VS_DPC _THRE3	0x10	RW	Bit[7:0]: Sensor 1 very short exposure DPC threshold 3 for calculation (m_nPatternThre2)
0x802062C8	SNR1_VS_DPC _THRE4	0x18	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC threshold 4 for calculation (m_nHCThre)
0x802062C9	SNR1_VS_DPC _WTHRE_LIST0	0x08	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC white threshold list0 (m_nWThresList[0])
0x802062CA	SNR1_VS_DPC _WTHRE_LIST1	0x04	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC white threshold list1 (m_nWThresList[1])
0x802062CB	SNR1_VS_DPC _WTHRE_LIST2	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC white threshold list2 (m_nWThresList[2])
0x802062CC	SNR1_VS_DPC _WTHRE_LIST3	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC white threshold list3 (m_nWThresList[3])
0x802062CD	SNR1_VS_DPC _BTHRE_LIST0	0x0C	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC black threshold list0 (m_nBThresList[0])
0x802062CE	SNR1_VS_DPC _BTHRE_LIST1	0x06	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC black threshold list1 (m_nBThresList[1])
0x802062CF	SNR1_VS_DPC _BTHRE_LIST2	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC black threshold list2 (m_nBThresList[2])

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table 4-38 DPC registers (sheet 14 of 14)

address	register name	default value	R/W	description
0x802062D0	SNR1_VS_DPC_BTHRE_LIST3	0x02	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC black threshold list3 (m_nBThresList[3])
0x802062D1	SNR1_VS_DPC_SAT	0xFF	RW	Bit[7:0]: Sensor 1 very short exposure DPC saturate level (m_nSaturate)
0x802062D2	SNR1_VS_DPC_VB_GAIN_TH1	0x07	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC m_nVB_gain_th1
0x802062D3	SNR1_VS_DPC_VB_GAIN_TH2	0x03	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC m_nVB_gain_th2
0x802062D4	SNR1_VS_DPC_SMOOTH_GLIST0	0x03	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC smooth gain list 0 (m_nGainListSmooth[0])
0x802062D5	SNR1_VS_DPC_SMOOTH_GLIST1	0x07	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC smooth gain list 1 (m_nGainListSmooth[1])
0x802062D6	SNR1_VS_DPC_SMOOTH_GLIST2	0x0F	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC smooth gain list 2 (m_nGainListSmooth[2])
0x802062D7	SNR1_VS_DPC_SMGAIN_TH1	0x07	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC smooth gain threshold 1 (m_nSmooth_gain_th1)
0x802062D8	SNR1_VS_DPC_SMGAIN_TH2	0x03	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 very short exposure DPC smooth gain threshold 2 (m_nSmooth_gain_th2)
0x802062D9	SNR1_VS_DPC_UNSAT	0xF0	RW	Bit[7:0]: Sensor 1 very short exposure DPC unsaturate level (m_nUnSaturate)
0x802062DA	SNR1_VS_DPC_TTHRE	0x08	RW	Bit[7:0]: Sensor 1 very short exposure DPC T cluster threshold (m_nTClusterThres)

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4.29 high dynamic range RAW data de-noise (HDR RAW DNS) control

table 4-39 HDR RAW DNS registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x80206300	SNR0_DNS_NOISELIST0_L	0x04	RW	Bit[7:0]: Sensor 0 noise list 0 for long exposure
0x80206301	SNR0_DNS_NOISELIST1_L	0x08	RW	Bit[7:0]: Sensor 0 noise list 1 for long exposure
0x80206302	SNR0_DNS_NOISELIST2_L	0x10	RW	Bit[7:0]: Sensor 0 noise list 2 for long exposure
0x80206303	SNR0_DNS_NOISELIST3_L	0x18	RW	Bit[7:0]: Sensor 0 noise list 3 for long exposure
0x80206304	SNR0_DNS_NOISELIST4_L	0x20	RW	Bit[7:0]: Sensor 0 noise list 4 for long exposure
0x80206305	SNR0_DNS_NOISELIST5_L	0x30	RW	Bit[7:0]: Sensor 0 noise list 5 for long exposure
0x80206306	SNR0_DNS_NOISELIST6_L	0x40	RW	Bit[7:0]: Sensor 0 noise list 6 for long exposure
0x80206307	SNR0_DNS_NOISELIST7_L	0x40	RW	Bit[7:0]: Sensor 0 noise list 7 for long exposure
0x80206308	SNR0_DNS_CTL_BITS_L	0x04	RW	Sensor 0 Long Exposure Channel Control Bit[7:5]: Reserved Bit[4]: G point denoise enable (m_bGDNSEnable) Bit[3:0]: NoiseYSlop (m_nNoiseYSlope)
0x80206309	SNR0_DNS_MAX_EDGE_THRE_L	0x3F	RW	Bit[7:0]: Sensor 0 maximum edge threshold for long exposure
0x8020630A	SNR0_DNS_NOISELIST0_S	0x04	RW	Bit[7:0]: Sensor 0 noise list 0 for short exposure
0x8020630B	SNR0_DNS_NOISELIST1_S	0x08	RW	Bit[7:0]: Sensor 0 noise list 1 for short exposure
0x8020630C	SNR0_DNS_NOISELIST2_S	0x10	RW	Bit[7:0]: Sensor 0 noise list 2 for short exposure
0x8020630D	SNR0_DNS_NOISELIST3_S	0x18	RW	Bit[7:0]: Sensor 0 noise list 3 for short exposure
0x8020630E	SNR0_DNS_NOISELIST4_S	0x20	RW	Bit[7:0]: Sensor 0 noise list 4 for short exposure

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table 4-39 HDR RAW DNS registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x8020630F	SNR0_DNS_NOISELIST5_S	0x30	RW	Bit[7:0]: Sensor 0 noise list 5 for short exposure
0x80206310	SNR0_DNS_NOISELIST6_S	0x40	RW	Bit[7:0]: Sensor 0 noise list 6 for short exposure
0x80206311	SNR0_DNS_NOISELIST7_S	0x40	RW	Bit[7:0]: Sensor 0 noise list 7 for short exposure
0x80206312	SNR0_DNS_CTL_BITS_S	0x04	RW	Sensor 0 Short Exposure Channel Control Bit[7:5]: Reserved Bit[4]: G point denoise enable (m_bGDNSEnable) Bit[3:0]: NoiseYSlop (m_nNoiseYSlope)
0x80206313	SNR0_DNS_MAX_EDGE_THRE_S	0x3F	RW	Bit[7:0]: Sensor 0 maximum edge threshold for short exposure
0x80206314	SNR0_DNS_NOISELIST0_VS	0x04	RW	Bit[7:0]: Sensor 0 noise list 0 for very short exposure
0x80206315	SNR0_DNS_NOISELIST1_VS	0x08	RW	Bit[7:0]: Sensor 0 noise list 1 for very short exposure
0x80206316	SNR0_DNS_NOISELIST2_VS	0x10	RW	Bit[7:0]: Sensor 0 noise list 2 for very short exposure
0x80206317	SNR0_DNS_NOISELIST3_VS	0x18	RW	Bit[7:0]: Sensor 0 noise list 3 for very short exposure
0x80206318	SNR0_DNS_NOISELIST4_VS	0x20	RW	Bit[7:0]: Sensor 0 noise list 4 for very short exposure
0x80206319	SNR0_DNS_NOISELIST5_VS	0x30	RW	Bit[7:0]: Sensor 0 noise list 5 for very short exposure
0x8020631A	SNR0_DNS_NOISELIST6_VS	0x40	RW	Bit[7:0]: Sensor 0 noise list 6 for very short exposure
0x8020631B	SNR0_DNS_NOISELIST7_VS	0x40	RW	Bit[7:0]: Sensor 0 noise list 7 for very short exposure
0x8020631C	SNR0_DNS_CTL_BITS_VS	0x04	RW	Sensor 0 Very Short Exposure Channel Control Bit[7:5]: Reserved Bit[4]: G point denoise enable (m_bGDNSEnable) Bit[3:0]: m_nNoiseYSlope

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table 4-39 HDR RAW DNS registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x8020631D	SNR0_DNS_MAX_EDGE_THRE_VS	0x3F	RW	Bit[7:0]: Sensor 0 maximum edge threshold for very short exposure
0x80206330	SNR1_DNS_NOISELIST0_L	0x04	RW	Bit[7:0]: Sensor 1 noise list 0 for long exposure
0x80206331	SNR1_DNS_NOISELIST1_L	0x08	RW	Bit[7:0]: Sensor 1 noise list 1 for long exposure
0x80206332	SNR1_DNS_NOISELIST2_L	0x10	RW	Bit[7:0]: Sensor 1 noise list 2 for long exposure
0x80206333	SNR1_DNS_NOISELIST3_L	0x18	RW	Bit[7:0]: Sensor 1 noise list 3 for long exposure
0x80206334	SNR1_DNS_NOISELIST4_L	0x20	RW	Bit[7:0]: Sensor 1 noise list 4 for long exposure
0x80206335	SNR1_DNS_NOISELIST5_L	0x30	RW	Bit[7:0]: Sensor 1 noise list 5 for long exposure
0x80206336	SNR1_DNS_NOISELIST6_L	0x40	RW	Bit[7:0]: Sensor 1 noise list 6 for long exposure
0x80206337	SNR1_DNS_NOISELIST7_L	0x40	RW	Bit[7:0]: Sensor 1 noise list 7 for long exposure
0x80206338	SNR1_DNS_CTL_BITS_L	0x04	RW	Sensor 1 Long Exposure Channel Control Bit[7:5]: Reserved Bit[4]: G point denoise enable (m_bGDNSEnable) Bit[3:0]: m_nNoiseYSlope
0x80206339	SNR1_DNS_MAX_EDGE_THRE_L	0x3F	RW	Bit[7:0]: Sensor 1 maximum edge threshold for long exposure
0x8020633A	SNR1_DNS_NOISELIST0_S	0x04	RW	Bit[7:0]: Sensor 1 noise list 0 for short exposure
0x8020633B	SNR1_DNS_NOISELIST1_S	0x08	RW	Bit[7:0]: Sensor 1 noise list 1 for short exposure
0x8020633C	SNR1_DNS_NOISELIST2_S	0x10	RW	Bit[7:0]: Sensor 1 noise list 2 for short exposure
0x8020633D	SNR1_DNS_NOISELIST3_S	0x18	RW	Bit[7:0]: Sensor 1 noise list 3 for short exposure
0x8020633E	SNR1_DNS_NOISELIST4_S	0x20	RW	Bit[7:0]: Sensor 1 noise list 4 for short exposure

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table 4-39 HDR RAW DNS registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x8020633F	SNR1_DNS_NOISELIST5_S	0x30	RW	Bit[7:0]: Sensor 1 noise list 5 for short exposure
0x80206340	SNR1_DNS_NOISELIST6_S	0x40	RW	Bit[7:0]: Sensor 1 noise list 6 for short exposure
0x80206341	SNR1_DNS_NOISELIST7_S	0x40	RW	Bit[7:0]: Sensor 1 noise list 7 for short exposure
0x80206342	SNR1_DNS_CTRL_BITS_S	0x04	RW	Sensor 1 Short Exposure Channel Control Bit[7:5]: Reserved Bit[4]: G point denoise enable (m_bGDNSEnable) Bit[3:0]: m_nNoiseYSlope
0x80206343	SNR1_DNS_MAX_EDGE_THRE_S	0x3F	RW	Bit[7:0]: Sensor 1 maximum edge threshold for short exposure
0x80206344	SNR1_DNS_NOISELIST0_VS	0x04	RW	Bit[7:0]: Sensor 1 noise list 0 for very short exposure
0x80206345	SNR1_DNS_NOISELIST1_VS	0x08	RW	Bit[7:0]: Sensor 1 noise list 1 for very short exposure
0x80206346	SNR1_DNS_NOISELIST2_VS	0x10	RW	Bit[7:0]: Sensor 1 noise list 2 for very short exposure
0x80206347	SNR1_DNS_NOISELIST3_VS	0x18	RW	Bit[7:0]: Sensor 1 noise list 3 for very short exposure
0x80206348	SNR1_DNS_NOISELIST4_VS	0x20	RW	Bit[7:0]: Sensor 1 noise list 4 for very short exposure
0x80206349	SNR1_DNS_NOISELIST5_VS	0x30	RW	Bit[7:0]: Sensor 1 noise list 5 for very short exposure
0x8020634A	SNR1_DNS_NOISELIST6_VS	0x40	RW	Bit[7:0]: Sensor 1 noise list 6 for very short exposure
0x8020634B	SNR1_DNS_NOISELIST7_VS	0x40	RW	Bit[7:0]: Sensor 1 noise list 7 for very short exposure
0x8020634C	SNR1_DNS_CTRL_BITS_VS	0x04	RW	Sensor 1 Very Short Exposure Channel Control Bit[7:5]: Reserved Bit[4]: G point denoise enable (m_bGDNSEnable) Bit[3:0]: m_nNoiseYSlope
0x8020634D	SNR1_DNS_MAX_EDGE_THRE_VS	0x3F	RW	Bit[7:0]: Sensor 1 maximum edge threshold for very short exposure

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4.30 ISP control

table 4-40 ISP control registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x80206000	R_ISP_CTRL_0	0x41	RW	ISP Control For Dual Sensors Bit[7]: Non-first frame flag select 0: Power on reset one 1: Logic reset one Bit[6]: YUV ROI statistic enable Bit[5]: ISP output SOF signal select 0: ISP generate SOF (default) 1: ISP input SOF Bit[4]: VSYNC edge select for internal process frame sync 0: Falling (default) 1: Rising Bit[3:2]: ISP output EOF signal select 00: ISP output last line HREF falling edge (default) 01: Pre_ISP generate EOF 10: CIP output EOF 11: AEC_AGC process done Bit[1]: ISP all sub modules clock enable Bit[0]: ISP enable
0x80206001	R_ISP_CTRL_1	0x00	RW	ISP Control For Dual Sensors Bit[7]: Reserved Bit[6]: VSYNC pulse length select 0: Three cycles 1: One cycle Bit[5]: UV DNS SRAM disable (active high) Bit[4]: RGBH DNS SRAM disable (active high) Bit[3]: OVPB buffer SRAM disable (active high) Bit[2]: HDR hist SRAM disable (active high) Bit[1]: Curve AWB SRAM disable (active high) Bit[0]: HDR buffer SRAM disable (active high)

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table 4-40 ISP control registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x80206002	R_ISP_CTRL_2	0x00	RW	ISP Control For Dual Sensors Bit[7]: Dummy line style 0: Line (sensor 0) by line (sensor 1) 1: One sensor first and then another one Bit[6]: Second sensor sub-modules manual control enable Bit[5]: First sensor sub-modules manual control enable Bit[4]: ISP RAW output manual format enable Bit[3:0]: ISP RAW output manual format
0x80206010	SNR0_ISP_CTRL_0	0xF7	RW	Bit[7]: Sensor 0 simple CIP enable Bit[6]: Sensor 0 HDR DNS enable Bit[5]: Sensor 0 DPC enable Bit[4]: Sensor 0 AWB gain enable Bit[3]: Sensor 0 make virtual long enable Bit[2]: Sensor 0 LENC enable Bit[1]: Sensor 0 digital gain enable Bit[0]: Sensor 0 enable
0x80206011	SNR0_ISP_CTRL_1	0xFF	RW	Bit[7]: Sensor 0 OVPB CIP enable Bit[6]: Sensor 0 OVPB RAW DNS enable Bit[5]: Sensor 0 stretch enable Bit[4]: Sensor 0 tone-mapping enable Bit[3]: Sensor 0 HDR statistic enable Bit[2]: Sensor 0 AEC_AGC enable Bit[1]: Sensor 0 curve AWB enable Bit[0]: Sensor 0 combine enable
0x80206012	SNR0_ISP_CTRL_2	0xFF	RW	Bit[7]: Sensor 0 pad enable Bit[6]: Sensor 0 window enable Bit[5]: Sensor 0 UV DNS enable Bit[4]: Sensor 0 SDE enable Bit[3]: Sensor 0 RGB2YUV enable Bit[2]: Reserved Bit[1]: Sensor 0 RGB gamma enable Bit[0]: Sensor 0 CMX enable

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table 4-40 ISP control registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x80206013	SNR0_ISP_CTRL_3	0x80	RW	Bit[7]: Sensor 0 PWL RAW/Y enable Bit[6]: Sensor 0 YUV drop enable Bit[5]: Sensor 0 manual input size enable Bit[4]: Sensor 0 UV output sequence select 0: U first (default) 1: V first Bit[3:2]: Sensor 0 RGB2YUV bypass channel select 0x: G 10: B 11: R Bit[1:0]: Sensor 0 CFA pattern
0x80206014	SNR0_ISP_CTRL_4	0x00	RW	Bit[7]: Sensor 0 YUV2RGB enable Bit[6]: Sensor 0 RGB output R/B swap Bit[5:4]: Sensor 0 Y skip Bit[3:2]: Sensor 0 X skip Bit[1]: Sensor 0 flip flag Bit[0]: Sensor 0 mirror flag
0x80206015	SNR0_ISP_CTRL_5	0x66	RW	Bit[7:5]: Sensor 0 OVPB buffer manual dummy line number Bit4]: Sensor 0 OVPB buffer manual dummy enable Bit[3:1]: Sensor 0 HDR buffer manual dummy line number Bit[0]: Sensor 0 HDR buffer manual dummy enable
0x80206016	SNR0_ISP_CTRL_6	0x01	RW	Bit[7:0]: Sensor 0 buffer manual dummy HREF blank number[15:8]
0x80206017	SNR0_ISP_CTRL_7	0x00	RW	Bit[7:0]: Sensor 0 buffer manual dummy HREF blank number[7:0]
0x80206018	SNR0_ISP_CTRL_8	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 array X offset[11:8]
0x80206019	SNR0_ISP_CTRL_9	0x00	RW	Bit[7:0]: Sensor 0 array X offset[7:0]
0x8020601A	SNR0_ISP_CTRL_A	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 array Y offset[10:8]
0x8020601B	SNR0_ISP_CTRL_B	0x00	RW	Bit[7:0]: Sensor 0 array Y offset[7:0]
0x8020601C	SNR0_ISP_CTRL_C	0x05	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual horizontal size[11:8]
0x8020601D	SNR0_ISP_CTRL_D	0x00	RW	Bit[7:0]: Sensor 0 manual horizontal size[7:0]

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table 4-40 ISP control registers (sheet 4 of 8)

address	register name	default value	R/W	description
0x8020601E	SNR0_ISP_CTRL_E	0x04	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 manual vertical size[10:8]
0x8020601F	SNR0_ISP_CTRL_F	0x38	RW	Bit[7:0]: Sensor 0 manual vertical size[7:0]
0x80206020	SNR0_ISP_CTRL_10	0x18	RW	Bit[7]: Reserved Bit[6]: Sensor 0 manual input/output format enable Bit[5:3]: Sensor 0 manual output format Bit[2:0]: Sensor 0 manual input format
0x80206021	SNR0_ISP_CTRL_11	0x00	RW	Bit[7:0]: Sensor 0 output window manual X start[7:0]
0x80206022	SNR0_ISP_CTRL_12	0x00	RW	Bit[7:0]: Sensor 0 output window manual Y start[7:0]
0x80206023	SNR0_ISP_CTRL_13	0x00	RW	Bit[7]: Sensor 0 output window manual control enable Bit[6:4]: Sensor 0 output window manual Y start[10:8] Bit[3:0]: Sensor 0 output window manual X start[11:8]
0x80206024	SNR0_ISP_CTRL_14	0x00	RW	Bit[7:0]: Sensor 0 output window manual horizontal size[7:0]
0x80206025	SNR0_ISP_CTRL_15	0x38	RW	Bit[7:0]: Sensor 0 output window manual vertical size[7:0]
0x80206026	SNR0_ISP_CTRL_16	0x45	RW	Bit[7]: Reserved Bit[6:4]: Sensor 0 output window manual vertical size[10:8] Bit[3:0]: Sensor 0 output window manual horizontal size[11:8]
0x80206027	SNR0_ISP_CTRL_17	0x00	RW	Bit[7:6]: Reserved Bit[5:4]: Sensor 0 gamma output bit-width select (RGB output case) 00: 12-bit 01: 8-bit 10: 10-bit 11: 12-bit Bit[3]: Sensor 0 OVPB buffer manual enable Bit[2]: Sensor 0 OVPB buffer manual control mode enable Bit[1]: Sensor 0 HDR buffer manual enable Bit[0]: Sensor 0 HDR buffer manual control mode enable

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table 4-40 ISP control registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x80206028	SNR0_ISP_CTRL_18	0x01	RW	Bit[7:4]: Sensor 0 manual dummy line valid blank cycles per period Bit[3:0]: Sensor 0 manual dummy line valid cycles per period
0x80206029	SNR0_ISP_CTRL_19	0x00	RW	Sensor 0 Control Bit[7:6]: Reserved Bit[5]: OVPB buffer manual dummy valid ratio enable Bit[4]: HDR buffer manual dummy valid ratio enable Bit[3]: OVPB buffer manual dummy valid blank number enable Bit[2]: HDR buffer manual dummy valid blank number enable Bit[1]: OVPB buffer manual dummy HREF blank number enable Bit[0]: HDR buffer manual dummy HREF blank number enable
0x8020602A	SNR0_ISP_CTRL_1A	0x00	RW	Bit[7:0]: Sensor 0 buffer manual dummy valid blank number of a line[15:8]
0x8020602B	SNR0_ISP_CTRL_1B	0x00	RW	Bit[7:0]: Sensor 0 buffer manual dummy valid blank number of a line[7:0]
0x80206030	SNR1_ISP_CTRL_0	0xF7	RW	Bit[7]: Sensor 1 simple CIP enable Bit[6]: Sensor 1 HDR DNS enable Bit[5]: Sensor 1 DPC enable Bit[4]: Sensor 1 AWB gain enable Bit[3]: Sensor 1 make virtual long enable Bit[2]: Sensor 1 LENC enable Bit[1]: Sensor 1 digital gain enable Bit[0]: Sensor 1 enable flag
0x80206031	SNR1_ISP_CTRL_1	0xFF	RW	Bit[7]: Sensor 1 OVPB CIP enable Bit[6]: Sensor 1 OVPB RAW DNS enable Bit[5]: Sensor 1 stretch enable Bit[4]: Sensor 1 tone-mapping enable Bit[3]: Sensor 1 HDR statistic enable Bit[2]: Sensor 1 AEC_AGC enable Bit[1]: Sensor 1 curve AWB enable Bit[0]: Sensor 1 combine enable
0x80206032	SNR1_ISP_CTRL_2	0xFF	RW	Bit[7]: Sensor 1 pad enable Bit[6]: Sensor 1 window enable Bit[5]: Sensor 1 UVDNS enable Bit[4]: Sensor 1 SDE enable Bit[3]: Sensor 1 RGB2YUV enable Bit[2]: Reserved Bit[1]: Sensor 1 RGB gamma enable Bit[0]: Sensor 1 CMX enable

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table 4-40 ISP control registers (sheet 6 of 8)

address	register name	default value	R/W	description
0x80206033	SNR1_ISP_CTRL_3	0x80	RW	Bit[7]: Sensor 1 PWL RAW/Y enable Bit[6]: Sensor 1 YUV drop enable Bit[5]: Sensor 1 manual input size enable Bit[4]: Sensor 1 UV output sequence select 0: U first (default) 1: V first Bit[3:2]: Sensor 1 RGB2YUV bypass channel select 0x: G 10: B 11: R Bit[1:0]: Sensor 1 CFA pattern
0x80206034	SNR1_ISP_CTRL_4	0x00	RW	Bit[7]: Sensor 1 YUV2RGB enable Bit[6]: Sensor 1 RGB output R/B swap Bit[5:4]: Sensor 1 Y skip Bit[3:2]: Sensor 1 X skip Bit[1]: Sensor 1 flip flag Bit[0]: Sensor 1 mirror flag
0x80206035	SNR1_ISP_CTRL_5	0x66	RW	Bit[7:5]: Sensor 1 OVPB buffer manual dummy line number Bit[4]: Sensor 1 OVPB buffer manual dummy line enable Bit[3:1]: Sensor 1 HDR buffer manual dummy line number Bit[0]: Sensor 1 HDR buffer manual dummy line enable
0x80206036	SNR1_ISP_CTRL_6	0x01	RW	Bit[7:0]: Sensor 1 buffer manual dummy HREF blank number[15:8]
0x80206037	SNR1_ISP_CTRL_7	0x00	RW	Bit[7:0]: Sensor 1 buffer manual dummy HREF blank number[7:0]
0x80206038	SNR1_ISP_CTRL_8	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 array crop X offset[11:8]
0x80206039	SNR1_ISP_CTRL_9	0x00	RW	Bit[7:0]: Sensor 1 array crop X offset[7:0]
0x8020603A	SNR1_ISP_CTRL_A	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 array crop Y offsett[10:8]
0x8020603B	SNR1_ISP_CTRL_B	0x00	RW	Bit[7:0]: Sensor 1 array crop Y offset[7:0]
0x8020603C	SNR1_ISP_CTRL_C	0x05	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual horizontal size[11:8]
0x8020603D	SNR1_ISP_CTRL_D	0x00	RW	Bit[7:0]: Sensor 1 manual horizontal size[7:0]

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table 4-40 ISP control registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x8020603E	SNR1_ISP_CTRL_E	0x04	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 manual vertical size[10:8]
0x8020603F	SNR1_ISP_CTRL_F	0x38	RW	Bit[7:0]: Sensor 1 manual vertical size[7:0]
0x80206040	SNR1_ISP_CTRL_10	0x30	RW	Bit[7]: Reserved Bit[6]: Sensor 1 manual input/output format enable Bit[5:3]: Sensor 1 manual output format Bit[2:0]: Sensor 1 manual input format
0x80206041	SNR1_ISP_CTRL_11	0x00	RW	Bit[7:0]: Sensor 1 output window manual X start[7:0]
0x80206042	SNR1_ISP_CTRL_12	0x00	RW	Bit[7:0]: Sensor 1 output window manual Y start[7:0]
0x80206043	SNR1_ISP_CTRL_13	0x00	RW	Bit[7]: Sensor 1 output window manual enable Bit[6:4]: Sensor 1 output window manual Y start[10:8] Bit[3:0]: Sensor 1 output window manual X start[11:8]
0x80206044	SNR1_ISP_CTRL_14	0x00	RW	Bit[7:0]: Sensor 1 output window manual horizontal size[7:0]
0x80206045	SNR1_ISP_CTRL_15	0x38	RW	Bit[7:0]: Sensor 1 output window manual vertical size[7:0]
0x80206046	SNR1_ISP_CTRL_16	0x45	RW	Bit[7]: Reserved Bit[6:4]: Sensor 1 output window manual vertical size[10:8] Bit[3:0]: Sensor 1 output window manual horizontal size[11:8]
0x80206047	SNR1_ISP_CTRL_17	0x00	RW	Bit[7:6]: Reserved Bit[5:4]: Sensor 1 gamma output bit-width select (RGB output case) 00: 12-bit 01: 8-bit 10: 10-bit 11: 12-bit Bit[3]: Sensor 1 OVPB buffer manual enable Bit[2]: Sensor 1 OVPB buffer manual control Bit[1]: Sensor 1 HDR buffer manual enable Bit[0]: Sensor 1 HDR buffer manual control

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table 4-40 ISP control registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x80206048	SNR1_ISP_CTRL_18	0x01	RW	Bit[7:4]: Sensor 1 manual dummy line valid blank cycles per period Bit[3:0]: Sensor 1 manual dummy line valid cycles per period
0x80206049	SNR1_ISP_CTRL_19	0x00	RW	Sensor 1 Control Bit[7:6]: Reserved Bit[5]: OVPB buffer manual dummy valid ratio enable Bit[4]: HDR buffer manual dummy valid ratio enable Bit[3]: OVPB buffer manual dummy valid blank number enable Bit[2]: HDR buffer manual dummy valid blank number enable Bit[1]: OVPB buffer manual dummy HREF blank number enable Bit[0]: HDR buffer manual dummy HREF blank number enable
0x8020604A	SNR1_ISP_CTRL_1A	0x00	RW	Bit[7:0]: Sensor 1 buffer manual dummy valid blank number[15:8]
0x8020604B	SNR1_ISP_CTRL_1B	0x00	RW	Bit[7:0]: Sensor 1 buffer manual dummy valid blank number[7:0]

4.31 lens correction (LENC) control

table 4-41 LENC registers (sheet 1 of 46)

address	register name	default value	R/W	description
0x80206400	SNR0_LENC_LV_G00	0x00	RW	Bit[7:0]: G00 of 8x8 G control point array for L/VS of sensor 0
0x80206401	SNR0_LENC_LV_G01	0x00	RW	Bit[7:0]: G01 of 8x8 G control point array for L/VS of sensor 0
0x80206402	SNR0_LENC_LV_G02	0x00	RW	Bit[7:0]: G02 of 8x8 G control point array for L/VS of sensor 0
0x80206403	SNR0_LENC_LV_G03	0x00	RW	Bit[7:0]: G03 of 8x8 G control point array for L/VS of sensor 0
0x80206404	SNR0_LENC_LV_G04	0x00	RW	Bit[7:0]: G04 of 8x8 G control point array for L/VS of sensor 0

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table 4-41 LENC registers (sheet 2 of 46)

address	register name	default value	R/W	description
0x80206405	SNR0_LENC_LV_G05	0x00	RW	Bit[7:0]: G05 of 8x8 G control point array for L/VS of sensor 0
0x80206406	SNR0_LENC_LV_G06	0x00	RW	Bit[7:0]: G06 of 8x8 G control point array for L/VS of sensor 0
0x80206407	SNR0_LENC_LV_G07	0x00	RW	Bit[7:0]: G07 of 8x8 G control point array for L/VS of sensor 0
0x80206408	SNR0_LENC_LV_G10	0x00	RW	Bit[7:0]: G10 of 8x8 G control point array for L/VS of sensor 0
0x80206409	SNR0_LENC_LV_G11	0x00	RW	Bit[7:0]: G11 of 8x8 G control point array for L/VS of sensor 0
0x8020640A	SNR0_LENC_LV_G12	0x00	RW	Bit[7:0]: G12 of 8x8 G control point array for L/VS of sensor 0
0x8020640B	SNR0_LENC_LV_G13	0x00	RW	Bit[7:0]: G13 of 8x8 G control point array for L/VS of sensor 0
0x8020640C	SNR0_LENC_LV_G14	0x00	RW	Bit[7:0]: G14 of 8x8 G control point array for L/VS of sensor 0
0x8020640D	SNR0_LENC_LV_G15	0x00	RW	Bit[7:0]: G15 of 8x8 G control point array for L/VS of sensor 0
0x8020640E	SNR0_LENC_LV_G16	0x00	RW	Bit[7:0]: G16 of 8x8 G control point array for L/VS of sensor 0
0x8020640F	SNR0_LENC_LV_G17	0x00	RW	Bit[7:0]: G17 of 8x8 G control point array for L/VS of sensor 0
0x80206410	SNR0_LENC_LV_G20	0x00	RW	Bit[7:0]: G20 of 8x8 G control point array for L/VS of sensor 0
0x80206411	SNR0_LENC_LV_G21	0x00	RW	Bit[7:0]: G21 of 8x8 G control point array for L/VS of sensor 0
0x80206412	SNR0_LENC_LV_G22	0x00	RW	Bit[7:0]: G22 of 8x8 G control point array for L/VS of sensor 0
0x80206413	SNR0_LENC_LV_G23	0x00	RW	Bit[7:0]: G23 of 8x8 G control point array for L/VS of sensor 0
0x80206414	SNR0_LENC_LV_G24	0x00	RW	Bit[7:0]: G24 of 8x8 G control point array for L/VS of sensor 0
0x80206415	SNR0_LENC_LV_G25	0x00	RW	Bit[7:0]: G25 of 8x8 G control point array for L/VS of sensor 0
0x80206416	SNR0_LENC_LV_G26	0x00	RW	Bit[7:0]: G26 of 8x8 G control point array for L/VS of sensor 0
0x80206417	SNR0_LENC_LV_G27	0x00	RW	Bit[7:0]: G27 of 8x8 G control point array for L/VS of sensor 0

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table 4-41 LENC registers (sheet 3 of 46)

address	register name	default value	R/W	description
0x80206418	SNR0_LENC_LV_G30	0x00	RW	Bit[7:0]: G30 of 8x8 G control point array for L/VS of sensor 0
0x80206419	SNR0_LENC_LV_G31	0x00	RW	Bit[7:0]: G31 of 8x8 G control point array for L/VS of sensor 0
0x8020641A	SNR0_LENC_LV_G32	0x00	RW	Bit[7:0]: G32 of 8x8 G control point array for L/VS of sensor 0
0x8020641B	SNR0_LENC_LV_G33	0x00	RW	Bit[7:0]: G33 of 8x8 G control point array for L/VS of sensor 0
0x8020641C	SNR0_LENC_LV_G34	0x00	RW	Bit[7:0]: G34 of 8x8 G control point array for L/VS of sensor 0
0x8020641D	SNR0_LENC_LV_G35	0x00	RW	Bit[7:0]: G35 of 8x8 G control point array for L/VS of sensor 0
0x8020641E	SNR0_LENC_LV_G36	0x00	RW	Bit[7:0]: G36 of 8x8 G control point array for L/VS of sensor 0
0x8020641F	SNR0_LENC_LV_G37	0x00	RW	Bit[7:0]: G37 of 8x8 G control point array for L/VS of sensor 0
0x80206420	SNR0_LENC_LV_G40	0x00	RW	Bit[7:0]: G40 of 8x8 G control point array for L/VS of sensor 0
0x80206421	SNR0_LENC_LV_G41	0x00	RW	Bit[7:0]: G41 of 8x8 G control point array for L/VS of sensor 0
0x80206422	SNR0_LENC_LV_G42	0x00	RW	Bit[7:0]: G42 of 8x8 G control point array for L/VS of sensor 0
0x80206423	SNR0_LENC_LV_G43	0x00	RW	Bit[7:0]: G43 of 8x8 G control point array for L/VS of sensor 0
0x80206424	SNR0_LENC_LV_G44	0x00	RW	Bit[7:0]: G44 of 8x8 G control point array for L/VS of sensor 0
0x80206425	SNR0_LENC_LV_G45	0x00	RW	Bit[7:0]: G45 of 8x8 G control point array for L/VS of sensor 0
0x80206426	SNR0_LENC_LV_G46	0x00	RW	Bit[7:0]: G46 of 8x8 G control point array for L/VS of sensor 0
0x80206427	SNR0_LENC_LV_G47	0x00	RW	Bit[7:0]: G47 of 8x8 G control point array for L/VS of sensor 0
0x80206428	SNR0_LENC_LV_G50	0x00	RW	Bit[7:0]: G50 of 8x8 G control point array for L/VS of sensor 0
0x80206429	SNR0_LENC_LV_G51	0x00	RW	Bit[7:0]: G51 of 8x8 G control point array for L/VS of sensor 0
0x8020642A	SNR0_LENC_LV_G52	0x00	RW	Bit[7:0]: G52 of 8x8 G control point array for L/VS of sensor 0

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table 4-41 LENC registers (sheet 4 of 46)

address	register name	default value	R/W	description
0x8020642B	SNR0_LENC_LV_G53	0x00	RW	Bit[7:0]: G53 of 8x8 G control point array for L/VS of sensor 0
0x8020642C	SNR0_LENC_LV_G54	0x00	RW	Bit[7:0]: G54 of 8x8 G control point array for L/VS of sensor 0
0x8020642D	SNR0_LENC_LV_G55	0x00	RW	Bit[7:0]: G55 of 8x8 G control point array for L/VS of sensor 0
0x8020642E	SNR0_LENC_LV_G56	0x00	RW	Bit[7:0]: G56 of 8x8 G control point array for L/VS of sensor 0
0x8020642F	SNR0_LENC_LV_G57	0x00	RW	Bit[7:0]: G57 of 8x8 G control point array for L/VS of sensor 0
0x80206430	SNR0_LENC_LV_G60	0x00	RW	Bit[7:0]: G60 of 8x8 G control point array for L/VS of sensor 0
0x80206431	SNR0_LENC_LV_G61	0x00	RW	Bit[7:0]: G61 of 8x8 G control point array for L/VS of sensor 0
0x80206432	SNR0_LENC_LV_G62	0x00	RW	Bit[7:0]: G62 of 8x8 G control point array for L/VS of sensor 0
0x80206433	SNR0_LENC_LV_G63	0x00	RW	Bit[7:0]: G63 of 8x8 G control point array for L/VS of sensor 0
0x80206434	SNR0_LENC_LV_G64	0x00	RW	Bit[7:0]: G64 of 8x8 G control point array for L/VS of sensor 0
0x80206435	SNR0_LENC_LV_G65	0x00	RW	Bit[7:0]: G65 of 8x8 G control point array for L/VS of sensor 0
0x80206436	SNR0_LENC_LV_G66	0x00	RW	Bit[7:0]: G66 of 8x8 G control point array for L/VS of sensor 0
0x80206437	SNR0_LENC_LV_G67	0x00	RW	Bit[7:0]: G67 of 8x8 G control point array for L/VS of sensor 0
0x80206438	SNR0_LENC_LV_G70	0x00	RW	Bit[7:0]: G70 of 8x8 G control point array for L/VS of sensor 0
0x80206439	SNR0_LENC_LV_G71	0x00	RW	Bit[7:0]: G71 of 8x8 G control point array for L/VS of sensor 0
0x8020643A	SNR0_LENC_LV_G72	0x00	RW	Bit[7:0]: G72 of 8x8 G control point array for L/VS of sensor 0
0x8020643B	SNR0_LENC_LV_G73	0x00	RW	Bit[7:0]: G73 of 8x8 G control point array for L/VS of sensor 0
0x8020643C	SNR0_LENC_LV_G74	0x00	RW	Bit[7:0]: G74 of 8x8 G control point array for L/VS of sensor 0
0x8020643D	SNR0_LENC_LV_G75	0x00	RW	Bit[7:0]: G75 of 8x8 G control point array for L/VS of sensor 0

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table 4-41 LENC registers (sheet 5 of 46)

address	register name	default value	R/W	description
0x8020643E	SNR0_LENC_LV_G76	0x00	RW	Bit[7:0]: G76 of 8x8 G control point array for L/VS of sensor 0
0x8020643F	SNR0_LENC_LV_G77	0x00	RW	Bit[7:0]: G77 of 8x8 G control point array for L/VS of sensor 0
0x80206440	SNR0_LENC_LV_B00	0x20	RW	Bit[7:0]: B00 of 8x8 B control point array for L/VS of sensor 0
0x80206441	SNR0_LENC_LV_B01	0x20	RW	Bit[7:0]: B01 of 8x8 B control point array for L/VS of sensor 0
0x80206442	SNR0_LENC_LV_B02	0x20	RW	Bit[7:0]: B02 of 8x8 B control point array for L/VS of sensor 0
0x80206443	SNR0_LENC_LV_B03	0x20	RW	Bit[7:0]: B03 of 8x8 B control point array for L/VS of sensor 0
0x80206444	SNR0_LENC_LV_B04	0x20	RW	Bit[7:0]: B04 of 8x8 B control point array for L/VS of sensor 0
0x80206445	SNR0_LENC_LV_B05	0x20	RW	Bit[7:0]: B05 of 8x8 B control point array for L/VS of sensor 0
0x80206446	SNR0_LENC_LV_B06	0x20	RW	Bit[7:0]: B06 of 8x8 B control point array for L/VS of sensor 0
0x80206447	SNR0_LENC_LV_B07	0x20	RW	Bit[7:0]: B07 of 8x8 B control point array for L/VS of sensor 0
0x80206448	SNR0_LENC_LV_B10	0x20	RW	Bit[7:0]: B10 of 8x8 B control point array for L/VS of sensor 0
0x80206449	SNR0_LENC_LV_B11	0x20	RW	Bit[7:0]: B11 of 8x8 B control point array for L/VS of sensor 0
0x8020644A	SNR0_LENC_LV_B12	0x20	RW	Bit[7:0]: B12 of 8x8 B control point array for L/VS of sensor 0
0x8020644B	SNR0_LENC_LV_B13	0x20	RW	Bit[7:0]: B13 of 8x8 B control point array for L/VS of sensor 0
0x8020644C	SNR0_LENC_LV_B14	0x20	RW	Bit[7:0]: B14 of 8x8 B control point array for L/VS of sensor 0
0x8020644D	SNR0_LENC_LV_B15	0x20	RW	Bit[7:0]: B15 of 8x8 B control point array for L/VS of sensor 0
0x8020644E	SNR0_LENC_LV_B16	0x20	RW	Bit[7:0]: B16 of 8x8 B control point array for L/VS of sensor 0
0x8020644F	SNR0_LENC_LV_B17	0x20	RW	Bit[7:0]: B17 of 8x8 B control point array for L/VS of sensor 0
0x80206450	SNR0_LENC_LV_B20	0x20	RW	Bit[7:0]: B20 of 8x8 B control point array for L/VS of sensor 0

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table 4-41 LENC registers (sheet 6 of 46)

address	register name	default value	R/W	description
0x80206451	SNR0_LENC_LV_B21	0x20	RW	Bit[7:0]: B21 of 8x8 B control point array for L/VS of sensor 0
0x80206452	SNR0_LENC_LV_B22	0x20	RW	Bit[7:0]: B22 of 8x8 B control point array for L/VS of sensor 0
0x80206453	SNR0_LENC_LV_B23	0x20	RW	Bit[7:0]: B23 of 8x8 B control point array for L/VS of sensor 0
0x80206454	SNR0_LENC_LV_B24	0x20	RW	Bit[7:0]: B24 of 8x8 B control point array for L/VS of sensor 0
0x80206455	SNR0_LENC_LV_B25	0x20	RW	Bit[7:0]: B25 of 8x8 B control point array for L/VS of sensor 0
0x80206456	SNR0_LENC_LV_B26	0x20	RW	Bit[7:0]: B26 of 8x8 B control point array for L/VS of sensor 0
0x80206457	SNR0_LENC_LV_B27	0x20	RW	Bit[7:0]: B27 of 8x8 B control point array for L/VS of sensor 0
0x80206458	SNR0_LENC_LV_B30	0x20	RW	Bit[7:0]: B30 of 8x8 B control point array for L/VS of sensor 0
0x80206459	SNR0_LENC_LV_B31	0x20	RW	Bit[7:0]: B31 of 8x8 B control point array for L/VS of sensor 0
0x8020645A	SNR0_LENC_LV_B32	0x20	RW	Bit[7:0]: B32 of 8x8 B control point array for L/VS of sensor 0
0x8020645B	SNR0_LENC_LV_B33	0x20	RW	Bit[7:0]: B33 of 8x8 B control point array for L/VS of sensor 0
0x8020645C	SNR0_LENC_LV_B34	0x20	RW	Bit[7:0]: B34 of 8x8 B control point array for L/VS of sensor 0
0x8020645D	SNR0_LENC_LV_B35	0x20	RW	Bit[7:0]: B35 of 8x8 B control point array for L/VS of sensor 0
0x8020645E	SNR0_LENC_LV_B36	0x20	RW	Bit[7:0]: B36 of 8x8 B control point array for L/VS of sensor 0
0x8020645F	SNR0_LENC_LV_B37	0x20	RW	Bit[7:0]: B37 of 8x8 B control point array for L/VS of sensor 0
0x80206460	SNR0_LENC_LV_B40	0x20	RW	Bit[7:0]: B40 of 8x8 B control point array for L/VS of sensor 0
0x80206461	SNR0_LENC_LV_B41	0x20	RW	Bit[7:0]: B41 of 8x8 B control point array for L/VS of sensor 0
0x80206462	SNR0_LENC_LV_B42	0x20	RW	Bit[7:0]: B42 of 8x8 B control point array for L/VS of sensor 0
0x80206463	SNR0_LENC_LV_B43	0x20	RW	Bit[7:0]: B43 of 8x8 B control point array for L/VS of sensor 0

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table 4-41 LENC registers (sheet 7 of 46)

address	register name	default value	R/W	description
0x80206464	SNR0_LENC_LV_B44	0x20	RW	Bit[7:0]: B44 of 8x8 B control point array for L/VS of sensor 0
0x80206465	SNR0_LENC_LV_B45	0x20	RW	Bit[7:0]: B45 of 8x8 B control point array for L/VS of sensor 0
0x80206466	SNR0_LENC_LV_B46	0x20	RW	Bit[7:0]: B46 of 8x8 B control point array for L/VS of sensor 0
0x80206467	SNR0_LENC_LV_B47	0x20	RW	Bit[7:0]: B47 of 8x8 B control point array for L/VS of sensor 0
0x80206468	SNR0_LENC_LV_B50	0x20	RW	Bit[7:0]: B50 of 8x8 B control point array for L/VS of sensor 0
0x80206469	SNR0_LENC_LV_B51	0x20	RW	Bit[7:0]: B51 of 8x8 B control point array for L/VS of sensor 0
0x8020646A	SNR0_LENC_LV_B52	0x20	RW	Bit[7:0]: B52 of 8x8 B control point array for L/VS of sensor 0
0x8020646B	SNR0_LENC_LV_B53	0x20	RW	Bit[7:0]: B53 of 8x8 B control point array for L/VS of sensor 0
0x8020646C	SNR0_LENC_LV_B54	0x20	RW	Bit[7:0]: B54 of 8x8 B control point array for L/VS of sensor 0
0x8020646D	SNR0_LENC_LV_B55	0x20	RW	Bit[7:0]: B55 of 8x8 B control point array for L/VS of sensor 0
0x8020646E	SNR0_LENC_LV_B56	0x20	RW	Bit[7:0]: B56 of 8x8 B control point array for L/VS of sensor 0
0x8020646F	SNR0_LENC_LV_B57	0x20	RW	Bit[7:0]: B57 of 8x8 B control point array for L/VS of sensor 0
0x80206470	SNR0_LENC_LV_B60	0x20	RW	Bit[7:0]: B60 of 8x8 B control point array for L/VS of sensor 0
0x80206471	SNR0_LENC_LV_B61	0x20	RW	Bit[7:0]: B61 of 8x8 B control point array for L/VS of sensor 0
0x80206472	SNR0_LENC_LV_B62	0x20	RW	Bit[7:0]: B62 of 8x8 B control point array for L/VS of sensor 0
0x80206473	SNR0_LENC_LV_B63	0x20	RW	Bit[7:0]: B63 of 8x8 B control point array for L/VS of sensor 0
0x80206474	SNR0_LENC_LV_B64	0x20	RW	Bit[7:0]: B64 of 8x8 B control point array for L/VS of sensor 0
0x80206475	SNR0_LENC_LV_B65	0x20	RW	Bit[7:0]: B65 of 8x8 B control point array for L/VS of sensor 0
0x80206476	SNR0_LENC_LV_B66	0x20	RW	Bit[7:0]: B66 of 8x8 B control point array for L/VS of sensor 0

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table 4-41 LENC registers (sheet 8 of 46)

address	register name	default value	R/W	description
0x80206477	SNR0_LENC_LV_B67	0x20	RW	Bit[7:0]: B67 of 8x8 B control point array for L/VS of sensor 0
0x80206478	SNR0_LENC_LV_B70	0x20	RW	Bit[7:0]: B70 of 8x8 B control point array for L/VS of sensor 0
0x80206479	SNR0_LENC_LV_B71	0x20	RW	Bit[7:0]: B71 of 8x8 B control point array for L/VS of sensor 0
0x8020647A	SNR0_LENC_LV_B72	0x20	RW	Bit[7:0]: B72 of 8x8 B control point array for L/VS of sensor 0
0x8020647B	SNR0_LENC_LV_B73	0x20	RW	Bit[7:0]: B73 of 8x8 B control point array for L/VS of sensor 0
0x8020647C	SNR0_LENC_LV_B74	0x20	RW	Bit[7:0]: B74 of 8x8 B control point array for L/VS of sensor 0
0x8020647D	SNR0_LENC_LV_B75	0x20	RW	Bit[7:0]: B75 of 8x8 B control point array for L/VS of sensor 0
0x8020647E	SNR0_LENC_LV_B76	0x20	RW	Bit[7:0]: B76 of 8x8 B control point array for L/VS of sensor 0
0x8020647F	SNR0_LENC_LV_B77	0x20	RW	Bit[7:0]: B77 of 8x8 B control point array for L/VS of sensor 0
0x80206480	SNR0_LENC_LV_R00	0x20	RW	Bit[7:0]: R00 of 8x8 R control point array for L/VS of sensor 0
0x80206481	SNR0_LENC_LV_R01	0x20	RW	Bit[7:0]: R01 of 8x8 R control point array for L/VS of sensor 0
0x80206482	SNR0_LENC_LV_R02	0x20	RW	Bit[7:0]: R02 of 8x8 R control point array for L/VS of sensor 0
0x80206483	SNR0_LENC_LV_R03	0x20	RW	Bit[7:0]: R03 of 8x8 R control point array for L/VS of sensor 0
0x80206484	SNR0_LENC_LV_R04	0x20	RW	Bit[7:0]: R04 of 8x8 R control point array for L/VS of sensor 0
0x80206485	SNR0_LENC_LV_R05	0x20	RW	Bit[7:0]: R05 of 8x8 R control point array for L/VS of sensor 0
0x80206486	SNR0_LENC_LV_R06	0x20	RW	Bit[7:0]: R06 of 8x8 R control point array for L/VS of sensor 0
0x80206487	SNR0_LENC_LV_R07	0x20	RW	Bit[7:0]: R07 of 8x8 R control point array for L/VS of sensor 0
0x80206488	SNR0_LENC_LV_R10	0x20	RW	Bit[7:0]: R10 of 8x8 R control point array for L/VS of sensor 0
0x80206489	SNR0_LENC_LV_R11	0x20	RW	Bit[7:0]: R11 of 8x8 R control point array for L/VS of sensor 0

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table 4-41 LENC registers (sheet 9 of 46)

address	register name	default value	R/W	description
0x8020648A	SNR0_LENC_LV_R12	0x20	RW	Bit[7:0]: R12 of 8x8 R control point array for L/VS of sensor 0
0x8020648B	SNR0_LENC_LV_R13	0x20	RW	Bit[7:0]: R13 of 8x8 R control point array for L/VS of sensor 0
0x8020648C	SNR0_LENC_LV_R14	0x20	RW	Bit[7:0]: R14 of 8x8 R control point array for L/VS of sensor 0
0x8020648D	SNR0_LENC_LV_R15	0x20	RW	Bit[7:0]: R15 of 8x8 R control point array for L/VS of sensor 0
0x8020648E	SNR0_LENC_LV_R16	0x20	RW	Bit[7:0]: R16 of 8x8 R control point array for L/VS of sensor 0
0x8020648F	SNR0_LENC_LV_R17	0x20	RW	Bit[7:0]: R17 of 8x8 R control point array for L/VS of sensor 0
0x80206490	SNR0_LENC_LV_R20	0x20	RW	Bit[7:0]: R20 of 8x8 R control point array for L/VS of sensor 0
0x80206491	SNR0_LENC_LV_R21	0x20	RW	Bit[7:0]: R21 of 8x8 R control point array for L/VS of sensor 0
0x80206492	SNR0_LENC_LV_R22	0x20	RW	Bit[7:0]: R22 of 8x8 R control point array for L/VS of sensor 0
0x80206493	SNR0_LENC_LV_R23	0x20	RW	Bit[7:0]: R23 of 8x8 R control point array for L/VS of sensor 0
0x80206494	SNR0_LENC_LV_R24	0x20	RW	Bit[7:0]: R24 of 8x8 R control point array for L/VS of sensor 0
0x80206495	SNR0_LENC_LV_R25	0x20	RW	Bit[7:0]: R25 of 8x8 R control point array for L/VS of sensor 0
0x80206496	SNR0_LENC_LV_R26	0x20	RW	Bit[7:0]: R26 of 8x8 R control point array for L/VS of sensor 0
0x80206497	SNR0_LENC_LV_R27	0x20	RW	Bit[7:0]: R27 of 8x8 R control point array for L/VS of sensor 0
0x80206498	SNR0_LENC_LV_R30	0x20	RW	Bit[7:0]: R30 of 8x8 R control point array for L/VS of sensor 0
0x80206499	SNR0_LENC_LV_R31	0x20	RW	Bit[7:0]: R31 of 8x8 R control point array for L/VS of sensor 0
0x8020649A	SNR0_LENC_LV_R32	0x20	RW	Bit[7:0]: R32 of 8x8 R control point array for L/VS of sensor 0
0x8020649B	SNR0_LENC_LV_R33	0x20	RW	Bit[7:0]: R33 of 8x8 R control point array for L/VS of sensor 0
0x8020649C	SNR0_LENC_LV_R34	0x20	RW	Bit[7:0]: R34 of 8x8 R control point array for L/VS of sensor 0

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table 4-41 LENC registers (sheet 10 of 46)

address	register name	default value	R/W	description
0x8020649D	SNR0_LENC_LV_R35	0x20	RW	Bit[7:0]: R35 of 8x8 R control point array for L/VS of sensor 0
0x8020649E	SNR0_LENC_LV_R36	0x20	RW	Bit[7:0]: R36 of 8x8 R control point array for L/VS of sensor 0
0x8020649F	SNR0_LENC_LV_R37	0x20	RW	Bit[7:0]: R37 of 8x8 R control point array for L/VS of sensor 0
0x802064A0	SNR0_LENC_LV_R40	0x20	RW	Bit[7:0]: R40 of 8x8 R control point array for L/VS of sensor 0
0x802064A1	SNR0_LENC_LV_R41	0x20	RW	Bit[7:0]: R41 of 8x8 R control point array for L/VS of sensor 0
0x802064A2	SNR0_LENC_LV_R42	0x20	RW	Bit[7:0]: R42 of 8x8 R control point array for L/VS of sensor 0
0x802064A3	SNR0_LENC_LV_R43	0x20	RW	Bit[7:0]: R43 of 8x8 R control point array for L/VS of sensor 0
0x802064A4	SNR0_LENC_LV_R44	0x20	RW	Bit[7:0]: R44 of 8x8 R control point array for L/VS of sensor 0
0x802064A5	SNR0_LENC_LV_R45	0x20	RW	Bit[7:0]: R45 of 8x8 R control point array for L/VS of sensor 0
0x802064A6	SNR0_LENC_LV_R46	0x20	RW	Bit[7:0]: R46 of 8x8 R control point array for L/VS of sensor 0
0x802064A7	SNR0_LENC_LV_R47	0x20	RW	Bit[7:0]: R47 of 8x8 R control point array for L/VS of sensor 0
0x802064A8	SNR0_LENC_LV_R50	0x20	RW	Bit[7:0]: R50 of 8x8 R control point array for L/VS of sensor 0
0x802064A9	SNR0_LENC_LV_R51	0x20	RW	Bit[7:0]: R51 of 8x8 R control point array for L/VS of sensor 0
0x802064AA	SNR0_LENC_LV_R52	0x20	RW	Bit[7:0]: R52 of 8x8 R control point array for L/VS of sensor 0
0x802064AB	SNR0_LENC_LV_R53	0x20	RW	Bit[7:0]: R53 of 8x8 R control point array for L/VS of sensor 0
0x802064AC	SNR0_LENC_LV_R54	0x20	RW	Bit[7:0]: R54 of 8x8 R control point array for L/VS of sensor 0
0x802064AD	SNR0_LENC_LV_R55	0x20	RW	Bit[7:0]: R55 of 8x8 R control point array for L/VS of sensor 0
0x802064AE	SNR0_LENC_LV_R56	0x20	RW	Bit[7:0]: R56 of 8x8 R control point array for L/VS of sensor 0
0x802064AF	SNR0_LENC_LV_R57	0x20	RW	Bit[7:0]: R57 of 8x8 R control point array for L/VS of sensor 0

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table 4-41 LENC registers (sheet 11 of 46)

address	register name	default value	R/W	description
0x802064B0	SNR0_LENC_LV_R60	0x20	RW	Bit[7:0]: R60 of 8x8 R control point array for L/VS of sensor 0
0x802064B1	SNR0_LENC_LV_R61	0x20	RW	Bit[7:0]: R61 of 8x8 R control point array for L/VS of sensor 0
0x802064B2	SNR0_LENC_LV_R62	0x20	RW	Bit[7:0]: R62 of 8x8 R control point array for L/VS of sensor 0
0x802064B3	SNR0_LENC_LV_R63	0x20	RW	Bit[7:0]: R63 of 8x8 R control point array for L/VS of sensor 0
0x802064B4	SNR0_LENC_LV_R64	0x20	RW	Bit[7:0]: R64 of 8x8 R control point array for L/VS of sensor 0
0x802064B5	SNR0_LENC_LV_R65	0x20	RW	Bit[7:0]: R65 of 8x8 R control point array for L/VS of sensor 0
0x802064B6	SNR0_LENC_LV_R66	0x20	RW	Bit[7:0]: R66 of 8x8 R control point array for L/VS of sensor 0
0x802064B7	SNR0_LENC_LV_R67	0x20	RW	Bit[7:0]: R67 of 8x8 R control point array for L/VS of sensor 0
0x802064B8	SNR0_LENC_LV_R70	0x20	RW	Bit[7:0]: R70 of 8x8 R control point array for L/VS of sensor 0
0x802064B9	SNR0_LENC_LV_R71	0x20	RW	Bit[7:0]: R71 of 8x8 R control point array for L/VS of sensor 0
0x802064BA	SNR0_LENC_LV_R72	0x20	RW	Bit[7:0]: R72 of 8x8 R control point array for L/VS of sensor 0
0x802064BB	SNR0_LENC_LV_R73	0x20	RW	Bit[7:0]: R73 of 8x8 R control point array for L/VS of sensor 0
0x802064BC	SNR0_LENC_LV_R74	0x20	RW	Bit[7:0]: R74 of 8x8 R control point array for L/VS of sensor 0
0x802064BD	SNR0_LENC_LV_R75	0x20	RW	Bit[7:0]: R75 of 8x8 R control point array for L/VS of sensor 0
0x802064BE	SNR0_LENC_LV_R76	0x20	RW	Bit[7:0]: R76 of 8x8 R control point array for L/VS of sensor 0
0x802064BF	SNR0_LENC_LV_R77	0x20	RW	Bit[7:0]: R77 of 8x8 R control point array for L/VS of sensor 0
0x802064C0	SNR0_LENC_S_G00	0x00	RW	Bit[7:0]: G00 of 8x8 G control point array for S of sensor 0
0x802064C1	SNR0_LENC_S_G01	0x00	RW	Bit[7:0]: G01 of 8x8 G control point array for S of sensor 0
0x802064C2	SNR0_LENC_S_G02	0x00	RW	Bit[7:0]: G02 of 8x8 G control point array for S of sensor 0

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table 4-41 LENC registers (sheet 12 of 46)

address	register name	default value	R/W	description
0x802064C3	SNR0_LENC_S_G03	0x00	RW	Bit[7:0]: G03 of 8x8 G control point array for S of sensor 0
0x802064C4	SNR0_LENC_S_G04	0x00	RW	Bit[7:0]: G04 of 8x8 G control point array for S of sensor 0
0x802064C5	SNR0_LENC_S_G05	0x00	RW	Bit[7:0]: G05 of 8x8 G control point array for S of sensor 0
0x802064C6	SNR0_LENC_S_G06	0x00	RW	Bit[7:0]: G06 of 8x8 G control point array for S of sensor 0
0x802064C7	SNR0_LENC_S_G07	0x00	RW	Bit[7:0]: G07 of 8x8 G control point array for S of sensor 0
0x802064C8	SNR0_LENC_S_G10	0x00	RW	Bit[7:0]: G10 of 8x8 G control point array for S of sensor 0
0x802064C9	SNR0_LENC_S_G11	0x00	RW	Bit[7:0]: G11 of 8x8 G control point array for S of sensor 0
0x802064CA	SNR0_LENC_S_G12	0x00	RW	Bit[7:0]: G12 of 8x8 G control point array for S of sensor 0
0x802064CB	SNR0_LENC_S_G13	0x00	RW	Bit[7:0]: G13 of 8x8 G control point array for S of sensor 0
0x802064CC	SNR0_LENC_S_G14	0x00	RW	Bit[7:0]: G14 of 8x8 G control point array for S of sensor 0
0x802064CD	SNR0_LENC_S_G15	0x00	RW	Bit[7:0]: G15 of 8x8 G control point array for S of sensor 0
0x802064CE	SNR0_LENC_S_G16	0x00	RW	Bit[7:0]: G16 of 8x8 G control point array for S of sensor 0
0x802064CF	SNR0_LENC_S_G17	0x00	RW	Bit[7:0]: G17 of 8x8 G control point array for S of sensor 0
0x802064D0	SNR0_LENC_S_G20	0x00	RW	Bit[7:0]: G20 of 8x8 G control point array for S of sensor 0
0x802064D1	SNR0_LENC_S_G21	0x00	RW	Bit[7:0]: G21 of 8x8 G control point array for S of sensor 0
0x802064D2	SNR0_LENC_S_G22	0x00	RW	Bit[7:0]: G22 of 8x8 G control point array for S of sensor 0
0x802064D3	SNR0_LENC_S_G23	0x00	RW	Bit[7:0]: G23 of 8x8 G control point array for S of sensor 0
0x802064D4	SNR0_LENC_S_G24	0x00	RW	Bit[7:0]: G24 of 8x8 G control point array for S of sensor 0
0x802064D5	SNR0_LENC_S_G25	0x00	RW	Bit[7:0]: G25 of 8x8 G control point array for S of sensor 0

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table 4-41 LENC registers (sheet 13 of 46)

address	register name	default value	R/W	description
0x802064D6	SNR0_LENC_S_G26	0x00	RW	Bit[7:0]: G26 of 8x8 G control point array for S of sensor 0
0x802064D7	SNR0_LENC_S_G27	0x00	RW	Bit[7:0]: G27 of 8x8 G control point array for S of sensor 0
0x802064D8	SNR0_LENC_S_G30	0x00	RW	Bit[7:0]: G30 of 8x8 G control point array for S of sensor 0
0x802064D9	SNR0_LENC_S_G31	0x00	RW	Bit[7:0]: G31 of 8x8 G control point array for S of sensor 0
0x802064DA	SNR0_LENC_S_G32	0x00	RW	Bit[7:0]: G32 of 8x8 G control point array for S of sensor 0
0x802064DB	SNR0_LENC_S_G33	0x00	RW	Bit[7:0]: G33 of 8x8 G control point array for S of sensor 0
0x802064DC	SNR0_LENC_S_G34	0x00	RW	Bit[7:0]: G34 of 8x8 G control point array for S of sensor 0
0x802064DD	SNR0_LENC_S_G35	0x00	RW	Bit[7:0]: G35 of 8x8 G control point array for S of sensor 0
0x802064DE	SNR0_LENC_S_G36	0x00	RW	Bit[7:0]: G36 of 8x8 G control point array for S of sensor 0
0x802064DF	SNR0_LENC_S_G37	0x00	RW	Bit[7:0]: G37 of 8x8 G control point array for S of sensor 0
0x802064E0	SNR0_LENC_S_G40	0x00	RW	Bit[7:0]: G40 of 8x8 G control point array for S of sensor 0
0x802064E1	SNR0_LENC_S_G41	0x00	RW	Bit[7:0]: G41 of 8x8 G control point array for S of sensor 0
0x802064E2	SNR0_LENC_S_G42	0x00	RW	Bit[7:0]: G42 of 8x8 G control point array for S of sensor 0
0x802064E3	SNR0_LENC_S_G43	0x00	RW	Bit[7:0]: G43 of 8x8 G control point array for S of sensor 0
0x802064E4	SNR0_LENC_S_G44	0x00	RW	Bit[7:0]: G44 of 8x8 G control point array for S of sensor 0
0x802064E5	SNR0_LENC_S_G45	0x00	RW	Bit[7:0]: G45 of 8x8 G control point array for S of sensor 0
0x802064E6	SNR0_LENC_S_G46	0x00	RW	Bit[7:0]: G46 of 8x8 G control point array for S of sensor 0
0x802064E7	SNR0_LENC_S_G47	0x00	RW	Bit[7:0]: G47 of 8x8 G control point array for S of sensor 0
0x802064E8	SNR0_LENC_S_G50	0x00	RW	Bit[7:0]: G50 of 8x8 G control point array for S of sensor 0

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table 4-41 LENC registers (sheet 14 of 46)

address	register name	default value	R/W	description
0x802064E9	SNR0_LENC_S_G51	0x00	RW	Bit[7:0]: G51 of 8x8 G control point array for S of sensor 0
0x802064EA	SNR0_LENC_S_G52	0x00	RW	Bit[7:0]: G52 of 8x8 G control point array for S of sensor 0
0x802064EB	SNR0_LENC_S_G53	0x00	RW	Bit[7:0]: G53 of 8x8 G control point array for S of sensor 0
0x802064EC	SNR0_LENC_S_G54	0x00	RW	Bit[7:0]: G54 of 8x8 G control point array for S of sensor 0
0x802064ED	SNR0_LENC_S_G55	0x00	RW	Bit[7:0]: G55 of 8x8 G control point array for S of sensor 0
0x802064EE	SNR0_LENC_S_G56	0x00	RW	Bit[7:0]: G56 of 8x8 G control point array for S of sensor 0
0x802064EF	SNR0_LENC_S_G57	0x00	RW	Bit[7:0]: G57 of 8x8 G control point array for S of sensor 0
0x802064F0	SNR0_LENC_S_G60	0x00	RW	Bit[7:0]: G60 of 8x8 G control point array for S of sensor 0
0x802064F1	SNR0_LENC_S_G61	0x00	RW	Bit[7:0]: G61 of 8x8 G control point array for S of sensor 0
0x802064F2	SNR0_LENC_S_G62	0x00	RW	Bit[7:0]: G62 of 8x8 G control point array for S of sensor 0
0x802064F3	SNR0_LENC_S_G63	0x00	RW	Bit[7:0]: G63 of 8x8 G control point array for S of sensor 0
0x802064F4	SNR0_LENC_S_G64	0x00	RW	Bit[7:0]: G64 of 8x8 G control point array for S of sensor 0
0x802064F5	SNR0_LENC_S_G65	0x00	RW	Bit[7:0]: G65 of 8x8 G control point array for S of sensor 0
0x802064F6	SNR0_LENC_S_G66	0x00	RW	Bit[7:0]: G66 of 8x8 G control point array for S of sensor 0
0x802064F7	SNR0_LENC_S_G67	0x00	RW	Bit[7:0]: G67 of 8x8 G control point array for S of sensor 0
0x802064F8	SNR0_LENC_S_G70	0x00	RW	Bit[7:0]: G70 of 8x8 G control point array for S of sensor 0
0x802064F9	SNR0_LENC_S_G71	0x00	RW	Bit[7:0]: G71 of 8x8 G control point array for S of sensor 0
0x802064FA	SNR0_LENC_S_G72	0x00	RW	Bit[7:0]: G72 of 8x8 G control point array for S of sensor 0
0x802064FB	SNR0_LENC_S_G73	0x00	RW	Bit[7:0]: G73 of 8x8 G control point array for S of sensor 0

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table 4-41 LENC registers (sheet 15 of 46)

address	register name	default value	R/W	description
0x802064FC	SNR0_LENC_S_G74	0x00	RW	Bit[7:0]: G74 of 8x8 G control point array for S of sensor 0
0x802064FD	SNR0_LENC_S_G75	0x00	RW	Bit[7:0]: G75 of 8x8 G control point array for S of sensor 0
0x802064FE	SNR0_LENC_S_G76	0x00	RW	Bit[7:0]: G76 of 8x8 G control point array for S of sensor 0
0x802064FF	SNR0_LENC_S_G77	0x00	RW	Bit[7:0]: G77 of 8x8 G control point array for S of sensor 0
0x80206500	SNR0_LENC_S_B00	0x20	RW	Bit[7:0]: B00 of 8x8 B control point array for S of sensor 0
0x80206501	SNR0_LENC_S_B01	0x20	RW	Bit[7:0]: B01 of 8x8 B control point array for S of sensor 0
0x80206502	SNR0_LENC_S_B02	0x20	RW	Bit[7:0]: B02 of 8x8 B control point array for S of sensor 0
0x80206503	SNR0_LENC_S_B03	0x20	RW	Bit[7:0]: B03 of 8x8 B control point array for S of sensor 0
0x80206504	SNR0_LENC_S_B04	0x20	RW	Bit[7:0]: B04 of 8x8 B control point array for S of sensor 0
0x80206505	SNR0_LENC_S_B05	0x20	RW	Bit[7:0]: B05 of 8x8 B control point array for S of sensor 0
0x80206506	SNR0_LENC_S_B06	0x20	RW	Bit[7:0]: B06 of 8x8 B control point array for S of sensor 0
0x80206507	SNR0_LENC_S_B07	0x20	RW	Bit[7:0]: B07 of 8x8 B control point array for S of sensor 0
0x80206508	SNR0_LENC_S_B10	0x20	RW	Bit[7:0]: B10 of 8x8 B control point array for S of sensor 0
0x80206509	SNR0_LENC_S_B11	0x20	RW	Bit[7:0]: B11 of 8x8 B control point array for S of sensor 0
0x8020650A	SNR0_LENC_S_B12	0x20	RW	Bit[7:0]: B12 of 8x8 B control point array for S of sensor 0
0x8020650B	SNR0_LENC_S_B13	0x20	RW	Bit[7:0]: B13 of 8x8 B control point array for S of sensor 0
0x8020650C	SNR0_LENC_S_B14	0x20	RW	Bit[7:0]: B14 of 8x8 B control point array for S of sensor 0
0x8020650D	SNR0_LENC_S_B15	0x20	RW	Bit[7:0]: B15 of 8x8 B control point array for S of sensor 0
0x8020650E	SNR0_LENC_S_B16	0x20	RW	Bit[7:0]: B16 of 8x8 B control point array for S of sensor 0

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table 4-41 LENC registers (sheet 16 of 46)

address	register name	default value	R/W	description
0x8020650F	SNR0_LENC_S_B17	0x20	RW	Bit[7:0]: B17 of 8x8 B control point array for S of sensor 0
0x80206510	SNR0_LENC_S_B20	0x20	RW	Bit[7:0]: B20 of 8x8 B control point array for S of sensor 0
0x80206511	SNR0_LENC_S_B21	0x20	RW	Bit[7:0]: B21 of 8x8 B control point array for S of sensor 0
0x80206512	SNR0_LENC_S_B22	0x20	RW	Bit[7:0]: B22 of 8x8 B control point array for S of sensor 0
0x80206513	SNR0_LENC_S_B23	0x20	RW	Bit[7:0]: B23 of 8x8 B control point array for S of sensor 0
0x80206514	SNR0_LENC_S_B24	0x20	RW	Bit[7:0]: B24 of 8x8 B control point array for S of sensor 0
0x80206515	SNR0_LENC_S_B25	0x20	RW	Bit[7:0]: B25 of 8x8 B control point array for S of sensor 0
0x80206516	SNR0_LENC_S_B26	0x20	RW	Bit[7:0]: B26 of 8x8 B control point array for S of sensor 0
0x80206517	SNR0_LENC_S_B27	0x20	RW	Bit[7:0]: B27 of 8x8 B control point array for S of sensor 0
0x80206518	SNR0_LENC_S_B30	0x20	RW	Bit[7:0]: B30 of 8x8 B control point array for S of sensor 0
0x80206519	SNR0_LENC_S_B31	0x20	RW	Bit[7:0]: B31 of 8x8 B control point array for S of sensor 0
0x8020651A	SNR0_LENC_S_B32	0x20	RW	Bit[7:0]: B32 of 8x8 B control point array for S of sensor 0
0x8020651B	SNR0_LENC_S_B33	0x20	RW	Bit[7:0]: B33 of 8x8 B control point array for S of sensor 0
0x8020651C	SNR0_LENC_S_B34	0x20	RW	Bit[7:0]: B34 of 8x8 B control point array for S of sensor 0
0x8020651D	SNR0_LENC_S_B35	0x20	RW	Bit[7:0]: B35 of 8x8 B control point array for S of sensor 0
0x8020651E	SNR0_LENC_S_B36	0x20	RW	Bit[7:0]: B36 of 8x8 B control point array for S of sensor 0
0x8020651F	SNR0_LENC_S_B37	0x20	RW	Bit[7:0]: B37 of 8x8 B control point array for S of sensor 0
0x80206520	SNR0_LENC_S_B40	0x20	RW	Bit[7:0]: B40 of 8x8 B control point array for S of sensor 0
0x80206521	SNR0_LENC_S_B41	0x20	RW	Bit[7:0]: B41 of 8x8 B control point array for S of sensor 0

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table 4-41 LENC registers (sheet 17 of 46)

address	register name	default value	R/W	description
0x80206522	SNR0_LENC_S_B42	0x20	RW	Bit[7:0]: B42 of 8x8 B control point array for S of sensor 0
0x80206523	SNR0_LENC_S_B43	0x20	RW	Bit[7:0]: B43 of 8x8 B control point array for S of sensor 0
0x80206524	SNR0_LENC_S_B44	0x20	RW	Bit[7:0]: B44 of 8x8 B control point array for S of sensor 0
0x80206525	SNR0_LENC_S_B45	0x20	RW	Bit[7:0]: B45 of 8x8 B control point array for S of sensor 0
0x80206526	SNR0_LENC_S_B46	0x20	RW	Bit[7:0]: B46 of 8x8 B control point array for S of sensor 0
0x80206527	SNR0_LENC_S_B47	0x20	RW	Bit[7:0]: B47 of 8x8 B control point array for S of sensor 0
0x80206528	SNR0_LENC_S_B50	0x20	RW	Bit[7:0]: B50 of 8x8 B control point array for S of sensor 0
0x80206529	SNR0_LENC_S_B51	0x20	RW	Bit[7:0]: B51 of 8x8 B control point array for S of sensor 0
0x8020652A	SNR0_LENC_S_B52	0x20	RW	Bit[7:0]: B52 of 8x8 B control point array for S of sensor 0
0x8020652B	SNR0_LENC_S_B53	0x20	RW	Bit[7:0]: B53 of 8x8 B control point array for S of sensor 0
0x8020652C	SNR0_LENC_S_B54	0x20	RW	Bit[7:0]: B54 of 8x8 B control point array for S of sensor 0
0x8020652D	SNR0_LENC_S_B55	0x20	RW	Bit[7:0]: B55 of 8x8 B control point array for S of sensor 0
0x8020652E	SNR0_LENC_S_B56	0x20	RW	Bit[7:0]: B56 of 8x8 B control point array for S of sensor 0
0x8020652F	SNR0_LENC_S_B57	0x20	RW	Bit[7:0]: B57 of 8x8 B control point array for S of sensor 0
0x80206530	SNR0_LENC_S_B60	0x20	RW	Bit[7:0]: B60 of 8x8 B control point array for S of sensor 0
0x80206531	SNR0_LENC_S_B61	0x20	RW	Bit[7:0]: B61 of 8x8 B control point array for S of sensor 0
0x80206532	SNR0_LENC_S_B62	0x20	RW	Bit[7:0]: B62 of 8x8 B control point array for S of sensor 0
0x80206533	SNR0_LENC_S_B63	0x20	RW	Bit[7:0]: B63 of 8x8 B control point array for S of sensor 0
0x80206534	SNR0_LENC_S_B64	0x20	RW	Bit[7:0]: B64 of 8x8 B control point array for S of sensor 0

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table 4-41 LENC registers (sheet 18 of 46)

address	register name	default value	R/W	description
0x80206535	SNR0_LENC_S_B65	0x20	RW	Bit[7:0]: B65 of 8x8 B control point array for S of sensor 0
0x80206536	SNR0_LENC_S_B66	0x20	RW	Bit[7:0]: B66 of 8x8 B control point array for S of sensor 0
0x80206537	SNR0_LENC_S_B67	0x20	RW	Bit[7:0]: B67 of 8x8 B control point array for S of sensor 0
0x80206538	SNR0_LENC_S_B70	0x20	RW	Bit[7:0]: B70 of 8x8 B control point array for S of sensor 0
0x80206539	SNR0_LENC_S_B71	0x20	RW	Bit[7:0]: B71 of 8x8 B control point array for S of sensor 0
0x8020653A	SNR0_LENC_S_B72	0x20	RW	Bit[7:0]: B72 of 8x8 B control point array for S of sensor 0
0x8020653B	SNR0_LENC_S_B73	0x20	RW	Bit[7:0]: B73 of 8x8 B control point array for S of sensor 0
0x8020653C	SNR0_LENC_S_B74	0x20	RW	Bit[7:0]: B74 of 8x8 B control point array for S of sensor 0
0x8020653D	SNR0_LENC_S_B75	0x20	RW	Bit[7:0]: B75 of 8x8 B control point array for S of sensor 0
0x8020653E	SNR0_LENC_S_B76	0x20	RW	Bit[7:0]: B76 of 8x8 B control point array for S of sensor 0
0x8020653F	SNR0_LENC_S_B77	0x20	RW	Bit[7:0]: B77 of 8x8 B control point array for S of sensor 0
0x80206540	SNR0_LENC_S_R00	0x20	RW	Bit[7:0]: R00 of 8x8 R control point array for S of sensor 0
0x80206541	SNR0_LENC_S_R01	0x20	RW	Bit[7:0]: R01 of 8x8 R control point array for S of sensor 0
0x80206542	SNR0_LENC_S_R02	0x20	RW	Bit[7:0]: R02 of 8x8 R control point array for S of sensor 0
0x80206543	SNR0_LENC_S_R03	0x20	RW	Bit[7:0]: R03 of 8x8 R control point array for S of sensor 0
0x80206544	SNR0_LENC_S_R04	0x20	RW	Bit[7:0]: R04 of 8x8 R control point array for S of sensor 0
0x80206545	SNR0_LENC_S_R05	0x20	RW	Bit[7:0]: R05 of 8x8 R control point array for S of sensor 0
0x80206546	SNR0_LENC_S_R06	0x20	RW	Bit[7:0]: R06 of 8x8 R control point array for S of sensor 0
0x80206547	SNR0_LENC_S_R07	0x20	RW	Bit[7:0]: R07 of 8x8 R control point array for S of sensor 0

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table 4-41 LENC registers (sheet 19 of 46)

address	register name	default value	R/W	description
0x80206548	SNR0_LENC_S_R10	0x20	RW	Bit[7:0]: R10 of 8x8 R control point array for S of sensor 0
0x80206549	SNR0_LENC_S_R11	0x20	RW	Bit[7:0]: R11 of 8x8 R control point array for S of sensor 0
0x8020654A	SNR0_LENC_S_R12	0x20	RW	Bit[7:0]: R12 of 8x8 R control point array for S of sensor 0
0x8020654B	SNR0_LENC_S_R13	0x20	RW	Bit[7:0]: R13 of 8x8 R control point array for S of sensor 0
0x8020654C	SNR0_LENC_S_R14	0x20	RW	Bit[7:0]: R14 of 8x8 R control point array for S of sensor 0
0x8020654D	SNR0_LENC_S_R15	0x20	RW	Bit[7:0]: R15 of 8x8 R control point array for S of sensor 0
0x8020654E	SNR0_LENC_S_R16	0x20	RW	Bit[7:0]: R16 of 8x8 R control point array for S of sensor 0
0x8020654F	SNR0_LENC_S_R17	0x20	RW	Bit[7:0]: R17 of 8x8 R control point array for S of sensor 0
0x80206550	SNR0_LENC_S_R20	0x20	RW	Bit[7:0]: R20 of 8x8 R control point array for S of sensor 0
0x80206551	SNR0_LENC_S_R21	0x20	RW	Bit[7:0]: R21 of 8x8 R control point array for S of sensor 0
0x80206552	SNR0_LENC_S_R22	0x20	RW	Bit[7:0]: R22 of 8x8 R control point array for S of sensor 0
0x80206553	SNR0_LENC_S_R23	0x20	RW	Bit[7:0]: R23 of 8x8 R control point array for S of sensor 0
0x80206554	SNR0_LENC_S_R24	0x20	RW	Bit[7:0]: R24 of 8x8 R control point array for S of sensor 0
0x80206555	SNR0_LENC_S_R25	0x20	RW	Bit[7:0]: R25 of 8x8 R control point array for S of sensor 0
0x80206556	SNR0_LENC_S_R26	0x20	RW	Bit[7:0]: R26 of 8x8 R control point array for S of sensor 0
0x80206557	SNR0_LENC_S_R27	0x20	RW	Bit[7:0]: R27 of 8x8 R control point array for S of sensor 0
0x80206558	SNR0_LENC_S_R30	0x20	RW	Bit[7:0]: R30 of 8x8 R control point array for S of sensor 0
0x80206559	SNR0_LENC_S_R31	0x20	RW	Bit[7:0]: R31 of 8x8 R control point array for S of sensor 0
0x8020655A	SNR0_LENC_S_R32	0x20	RW	Bit[7:0]: R32 of 8x8 R control point array for S of sensor 0

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table 4-41 LENC registers (sheet 20 of 46)

address	register name	default value	R/W	description
0x8020655B	SNR0_LENC_S_R33	0x20	RW	Bit[7:0]: R33 of 8x8 R control point array for S of sensor 0
0x8020655C	SNR0_LENC_S_R34	0x20	RW	Bit[7:0]: R34 of 8x8 R control point array for S of sensor 0
0x8020655D	SNR0_LENC_S_R35	0x20	RW	Bit[7:0]: R35 of 8x8 R control point array for S of sensor 0
0x8020655E	SNR0_LENC_S_R36	0x20	RW	Bit[7:0]: R36 of 8x8 R control point array for S of sensor 0
0x8020655F	SNR0_LENC_S_R37	0x20	RW	Bit[7:0]: R37 of 8x8 R control point array for S of sensor 0
0x80206560	SNR0_LENC_S_R40	0x20	RW	Bit[7:0]: R40 of 8x8 R control point array for S of sensor 0
0x80206561	SNR0_LENC_S_R41	0x20	RW	Bit[7:0]: R41 of 8x8 R control point array for S of sensor 0
0x80206562	SNR0_LENC_S_R42	0x20	RW	Bit[7:0]: R42 of 8x8 R control point array for S of sensor 0
0x80206563	SNR0_LENC_S_R43	0x20	RW	Bit[7:0]: R43 of 8x8 R control point array for S of sensor 0
0x80206564	SNR0_LENC_S_R44	0x20	RW	Bit[7:0]: R44 of 8x8 R control point array for S of sensor 0
0x80206565	SNR0_LENC_S_R45	0x20	RW	Bit[7:0]: R45 of 8x8 R control point array for S of sensor 0
0x80206566	SNR0_LENC_S_R46	0x20	RW	Bit[7:0]: R46 of 8x8 R control point array for S of sensor 0
0x80206567	SNR0_LENC_S_R47	0x20	RW	Bit[7:0]: R47 of 8x8 R control point array for S of sensor 0
0x80206568	SNR0_LENC_S_R50	0x20	RW	Bit[7:0]: R50 of 8x8 R control point array for S of sensor 0
0x80206569	SNR0_LENC_S_R51	0x20	RW	Bit[7:0]: R51 of 8x8 R control point array for S of sensor 0
0x8020656A	SNR0_LENC_S_R52	0x20	RW	Bit[7:0]: R52 of 8x8 R control point array for S of sensor 0
0x8020656B	SNR0_LENC_S_R53	0x20	RW	Bit[7:0]: R53 of 8x8 R control point array for S of sensor 0
0x8020656C	SNR0_LENC_S_R54	0x20	RW	Bit[7:0]: R54 of 8x8 R control point array for S of sensor 0
0x8020656D	SNR0_LENC_S_R55	0x20	RW	Bit[7:0]: R55 of 8x8 R control point array for S of sensor 0

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table 4-41 LENC registers (sheet 21 of 46)

address	register name	default value	R/W	description
0x8020656E	SNR0_LENC_S_R56	0x20	RW	Bit[7:0]: R56 of 8x8 R control point array for S of sensor 0
0x8020656F	SNR0_LENC_S_R57	0x20	RW	Bit[7:0]: R57 of 8x8 R control point array for S of sensor 0
0x80206570	SNR0_LENC_S_R60	0x20	RW	Bit[7:0]: R60 of 8x8 R control point array for S of sensor 0
0x80206571	SNR0_LENC_S_R61	0x20	RW	Bit[7:0]: R61 of 8x8 R control point array for S of sensor 0
0x80206572	SNR0_LENC_S_R62	0x20	RW	Bit[7:0]: R62 of 8x8 R control point array for S of sensor 0
0x80206573	SNR0_LENC_S_R63	0x20	RW	Bit[7:0]: R63 of 8x8 R control point array for S of sensor 0
0x80206574	SNR0_LENC_S_R64	0x20	RW	Bit[7:0]: R64 of 8x8 R control point array for S of sensor 0
0x80206575	SNR0_LENC_S_R65	0x20	RW	Bit[7:0]: R65 of 8x8 R control point array for S of sensor 0
0x80206576	SNR0_LENC_S_R66	0x20	RW	Bit[7:0]: R66 of 8x8 R control point array for S of sensor 0
0x80206577	SNR0_LENC_S_R67	0x20	RW	Bit[7:0]: R67 of 8x8 R control point array for S of sensor 0
0x80206578	SNR0_LENC_S_R70	0x20	RW	Bit[7:0]: R70 of 8x8 R control point array for S of sensor 0
0x80206579	SNR0_LENC_S_R71	0x20	RW	Bit[7:0]: R71 of 8x8 R control point array for S of sensor 0
0x8020657A	SNR0_LENC_S_R72	0x20	RW	Bit[7:0]: R72 of 8x8 R control point array for S of sensor 0
0x8020657B	SNR0_LENC_S_R73	0x20	RW	Bit[7:0]: R73 of 8x8 R control point array for S of sensor 0
0x8020657C	SNR0_LENC_S_R74	0x20	RW	Bit[7:0]: R74 of 8x8 R control point array for S of sensor 0
0x8020657D	SNR0_LENC_S_R75	0x20	RW	Bit[7:0]: R75 of 8x8 R control point array for S of sensor 0
0x8020657E	SNR0_LENC_S_R76	0x20	RW	Bit[7:0]: R76 of 8x8 R control point array for S of sensor 0
0x8020657F	SNR0_LENC_S_R77	0x20	RW	Bit[7:0]: R77 of 8x8 R control point array for S of sensor 0
0x80206580	SNR1_LENC_LV_G00	0x00	RW	Bit[7:0]: G00 of 8x8 G control point array for L/VS of sensor 1

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table 4-41 LENC registers (sheet 22 of 46)

address	register name	default value	R/W	description
0x80206581	SNR1_LENC_LV_G01	0x00	RW	Bit[7:0]: G01 of 8x8 G control point array for L/VS of sensor 1
0x80206582	SNR1_LENC_LV_G02	0x00	RW	Bit[7:0]: G02 of 8x8 G control point array for L/VS of sensor 1
0x80206583	SNR1_LENC_LV_G03	0x00	RW	Bit[7:0]: G03 of 8x8 G control point array for L/VS of sensor 1
0x80206584	SNR1_LENC_LV_G04	0x00	RW	Bit[7:0]: G04 of 8x8 G control point array for L/VS of sensor 1
0x80206585	SNR1_LENC_LV_G05	0x00	RW	Bit[7:0]: G05 of 8x8 G control point array for L/VS of sensor 1
0x80206586	SNR1_LENC_LV_G06	0x00	RW	Bit[7:0]: G06 of 8x8 G control point array for L/VS of sensor 1
0x80206587	SNR1_LENC_LV_G07	0x00	RW	Bit[7:0]: G07 of 8x8 G control point array for L/VS of sensor 1
0x80206588	SNR1_LENC_LV_G10	0x00	RW	Bit[7:0]: G10 of 8x8 G control point array for L/VS of sensor 1
0x80206589	SNR1_LENC_LV_G11	0x00	RW	Bit[7:0]: G11 of 8x8 G control point array for L/VS of sensor 1
0x8020658A	SNR1_LENC_LV_G12	0x00	RW	Bit[7:0]: G12 of 8x8 G control point array for L/VS of sensor 1
0x8020658B	SNR1_LENC_LV_G13	0x00	RW	Bit[7:0]: G13 of 8x8 G control point array for L/VS of sensor 1
0x8020658C	SNR1_LENC_LV_G14	0x00	RW	Bit[7:0]: G14 of 8x8 G control point array for L/VS of sensor 1
0x8020658D	SNR1_LENC_LV_G15	0x00	RW	Bit[7:0]: G15 of 8x8 G control point array for L/VS of sensor 1
0x8020658E	SNR1_LENC_LV_G16	0x00	RW	Bit[7:0]: G16 of 8x8 G control point array for L/VS of sensor 1
0x8020658F	SNR1_LENC_LV_G17	0x00	RW	Bit[7:0]: G17 of 8x8 G control point array for L/VS of sensor 1
0x80206590	SNR1_LENC_LV_G20	0x00	RW	Bit[7:0]: G20 of 8x8 G control point array for L/VS of sensor 1
0x80206591	SNR1_LENC_LV_G21	0x00	RW	Bit[7:0]: G21 of 8x8 G control point array for L/VS of sensor 1
0x80206592	SNR1_LENC_LV_G22	0x00	RW	Bit[7:0]: G22 of 8x8 G control point array for L/VS of sensor 1
0x80206593	SNR1_LENC_LV_G23	0x00	RW	Bit[7:0]: G23 of 8x8 G control point array for L/VS of sensor 1

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table 4-41 LENC registers (sheet 23 of 46)

address	register name	default value	R/W	description
0x80206594	SNR1_LENC_LV_G24	0x00	RW	Bit[7:0]: G24 of 8x8 G control point array for L/VS of sensor 1
0x80206595	SNR1_LENC_LV_G25	0x00	RW	Bit[7:0]: G25 of 8x8 G control point array for L/VS of sensor 1
0x80206596	SNR1_LENC_LV_G26	0x00	RW	Bit[7:0]: G26 of 8x8 G control point array for L/VS of sensor 1
0x80206597	SNR1_LENC_LV_G27	0x00	RW	Bit[7:0]: G27 of 8x8 G control point array for L/VS of sensor 1
0x80206598	SNR1_LENC_LV_G30	0x00	RW	Bit[7:0]: G30 of 8x8 G control point array for L/VS of sensor 1
0x80206599	SNR1_LENC_LV_G31	0x00	RW	Bit[7:0]: G31 of 8x8 G control point array for L/VS of sensor 1
0x8020659A	SNR1_LENC_LV_G32	0x00	RW	Bit[7:0]: G32 of 8x8 G control point array for L/VS of sensor 1
0x8020659B	SNR1_LENC_LV_G33	0x00	RW	Bit[7:0]: G33 of 8x8 G control point array for L/VS of sensor 1
0x8020659C	SNR1_LENC_LV_G34	0x00	RW	Bit[7:0]: G34 of 8x8 G control point array for L/VS of sensor 1
0x8020659D	SNR1_LENC_LV_G35	0x00	RW	Bit[7:0]: G35 of 8x8 G control point array for L/VS of sensor 1
0x8020659E	SNR1_LENC_LV_G36	0x00	RW	Bit[7:0]: G36 of 8x8 G control point array for L/VS of sensor 1
0x8020659F	SNR1_LENC_LV_G37	0x00	RW	Bit[7:0]: G37 of 8x8 G control point array for L/VS of sensor 1
0x802065A0	SNR1_LENC_LV_G40	0x00	RW	Bit[7:0]: G40 of 8x8 G control point array for L/VS of sensor 1
0x802065A1	SNR1_LENC_LV_G41	0x00	RW	Bit[7:0]: G41 of 8x8 G control point array for L/VS of sensor 1
0x802065A2	SNR1_LENC_LV_G42	0x00	RW	Bit[7:0]: G42 of 8x8 G control point array for L/VS of sensor 1
0x802065A3	SNR1_LENC_LV_G43	0x00	RW	Bit[7:0]: G43 of 8x8 G control point array for L/VS of sensor 1
0x802065A4	SNR1_LENC_LV_G44	0x00	RW	Bit[7:0]: G44 of 8x8 G control point array for L/VS of sensor 1
0x802065A5	SNR1_LENC_LV_G45	0x00	RW	Bit[7:0]: G45 of 8x8 G control point array for L/VS of sensor 1
0x802065A6	SNR1_LENC_LV_G46	0x00	RW	Bit[7:0]: G46 of 8x8 G control point array for L/VS of sensor 1

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table 4-41 LENC registers (sheet 24 of 46)

address	register name	default value	R/W	description
0x802065A7	SNR1_LENC_LV_G47	0x00	RW	Bit[7:0]: G47 of 8x8 G control point array for L/VS of sensor 1
0x802065A8	SNR1_LENC_LV_G50	0x00	RW	Bit[7:0]: G50 of 8x8 G control point array for L/VS of sensor 1
0x802065A9	SNR1_LENC_LV_G51	0x00	RW	Bit[7:0]: G51 of 8x8 G control point array for L/VS of sensor 1
0x802065AA	SNR1_LENC_LV_G52	0x00	RW	Bit[7:0]: G52 of 8x8 G control point array for L/VS of sensor 1
0x802065AB	SNR1_LENC_LV_G53	0x00	RW	Bit[7:0]: G53 of 8x8 G control point array for L/VS of sensor 1
0x802065AC	SNR1_LENC_LV_G54	0x00	RW	Bit[7:0]: G54 of 8x8 G control point array for L/VS of sensor 1
0x802065AD	SNR1_LENC_LV_G55	0x00	RW	Bit[7:0]: G55 of 8x8 G control point array for L/VS of sensor 1
0x802065AE	SNR1_LENC_LV_G56	0x00	RW	Bit[7:0]: G56 of 8x8 G control point array for L/VS of sensor 1
0x802065AF	SNR1_LENC_LV_G57	0x00	RW	Bit[7:0]: G57 of 8x8 G control point array for L/VS of sensor 1
0x802065B0	SNR1_LENC_LV_G60	0x00	RW	Bit[7:0]: G60 of 8x8 G control point array for L/VS of sensor 1
0x802065B1	SNR1_LENC_LV_G61	0x00	RW	Bit[7:0]: G61 of 8x8 G control point array for L/VS of sensor 1
0x802065B2	SNR1_LENC_LV_G62	0x00	RW	Bit[7:0]: G62 of 8x8 G control point array for L/VS of sensor 1
0x802065B3	SNR1_LENC_LV_G63	0x00	RW	Bit[7:0]: G63 of 8x8 G control point array for L/VS of sensor 1
0x802065B4	SNR1_LENC_LV_G64	0x00	RW	Bit[7:0]: G64 of 8x8 G control point array for L/VS of sensor 1
0x802065B5	SNR1_LENC_LV_G65	0x00	RW	Bit[7:0]: G65 of 8x8 G control point array for L/VS of sensor 1
0x802065B6	SNR1_LENC_LV_G66	0x00	RW	Bit[7:0]: G66 of 8x8 G control point array for L/VS of sensor 1
0x802065B7	SNR1_LENC_LV_G67	0x00	RW	Bit[7:0]: G67 of 8x8 G control point array for L/VS of sensor 1
0x802065B8	SNR1_LENC_LV_G70	0x00	RW	Bit[7:0]: G70 of 8x8 G control point array for L/VS of sensor 1
0x802065B9	SNR1_LENC_LV_G71	0x00	RW	Bit[7:0]: G71 of 8x8 G control point array for L/VS of sensor 1

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table 4-41 LENC registers (sheet 25 of 46)

address	register name	default value	R/W	description
0x802065BA	SNR1_LENC_LV_G72	0x00	RW	Bit[7:0]: G72 of 8x8 G control point array for L/VS of sensor 1
0x802065BB	SNR1_LENC_LV_G73	0x00	RW	Bit[7:0]: G73 of 8x8 G control point array for L/VS of sensor 1
0x802065BC	SNR1_LENC_LV_G74	0x00	RW	Bit[7:0]: G74 of 8x8 G control point array for L/VS of sensor 1
0x802065BD	SNR1_LENC_LV_G75	0x00	RW	Bit[7:0]: G75 of 8x8 G control point array for L/VS of sensor 1
0x802065BE	SNR1_LENC_LV_G76	0x00	RW	Bit[7:0]: G76 of 8x8 G control point array for L/VS of sensor 1
0x802065BF	SNR1_LENC_LV_G77	0x00	RW	Bit[7:0]: G77 of 8x8 G control point array for L/VS of sensor 1
0x802065C0	SNR1_LENC_LV_B00	0x20	RW	Bit[7:0]: B00 of 8x8 B control point array for L/VS of sensor 1
0x802065C1	SNR1_LENC_LV_B01	0x20	RW	Bit[7:0]: B01 of 8x8 B control point array for L/VS of sensor 1
0x802065C2	SNR1_LENC_LV_B02	0x20	RW	Bit[7:0]: B02 of 8x8 B control point array for L/VS of sensor 1
0x802065C3	SNR1_LENC_LV_B03	0x20	RW	Bit[7:0]: B03 of 8x8 B control point array for L/VS of sensor 1
0x802065C4	SNR1_LENC_LV_B04	0x20	RW	Bit[7:0]: B04 of 8x8 B control point array for L/VS of sensor 1
0x802065C5	SNR1_LENC_LV_B05	0x20	RW	Bit[7:0]: B05 of 8x8 B control point array for L/VS of sensor 1
0x802065C6	SNR1_LENC_LV_B06	0x20	RW	Bit[7:0]: B06 of 8x8 B control point array for L/VS of sensor 1
0x802065C7	SNR1_LENC_LV_B07	0x20	RW	Bit[7:0]: B07 of 8x8 B control point array for L/VS of sensor 1
0x802065C8	SNR1_LENC_LV_B10	0x20	RW	Bit[7:0]: B10 of 8x8 B control point array for L/VS of sensor 1
0x802065C9	SNR1_LENC_LV_B11	0x20	RW	Bit[7:0]: B11 of 8x8 B control point array for L/VS of sensor 1
0x802065CA	SNR1_LENC_LV_B12	0x20	RW	Bit[7:0]: B12 of 8x8 B control point array for L/VS of sensor 1
0x802065CB	SNR1_LENC_LV_B13	0x20	RW	Bit[7:0]: B13 of 8x8 B control point array for L/VS of sensor 1
0x802065CC	SNR1_LENC_LV_B14	0x20	RW	Bit[7:0]: B14 of 8x8 B control point array for L/VS of sensor 1

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table 4-41 LENC registers (sheet 26 of 46)

address	register name	default value	R/W	description
0x802065CD	SNR1_LENC_LV_B15	0x20	RW	Bit[7:0]: B15 of 8x8 B control point array for L/VS of sensor 1
0x802065CE	SNR1_LENC_LV_B16	0x20	RW	Bit[7:0]: B16 of 8x8 B control point array for L/VS of sensor 1
0x802065CF	SNR1_LENC_LV_B17	0x20	RW	Bit[7:0]: B17 of 8x8 B control point array for L/VS of sensor 1
0x802065D0	SNR1_LENC_LV_B20	0x20	RW	Bit[7:0]: B20 of 8x8 B control point array for L/VS of sensor 1
0x802065D1	SNR1_LENC_LV_B21	0x20	RW	Bit[7:0]: B21 of 8x8 B control point array for L/VS of sensor 1
0x802065D2	SNR1_LENC_LV_B22	0x20	RW	Bit[7:0]: B22 of 8x8 B control point array for L/VS of sensor 1
0x802065D3	SNR1_LENC_LV_B23	0x20	RW	Bit[7:0]: B23 of 8x8 B control point array for L/VS of sensor 1
0x802065D4	SNR1_LENC_LV_B24	0x20	RW	Bit[7:0]: B24 of 8x8 B control point array for L/VS of sensor 1
0x802065D5	SNR1_LENC_LV_B25	0x20	RW	Bit[7:0]: B25 of 8x8 B control point array for L/VS of sensor 1
0x802065D6	SNR1_LENC_LV_B26	0x20	RW	Bit[7:0]: B26 of 8x8 B control point array for L/VS of sensor 1
0x802065D7	SNR1_LENC_LV_B27	0x20	RW	Bit[7:0]: B27 of 8x8 B control point array for L/VS of sensor 1
0x802065D8	SNR1_LENC_LV_B30	0x20	RW	Bit[7:0]: B30 of 8x8 B control point array for L/VS of sensor 1
0x802065D9	SNR1_LENC_LV_B31	0x20	RW	Bit[7:0]: B31 of 8x8 B control point array for L/VS of sensor 1
0x802065DA	SNR1_LENC_LV_B32	0x20	RW	Bit[7:0]: B32 of 8x8 B control point array for L/VS of sensor 1
0x802065DB	SNR1_LENC_LV_B33	0x20	RW	Bit[7:0]: B33 of 8x8 B control point array for L/VS of sensor 1
0x802065DC	SNR1_LENC_LV_B34	0x20	RW	Bit[7:0]: B34 of 8x8 B control point array for L/VS of sensor 1
0x802065DD	SNR1_LENC_LV_B35	0x20	RW	Bit[7:0]: B35 of 8x8 B control point array for L/VS of sensor 1
0x802065DE	SNR1_LENC_LV_B36	0x20	RW	Bit[7:0]: B36 of 8x8 B control point array for L/VS of sensor 1
0x802065DF	SNR1_LENC_LV_B37	0x20	RW	Bit[7:0]: B37 of 8x8 B control point array for L/VS of sensor 1

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table 4-41 LENC registers (sheet 27 of 46)

address	register name	default value	R/W	description
0x802065E0	SNR1_LENC_LV_B40	0x20	RW	Bit[7:0]: B40 of 8x8 B control point array for L/VS of sensor 1
0x802065E1	SNR1_LENC_LV_B41	0x20	RW	Bit[7:0]: B41 of 8x8 B control point array for L/VS of sensor 1
0x802065E2	SNR1_LENC_LV_B42	0x20	RW	Bit[7:0]: B42 of 8x8 B control point array for L/VS of sensor 1
0x802065E3	SNR1_LENC_LV_B43	0x20	RW	Bit[7:0]: B43 of 8x8 B control point array for L/VS of sensor 1
0x802065E4	SNR1_LENC_LV_B44	0x20	RW	Bit[7:0]: B44 of 8x8 B control point array for L/VS of sensor 1
0x802065E5	SNR1_LENC_LV_B45	0x20	RW	Bit[7:0]: B45 of 8x8 B control point array for L/VS of sensor 1
0x802065E6	SNR1_LENC_LV_B46	0x20	RW	Bit[7:0]: B46 of 8x8 B control point array for L/VS of sensor 1
0x802065E7	SNR1_LENC_LV_B47	0x20	RW	Bit[7:0]: B47 of 8x8 B control point array for L/VS of sensor 1
0x802065E8	SNR1_LENC_LV_B50	0x20	RW	Bit[7:0]: B50 of 8x8 B control point array for L/VS of sensor 1
0x802065E9	SNR1_LENC_LV_B51	0x20	RW	Bit[7:0]: B51 of 8x8 B control point array for L/VS of sensor 1
0x802065EA	SNR1_LENC_LV_B52	0x20	RW	Bit[7:0]: B52 of 8x8 B control point array for L/VS of sensor 1
0x802065EB	SNR1_LENC_LV_B53	0x20	RW	Bit[7:0]: B53 of 8x8 B control point array for L/VS of sensor 1
0x802065EC	SNR1_LENC_LV_B54	0x20	RW	Bit[7:0]: B54 of 8x8 B control point array for L/VS of sensor 1
0x802065ED	SNR1_LENC_LV_B55	0x20	RW	Bit[7:0]: B55 of 8x8 B control point array for L/VS of sensor 1
0x802065EE	SNR1_LENC_LV_B56	0x20	RW	Bit[7:0]: B56 of 8x8 B control point array for L/VS of sensor 1
0x802065EF	SNR1_LENC_LV_B57	0x20	RW	Bit[7:0]: B57 of 8x8 B control point array for L/VS of sensor 1
0x802065F0	SNR1_LENC_LV_B60	0x20	RW	Bit[7:0]: B60 of 8x8 B control point array for L/VS of sensor 1
0x802065F1	SNR1_LENC_LV_B61	0x20	RW	Bit[7:0]: B61 of 8x8 B control point array for L/VS of sensor 1
0x802065F2	SNR1_LENC_LV_B62	0x20	RW	Bit[7:0]: B62 of 8x8 B control point array for L/VS of sensor 1

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table 4-41 LENC registers (sheet 28 of 46)

address	register name	default value	R/W	description
0x802065F3	SNR1_LENC_LV_B63	0x20	RW	Bit[7:0]: B63 of 8x8 B control point array for L/VS of sensor 1
0x802065F4	SNR1_LENC_LV_B64	0x20	RW	Bit[7:0]: B64 of 8x8 B control point array for L/VS of sensor 1
0x802065F5	SNR1_LENC_LV_B65	0x20	RW	Bit[7:0]: B65 of 8x8 B control point array for L/VS of sensor 1
0x802065F6	SNR1_LENC_LV_B66	0x20	RW	Bit[7:0]: B66 of 8x8 B control point array for L/VS of sensor 1
0x802065F7	SNR1_LENC_LV_B67	0x20	RW	Bit[7:0]: B67 of 8x8 B control point array for L/VS of sensor 1
0x802065F8	SNR1_LENC_LV_B70	0x20	RW	Bit[7:0]: B70 of 8x8 B control point array for L/VS of sensor 1
0x802065F9	SNR1_LENC_LV_B71	0x20	RW	Bit[7:0]: B71 of 8x8 B control point array for L/VS of sensor 1
0x802065FA	SNR1_LENC_LV_B72	0x20	RW	Bit[7:0]: B72 of 8x8 B control point array for L/VS of sensor 1
0x802065FB	SNR1_LENC_LV_B73	0x20	RW	Bit[7:0]: B73 of 8x8 B control point array for L/VS of sensor 1
0x802065FC	SNR1_LENC_LV_B74	0x20	RW	Bit[7:0]: B74 of 8x8 B control point array for L/VS of sensor 1
0x802065FD	SNR1_LENC_LV_B75	0x20	RW	Bit[7:0]: B75 of 8x8 B control point array for L/VS of sensor 1
0x802065FE	SNR1_LENC_LV_B76	0x20	RW	Bit[7:0]: B76 of 8x8 B control point array for L/VS of sensor 1
0x802065FF	SNR1_LENC_LV_B77	0x20	RW	Bit[7:0]: B77 of 8x8 B control point array for L/VS of sensor 1
0x80206600	SNR1_LENC_LV_R00	0x20	RW	Bit[7:0]: R00 of 8x8 R control point array for L/VS of sensor 1
0x80206601	SNR1_LENC_LV_R01	0x20	RW	Bit[7:0]: R01 of 8x8 R control point array for L/VS of sensor 1
0x80206602	SNR1_LENC_LV_R02	0x20	RW	Bit[7:0]: R02 of 8x8 R control point array for L/VS of sensor 1
0x80206603	SNR1_LENC_LV_R03	0x20	RW	Bit[7:0]: R03 of 8x8 R control point array for L/VS of sensor 1
0x80206604	SNR1_LENC_LV_R04	0x20	RW	Bit[7:0]: R04 of 8x8 R control point array for L/VS of sensor 1
0x80206605	SNR1_LENC_LV_R05	0x20	RW	Bit[7:0]: R05 of 8x8 R control point array for L/VS of sensor 1

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table 4-41 LENC registers (sheet 29 of 46)

address	register name	default value	R/W	description
0x80206606	SNR1_LENC_LV_R06	0x20	RW	Bit[7:0]: R06 of 8x8 R control point array for L/VS of sensor 1
0x80206607	SNR1_LENC_LV_R07	0x20	RW	Bit[7:0]: R07 of 8x8 R control point array for L/VS of sensor 1
0x80206608	SNR1_LENC_LV_R10	0x20	RW	Bit[7:0]: R10 of 8x8 R control point array for L/VS of sensor 1
0x80206609	SNR1_LENC_LV_R11	0x20	RW	Bit[7:0]: R11 of 8x8 R control point array for L/VS of sensor 1
0x8020660A	SNR1_LENC_LV_R12	0x20	RW	Bit[7:0]: R12 of 8x8 R control point array for L/VS of sensor 1
0x8020660B	SNR1_LENC_LV_R13	0x20	RW	Bit[7:0]: R13 of 8x8 R control point array for L/VS of sensor 1
0x8020660C	SNR1_LENC_LV_R14	0x20	RW	Bit[7:0]: R14 of 8x8 R control point array for L/VS of sensor 1
0x8020660D	SNR1_LENC_LV_R15	0x20	RW	Bit[7:0]: R15 of 8x8 R control point array for L/VS of sensor 1
0x8020660E	SNR1_LENC_LV_R16	0x20	RW	Bit[7:0]: R16 of 8x8 R control point array for L/VS of sensor 1
0x8020660F	SNR1_LENC_LV_R17	0x20	RW	Bit[7:0]: R17 of 8x8 R control point array for L/VS of sensor 1
0x80206610	SNR1_LENC_LV_R20	0x20	RW	Bit[7:0]: R20 of 8x8 R control point array for L/VS of sensor 1
0x80206611	SNR1_LENC_LV_R21	0x20	RW	Bit[7:0]: R21 of 8x8 R control point array for L/VS of sensor 1
0x80206612	SNR1_LENC_LV_R22	0x20	RW	Bit[7:0]: R22 of 8x8 R control point array for L/VS of sensor 1
0x80206613	SNR1_LENC_LV_R23	0x20	RW	Bit[7:0]: R23 of 8x8 R control point array for L/VS of sensor 1
0x80206614	SNR1_LENC_LV_R24	0x20	RW	Bit[7:0]: R24 of 8x8 R control point array for L/VS of sensor 1
0x80206615	SNR1_LENC_LV_R25	0x20	RW	Bit[7:0]: R25 of 8x8 R control point array for L/VS of sensor 1
0x80206616	SNR1_LENC_LV_R26	0x20	RW	Bit[7:0]: R26 of 8x8 R control point array for L/VS of sensor 1
0x80206617	SNR1_LENC_LV_R27	0x20	RW	Bit[7:0]: R27 of 8x8 R control point array for L/VS of sensor 1
0x80206618	SNR1_LENC_LV_R30	0x20	RW	Bit[7:0]: R30 of 8x8 R control point array for L/VS of sensor 1

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table 4-41 LENC registers (sheet 30 of 46)

address	register name	default value	R/W	description
0x80206619	SNR1_LENC_LV_R31	0x20	RW	Bit[7:0]: R31 of 8x8 R control point array for L/VS of sensor 1
0x8020661A	SNR1_LENC_LV_R32	0x20	RW	Bit[7:0]: R32 of 8x8 R control point array for L/VS of sensor 1
0x8020661B	SNR1_LENC_LV_R33	0x20	RW	Bit[7:0]: R33 of 8x8 R control point array for L/VS of sensor 1
0x8020661C	SNR1_LENC_LV_R34	0x20	RW	Bit[7:0]: R34 of 8x8 R control point array for L/VS of sensor 1
0x8020661D	SNR1_LENC_LV_R35	0x20	RW	Bit[7:0]: R35 of 8x8 R control point array for L/VS of sensor 1
0x8020661E	SNR1_LENC_LV_R36	0x20	RW	Bit[7:0]: R36 of 8x8 R control point array for L/VS of sensor 1
0x8020661F	SNR1_LENC_LV_R37	0x20	RW	Bit[7:0]: R37 of 8x8 R control point array for L/VS of sensor 1
0x80206620	SNR1_LENC_LV_R40	0x20	RW	Bit[7:0]: R40 of 8x8 R control point array for L/VS of sensor 1
0x80206621	SNR1_LENC_LV_R41	0x20	RW	Bit[7:0]: R41 of 8x8 R control point array for L/VS of sensor 1
0x80206622	SNR1_LENC_LV_R42	0x20	RW	Bit[7:0]: R42 of 8x8 R control point array for L/VS of sensor 1
0x80206623	SNR1_LENC_LV_R43	0x20	RW	Bit[7:0]: R43 of 8x8 R control point array for L/VS of sensor 1
0x80206624	SNR1_LENC_LV_R44	0x20	RW	Bit[7:0]: R44 of 8x8 R control point array for L/VS of sensor 1
0x80206625	SNR1_LENC_LV_R45	0x20	RW	Bit[7:0]: R45 of 8x8 R control point array for L/VS of sensor 1
0x80206626	SNR1_LENC_LV_R46	0x20	RW	Bit[7:0]: R46 of 8x8 R control point array for L/VS of sensor 1
0x80206627	SNR1_LENC_LV_R47	0x20	RW	Bit[7:0]: R47 of 8x8 R control point array for L/VS of sensor 1
0x80206628	SNR1_LENC_LV_R50	0x20	RW	Bit[7:0]: R50 of 8x8 R control point array for L/VS of sensor 1
0x80206629	SNR1_LENC_LV_R51	0x20	RW	Bit[7:0]: R51 of 8x8 R control point array for L/VS of sensor 1
0x8020662A	SNR1_LENC_LV_R52	0x20	RW	Bit[7:0]: R52 of 8x8 R control point array for L/VS of sensor 1
0x8020662B	SNR1_LENC_LV_R53	0x20	RW	Bit[7:0]: R53 of 8x8 R control point array for L/VS of sensor 1

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table 4-41 LENC registers (sheet 31 of 46)

address	register name	default value	R/W	description
0x8020662C	SNR1_LENC_LV_R54	0x20	RW	Bit[7:0]: R54 of 8x8 R control point array for L/VS of sensor 1
0x8020662D	SNR1_LENC_LV_R55	0x20	RW	Bit[7:0]: R55 of 8x8 R control point array for L/VS of sensor 1
0x8020662E	SNR1_LENC_LV_R56	0x20	RW	Bit[7:0]: R56 of 8x8 R control point array for L/VS of sensor 1
0x8020662F	SNR1_LENC_LV_R57	0x20	RW	Bit[7:0]: R57 of 8x8 R control point array for L/VS of sensor 1
0x80206630	SNR1_LENC_LV_R60	0x20	RW	Bit[7:0]: R60 of 8x8 R control point array for L/VS of sensor 1
0x80206631	SNR1_LENC_LV_R61	0x20	RW	Bit[7:0]: R61 of 8x8 R control point array for L/VS of sensor 1
0x80206632	SNR1_LENC_LV_R62	0x20	RW	Bit[7:0]: R62 of 8x8 R control point array for L/VS of sensor 1
0x80206633	SNR1_LENC_LV_R63	0x20	RW	Bit[7:0]: R63 of 8x8 R control point array for L/VS of sensor 1
0x80206634	SNR1_LENC_LV_R64	0x20	RW	Bit[7:0]: R64 of 8x8 R control point array for L/VS of sensor 1
0x80206635	SNR1_LENC_LV_R65	0x20	RW	Bit[7:0]: R65 of 8x8 R control point array for L/VS of sensor 1
0x80206636	SNR1_LENC_LV_R66	0x20	RW	Bit[7:0]: R66 of 8x8 R control point array for L/VS of sensor 1
0x80206637	SNR1_LENC_LV_R67	0x20	RW	Bit[7:0]: R67 of 8x8 R control point array for L/VS of sensor 1
0x80206638	SNR1_LENC_LV_R70	0x20	RW	Bit[7:0]: R70 of 8x8 R control point array for L/VS of sensor 1
0x80206639	SNR1_LENC_LV_R71	0x20	RW	Bit[7:0]: R71 of 8x8 R control point array for L/VS of sensor 1
0x8020663A	SNR1_LENC_LV_R72	0x20	RW	Bit[7:0]: R72 of 8x8 R control point array for L/VS of sensor 1
0x8020663B	SNR1_LENC_LV_R73	0x20	RW	Bit[7:0]: R73 of 8x8 R control point array for L/VS of sensor 1
0x8020663C	SNR1_LENC_LV_R74	0x20	RW	Bit[7:0]: R74 of 8x8 R control point array for L/VS of sensor 1
0x8020663D	SNR1_LENC_LV_R75	0x20	RW	Bit[7:0]: R75 of 8x8 R control point array for L/VS of sensor 1
0x8020663E	SNR1_LENC_LV_R76	0x20	RW	Bit[7:0]: R76 of 8x8 R control point array for L/VS of sensor 1

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table 4-41 LENC registers (sheet 32 of 46)

address	register name	default value	R/W	description
0x8020663F	SNR1_LENC_LV_R77	0x20	RW	Bit[7:0]: R77 of 8x8 R control point array for L/VS of sensor 1
0x80206640	SNR1_LENC_S_G00	0x00	RW	Bit[7:0]: G00 of 8x8 G control point array for S of sensor 1
0x80206641	SNR1_LENC_S_G01	0x00	RW	Bit[7:0]: G01 of 8x8 G control point array for S of sensor 1
0x80206642	SNR1_LENC_S_G02	0x00	RW	Bit[7:0]: G02 of 8x8 G control point array for S of sensor 1
0x80206643	SNR1_LENC_S_G03	0x00	RW	Bit[7:0]: G03 of 8x8 G control point array for S of sensor 1
0x80206644	SNR1_LENC_S_G04	0x00	RW	Bit[7:0]: G04 of 8x8 G control point array for S of sensor 1
0x80206645	SNR1_LENC_S_G05	0x00	RW	Bit[7:0]: G05 of 8x8 G control point array for S of sensor 1
0x80206646	SNR1_LENC_S_G06	0x00	RW	Bit[7:0]: G06 of 8x8 G control point array for S of sensor 1
0x80206647	SNR1_LENC_S_G07	0x00	RW	Bit[7:0]: G07 of 8x8 G control point array for S of sensor 1
0x80206648	SNR1_LENC_S_G10	0x00	RW	Bit[7:0]: G10 of 8x8 G control point array for S of sensor 1
0x80206649	SNR1_LENC_S_G11	0x00	RW	Bit[7:0]: G11 of 8x8 G control point array for S of sensor 1
0x8020664A	SNR1_LENC_S_G12	0x00	RW	Bit[7:0]: G12 of 8x8 G control point array for S of sensor 1
0x8020664B	SNR1_LENC_S_G13	0x00	RW	Bit[7:0]: G13 of 8x8 G control point array for S of sensor 1
0x8020664C	SNR1_LENC_S_G14	0x00	RW	Bit[7:0]: G14 of 8x8 G control point array for S of sensor 1
0x8020664D	SNR1_LENC_S_G15	0x00	RW	Bit[7:0]: G15 of 8x8 G control point array for S of sensor 1
0x8020664E	SNR1_LENC_S_G16	0x00	RW	Bit[7:0]: G16 of 8x8 G control point array for S of sensor 1
0x8020664F	SNR1_LENC_S_G17	0x00	RW	Bit[7:0]: G17 of 8x8 G control point array for S of sensor 1
0x80206650	SNR1_LENC_S_G20	0x00	RW	Bit[7:0]: G20 of 8x8 G control point array for S of sensor 1
0x80206651	SNR1_LENC_S_G21	0x00	RW	Bit[7:0]: G21 of 8x8 G control point array for S of sensor 1

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table 4-41 LENC registers (sheet 33 of 46)

address	register name	default value	R/W	description
0x80206652	SNR1_LENC_S_G22	0x00	RW	Bit[7:0]: G22 of 8x8 G control point array for S of sensor 1
0x80206653	SNR1_LENC_S_G23	0x00	RW	Bit[7:0]: G23 of 8x8 G control point array for S of sensor 1
0x80206654	SNR1_LENC_S_G24	0x00	RW	Bit[7:0]: G24 of 8x8 G control point array for S of sensor 1
0x80206655	SNR1_LENC_S_G25	0x00	RW	Bit[7:0]: G25 of 8x8 G control point array for S of sensor 1
0x80206656	SNR1_LENC_S_G26	0x00	RW	Bit[7:0]: G26 of 8x8 G control point array for S of sensor 1
0x80206657	SNR1_LENC_S_G27	0x00	RW	Bit[7:0]: G27 of 8x8 G control point array for S of sensor 1
0x80206658	SNR1_LENC_S_G30	0x00	RW	Bit[7:0]: G30 of 8x8 G control point array for S of sensor 1
0x80206659	SNR1_LENC_S_G31	0x00	RW	Bit[7:0]: G31 of 8x8 G control point array for S of sensor 1
0x8020665A	SNR1_LENC_S_G32	0x00	RW	Bit[7:0]: G32 of 8x8 G control point array for S of sensor 1
0x8020665B	SNR1_LENC_S_G33	0x00	RW	Bit[7:0]: G33 of 8x8 G control point array for S of sensor 1
0x8020665C	SNR1_LENC_S_G34	0x00	RW	Bit[7:0]: G34 of 8x8 G control point array for S of sensor 1
0x8020665D	SNR1_LENC_S_G35	0x00	RW	Bit[7:0]: G35 of 8x8 G control point array for S of sensor 1
0x8020665E	SNR1_LENC_S_G36	0x00	RW	Bit[7:0]: G36 of 8x8 G control point array for S of sensor 1
0x8020665F	SNR1_LENC_S_G37	0x00	RW	Bit[7:0]: G37 of 8x8 G control point array for S of sensor 1
0x80206660	SNR1_LENC_S_G40	0x00	RW	Bit[7:0]: G40 of 8x8 G control point array for S of sensor 1
0x80206661	SNR1_LENC_S_G41	0x00	RW	Bit[7:0]: G41 of 8x8 G control point array for S of sensor 1
0x80206662	SNR1_LENC_S_G42	0x00	RW	Bit[7:0]: G42 of 8x8 G control point array for S of sensor 1
0x80206663	SNR1_LENC_S_G43	0x00	RW	Bit[7:0]: G43 of 8x8 G control point array for S of sensor 1
0x80206664	SNR1_LENC_S_G44	0x00	RW	Bit[7:0]: G44 of 8x8 G control point array for S of sensor 1

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table 4-41 LENC registers (sheet 34 of 46)

address	register name	default value	R/W	description
0x80206665	SNR1_LENC_S_G45	0x00	RW	Bit[7:0]: G45 of 8x8 G control point array for S of sensor 1
0x80206666	SNR1_LENC_S_G46	0x00	RW	Bit[7:0]: G46 of 8x8 G control point array for S of sensor 1
0x80206667	SNR1_LENC_S_G47	0x00	RW	Bit[7:0]: G47 of 8x8 G control point array for S of sensor 1
0x80206668	SNR1_LENC_S_G50	0x00	RW	Bit[7:0]: G50 of 8x8 G control point array for S of sensor 1
0x80206669	SNR1_LENC_S_G51	0x00	RW	Bit[7:0]: G51 of 8x8 G control point array for S of sensor 1
0x8020666A	SNR1_LENC_S_G52	0x00	RW	Bit[7:0]: G52 of 8x8 G control point array for S of sensor 1
0x8020666B	SNR1_LENC_S_G53	0x00	RW	Bit[7:0]: G53 of 8x8 G control point array for S of sensor 1
0x8020666C	SNR1_LENC_S_G54	0x00	RW	Bit[7:0]: G54 of 8x8 G control point array for S of sensor 1
0x8020666D	SNR1_LENC_S_G55	0x00	RW	Bit[7:0]: G55 of 8x8 G control point array for S of sensor 1
0x8020666E	SNR1_LENC_S_G56	0x00	RW	Bit[7:0]: G56 of 8x8 G control point array for S of sensor 1
0x8020666F	SNR1_LENC_S_G57	0x00	RW	Bit[7:0]: G57 of 8x8 G control point array for S of sensor 1
0x80206670	SNR1_LENC_S_G60	0x00	RW	Bit[7:0]: G60 of 8x8 G control point array for S of sensor 1
0x80206671	SNR1_LENC_S_G61	0x00	RW	Bit[7:0]: G61 of 8x8 G control point array for S of sensor 1
0x80206672	SNR1_LENC_S_G62	0x00	RW	Bit[7:0]: G62 of 8x8 G control point array for S of sensor 1
0x80206673	SNR1_LENC_S_G63	0x00	RW	Bit[7:0]: G63 of 8x8 G control point array for S of sensor 1
0x80206674	SNR1_LENC_S_G64	0x00	RW	Bit[7:0]: G64 of 8x8 G control point array for S of sensor 1
0x80206675	SNR1_LENC_S_G65	0x00	RW	Bit[7:0]: G65 of 8x8 G control point array for S of sensor 1
0x80206676	SNR1_LENC_S_G66	0x00	RW	Bit[7:0]: G66 of 8x8 G control point array for S of sensor 1
0x80206677	SNR1_LENC_S_G67	0x00	RW	Bit[7:0]: G67 of 8x8 G control point array for S of sensor 1

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table 4-41 LENC registers (sheet 35 of 46)

address	register name	default value	R/W	description
0x80206678	SNR1_LENC_S_G70	0x00	RW	Bit[7:0]: G70 of 8x8 G control point array for S of sensor 1
0x80206679	SNR1_LENC_S_G71	0x00	RW	Bit[7:0]: G71 of 8x8 G control point array for S of sensor 1
0x8020667A	SNR1_LENC_S_G72	0x00	RW	Bit[7:0]: G72 of 8x8 G control point array for S of sensor 1
0x8020667B	SNR1_LENC_S_G73	0x00	RW	Bit[7:0]: G73 of 8x8 G control point array for S of sensor 1
0x8020667C	SNR1_LENC_S_G74	0x00	RW	Bit[7:0]: G74 of 8x8 G control point array for S of sensor 1
0x8020667D	SNR1_LENC_S_G75	0x00	RW	Bit[7:0]: G75 of 8x8 G control point array for S of sensor 1
0x8020667E	SNR1_LENC_S_G76	0x00	RW	Bit[7:0]: G76 of 8x8 G control point array for S of sensor 1
0x8020667F	SNR1_LENC_S_G77	0x00	RW	Bit[7:0]: G77 of 8x8 G control point array for S of sensor 1
0x80206680	SNR1_LENC_S_B00	0x20	RW	Bit[7:0]: B00 of 8x8 B control point array for S of sensor 1
0x80206681	SNR1_LENC_S_B01	0x20	RW	Bit[7:0]: B01 of 8x8 B control point array for S of sensor 1
0x80206682	SNR1_LENC_S_B02	0x20	RW	Bit[7:0]: B02 of 8x8 B control point array for S of sensor 1
0x80206683	SNR1_LENC_S_B03	0x20	RW	Bit[7:0]: B03 of 8x8 B control point array for S of sensor 1
0x80206684	SNR1_LENC_S_B04	0x20	RW	Bit[7:0]: B04 of 8x8 B control point array for S of sensor 1
0x80206685	SNR1_LENC_S_B05	0x20	RW	Bit[7:0]: B05 of 8x8 B control point array for S of sensor 1
0x80206686	SNR1_LENC_S_B06	0x20	RW	Bit[7:0]: B06 of 8x8 B control point array for S of sensor 1
0x80206687	SNR1_LENC_S_B07	0x20	RW	Bit[7:0]: B07 of 8x8 B control point array for S of sensor 1
0x80206688	SNR1_LENC_S_B10	0x20	RW	Bit[7:0]: B10 of 8x8 B control point array for S of sensor 1
0x80206689	SNR1_LENC_S_B11	0x20	RW	Bit[7:0]: B11 of 8x8 B control point array for S of sensor 1
0x8020668A	SNR1_LENC_S_B12	0x20	RW	Bit[7:0]: B12 of 8x8 B control point array for S of sensor 1

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table 4-41 LENC registers (sheet 36 of 46)

address	register name	default value	R/W	description
0x8020668B	SNR1_LENC_S_B13	0x20	RW	Bit[7:0]: B13 of 8x8 B control point array for S of sensor 1
0x8020668C	SNR1_LENC_S_B14	0x20	RW	Bit[7:0]: B14 of 8x8 B control point array for S of sensor 1
0x8020668D	SNR1_LENC_S_B15	0x20	RW	Bit[7:0]: B15 of 8x8 B control point array for S of sensor 1
0x8020668E	SNR1_LENC_S_B16	0x20	RW	Bit[7:0]: B16 of 8x8 B control point array for S of sensor 1
0x8020668F	SNR1_LENC_S_B17	0x20	RW	Bit[7:0]: B17 of 8x8 B control point array for S of sensor 1
0x80206690	SNR1_LENC_S_B20	0x20	RW	Bit[7:0]: B20 of 8x8 B control point array for S of sensor 1
0x80206691	SNR1_LENC_S_B21	0x20	RW	Bit[7:0]: B21 of 8x8 B control point array for S of sensor 1
0x80206692	SNR1_LENC_S_B22	0x20	RW	Bit[7:0]: B22 of 8x8 B control point array for S of sensor 1
0x80206693	SNR1_LENC_S_B23	0x20	RW	Bit[7:0]: B23 of 8x8 B control point array for S of sensor 1
0x80206694	SNR1_LENC_S_B24	0x20	RW	Bit[7:0]: B24 of 8x8 B control point array for S of sensor 1
0x80206695	SNR1_LENC_S_B25	0x20	RW	Bit[7:0]: B25 of 8x8 B control point array for S of sensor 1
0x80206696	SNR1_LENC_S_B26	0x20	RW	Bit[7:0]: B26 of 8x8 B control point array for S of sensor 1
0x80206697	SNR1_LENC_S_B27	0x20	RW	Bit[7:0]: B27 of 8x8 B control point array for S of sensor 1
0x80206698	SNR1_LENC_S_B30	0x20	RW	Bit[7:0]: B30 of 8x8 B control point array for S of sensor 1
0x80206699	SNR1_LENC_S_B31	0x20	RW	Bit[7:0]: B31 of 8x8 B control point array for S of sensor 1
0x8020669A	SNR1_LENC_S_B32	0x20	RW	Bit[7:0]: B32 of 8x8 B control point array for S of sensor 1
0x8020669B	SNR1_LENC_S_B33	0x20	RW	Bit[7:0]: B33 of 8x8 B control point array for S of sensor 1
0x8020669C	SNR1_LENC_S_B34	0x20	RW	Bit[7:0]: B34 of 8x8 B control point array for S of sensor 1
0x8020669D	SNR1_LENC_S_B35	0x20	RW	Bit[7:0]: B35 of 8x8 B control point array for S of sensor 1

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table 4-41 LENC registers (sheet 37 of 46)

address	register name	default value	R/W	description
0x8020669E	SNR1_LENC_S_B36	0x20	RW	Bit[7:0]: B36 of 8x8 B control point array for S of sensor 1
0x8020669F	SNR1_LENC_S_B37	0x20	RW	Bit[7:0]: B37 of 8x8 B control point array for S of sensor 1
0x802066A0	SNR1_LENC_S_B40	0x20	RW	Bit[7:0]: B40 of 8x8 B control point array for S of sensor 1
0x802066A1	SNR1_LENC_S_B41	0x20	RW	Bit[7:0]: B41 of 8x8 B control point array for S of sensor 1
0x802066A2	SNR1_LENC_S_B42	0x20	RW	Bit[7:0]: B42 of 8x8 B control point array for S of sensor 1
0x802066A3	SNR1_LENC_S_B43	0x20	RW	Bit[7:0]: B43 of 8x8 B control point array for S of sensor 1
0x802066A4	SNR1_LENC_S_B44	0x20	RW	Bit[7:0]: B44 of 8x8 B control point array for S of sensor 1
0x802066A5	SNR1_LENC_S_B45	0x20	RW	Bit[7:0]: B45 of 8x8 B control point array for S of sensor 1
0x802066A6	SNR1_LENC_S_B46	0x20	RW	Bit[7:0]: B46 of 8x8 B control point array for S of sensor 1
0x802066A7	SNR1_LENC_S_B47	0x20	RW	Bit[7:0]: B47 of 8x8 B control point array for S of sensor 1
0x802066A8	SNR1_LENC_S_B50	0x20	RW	Bit[7:0]: B50 of 8x8 B control point array for S of sensor 1
0x802066A9	SNR1_LENC_S_B51	0x20	RW	Bit[7:0]: B51 of 8x8 B control point array for S of sensor 1
0x802066AA	SNR1_LENC_S_B52	0x20	RW	Bit[7:0]: B52 of 8x8 B control point array for S of sensor 1
0x802066AB	SNR1_LENC_S_B53	0x20	RW	Bit[7:0]: B53 of 8x8 B control point array for S of sensor 1
0x802066AC	SNR1_LENC_S_B54	0x20	RW	Bit[7:0]: B54 of 8x8 B control point array for S of sensor 1
0x802066AD	SNR1_LENC_S_B55	0x20	RW	Bit[7:0]: B55 of 8x8 B control point array for S of sensor 1
0x802066AE	SNR1_LENC_S_B56	0x20	RW	Bit[7:0]: B56 of 8x8 B control point array for S of sensor 1
0x802066AF	SNR1_LENC_S_B57	0x20	RW	Bit[7:0]: B57 of 8x8 B control point array for S of sensor 1
0x802066B0	SNR1_LENC_S_B60	0x20	RW	Bit[7:0]: B60 of 8x8 B control point array for S of sensor 1

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table 4-41 LENC registers (sheet 38 of 46)

address	register name	default value	R/W	description
0x802066B1	SNR1_LENC_S_B61	0x20	RW	Bit[7:0]: B61 of 8x8 B control point array for S of sensor 1
0x802066B2	SNR1_LENC_S_B62	0x20	RW	Bit[7:0]: B62 of 8x8 B control point array for S of sensor 1
0x802066B3	SNR1_LENC_S_B63	0x20	RW	Bit[7:0]: B63 of 8x8 B control point array for S of sensor 1
0x802066B4	SNR1_LENC_S_B64	0x20	RW	Bit[7:0]: B64 of 8x8 B control point array for S of sensor 1
0x802066B5	SNR1_LENC_S_B65	0x20	RW	Bit[7:0]: B65 of 8x8 B control point array for S of sensor 1
0x802066B6	SNR1_LENC_S_B66	0x20	RW	Bit[7:0]: B66 of 8x8 B control point array for S of sensor 1
0x802066B7	SNR1_LENC_S_B67	0x20	RW	Bit[7:0]: B67 of 8x8 B control point array for S of sensor 1
0x802066B8	SNR1_LENC_S_B70	0x20	RW	Bit[7:0]: B70 of 8x8 B control point array for S of sensor 1
0x802066B9	SNR1_LENC_S_B71	0x20	RW	Bit[7:0]: B71 of 8x8 B control point array for S of sensor 1
0x802066BA	SNR1_LENC_S_B72	0x20	RW	Bit[7:0]: B72 of 8x8 B control point array for S of sensor 1
0x802066BB	SNR1_LENC_S_B73	0x20	RW	Bit[7:0]: B73 of 8x8 B control point array for S of sensor 1
0x802066BC	SNR1_LENC_S_B74	0x20	RW	Bit[7:0]: B74 of 8x8 B control point array for S of sensor 1
0x802066BD	SNR1_LENC_S_B75	0x20	RW	Bit[7:0]: B75 of 8x8 B control point array for S of sensor 1
0x802066BE	SNR1_LENC_S_B76	0x20	RW	Bit[7:0]: B76 of 8x8 B control point array for S of sensor 1
0x802066BF	SNR1_LENC_S_B77	0x20	RW	Bit[7:0]: B77 of 8x8 B control point array for S of sensor 1
0x802066C0	SNR1_LENC_S_R00	0x20	RW	Bit[7:0]: R00 of 8x8 R control point array for S of sensor 1
0x802066C1	SNR1_LENC_S_R01	0x20	RW	Bit[7:0]: R01 of 8x8 R control point array for S of sensor 1
0x802066C2	SNR1_LENC_S_R02	0x20	RW	Bit[7:0]: R02 of 8x8 R control point array for S of sensor 1
0x802066C3	SNR1_LENC_S_R03	0x20	RW	Bit[7:0]: R03 of 8x8 R control point array for S of sensor 1

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table 4-41 LENC registers (sheet 39 of 46)

address	register name	default value	R/W	description
0x802066C4	SNR1_LENC_S_R04	0x20	RW	Bit[7:0]: R04 of 8x8 R control point array for S of sensor 1
0x802066C5	SNR1_LENC_S_R05	0x20	RW	Bit[7:0]: R05 of 8x8 R control point array for S of sensor 1
0x802066C6	SNR1_LENC_S_R06	0x20	RW	Bit[7:0]: R06 of 8x8 R control point array for S of sensor 1
0x802066C7	SNR1_LENC_S_R07	0x20	RW	Bit[7:0]: R07 of 8x8 R control point array for S of sensor 1
0x802066C8	SNR1_LENC_S_R10	0x20	RW	Bit[7:0]: R10 of 8x8 R control point array for S of sensor 1
0x802066C9	SNR1_LENC_S_R11	0x20	RW	Bit[7:0]: R11 of 8x8 R control point array for S of sensor 1
0x802066CA	SNR1_LENC_S_R12	0x20	RW	Bit[7:0]: R12 of 8x8 R control point array for S of sensor 1
0x802066CB	SNR1_LENC_S_R13	0x20	RW	Bit[7:0]: R13 of 8x8 R control point array for S of sensor 1
0x802066CC	SNR1_LENC_S_R14	0x20	RW	Bit[7:0]: R14 of 8x8 R control point array for S of sensor 1
0x802066CD	SNR1_LENC_S_R15	0x20	RW	Bit[7:0]: R15 of 8x8 R control point array for S of sensor 1
0x802066CE	SNR1_LENC_S_R16	0x20	RW	Bit[7:0]: R16 of 8x8 R control point array for S of sensor 1
0x802066CF	SNR1_LENC_S_R17	0x20	RW	Bit[7:0]: R17 of 8x8 R control point array for S of sensor 1
0x802066D0	SNR1_LENC_S_R20	0x20	RW	Bit[7:0]: R20 of 8x8 R control point array for S of sensor 1
0x802066D1	SNR1_LENC_S_R21	0x20	RW	Bit[7:0]: R21 of 8x8 R control point array for S of sensor 1
0x802066D2	SNR1_LENC_S_R22	0x20	RW	Bit[7:0]: R22 of 8x8 R control point array for S of sensor 1
0x802066D3	SNR1_LENC_S_R23	0x20	RW	Bit[7:0]: R23 of 8x8 R control point array for S of sensor 1
0x802066D4	SNR1_LENC_S_R24	0x20	RW	Bit[7:0]: R24 of 8x8 R control point array for S of sensor 1
0x802066D5	SNR1_LENC_S_R25	0x20	RW	Bit[7:0]: R25 of 8x8 R control point array for S of sensor 1
0x802066D6	SNR1_LENC_S_R26	0x20	RW	Bit[7:0]: R26 of 8x8 R control point array for S of sensor 1

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table 4-41 LENC registers (sheet 40 of 46)

address	register name	default value	R/W	description
0x802066D7	SNR1_LENC_S_R27	0x20	RW	Bit[7:0]: R27 of 8x8 R control point array for S of sensor 1
0x802066D8	SNR1_LENC_S_R30	0x20	RW	Bit[7:0]: R30 of 8x8 R control point array for S of sensor 1
0x802066D9	SNR1_LENC_S_R31	0x20	RW	Bit[7:0]: R31 of 8x8 R control point array for S of sensor 1
0x802066DA	SNR1_LENC_S_R32	0x20	RW	Bit[7:0]: R32 of 8x8 R control point array for S of sensor 1
0x802066DB	SNR1_LENC_S_R33	0x20	RW	Bit[7:0]: R33 of 8x8 R control point array for S of sensor 1
0x802066DC	SNR1_LENC_S_R34	0x20	RW	Bit[7:0]: R34 of 8x8 R control point array for S of sensor 1
0x802066DD	SNR1_LENC_S_R35	0x20	RW	Bit[7:0]: R35 of 8x8 R control point array for S of sensor 1
0x802066DE	SNR1_LENC_S_R36	0x20	RW	Bit[7:0]: R36 of 8x8 R control point array for S of sensor 1
0x802066DF	SNR1_LENC_S_R37	0x20	RW	Bit[7:0]: R37 of 8x8 R control point array for S of sensor 1
0x802066E0	SNR1_LENC_S_R40	0x20	RW	Bit[7:0]: R40 of 8x8 R control point array for S of sensor 1
0x802066E1	SNR1_LENC_S_R41	0x20	RW	Bit[7:0]: R41 of 8x8 R control point array for S of sensor 1
0x802066E2	SNR1_LENC_S_R42	0x20	RW	Bit[7:0]: R42 of 8x8 R control point array for S of sensor 1
0x802066E3	SNR1_LENC_S_R43	0x20	RW	Bit[7:0]: R43 of 8x8 R control point array for S of sensor 1
0x802066E4	SNR1_LENC_S_R44	0x20	RW	Bit[7:0]: R44 of 8x8 R control point array for S of sensor 1
0x802066E5	SNR1_LENC_S_R45	0x20	RW	Bit[7:0]: R45 of 8x8 R control point array for S of sensor 1
0x802066E6	SNR1_LENC_S_R46	0x20	RW	Bit[7:0]: R46 of 8x8 R control point array for S of sensor 1
0x802066E7	SNR1_LENC_S_R47	0x20	RW	Bit[7:0]: R47 of 8x8 R control point array for S of sensor 1
0x802066E8	SNR1_LENC_S_R50	0x20	RW	Bit[7:0]: R50 of 8x8 R control point array for S of sensor 1
0x802066E9	SNR1_LENC_S_R51	0x20	RW	Bit[7:0]: R51 of 8x8 R control point array for S of sensor 1

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table 4-41 LENC registers (sheet 41 of 46)

address	register name	default value	R/W	description
0x802066EA	SNR1_LENC_S_R52	0x20	RW	Bit[7:0]: R52 of 8x8 R control point array for S of sensor 1
0x802066EB	SNR1_LENC_S_R53	0x20	RW	Bit[7:0]: R53 of 8x8 R control point array for S of sensor 1
0x802066EC	SNR1_LENC_S_R54	0x20	RW	Bit[7:0]: R54 of 8x8 R control point array for S of sensor 1
0x802066ED	SNR1_LENC_S_R55	0x20	RW	Bit[7:0]: R55 of 8x8 R control point array for S of sensor 1
0x802066EE	SNR1_LENC_S_R56	0x20	RW	Bit[7:0]: R56 of 8x8 R control point array for S of sensor 1
0x802066EF	SNR1_LENC_S_R57	0x20	RW	Bit[7:0]: R57 of 8x8 R control point array for S of sensor 1
0x802066F0	SNR1_LENC_S_R60	0x20	RW	Bit[7:0]: R60 of 8x8 R control point array for S of sensor 1
0x802066F1	SNR1_LENC_S_R61	0x20	RW	Bit[7:0]: R61 of 8x8 R control point array for S of sensor 1
0x802066F2	SNR1_LENC_S_R62	0x20	RW	Bit[7:0]: R62 of 8x8 R control point array for S of sensor 1
0x802066F3	SNR1_LENC_S_R63	0x20	RW	Bit[7:0]: R63 of 8x8 R control point array for S of sensor 1
0x802066F4	SNR1_LENC_S_R64	0x20	RW	Bit[7:0]: R64 of 8x8 R control point array for S of sensor 1
0x802066F5	SNR1_LENC_S_R65	0x20	RW	Bit[7:0]: R65 of 8x8 R control point array for S of sensor 1
0x802066F6	SNR1_LENC_S_R66	0x20	RW	Bit[7:0]: R66 of 8x8 R control point array for S of sensor 1
0x802066F7	SNR1_LENC_S_R67	0x20	RW	Bit[7:0]: R67 of 8x8 R control point array for S of sensor 1
0x802066F8	SNR1_LENC_S_R70	0x20	RW	Bit[7:0]: R70 of 8x8 R control point array for S of sensor 1
0x802066F9	SNR1_LENC_S_R71	0x20	RW	Bit[7:0]: R71 of 8x8 R control point array for S of sensor 1
0x802066FA	SNR1_LENC_S_R72	0x20	RW	Bit[7:0]: R72 of 8x8 R control point array for S of sensor 1
0x802066FB	SNR1_LENC_S_R73	0x20	RW	Bit[7:0]: R73 of 8x8 R control point array for S of sensor 1
0x802066FC	SNR1_LENC_S_R74	0x20	RW	Bit[7:0]: R74 of 8x8 R control point array for S of sensor 1

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table 4-41 LENC registers (sheet 42 of 46)

address	register name	default value	R/W	description
0x802066FD	SNR1_LENC_S_R75	0x20	RW	Bit[7:0]: R75 of 8x8 R control point array for S of sensor 1
0x802066FE	SNR1_LENC_S_R76	0x20	RW	Bit[7:0]: R76 of 8x8 R control point array for S of sensor 1
0x802066FF	SNR1_LENC_S_R77	0x20	RW	Bit[7:0]: R77 of 8x8 R control point array for S of sensor 1
0x80206700	SNR0_LENC_CTRL10	0x05	RW	Bit[7:3]: Reserved Bit[2]: Less than 1x gain enable for L of sensor 0 Bit[1]: Add random bits enable for L of sensor 0 Bit[0]: Auto lens switch enable for L of sensor 0
0x80206701	SNR0_MAXGAIN_L_ BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensorGain2 for L of sensor 0[11:8]
0x80206702	SNR0_MAXGAIN_L_ BYTE0	0x60	RW	Bit[7:0]: m_nSensorGain2 for L of sensor 0[7:0]
0x80206703	SNR0_MINGAIN_L_ BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensorGain1 for L of sensor 0[11:8]
0x80206704	SNR0_MINGAIN_L_ BYTE0	0x20	RW	Bit[7:0]: m_nSensorGain1 for L of sensor 0[7:0]
0x80206705	SNR0_MINQ_L	0x18	RW	Bit[7]: Reserved Bit[6:0]: Minimum Q for L of sensor 0
0x80206706	SNR0_MAXQ_L	0x40	RW	Bit[7]: Reserved Bit[6:0]: Maximum Q for L of sensor 0
0x80206707	SNR0_LENC_CTRL11	0x05	RW	Bit[7:3]: Reserved Bit[2]: Less than 1x gain enable for S of sensor 0 Bit[1]: Add random bits enable for S of sensor 0 Bit[0]: Auto lens switch enable for S of sensor 0
0x80206708	SNR0_MAXGAIN_S_ BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensorGain2 for S of sensor 0[11:8]
0x80206709	SNR0_MAXGAIN_S_ BYTE0	0x60	RW	Bit[7:0]: m_nSensorGain2 for S of sensor 0[7:0]

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table 4-41 LENC registers (sheet 43 of 46)

address	register name	default value	R/W	description
0x8020670A	SNR0_MINGAIN_S_BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensorGain1 for S of sensor 0[11:8]
0x8020670B	SNR0_MINGAIN_S_BYTE0	0x20	RW	Bit[7:0]: m_nSensorGain1 for S of sensor 0[7:0]
0x8020670C	SNR0_MINQ_S	0x18	RW	Bit[7]: Reserved Bit[6:0]: Minimum Q for S of sensor 0
0x8020670D	SNR0_MAXQ_S	0x40	RW	Bit[7]: Reserved Bit[6:0]: Maximum Q for S of sensor 0
0x8020670E	SNR0_LENC_CTRL12	0x05	RW	Bit[7:3]: Reserved Bit[2]: Less than 1x gain enable for VS of sensor 0 Bit[1]: Add random bits enable for VS of sensor 0 Bit[0]: Auto lens switch enable for VS of sensor 0
0x8020670F	SNR0_MAXGAIN_VS_BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensorGain2 for VS of sensor 0[11:8]
0x80206710	SNR0_MAXGAIN_VS_BYTE0	0x60	RW	Bit[7:0]: m_nSensorGain2 for VS of sensor 0[7:0]
0x80206711	SNR0_MINGAIN_VS_BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensorGain1 for VS of sensor 0[11:8]
0x80206712	SNR0_MINGAIN_VS_BYTE0	0x20	RW	Bit[7:0]: m_nSensorGain1 for VS of sensor 0[7:0]
0x80206713	SNR0_MINQ_VS	0x18	RW	Bit[7]: Reserved Bit[6:0]: Minimum Q for VS of sensor 0
0x80206714	SNR0_MAXQ_VS	0x40	RW	Bit[7]: Reserved Bit[6:0]: Maximum Q for VS of sensor 0
0x80206715	SNR0_BR_HSCALE_BYTE1	0x02	RW	Bit[7:0]: H scale for sensor 0[15:8]
0x80206716	SNR0_BR_HSCALE_BYTE0	0x0A	RW	Bit[7:0]: H scale for sensor 0[7:0]
0x80206717	SNR0_BR_VSCALE_BYTE1	0x02	RW	Bit[7:0]: V scale for sensor 0[15:8]
0x80206718	SNR0_BR_VSCALE_BYTE0	0xF4	RW	Bit[7:0]: V scale for sensor 0[7:0]
0x80206719	SNR0_G_HSCALE_BYTE1	0x02	RW	Bit[7:0]: H scale for sensor 0[15:8]

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table 4-41 LENC registers (sheet 44 of 46)

address	register name	default value	R/W	description
0x8020671A	SNR0_G_HSCALE_BYTE0	0x0A	RW	Bit[7:0]: H scale for sensor 0[7:0]
0x8020671B	SNR0_G_VSCALE_BYTE1	0x01	RW	Bit[7:0]: V scale for sensor 0[15:8]
0x8020671C	SNR0_G_VSCALE_BYTE0	0x7A	RW	Bit[7:0]: V scale for sensor 0[7:0]
0x8020671D	SNR0_MQ_OPTION	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 m_nQ option 000: L/S/VS use m_nQ of themselves 001: L/S/VS all use m_nQ of VS 010: L/S/VS all use m_nQ of S 100: L/S/VS all use m_nQ of L Others: Reserved
0x80206724	SNR1_LENC_CTRL10	0x05	RW	Bit[7:3]: Reserved Bit[2]: Less than 1x gain enable for L of sensor 1 Bit[1]: Add random bits enable for L of sensor 1 Bit[0]: Auto lens switch enable for L of sensor 1
0x80206725	SNR1_MAXGAIN_L_BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensorGain2 for L of sensor 1[11:8]
0x80206726	SNR1_MAXGAIN_L_BYTE0	0x60	RW	Bit[7:0]: m_nSensorGain2 for L of sensor 1[7:0]
0x80206727	SNR1_MINGAIN_L_BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensorGain1 for L of sensor 1[11:8]
0x80206728	SNR1_MINGAIN_L_BYTE0	0x20	RW	Bit[7:0]: m_nSensorGain1 for L of sensor 1[7:0]
0x80206729	SNR1_MINQ_L	0x18	RW	Bit[7]: Reserved Bit[6:0]: Minimum Q for L of sensor 1
0x8020672A	SNR1_MAXQ_L	0x40	RW	Bit[7]: Reserved Bit[6:0]: Maximum Q for L of sensor 1

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table 4-41 LENC registers (sheet 45 of 46)

address	register name	default value	R/W	description
0x8020672B	SNR1_LENC_CTRL11	0x05	RW	Bit[7:3]: Reserved Bit[2]: Less than 1x gain enable for S of sensor 1 Bit[1]: Add random bits enable for S of sensor 1 Bit[0]: Auto lens switch enable for S of sensor 1
0x8020672C	SNR1_MAXGAIN_S_BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensorGain2 for S of sensor 1[11:8]
0x8020672D	SNR1_MAXGAIN_S_BYTE0	0x60	RW	Bit[7:0]: m_nSensorGain2 for S of sensor 1[7:0]
0x8020672E	SNR1_MINGAIN_S_BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensorGain1 for S of sensor 1[11:8]
0x8020672F	SNR1_MINGAIN_S_BYTE0	0x20	RW	Bit[7:0]: m_nSensorGain1 for S of sensor 1[7:0]
0x80206730	SNR1_MINQ_S	0x18	RW	Bit[7]: Reserved Bit[6:0]: Minimum Q for S of sensor 1
0x80206731	SNR1_MAXQ_S	0x40	RW	Bit[7]: Reserved Bit[6:0]: Maximum Q for S of sensor 1
0x80206732	SNR1_LENC_CTRL12	0x05	RW	Bit[7:3]: Reserved Bit[2]: Less than 1x gain enable for VS of sensor 1 Bit[1]: Add random bits enable for VS of sensor 1 Bit[0]: Auto lens switch enable for VS of sensor 1
0x80206733	SNR1_MAXGAIN_VS_BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensorGain2 for VS of sensor 1[11:8]
0x80206734	SNR1_MAXGAIN_VS_BYTE0	0x60	RW	Bit[7:0]: m_nSensorGain2 for VS of sensor 1[7:0]
0x80206735	SNR1_MINGAIN_VS_BYTE1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: m_nSensorGain1 for VS of sensor 1[11:8]
0x80206736	SNR1_MINGAIN_VS_BYTE0	0x20	RW	Bit[7:0]: m_nSensorGain1 for VS of sensor 1[7:0]
0x80206737	SNR1_MINQ_VS	0x18	RW	Bit[7]: Reserved Bit[6:0]: Minimum Q for VS of sensor 1

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table 4-41 LENC registers (sheet 46 of 46)

address	register name	default value	R/W	description
0x80206738	SNR1_MAXQ_VS	0x40	RW	Bit[7]: Reserved Bit[6:0]: Maximum Q for VS of sensor 1
0x80206739	SNR1_BR_HSCALE_BYTE1	0x02	RW	Bit[7:0]: H scale for sensor 1[15:8]
0x8020673A	SNR1_BR_HSCALE_BYTE0	0x0A	RW	Bit[7:0]: H scale for sensor 1[7:0]
0x8020673B	SNR1_BR_VSCALE_BYTE1	0x02	RW	Bit[7:0]: V scale for sensor 1[15:8]
0x8020673C	SNR1_BR_VSCALE_BYTE0	0xF4	RW	Bit[7:0]: V scale for sensor 1[7:0]
0x8020673D	SNR1_G_HSCALE_BYTE1	0x02	RW	Bit[7:0]: H scale for sensor 1[15:8]
0x8020673E	SNR1_G_HSCALE_BYTE0	0x0A	RW	Bit[7:0]: H scale for sensor 1[7:0]
0x8020673F	SNR1_G_VSCALE_BYTE1	0x01	RW	Bit[7:0]: V scale for sensor 1[15:8]
0x80206740	SNR1_G_VSCALE_BYTE0	0x7A	RW	Bit[7:0]: V scale for sensor 1[7:0]
0x80206741	SNR1_MQ_OPTION	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 m_nQ option 000: L/S/VS use m_nQ of themselves 001: L/S/VS all use m_nQ of VS 010: L/S/VS all use m_nQ of S 100: L/S/VS all use m_nQ of L Others: Reserved

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4.32 RAW data de-noise (RAW DNS) control

table 4-42 RAW DNS registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x80206380	SNR0_DNS_CTRL0	0x0D	RW	Sensor 0 Control Bit[7:6]: Reserved Bit[5:2]: m_nNoiseYSlope Bit[1]: Manual noise/edge threshold enable Bit[0]: m_bGDNSEnable
0x80206381	SNR0_DNS_NOISE_LIST_0	0x04	RW	Bit[7:0]: Sensor 0 noise list 0
0x80206382	SNR0_DNS_NOISE_LIST_1	0x08	RW	Bit[7:0]: Sensor 0 noise list 1
0x80206383	SNR0_DNS_NOISE_LIST_2	0x10	RW	Bit[7:0]: Sensor 0 noise list 2
0x80206384	SNR0_DNS_NOISE_LIST_3	0x18	RW	Bit[7:0]: Sensor 0 noise list 3
0x80206385	SNR0_DNS_NOISE_LIST_4	0x20	RW	Bit[7:0]: Sensor 0 noise list 4
0x80206386	SNR0_DNS_NOISE_LIST_5	0x30	RW	Bit[7:0]: Sensor 0 noise list 5
0x80206387	SNR0_DNS_NOISE_LIST_6	0x40	RW	Bit[7:0]: Sensor 0 noise list 6
0x80206388	SNR0_DNS_NOISE_LIST_7	0x40	RW	Bit[7:0]: Sensor 0 noise list 7
0x80206389	SNR0_DNS_MAX_EDGETHRE	0xFF	RW	Bit[7:0]: Sensor 0 maximum edge threshold
0x8020638A	SNR0_DNS_NOISE_MAN	0x08	RW	Bit[7:0]: Sensor 0 manual noise level
0x8020638B	SNR0_DNS_EDGETHRE_MAN	0x18	RW	Bit[7:0]: Sensor 0 manual edge threshold
0x8020638C	SNR0_DNS_NOISE	–	R	Bit[7:0]: Sensor 0 noise
0x8020638D	SNR0_DNS_EDGETHRE	–	R	Bit[7:0]: Sensor 0 edge threshold
0x80206390	SNR1_DNS_CTRL0	0x0D	RW	Sensor 1 Control Bit[7:6]: Reserved Bit[5:2]: m_nNoiseYSlope Bit[1]: Manual noise/edge threshold enable Bit[0]: m_bGDNSEnable
0x80206391	SNR1_DNS_NOISE_LIST_0	0x04	RW	Bit[7:0]: Sensor 1 noise list 0
0x80206392	SNR1_DNS_NOISE_LIST_1	0x08	RW	Bit[7:0]: Sensor 1 noise list 1
0x80206393	SNR1_DNS_NOISE_LIST_2	0x10	RW	Bit[7:0]: Sensor 1 noise list 2
0x80206394	SNR1_DNS_NOISE_LIST_3	0x18	RW	Bit[7:0]: Sensor 1 noise list 3
0x80206395	SNR1_DNS_NOISE_LIST_4	0x20	RW	Bit[7:0]: Sensor 1 noise list 4

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table 4-42 RAW DNS registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x80206396	SNR1_DNS_NOISE_LIST_5	0x30	RW	Bit[7:0]: Sensor 1 noise list 5
0x80206397	SNR1_DNS_NOISE_LIST_6	0x40	RW	Bit[7:0]: Sensor 1 noise list 6
0x80206398	SNR1_DNS_NOISE_LIST_7	0x40	RW	Bit[7:0]: Sensor 1 noise list 7
0x80206399	SNR1_DNS_MAX_EDGETHRE	0xFF	RW	Bit[7:0]: Sensor 1 maximum edge threshold
0x8020639A	SNR1_DNS_NOISE_MAN	0x08	RW	Bit[7:0]: Sensor 1 manual noise level
0x8020639B	SNR1_DNS_EDGETHRE_MAN	0x18	RW	Bit[7:0]: Sensor 1 manual edge threshold
0x8020639C	SNR1_DNS_NOISE	–	R	Bit[7:0]: Sensor 1 noise
0x8020639D	SNR1_DNS_EDGETHRE	–	R	Bit[7:0]: Sensor 1 edge threshold

4.33 pre ISP control

table 4-43 pre ISP registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x80206080	SNR_PRE_CTRL	0x01	RW	Pre_ISP Control For Dual Sensors Bit[7:5]: Reserved Bit[4]: Random image with same seed enable Bit[3:0]: Random image seed
0x80206081	SNR0_PRE_CTRL0	0x00	RW	Pre_ISP Sensor 0 Control Bit[7]: Reserved Bit[6]: Rolling lines enable Bit[5]: Transport mode enable Bit[4]: Square black/white enable Bit[3:2]: Color bar style Bit[1:0]: Test image select
0x80206082	SNR0_PRE_CTRL1	0x11	RW	Pre_ISP Sensor 0 Control Bit[7]: Reserved Bit[6]: Low bits with 0 enable Bit[5:3]: Long/short exposure test data ratio (2^n) Bit[2:0]: Short/vshort exposure test data ratio (2^n)

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table 4-43 pre ISP registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x80206083	SNR0_PRE_CTRL2	0x00	RW	Pre_ISP Sensor 0 Interrupt Line Number High Byte
0x80206084	SNR0_PRE_CTRL3	0x13	RW	Pre_ISP Sensor 0 Interrupt Line Number Low Byte
0x80206085	SNR0_PRE_CTRL4	–	R	Pre_ISP Sensor 0 Actual Pixel Number of a Line High Byte
0x80206086	SNR0_PRE_CTRL5	–	R	Pre_ISP Sensor 0 Actual Pixel Number of a Line Low Byte
0x80206087	SNR0_PRE_CTRL6	–	R	Pre_ISP Sensor 0 Actual Line Number of a Frame High Byte
0x80206088	SNR0_PRE_CTRL7	–	R	Pre_ISP Sensor 0 Actual Line Number of a Frame Low Byte
0x80206090	SNR1_PRE_CTRL0	0x00	RW	Pre_ISP Sensor 1 Control Bit[7]: Test mode enable Bit[6]: Rolling lines enable Bit[5]: Transport mode enable Bit[4]: Square black/white enable Bit[3:2]: Color bar style Bit[1:0]: Test image select
0x80206091	SNR1_PRE_CTRL1	0x11	RW	Pre_ISP Sensor 1 Control Bit[7]: Reserved Bit[6]: Low bits with 0 enable Bit[5:3]: Long/short exposure test data ratio(2^n) Bit[2:0]: Short/vshort exposure test data ratio (2^n)
0x80206092	SNR1_PRE_CTRL2	0x00	RW	Pre_ISP Sensor 1 Interrupt Line Number High Byte
0x80206093	SNR1_PRE_CTRL3	0x13	RW	Pre_ISP Sensor 1 Interrupt Line Number Low Byte
0x80206094	SNR1_PRE_CTRL4	–	R	Pre_ISP Sensor 1 Actual Pixel Number of a Line High Byte
0x80206095	SNR1_PRE_CTRL5	–	R	Pre_ISP Sensor 1 Actual Pixel Number of a Line Low Byte
0x80206096	SNR1_PRE_CTRL6	–	R	Pre_ISP Sensor 1 Actual Line Number of a Frame High Byte
0x80206097	SNR1_PRE_CTRL7	–	R	Pre_ISP Sensor 1 Actual Line Number of a Frame Low Byte

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4.34 RGBH data de-noise (RGBH DNS) control

table 4-44 RGBH DNS registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x80207B00	SNR0_RGB_DNS_CTRL0	0x0D	RW	Bit[7:6]: Reserved Bit[5:1]: Sensor 0 shadow extra noise Bit[0]: Sensor 0 smooth Y enable
0x80207B01	SNR0_RGB_DNS_CTRL1	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 RGB DNS edgethre
0x80207B02	SNR0_RGB_DNS_CTRL2	0x08	RW	Bit[7:6]: Reserved Bit[5:3]: Sensor 0 Y noise list1 Bit[2:0]: Sensor 0 Y noise list0
0x80207B03	SNR0_RGB_DNS_CTRL3	0x1A	RW	Bit[7:6]: Reserved Bit[5:3]: Sensor 0 Y noise list3 Bit[2:0]: Sensor 0 Y noise list2
0x80207B04	SNR0_RGB_DNS_CTRL4	0x24	RW	Bit[7:6]: Reserved Bit[5:3]: Sensor 0 Y noise list5 Bit[2:0]: Sensor 0 Y noise list4
0x80207B05	SNR0_RGB_DNS_CTRL5	0x24	RW	Bit[7:6]: Reserved Bit[5:3]: Sensor 0 Y noise list7 Bit[2:0]: Sensor 0 Y noise list6
0x80207B06	SNR0_RGB_DNS_CTRL6	0x02	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 UV noise list0
0x80207B07	SNR0_RGB_DNS_CTRL7	0x04	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 UV noise list1
0x80207B08	SNR0_RGB_DNS_CTRL8	0x06	RW	Bit[7:6]: Reserved Bit[5:0: Sensor 0 UV noise list2
0x80207B09	SNR0_RGB_DNS_CTRL9	0x08	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 UV noise list3
0x80207B0A	SNR0_RGB_DNS_CTRLA	0x0A	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 UV noise list4
0x80207B0B	SNR0_RGB_DNS_CTRLB	0x0A	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 UV noise list5
0x80207B0C	SNR0_RGB_DNS_CTRLC	0x0A	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 UV noise list6
0x80207B0D	SNR0_RGB_DNS_CTRLD	0x0A	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 UV noise list7

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table 4-44 RGBH DNS registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x80207B0E	SNR0_RGB_DNS_CTRLE	0x02	RW	Bit[7:4]: Reserved Bit[3:1]: Sensor 0 Y noise manual value Bit[0]: Sensor 0 RGB DNS manual mode
0x80207B0F	SNR0_RGB_DNS_CTRLF	0x04	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 UV noise manual value
0x80207B10	SNR0_RGB_DNS_CTRL10	–	R	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 Y noise
0x80207B11	SNR0_RGB_DNS_CTRL11	–	R	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 UV noise
0x80207B20	SNR1_RGB_DNS_CTRL0	0x0D	RW	Bit[7:6]: Reserved Bit[5:1]: Sensor 1 shadow extra noise Bit[0]: Sensor 1 smooth Y enable
0x80207B21	SNR1_RGB_DNS_CTRL1	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 RGB DNS edgethre
0x80207B22	SNR1_RGB_DNS_CTRL2	0x08	RW	Bit[7:6]: Reserved Bit[5:3]: Sensor 1 Y noise list1 Bit[2:0]: Sensor 1 Y noise list0
0x80207B23	SNR1_RGB_DNS_CTRL3	0x1A	RW	Bit[7:6]: Reserved Bit[5:3]: Sensor 1 Y noise list3 Bit[2:0]: Sensor 1 Y noise list2
0x80207B24	SNR1_RGB_DNS_CTRL4	0x24	RW	Bit[7:6]: Reserved Bit[5:3]: Sensor 1 Y noise list5 Bit[2:0]: Sensor 1 Y noise list4
0x80207B25	SNR1_RGB_DNS_CTRL5	0x24	RW	Bit[7:6]: Reserved Bit[5:3]: Sensor 1 Y noise list7 Bit[2:0]: Sensor 1 Y noise list6
0x80207B26	SNR1_RGB_DNS_CTRL6	0x02	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 UV noise list0
0x80207B27	SNR1_RGB_DNS_CTRL7	0x04	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 UV noise list1
0x80207B28	SNR1_RGB_DNS_CTRL8	0x06	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 UV noise list2
0x80207B29	SNR1_RGB_DNS_CTRL9	0x08	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 UV noise list3
0x80207B2A	SNR1_RGB_DNS_CTRLA	0x0A	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 UV noise list4

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table 4-44 RGBH DNS registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x80207B2B	SNR1_RGB_DNS_CTRLB	0x0A	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 UV noise list5
0x80207B2C	SNR1_RGB_DNS_CTRLC	0x0A	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 UV noise list6
0x80207B2D	SNR1_RGB_DNS_CTRLD	0x0A	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 UV noise list7
0x80207B2E	SNR1_RGB_DNS_CTRLE	0x02	RW	Bit[7:4]: Reserved Bit[3:1]: Sensor 1 Y noise manual value Bit[0]: Sensor 1 RGB DNS manual mode
0x80207B2F	SNR1_RGB_DNS_CTRLF	0x04	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 UV noise manual value
0x80207B30	SNR1_RGB_DNS_CTRL10	–	R	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 Y noise value
0x80207B31	SNR1_RGB_DNS_CTRL11	–	R	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 UV noise value

4.35 RGB gamma control

table 4-45 RGB gamma registers (sheet 1 of 7)

address	register name	default value	R/W	description
0x80207A01	SNR0_GAMMA_CTRL_01	0x12	RW	Bit[7:0]: Sensor 0 gamma Y list00 before auto bit-shift
0x80207A03	SNR0_GAMMA_CTRL_03	0x20	RW	Bit[7:0]: Sensor 0 gamma Y list01 before auto bit-shift
0x80207A05	SNR0_GAMMA_CTRL_05	0x3B	RW	Bit[7:0]: Sensor 0 gamma Y list02 before auto bit-shift
0x80207A07	SNR0_GAMMA_CTRL_07	0x5D	RW	Bit[7:0]: Sensor 0 gamma Y list03 before auto bit-shift
0x80207A09	SNR0_GAMMA_CTRL_09	0x6A	RW	Bit[7:0]: Sensor 0 gamma Y list04 before auto bit-shift
0x80207A0B	SNR0_GAMMA_CTRL_0B	0x76	RW	Bit[7:0]: Sensor 0 gamma Y list05 before auto bit-shift

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table 4-45 RGB gamma registers (sheet 2 of 7)

address	register name	default value	R/W	description
0x80207A0D	SNR0_GAMMA_CTRL_0D	0x81	RW	Bit[7:0]: Sensor 0 gamma Y list06 before auto bit-shift
0x80207A0F	SNR0_GAMMA_CTRL_0F	0x8B	RW	Bit[7:0]: Sensor 0 gamma Y list07 before auto bit-shift
0x80207A11	SNR0_GAMMA_CTRL_11	0x96	RW	Bit[7:0]: Sensor 0 gamma Y list08 before auto bit-shift
0x80207A13	SNR0_GAMMA_CTRL_13	0x9E	RW	Bit[7:0]: Sensor 0 gamma Y list09 before auto bit-shift
0x80207A15	SNR0_GAMMA_CTRL_15	0xAE	RW	Bit[7:0]: Sensor 0 gamma Y list0a before auto bit-shift
0x80207A17	SNR0_GAMMA_CTRL_17	0xBC	RW	Bit[7:0]: Sensor 0 gamma Y list0b before auto bit-shift
0x80207A19	SNR0_GAMMA_CTRL_19	0xCF	RW	Bit[7:0]: Sensor 0 gamma Y list0c before auto bit-shift
0x80207A1B	SNR0_GAMMA_CTRL_1B	0xDE	RW	Bit[7:0]: Sensor 0 gamma Y list0d before auto bit-shift
0x80207A1D	SNR0_GAMMA_CTRL_1D	0xEC	RW	Bit[7:0]: Sensor 0 gamma Y list0e before auto bit-shift
0x80207A1F	SNR0_GAMMA_MAX_SHD_H_GAIN	0xFF	RW	Bit[7:0]: Sensor 0 gamma m_nMaxShadowHGain[7:0]
0x80207A20	SNR0_GAMMA_PARA_MANUAL_EN	0x00	RW	Bit[7:1]: Reserved Bit[0]: Sensor 0 gamma manual control enable
0x80207A22	SNR0_GAMMA_MID_TONE_H_GAIN	0x6E	RW	Bit[7:0]: Sensor 0 gamma m_nMiddleToneHGain[7:0]
0x80207A24	SNR0_GAMMA_HIGH_LIGHT_H_GAIN	0x10	RW	Bit[7:0]: Sensor 0 gamma m_nHighLightHGain[7:0]
0x80207A26	SNR0_GAMMA_26	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list00[11:8]
0x80207A27	SNR0_GAMMA_27	0xE0	RW	Bit[7:0]: Sensor 0 manual gamma Y list00[7:0]
0x80207A28	SNR0_GAMMA_28	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list01[11:8]
0x80207A29	SNR0_GAMMA_29	0xA0	RW	Bit[7:0]: Sensor 0 manual gamma Y list01[7:0]

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table 4-45 RGB gamma registers (sheet 3 of 7)

address	register name	default value	R/W	description
0x80207A2A	SNR0_GAMMA_2A	0x03	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list02[11:8]
0x80207A2B	SNR0_GAMMA_2B	0x10	RW	Bit[7:0]: Sensor 0 manual gamma Y list02[7:0]
0x80207A2C	SNR0_GAMMA_2C	0x05	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list03[11:8]
0x80207A2D	SNR0_GAMMA_2D	0xA0	RW	Bit[7:0]: Sensor 0 manual gamma Y list03[7:0]
0x80207A2E	SNR0_GAMMA_2E	0x06	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list04[11:8]
0x80207A2F	SNR0_GAMMA_2F	0x90	RW	Bit[7:0]: Sensor 0 manual gamma Y list04[7:0]
0x80207A30	SNR0_GAMMA_30	0x07	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list05[11:8]
0x80207A31	SNR0_GAMMA_31	0x50	RW	Bit[7:0]: Sensor 0 manual gamma Y list05[7:0]
0x80207A32	SNR0_GAMMA_32	0x07	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list06[11:8]
0x80207A33	SNR0_GAMMA_33	0xE0	RW	Bit[7:0]: Sensor 0 manual gamma Y list06[7:0]
0x80207A34	SNR0_GAMMA_34	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list07[11:8]
0x80207A35	SNR0_GAMMA_35	0x80	RW	Bit[7:0]: Sensor 0 manual gamma Y list07[7:0]
0x80207A36	SNR0_GAMMA_36	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list08[11:8]
0x80207A37	SNR0_GAMMA_37	0xF0	RW	Bit[7:0]: Sensor 0 manual gamma Y list08[7:0]
0x80207A38	SNR0_GAMMA_38	0x09	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list09[11:8]
0x80207A39	SNR0_GAMMA_39	0x60	RW	Bit[7:0]: Sensor 0 manual gamma Y list09[7:0]

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table 4-45 RGB gamma registers (sheet 4 of 7)

address	register name	default value	R/W	description
0x80207A3A	SNR0_GAMMA_3A	0x0A	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list0a[11:8]
0x80207A3B	SNR0_GAMMA_3B	0x30	RW	Bit[7:0]: Sensor 0 manual gamma Y list0a[7:0]
0x80207A3C	SNR0_GAMMA_3C	0x0A	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list0b[11:8]
0x80207A3D	SNR0_GAMMA_3D	0xF0	RW	Bit[7:0]: Sensor 0 manual gamma Y list0b[7:0]
0x80207A3E	SNR0_GAMMA_3E	0x0C	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list0c[11:8]
0x80207A3F	SNR0_GAMMA_3F	0x40	RW	Bit[7:0]: Sensor 0 manual gamma Y list0c[7:0]
0x80207A40	SNR0_GAMMA_40	0x0D	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list0d[11:8]
0x80207A41	SNR0_GAMMA_41	0x70	RW	Bit[7:0]: Sensor 0 manual gamma Y list0d[7:0]
0x80207A42	SNR0_GAMMA_42	0x0E	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 manual gamma Y list0e[11:8]
0x80207A43	SNR0_GAMMA_43	0x80	RW	Bit[7:0]: Sensor 0 manual gamma Y list0e[7:0]
0x80207A51	SNR1_GAMMA_CTRL_01	0x12	RW	Bit[7:0]: Sensor 1 gamma Y list00 before auto bit-shift
0x80207A53	SNR1_GAMMA_CTRL_03	0x20	RW	Bit[7:0]: Sensor 1 gamma Y list01 before auto bit-shift
0x80207A55	SNR1_GAMMA_CTRL_05	0x3B	RW	Bit[7:0]: Sensor 1 gamma Y list02 before auto bit-shift
0x80207A57	SNR1_GAMMA_CTRL_07	0x5D	RW	Bit[7:0]: Sensor 1 gamma Y list03 before auto bit-shift
0x80207A59	SNR1_GAMMA_CTRL_09	0x6A	RW	Bit[7:0]: Sensor 1 gamma Y list04 before auto bit-shift
0x80207A5B	SNR1_GAMMA_CTRL_0B	0x76	RW	Bit[7:0]: Sensor 1 gamma Y list05 before auto bit-shift
0x80207A5D	SNR1_GAMMA_CTRL_0D	0x81	RW	Bit[7:0]: Sensor 1 gamma Y list06 before auto bit-shift

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table 4-45 RGB gamma registers (sheet 5 of 7)

address	register name	default value	R/W	description
0x80207A5F	SNR1_GAMMA_CTRL_0F	0x8B	RW	Bit[7:0]: Sensor 1 gamma Y list07 before auto bit-shift
0x80207A61	SNR1_GAMMA_CTRL_11	0x96	RW	Bit[7:0]: Sensor 1 gamma Y list08 before auto bit-shift
0x80207A63	SNR1_GAMMA_CTRL_13	0x9E	RW	Bit[7:0]: Sensor 1 gamma Y list09 before auto bit-shift
0x80207A65	SNR1_GAMMA_CTRL_15	0xAE	RW	Bit[7:0]: Sensor 1 gamma Y list0a before auto bit-shift
0x80207A67	SNR1_GAMMA_CTRL_17	0xBC	RW	Bit[7:0]: Sensor 1 gamma Y list0b before auto bit-shift
0x80207A69	SNR1_GAMMA_CTRL_19	0xCF	RW	Bit[7:0]: Sensor 1 gamma Y list0c before auto bit-shift
0x80207A6B	SNR1_GAMMA_CTRL_1B	0xDE	RW	Bit[7:0]: Sensor 1 gamma Y list0d before auto bit-shift
0x80207A6D	SNR1_GAMMA_CTRL_1D	0xEC	RW	Bit[7:0]: Sensor 1 gamma Y list0e before auto bit-shift
0x80207A6F	SNR1_GAMMA_MAX_SHD_H_GAIN	0xFF	RW	Bit[7:0]: Sensor 1 gamma m_nMaxShadowHGain[7:0]
0x80207A70	SNR1_GAMMA_PARA_MANUAL_EN	0x00	RW	Bit[7:1]: Reserved Bit[0]: Sensor 1 gamma manual control enable
0x80207A72	SNR1_GAMMA_MID_TONE_H_GAIN	0x6E	RW	Bit[7:0]: Sensor 1 gamma m_nMiddleToneHGain[7:0]
0x80207A74	SNR1_GAMMA_HIGH_LIGHT_H_GAIN	0x10	RW	Bit[7:0]: Sensor 1 gamma m_nHighLightHGain[7:0]
0x80207A76	SNR1_GAMMA_26	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list00[11:8]
0x80207A77	SNR1_GAMMA_27	0xE0	RW	Bit[7:0]: Sensor 1 manual gamma Y list00[7:0]
0x80207A78	SNR1_GAMMA_28	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list01[11:8]
0x80207A79	SNR1_GAMMA_29	0xA0	RW	Bit[7:0]: Sensor 1 manual gamma Y list01[7:0]
0x80207A7A	SNR1_GAMMA_2A	0x03	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list02[11:8]

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table 4-45 RGB gamma registers (sheet 6 of 7)

address	register name	default value	R/W	description
0x80207A7B	SNR1_GAMMA_2B	0x10	RW	Bit[7:0]: Sensor 1 manual gamma Y list02[7:0]
0x80207A7C	SNR1_GAMMA_2C	0x05	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list03[11:8]
0x80207A7D	SNR1_GAMMA_2D	0xA0	RW	Bit[7:0]: Sensor 1 manual gamma Y list03[7:0]
0x80207A7E	SNR1_GAMMA_2E	0x06	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list04[11:8]
0x80207A7F	SNR1_GAMMA_2F	0x90	RW	Bit[7:0]: Sensor 1 manual gamma Y list04[7:0]
0x80207A80	SNR1_GAMMA_30	0x07	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list05[11:8]
0x80207A81	SNR1_GAMMA_31	0x50	RW	Bit[7:0]: Sensor 1 manual gamma Y list05[7:0]
0x80207A82	SNR1_GAMMA_32	0x07	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list06[11:8]
0x80207A83	SNR1_GAMMA_33	0xE0	RW	Bit[7:0]: Sensor 1 manual gamma Y list06[7:0]
0x80207A84	SNR1_GAMMA_34	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list07[11:8]
0x80207A85	SNR1_GAMMA_35	0x80	RW	Bit[7:0]: Sensor 1 manual gamma Y list07[7:0]
0x80207A86	SNR1_GAMMA_36	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list08[11:8]
0x80207A87	SNR1_GAMMA_37	0xF0	RW	Bit[7:0]: Sensor 1 manual gamma Y list08[7:0]
0x80207A88	SNR1_GAMMA_38	0x09	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list09[11:8]
0x80207A89	SNR1_GAMMA_39	0x60	RW	Bit[7:0]: Sensor 1 manual gamma Y list09[7:0]
0x80207A8A	SNR1_GAMMA_3A	0x0A	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list0a[11:8]

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table 4-45 RGB gamma registers (sheet 7 of 7)

address	register name	default value	R/W	description
0x80207A8B	SNR1_GAMMA_3B	0x30	RW	Bit[7:0]: Sensor 1 manual gamma Y list0a[7:0]
0x80207A8C	SNR1_GAMMA_3C	0x0A	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list0b[11:8]
0x80207A8D	SNR1_GAMMA_3D	0xF0	RW	Bit[7:0]: Sensor 1 manual gamma Y list0b[7:0]
0x80207A8E	SNR1_GAMMA_3E	0x0C	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list0c[11:8]
0x80207A8F	SNR1_GAMMA_3F	0x40	RW	Bit[7:0]: Sensor 1 manual gamma Y list0c[7:0]
0x80207A90	SNR1_GAMMA_40	0x0D	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list0d[11:8]
0x80207A91	SNR1_GAMMA_41	0x70	RW	Bit[7:0]: Sensor 1 manual gamma Y list0d[7:0]
0x80207A92	SNR1_GAMMA_42	0x0E	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 manual gamma Y list0e[11:8]
0x80207A93	SNR1_GAMMA_43	0x80	RW	Bit[7:0]: Sensor 1 manual gamma Y list0e[7:0]

4.36 special digital effect (SDE) control

table 4-46 SDE registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x80207B80	SNR0_SDE_CTRL00	0x08	RW	Sensor 0 SDE Control Bit[7:4]: Reserved Bit[3]: Auto calculated brightness enable Bit[2]: m_nSDECtrl for hue adjustment Bit[1]: m_nSDECtrl for saturation adjustment Bit[0]: m_nSDECtrl for contrast and brightness adjustment

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table 4-46 SDE registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x80207B81	SNR0_SDE_CTRL01	0x00	RW	Sensor 0 SDE Control Bit[7:2]: Reserved Bit[1]: m_bAutoSaturationEnable Bit[0]: m_bAutoYOffsetEnable
0x80207B82	SNR0_SDE_YOFFSET_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 SDE Y offset[11:8]
0x80207B83	SNR0_SDE_YOFFSET_L	0x00	RW	Bit[7:0]: Sensor 0 SDE Y offset[7:0]
0x80207B84	SNR0_SDE_GAIN	0x20	RW	Bit[7:0]: Sensor 0 SDE Y gain
0x80207B85	SNR0_SDE_ BRIGHTNESS_H	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 SDE manual brightness[12:8]
0x80207B86	SNR0_SDE_ BRIGHTNESS_L	0x00	RW	Bit[7:0]: Sensor 0 SDE manual brightness[7:0]
0x80207B87	SNR0_SDE_YLEFT_STEP _H	0x00	RW	Bit[7:0]: Sensor 0 SDE brightness step of Y left[23:16]
0x80207B88	SNR0_SDE_YLEFT_STEP _M	0x00	RW	Bit[7:0]: Sensor 0 SDE brightness step of Y left[15:8]
0x80207B89	SNR0_SDE_YLEFT_STEP _L	0x00	RW	Bit[7:0]: Sensor 0 SDE brightness step of Y left[7:0]
0x80207B8A	SNR0_SDE_YRIGHT_ STEP_H	0x00	RW	Bit[7:0]: Sensor 0 SDE brightness step of Y right[23:16]
0x80207B8B	SNR0_SDE_YRIGHT_ STEP_M	0x00	RW	Bit[7:0]: Sensor 0 SDE brightness step of Y right[15:8]
0x80207B8C	SNR0_SDE_YRIGHT_ STEP_L	0x00	RW	Bit[7:0]: Sensor 0 SDE brightness step of Y right[7:0]
0x80207B8D	SNR0_SDE_YLEFT_H	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 SDE brightness Y left[12:8]
0x80207B8E	SNR0_SDE_YLEFT_L	0x00	RW	Bit[7:0]: Sensor 0 SDE brightness Y left[7:0]
0x80207B8F	SNR0_SDE_YRIGHT_H	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 SDE brightness Y right[12:8]
0x80207B90	SNR0_SDE_YRIGHT_L	0x00	RW	Bit[7:0]: Sensor 0 SDE brightness Y right[7:0]
0x80207B91	SNR0_SDE_SATU_U0	0x20	RW	Bit[7:0]: Sensor 0 SDE saturation U0
0x80207B92	SNR0_SDE_SATU_V0	0x20	RW	Bit[7:0]: Sensor 0 SDE saturation V0
0x80207B93	SNR0_SDE_SATU_U1	0x40	RW	Bit[7:0]: Sensor 0 SDE saturation U1

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table 4-46 SDE registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x80207B94	SNR0_SDE_SATU_V1	0x40	RW	Bit[7:0]: Sensor 0 SDE saturation V1
0x80207B95	SNR0_SDE_SATU_GAIN0	0x20	RW	Bit[7:0]: Sensor 0 SDE saturation gain0
0x80207B96	SNR0_SDE_SATU_GAIN1	0x80	RW	Bit[7:0]: Sensor 0 SDE saturation gain1
0x80207B97	SNR0_SDE_HUE_COS	0x01	RW	Bit[7:0]: Sensor 0 SDE hue cos
0x80207B98	SNR0_SDE_HUE_SIN	0x00	RW	Bit[7:0]: Sensor 0 SDE hue sin
0x80207B99	SNR0_SDE_XSKIP	0x01	RW	Bit[7:0]: Sensor 0 SDE X skip
0x80207B9A	SNR0_SDE_YMOVING_AVE_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 SDE Y moving average[11:8]
0x80207B9B	SNR0_SDE_YMOVING_AVE_L	0x10	RW	Bit[7:0]: Sensor 0 SDE Y moving average[7:0]
0x80207B9C	SNR0_SDE_INVWIDTH	0x00	RW	Bit[7:0]: Sensor 0 SDE inverse width (=(1<<16)/img_width)
0x80207B9D	SNR0_SDE_AVERAGE_IN_H	–	R	Bit[7:0]: Sensor 0 SDE average[15:8]
0x80207B9E	SNR0_SDE_AVERAGE_IN_L	–	R	Bit[7:0]: Sensor 0 SDE average[7:0]
0x80207B9F	SNR0_SDE_SAT_U_ADJUST_H	–	R	Bit[7:0]: Sensor 0 SDE saturation U adjust value[15:8]
0x80207BA0	SNR0_SDE_SAT_U_ADJUST_L	–	R	Bit[7:0]: Sensor 0 SDE saturation U adjust value[7:0]
0x80207BA1	SNR0_SDE_SAT_V_ADJUST_H	–	R	Bit[7:0]: Sensor 0 SDE saturation V adjust value[15:8]
0x80207BA2	SNR0_SDE_SAT_V_ADJUST_L	–	R	Bit[7:0]: Sensor 0 SDE saturation V adjust value[7:0]
0x80207BA3	SNR1_SDE_CTRL00	0x08	RW	Sensor 1 SDE Control Bit[7:4]: Reserved Bit[3]: Auto calculated brightness enable Bit[2]: m_nSDECtrl for hue adjustment Bit[1]: m_nSDECtrl for saturation adjustment Bit[0]: m_nSDECtrl for contrast and brightness adjustment

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table 4-46 SDE registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x80207BA4	SNR1_SDE_CTRL01	0x00	RW	Sensor 1 SDE Control Bit[7:2]: Reserved Bit[1]: m_bAutoSaturationEnable Bit[0]: m_bAutoYOffsetEnable
0x80207BA5	SNR1_SDE_YOFFSET_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 SDE Y offset[11:8]
0x80207BA6	SNR1_SDE_YOFFSET_L	0x00	RW	Bit[7:0]: Sensor 1 SDE Y offset[7:0]
0x80207BA7	SNR1_SDE_GAIN	0x20	RW	Bit[7:0]: Sensor 1 SDE Y gain
0x80207BA8	SNR1_SDE_ BRIGHTNESS_H	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 SDE manual brightness[12:8]
0x80207BA9	SNR1_SDE_ BRIGHTNESS_L	0x00	RW	Bit[7:0]: Sensor 1 SDE manual brightness[7:0]
0x80207BAA	SNR1_SDE_YLEFT_STEP _H	0x00	RW	Bit[7:0]: Sensor 1 SDE brightness step of Y left[23:16]
0x80207BAB	SNR1_SDE_YLEFT_STEP _M	0x00	RW	Bit[7:0]: Sensor 1 SDE brightness step of Y left[15:8]
0x80207BAC	SNR1_SDE_YLEFT_STEP _L	0x00	RW	Bit[7:0]: Sensor 1 SDE brightness step of Y left[7:0]
0x80207BAD	SNR1_SDE_YRIGHT_ STEP_H	0x00	RW	Bit[7:0]: Sensor 1 SDE brightness step of Y right[23:16]
0x80207BAE	SNR1_SDE_YRIGHT_ STEP_M	0x00	RW	Bit[7:0]: Sensor 1 SDE brightness step of Y right[15:8]
0x80207BAF	SNR1_SDE_YRIGHT_ STEP_L	0x00	RW	Bit[7:0]: Sensor 1 SDE brightness step of Y right[7:0]
0x80207BB0	SNR1_SDE_YLEFT_H	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 SDE brightness Y left[12:8]
0x80207BB1	SNR1_SDE_YLEFT_L	0x00	RW	Bit[7:0]: Sensor 1 SDE brightness Y left[7:0]
0x80207BB2	SNR1_SDE_YRIGHT_H	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 SDE brightness Y right[12:8]
0x80207BB3	SNR1_SDE_YRIGHT_L	0x00	RW	Bit[7:0]: Sensor 1 SDE brightness Y right[7:0]
0x80207BB4	SNR1_SDE_SATU_U0	0x20	RW	Bit[7:0]: Sensor 1 SDE saturation U0
0x80207BB5	SNR1_SDE_SATU_V0	0x20	RW	Bit[7:0]: Sensor 1 SDE saturation V0
0x80207BB6	SNR1_SDE_SATU_U1	0x40	RW	Bit[7:0]: Sensor 1 SDE saturation U1

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table 4-46 SDE registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x80207BB7	SNR1_SDE_SATU_V1	0x40	RW	Bit[7:0]: Sensor 1 SDE saturation V1
0x80207BB8	SNR1_SDE_SATU_GAIN0	0x20	RW	Bit[7:0]: Sensor 1 SDE saturation gain0
0x80207BB9	SNR1_SDE_SATU_GAIN1	0x80	RW	Bit[7:0]: Sensor 1 SDE saturation gain1
0x80207BBA	SNR1_SDE_HUE_COS	0x01	RW	Bit[7:0]: Sensor 1 SDE hue cos
0x80207BBB	SNR1_SDE_HUE_SIN	0x00	RW	Bit[7:0]: Sensor 1 SDE hue sin
0x80207BBC	SNR1_SDE_XSKIP	0x01	RW	Bit[7:0]: Sensor 1 SDE X skip
0x80207BBD	SNR1_SDE_YMOVING_AVE_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 SDE Y moving average[11:8]
0x80207BBE	SNR1_SDE_YMOVING_AVE_L	0x00	RW	Bit[7:0]: Sensor 1 SDE Y moving average[7:0]
0x80207BBF	SNR1_SDE_INVWIDTH	0x00	RW	Bit[7:0]: Sensor 1 SDE inverse width (=(1<<16)/img_width)
0x80207BC0	SNR1_SDE_AVERAGE_IN_H	–	R	Bit[7:0]: Sensor 1 SDE average[15:8]
0x80207BC1	SNR1_SDE_AVERAGE_IN_L	–	R	Bit[7:0]: Sensor 1 SDE average[7:0]
0x80207BC2	SNR1_SDE_SAT_U_ADJUST_H	–	R	Bit[7:0]: Sensor 1 SDE saturation U adjust value[15:8]
0x80207BC3	SNR1_SDE_SAT_U_ADJUST_L	–	R	Bit[7:0]: Sensor 1 SDE saturation U adjust value[7:0]
0x80207BC4	SNR1_SDE_SAT_V_ADJUST_H	–	R	Bit[7:0]: Sensor 1 SDE saturation V adjust value[15:8]
0x80207BC5	SNR1_SDE_SAT_V_ADJUST_L	–	R	Bit[7:0]: Sensor 1 SDE saturation V adjust value[7:0]

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4.37 RAW stretch control

table 4-47 RAW stretch registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x80207800	SNR0_STRETCH_CTRL_0	0x09	RW	Bit[7:4]: Reserved Bit[3:2]: Sensor 0 stretch minimum number Bit[1:0]: Sensor 0 manual/auto low/high level select 10: Manual set low/high level Others:Auto calculated low/high level
0x80207801	SNR0_STRETCH_CTRL_1	0x06	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 stretch maximum low level
0x80207802	SNR0_STRETCH_CTRL_2	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 stretch minimum low level
0x80207803	SNR0_STRETCH_CTRL_3	0x10	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 stretch minimum high level
0x80207804	SNR0_STRETCH_CTRL_4	0x41	RW	Bit[7:4]: Sensor 0 stretch step2 value Bit[3:0]: Sensor 0 stretch step1 value
0x80207806	SNR0_STRETCH_CTRL_5	0xB0	RW	Bit[7:1]: Reserved Bit[0]: Sensor 0 stretch initial low level[8]
0x80207807	SNR0_STRETCH_CTRL_6	0x40	RW	Bit[7:0]: Sensor 0 stretch initial low level[7:0]
0x80207808	SNR0_STRETCH_CTRL_7	0x0F	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 stretch initial high level[11:8]
0x80207809	SNR0_STRETCH_CTRL_8	0xFC	RW	Bit[7:0]: Sensor 0 stretch initial high level[7:0]
0x8020780A	SNR0_STRETCH_CTRL_9	0x00	RW	Bit[7:1]: Reserved Bit[0]: Sensor 0 stretch manual low level[8]
0x8020780B	SNR0_STRETCH_CTRL_A	0x40	RW	Bit[7:0]: Sensor 0 stretch manual low level[7:0]

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table 4-47 RAW stretch registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x8020780C	SNR0_STRETCH_CTRL_B	0x0F	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 stretch manual high level[11:8]
0x8020780D	SNR0_STRETCH_CTRL_C	0xFC	RW	Bit[7:0]: Sensor 0 stretch manual high level[7:0]
0x8020780E	SNR0_STRETCH_CTRL_E	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 stretch threshold 1[20:16]
0x8020780F	SNR0_STRETCH_CTRL_F	0x3B	RW	Bit[7:0]: Sensor 0 stretch threshold 1[15:8]
0x80207810	SNR0_STRETCH_CTRL_10	0xC4	RW	Bit[7:0]: Sensor 0 stretch threshold 1[7:0]
0x80207811	SNR0_STRETCH_CTRL_11	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 stretch threshold 2[20:16]
0x80207812	SNR0_STRETCH_CTRL_12	0x3B	RW	Bit[7:0]: Sensor 0 stretch threshold 2[15:8]
0x80207813	SNR0_STRETCH_CTRL_13	0xC4	RW	Bit[7:0]: Sensor 0 stretch threshold 2[7:0]
0x80207814	SNR0_STRETCH_RO_LLV_H	–	R	Bit[7:1]: Reserved Bit[0]: Sensor 0 stretch current low level[8]
0x80207816	SNR0_STRETCH_RO_LLV_L	–	R	Bit[7:0]: Sensor 0 stretch current low level[7:0]
0x80207817	SNR0_STRETCH_RO_HLV_H	–	R	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 stretch current high level[11:8]
0x80207818	SNR0_STRETCH_RO_HLV_L	–	R	Bit[7:0]: Sensor 0 stretch current high level[7:0]
0x80207819	SNR0_STRETCH_RO_GAIN_H	–	R	Bit[7:1]: Reserved Bit[0]: Sensor 0 stretch gain[8]
0x8020781A	SNR0_STRETCH_RO_GAIN_L	–	R	Bit[7:0]: Sensor 0 stretch gain[7:0]

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table 4-47 RAW stretch registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x80207820	SNR1_STRETCH_CTRL_0	0x09	RW	Bit[7:4]: Reserved Bit[3:2]: Sensor 1 stretch minimum number Bit[1:0]: Sensor 1 manual/auto low/high level select 10: Manual set low/high level Others: Auto calculated low/high level
0x80207821	SNR1_STRETCH_CTRL_1	0x06	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 stretch maximum low level
0x80207822	SNR1_STRETCH_CTRL_2	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 stretch minimum low level
0x80207823	SNR1_STRETCH_CTRL_3	0x10	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 stretch minimum high level
0x80207824	SNR1_STRETCH_CTRL_4	0x41	RW	Bit[7:4]: Sensor 1 stretch step2 value Bit[3:0]: Sensor 1 stretch step1 value
0x80207826	SNR1_STRETCH_CTRL_5	0x00	RW	Bit[7:1]: Reserved Bit[0]: Sensor 1 stretch initial low level[8]
0x80207827	SNR1_STRETCH_CTRL_6	0x40	RW	Bit[7:0]: Sensor 1 stretch initial low level[7:0]
0x80207828	SNR1_STRETCH_CTRL_7	0x0F	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 stretch initial high level[11:8]
0x80207829	SNR1_STRETCH_CTRL_8	0xFC	RW	Bit[7:0]: Sensor 1 stretch initial high level[7:0]
0x8020782A	SNR1_STRETCH_CTRL_9	0x00	RW	Bit[7:1]: Reserved Bit[0]: Sensor 1 stretch manual low level[8]
0x8020782B	SNR1_STRETCH_CTRL_A	0x40	RW	Bit[7:0]: Sensor 1 stretch manual low level[7:0]
0x8020782C	SNR1_STRETCH_CTRL_B	0x0F	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 stretch manual high level[11:8]
0x8020782D	SNR1_STRETCH_CTRL_C	0xFC	RW	Bit[7:0]: Sensor 1 stretch manual high level[7:0]

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table 4-47 RAW stretch registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x8020782E	SNR1_STRETCH_CTRL_E	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 stretch threshold 1[20:16]
0x8020782F	SNR1_STRETCH_CTRL_F	0x3B	RW	Bit[7:0]: Sensor 1 stretch threshold 1[15:8]
0x80207830	SNR1_STRETCH_CTRL_10	0xC4	RW	Bit[7:0]: Sensor 1 stretch threshold 1[7:0]
0x80207831	SNR1_STRETCH_CTRL_11	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 stretch threshold 2[20:16]
0x80207832	SNR1_STRETCH_CTRL_12	0x3B	RW	Bit[7:0]: Sensor 1 stretch threshold 2[15:8]
0x80207833	SNR1_STRETCH_CTRL_13	0xC4	RW	Bit[7:0]: Sensor 1 stretch threshold 2[7:0]
0x80207834	SNR1_STRETCH_RO_LLV_H	–	R	Bit[7:1]: Reserved Bit[0]: Sensor 1 stretch current low level[8]
0x80207836	SNR1_STRETCH_RO_LLV_L	–	R	Bit[7:0]: Sensor 1 stretch current low level[7:0]
0x80207837	SNR1_STRETCH_RO_HLV_H	–	R	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 stretch current high level[11:8]
0x80207838	SNR1_STRETCH_RO_HLV_L	–	R	Bit[7:0]: Sensor 1 stretch current high level[7:0]
0x80207839	SNR1_STRETCH_RO_GAIN_H	–	R	Bit[7:1]: Reserved Bit[0]: Sensor 1 stretch gain[8]
0x8020783A	SNR1_STRETCH_RO_GAIN_L	–	R	Bit[7:0]: Sensor 1 stretch gain[7:0]

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4.38 tone mapping control

table 4-48 tone mapping registers (sheet 1 of 34)

address	register name	default value	R/W	description
0x80207400	SNR0_TMP_CTRL0	0x03	RW	Sensor 0 Tone Mapping Control Bit[7:5]: m_nGlobalMeanStatShift ROI statistic pixel selection 000: All pixels in ROI are used for statistics 001: 1/4 sample in both horizontal and vertical directions 010: 1/16 sample in both horizontal and vertical directions 011: 1/64 sample in both horizontal and vertical directions 100: 1/256 sample in both horizontal and vertical directions Others: Not supported Bit[4]: m_nGlobalMeanStatROIEnable 0: Use 4x4 window local statistics results to calculate globalmean 1: Use ROI to calculate globalmean Bit[3]: m_bLogHDRGainShiftEnable 0: Use log value direct from combine output 1: Add a shift value to compensate combine output log value Bit[2]: m_nFisheyeStatEnable 0: Statistics all the 4x4 windows with the same method 1: Use special method for statistics of 4 corner windows Bit[1]: m_bContrastBoost Bit[0]: m_bContrastEnable
0x80207401	SNR0_TMP_CTRL1	0x24	RW	Sensor 0 Tone Mapping Control Bit[7:0]: Reserved
0x80207402	SNR0_TMP_WIN_H_B1	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 sub-window height[10:8]

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table 4-48 tone mapping registers (sheet 2 of 34)

address	register name	default value	R/W	description
0x80207403	SNR0_TMP_WIN_H_B0	0x0E	RW	Bit[7:0]: Sensor 0 sub-window height[7:0]
0x80207404	SNR0_TMP_WIN_W_B1	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 sub-window width[11:8]
0x80207405	SNR0_TMP_WIN_W_B0	0xE0	RW	Bit[7:0]: Sensor 0 sub-window width[7:0]
0x80207406	SNR0_TMP_INV_WIN_H_B1	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 reciprocal of window height[13:8]
0x80207407	SNR0_TMP_INV_WIN_H_B0	0x3C	RW	Bit[7:0]: Sensor 0 reciprocal of window height[7:0]
0x80207408	SNR0_TMP_INV_WIN_W_B1	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 0 reciprocal of window width[13:8]
0x80207409	SNR0_TMP_INV_WIN_W_B0	0x22	RW	Bit[7:0]: Sensor 0 reciprocal of window width[7:0]
0x8020740A	SNR0_TMP_CTRL2	0x0A	RW	Bit[7:6]: Reserved Bit[5]: Sensor 0 manual set output raw bit enable 0: Use auto value from input port 1: Use manual value from internal register Bit[4:0]: Sensor 0 manual output raw bit
0x8020740B	SNR0_TMP_E_DITHER	0x02	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 dithering bits
0x8020740C	SNR0_TMP_ROI_TOP_B1	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 ROI top boundary line[10:8]
0x8020740D	SNR0_TMP_ROI_TOP_B0	0x10	RW	Bit[7:0]: Sensor 0 ROI top boundary line[7:0]
0x8020740E	SNR0_TMP_ROI_BOTTOM_B1	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 0 ROI bottom boundary line[10:8]
0x8020740F	SNR0_TMP_ROI_BOTTOM_B0	0x10	RW	Bit[7:0]: Sensor 0 ROI bottom boundary line[7:0]
0x80207410	SNR0_TMP_ROI_LEFT_B1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 ROI left boundary column[11:8]

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table 4-48 tone mapping registers (sheet 3 of 34)

address	register name	default value	R/W	description
0x80207411	SNR0_TMP_ROI_LEFT_B0	0x10	RW	Bit[7:0]: Sensor 0 ROI left boundary column[7:0]
0x80207412	SNR0_TMP_ROI_RIGHT_B1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 0 ROI right boundary column[11:8]
0x80207413	SNR0_TMP_ROI_RIGHT_B0	0x10	RW	Bit[7:0]: Sensor 0 ROI right boundary column[7:0]
0x80207414	SNR0_TMP_GLOBAL_ST_TH_B2	0x00	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 global mean statistic threshold[22:16]
0x80207415	SNR0_TMP_GLOBAL_ST_TH_B1	0x04	RW	Bit[7:0]: Sensor 0 global mean statistic threshold[15:8]
0x80207416	SNR0_TMP_GLOBAL_ST_TH_B0	0x00	RW	Bit[7:0]: Sensor 0 global mean statistic threshold[7:0]
0x80207417	SNR0_TMP_HDR_GAIN_SH_B1	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 log HDR gain shift[12:8]
0x80207418	SNR0_TMP_HDR_GAIN_SH_B0	0x00	RW	Bit[7:0]: Sensor 0 log HDR gain shift[7:0]
0x80207419	SNR0_TMP_CURVE_LIST_0_B1	0x50	RW	Bit[7:0]: Sensor 0 curve list 0[15:8]
0x8020741A	SNR0_TMP_CURVE_LIST_0_B0	0x00	RW	Bit[7:0]: Sensor 0 curve list 0[7:0]
0x8020741B	SNR0_TMP_CURVE_LIST_1_B1	0x70	RW	Bit[7:0]: Sensor 0 curve list 1[15:8]
0x8020741C	SNR0_TMP_CURVE_LIST_1_B0	0x00	RW	Bit[7:0]: Sensor 0 curve list 1[7:0]
0x8020741D	SNR0_TMP_CURVE_LIST_2_B1	0x78	RW	Bit[7:0]: Sensor 0 curve list 2[15:8]
0x8020741E	SNR0_TMP_CURVE_LIST_2_B0	0x00	RW	Bit[7:0]: Sensor 0 curve list 2[7:0]
0x8020741F	SNR0_TMP_CURVE_LIST_3_B1	0x80	RW	Bit[7:0]: Sensor 0 curve list 3[15:8]
0x80207420	SNR0_TMP_CURVE_LIST_3_B0	0x00	RW	Bit[7:0]: Sensor 0 curve list 3[7:0]
0x80207421	SNR0_TMP_CURVE_LIST_4_B1	0x88	RW	Bit[7:0]: Sensor 0 curve list 4[15:8]

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table 4-48 tone mapping registers (sheet 4 of 34)

address	register name	default value	R/W	description
0x80207422	SNR0_TMP_CURVE_LIST _4_B0	0x00	RW	Bit[7:0]: Sensor 0 curve list 4[7:0]
0x80207423	SNR0_TMP_CURVE_LIST _5_B1	0x8C	RW	Bit[7:0]: Sensor 0 curve list 5[15:8]
0x80207424	SNR0_TMP_CURVE_LIST _5_B0	0x00	RW	Bit[7:0]: Sensor 0 curve list 5[7:0]
0x80207425	SNR0_TMP_CURVE_LIST _6_B1	0x90	RW	Bit[7:0]: Sensor 0 curve list 6[15:8]
0x80207426	SNR0_TMP_CURVE_LIST _6_B0	0x00	RW	Bit[7:0]: Sensor 0 curve list 6[7:0]
0x80207427	SNR0_TMP_CURVE_LIST _7_B1	0x92	RW	Bit[7:0]: Sensor 0 curve list 7[15:8]
0x80207428	SNR0_TMP_CURVE_LIST _7_B0	0x00	RW	Bit[7:0]: Sensor 0 curve list 7[7:0]
0x80207429	SNR0_TMP_CURVE_LIST _8_B1	0x94	RW	Bit[7:0]: Sensor 0 curve list 8[15:8]
0x8020742A	SNR0_TMP_CURVE_LIST _8_B0	0x00	RW	Bit[7:0]: Sensor 0 curve list 8[7:0]
0x8020742B	SNR0_TMP_CURVE_LIST _9_B1	0x96	RW	Bit[7:0]: Sensor 0 curve list 9[15:8]
0x8020742C	SNR0_TMP_CURVE_LIST _9_B0	0x00	RW	Bit[7:0]: Sensor 0 curve list 9[7:0]
0x8020742D	SNR0_TMP_CURVE_LIST _A_B1	0x98	RW	Bit[7:0]: Sensor 0 curve list A[15:8]
0x8020742E	SNR0_TMP_CURVE_LIST _A_B0	0x00	RW	Bit[7:0]: Sensor 0 curve list A[7:0]
0x8020742F	SNR0_TMP_CURVE_LIST _B_B1	0x9A	RW	Bit[7:0]: Sensor 0 curve list B[15:8]
0x80207430	SNR0_TMP_CURVE_LIST _B_B0	0x00	RW	Bit[7:0]: Sensor 0 curve list B[7:0]
0x80207431	SNR0_TMP_CURVE_LIST _C_B1	0x9C	RW	Bit[7:0]: Sensor 0 curve list C[7:0]
0x80207432	SNR0_TMP_CURVE_LIST _C_B0	0x00	RW	Bit[7:0]: Sensor 0 curve list C[7:0]
0x80207433	SNR0_TMP_CURVE_LIST _D_B1	0x9E	RW	Bit[7:0]: Sensor 0 curve list D[15:8]
0x80207434	SNR0_TMP_CURVE_LIST _D_B0	0x00	RW	Bit[7:0]: Sensor 0 curve list D[7:0]

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table 4-48 tone mapping registers (sheet 5 of 34)

address	register name	default value	R/W	description
0x80207435	SNR0_TMP_CURVE_LIST _E_B1	0x9F	RW	Bit[7:0]: Sensor 0 curve list E[15:8]
0x80207436	SNR0_TMP_CURVE_LIST _E_B0	0x00	RW	Bit[7:0]: Sensor 0 curve list E[7:0]
0x80207437	SNR0_TMP_CURVE_LIST _F_B1	0x9F	RW	Bit[7:0]: Sensor 0 curve list F[15:8]
0x80207438	SNR0_TMP_CURVE_LIST _F_B0	0xFF	RW	Bit[7:0]: Sensor 0 curve list F[7:0]
0x80207440	SNR0_TMP_CONST_ CURVE_0_B1	0x50	RW	Bit[7:0]: Sensor 0 contrast curve 0[15:8]
0x80207441	SNR0_TMP_CONST_ CURVE_0_B0	0x00	RW	Bit[7:0]: Sensor 0 contrast curve 0[7:0]
0x80207442	SNR0_TMP_CONST_ CURVE_1_B1	0x70	RW	Bit[7:0]: Sensor 0 contrast curve 1[15:8]
0x80207443	SNR0_TMP_CONST_ CURVE_1_B0	0x00	RW	Bit[7:0]: Sensor 0 contrast curve 1[7:0]
0x80207444	SNR0_TMP_CONST_ CURVE_2_B1	0x78	RW	Bit[7:0]: Sensor 0 contrast curve 2[15:8]
0x80207445	SNR0_TMP_CONST_ CURVE_2_B0	0x00	RW	Bit[7:0]: Sensor 0 contrast curve 2[7:0]
0x80207446	SNR0_TMP_CONST_ CURVE_3_B1	0x80	RW	Bit[7:0]: Sensor 0 contrast curve 3[15:8]
0x80207447	SNR0_TMP_CONST_ CURVE_3_B0	0x00	RW	Bit[7:0]: Sensor 0 contrast curve 3[7:0]
0x80207448	SNR0_TMP_CONST_ CURVE_4_B1	0x88	RW	Bit[7:0]: Sensor 0 contrast curve 4[15:8]
0x80207449	SNR0_TMP_CONST_ CURVE_4_B0	0x00	RW	Bit[7:0]: Sensor 0 contrast curve 4[7:0]
0x8020744A	SNR0_TMP_CONST_ CURVE_5_B1	0x8C	RW	Bit[7:0]: Sensor 0 contrast curve 5[15:8]
0x8020744B	SNR0_TMP_CONST_ CURVE_5_B0	0x00	RW	Bit[7:0]: Sensor 0 contrast curve 5[7:0]
0x8020744C	SNR0_TMP_CONST_ CURVE_6_B1	0x90	RW	Bit[7:0]: Sensor 0 contrast curve 6[15:8]
0x8020744D	SNR0_TMP_CONST_ CURVE_6_B0	0x00	RW	Bit[7:0]: Sensor 0 contrast curve 6[7:0]
0x8020744E	SNR0_TMP_CONST_ CURVE_7_B1	0x92	RW	Bit[7:0]: Sensor 0 contrast curve 7[15:8]

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table 4-48 tone mapping registers (sheet 6 of 34)

address	register name	default value	R/W	description
0x8020744F	SNR0_TMP_CONST_CURVE_7_B0	0x00	RW	Bit[7:0]: Sensor 0 contrast curve 7[7:0]
0x80207450	SNR0_TMP_CONST_CURVE_8_B1	0x94	RW	Bit[7:0]: Sensor 0 contrast curve 8[15:8]
0x80207451	SNR0_TMP_CONST_CURVE_8_B0	0x00	RW	Bit[7:0]: Sensor 0 contrast curve 8[7:0]
0x80207452	SNR0_TMP_CONST_CURVE_9_B1	0x96	RW	Bit[7:0]: Sensor 0 contrast curve 9[15:8]
0x80207453	SNR0_TMP_CONST_CURVE_9_B0	0x00	RW	Bit[7:0]: Sensor 0 contrast curve 9[7:0]
0x80207454	SNR0_TMP_CONST_CURVE_A_B1	0x98	RW	Bit[7:0]: Sensor 0 contrast curve A[15:8]
0x80207455	SNR0_TMP_CONST_CURVE_A_B0	0x00	RW	Bit[7:0]: Sensor 0 contrast curve A[7:0]
0x80207456	SNR0_TMP_CONST_CURVE_B_B1	0x9A	RW	Bit[7:0]: Sensor 0 contrast curve B[15:8]
0x80207457	SNR0_TMP_CONST_CURVE_B_B0	0x00	RW	Bit[7:0]: Sensor 0 contrast curve B[7:0]
0x80207458	SNR0_TMP_CONST_CURVE_C_B1	0x9C	RW	Bit[7:0]: Sensor 0 contrast curve C[15:8]
0x80207459	SNR0_TMP_CONST_CURVE_C_B0	0x00	RW	Bit[7:0]: Sensor 0 contrast curve C[7:0]
0x8020745A	SNR0_TMP_CONST_CURVE_D_B1	0x9E	RW	Bit[7:0]: Sensor 0 contrast curve D[15:8]
0x8020745B	SNR0_TMP_CONST_CURVE_D_B0	0x00	RW	Bit[7:0]: Sensor 0 contrast curve D[7:0]
0x8020745C	SNR0_TMP_CONST_CURVE_E_B1	0x9F	RW	Bit[7:0]: Sensor 0 contrast curve E[15:8]
0x8020745D	SNR0_TMP_CONST_CURVE_E_B0	0x00	RW	Bit[7:0]: Sensor 0 contrast curve E[7:0]
0x8020745E	SNR0_TMP_CONST_CURVE_F_B1	0x9F	RW	Bit[7:0]: Sensor 0 contrast curve F[15:8]
0x8020745F	SNR0_TMP_CONST_CURVE_F_B0	0xFF	RW	Bit[7:0]: Sensor 0 contrast curve F[7:0]
0x80207460	SNR0_TMP_GAMMA_GAIN_00_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 00[9:8]

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table 4-48 tone mapping registers (sheet 7 of 34)

address	register name	default value	R/W	description
0x80207461	SNR0_TMP_GAMMA_GAIN_00_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 00[7:0]
0x80207462	SNR0_TMP_GAMMA_GAIN_01_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 01[9:8]
0x80207463	SNR0_TMP_GAMMA_GAIN_01_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 01[7:0]
0x80207464	SNR0_TMP_GAMMA_GAIN_02_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 02[9:8]
0x80207465	SNR0_TMP_GAMMA_GAIN_02_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 02[7:0]
0x80207466	SNR0_TMP_GAMMA_GAIN_03_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 03[9:8]
0x80207467	SNR0_TMP_GAMMA_GAIN_03_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 03[7:0]
0x80207468	SNR0_TMP_GAMMA_GAIN_04_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 04[9:8]
0x80207469	SNR0_TMP_GAMMA_GAIN_04_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 04[7:0]
0x8020746A	SNR0_TMP_GAMMA_GAIN_10_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 10[9:8]
0x8020746B	SNR0_TMP_GAMMA_GAIN_10_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 10[7:0]
0x8020746C	SNR0_TMP_GAMMA_GAIN_11_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 11[9:8]
0x8020746D	SNR0_TMP_GAMMA_GAIN_11_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 11[7:0]
0x8020746E	SNR0_TMP_GAMMA_GAIN_12_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 12[9:8]
0x8020746F	SNR0_TMP_GAMMA_GAIN_12_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 12[7:0]
0x80207470	SNR0_TMP_GAMMA_GAIN_13_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 13[9:8]

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table 4-48 tone mapping registers (sheet 8 of 34)

address	register name	default value	R/W	description
0x80207471	SNR0_TMP_GAMMA_GAIN_13_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 13[7:0]
0x80207472	SNR0_TMP_GAMMA_GAIN_14_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 14[9:8]
0x80207473	SNR0_TMP_GAMMA_GAIN_14_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 14[7:0]
0x80207474	SNR0_TMP_GAMMA_GAIN_20_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 20[9:8]
0x80207475	SNR0_TMP_GAMMA_GAIN_20_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 20[7:0]
0x80207476	SNR0_TMP_GAMMA_GAIN_21_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 21[9:8]
0x80207477	SNR0_TMP_GAMMA_GAIN_21_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 21[7:0]
0x80207478	SNR0_TMP_GAMMA_GAIN_22_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 22[9:8]
0x80207479	SNR0_TMP_GAMMA_GAIN_22_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 22[7:0]
0x8020747A	SNR0_TMP_GAMMA_GAIN_23_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 23[9:8]
0x8020747B	SNR0_TMP_GAMMA_GAIN_23_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 23[7:0]
0x8020747C	SNR0_TMP_GAMMA_GAIN_24_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 24[9:8]
0x8020747D	SNR0_TMP_GAMMA_GAIN_24_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 24[7:0]
0x8020747E	SNR0_TMP_GAMMA_GAIN_30_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 30[9:8]
0x8020747F	SNR0_TMP_GAMMA_GAIN_30_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 30[7:0]
0x80207480	SNR0_TMP_GAMMA_GAIN_31_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 31[9:8]

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table 4-48 tone mapping registers (sheet 9 of 34)

address	register name	default value	R/W	description
0x80207481	SNR0_TMP_GAMMA_GAIN_31_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 31[7:0]
0x80207482	SNR0_TMP_GAMMA_GAIN_32_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 32[9:8]
0x80207483	SNR0_TMP_GAMMA_GAIN_32_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 32[7:0]
0x80207484	SNR0_TMP_GAMMA_GAIN_33_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 33[9:8]
0x80207485	SNR0_TMP_GAMMA_GAIN_33_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 33[7:0]
0x80207486	SNR0_TMP_GAMMA_GAIN_34_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 34[9:8]
0x80207487	SNR0_TMP_GAMMA_GAIN_34_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 34[7:0]
0x80207488	SNR0_TMP_GAMMA_GAIN_40_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 40[9:8]
0x80207489	SNR0_TMP_GAMMA_GAIN_40_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 40[7:0]
0x8020748A	SNR0_TMP_GAMMA_GAIN_41_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 41[9:8]
0x8020748B	SNR0_TMP_GAMMA_GAIN_41_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 41[7:0]
0x8020748C	SNR0_TMP_GAMMA_GAIN_42_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 42[9:8]
0x8020748D	SNR0_TMP_GAMMA_GAIN_42_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 42[7:0]
0x8020748E	SNR0_TMP_GAMMA_GAIN_43_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 43[9:8]
0x8020748F	SNR0_TMP_GAMMA_GAIN_43_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 43[7:0]
0x80207490	SNR0_TMP_GAMMA_GAIN_44_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 gamma gain of window 44[9:8]

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table 4-48 tone mapping registers (sheet 10 of 34)

address	register name	default value	R/W	description
0x80207491	SNR0_TMP_GAMMA_GAIN_44_B0	0xFF	RW	Bit[7:0]: Sensor 0 gamma gain of window 44[7:0]
0x80207492	SNR0_TMP_GLOBAL_GAIN_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 global gamma gain[9:8]
0x80207493	SNR0_TMP_GLOBAL_GAIN_B0	0xFF	RW	Bit[7:0]: Sensor 0 global gamma gain[7:0]
0x80207494	SNR0_TMP_LOG_GAIN_B1	0x00	RW	Bit[7]: Reserved Bit[6:0]: Sensor 0 expect log gamma gain[14:8]
0x80207495	SNR0_TMP_LOG_GAIN_B0	0x00	RW	Bit[7:0]: Sensor 0 expect log gamma gain[7:0]
0x80207496	SNR0_TMP_LOG_MAX_B1	0x4F	RW	Bit[7:0]: Sensor 0 log max value[15:8]
0x80207497	SNR0_TMP_LOG_MAX_B0	0xFF	RW	Bit[7:0]: Sensor 0 log max value[7:0]
0x80207498	SNR0_TMP_Y_TH0_B1	0x00	RW	Bit[7:0]: Sensor 0 Y threshold 0[15:8]
0x80207499	SNR0_TMP_Y_TH0_B0	0x00	RW	Bit[7:0]: Sensor 0 Y threshold 0[7:0]
0x8020749A	SNR0_TMP_Y_TH1_B1	0x00	RW	Bit[7:0]: Sensor 0 Y threshold 1[15:8]
0x8020749B	SNR0_TMP_Y_TH1_B0	0x00	RW	Bit[7:0]: Sensor 0 Y threshold 1[7:0]
0x8020749C	SNR0_TMP_Y_TH2_B1	0x00	RW	Bit[7:0]: Sensor 0 Y threshold 2[15:8]
0x8020749D	SNR0_TMP_Y_TH2_B0	0x00	RW	Bit[7:0]: Sensor 0 Y threshold 2[7:0]
0x8020749E	SNR0_TMP_Y_TH3_B1	0x00	RW	Bit[7:0]: Sensor 0 Y threshold 3[15:8]
0x8020749F	SNR0_TMP_Y_TH3_B0	0x00	RW	Bit[7:0]: Sensor 0 Y threshold 3[7:0]
0x802074A1	SNR0_TMP_Y_TH0TH1_B2	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 th0/th1 difference[17:16]
0x802074A2	SNR0_TMP_Y_TH0TH1_B1	0x00	RW	Bit[7:0]: Sensor 0 th0/th1 difference[15:8]
0x802074A3	SNR0_TMP_Y_TH0TH1_B0	0x00	RW	Bit[7:0]: Sensor 0 th0/th1 difference[7:0]
0x802074A5	SNR0_TMP_Y_TH2TH3_B2	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 0 th2/th3 difference[17:16]
0x802074A6	SNR0_TMP_Y_TH2TH3_B1	0x00	RW	Bit[7:0]: Sensor 0 th2/th3 difference[15:8]

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table 4-48 tone mapping registers (sheet 11 of 34)

address	register name	default value	R/W	description
0x802074A7	SNR0_TMP_Y_TH2TH3_B0	0x00	RW	Bit[7:0]: Sensor 0 th2/th3 difference[7:0]
0x802074B0	SNR0_TMP_LOCAL_MEAN_0_B1	–	R	Bit[7:0]: Sensor 0 local mean value for window 0[15:8]
0x802074B1	SNR0_TMP_LOCAL_MEAN_0_B0	–	R	Bit[7:0]: Sensor 0 local mean value for window 0[7:0]
0x802074B2	SNR0_TMP_LOCAL_MEAN_1_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 1[15:8]
0x802074B3	SNR0_TMP_LOCAL_MEAN_1_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 1[7:0]
0x802074B4	SNR0_TMP_LOCAL_MEAN_2_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 2[15:8]
0x802074B5	SNR0_TMP_LOCAL_MEAN_2_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 2[7:0]
0x802074B6	SNR0_TMP_LOCAL_MEAN_3_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 3[15:8]
0x802074B7	SNR0_TMP_LOCAL_MEAN_3_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 3[7:0]
0x802074B8	SNR0_TMP_LOCAL_MEAN_4_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 4[15:8]
0x802074B9	SNR0_TMP_LOCAL_MEAN_4_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 4[7:0]
0x802074BA	SNR0_TMP_LOCAL_MEAN_5_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 5[15:8]
0x802074BB	SNR0_TMP_LOCAL_MEAN_5_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 5[7:0]
0x802074BC	SNR0_TMP_LOCAL_MEAN_6_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 6[15:8]
0x802074BD	SNR0_TMP_LOCAL_MEAN_6_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 6[7:0]
0x802074BE	SNR0_TMP_LOCAL_MEAN_7_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 7[15:8]
0x802074BF	SNR0_TMP_LOCAL_MEAN_7_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 7[7:0]
0x802074C0	SNR0_TMP_LOCAL_MEAN_8_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 8[15:8]
0x802074C1	SNR0_TMP_LOCAL_MEAN_8_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 8[7:0]

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table 4-48 tone mapping registers (sheet 12 of 34)

address	register name	default value	R/W	description
0x802074C2	SNR0_TMP_LOCAL_MEAN_9_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 9[15:8]
0x802074C3	SNR0_TMP_LOCAL_MEAN_9_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 9[7:0]
0x802074C4	SNR0_TMP_LOCAL_MEAN_10_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 10[15:8]
0x802074C5	SNR0_TMP_LOCAL_MEAN_10_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 10[7:0]
0x802074C6	SNR0_TMP_LOCAL_MEAN_11_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 11[15:8]
0x802074C7	SNR0_TMP_LOCAL_MEAN_11_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 11[7:0]
0x802074C8	SNR0_TMP_LOCAL_MEAN_12_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 12[15:8]
0x802074C9	SNR0_TMP_LOCAL_MEAN_12_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 12[7:0]
0x802074CA	SNR0_TMP_LOCAL_MEAN_13_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 13[15:8]
0x802074CB	SNR0_TMP_LOCAL_MEAN_13_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 13[7:0]
0x802074CC	SNR0_TMP_LOCAL_MEAN_14_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 14[15:8]
0x802074CD	SNR0_TMP_LOCAL_MEAN_14_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 14[7:0]
0x802074CE	SNR0_TMP_LOCAL_MEAN_15_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 15[15:8]
0x802074CF	SNR0_TMP_LOCAL_MEAN_15_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 15[7:0]
0x802074D0	SNR0_TMP_LOCAL_MEAN_16_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 16[15:8]
0x802074D1	SNR0_TMP_LOCAL_MEAN_16_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 16[7:0]
0x802074D2	SNR0_TMP_LOCAL_MEAN_17_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 17[15:8]
0x802074D3	SNR0_TMP_LOCAL_MEAN_17_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 17[7:0]
0x802074D4	SNR0_TMP_LOCAL_MEAN_18_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 18[15:8]

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table 4-48 tone mapping registers (sheet 13 of 34)

address	register name	default value	R/W	description
0x802074D5	SNR0_TMP_LOCAL_MEAN_18_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 18[7:0]
0x802074D6	SNR0_TMP_LOCAL_MEAN_19_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 19[15:8]
0x802074D7	SNR0_TMP_LOCAL_MEAN_19_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 19[7:0]
0x802074D8	SNR0_TMP_LOCAL_MEAN_20_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 20[15:8]
0x802074D9	SNR0_TMP_LOCAL_MEAN_20_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 20[7:0]
0x802074DA	SNR0_TMP_LOCAL_MEAN_21_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 21[15:8]
0x802074DB	SNR0_TMP_LOCAL_MEAN_21_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 21[7:0]
0x802074DC	SNR0_TMP_LOCAL_MEAN_22_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 22[15:8]
0x802074DD	SNR0_TMP_LOCAL_MEAN_22_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 22[7:0]
0x802074DE	SNR0_TMP_LOCAL_MEAN_23_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 23[15:8]
0x802074DF	SNR0_TMP_LOCAL_MEAN_23_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 23[7:0]
0x802074E0	SNR0_TMP_LOCAL_MEAN_24_B1	–	R	Bit[7:0]: Sensor 0 local mean for window 24[15:8]
0x802074E1	SNR0_TMP_LOCAL_MEAN_24_B0	–	R	Bit[7:0]: Sensor 0 local mean for window 24[7:0]
0x802074E2	SNR0_TMP_GLOBAL_MEAN_B1	–	R	Bit[7:0]: Sensor 0 global mean value[15:8]
0x802074E3	SNR0_TMP_GLOBAL_MEAN_B0	–	R	Bit[7:0]: Sensor 0 global mean value[7:0]
0x802074E4	SNR0_TMP_NORMALIZE_LOG_MEAN_B1	–	R	Bit[7:0]: Sensor 0 normalize mean value[15:8]
0x802074E5	SNR0_TMP_NORMALIZE_LOG_MEAN_B0	–	R	Bit[7:0]: Sensor 0 normalize mean value[7:0]
0x802074E8	SNR0_TMP_HIST_0_B3	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 0[31:24]
0x802074E9	SNR0_TMP_HIST_0_B2	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 0[23:16]

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table 4-48 tone mapping registers (sheet 14 of 34)

address	register name	default value	R/W	description
0x802074EA	SNR0_TMP_HIST_0_B1	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 0[15:8]
0x802074EB	SNR0_TMP_HIST_0_B0	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 0[7:0]
0x802074EC	SNR0_TMP_HIST_1_B3	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 1[31:24]
0x802074ED	SNR0_TMP_HIST_1_B2	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 1[23:16]
0x802074EE	SNR0_TMP_HIST_1_B1	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 1[15:8]
0x802074EF	SNR0_TMP_HIST_1_B0	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 1[7:0]
0x802074F0	SNR0_TMP_HIST_2_B3	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 2[31:24]
0x802074F1	SNR0_TMP_HIST_2_B2	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 2[23:16]
0x802074F2	SNR0_TMP_HIST_2_B1	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 2[15:8]
0x802074F3	SNR0_TMP_HIST_2_B0	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 2[7:0]
0x802074F4	SNR0_TMP_HIST_3_B3	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 3[31:24]
0x802074F5	SNR0_TMP_HIST_3_B2	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 3[23:16]
0x802074F6	SNR0_TMP_HIST_3_B1	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 3[15:8]
0x802074F7	SNR0_TMP_HIST_3_B0	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 3[7:0]
0x802074F8	SNR0_TMP_HIST_4_B3	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 4[31:24]
0x802074F9	SNR0_TMP_HIST_4_B2	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 4[23:16]
0x802074FA	SNR0_TMP_HIST_4_B1	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 4[15:8]
0x802074FB	SNR0_TMP_HIST_4_B0	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 4[7:0]
0x802074FC	SNR0_TMP_HIST_5_B3	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 5[31:24]

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table 4-48 tone mapping registers (sheet 15 of 34)

address	register name	default value	R/W	description
0x802074FD	SNR0_TMP_HIST_5_B2	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 5[23:16]
0x802074FE	SNR0_TMP_HIST_5_B1	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 5[15:8]
0x802074FF	SNR0_TMP_HIST_5_B0	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 5[7:0]
0x80207500	SNR0_TMP_HIST_6_B3	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 6[31:24]
0x80207501	SNR0_TMP_HIST_6_B2	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 6[23:16]
0x80207502	SNR0_TMP_HIST_6_B1	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 6[15:8]
0x80207503	SNR0_TMP_HIST_6_B0	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 6[7:0]
0x80207504	SNR0_TMP_HIST_7_B3	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 7[31:24]
0x80207505	SNR0_TMP_HIST_7_B2	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 7[23:16]
0x80207506	SNR0_TMP_HIST_7_B1	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 7[15:8]
0x80207507	SNR0_TMP_HIST_7_B0	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 7[7:0]
0x80207508	SNR0_TMP_HIST_8_B3	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 8[31:24]
0x80207509	SNR0_TMP_HIST_8_B2	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 8[23:16]
0x8020750A	SNR0_TMP_HIST_8_B1	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 8[15:8]
0x8020750B	SNR0_TMP_HIST_8_B0	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 8[7:0]
0x8020750C	SNR0_TMP_HIST_9_B3	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 9[31:24]
0x8020750D	SNR0_TMP_HIST_9_B2	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 9[23:16]
0x8020750E	SNR0_TMP_HIST_9_B1	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 9[15:8]
0x8020750F	SNR0_TMP_HIST_9_B0	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 9[7:0]

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table 4-48 tone mapping registers (sheet 16 of 34)

address	register name	default value	R/W	description
0x80207510	SNR0_TMP_HIST_10_B3	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 10[31:24]
0x80207511	SNR0_TMP_HIST_10_B2	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 10[23:16]
0x80207512	SNR0_TMP_HIST_10_B1	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 10[15:8]
0x80207513	SNR0_TMP_HIST_10_B0	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 10[7:0]
0x80207514	SNR0_TMP_HIST_11_B3	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 11[31:24]
0x80207515	SNR0_TMP_HIST_11_B2	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 11[23:16]
0x80207516	SNR0_TMP_HIST_11_B1	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 11[15:8]
0x80207517	SNR0_TMP_HIST_11_B0	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 11[7:0]
0x80207518	SNR0_TMP_HIST_12_B3	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 12[31:24]
0x80207519	SNR0_TMP_HIST_12_B2	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 12[23:16]
0x8020751A	SNR0_TMP_HIST_12_B1	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 12[15:8]
0x8020751B	SNR0_TMP_HIST_12_B0	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 12[7:0]
0x8020751C	SNR0_TMP_HIST_13_B3	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 13[31:24]
0x8020751D	SNR0_TMP_HIST_13_B2	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 13[23:16]
0x8020751E	SNR0_TMP_HIST_13_B1	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 13[15:8]
0x8020751F	SNR0_TMP_HIST_13_B0	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 13[7:0]
0x80207520	SNR0_TMP_HIST_14_B3	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 14[31:24]
0x80207521	SNR0_TMP_HIST_14_B2	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 14[23:16]
0x80207522	SNR0_TMP_HIST_14_B1	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 14[15:8]

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table 4-48 tone mapping registers (sheet 17 of 34)

address	register name	default value	R/W	description
0x80207523	SNR0_TMP_HIST_14_B0	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 14[7:0]
0x80207524	SNR0_TMP_HIST_15_B3	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 15[31:24]
0x80207525	SNR0_TMP_HIST_15_B2	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 15[23:16]
0x80207526	SNR0_TMP_HIST_15_B1	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 15[15:8]
0x80207527	SNR0_TMP_HIST_15_B0	–	R	Bit[7:0]: Sensor 0 log curve histogram segment 15[7:0]

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table 4-48 tone mapping registers (sheet 18 of 34)

address	register name	default value	R/W	description
0x80207600	SNR1_TMP_CTRL0	0x03	RW	Sensor 1 Tone Mapping Control Bit[7:5]: m_nGlobalMeanStatShift ROI statistic pixel selection 000: All pixels in ROI are used for statistics 001: 1/4 sample in both horizontal and vertical directions 010: 1/16 sample in both horizontal and vertical directions 011: 1/64 sample in both horizontal and vertical directions 100: 1/256 sample in both horizontal and vertical directions Others: Not supported Bit[4]: m_nGlobalMeanStatROIEnable 0: Use 4x4 window local statistics results to calculate globalmean 1: Use ROI to calculate globalmean Bit[3]: m_bLogHDRGainShiftEnable 0: Use log value direct from combine output 1: Add a shift value to compensate combine output log value Bit[2]: m_nFisheyeStatEnable 0: Statistics all the 4x4 windows with the same method 1: Use special method for statistics of 4 corner windows Bit[1]: m_bContrastBoost Bit[0]: m_bContrastEnable
0x80207601	SNR1_TMP_CTRL1	0x24	RW	Sensor 1 Tone Mapping Control Bit[7:0]: Reserved
0x80207602	SNR1_TMP_WIN_H_B1	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 sub-window height[10:8]
0x80207603	SNR1_TMP_WIN_H_B0	0x0E	RW	Bit[7:0]: Sensor 1 sub-window height[7:0]

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table 4-48 tone mapping registers (sheet 19 of 34)

address	register name	default value	R/W	description
0x80207604	SNR1_TMP_WIN_W_B1	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 sub-window width[11:8]
0x80207605	SNR1_TMP_WIN_W_B0	0xE0	RW	Bit[7:0]: Sensor 1 sub-window width[7:0]
0x80207606	SNR1_TMP_INV_WIN_H_B1	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 reciprocal of window height[13:8]
0x80207607	SNR1_TMP_INV_WIN_H_B0	0x3C	RW	Bit[7:0]: Sensor 1 reciprocal of window height[7:0]
0x80207608	SNR1_TMP_INV_WIN_W_B1	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Sensor 1 reciprocal of window width[13:8]
0x80207609	SNR1_TMP_INV_WIN_W_B0	0x22	RW	Bit[7:0]: Sensor 1 reciprocal of window width[7:0]
0x8020760A	SNR1_TMP_CTRL2	0x0A	RW	Bit[7:6]: Reserved Bit[5]: Sensor 1 manual set output raw bit enable 0: Use auto value from input port 1: Use manual value from internal register Bit[4:0]: Sensor 1 manual output raw bit
0x8020760B	SNR1_TMP_E_DITHER	0x02	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 dithering bits
0x8020760C	SNR1_TMP_ROI_TOP_B1	0x00	RW	Bit[7:2]: Reserved Bit[2:0]: Sensor 1 ROI top boundary line[10:8]
0x8020760D	SNR1_TMP_ROI_TOP_B0	0x10	RW	Bit[7:0]: Sensor 1 ROI top boundary line[7:0]
0x8020760E	SNR1_TMP_ROI_BOTTOM_B1	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Sensor 1 ROI bottom boundary line[10:8]
0x8020760F	SNR1_TMP_ROI_BOTTOM_B0	0x10	RW	Bit[7:0]: Sensor 1 ROI bottom boundary line[7:0]
0x80207610	SNR1_TMP_ROI_LEFT_B1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 ROI left boundary column[11:8]
0x80207611	SNR1_TMP_ROI_LEFT_B0	0x10	RW	Bit[7:0]: Sensor 1 ROI left boundary column[7:0]

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table 4-48 tone mapping registers (sheet 20 of 34)

address	register name	default value	R/W	description
0x80207612	SNR1_TMP_ROI_RIGHT_B1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Sensor 1 ROI right boundary column[11:8]
0x80207613	SNR1_TMP_ROI_RIGHT_B0	0x10	RW	Bit[7:0]: Sensor 1 ROI right boundary column[7:0]
0x80207614	SNR1_TMP_GLOBAL_ST_TH_B2	0x00	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 global mean statistic threshold[22:16]
0x80207615	SNR1_TMP_GLOBAL_ST_TH_B1	0x04	RW	Bit[7:0]: Sensor 1 global mean statistic threshold[15:8]
0x80207616	SNR1_TMP_GLOBAL_ST_TH_B0	0x00	RW	Bit[7:0]: Sensor 1 global mean statistic threshold[7:0]
0x80207617	SNR1_TMP_HDR_GAIN_SH_B1	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 log HDR gain shift[12:8]
0x80207618	SNR1_TMP_HDR_GAIN_SH_B0	0x00	RW	Bit[7:0]: Sensor 1 log HDR gain shift[7:0]
0x80207619	SNR1_TMP_CURVE_LIST_0_B1	0x50	RW	Bit[7:0]: Sensor 1 curve list 0[15:8]
0x8020761A	SNR1_TMP_CURVE_LIST_0_B0	0x00	RW	Bit[7:0]: Sensor 1 curve list 0[7:0]
0x8020761B	SNR1_TMP_CURVE_LIST_1_B1	0x70	RW	Bit[7:0]: Sensor 1 curve list 1[15:8]
0x8020761C	SNR1_TMP_CURVE_LIST_1_B0	0x00	RW	Bit[7:0]: Sensor 1 curve list 1[7:0]
0x8020761D	SNR1_TMP_CURVE_LIST_2_B1	0x78	RW	Bit[7:0]: Sensor 1 curve list 2[15:8]
0x8020761E	SNR1_TMP_CURVE_LIST_2_B0	0x00	RW	Bit[7:0]: Sensor 1 curve list 2[7:0]
0x8020761F	SNR1_TMP_CURVE_LIST_3_B1	0x80	RW	Bit[7:0]: Sensor 1 curve list 3[15:8]
0x80207620	SNR1_TMP_CURVE_LIST_3_B0	0x00	RW	Bit[7:0]: Sensor 1 curve list 3[7:0]
0x80207621	SNR1_TMP_CURVE_LIST_4_B1	0x88	RW	Bit[7:0]: Sensor 1 curve list 4[15:8]
0x80207622	SNR1_TMP_CURVE_LIST_4_B0	0x00	RW	Bit[7:0]: Sensor 1 curve list 4[7:0]

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table 4-48 tone mapping registers (sheet 21 of 34)

address	register name	default value	R/W	description
0x80207623	SNR1_TMP_CURVE_LIST _5_B1	0x8C	RW	Bit[7:0]: Sensor 1 curve list 5[15:8]
0x80207624	SNR1_TMP_CURVE_LIST _5_B0	0x00	RW	Bit[7:0]: Sensor 1 curve list 5[7:0]
0x80207625	SNR1_TMP_CURVE_LIST _6_B1	0x90	RW	Bit[7:0]: Sensor 1 curve list 6[15:8]
0x80207626	SNR1_TMP_CURVE_LIST _6_B0	0x00	RW	Bit[7:0]: Sensor 1 curve list 6[7:0]
0x80207627	SNR1_TMP_CURVE_LIST _7_B1	0x92	RW	Bit[7:0]: Sensor 1 curve list 7[15:8]
0x80207628	SNR1_TMP_CURVE_LIST _7_B0	0x00	RW	Bit[7:0]: Sensor 1 curve list 7[7:0]
0x80207629	SNR1_TMP_CURVE_LIST _8_B1	0x94	RW	Bit[7:0]: Sensor 1 curve list 8[15:8]
0x8020762A	SNR1_TMP_CURVE_LIST _8_B0	0x00	RW	Bit[7:0]: Sensor 1 curve list 8[7:0]
0x8020762B	SNR1_TMP_CURVE_LIST _9_B1	0x96	RW	Bit[7:0]: Sensor 1 curve list 9[15:8]
0x8020762C	SNR1_TMP_CURVE_LIST _9_B0	0x00	RW	Bit[7:0]: Sensor 1 curve list 9[7:0]
0x8020762D	SNR1_TMP_CURVE_LIST _A_B1	0x98	RW	Bit[7:0]: Sensor 1 curve list A[15:8]
0x8020762E	SNR1_TMP_CURVE_LIST _A_B0	0x00	RW	Bit[7:0]: Sensor 1 curve list A[7:0]
0x8020762F	SNR1_TMP_CURVE_LIST _B_B1	0x9A	RW	Bit[7:0]: Sensor 1 curve list B[15:8]
0x80207630	SNR1_TMP_CURVE_LIST _B_B0	0x00	RW	Bit[7:0]: Sensor 1 curve list B[7:0]
0x80207631	SNR1_TMP_CURVE_LIST _C_B1	0x9C	RW	Bit[7:0]: Sensor 1 curve list C[7:0]
0x80207632	SNR1_TMP_CURVE_LIST _C_B0	0x00	RW	Bit[7:0]: Sensor 1 curve list C[7:0]
0x80207633	SNR1_TMP_CURVE_LIST _D_B1	0x9E	RW	Bit[7:0]: Sensor 1 curve list D[15:8]
0x80207634	SNR1_TMP_CURVE_LIST _D_B0	0x00	RW	Bit[7:0]: Sensor 1 curve list D[7:0]
0x80207635	SNR1_TMP_CURVE_LIST _E_B1	0x9F	RW	Bit[7:0]: Sensor 1 curve list E[15:8]

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table 4-48 tone mapping registers (sheet 22 of 34)

address	register name	default value	R/W	description
0x80207636	SNR1_TMP_CURVE_LIST _E_B0	0x00	RW	Bit[7:0]: Sensor 1 curve list E[7:0]
0x80207637	SNR1_TMP_CURVE_LIST _F_B1	0x9F	RW	Bit[7:0]: Sensor 1 curve list F[15:8]
0x80207638	SNR1_TMP_CURVE_LIST _F_B0	0xFF	RW	Bit[7:0]: Sensor 1 curve list F[7:0]
0x80207640	SNR1_TMP_CONST_ CURVE_0_B1	0x50	RW	Bit[7:0]: Sensor 1 contrast curve 0[15:8]
0x80207641	SNR1_TMP_CONST_ CURVE_0_B0	0x00	RW	Bit[7:0]: Sensor 1 contrast curve 0[7:0]
0x80207642	SNR1_TMP_CONST_ CURVE_1_B1	0x70	RW	Bit[7:0]: Sensor 1 contrast curve 1[15:8]
0x80207643	SNR1_TMP_CONST_ CURVE_1_B0	0x00	RW	Bit[7:0]: Sensor 1 contrast curve 1[7:0]
0x80207644	SNR1_TMP_CONST_ CURVE_2_B1	0x78	RW	Bit[7:0]: Sensor 1 contrast curve 2[15:8]
0x80207645	SNR1_TMP_CONST_ CURVE_2_B0	0x00	RW	Bit[7:0]: Sensor 1 contrast curve 2[7:0]
0x80207646	SNR1_TMP_CONST_ CURVE_3_B1	0x80	RW	Bit[7:0]: Sensor 1 contrast curve 3[15:8]
0x80207647	SNR1_TMP_CONST_ CURVE_3_B0	0x00	RW	Bit[7:0]: Sensor 1 contrast curve 3[7:0]
0x80207648	SNR1_TMP_CONST_ CURVE_4_B1	0x88	RW	Bit[7:0]: Sensor 1 contrast curve 4[15:8]
0x80207649	SNR1_TMP_CONST_ CURVE_4_B0	0x00	RW	Bit[7:0]: Sensor 1 contrast curve 4[7:0]
0x8020764A	SNR1_TMP_CONST_ CURVE_5_B1	0x8C	RW	Bit[7:0]: Sensor 1 contrast curve 5[15:8]
0x8020764B	SNR1_TMP_CONST_ CURVE_5_B0	0x00	RW	Bit[7:0]: Sensor 1 contrast curve 5[7:0]
0x8020764C	SNR1_TMP_CONST_ CURVE_6_B1	0x90	RW	Bit[7:0]: Sensor 1 contrast curve 6[15:8]
0x8020764D	SNR1_TMP_CONST_ CURVE_6_B0	0x00	RW	Bit[7:0]: Sensor 1 contrast curve 6[7:0]
0x8020764E	SNR1_TMP_CONST_ CURVE_7_B1	0x92	RW	Bit[7:0]: Sensor 1 contrast curve 7[15:8]
0x8020764F	SNR1_TMP_CONST_ CURVE_7_B0	0x00	RW	Bit[7:0]: Sensor 1 contrast curve 7[7:0]

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table 4-48 tone mapping registers (sheet 23 of 34)

address	register name	default value	R/W	description
0x80207650	SNR1_TMP_CONST_CURVE_8_B1	0x94	RW	Bit[7:0]: Sensor 1 contrast curve 8[15:8]
0x80207651	SNR1_TMP_CONST_CURVE_8_B0	0x00	RW	Bit[7:0]: Sensor 1 contrast curve 8[7:0]
0x80207652	SNR1_TMP_CONST_CURVE_9_B1	0x96	RW	Bit[7:0]: Sensor 1 contrast curve 9[15:8]
0x80207653	SNR1_TMP_CONST_CURVE_9_B0	0x00	RW	Bit[7:0]: Sensor 1 contrast curve 9[7:0]
0x80207654	SNR1_TMP_CONST_CURVE_A_B1	0x98	RW	Bit[7:0]: Sensor 1 contrast curve A[15:8]
0x80207655	SNR1_TMP_CONST_CURVE_A_B0	0x00	RW	Bit[7:0]: Sensor 1 contrast curve A[7:0]
0x80207656	SNR1_TMP_CONST_CURVE_B_B1	0x9A	RW	Bit[7:0]: Sensor 1 contrast curve B[15:8]
0x80207657	SNR1_TMP_CONST_CURVE_B_B0	0x00	RW	Bit[7:0]: Sensor 1 contrast curve B[7:0]
0x80207658	SNR1_TMP_CONST_CURVE_C_B1	0x9C	RW	Bit[7:0]: Sensor 1 contrast curve C[15:8]
0x80207659	SNR1_TMP_CONST_CURVE_C_B0	0x00	RW	Bit[7:0]: Sensor 1 contrast curve C[7:0]
0x8020765A	SNR1_TMP_CONST_CURVE_D_B1	0x9E	RW	Bit[7:0]: Sensor 1 contrast curve D[15:8]
0x8020765B	SNR1_TMP_CONST_CURVE_D_B0	0x00	RW	Bit[7:0]: Sensor 1 contrast curve D[7:0]
0x8020765C	SNR1_TMP_CONST_CURVE_E_B1	0x9F	RW	Bit[7:0]: Sensor 1 contrast curve E[15:8]
0x8020765D	SNR1_TMP_CONST_CURVE_E_B0	0x00	RW	Bit[7:0]: Sensor 1 contrast curve E[7:0]
0x8020765E	SNR1_TMP_CONST_CURVE_F_B1	0x9F	RW	Bit[7:0]: Sensor 1 contrast curve F[15:8]
0x8020765F	SNR1_TMP_CONST_CURVE_F_B0	0xFF	RW	Bit[7:0]: Sensor 1 contrast curve F[7:0]
0x80207660	SNR1_TMP_GAMMA_GAIN_00_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 00[9:8]
0x80207661	SNR1_TMP_GAMMA_GAIN_00_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 00[7:0]

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table 4-48 tone mapping registers (sheet 24 of 34)

address	register name	default value	R/W	description
0x80207662	SNR1_TMP_GAMMA_GAIN_01_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 01[9:8]
0x80207663	SNR1_TMP_GAMMA_GAIN_01_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 01[7:0]
0x80207664	SNR1_TMP_GAMMA_GAIN_02_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 02[9:8]
0x80207665	SNR1_TMP_GAMMA_GAIN_02_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 02[7:0]
0x80207666	SNR1_TMP_GAMMA_GAIN_03_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 03[9:8]
0x80207667	SNR1_TMP_GAMMA_GAIN_03_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 03[7:0]
0x80207668	SNR1_TMP_GAMMA_GAIN_04_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 04[9:8]
0x80207669	SNR1_TMP_GAMMA_GAIN_04_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 04[7:0]
0x8020766A	SNR1_TMP_GAMMA_GAIN_10_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 10[9:8]
0x8020766B	SNR1_TMP_GAMMA_GAIN_10_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 10[7:0]
0x8020766C	SNR1_TMP_GAMMA_GAIN_11_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 11[9:8]
0x8020766D	SNR1_TMP_GAMMA_GAIN_11_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 11[7:0]
0x8020766E	SNR1_TMP_GAMMA_GAIN_12_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 12[9:8]
0x8020766F	SNR1_TMP_GAMMA_GAIN_12_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 12[7:0]
0x80207670	SNR1_TMP_GAMMA_GAIN_13_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 13[9:8]
0x80207671	SNR1_TMP_GAMMA_GAIN_13_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 13[7:0]

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table 4-48 tone mapping registers (sheet 25 of 34)

address	register name	default value	R/W	description
0x80207672	SNR1_TMP_GAMMA_GAIN_14_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 14[9:8]
0x80207673	SNR1_TMP_GAMMA_GAIN_14_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 14[7:0]
0x80207674	SNR1_TMP_GAMMA_GAIN_20_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 20[9:8]
0x80207675	SNR1_TMP_GAMMA_GAIN_20_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 20[7:0]
0x80207676	SNR1_TMP_GAMMA_GAIN_21_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 21[9:8]
0x80207677	SNR1_TMP_GAMMA_GAIN_21_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 21[7:0]
0x80207678	SNR1_TMP_GAMMA_GAIN_22_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 22[9:8]
0x80207679	SNR1_TMP_GAMMA_GAIN_22_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 22[7:0]
0x8020767A	SNR1_TMP_GAMMA_GAIN_23_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 23[9:8]
0x8020767B	SNR1_TMP_GAMMA_GAIN_23_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 23[7:0]
0x8020767C	SNR1_TMP_GAMMA_GAIN_24_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 24[9:8]
0x8020767D	SNR1_TMP_GAMMA_GAIN_24_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 24[7:0]
0x8020767E	SNR1_TMP_GAMMA_GAIN_30_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 30[9:8]
0x8020767F	SNR1_TMP_GAMMA_GAIN_30_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 30[7:0]
0x80207680	SNR1_TMP_GAMMA_GAIN_31_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 31[9:8]
0x80207681	SNR1_TMP_GAMMA_GAIN_31_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 31[7:0]

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table 4-48 tone mapping registers (sheet 26 of 34)

address	register name	default value	R/W	description
0x80207682	SNR1_TMP_GAMMA_GAIN_32_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 32[9:8]
0x80207683	SNR1_TMP_GAMMA_GAIN_32_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 32[7:0]
0x80207684	SNR1_TMP_GAMMA_GAIN_33_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 33[9:8]
0x80207685	SNR1_TMP_GAMMA_GAIN_33_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 33[7:0]
0x80207686	SNR1_TMP_GAMMA_GAIN_34_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 34[9:8]
0x80207687	SNR1_TMP_GAMMA_GAIN_34_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 34[7:0]
0x80207688	SNR1_TMP_GAMMA_GAIN_40_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 40[9:8]
0x80207689	SNR1_TMP_GAMMA_GAIN_40_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 40[7:0]
0x8020768A	SNR1_TMP_GAMMA_GAIN_41_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 41[9:8]
0x8020768B	SNR1_TMP_GAMMA_GAIN_41_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 41[7:0]
0x8020768C	SNR1_TMP_GAMMA_GAIN_42_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 42[9:8]
0x8020768D	SNR1_TMP_GAMMA_GAIN_42_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 42[7:0]
0x8020768E	SNR1_TMP_GAMMA_GAIN_43_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 43[9:8]
0x8020768F	SNR1_TMP_GAMMA_GAIN_43_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 43[7:0]
0x80207690	SNR1_TMP_GAMMA_GAIN_44_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 gamma gain of window 44[9:8]
0x80207691	SNR1_TMP_GAMMA_GAIN_44_B0	0xFF	RW	Bit[7:0]: Sensor 1 gamma gain of window 44[7:0]

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table 4-48 tone mapping registers (sheet 27 of 34)

address	register name	default value	R/W	description
0x80207692	SNR1_TMP_GLOBAL_GAIN_B1	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 global gamma gain[9:8]
0x80207693	SNR1_TMP_GLOBAL_GAIN_B0	0xFF	RW	Bit[7:0]: Sensor 1 global gamma gain[7:0]
0x80207694	SNR1_TMP_LOG_GAIN_B1	0x00	RW	Bit[7]: Reserved Bit[6:0]: Sensor 1 expect log gamma gain[14:8]
0x80207695	SNR1_TMP_LOG_GAIN_B0	0x00	RW	Bit[7:0]: Sensor 1 expect log gamma gain[7:0]
0x80207696	SNR1_TMP_LOG_MAX_B1	0x4F	RW	Bit[7:0]: Sensor 1 log max value[15:8]
0x80207697	SNR1_TMP_LOG_MAX_B0	0xFF	RW	Bit[7:0]: Sensor 1 log max value[7:0]
0x80207698	SNR1_TMP_Y_TH0_B1	0x00	RW	Bit[7:0]: Sensor 1 Y threshold 0[15:8]
0x80207699	SNR1_TMP_Y_TH0_B0	0x00	RW	Bit[7:0]: Sensor 1 Y threshold 0[7:0]
0x8020769A	SNR1_TMP_Y_TH1_B1	0x00	RW	Bit[7:0]: Sensor 1 Y threshold 1[15:8]
0x8020769B	SNR1_TMP_Y_TH1_B0	0x00	RW	Bit[7:0]: Sensor 1 Y threshold 1[7:0]
0x8020769C	SNR1_TMP_Y_TH2_B1	0x00	RW	Bit[7:0]: Sensor 1 Y threshold 2[15:8]
0x8020769D	SNR1_TMP_Y_TH2_B0	0x00	RW	Bit[7:0]: Sensor 1 Y threshold 2[7:0]
0x8020769E	SNR1_TMP_Y_TH3_B1	0x00	RW	Bit[7:0]: Sensor 1 Y threshold 3[15:8]
0x8020769F	SNR1_TMP_Y_TH3_B0	0x00	RW	Bit[7:0]: Sensor 1 Y threshold 3[7:0]
0x802076A1	SNR1_TMP_Y_TH0TH1_B2	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 th0/th1 difference[17:16]
0x802076A2	SNR1_TMP_Y_TH0TH1_B1	0x00	RW	Bit[7:0]: Sensor 1 th0/th1 difference[15:8]
0x802076A3	SNR1_TMP_Y_TH0TH1_B0	0x00	RW	Bit[7:0]: Sensor 1 th0/th1 difference[7:0]
0x802076A5	SNR1_TMP_Y_TH2TH3_B2	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Sensor 1 th2/th3 difference[17:16]
0x802076A6	SNR1_TMP_Y_TH2TH3_B1	0x00	RW	Bit[7:0]: Sensor 1 th2/th3 difference[15:8]
0x802076A7	SNR1_TMP_Y_TH2TH3_B0	0x00	RW	Bit[7:0]: Sensor 1 th2/th3 difference[7:0]

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table 4-48 tone mapping registers (sheet 28 of 34)

address	register name	default value	R/W	description
0x802076B0	SNR1_TMP_LOCAL_MEAN_0_B1	–	R	Bit[7:0]: Sensor 1 local mean value for window 0[15:8]
0x802076B1	SNR1_TMP_LOCAL_MEAN_0_B0	–	R	Bit[7:0]: Sensor 1 local mean value for window 0[7:0]
0x802076B2	SNR1_TMP_LOCAL_MEAN_1_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 1[15:8]
0x802076B3	SNR1_TMP_LOCAL_MEAN_1_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 1[7:0]
0x802076B4	SNR1_TMP_LOCAL_MEAN_2_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 2[15:8]
0x802076B5	SNR1_TMP_LOCAL_MEAN_2_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 2[7:0]
0x802076B6	SNR1_TMP_LOCAL_MEAN_3_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 3[15:8]
0x802076B7	SNR1_TMP_LOCAL_MEAN_3_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 3[7:0]
0x802076B8	SNR1_TMP_LOCAL_MEAN_4_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 4[15:8]
0x802076B9	SNR1_TMP_LOCAL_MEAN_4_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 4[7:0]
0x802076BA	SNR1_TMP_LOCAL_MEAN_5_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 5[15:8]
0x802076BB	SNR1_TMP_LOCAL_MEAN_5_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 5[7:0]
0x802076BC	SNR1_TMP_LOCAL_MEAN_6_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 6[15:8]
0x802076BD	SNR1_TMP_LOCAL_MEAN_6_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 6[7:0]
0x802076BE	SNR1_TMP_LOCAL_MEAN_7_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 7[15:8]
0x802076BF	SNR1_TMP_LOCAL_MEAN_7_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 7[7:0]
0x802076C0	SNR1_TMP_LOCAL_MEAN_8_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 8[15:8]
0x802076C1	SNR1_TMP_LOCAL_MEAN_8_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 8[7:0]
0x802076C2	SNR1_TMP_LOCAL_MEAN_9_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 9[15:8]

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table 4-48 tone mapping registers (sheet 29 of 34)

address	register name	default value	R/W	description
0x802076C3	SNR1_TMP_LOCAL_MEAN_9_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 9[7:0]
0x802076C4	SNR1_TMP_LOCAL_MEAN_10_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 10[15:8]
0x802076C5	SNR1_TMP_LOCAL_MEAN_10_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 10[7:0]
0x802076C6	SNR1_TMP_LOCAL_MEAN_11_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 11[15:8]
0x802076C7	SNR1_TMP_LOCAL_MEAN_11_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 11[7:0]
0x802076C8	SNR1_TMP_LOCAL_MEAN_12_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 12[15:8]
0x802076C9	SNR1_TMP_LOCAL_MEAN_12_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 12[7:0]
0x802076CA	SNR1_TMP_LOCAL_MEAN_13_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 13[15:8]
0x802076CB	SNR1_TMP_LOCAL_MEAN_13_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 13[7:0]
0x802076CC	SNR1_TMP_LOCAL_MEAN_14_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 14[15:8]
0x802076CD	SNR1_TMP_LOCAL_MEAN_14_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 14[7:0]
0x802076CE	SNR1_TMP_LOCAL_MEAN_15_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 15[15:8]
0x802076CF	SNR1_TMP_LOCAL_MEAN_15_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 15[7:0]
0x802076D0	SNR1_TMP_LOCAL_MEAN_16_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 16[15:8]
0x802076D1	SNR1_TMP_LOCAL_MEAN_16_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 16[7:0]
0x802076D2	SNR1_TMP_LOCAL_MEAN_17_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 17[15:8]
0x802076D3	SNR1_TMP_LOCAL_MEAN_17_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 17[7:0]
0x802076D4	SNR1_TMP_LOCAL_MEAN_18_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 18[15:8]
0x802076D5	SNR1_TMP_LOCAL_MEAN_18_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 18[7:0]

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table 4-48 tone mapping registers (sheet 30 of 34)

address	register name	default value	R/W	description
0x802076D6	SNR1_TMP_LOCAL_ MEAN_19_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 19[15:8]
0x802076D7	SNR1_TMP_LOCAL_ MEAN_19_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 19[7:0]
0x802076D8	SNR1_TMP_LOCAL_ MEAN_20_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 20[15:8]
0x802076D9	SNR1_TMP_LOCAL_ MEAN_20_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 20[7:0]
0x802076DA	SNR1_TMP_LOCAL_ MEAN_21_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 21[15:8]
0x802076DB	SNR1_TMP_LOCAL_ MEAN_21_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 21[7:0]
0x802076DC	SNR1_TMP_LOCAL_ MEAN_22_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 22[15:8]
0x802076DD	SNR1_TMP_LOCAL_ MEAN_22_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 22[7:0]
0x802076DE	SNR1_TMP_LOCAL_ MEAN_23_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 23[15:8]
0x802076DF	SNR1_TMP_LOCAL_ MEAN_23_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 23[7:0]
0x802076E0	SNR1_TMP_LOCAL_ MEAN_24_B1	–	R	Bit[7:0]: Sensor 1 local mean for window 24[15:8]
0x802076E1	SNR1_TMP_LOCAL_ MEAN_24_B0	–	R	Bit[7:0]: Sensor 1 local mean for window 24[7:0]
0x802076E2	SNR1_TMP_GLOBAL_ MEAN_B1	–	R	Bit[7:0]: Sensor 1 global mean value[15:8]
0x802076E3	SNR1_TMP_GLOBAL_ MEAN_B0	–	R	Bit[7:0]: Sensor 1 global mean value[7:0]
0x802076E4	SNR1_TMP_NORMALIZE_ LOG_MEAN_B1	–	R	Bit[7:0]: Sensor 1 normalize mean value[15:8]
0x802076E5	SNR1_TMP_NORMALIZE_ LOG_MEAN_B0	–	R	Bit[7:0]: Sensor 1 normalize mean value[7:0]
0x802076E8	SNR1_TMP_HIST_0_B3	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 0[31:24]
0x802076E9	SNR1_TMP_HIST_0_B2	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 0[23:16]
0x802076EA	SNR1_TMP_HIST_0_B1	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 0[15:8]

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table 4-48 tone mapping registers (sheet 31 of 34)

address	register name	default value	R/W	description
0x802076EB	SNR1_TMP_HIST_0_B0	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 0[7:0]
0x802076EC	SNR1_TMP_HIST_1_B3	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 1[31:24]
0x802076ED	SNR1_TMP_HIST_1_B2	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 1[23:16]
0x802076EE	SNR1_TMP_HIST_1_B1	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 1[15:8]
0x802076EF	SNR1_TMP_HIST_1_B0	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 1[7:0]
0x802076F0	SNR1_TMP_HIST_2_B3	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 2[31:24]
0x802076F1	SNR1_TMP_HIST_2_B2	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 2[23:16]
0x802076F2	SNR1_TMP_HIST_2_B1	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 2[15:8]
0x802076F3	SNR1_TMP_HIST_2_B0	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 2[7:0]
0x802076F4	SNR1_TMP_HIST_3_B3	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 3[31:24]
0x802076F5	SNR1_TMP_HIST_3_B2	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 3[23:16]
0x802076F6	SNR1_TMP_HIST_3_B1	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 3[15:8]
0x802076F7	SNR1_TMP_HIST_3_B0	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 3[7:0]
0x802076F8	SNR1_TMP_HIST_4_B3	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 4[31:24]
0x802076F9	SNR1_TMP_HIST_4_B2	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 4[23:16]
0x802076FA	SNR1_TMP_HIST_4_B1	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 4[15:8]
0x802076FB	SNR1_TMP_HIST_4_B0	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 4[7:0]
0x802076FC	SNR1_TMP_HIST_5_B3	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 5[31:24]
0x802076FD	SNR1_TMP_HIST_5_B2	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 5[23:16]

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table 4-48 tone mapping registers (sheet 32 of 34)

address	register name	default value	R/W	description
0x802076FE	SNR1_TMP_HIST_5_B1	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 5[15:8]
0x802076FF	SNR1_TMP_HIST_5_B0	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 5[7:0]
0x80207700	SNR1_TMP_HIST_6_B3	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 6[31:24]
0x80207701	SNR1_TMP_HIST_6_B2	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 6[23:16]
0x80207702	SNR1_TMP_HIST_6_B1	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 6[15:8]
0x80207703	SNR1_TMP_HIST_6_B0	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 6[7:0]
0x80207704	SNR1_TMP_HIST_7_B3	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 7[31:24]
0x80207705	SNR1_TMP_HIST_7_B2	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 7[23:16]
0x80207706	SNR1_TMP_HIST_7_B1	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 7[15:8]
0x80207707	SNR1_TMP_HIST_7_B0	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 7[7:0]
0x80207708	SNR1_TMP_HIST_8_B3	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 8[31:24]
0x80207709	SNR1_TMP_HIST_8_B2	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 8[23:16]
0x8020770A	SNR1_TMP_HIST_8_B1	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 8[15:8]
0x8020770B	SNR1_TMP_HIST_8_B0	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 8[7:0]
0x8020770C	SNR1_TMP_HIST_9_B3	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 9[31:24]
0x8020770D	SNR1_TMP_HIST_9_B2	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 9[23:16]
0x8020770E	SNR1_TMP_HIST_9_B1	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 9[15:8]
0x8020770F	SNR1_TMP_HIST_9_B0	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 9[7:0]
0x80207710	SNR1_TMP_HIST_10_B3	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 10[31:24]

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table 4-48 tone mapping registers (sheet 33 of 34)

address	register name	default value	R/W	description
0x80207711	SNR1_TMP_HIST_10_B2	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 10[23:16]
0x80207712	SNR1_TMP_HIST_10_B1	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 10[15:8]
0x80207713	SNR1_TMP_HIST_10_B0	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 10[7:0]
0x80207714	SNR1_TMP_HIST_11_B3	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 11[31:24]
0x80207715	SNR1_TMP_HIST_11_B2	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 11[23:16]
0x80207716	SNR1_TMP_HIST_11_B1	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 11[15:8]
0x80207717	SNR1_TMP_HIST_11_B0	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 11[7:0]
0x80207718	SNR1_TMP_HIST_12_B3	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 12[31:24]
0x80207719	SNR1_TMP_HIST_12_B2	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 12[23:16]
0x8020771A	SNR1_TMP_HIST_12_B1	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 12[15:8]
0x8020771B	SNR1_TMP_HIST_12_B0	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 12[7:0]
0x8020771C	SNR1_TMP_HIST_13_B3	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 13[31:24]
0x8020771D	SNR1_TMP_HIST_13_B2	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 13[23:16]
0x8020771E	SNR1_TMP_HIST_13_B1	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 13[15:8]
0x8020771F	SNR1_TMP_HIST_13_B0	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 13[7:0]
0x80207720	SNR1_TMP_HIST_14_B3	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 14[31:24]
0x80207721	SNR1_TMP_HIST_14_B2	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 14[23:16]
0x80207722	SNR1_TMP_HIST_14_B1	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 14[15:8]
0x80207723	SNR1_TMP_HIST_14_B0	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 14[7:0]

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table 4-48 tone mapping registers (sheet 34 of 34)

address	register name	default value	R/W	description
0x80207724	SNR1_TMP_HIST_15_B3	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 15[31:24]
0x80207725	SNR1_TMP_HIST_15_B2	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 15[23:16]
0x80207726	SNR1_TMP_HIST_15_B1	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 15[15:8]
0x80207727	SNR1_TMP_HIST_15_B0	–	R	Bit[7:0]: Sensor 1 log curve histogram segment 15[7:0]

4.39 YUV data de-noise (UVDNS) control

table 4-49 UVDNS registers (sheet 1 of 2)

address	register name	default value	RW	description
0x80207D00	SNR0_UVDNS_NOISE_LIST_0	0x01	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 noise list 0
0x80207D01	SNR0_UVDNS_NOISE_LIST_1	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 noise list 1
0x80207D02	SNR0_UVDNS_NOISE_LIST_2	0x04	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 noise list 2
0x80207D03	SNR0_UVDNS_NOISE_LIST_3	0x08	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 noise list 3
0x80207D04	SNR0_UVDNS_NOISE_LIST_4	0x0C	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 noise list 4
0x80207D05	SNR0_UVDNS_NOISE_LIST_5	0x10	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 noise list 5
0x80207D06	SNR0_UVDNS_NOISE_LIST_6	0x14	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 noise list 6
0x80207D07	SNR0_UVDNS_NOISE_LIST_7	0x18	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 noise list 7
0x80207D08	SNR0_UVDNS_CTRL	0x04	RW	Bit[7:6]: Reserved Bit[5]: Manual noise enable Bit[4:0]: Shadow extra noise
0x80207D09	SNR0_UVDNS_MAN_NOISE	0x0A	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 manual noise

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table 4-49 UVDNS registers (sheet 2 of 2)

address	register name	default value	RW	description
0x80207D0A	SNR0_UVDNS_NOISE_RO	–	R	Bit[7:5]: Reserved Bit[4:0]: Sensor 0 read out noise
0x80207D10	SNR1_UVDNS_NOISE_LIST_0	0x01	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 noise list 0
0x80207D11	SNR1_UVDNS_NOISE_LIST_1	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 noise list 1
0x80207D12	SNR1_UVDNS_NOISE_LIST_2	0x04	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 noise list 2
0x80207D13	SNR1_UVDNS_NOISE_LIST_3	0x08	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 noise list 3
0x80207D14	SNR1_UVDNS_NOISE_LIST_4	0x0C	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 noise list 4
0x80207D15	SNR1_UVDNS_NOISE_LIST_5	0x10	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 noise list 5
0x80207D16	SNR1_UVDNS_NOISE_LIST_6	0x14	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 noise list 6
0x80207D17	SNR1_UVDNS_NOISE_LIST_7	0x18	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 noise list 7
0x80207D18	SNR1_UVDNS_CTRL	0x04	RW	Bit[7:6]: Reserved Bit[5]: Manual noise enable Bit[4:0]: Shadow extra noise
0x80207D19	SNR1_UVDNS_MAN_NOISE	0x0A	RW	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 manual noise
0x80207D1A	SNR1_UVDNS_NOISE_RO	–	R	Bit[7:5]: Reserved Bit[4:0]: Sensor 1 read out noise

4.40 YUV (ROI based) statistics (YUV stat) control

table 4-50 YUV stat registers (sheet 1 of 15)

address	register name	default value	R/W	description
0x80207C00	ROI_0_CTRL_00	0x00	RW	ROI 0 Control Byte 00 Bit[7:4]: Reserved Bit[3:0]: ROI 0 x start[11:8]
0x80207C01	ROI_0_CTRL_01	0x00	RW	ROI 0 Control Byte 01 Bit[7:0]: ROI 0 x start[7:0]

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table 4-50 YUV stat registers (sheet 2 of 15)

address	register name	default value	R/W	description
0x80207C02	ROI_0_CTRL_02	0x00	RW	ROI 0 Control Byte 02 Bit[7:3]: Reserved Bit[2:0]: ROI 0 y start[10:8]
0x80207C03	ROI_0_CTRL_03	0x00	RW	ROI 0 Control Byte 03 Bit[7:0]: ROI 0 y start[7:0]
0x80207C04	ROI_0_CTRL_04	0x01	RW	ROI 0 Control Byte 04 Bit[7:4]: Reserved Bit[3:0]: ROI 0 width[11:8]
0x80207C05	ROI_0_CTRL_05	0x00	RW	ROI 0 Control Byte 05 Bit[7:0]: ROI 0 width[7:0]
0x80207C06	ROI_0_CTRL_06	0x01	RW	ROI 0 Control Byte 06 Bit[7:3]: Reserved Bit[2:0]: ROI 0 height[10:8]
0x80207C07	ROI_0_CTRL_07	0x00	RW	ROI 0 Control Byte 07 Bit[7:0]: ROI 0 height[7:0]
0x80207C08	ROI_1_CTRL_00	0x00	RW	ROI 1 Control Byte 00 Bit[7:4]: Reserved Bit[3:0]: ROI 1 x start[11:8]
0x80207C09	ROI_1_CTRL_01	0x00	RW	ROI 1 Control Byte 01 Bit[7:0]: ROI 1 x start[7:0]
0x80207C0A	ROI_1_CTRL_02	0x00	RW	ROI 1 Control Byte 02 Bit[7:3]: Reserved Bit[2:0]: ROI 1 y start[10:8]
0x80207C0B	ROI_1_CTRL_03	0x00	RW	ROI 1 Control Byte 03 Bit[7:0]: ROI 1 y start[7:0]
0x80207C0C	ROI_1_CTRL_04	0x01	RW	ROI 1 Control Byte 04 Bit[7:4]: Reserved Bit[3:0]: ROI 1 width[11:8]
0x80207C0D	ROI_1_CTRL_05	0x00	RW	ROI 1 Control Byte 05 Bit[7:0]: ROI 1 width[7:0]
0x80207C0E	ROI_1_CTRL_06	0x01	RW	ROI 1 Control Byte 06 Bit[7:3]: Reserved Bit[2:0]: ROI 1 height[10:8]
0x80207C0F	ROI_1_CTRL_07	0x00	RW	ROI 1 Control Byte 07 Bit[7:0]: ROI 1 height[7:0]
0x80207C10	ROI_2_CTRL_00	0x00	RW	ROI 2 Control Byte 00 Bit[7:4]: Reserved Bit[3:0]: ROI 2 x start[11:8]
0x80207C11	ROI_2_CTRL_01	0x00	RW	ROI 2 Control Byte 01 Bit[7:0]: ROI 2 x start[7:0]

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table 4-50 YUV stat registers (sheet 3 of 15)

address	register name	default value	R/W	description
0x80207C12	ROI_2_CTRL_02	0x00	RW	ROI 2 Control Byte 02 Bit[7:3]: Reserved Bit[2:0]: ROI 2 y start[10:8]
0x80207C13	ROI_2_CTRL_03	0x00	RW	ROI 2 Control Byte 03 Bit[7:0]: ROI 2 y start[7:0]
0x80207C14	ROI_2_CTRL_04	0x01	RW	ROI 2 Control Byte 04 Bit[7:4]: Reserved Bit[3:0]: ROI 2 width[11:8]
0x80207C15	ROI_2_CTRL_05	0x00	RW	ROI 2 Control Byte 05 Bit[7:0]: ROI 2 width[7:0]
0x80207C16	ROI_2_CTRL_06	0x01	RW	ROI 2 Control Byte 06 Bit[7:3]: Reserved Bit[2:0]: ROI 2 height[10:8]
0x80207C17	ROI_2_CTRL_07	0x00	RW	ROI 2 Control Byte 07 Bit[7:0]: ROI 2 height[7:0]
0x80207C18	ROI_3_CTRL_00	0x00	RW	ROI 3 Control Byte 00 Bit[7:4]: Reserved Bit[3:0]: ROI 3 x start[11:8]
0x80207C19	ROI_3_CTRL_01	0x00	RW	ROI 3 Control Byte 01 Bit[7:0]: ROI 3 x start[7:0]
0x80207C1A	ROI_3_CTRL_02	0x00	RW	ROI 3 Control Byte 02 Bit[7:3]: Reserved Bit[2:0]: ROI 3 y start[10:8]
0x80207C1B	ROI_3_CTRL_03	0x00	RW	ROI 3 Control Byte 03 Bit[7:0]: ROI 3 y start[7:0]
0x80207C1C	ROI_3_CTRL_04	0x01	RW	ROI 3 Control Byte 04 Bit[7:4]: Reserved Bit[3:0]: ROI 3 width[11:8]
0x80207C1D	ROI_3_CTRL_05	0x00	RW	ROI 3 Control Byte 05 Bit[7:0]: ROI 3 width[7:0]
0x80207C1E	ROI_3_CTRL_06	0x01	RW	ROI 3 Control Byte 06 Bit[7:3]: Reserved Bit[2:0]: ROI 3 height[10:8]
0x80207C1F	ROI_3_CTRL_07	0x00	RW	ROI 3 Control Byte 07 Bit[7:0]: ROI 3 height[7:0]

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table 4-50 YUV stat registers (sheet 4 of 15)

address	register name	default value	R/W	description
0x80207C20	ROI_CTRL_00_ALL	0x0C	RW	Bit[7:4]: Reserved Bit[3]: ROI 3 sensor select 0: Sensor 0 1: Sensor 1 Bit[2]: ROI 2 sensor select 0: Sensor 0 1: Sensor 1 Bit[1]: ROI 1 sensor select 0: Sensor 0 1: Sensor 1 Bit[0]: ROI 0 sensor select 0: Sensor 0 1: Sensor 1
0x80207C21	ROI_CTRL_01_ALL	0x00	RW	Bit[7:4]: Sampling rate for sensor 1 ROI Bit[3:0]: Sampling rate for sensor 0 ROI
0x80207C28	ROI_0_READ_00	–	R	ROI 0 Read Out Byte 00 Bit[7:0]: ROI 0 Y average[15:8]
0x80207C29	ROI_0_READ_01	–	R	ROI 0 Read Out Byte 01 Bit[7:0]: ROI 0 Y average[7:0]
0x80207C2A	ROI_0_READ_02	–	R	ROI 0 Read Out Byte 02 Bit[7:0]: ROI 0 U average[15:8]
0x80207C2B	ROI_0_READ_03	–	R	ROI 0 Read Out Byte 03 Bit[7:0]: ROI 0 U average[7:0]
0x80207C2C	ROI_0_READ_04	–	R	ROI 0 Read Out Byte 04 Bit[7:0]: ROI 0 V average[15:8]
0x80207C2D	ROI_0_READ_05	–	R	ROI 0 Read Out Byte 05 Bit[7:0]: ROI 0 V average[7:0]
0x80207C2E	ROI_0_READ_06	–	R	ROI 0 Read Out Byte 06 Bit[7:0]: ROI 0 Y hist bin 0[23:16]
0x80207C2F	ROI_0_READ_07	–	R	ROI 0 Read Out Byte 07 Bit[7:0]: ROI 0 Y hist bin 0[15:8]
0x80207C30	ROI_0_READ_08	–	R	ROI 0 Read Out Byte 08 Bit[7:0]: ROI 0 Y hist bin 0[7:0]
0x80207C31	ROI_0_READ_09	–	R	ROI 0 Read Out Byte 09 Bit[7:0]: ROI 0 Y hist bin 1[23:16]
0x80207C32	ROI_0_READ_0A	–	R	ROI 0 Read Out Byte 0A Bit[7:0]: ROI 0 Y hist bin 1[15:8]
0x80207C33	ROI_0_READ_0B	–	R	ROI 0 Read Out Byte 0B Bit[7:0]: ROI 0 Y hist bin 1[7:0]

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table 4-50 YUV stat registers (sheet 5 of 15)

address	register name	default value	R/W	description
0x80207C34	ROI_0_READ_0C	–	R	ROI 0 Read Out Byte 0C Bit[7:0]: ROI 0 Y hist bin 2[23:16]
0x80207C35	ROI_0_READ_0D	–	R	ROI 0 Read Out Byte 0D Bit[7:0]: ROI 0 Y hist bin 2[15:8]
0x80207C36	ROI_0_READ_0E	–	R	ROI 0 Read Out Byte 0E Bit[7:0]: ROI 0 Y hist bin 2[7:0]
0x80207C37	ROI_0_READ_0F	–	R	ROI 0 Read Out Byte 0F Bit[7:0]: ROI 0 Y hist bin 3[23:16]
0x80207C38	ROI_0_READ_10	–	R	ROI 0 Read Out Byte 10 Bit[7:0]: ROI 0 Y hist bin 3[15:8]
0x80207C39	ROI_0_READ_11	–	R	ROI 0 Read Out Byte 11 Bit[7:0]: ROI 0 Y hist bin 3[7:0]
0x80207C3A	ROI_0_READ_12	–	R	ROI 0 Read Out Byte 12 Bit[7:0]: ROI 0 Y hist bin 4[23:16]
0x80207C3B	ROI_0_READ_13	–	R	ROI 0 Read Out Byte 13 Bit[7:0]: ROI 0 Y hist bin 4[15:8]
0x80207C3C	ROI_0_READ_14	–	R	ROI 0 Read Out Byte 14 Bit[7:0]: ROI 0 Y hist bin 4[7:0]
0x80207C3D	ROI_0_READ_15	–	R	ROI 0 Read Out Byte 15 Bit[7:0]: ROI 0 Y hist bin 5[23:16]
0x80207C3E	ROI_0_READ_16	–	R	ROI 0 Read Out Byte 16 Bit[7:0]: ROI 0 Y hist bin 5[15:8]
0x80207C3F	ROI_0_READ_17	–	R	ROI 0 Read Out Byte 17 Bit[7:0]: ROI 0 Y hist bin 5[7:0]
0x80207C40	ROI_0_READ_18	–	R	ROI 0 Read Out Byte 18 Bit[7:0]: ROI 0 Y hist bin 6[23:16]
0x80207C41	ROI_0_READ_19	–	R	ROI 0 Read Out Byte 19 Bit[7:0]: ROI 0 Y hist bin 6[15:8]
0x80207C42	ROI_0_READ_1A	–	R	ROI 0 Read Out Byte 1A Bit[7:0]: ROI 0 Y hist bin 6[7:0]
0x80207C43	ROI_0_READ_1B	–	R	ROI 0 Read Out Byte 1B Bit[7:0]: ROI 0 Y hist bin 7[23:16]
0x80207C44	ROI_0_READ_1C	–	R	ROI 0 Read Out Byte 1C Bit[7:0]: ROI 0 Y hist bin 7[15:8]
0x80207C45	ROI_0_READ_1D	–	R	ROI 0 Read Out Byte 1D Bit[7:0]: ROI 0 Y hist bin 7[7:0]
0x80207C46	ROI_0_READ_1E	–	R	ROI 0 Read Out Byte 1E Bit[7:0]: ROI 0 Y hist bin 8[23:16]

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table 4-50 YUV stat registers (sheet 6 of 15)

address	register name	default value	R/W	description
0x80207C47	ROI_0_READ_1F	–	R	ROI 0 Read Out Byte 1F Bit[7:0]: ROI 0 Y hist bin 8[15:8]
0x80207C48	ROI_0_READ_20	–	R	ROI 0 Read Out Byte 20 Bit[7:0]: ROI 0 Y hist bin 8[7:0]
0x80207C49	ROI_0_READ_21	–	R	ROI 0 Read Out Byte 21 Bit[7:0]: ROI 0 Y hist bin 9[23:16]
0x80207C4A	ROI_0_READ_22	–	R	ROI 0 Read Out Byte 22 Bit[7:0]: ROI 0 Y hist bin 9[15:8]
0x80207C4B	ROI_0_READ_23	–	R	ROI 0 Read Out Byte 23 Bit[7:0]: ROI 0 Y hist bin 9[7:0]
0x80207C4C	ROI_0_READ_24	–	R	ROI 0 Read Out Byte 24 Bit[7:0]: ROI 0 Y hist bin 10[23:16]
0x80207C4D	ROI_0_READ_25	–	R	ROI 0 Read Out Byte 25 Bit[7:0]: ROI 0 Y hist bin 10[15:8]
0x80207C4E	ROI_0_READ_26	–	R	ROI 0 Read Out Byte 26 Bit[7:0]: ROI 0 Y hist bin 10[7:0]
0x80207C4F	ROI_0_READ_27	–	R	ROI 0 Read Out Byte 27 Bit[7:0]: ROI 0 Y hist bin 11[23:16]
0x80207C50	ROI_0_READ_28	–	R	ROI 0 Read Out Byte 28 Bit[7:0]: ROI 0 Y hist bin 11[15:8]
0x80207C51	ROI_0_READ_29	–	R	ROI 0 Read Out Byte 29 Bit[7:0]: ROI 0 Y hist bin 11[7:0]
0x80207C52	ROI_0_READ_2A	–	R	ROI 0 Read Out Byte 2A Bit[7:0]: ROI 0 Y hist bin 12[23:16]
0x80207C53	ROI_0_READ_2B	–	R	ROI 0 Read Out Byte 2B Bit[7:0]: ROI 0 Y hist bin 12[15:8]
0x80207C54	ROI_0_READ_2C	–	R	ROI 0 Read Out Byte 2C Bit[7:0]: ROI 0 Y hist bin 12[7:0]
0x80207C55	ROI_0_READ_2D	–	R	ROI 0 Read Out Byte 2D Bit[7:0]: ROI 0 Y hist bin 13[23:16]
0x80207C56	ROI_0_READ_2E	–	R	ROI 0 Read Out Byte 2E Bit[7:0]: ROI 0 Y hist bin 13[15:8]
0x80207C57	ROI_0_READ_2F	–	R	ROI 0 Read Out Byte 2F Bit[7:0]: ROI 0 Y hist bin 13[7:0]
0x80207C58	ROI_0_READ_30	–	R	ROI 0 Read Out Byte 30 Bit[7:0]: ROI 0 Y hist bin 14[23:16]
0x80207C59	ROI_0_READ_31	–	R	ROI 0 Read Out Byte 31 Bit[7:0]: ROI 0 Y hist bin 14[15:8]

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table 4-50 YUV stat registers (sheet 7 of 15)

address	register name	default value	R/W	description
0x80207C5A	ROI_0_READ_32	–	R	ROI 0 Read Out Byte 32 Bit[7:0]: ROI 0 Y hist bin 14[7:0]
0x80207C5B	ROI_0_READ_33	–	R	ROI 0 Read Out Byte 33 Bit[7:0]: ROI 0 Y hist bin 15[23:16]
0x80207C5C	ROI_0_READ_34	–	R	ROI 0 Read Out Byte 34 Bit[7:0]: ROI 0 Y hist bin 15[15:8]
0x80207C5D	ROI_0_READ_35	–	R	ROI 0 Read Out Byte 35 Bit[7:0]: ROI 0 Y hist bin 15[7:0]
0x80207C5E	ROI_1_READ_00	–	R	ROI 1 Read Out Byte 00 Bit[7:0]: ROI 1 Y average[15:8]
0x80207C5F	ROI_1_READ_01	–	R	ROI 1 Read Out Byte 01 Bit[7:0]: ROI 1 Y average[7:0]
0x80207C60	ROI_1_READ_02	–	R	ROI 1 Read Out Byte 02 Bit[7:0]: ROI 1 U average[15:8]
0x80207C61	ROI_1_READ_03	–	R	ROI 1 Read Out Byte 03 Bit[7:0]: ROI 1 U average[7:0]
0x80207C62	ROI_1_READ_04	–	R	ROI 1 Read Out Byte 04 Bit[7:0]: ROI 1 V average[15:8]
0x80207C63	ROI_1_READ_05	–	R	ROI 1 Read Out Byte 05 Bit[7:0]: ROI 1 V average[7:0]
0x80207C64	ROI_1_READ_06	–	R	ROI 1 Read Out Byte 06 Bit[7:0]: ROI 1 Y hist bin 0[23:16]
0x80207C65	ROI_1_READ_07	–	R	ROI 1 Read Out Byte 07 Bit[7:0]: ROI 1 Y hist bin 0[15:8]
0x80207C66	ROI_1_READ_08	–	R	ROI 1 Read Out Byte 08 Bit[7:0]: ROI 1 Y hist bin 0[7:0]
0x80207C67	ROI_1_READ_09	–	R	ROI 1 Read Out Byte 09 Bit[7:0]: ROI 1 Y hist bin 1[23:16]
0x80207C68	ROI_1_READ_0A	–	R	ROI 1 Read Out Byte 0A Bit[7:0]: ROI 1 Y hist bin 1[15:8]
0x80207C69	ROI_1_READ_0B	–	R	ROI 1 Read Out Byte 0B Bit[7:0]: ROI 1 Y hist bin 1[7:0]
0x80207C6A	ROI_1_READ_0C	–	R	ROI 1 Read Out Byte 0C Bit[7:0]: ROI 1 Y hist bin 2[23:16]
0x80207C6B	ROI_1_READ_0D	–	R	ROI 1 Read Out Byte 0D Bit[7:0]: ROI 1 Y hist bin 2[15:8]
0x80207C6C	ROI_1_READ_0E	–	R	ROI 1 Read Out Byte 0E Bit[7:0]: ROI 1 Y hist bin 2[7:0]

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table 4-50 YUV stat registers (sheet 8 of 15)

address	register name	default value	R/W	description
0x80207C6D	ROI_1_READ_0F	–	R	ROI 1 Read Out Byte 0F Bit[7:0]: ROI 1 Y hist bin 3[23:16]
0x80207C6E	ROI_1_READ_10	–	R	ROI 1 Read Out Byte 10 Bit[7:0]: ROI 1 Y hist bin 3[15:8]
0x80207C6F	ROI_1_READ_11	–	R	ROI 1 Read Out Byte 11 Bit[7:0]: ROI 1 Y hist bin 3[7:0]
0x80207C70	ROI_1_READ_12	–	R	ROI 1 Read Out Byte 12 Bit[7:0]: ROI 1 Y hist bin 4[23:16]
0x80207C71	ROI_1_READ_13	–	R	ROI 1 Read Out Byte 13 Bit[7:0]: ROI 1 Y hist bin 4[15:8]
0x80207C72	ROI_1_READ_14	–	R	ROI 1 Read Out Byte 14 Bit[7:0]: ROI 1 Y hist bin 4[7:0]
0x80207C73	ROI_1_READ_15	–	R	ROI 1 Read Out Byte 15 Bit[7:0]: ROI 1 Y hist bin 5[23:16]
0x80207C74	ROI_1_READ_16	–	R	ROI 1 Read Out Byte 16 Bit[7:0]: ROI 1 Y hist bin 5[15:8]
0x80207C75	ROI_1_READ_17	–	R	ROI 1 Read Out Byte 17 Bit[7:0]: ROI 1 Y hist bin 5[7:0]
0x80207C76	ROI_1_READ_18	–	R	ROI 1 Read Out Byte 18 Bit[7:0]: ROI 1 Y hist bin 6[23:16]
0x80207C77	ROI_1_READ_19	–	R	ROI 1 Read Out Byte 19 Bit[7:0]: ROI 1 Y hist bin 6[15:8]
0x80207C78	ROI_1_READ_1A	–	R	ROI 1 Read Out Byte 1A Bit[7:0]: ROI 1 Y hist bin 6[7:0]
0x80207C79	ROI_1_READ_1B	–	R	ROI 1 Read Out Byte 1B Bit[7:0]: ROI 1 Y hist bin 7[23:16]
0x80207C7A	ROI_1_READ_1C	–	R	ROI 1 Read Out Byte 1C Bit[7:0]: ROI 1 Y hist bin 7[15:8]
0x80207C7B	ROI_1_READ_1D	–	R	ROI 1 Read Out Byte 1D Bit[7:0]: ROI 1 Y hist bin 7[7:0]
0x80207C7C	ROI_1_READ_1E	–	R	ROI 1 Read Out Byte 1E Bit[7:0]: ROI 1 Y hist bin 8[23:16]
0x80207C7D	ROI_1_READ_1F	–	R	ROI 1 Read Out Byte 1F Bit[7:0]: ROI 1 Y hist bin 8[15:8]
0x80207C7E	ROI_1_READ_20	–	R	ROI 1 Read Out Byte 20 Bit[7:0]: ROI 1 Y hist bin 8[7:0]
0x80207C7F	ROI_1_READ_21	–	R	ROI 1 Read Out Byte 21 Bit[7:0]: ROI 1 Y hist bin 9[23:16]

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table 4-50 YUV stat registers (sheet 9 of 15)

address	register name	default value	R/W	description
0x80207C80	ROI_1_READ_22	–	R	ROI 1 Read Out Byte 22 Bit[7:0]: ROI 1 Y hist bin 9[15:8]
0x80207C81	ROI_1_READ_23	–	R	ROI 1 Read Out Byte 23 Bit[7:0]: ROI 1 Y hist bin 9[7:0]
0x80207C82	ROI_1_READ_24	–	R	ROI 1 Read Out Byte 24 Bit[7:0]: ROI 1 Y hist bin 10[23:16]
0x80207C83	ROI_1_READ_25	–	R	ROI 1 Read Out Byte 25 Bit[7:0]: ROI 1 Y hist bin 10[15:8]
0x80207C84	ROI_1_READ_26	–	R	ROI 1 Read Out Byte 26 Bit[7:0]: ROI 1 Y hist bin 10[7:0]
0x80207C85	ROI_1_READ_27	–	R	ROI 1 Read Out Byte 27 Bit[7:0]: ROI 1 Y hist bin 11[23:16]
0x80207C86	ROI_1_READ_28	–	R	ROI 1 Read Out Byte 28 Bit[7:0]: ROI 1 Y hist bin 11[15:8]
0x80207C87	ROI_1_READ_29	–	R	ROI 1 Read Out Byte 29 Bit[7:0]: ROI 1 Y hist bin 11[7:0]
0x80207C88	ROI_1_READ_2A	–	R	ROI 1 Read Out Byte 2A Bit[7:0]: ROI 1 Y hist bin 12[23:16]
0x80207C89	ROI_1_READ_2B	–	R	ROI 1 Read Out Byte 2B Bit[7:0]: ROI 1 Y hist bin 12[15:8]
0x80207C8A	ROI_1_READ_2C	–	R	ROI 1 Read Out Byte 2C Bit[7:0]: ROI 1 Y hist bin 12[7:0]
0x80207C8B	ROI_1_READ_2D	–	R	ROI 1 Read Out Byte 2D Bit[7:0]: ROI 1 Y hist bin 13[23:16]
0x80207C8C	ROI_1_READ_2E	–	R	ROI 1 Read Out Byte 2E Bit[7:0]: ROI 1 Y hist bin 13[15:8]
0x80207C8D	ROI_1_READ_2F	–	R	ROI 1 Read Out Byte 2F Bit[7:0]: ROI 1 Y hist bin 13[7:0]
0x80207C8E	ROI_1_READ_30	–	R	ROI 1 Read Out Byte 30 Bit[7:0]: ROI 1 Y hist bin 14[23:16]
0x80207C8F	ROI_1_READ_31	–	R	ROI 1 Read Out Byte 31 Bit[7:0]: ROI 1 Y hist bin 14[15:8]
0x80207C90	ROI_1_READ_32	–	R	ROI 1 Read Out Byte 32 Bit[7:0]: ROI 1 Y hist bin 14[7:0]
0x80207C91	ROI_1_READ_33	–	R	ROI 1 Read Out Byte 33 Bit[7:0]: ROI 1 Y hist bin 15[23:16]
0x80207C92	ROI_1_READ_34	–	R	ROI 1 Read Out Byte 34 Bit[7:0]: ROI 1 Y hist bin 15[15:8]

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table 4-50 YUV stat registers (sheet 10 of 15)

address	register name	default value	R/W	description
0x80207C93	ROI_1_READ_35	–	R	ROI 1 Read Out Byte 35 Bit[7:0]: ROI 1 Y hist bin 15[7:0]
0x80207C94	ROI_2_READ_00	–	R	ROI 2 Read Out Byte 00 Bit[7:0]: ROI 2 Y average[15:8]
0x80207C95	ROI_2_READ_01	–	R	ROI 2 Read Out Byte 01 Bit[7:0]: ROI 2 Y average[7:0]
0x80207C96	ROI_2_READ_02	–	R	ROI 2 Read Out Byte 02 Bit[7:0]: ROI 2 U average[15:8]
0x80207C97	ROI_2_READ_03	–	R	ROI 2 Read Out Byte 03 Bit[7:0]: ROI 2 U average[7:0]
0x80207C98	ROI_2_READ_04	–	R	ROI 2 Read Out Byte 04 Bit[7:0]: ROI 2 V average[15:8]
0x80207C99	ROI_2_READ_05	–	R	ROI 2 Read Out Byte 05 Bit[7:0]: ROI 2 V average[7:0]
0x80207C9A	ROI_2_READ_06	–	R	ROI 2 Read Out Byte 06 Bit[7:0]: ROI 2 Y hist bin 0[23:16]
0x80207C9B	ROI_2_READ_07	–	R	ROI 2 Read Out Byte 07 Bit[7:0]: ROI 2 Y hist bin 0[15:8]
0x80207C9C	ROI_2_READ_08	–	R	ROI 2 Read Out Byte 08 Bit[7:0]: ROI 2 Y hist bin 0[7:0]
0x80207C9D	ROI_2_READ_09	–	R	ROI 2 Read Out Byte 09 Bit[7:0]: ROI 2 Y hist bin 1[23:16]
0x80207C9E	ROI_2_READ_0A	–	R	ROI 2 Read Out Byte 0A Bit[7:0]: ROI 2 Y hist bin 1[15:8]
0x80207C9F	ROI_2_READ_0B	–	R	ROI 2 Read Out Byte 0B Bit[7:0]: ROI 2 Y hist bin 1[7:0]
0x80207CA0	ROI_2_READ_0C	–	R	ROI 2 Read Out Byte 0C Bit[7:0]: ROI 2 Y hist bin 2[23:16]
0x80207CA1	ROI_2_READ_0D	–	R	ROI 2 Read Out Byte 0D Bit[7:0]: ROI 2 Y hist bin 2[15:8]
0x80207CA2	ROI_2_READ_0E	–	R	ROI 2 Read Out Byte 0E Bit[7:0]: ROI 2 Y hist bin 2[7:0]
0x80207CA3	ROI_2_READ_0F	–	R	ROI 2 Read Out Byte 0F Bit[7:0]: ROI 2 Y hist bin 3[23:16]
0x80207CA4	ROI_2_READ_10	–	R	ROI 2 Read Out Byte 10 Bit[7:0]: ROI 2 Y hist bin 3[15:8]
0x80207CA5	ROI_2_READ_11	–	R	ROI 2 Read Out Byte 11 Bit[7:0]: ROI 2 Y hist bin 3[7:0]

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table 4-50 YUV stat registers (sheet 11 of 15)

address	register name	default value	R/W	description
0x80207CA6	ROI_2_READ_12	–	R	ROI 2 Read Out Byte 12 Bit[7:0]: ROI 2 Y hist bin 4[23:16]
0x80207CA7	ROI_2_READ_13	–	R	ROI 2 Read Out Byte 13 Bit[7:0]: ROI 2 Y hist bin 4[15:8]
0x80207CA8	ROI_2_READ_14	–	R	ROI 2 Read Out Byte 14 Bit[7:0]: ROI 2 Y hist bin 4[7:0]
0x80207CA9	ROI_2_READ_15	–	R	ROI 2 Read Out Byte 15 Bit[7:0]: ROI 2 Y hist bin 5[23:16]
0x80207CAA	ROI_2_READ_16	–	R	ROI 2 Read Out Byte 16 Bit[7:0]: ROI 2 Y hist bin 5[15:8]
0x80207CAB	ROI_2_READ_17	–	R	ROI 2 Read Out Byte 17 Bit[7:0]: ROI 2 Y hist bin 5[7:0]
0x80207CAC	ROI_2_READ_18	–	R	ROI 2 Read Out Byte 18 Bit[7:0]: ROI 2 Y hist bin 6[23:16]
0x80207CAD	ROI_2_READ_19	–	R	ROI 2 Read Out Byte 19 Bit[7:0]: ROI 2 Y hist bin 6[15:8]
0x80207CAE	ROI_2_READ_1A	–	R	ROI 2 Read Out Byte 1A Bit[7:0]: ROI 2 Y hist bin 6[7:0]
0x80207CAF	ROI_2_READ_1B	–	R	ROI 2 Read Out Byte 1B Bit[7:0]: ROI 2 Y hist bin 7[23:16]
0x80207CB0	ROI_2_READ_1C	–	R	ROI 2 Read Out Byte 1C Bit[7:0]: ROI 2 Y hist bin 7[15:8]
0x80207CB1	ROI_2_READ_1D	–	R	ROI 2 Read Out Byte 1D Bit[7:0]: ROI 2 Y hist bin 7[7:0]
0x80207CB2	ROI_2_READ_1E	–	R	ROI 2 Read Out Byte 1E Bit[7:0]: ROI 2 Y hist bin 8[23:16]
0x80207CB3	ROI_2_READ_1F	–	R	ROI 2 Read Out Byte 1F Bit[7:0]: ROI 2 Y hist bin 8[15:8]
0x80207CB4	ROI_2_READ_20	–	R	ROI 2 Read Out Byte 20 Bit[7:0]: ROI 2 Y hist bin 8[7:0]
0x80207CB5	ROI_2_READ_21	–	R	ROI 2 Read Out Byte 21 Bit[7:0]: ROI 2 Y hist bin 9[23:16]
0x80207CB6	ROI_2_READ_22	–	R	ROI 2 Read Out Byte 22 Bit[7:0]: ROI 2 Y hist bin 9[15:8]
0x80207CB7	ROI_2_READ_23	–	R	ROI 2 Read Out Byte 23 Bit[7:0]: ROI 2 Y hist bin 9[7:0]
0x80207CB8	ROI_2_READ_24	–	R	ROI 2 Read Out Byte 24 Bit[7:0]: ROI 2 Y hist bin 10[23:16]

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table 4-50 YUV stat registers (sheet 12 of 15)

address	register name	default value	R/W	description
0x80207CB9	ROI_2_READ_25	–	R	ROI 2 Read Out Byte 25 Bit[7:0]: ROI 2 Y hist bin 10[15:8]
0x80207CBA	ROI_2_READ_26	–	R	ROI 2 Read Out Byte 26 Bit[7:0]: ROI 2 Y hist bin 10[7:0]
0x80207CBB	ROI_2_READ_27	–	R	ROI 2 Read Out Byte 27 Bit[7:0]: ROI 2 Y hist bin 11[23:16]
0x80207CBC	ROI_2_READ_28	–	R	ROI 2 Read Out Byte 28 Bit[7:0]: ROI 2 Y hist bin 11[15:8]
0x80207CBD	ROI_2_READ_29	–	R	ROI 2 Read Out Byte 29 Bit[7:0]: ROI 2 Y hist bin 11[7:0]
0x80207CBE	ROI_2_READ_2A	–	R	ROI 2 Read Out Byte 2A Bit[7:0]: ROI 2 Y hist bin 12[23:16]
0x80207CBF	ROI_2_READ_2B	–	R	ROI 2 Read Out Byte 2B Bit[7:0]: ROI 2 Y hist bin 12[15:8]
0x80207CC0	ROI_2_READ_2C	–	R	ROI 2 Read Out Byte 2C Bit[7:0]: ROI 2 Y hist bin 12[7:0]
0x80207CC1	ROI_2_READ_2D	–	R	ROI 2 Read Out Byte 2D Bit[7:0]: ROI 2 Y hist bin 13[23:16]
0x80207CC2	ROI_2_READ_2E	–	R	ROI 2 Read Out Byte 2E Bit[7:0]: ROI 2 Y hist bin 13[15:8]
0x80207CC3	ROI_2_READ_2F	–	R	ROI 2 Read Out Byte 2F Bit[7:0]: ROI 2 Y hist bin 13[7:0]
0x80207CC4	ROI_2_READ_30	–	R	ROI 2 Read Out Byte 30 Bit[7:0]: ROI 2 Y hist bin 14[23:16]
0x80207CC5	ROI_2_READ_31	–	R	ROI 2 Read Out Byte 31 Bit[7:0]: ROI 2 Y hist bin 14[15:8]
0x80207CC6	ROI_2_READ_32	–	R	ROI 2 Read Out Byte 32 Bit[7:0]: ROI 2 Y hist bin 14[7:0]
0x80207CC7	ROI_2_READ_33	–	R	ROI 2 Read Out Byte 33 Bit[7:0]: ROI 2 Y hist bin 15[23:16]
0x80207CC8	ROI_2_READ_34	–	R	ROI 2 Read Out Byte 34 Bit[7:0]: ROI 2 Y hist bin 15[15:8]
0x80207CC9	ROI_2_READ_35	–	R	ROI 2 Read Out Byte 35 Bit[7:0]: ROI 2 Y hist bin 15[7:0]
0x80207CCA	ROI_3_READ_00	–	R	ROI 3 Read Out Byte 00 Bit[7:0]: ROI 3 Y average[15:8]
0x80207CCB	ROI_3_READ_01	–	R	ROI 3 Read Out Byte 01 Bit[7:0]: ROI 3 Y average[7:0]

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table 4-50 YUV stat registers (sheet 13 of 15)

address	register name	default value	R/W	description
0x80207CCC	ROI_3_READ_02	–	R	ROI 3 Read Out Byte 02 Bit[7:0]: ROI 3 U average[15:8]
0x80207CCD	ROI_3_READ_03	–	R	ROI 3 Read Out Byte 03 Bit[7:0]: ROI 3 U average[7:0]
0x80207CCE	ROI_3_READ_04	–	R	ROI 3 Read Out Byte 04 Bit[7:0]: ROI 3 V average[15:8]
0x80207CCF	ROI_3_READ_05	–	R	ROI 3 Read Out Byte 05 Bit[7:0]: ROI 3 V average[7:0]
0x80207CD0	ROI_3_READ_06	–	R	ROI 3 Read Out Byte 06 Bit[7:0]: ROI 3 Y hist bin 0[23:16]
0x80207CD1	ROI_3_READ_07	–	R	ROI 3 Read Out Byte 07 Bit[7:0]: ROI 3 Y hist bin 0[15:8]
0x80207CD2	ROI_3_READ_08	–	R	ROI 3 Read Out Byte 08 Bit[7:0]: ROI 3 Y hist bin 0[7:0]
0x80207CD3	ROI_3_READ_09	–	R	ROI 3 Read Out Byte 09 Bit[7:0]: ROI 3 Y hist bin 1[23:16]
0x80207CD4	ROI_3_READ_0A	–	R	ROI 3 Read Out Byte 0A Bit[7:0]: ROI 3 Y hist bin 1[15:8]
0x80207CD5	ROI_3_READ_0B	–	R	ROI 3 Read Out Byte 0B Bit[7:0]: ROI 3 Y hist bin 1[7:0]
0x80207CD6	ROI_3_READ_0C	–	R	ROI 3 Read Out Byte 0C Bit[7:0]: ROI 3 Y hist bin 2[23:16]
0x80207CD7	ROI_3_READ_0D	–	R	ROI 3 Read Out Byte 0D Bit[7:0]: ROI 3 Y hist bin 2[15:8]
0x80207CD8	ROI_3_READ_0E	–	R	ROI 3 Read Out Byte 0E Bit[7:0]: ROI 3 Y hist bin 2[7:0]
0x80207CD9	ROI_3_READ_0F	–	R	ROI 3 Read Out Byte 0F Bit[7:0]: ROI 3 Y hist bin 3[23:16]
0x80207CDA	ROI_3_READ_10	–	R	ROI 3 Read Out Byte 10 Bit[7:0]: ROI 3 Y hist bin 3[15:8]
0x80207CDB	ROI_3_READ_11	–	R	ROI 3 Read Out Byte 11 Bit[7:0]: ROI 3 Y hist bin 3[7:0]
0x80207CDC	ROI_3_READ_12	–	R	ROI 3 Read Out Byte 12 Bit[7:0]: ROI 3 Y hist bin 4[23:16]
0x80207CDD	ROI_3_READ_13	–	R	ROI 3 Read Out Byte 13 Bit[7:0]: ROI 3 Y hist bin 4[15:8]
0x80207CDE	ROI_3_READ_14	–	R	ROI 3 Read Out Byte 14 Bit[7:0]: ROI 3 Y hist bin 4[7:0]

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table 4-50 YUV stat registers (sheet 14 of 15)

address	register name	default value	R/W	description
0x80207CDF	ROI_3_READ_15	–	R	ROI 3 Read Out Byte 15 Bit[7:0]: ROI 3 Y hist bin 5[23:16]
0x80207CE0	ROI_3_READ_16	–	R	ROI 3 Read Out Byte 16 Bit[7:0]: ROI 3 Y hist bin 5[15:8]
0x80207CE1	ROI_3_READ_17	–	R	ROI 3 Read Out Byte 17 Bit[7:0]: ROI 3 Y hist bin 5[7:0]
0x80207CE2	ROI_3_READ_18	–	R	ROI 3 Read Out Byte 18 Bit[7:0]: ROI 3 Y hist bin 6[23:16]
0x80207CE3	ROI_3_READ_19	–	R	ROI 3 Read Out Byte 19 Bit[7:0]: ROI 3 Y hist bin 6[15:8]
0x80207CE4	ROI_3_READ_1A	–	R	ROI 3 Read Out Byte 1A Bit[7:0]: ROI 3 Y hist bin 6[7:0]
0x80207CE5	ROI_3_READ_1B	–	R	ROI 3 Read Out Byte 1B Bit[7:0]: ROI 3 Y hist bin 7[23:16]
0x80207CE6	ROI_3_READ_1C	–	R	ROI 3 Read Out Byte 1C Bit[7:0]: ROI 3 Y hist bin 7[15:8]
0x80207CE7	ROI_3_READ_1D	–	R	ROI 3 Read Out Byte 1D Bit[7:0]: ROI 3 Y hist bin 7[7:0]
0x80207CE8	ROI_3_READ_1E	–	R	ROI 3 Read Out Byte 1E Bit[7:0]: ROI 3 Y hist bin 8[23:16]
0x80207CE9	ROI_3_READ_1F	–	R	ROI 3 Read Out Byte 1F Bit[7:0]: ROI 3 Y hist bin 8[15:8]
0x80207CEA	ROI_3_READ_20	–	R	ROI 3 Read Out Byte 20 Bit[7:0]: ROI 3 Y hist bin 8[7:0]
0x80207CEB	ROI_3_READ_21	–	R	ROI 3 Read Out Byte 21 Bit[7:0]: ROI 3 Y hist bin 9[23:16]
0x80207CEC	ROI_3_READ_22	–	R	ROI 3 Read Out Byte 22 Bit[7:0]: ROI 3 Y hist bin 9[15:8]
0x80207CED	ROI_3_READ_23	–	R	ROI 3 Read Out Byte 23 Bit[7:0]: ROI 3 Y hist bin 9[7:0]
0x80207CEE	ROI_3_READ_24	–	R	ROI 3 Read Out Byte 24 Bit[7:0]: ROI 3 Y hist bin 10[23:16]
0x80207CEF	ROI_3_READ_25	–	R	ROI 3 Read Out Byte 25 Bit[7:0]: ROI 3 Y hist bin 10[15:8]
0x80207CF0	ROI_3_READ_26	–	R	ROI 3 Read Out Byte 26 Bit[7:0]: ROI 3 Y hist bin 10[7:0]
0x80207CF1	ROI_3_READ_27	–	R	ROI 3 Read Out Byte 27 Bit[7:0]: ROI 3 Y hist bin 11[23:16]

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table 4-50 YUV stat registers (sheet 15 of 15)

address	register name	default value	R/W	description
0x80207CF2	ROI_3_READ_28	–	R	ROI 3 Read Out Byte 28 Bit[7:0]: ROI 3 Y hist bin 11[15:8]
0x80207CF3	ROI_3_READ_29	–	R	ROI 3 Read Out Byte 29 Bit[7:0]: ROI 3 Y hist bin 11[7:0]
0x80207CF4	ROI_3_READ_2A	–	R	ROI 3 Read Out Byte 2A Bit[7:0]: ROI 3 Y hist bin 12[23:16]
0x80207CF5	ROI_3_READ_2B	–	R	ROI 3 Read Out Byte 2B Bit[7:0]: ROI 3 Y hist bin 12[15:8]
0x80207CF6	ROI_3_READ_2C	–	R	ROI 3 Read Out Byte 2C Bit[7:0]: ROI 3 Y hist bin 12[7:0]
0x80207CF7	ROI_3_READ_2D	–	R	ROI 3 Read Out Byte 2D Bit[7:0]: ROI 3 Y hist bin 13[23:16]
0x80207CF8	ROI_3_READ_2E	–	R	ROI 3 Read Out Byte 2E Bit[7:0]: ROI 3 Y hist bin 13[15:8]
0x80207CF9	ROI_3_READ_2F	–	R	ROI 3 Read Out Byte 2F Bit[7:0]: ROI 3 Y hist bin 13[7:0]
0x80207CFA	ROI_3_READ_30	–	R	ROI 3 Read Out Byte 30 Bit[7:0]: ROI 3 Y hist bin 14[23:16]
0x80207CFB	ROI_3_READ_31	–	R	ROI 3 Read Out Byte 31 Bit[7:0]: ROI 3 Y hist bin 14[15:8]
0x80207CFC	ROI_3_READ_32	–	R	ROI 3 Read Out Byte 32 Bit[7:0]: ROI 3 Y hist bin 14[7:0]
0x80207CFD	ROI_3_READ_33	–	R	ROI 3 Read Out Byte 33 Bit[7:0]: ROI 3 Y hist bin 15[23:16]
0x80207CFE	ROI_3_READ_34	–	R	ROI 3 Read Out Byte 34 Bit[7:0]: ROI 3 Y hist bin 15[15:8]
0x80207CFF	ROI_3_READ_35	–	R	ROI 3 Read Out Byte 35 Bit[7:0]: ROI 3 Y hist bin 15[7:0]

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4.41 firmware register table

table 4-51 to **table 4-56** list the firmware (FW) registers address offsets. The base address is 0x80180120. Besides using the firmware register R/W host command described in the *OV490 Application Note*, certain functions can be accessed by using the absolute address (base address + offset). The base address may be changed to a different value; therefore, OmniVision recommends host commands as their default values may change based on different firmware versions.

table 4-51 ISP general control register

address offset	register name	default value	R/W	description
0x00	TARGETNUM	0x01	RW	Bit[7:2]: Reserved Bit[1:0]: ABC target number
0x02	VTS_H	0x03	RW	Bit[7:0]: VTS[15:8]
0x03	VTS_L	0xEC	RW	Bit[7:0]: VTS[7:0]
0x04	EXPOSUREMODE	0x00	RW	Exposure Mode

table 4-52 AWB firmware registers (sheet 1 of 7)

address offset	register name	default value	R/W	description
0x0C	MAXAWBGAIN_0_H	0x07	RW	Max AWB Gain (B Gain) for L Channel
0x0D	MAXAWBGAIN_0_L	0xFF	RW	Max AWB Gain (B Gain) for L Channel
0x0E	MAXAWBGAIN_1_H	0x07	RW	Max AWB Gain (G Gain) for S Channel
0x0F	MAXAWBGAIN_1_L	0xFF	RW	Max AWB Gain (G Gain) for S Channel
0x10	MAXAWBGAIN_2_H	0x07	RW	Max AWB Gain (R Gain) for VS Channel
0x11	MAXAWBGAIN_2_L	0xFF	RW	Max AWB Gain (R Gain) for VS Channel
0x12	CURVEAWBOPTIONS	0xA1	RW	Bit[7]: Enable advanced AWB map Bit[6:0]: Reserved
0x20	CURVEAWBMINNUM_H	0x04	RW	AWB Minimum Statistics Number High Byte
0x21	CURVEAWBMINNUM_L	0x00	RW	AWB Minimum Statistics Number Low Byte
0x22	CURVEAWBXSCALE_H	0x00	RW	XScale High Byte
0x23	CURVEAWBXSCALE_L	0x2E	RW	XScale Low Byte
0x24	CURVEAWBYSCALE_H	0x00	RW	YScale High Byte
0x25	CURVEAWBYSCALE_L	0x19	RW	YScale Low Byte

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table 4-52 AWB firmware registers (sheet 2 of 7)

address offset	register name	default value	R/W	description
0x37	CURVEAWBDEBUG	0x00	RW	Debug Option
0x4C	ADJUSTSMALLPDGAIN ENBLE	0x01	RW	Bit[7:0]: Adjust short channel AWB gain enable
0x4D	ADAPTIVEPDGAINENABLE	0x00	RW	Bit[7:0]: Adaptive short channel AWB gain enable
0x4E	BRGAINTH_0_H	0x00	RW	Bit[7:0]: Day light threshold for B/G[15:8]
0x4F	BRGAINTH_0_L	0x81	RW	Bit[7:0]: Day light threshold for B/G[7:0]
0x50	BRGAINTH_1_H	0x00	RW	Bit[7:0]: CWF light threshold for B/G[15:8]
0x51	BRGAINTH_1_L	0xB0	RW	Bit[7:0]: CWF light threshold for B/G[7:0]
0x52	BRGAINTH_2_H	0x01	RW	Bit[7:0]: A light threshold for B/G[15:8]
0x53	BRGAINTH_2_L	0x1E	RW	Bit[7:0]: A light threshold for B/G[7:0]
0x54	PDGAINB_0_H	0x00	RW	Bit[7:0]: Blue gain for Day light[15:8]
0x55	PDGAINB_0_L	0x80	RW	Bit[7:0]: Blue gain for Day light[7:0]
0x56	PDGAINB_1_H	0x00	RW	Bit[7:0]: Blue gain for CWF light[15:8]
0x57	PDGAINB_1_L	0x80	RW	Bit[7:0]: Blue gain for CWF light[7:0]
0x58	PDGAINB_2_H	0x00	RW	Bit[7:0]: Blue gain for A light[15:8]
0x59	PDGAINB_2_L	0x80	RW	Bit[7:0]: Blue gain for A light[7:0]
0x5A	PDGAING_0_H	0x00	RW	Bit[7:0]: Green gain for Day light[15:8]
0x5B	PDGAING_0_L	0x94	RW	Bit[7:0]: Green gain for Day light[7:0]
0x5C	PDGAING_1_H	0x00	RW	Bit[7:0]: Green gain for CWF light[15:8]
0x5D	PDGAING_1_L	0x94	RW	Bit[7:0]: Green gain for CWF light[7:0]
0x5E	PDGAING_2_H	0x00	RW	Bit[7:0]: Green gain for A light[15:8]
0x5F	PDGAING_2_L	0x94	RW	Bit[7:0]: Green gain for A light[7:0]
0x60	PDGAINR_0_H	0x00	RW	Bit[7:0]: Red gain for Day light[15:8]
0x61	PDGAINR_0_L	0xA0	RW	Bit[7:0]: Red gain for Day light[7:0]
0x62	PDGAINR_1_H	0x00	RW	Bit[7:0]: Red gain for CWF light[15:8]
0x63	PDGAINR_1_L	0xA0	RW	Bit[7:0]: Red gain for CWF light[7:0]
0x64	PDGAINR_2_H	0x00	RW	Bit[7:0]: Red gain for A light[15:8]
0x65	PDGAINR_2_L	0xA0	RW	Bit[7:0]: Red gain for A light[7:0]

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table 4-52 AWB firmware registers (sheet 3 of 7)

address offset	register name	default value	R/W	description
0x66	AWBSTEP1	0x04	RW	Relative AWB Adjustment Step
0x67	AWBSTEP2	0x80	RW	Maximum Number of Adjustments
0x7C	MANUALAWBGAIN_0_0_H	0x01	RW	Manual AWB R Gain for L Channel High Byte
0x7D	MANUALAWBGAIN_0_0_L	0x28	RW	Manual AWB R Gain for L Channel Low Byte
0x7E	MANUALAWBGAIN_0_1_H	0x01	RW	Manual AWB Gr Gain for L Channel High Byte
0x7F	MANUALAWBGAIN_0_1_L	0x00	RW	Manual AWB Gr Gain for L Channel Low Byte
0x80	MANUALAWBGAIN_0_2_H	0x01	RW	Manual AWB Gb Gain for L Channel High Byte
0x81	MANUALAWBGAIN_0_2_L	0x00	RW	Manual AWB Gb Gain for L Channel Low Byte
0x82	MANUALAWBGAIN_0_3_H	0x02	RW	Manual AWB B Gain for L Channel High Byte
0x83	MANUALAWBGAIN_0_3_L	0x00	RW	Manual AWB B Gain for L Channel Low Byte
0x84	MANUALAWBGAIN_1_0_H	0x01	RW	Manual AWB R Gain for S Channel High Byte
0x85	MANUALAWBGAIN_1_0_L	0x28	RW	Manual AWB R Gain for S Channel Low Byte
0x86	MANUALAWBGAIN_1_1_H	0x01	RW	Manual AWB Gr Gain for S Channel High Byte
0x87	MANUALAWBGAIN_1_1_L	0x00	RW	Manual AWB Gr Gain for S Channel Low Byte
0x88	MANUALAWBGAIN_1_2_H	0x01	RW	Manual AWB Gb Gain for S Channel High Byte
0x89	MANUALAWBGAIN_1_2_L	0x00	RW	Manual AWB Gb Gain for S Channel Low Byte
0x8A	MANUALAWBGAIN_1_3_H	0x02	RW	Manual AWB B Gain for S Channel High Byte
0x8B	MANUALAWBGAIN_1_3_L	0x00	RW	Manual AWB B Gain for S Channel Low Byte
0x8C	MANUALAWBGAIN_2_0_H	0x01	RW	Manual AWB R Gain for VS Channel High Byte

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table 4-52 AWB firmware registers (sheet 4 of 7)

address offset	register name	default value	R/W	description
0x8D	MANUALAWBGAIN_2_0_L	0x28	RW	Manual AWB R Gain for VS Channel Low Byte
0x8E	MANUALAWBGAIN_2_1_H	0x01	RW	Manual AWB Gr Gain for VS Channel High Byte
0x8F	MANUALAWBGAIN_2_1_L	0x00	RW	Manual AWB Gr Gain for VS Channel Low Byte
0x90	MANUALAWBGAIN_2_2_H	0x01	RW	Manual AWB Gb Gain for VS Channel High Byte
0x91	MANUALAWBGAIN_2_2_L	0x00	RW	Manual AWB Gb Gain for VS Channel Low Byte
0x92	MANUALAWBGAIN_2_3_H	0x02	RW	Manual AWB B Gain for VS Channel High Byte
0x93	MANUALAWBGAIN_2_3_L	0x00	RW	Manual AWB B Gain for VS Channel Low Byte
0x94	MANUALAWBOFFSET_0_BYTE0	0x00	RW	ManualAWBOffset_0_Byte0
0x95	MANUALAWBOFFSET_0_BYTE1	0x00	RW	ManualAWBOffset_0_Byte1
0x96	MANUALAWBOFFSET_0_BYTE2	0x00	RW	ManualAWBOffset_0_Byte2
0x97	MANUALAWBOFFSET_0_BYTE3	0x00	RW	ManualAWBOffset_0_Byte3
0x98	MANUALAWBOFFSET_1_BYTE0	0x00	RW	ManualAWBOffset_1_Byte0
0x99	MANUALAWBOFFSET_1_BYTE1	0x00	RW	ManualAWBOffset_1_Byte1
0x9A	MANUALAWBOFFSET_1_BYTE2	0x00	RW	ManualAWBOffset_1_Byte2
0x9B	MANUALAWBOFFSET_1_BYTE3	0x00	RW	ManualAWBOffset_1_Byte3
0x9C	MANUALAWBOFFSET_2_BYTE0	0x00	RW	ManualAWBOffset_2_Byte0
0x9D	MANUALAWBOFFSET_2_BYTE1	0x00	RW	ManualAWBOffset_2_Byte1
0x9E	MANUALAWBOFFSET_2_BYTE2	0x00	RW	ManualAWBOffset_2_Byte2
0x9F	MANUALAWBOFFSET_2_BYTE3	0x00	RW	ManualAWBOffset_2_Byte3

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table 4-52 AWB firmware registers (sheet 5 of 7)

address offset	register name	default value	R/W	description
0xA0	MANUALAWBOFFSET_3_BYTE0	0x00	RW	ManualAWBOffset_3_Byte0
0xA1	MANUALAWBOFFSET_3_BYTE1	0x00	RW	ManualAWBOffset_3_Byte1
0xA2	MANUALAWBOFFSET_3_BYTE2	0x00	RW	ManualAWBOffset_3_Byte2
0xA3	MANUALAWBOFFSET_3_BYTE3	0x00	RW	ManualAWBOffset_3_Byte3
0xA4	MANUALAWBOFFSETS_0_BYTE0	0x00	RW	ManualAWBOffsetS_0_Byte0
0xA5	MANUALAWBOFFSETS_0_BYTE1	0x00	RW	ManualAWBOffsetS_0_Byte1
0xA6	MANUALAWBOFFSETS_0_BYTE2	0x00	RW	ManualAWBOffsetS_0_Byte2
0xA7	MANUALAWBOFFSETS_0_BYTE3	0x00	RW	ManualAWBOffsetS_0_Byte3
0xA8	MANUALAWBOFFSETS_1_BYTE0	0x00	RW	ManualAWBOffsetS_1_Byte0
0xA9	MANUALAWBOFFSETS_1_BYTE1	0x00	RW	ManualAWBOffsetS_1_Byte1
0xAA	MANUALAWBOFFSETS_1_BYTE2	0x00	RW	ManualAWBOffsetS_1_Byte2
0xAB	MANUALAWBOFFSETS_1_BYTE3	0x00	RW	ManualAWBOffsetS_1_Byte3
0xAC	MANUALAWBOFFSETS_2_BYTE0	0x00	RW	ManualAWBOffsetS_2_Byte0
0xAD	MANUALAWBOFFSETS_2_BYTE1	0x00	RW	ManualAWBOffsetS_2_Byte1
0xAE	MANUALAWBOFFSETS_2_BYTE2	0x00	RW	ManualAWBOffsetS_2_Byte2
0xAF	MANUALAWBOFFSETS_2_BYTE3	0x00	RW	ManualAWBOffsetS_2_Byte3
0xB0	MANUALAWBOFFSETS_3_BYTE0	0x00	RW	ManualAWBOffsetS_3_Byte0
0xB1	MANUALAWBOFFSETS_3_BYTE1	0x00	RW	ManualAWBOffsetS_3_Byte1
0xB2	MANUALAWBOFFSETS_3_BYTE2	0x00	RW	ManualAWBOffsetS_3_Byte2

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table 4-52 AWB firmware registers (sheet 6 of 7)

address offset	register name	default value	R/W	description
0xB3	MANUALAWBOFFSETS_3_BYTE3	0x00	RW	ManualAWBOffsetS_3_Byte3
0xB4	AWBREGIONLLBRTH0_H	0x08	RW	AWBRegionLLBrTh0 High Byte
0xB5	AWBREGIONLLBRTH0_L	0x20	RW	AWBRegionLLBrTh0 Low Byte
0xB6	AWBREGIONLLBRTH1_H	0x05	RW	AWBRegionLLBrTh1 High Byte
0xB7	AWBREGIONLLBRTH1_L	0x00	RW	AWBRegionLLBrTh1 Low Byte
0xB8	AWBREGIONLLBRTH2_H	0x04	RW	AWBRegionLLBrTh2 High Byte
0xB9	AWBREGIONLLBRTH2_L	0x10	RW	AWBRegionLLBrTh2 Low Byte
0xBA	AWBREGIONLLBRTH3_H	0x02	RW	AWBRegionLLBrTh3 High Byte
0xBB	AWBREGIONLLBRTH3_L	0x08	RW	AWBRegionLLBrTh3 Low Byte
0xBC	BGAINSHIFT_H	0x01	RW	Bit[7:0]: Long channel blue gain adjustment[15:8] Bgain = Bgain × BgainShift/128
0xBD	BGAINSHIFT_L	0x01	RW	Bit[7:0]: Long channel blue gain adjustment[7:0]
0xBE	GGAINSHIFT_H	0x01	RW	Bit[7:0]: Long channel green gain adjustment[15:8] Ggain = Ggain × GgainShift/128
0xBF	GGAINSHIFT_L	0x00	RW	Bit[7:0]: Long channel green gain adjustment[7:0]
0xC0	RGAINSHIFT_H	0x01	RW	Bit[7:0]: Long channel red gain adjustment[15:8] Rgain = Rgain × RgainShift/128
0xC1	RGAINSHIFT_L	0x00	RW	Bit[7:0]: Long channel red gain adjustment[7:0]
0xC2	MANUALAWBGAINSHIFT ENABLE	0x01	RW	Bit[0]: Post AWB shift function control 0: Disable 1: Enable
0xC3	AWBMAP_0	0x08	RW	Bit[7:0]: AWB map_0
0x142	AWBMAP_127	0x08	RW	Bit[7:0]: AWB map_127
0x143	MASK1_0	0xFF	RW	Mask1_0
0x162	MASK1_31	0xFF	RW	Mask1_31
0x163	MASK2_0	0xFF	RW	Mask2_0

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table 4-52 AWB firmware registers (sheet 7 of 7)

address offset	register name	default value	R/W	description
0x182	MASK2_31	0xFF	RW	Mask2_31
0x183	REGIONAWBMODE	0x00	RW	RegionAWBMode
0x184	REGIONSTATISTICS ENABLE	0x01	RW	RegionStatisticsEnable
0x195	NAWBSTABLERANGE_1	0x20	RW	AWB Stable Range Threshold 1
0x196	NAWBSTABLERANGE_2	0x40	RW	AWB Stable Range Threshold 2
0x8C4	MANUALAWBENABLE	0x00	RW	Manual AWB Enable 0: Disable 1: Enable

table 4-53 HDR firmware registers (sheet 1 of 12)

address offset	register name	default value	R/W	description
0x1A4	COMBINEERROR CONTROLPOINT_BYTE0	0x00	RW	Bit[7:0]: Threshold to enable combination error statistics calculation[31:24]
0x1A5	COMBINEERROR CONTROLPOINT_BYTE1	0x02	RW	Bit[7:0]: Threshold to enable combination error statistics calculation[23:16]
0x1A6	COMBINEERROR CONTROLPOINT_BYTE2	0x00	RW	Bit[7:0]: Threshold to enable combination error statistics calculation[15:8]
0x1A7	COMBINEERROR CONTROLPOINT_BYTE3	0x00	RW	Bit[7:0]: Threshold to enable combination error statistics calculation[7:0]
0x1A8	STEPE	0x02	RW	Combine Error Change Step
0x1A9	TONEMAPPINGENABLE	0x01	RW	Tone Mapping Enable 0: Disable 1: Enable
0x1AA	GAINENHANCEMENT CONTROL	0x01	RW	Auto Tone Curve Enhancement Level Reduction Enable 0: Disable 1: Enable
0x1AB	MANUALGAMMA ENABLE	0x00	RW	Bit[0]: Manual gamma Enable 0: Disable 1: Enable
0x1AC	AUTOTONEMAPPING CURVE	0x01	RW	Auto Tone Mapping Curve Enable 0: Disable 1: Enable

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table 4-53 HDR firmware registers (sheet 2 of 12)

address offset	register name	default value	R/W	description
0x1AD	CURVESTEP	0x02	RW	Tone Curve Change Step
0x1AE	HDRGAINSTEP	0x10	RW	Bit[7:0]: HDRGainStep
0x1B4	MINDYNAMICRANGE_H	0x00	RW	Bit[7:0]: EQ_α _DR_Thre1[15:8] EQ_ α _DR_Thre1 equals to 16 times of long short ratio
0x1B5	MINDYNAMICRANGE_L	0x10	RW	Bit[7:0]: EQ_α _DR_Thre1[7:0] EQ_ α _DR_Thre1 equals to 16 times of long short ratio
0x1B6	MAXDYNAMICRANGE_H	0x00	RW	Bit[7:0]: EQ_α _DR_Thre2[15:8] EQ_ α _DR_Thre2 equals to 16 times of long short ratio
0x1B7	MAXDYNAMICRANGE_L	0x40	RW	Bit[7:0]: EQ_α _DR_Thre2[7:0] EQ_ α _DR_Thre2 equals to 16 times of long short ratio
0x1B8	GAMMALIST_0_H	0x00	RW	Bit[7:0]: Base curve for tone curve P0[15:8]
0x1B9	GAMMALIST_0_L	0x2C	RW	Bit[7:0]: Base curve for tone curve P0[7:0]
0x1BA	GAMMALIST_1_H	0x00	RW	Bit[7:0]: Base curve for tone curve P1[15:8]
0x1BB	GAMMALIST_1_L	0x9B	RW	Bit[7:0]: Base curve for tone curve P1[7:0]
0x1BC	GAMMALIST_2_H	0x00	RW	Bit[7:0]: Base curve for tone curve P2[15:8]
0x1BD	GAMMALIST_2_L	0xD4	RW	Bit[7:0]: Base curve for tone curve P2[7:0]
0x1BE	GAMMALIST_3_H	0x01	RW	Bit[7:0]: Base curve for tone curve P3[15:8]
0x1BF	GAMMALIST_3_L	0x22	RW	Bit[7:0]: Base curve for tone curve P3[7:0]
0x1C0	GAMMALIST_4_H	0x01	RW	Bit[7:0]: Base curve for tone curve P4[15:8]
0x1C1	GAMMALIST_4_L	0x8E	RW	Bit[7:0]: Base curve for tone curve P4[7:0]
0x1C2	GAMMALIST_5_H	0x01	RW	Bit[7:0]: Base curve for tone curve P5[15:8]
0x1C3	GAMMALIST_5_L	0xD2	RW	Bit[7:0]: Base curve for tone curve P5[7:0]
0x1C4	GAMMALIST_6_H	0x02	RW	Bit[7:0]: Base curve for tone curve P6[15:8]
0x1C5	GAMMALIST_6_L	0x21	RW	Bit[7:0]: Base curve for tone curve P6[7:0]
0x1C6	GAMMALIST_7_H	0x02	RW	Bit[7:0]: Base curve for tone curve P7[15:8]
0x1C7	GAMMALIST_7_L	0x4E	RW	Bit[7:0]: Base curve for tone curve P7[7:0]
0x1C8	GAMMALIST_8_H	0x02	RW	Bit[7:0]: Base curve for tone curve P8[15:8]
0x1C9	GAMMALIST_8_L	0x7E	RW	Bit[7:0]: Base curve for tone curve P8[7:0]
0x1CA	GAMMALIST_9_H	0x02	RW	Bit[7:0]: Base curve for tone curve P9[15:8]

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table 4-53 HDR firmware registers (sheet 3 of 12)

address offset	register name	default value	R/W	description
0x1CB	GAMMALIST_9_L	0xB3	RW	Bit[7:0]: Base curve for tone curve P9[7:0]
0x1CC	GAMMALIST_10_H	0x02	RW	Bit[7:0]: Base curve for tone curve P10[15:8]
0x1CD	GAMMALIST_10_L	0xEB	RW	Bit[7:0]: Base curve for tone curve P10[7:0]
0x1CE	GAMMALIST_11_H	0x03	RW	Bit[7:0]: Base curve for tone curve P11[15:8]
0x1CF	GAMMALIST_11_L	0x29	RW	Bit[7:0]: Base curve for tone curve P11[7:0]
0x1D0	GAMMALIST_12_H	0x03	RW	Bit[7:0]: Base curve for tone curve P12[15:8]
0x1D1	GAMMALIST_12_L	0x6B	RW	Bit[7:0]: Base curve for tone curve P12[7:0]
0x1D2	GAMMALIST_13_H	0x03	RW	Bit[7:0]: Base curve for tone curve P13[15:8]
0x1D3	GAMMALIST_13_L	0xB2	RW	Bit[7:0]: Base curve for tone curve P13[7:0]
0x1D4	GAMMALIST_14_H	0x03	RW	Bit[7:0]: Base curve for tone curve P14[15:8]
0x1D5	GAMMALIST_14_L	0xD8	RW	Bit[7:0]: Base curve for tone curve P14[7:0]
0x1D6	GAMMALIST_15_H	0x03	RW	Bit[7:0]: Base curve for tone curve P15[15:8]
0x1D7	GAMMALIST_15_L	0xFF	RW	Bit[7:0]: Base curve for tone curve P15[7:0]
0x1D8	LIGHTCURVE_0_H	0x01	RW	Bit[7:0]: High bound of tone curve P0[15:8]
0x1D9	LIGHTCURVE_0_L	0x28	RW	Bit[7:0]: High bound of tone curve P0[7:0]
0x1DA	LIGHTCURVE_1_H	0x01	RW	Bit[7:0]: High bound of tone curve P1[15:8]
0x1DB	LIGHTCURVE_1_L	0x45	RW	Bit[7:0]: High bound of tone curve P1[7:0]
0x1DC	LIGHTCURVE_2_H	0x01	RW	Bit[7:0]: High bound of tone curve P2[15:8]
0x1DD	LIGHTCURVE_2_L	0x88	RW	Bit[7:0]: High bound of tone curve P2[7:0]
0x1DE	LIGHTCURVE_3_H	0x01	RW	Bit[7:0]: High bound of tone curve P3[15:8]
0x1DF	LIGHTCURVE_3_L	0xEE	RW	Bit[7:0]: High bound of tone curve P3[7:0]
0x1E0	LIGHTCURVE_4_H	0x02	RW	Bit[7:0]: High bound of tone curve P4[15:8]
0x1E1	LIGHTCURVE_4_L	0x17	RW	Bit[7:0]: High bound of tone curve P4[7:0]
0x1E2	LIGHTCURVE_5_H	0x02	RW	Bit[7:0]: High bound of tone curve P5[15:8]
0x1E3	LIGHTCURVE_5_L	0x40	RW	Bit[7:0]: High bound of tone curve P5[7:0]
0x1E4	LIGHTCURVE_6_H	0x02	RW	Bit[7:0]: High bound of tone curve P6[15:8]
0x1E5	LIGHTCURVE_6_L	0x6B	RW	Bit[7:0]: High bound of tone curve P6[7:0]

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table 4-53 HDR firmware registers (sheet 4 of 12)

address offset	register name	default value	R/W	description
0x1E6	LIGHTCURVE_7_H	0x02	RW	Bit[7:0]: High bound of tone curve P7[15:8]
0x1E7	LIGHTCURVE_7_L	0x98	RW	Bit[7:0]: High bound of tone curve P7[7:0]
0x1E8	LIGHTCURVE_8_H	0x02	RW	Bit[7:0]: High bound of tone curve P8[15:8]
0x1E9	LIGHTCURVE_8_L	0xC2	RW	Bit[7:0]: High bound of tone curve P8[7:0]
0x1EA	LIGHTCURVE_9_H	0x02	RW	Bit[7:0]: High bound of tone curve P9[15:8]
0x1EB	LIGHTCURVE_9_L	0xE7	RW	Bit[7:0]: High bound of tone curve P9[7:0]
0x1EC	LIGHTCURVE_10_H	0x03	RW	Bit[7:0]: High bound of tone curve P10[15:8]
0x1ED	LIGHTCURVE_10_L	0x20	RW	Bit[7:0]: High bound of tone curve P10[7:0]
0x1EE	LIGHTCURVE_11_H	0x03	RW	Bit[7:0]: High bound of tone curve P11[15:8]
0x1EF	LIGHTCURVE_11_L	0x4E	RW	Bit[7:0]: High bound of tone curve P11[7:0]
0x1F0	LIGHTCURVE_12_H	0x03	RW	Bit[7:0]: High bound of tone curve P12[15:8]
0x1F1	LIGHTCURVE_12_L	0x89	RW	Bit[7:0]: High bound of tone curve P12[7:0]
0x1F2	LIGHTCURVE_13_H	0x03	RW	Bit[7:0]: High bound of tone curve P13[15:8]
0x1F3	LIGHTCURVE_13_L	0xBF	RW	Bit[7:0]: High bound of tone curve P13[7:0]
0x1F4	LIGHTCURVE_14_H	0x03	RW	Bit[7:0]: High bound of tone curve P14[15:8]
0x1F5	LIGHTCURVE_14_L	0xE0	RW	Bit[7:0]: High bound of tone curve P14[7:0]
0x1F6	LIGHTCURVE_15_H	0x03	RW	Bit[7:0]: High bound of tone curve P15[15:8]
0x1F7	LIGHTCURVE_15_L	0xFF	RW	Bit[7:0]: High bound of tone curve P15[7:0]
0x1F8	DARKCURVE_0_H	0x00	RW	Bit[7:0]: Low bound of tone curve P0[15:8]
0x1F9	DARKCURVE_0_L	0x11	RW	Bit[7:0]: Low bound of tone curve P0[7:0]
0x1FA	DARKCURVE_1_H	0x00	RW	Bit[7:0]: Low bound of tone curve P1[15:8]
0x1FB	DARKCURVE_1_L	0x28	RW	Bit[7:0]: Low bound of tone curve P1[7:0]
0x1FC	DARKCURVE_2_H	0x00	RW	Bit[7:0]: Low bound of tone curve P2[15:8]
0x1FD	DARKCURVE_2_L	0x5B	RW	Bit[7:0]: Low bound of tone curve P[7:0]
0x1FE	DARKCURVE_3_H	0x00	RW	Bit[7:0]: Low bound of tone curve P3[15:8]
0x1FF	DARKCURVE_3_L	0xC8	RW	Bit[7:0]: Low bound of tone curve P3[7:0]
0x200	DARKCURVE_4_H	0x01	RW	Bit[7:0]: Low bound of tone curve P4[15:8]
0x201	DARKCURVE_4_L	0x09	RW	Bit[7:0]: Low bound of tone curve P4[7:0]
0x202	DARKCURVE_5_H	0x01	RW	Bit[7:0]: Low bound of tone curve P5[15:8]
0x203	DARKCURVE_5_L	0x57	RW	Bit[7:0]: Low bound of tone curve P5[7:0]

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table 4-53 HDR firmware registers (sheet 5 of 12)

address offset	register name	default value	R/W	description
0x204	DARKCURVE_6_H	0x01	RW	Bit[7:0]: Low bound of tone curve P6[15:8]
0x205	DARKCURVE_6_L	0x9B	RW	Bit[7:0]: Low bound of tone curve P6[7:0]
0x206	DARKCURVE_7_H	0x01	RW	Bit[7:0]: Low bound of tone curve P7[15:8]
0x207	DARKCURVE_7_L	0xD4	RW	Bit[7:0]: Low bound of tone curve P7[7:0]
0x208	DARKCURVE_8_H	0x02	RW	Bit[7:0]: Low bound of tone curve P8[15:8]
0x209	DARKCURVE_8_L	0x01	RW	Bit[7:0]: Low bound of tone curve P8[7:0]
0x20A	DARKCURVE_9_H	0x02	RW	Bit[7:0]: Low bound of tone curve P9[15:8]
0x20B	DARKCURVE_9_L	0x25	RW	Bit[7:0]: Low bound of tone curve P9[7:0]
0x20C	DARKCURVE_10_H	0x02	RW	Bit[7:0]: Low bound of tone curve P10[15:8]
0x20D	DARKCURVE_10_L	0x64	RW	Bit[7:0]: Low bound of tone curve P10[7:0]
0x20E	DARKCURVE_11_H	0x02	RW	Bit[7:0]: Low bound of tone curve P11[15:8]
0x20F	DARKCURVE_11_L	0x9B	RW	Bit[7:0]: Low bound of tone curve P11[7:0]
0x210	DARKCURVE_12_H	0x02	RW	Bit[7:0]: Low bound of tone curve P12[15:8]
0x211	DARKCURVE_12_L	0xF9	RW	Bit[7:0]: Low bound of tone curve P12[7:0]
0x212	DARKCURVE_13_H	0x03	RW	Bit[7:0]: Low bound of tone curve P13[15:8]
0x213	DARKCURVE_13_L	0x4E	RW	Bit[7:0]: Low bound of tone curve P13[7:0]
0x214	DARKCURVE_14_H	0x03	RW	Bit[7:0]: Low bound of tone curve P14[15:8]
0x215	DARKCURVE_14_L	0x99	RW	Bit[7:0]: Low bound of tone curve P14[7:0]
0x216	DARKCURVE_15_H	0x03	RW	Bit[7:0]: Low bound of tone curve P15[15:8]
0x217	DARKCURVE_15_L	0xFF	RW	Bit[7:0]: Low bound of tone curve P15[7:0]
0x218	MANUALTONECURVE_0_H	0x00	RW	Bit[7:0]: Manual tone curve P0[15:8]
0x219	MANUALTONECURVE_0_L	0x01	RW	Bit[7:0]: Manual tone curve P0[7:0]
0x21A	MANUALTONECURVE_1_H	0x00	RW	Bit[7:0]: Manual tone curve P1[15:8]
0x21B	MANUALTONECURVE_1_L	0x10	RW	Bit[7:0]: Manual tone curve P1[7:0]
0x21C	MANUALTONECURVE_2_H	0x00	RW	Bit[7:0]: Manual tone curve P2[15:8]
0x21D	MANUALTONECURVE_2_L	0x20	RW	Bit[7:0]: Manual tone curve P2[7:0]

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table 4-53 HDR firmware registers (sheet 6 of 12)

address offset	register name	default value	R/W	description
0x21E	MANUALTONECURVE_3_H	0x00	RW	Bit[7:0]: Manual tone curve P3[15:8]
0x21F	MANUALTONECURVE_3_L	0x40	RW	Bit[7:0]: Manual tone curve P3[7:0]
0x220	MANUALTONECURVE_4_H	0x00	RW	Bit[7:0]: Manual tone curve P4[15:8]
0x221	MANUALTONECURVE_4_L	0x80	RW	Bit[7:0]: Manual tone curve P4[7:0]
0x222	MANUALTONECURVE_5_H	0x00	RW	Bit[7:0]: Manual tone curve P5[15:8]
0x223	MANUALTONECURVE_5_L	0xB5	RW	Bit[7:0]: Manual tone curve P5[7:0]
0x224	MANUALTONECURVE_6_H	0x01	RW	Bit[7:0]: Manual tone curve P6[15:8]
0x225	MANUALTONECURVE_6_L	0x00	RW	Bit[7:0]: Manual tone curve P6[7:0]
0x226	MANUALTONECURVE_7_H	0x01	RW	Bit[7:0]: Manual tone curve P7[15:8]
0x227	MANUALTONECURVE_7_L	0x30	RW	Bit[7:0]: Manual tone curve P7[7:0]
0x228	MANUALTONECURVE_8_H	0x01	RW	Bit[7:0]: Manual tone curve P8[15:8]
0x229	MANUALTONECURVE_8_L	0x6A	RW	Bit[7:0]: Manual tone curve P8[7:0]
0x22A	MANUALTONECURVE_9_H	0x01	RW	Bit[7:0]: Manual tone curve P9[15:8]
0x22B	MANUALTONECURVE_9_L	0xAF	RW	Bit[7:0]: Manual tone curve P9[7:0]
0x22C	MANUALTONECURVE_10_H	0x02	RW	Bit[7:0]: Manual tone curve P10[15:8]
0x22D	MANUALTONECURVE_10_L	0x00	RW	Bit[7:0]: Manual tone curve P10[7:0]
0x22E	MANUALTONECURVE_11_H	0x02	RW	Bit[7:0]: Manual tone curve P11[15:8]
0x22F	MANUALTONECURVE_11_L	0x61	RW	Bit[7:0]: Manual tone curve P11[7:0]
0x230	MANUALTONECURVE_12_H	0x02	RW	Bit[7:0]: Manual tone curve P12[15:8]

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table 4-53 HDR firmware registers (sheet 7 of 12)

address offset	register name	default value	R/W	description
0x231	MANUALTONECURVE_12_L	0xD4	RW	Bit[7:0]: Manual tone curve P12[7:0]
0x232	MANUALTONECURVE_13_H	0x03	RW	Bit[7:0]: Manual tone curve P13[15:8]
0x233	MANUALTONECURVE_13_L	0x5D	RW	Bit[7:0]: Manual tone curve P13[7:0]
0x234	MANUALTONECURVE_14_H	0x03	RW	Bit[7:0]: Manual tone curve P14[15:8]
0x235	MANUALTONECURVE_14_L	0xAB	RW	Bit[7:0]: Manual tone curve P14[7:0]
0x236	MANUALTONECURVE_15_H	0x03	RW	Bit[7:0]: Manual tone curve P15[15:8]
0x237	MANUALTONECURVE_15_L	0xFF	RW	Bit[7:0]: Manual tone curve P15[7:0]
0x238	MINGAMMALIST_0_H	0x01	RW	Bit[7:0]: Min tone compression gamma list 1[15:8]
0x239	MINGAMMALIST_0_L	0x00	RW	Bit[7:0]: Min tone compression gamma list 1[7:0]
0x23A	MINGAMMALIST_1_H	0x01	RW	Bit[7:0]: Min tone compression gamma list 2[15:8]
0x23B	MINGAMMALIST_1_L	0x00	RW	Bit[7:0]: Min tone compression gamma list 2[7:0]
0x23C	MINGAMMALIST_2_H	0x01	RW	Bit[7:0]: Min tone compression gamma list 3[15:8]
0x23D	MINGAMMALIST_2_L	0x00	RW	Bit[7:0]: Min tone compression gamma list 3[7:0]
0x23E	MAXGAMMALIST_0_H	0x01	RW	Bit[7:0]: Max tone compression gamma list 1[15:8]
0x23F	MAXGAMMALIST_0_L	0x32	RW	Bit[7:0]: Max tone compression gamma list 1[7:0]
0x240	MAXGAMMALIST_1_H	0x01	RW	Bit[7:0]: Max tone compression gamma list 2[15:8]
0x241	MAXGAMMALIST_1_L	0xE8	RW	Bit[7:0]: Max tone compression gamma list 2[7:0]
0x242	MAXGAMMALIST_2_H	0x02	RW	Bit[7:0]: Max tone compression gamma list 3[15:8]
0x243	MAXGAMMALIST_2_L	0x74	RW	Bit[7:0]: Max tone compression gamma list 3[7:0]

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table 4-53 HDR firmware registers (sheet 8 of 12)

address offset	register name	default value	R/W	description
0x244	DYNAMICRANGELIST_0_H	0x00	RW	Bit[7:0]: Dynamic range list 1[15:8]
0x245	DYNAMICRANGELIST_0_L	0x10	RW	Bit[7:0]: Dynamic range list 1[7:0]
0x246	DYNAMICRANGELIST_1_H	0x00	RW	Bit[7:0]: Dynamic range list 2[15:8]
0x247	DYNAMICRANGELIST_1_L	0x40	RW	Bit[7:0]: Dynamic range list 2[7:0]
0x248	DYNAMICRANGELIST_2_H	0x00	RW	Bit[7:0]: Dynamic range list 3[15:8]
0x249	DYNAMICRANGELIST_2_L	0x80	RW	Bit[7:0]: Dynamic range list 3[7:0]
0x24A	MANUALGAMMA_H	0x00	RW	Bit[7:0]: Manual tone compression gamma[15:8]
0x24B	MANUALGAMMA_L	0x32	RW	Bit[7:0]: Manual tone compression gamma[7:0]
0x24C	LOGTARGETY_A_H	0x97	RW	Bit[7:0]: Image mean value target for frame A in ABC mode[15:8]
0x24D	LOGTARGETY_A_L	0x00	RW	Bit[7:0]: Image mean value target for frame A in ABC mode[7:0]
0x24E	LOGTARGETY_B_H	0x97	RW	Bit[7:0]: Image mean value target for frame B in ABC mode[15:8]
0x24F	LOGTARGETY_B_L	0x00	RW	Bit[7:0]: Image mean value target for frame B in ABC mode[7:0]
0x250	LOGTARGETY_C_H	0x97	RW	Bit[7:0]: Image mean value target for frame C in ABC mode[15:8]
0x251	LOGTARGETY_C_L	0x00	RW	Bit[7:0]: Image mean value target for frame C in ABC mode[7:0]
0x252	SHAPESMOOTH ENABLE	0x01	RW	Bit[0]: Tone curve smooth enable 0: Disable 1: Enable
0x253	MINSATURATELEVEL	0x10	RW	Bit[7:0]: Minimum saturate level for VS/short
0x254	GLOBALGAMMASTEP	0x04	RW	Bit[7:0]: Tone compression gamma step
0x255	REDUCENOISEINDARK ENABLE	0x00	RW	Bit[7:0]: Reduce noise for dark scenes enable 0: Disable 1: Enable

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table 4-53 HDR firmware registers (sheet 9 of 12)

address offset	register name	default value	R/W	description
0x256	REDUCENOISEMAX GAIN_H	0x02	RW	Bit[0]: High gain boundary for reduce noise function[15:8]
0x257	REDUCENOISEMAX GAIN_L	0x00	RW	Bit[7:0]: High gain boundary for reduce noise function[7:0]
0x258	REDUCENOISEMINGAIN _H	0x00	RW	Bit[7:0]: Low gain boundary for reduce noise function[15:8]
0x259	REDUCENOISEMINGAIN _L	0xA0	RW	Bit[7:0]: Low gain boundary for reduce noise function[7:0]
0x25A	REDUCENOISESTEP	0x02	RW	Bit[7:0]: Gain step value for reduce noise
0x25B	GLOBALMEANW	0x00	RW	Bit[7:0]: Current global mean value weight to the final target
0x25C	GAMMASTEP	0x04	RW	Bit[7:0]: Tone compression gamma change step
0x25D	FRAMESTABLE	0x05	RW	Frame Stable Number For Saturated Pixel Preserved Mode (2^framestable)
0x25E	SATURATEDPIXEL PRESERVED	0x00	RW	Saturated Pixel Preserved Mode 0: Disable 1: Enable
0x25F	GLOBALGAMMASHIFT ENABLE	0x00	RW	Tone Compression Gamma Shift Enable 0: Disable 1: Enable
0x260	GLOBALGAMMASHIFT	0x00	RW	Tone Compression Gamma Shift Value
0x261	LOCALENHANCEMENT LEVEL	0x21	RW	Local Enhancement Level
0x262	LOWCONTRASTLEVEL	0x01	RW	Bit[7:0]: Min_α Minimum weight of histogram equalization curve when dynamic range is below EQ_α _DR_Thre1
0x263	HIGHCONTRASTLEVEL	0x03	RW	Bit[7:0]: Max_α Maximum weight of histogram equalization curve when dynamic range is above EQ_α _DR_Thre2
0x264	SPREMATRIXENABLE	0x00	RW	SPD Pre Matrix Enable 0: Disable 1: Enable
0x265	SPREAUTOCTENABLE	0x01	RW	SPD Pre Matrix Illuminant Adaptation Enable 0: Disable 1: Enable
0x266	EXPCHANGELOGTH_H	0x00	RW	Bit[7:0]: Exposure change threshold[15:8]

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table 4-53 HDR firmware registers (sheet 10 of 12)

address offset	register name	default value	R/W	description
0x267	EXPCHANGELOGTH_L	0x10	RW	Bit[7:0]: Exposure change threshold[7:0]
0x268	YTH0TARGET_0_H	0x78	RW	Bit[7:0]: Dark contrast enhancement Y th0[15:8]
0x269	YTH0TARGET_0_L	0x00	RW	Bit[7:0]: Dark contrast enhancement Y th0[7:0]
0x26A	YTH1TARGET_1_H	0x80	RW	Bit[7:0]: Dark contrast enhancement Y th1[15:8]
0x26B	YTH1TARGET_1_L	0x00	RW	Bit[7:0]: Dark contrast enhancement Y th1[7:0]
0x26C	YTH0TARGET_2_H	0x98	RW	Bit[7:0]: Dark contrast enhancement Y th2[15:8]
0x26D	YTH0TARGET_2_L	0x00	RW	Bit[7:0]: Dark contrast enhancement Y th2[7:0]
0x26E	YTH1TARGET_3_H	0x9C	RW	Bit[7:0]: Dark contrast enhancement Y th3[15:8]
0x26F	YTH1TARGET_3_L	0xEC	RW	Bit[7:0]: Dark contrast enhancement Y th3[7:0]
0x270	SPRECTLIST_0_H	0x00	RW	Bit[7:0]: B/R for D65[15:8]
0x271	SPRECTLIST_0_L	0x98	RW	Bit[7:0]: B/R for D65[7:0]
0x272	SPRECTLIST_1_H	0x00	RW	Bit[7:0]: B/R for CWF[15:8]
0x273	SPRECTLIST_1_L	0xAC	RW	Bit[7:0]: B/R for CWF[7:0]
0x274	SPRECTLIST_2_H	0x01	RW	Bit[7:0]: B/R for A[15:8]
0x275	SPRECTLIST_2_L	0x00	RW	Bit[7:0]: B/R for A[7:0]
0x276	INVMLMS_D_0_0_H	0x01	RW	Bit[7:0]: SPD to LPD D65 matrix 00[15:8]
0x277	INVMLMS_D_0_0_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 00[7:0]
0x278	INVMLMS_D_0_1_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 01[15:8]
0x279	INVMLMS_D_0_1_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 01[7:0]
0x27A	INVMLMS_D_0_2_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 02[15:8]
0x27B	INVMLMS_D_0_2_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 02[7:0]
0x27C	INVMLMS_D_1_0_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 10[15:8]
0x27D	INVMLMS_D_1_0_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 10[7:0]
0x27E	INVMLMS_D_1_1_H	0x01	RW	Bit[7:0]: SPD to LPD D65 matrix 11[15:8]
0x27F	INVMLMS_D_1_1_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 11[7:0]

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table 4-53 HDR firmware registers (sheet 11 of 12)

address offset	register name	default value	R/W	description
0x280	INVMLMS_D_1_2_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 12[15:8]
0x281	INVMLMS_D_1_2_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 12[7:0]
0x282	INVMLMS_D_2_0_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 20[15:8]
0x283	INVMLMS_D_2_0_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 20[7:0]
0x284	INVMLMS_D_2_1_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 21[15:8]
0x285	INVMLMS_D_2_1_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 21[7:0]
0x286	INVMLMS_D_2_2_H	0x01	RW	Bit[7:0]: SPD to LPD D65 matrix 22[15:8]
0x287	INVMLMS_D_2_2_L	0x00	RW	Bit[7:0]: B/R for D65[15:8]
0x288	INVMLMS_C_0_0_H	0x01	RW	Bit[7:0]: B/R for D65[7:0]
0x289	INVMLMS_C_0_0_L	0x00	RW	Bit[7:0]: B/R for CWF[15:8]
0x28A	INVMLMS_C_0_1_H	0x00	RW	Bit[7:0]: B/R for CWF[7:0]
0x28B	INVMLMS_C_0_1_L	0x00	RW	Bit[7:0]: B/R for A[15:8]
0x28C	INVMLMS_C_0_2_H	0x00	RW	Bit[7:0]: B/R for A[7:0]
0x28D	INVMLMS_C_0_2_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 00[15:8]
0x28E	INVMLMS_C_1_0_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 00[7:0]
0x28F	INVMLMS_C_1_0_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 01[15:8]
0x290	INVMLMS_C_1_1_H	0x01	RW	Bit[7:0]: SPD to LPD D65 matrix 01[7:0]
0x291	INVMLMS_C_1_1_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 02[15:8]
0x292	INVMLMS_C_1_2_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 02[7:0]
0x293	INVMLMS_C_1_2_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 10[15:8]
0x294	INVMLMS_C_2_0_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 10[7:0]
0x295	INVMLMS_C_2_0_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 11[15:8]
0x296	INVMLMS_C_2_1_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 11[7:0]
0x297	INVMLMS_C_2_1_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 12[15:8]
0x298	INVMLMS_C_2_2_H	0x01	RW	Bit[7:0]: SPD to LPD D65 matrix 12[7:0]
0x299	INVMLMS_C_2_2_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 20[15:8]
0x29A	INVMLMS_A_0_0_H	0x01	RW	Bit[7:0]: SPD to LPD D65 matrix 20[7:0]
0x29B	INVMLMS_A_0_0_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 21[15:8]
0x29C	INVMLMS_A_0_1_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 21[7:0]
0x29D	INVMLMS_A_0_1_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 22[15:8]

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table 4-53 HDR firmware registers (sheet 12 of 12)

address offset	register name	default value	R/W	description
0x29E	INVMLMS_A_0_2_H	0x00	RW	Bit[7:0]: B/R for D65[15:8]
0x29F	INVMLMS_A_0_2_L	0x00	RW	Bit[7:0]: B/R for D65[7:0]
0x2A0	INVMLMS_A_1_0_H	0x00	RW	Bit[7:0]: B/R for CWF[15:8]
0x2A1	INVMLMS_A_1_0_L	0x00	RW	Bit[7:0]: B/R for CWF[7:0]
0x2A2	INVMLMS_A_1_1_H	0x01	RW	Bit[7:0]: B/R for A[15:8]
0x2A3	INVMLMS_A_1_1_L	0x00	RW	Bit[7:0]: B/R for A[7:0]
0x2A4	INVMLMS_A_1_2_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 00[15:8]
0x2A5	INVMLMS_A_1_2_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 00[7:0]
0x2A6	INVMLMS_A_2_0_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 01[15:8]
0x2A7	INVMLMS_A_2_0_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 01[7:0]
0x2A8	INVMLMS_A_2_1_H	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 02[15:8]
0x2A9	INVMLMS_A_2_1_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 02[7:0]
0x2AA	INVMLMS_A_2_2_H	0x01	RW	Bit[7:0]: SPD to LPD D65 matrix 10[15:8]
0x2AB	INVMLMS_A_2_2_L	0x00	RW	Bit[7:0]: SPD to LPD D65 matrix 10[7:0]
0x2AC	LOGTARGETLD_H	0x98	RW	Bit[7:0]: Low dynamic range scene target[15:8]
0x2AD	LOGTARGETLD_L	0x00	RW	Bit[7:0]: Low dynamic range scene target[7:0]
0x2B2	MANUALHDRGAIN ENABLE	0x00	RW	Manual HDR Gain Enable
0x2B4	MANUALHDRGAIN_H	0x01	RW	Manual HDR Gain High Byte
0x2B5	MANUALHDRGAIN_L	0x00	RW	Manual HDR Gain Low Byte
0x2B6	MAXSUPPRESSGAIN_H	0x03	RW	Bit[7:0]: Max suppress gain for shadow and highlights[15:8]
0x2B7	MAXSUPPRESSGAIN_L	0x00	RW	Bit[7:0]: Max suppress gain for shadow and highlights[7:0]
0x2B8	MANUALSUPPRESS GAIN	0x01	RW	Bit[7:0]: Manual suppress gain enable

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table 4-54 AEC firmware registers (sheet 1 of 8)

address offset	register name	default value	R/W	description
0x2D1	BLCBASES_H	0x00	RW	Bit[7:0]: BLC target value[15:8] For S channel in normal temperature
0x2D2	BLCBASES_L	0x88	RW	Bit[7:0]: BLC target value[7:0] For S channel in normal temperature
0x2D8	BLCBASEVS_H	0x00	RW	Bit[7:0]: BLC target value[15:8] For VS channel in normal temperature
0x2D9	BLCBASEVS_L	0x88	RW	Bit[7:0]: BLC target value[7:0] For VS channel in normal temperature
0x2E1	FIXEDRATIOENABLE	0x00	RW	Fixed Ratio Between L and S Enable 0: Disable 1: Enable
0x2E2	GPMODEEN	0x00	RW	Geometric Proportion Mode 0: Disable 1: Enable
0x2E3	NIGHTMODE	0x00	RW	Night Mode 0: Disable 1: Enable
0x2E4	ONLYINSERTFRAMEEN	0x00	RW	Only Insert Frame When in Night Mode 0: Disable 1: Enable
0x2E5	BANDINGFILTERENABLE	0x00	RW	Banding Filter 0: Disable 1: Enable
0x2E6	BANDINGFILTERSHORT ENABLE	0x00	RW	Short Banding Filter 0: Disable 1: Enable
0x2E7	BANDINGFILTERVSENABLE	0x00	RW	VS Banding Filter 0: Disable 1: Enable
0x2E8	LESSTHAN1BANDENABLE	0x01	RW	Less Than One Band Exposure Mode 0: Disable 1: Enable
0x2E9	LESSTHAN1BANDSHORT ENABLE	0x01	RW	Less Than One Band Exposure For Short 0: Disable 1: Enable

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table 4-54 AEC firmware registers (sheet 2 of 8)

address offset	register name	default value	R/W	description
0x2EA	LESSTHAN1BANDVS ENABLE	0x01	RW	Less Than One Band Exposure For VS 0: Disable 1: Enable
0x2EB	BANDINGFILTERFLAG	0x01	RW	Light Source Type 00: Frequency is zero or very high 01: 60Hz 10: 50Hz
0x2EC	TARGETY_L_A	0x40	RW	Target of Raw Data for Long Channel for Frame A in ABC Mode
0x2ED	TARGETY_L_B	0x40	RW	Target of Raw Data for Long Channel for Frame B in ABC Mode
0x2EE	TARGETY_L_C	0x40	RW	Target of Raw Data for Long Channel for Frame C in ABC mode
0x2EF	TARGETY_S_A	0x80	RW	Target of Raw Data for Short Channel for Frame A in ABC Mode
0x2F0	TARGETY_S_B	0x80	RW	Target of Raw Data for Short Channel for Frame B in ABC Mode
0x2F1	TARGETY_S_C	0x80	RW	Target of Raw Data for Short Channel for Frame C in ABC Mode
0x2F2	SLOWRANGE_0	0x20	RW	Slow Range for Long
0x2F3	SLOWRANGE_1	0x20	RW	Slow Range for Short
0x2F4	STABLERANGE_0	0x08	RW	Range Becomes Stable From Unstable
0x2F5	STABLERANGE_1	0x18	RW	Range Becomes Unstable From Stable
0x2F6	FASTSTEP_0	0x0C	RW	Fast AEC Adjustment Step for Long
0x2F7	FASTSTEP_1	0x0C	RW	Fast AEC Adjustment Step for Short
0x2F8	SLOWSTEP_0	0x02	RW	Slow AEC Adjustment Step for Long
0x2F9	SLOWSTEP_1	0x08	RW	Slow AEC Adjustment Step for Short
0x2FA	MAXFASTRATIO	0x40	RW	Max Fast Adjustment Ratio
0x2FB	MAXSLOWRATIO	0x04	RW	Max Slow Adjustment Ratio
0x2FC	LSFIXEDRATIO	0x20	RW	Fixed Ratio Between L and S
0x2FD	NIGHTMODESTEP	0x0C	RW	AEC Adjustment Step in Night Mode
0x304	MAXCAMERAGAIN_0_H	0x02	RW	Bit[1:0]: Max gain for long[9:8]
0x305	MAXCAMERAGAIN_0_L	0x00	RW	Bit[7:0]: Max gain for long[7:0]
0x306	MAXCAMERAGAIN_1_H	0x02	RW	Bit[1:0]: Max gain for short[9:8]

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table 4-54 AEC firmware registers (sheet 3 of 8)

address offset	register name	default value	R/W	description
0x307	MAXCAMERAGAIN_1_L	0x00	RW	Bit[7:0]: Max gain for short[7:0]
0x308	MAXCAMERAGAIN_2_H	0x02	RW	Bit[1:0]: Max gain for VS[9:8]
0x309	MAXCAMERAGAIN_2_L	0x00	RW	Bit[7:0]: Max gain for VS[7:0]
0x30A	MINCAMERAGAIN_0_H	0x00	RW	Bit[1:0]: Min gain for long[9:8]
0x30B	MINCAMERAGAIN_0_L	0x20	RW	Bit[7:0]: Min gain for long[7:0]
0x30C	MINCAMERAGAIN_1_H	0x00	RW	Bit[1:0]: Min gain for short[9:8]
0x30D	MINCAMERAGAIN_1_L	0x20	RW	Bit[7:0]: Min gain for short[7:0]
0x30E	MINCAMERAGAIN_2_H	0x00	RW	Bit[1:0]: Min gain for VS[9:8]
0x30F	MINCAMERAGAIN_2_L	0x20	RW	Bit[7:0]: Min gain for VS[7:0]
0x310	MAXEXPOSURE_0_H	0x02	RW	Bit[7:0]: Max exposure for long[15:8]
0x311	MAXEXPOSURE_0_L	0x08	RW	Bit[7:0]: Max exposure for long[7:0]
0x312	MAXEXPOSURE_1_H	0x02	RW	Bit[7:0]: Max exposure for short[15:8]
0x313	MAXEXPOSURE_1_L	0x08	RW	Bit[7:0]: Max exposure for short[7:0]
0x314	MAXEXPOSURE_2_H	0x00	RW	Bit[7:0]: Max exposure for VS[15:8]
0x315	MAXEXPOSURE_2_L	0x78	RW	Bit[7:0]: Max exposure for VS[7:0]
0x316	MINEXPOSURE_0_H	0x00	RW	Bit[7:0]: Min exposure for long[15:8]
0x317	MINEXPOSURE_0_L	0x01	RW	Bit[7:0]: Min exposure for long[7:0]
0x318	MINEXPOSURE_1_H	0x00	RW	Bit[7:0]: Min exposure for short[15:8]
0x319	MINEXPOSURE_1_L	0x01	RW	Bit[7:0]: Min exposure for short[7:0]
0x31A	MINEXPOSURE_2_H	0x00	RW	Bit[7:0]: Min exposure for VS[15:8]
0x31B	MINEXPOSURE_2_L	0x01	RW	Bit[7:0]: Min exposure for VS[7:0]
0x31C	LSSENSITIVITYRATIO_H	0x08	RW	Bit[7:0]: L/S sensitivity ratio[15:8]
0x31D	LSSENSITIVITYRATIO_L	0x00	RW	Bit[7:0]: L/S sensitivity ratio[7:0]
0x31E	SVSFIXEDRATIO_H	0x00	RW	Bit[7:0]: S/VS exposure ratio[15:8]
0x31F	SVSFIXEDRATIO_L	0x80	RW	Bit[7:0]: S/VS exposure ratio[7:0]
0x320	BANDVALUE60HZ_H	0x20	RW	Bit[7:0]: Band filter value for 60Hz[15:8]
0x321	BANDVALUE60HZ_L	0xD0	RW	Bit[7:0]: Band filter value for 60Hz[7:0]
0x322	BANDVALUE50HZ_H	0x27	RW	Bit[7:0]: Band filter value for 50Hz[15:8]
0x323	BANDVALUE50HZ_L	0x60	RW	Bit[7:0]: Band filter value for 50Hz[7:0]
0x324	MAXRATIO_H	0x00	RW	Bit[7:0]: Max L/S ratio[15:8]

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table 4-54 AEC firmware registers (sheet 4 of 8)

address offset	register name	default value	R/W	description
0x325	MAXRATIO_L	0x20	RW	Bit[7:0]: Max L/S ratio[7:0]
0x326	MINRATIO	0x02	RW	Min L/S Ratio
0x327	MAXINSERTFRAME	0x03	RW	Maximum Insert Frames At Night Mode
0x328	NVTSWRITEMODE	0x01	RW	VTS Write Mode 0: Write with exposure 1: Write with gain
0x329	AECMANUALMODE	0x07	RW	Bit[2]: Frame C manual exposure/gain enable 0: Disable 1: Enable Bit[1]: Frame B manual exposure/gain enable 0: Disable 1: Enable Bit[0]: Frame A manual exposure/gain enable 0: Disable 1: Enable
0x32A	AECMANUALDONE	0x02	RW	Bit[1:0]: A, B and C frame manual exposure/gain validate 00: OV490 does not take new manual exposure/gain 01: OV490 takes manual exposure/gain only once 10: OV490 always takes manual exposure/gain
0x32B	ALLOWFRACTALEXP	0x01	RW	Allow Fractal Resolution For VS Exposure
0x32C	AECMANUALEXP_L_A_H	0x00	RW	Bit[7:0]: Manual exposure for long[15:8] for frame A in ABC mode
0x32D	AECMANUALEXP_L_A_L	0x40	RW	Bit[7:0]: Manual exposure for long[7:0] for frame A in ABC mode
0x32E	AECMANUALEXP_L_B_H	0x00	RW	Bit[7:0]: Manual exposure for long[15:8] for frame B in ABC mode
0x32F	AECMANUALEXP_L_B_L	0x40	RW	Bit[7:0]: Manual exposure for long[7:0] for frame B in ABC mode
0x330	AECMANUALEXP_L_C_H	0x00	RW	Bit[7:0]: Manual exposure for long[15:8] for frame C in ABC mode
0x331	AECMANUALEXP_L_C_L	0x40	RW	Bit[7:0]: Manual exposure for long[7:0] for frame C in ABC mode
0x332	AECMANUALEXP_S_A_H	0x00	RW	Bit[7:0]: Manual exposure for short[15:8] for frame A in ABC mode

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table 4-54 AEC firmware registers (sheet 5 of 8)

address offset	register name	default value	R/W	description
0x333	AECMANUALEXP_S_A_L	0x10	RW	Bit[7:0]: Manual exposure for short[7:0] for frame A in ABC mode
0x334	AECMANUALEXP_S_B_H	0x00	RW	Bit[7:0]: Manual exposure for Short[15:8] for frame B in ABC mode
0x335	AECMANUALEXP_S_B_L	0x10	RW	Bit[7:0]: Manual exposure for short[7:0] for frame B in ABC mode
0x336	AECMANUALEXP_S_C_H	0x00	RW	Bit[7:0]: Manual exposure for short[15:8] for frame C in ABC mode
0x337	AECMANUALEXP_S_C_L	0x10	RW	Bit[7:0]: Manual exposure for short[7:0] for frame C in ABC mode
0x338	AECMANUALEXP_VS_A_H	0x00	RW	Bit[7:0]: Manual exposure for VS[15:8] for frame A in ABC mode
0x339	AECMANUALEXP_VS_A_L	0x20	RW	Bit[7:0]: Manual exposure for VS[7:0] for frame A in ABC mode
0x33A	AECMANUALEXP_VS_B_H	0x00	RW	Bit[7:0]: Manual exposure for VS[15:8] for frame B in ABC mode
0x33B	AECMANUALEXP_VS_B_L	0x20	RW	Bit[7:0]: Manual exposure for VS[7:0] for frame B in ABC mode
0x33C	AECMANUALEXP_VS_C_H	0x00	RW	Bit[7:0]: Manual exposure for VS[15:8] for frame C in ABC mode
0x33D	AECMANUALEXP_VS_C_L	0x20	RW	Bit[7:0]: Manual exposure for VS[7:0] for frame C in ABC mode
0x33E	AECMANUALGAIN_L_A_H	0x00	RW	Bit[7:0]: Manual gain for long[15:8] for frame A in ABC mode
0x33F	AECMANUALGAIN_L_A_L	0x20	RW	Bit[7:0]: Manual gain for long[7:0] for frame A in ABC mode
0x340	AECMANUALGAIN_L_B_H	0x00	RW	Bit[7:0]: Manual gain for long[15:8] for frame B in ABC mode
0x341	AECMANUALGAIN_L_B_L	0x20	RW	Bit[7:0]: Manual gain for long[7:0] for frame B in ABC mode
0x342	AECMANUALGAIN_L_C_H	0x00	RW	Bit[7:0]: Manual gain for long[15:8] for frame C in ABC mode
0x343	AECMANUALGAIN_L_C_L	0x20	RW	Bit[7:0]: Manual gain for long[7:0] for frame C in ABC mode
0x344	AECMANUALGAIN_S_A_H	0x00	RW	Bit[7:0]: Manual gain for short[15:8] for frame A in ABC mode

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table 4-54 AEC firmware registers (sheet 6 of 8)

address offset	register name	default value	R/W	description
0x345	AECMANUALGAIN_S_A_L	0x20	RW	Bit[7:0]: Manual gain for short[7:0] for frame A in ABC mode
0x346	AECMANUALGAIN_S_B_H	0x00	RW	Bit[7:0]: Manual gain for short[15:8] for frame B in ABC mode
0x347	AECMANUALGAIN_S_B_L	0x20	RW	Bit[7:0]: Manual gain for short[7:0] for frame B in ABC mode
0x348	AECMANUALGAIN_S_C_H	0x00	RW	Bit[7:0]: Manual gain for short[15:8] for frame C in ABC mode
0x349	AECMANUALGAIN_S_C_L	0x20	RW	Bit[7:0]: Manual gain for short[7:0] for frame C in ABC mode
0x34A	AECMANUALGAIN_VS_A_H	0x00	RW	Bit[7:0]: Manual gain for VS[15:8] for frame A in ABC mode
0x34B	AECMANUALGAIN_VS_A_L	0x20	RW	Bit[7:0]: Manual gain for VS[7:0] for frame A in ABC mode
0x34C	AECMANUALGAIN_VS_B_H	0x00	RW	Bit[7:0]: Manual gain for VS[15:8] for frame B in ABC mode
0x34D	AECMANUALGAIN_VS_B_L	0x20	RW	Bit[7:0]: Manual gain for VS[7:0] for frame B in ABC mode
0x34E	AECMANUALGAIN_VS_C_H	0x00	RW	Bit[7:0]: Manual gain for VS[15:8] for frame C in ABC mode
0x34F	AECMANUALGAIN_VS_C_L	0x20	RW	Bit[7:0]: Manual gain for VS[7:0] for frame C in ABC mode
0x350	MAXTOTALEXP_L_BYTE0	0x00	RW	Bit[7:0]: Max total exposure for long[31:24]
0x351	MAXTOTALEXP_L_BYTE1	0x0A	RW	Bit[7:0]: Max total exposure for long[23:16]
0x352	MAXTOTALEXP_L_BYTE2	0x28	RW	Bit[7:0]: Max total exposure for long[15:8]
0x353	MAXTOTALEXP_L_BYTE3	0x00	RW	Bit[7:0]: Max total exposure for long[7:0]
0x354	MAXTOTALEXP_S_BYTE0	0x00	RW	Bit[7:0]: Max total exposure for short[31:24]
0x355	MAXTOTALEXP_S_BYTE1	0x04	RW	Bit[7:0]: Max total exposure for short[23:16]
0x356	MAXTOTALEXP_S_BYTE2	0x10	RW	Bit[7:0]: Max total exposure for short[15:8]
0x357	MAXTOTALEXP_S_BYTE3	0x00	RW	Bit[7:0]: Max total exposure for short[7:0]

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table 4-54 AEC firmware registers (sheet 7 of 8)

address offset	register name	default value	R/W	description
0x358	MAXTOTALEXP_VS_BYTE0	0x00	RW	Bit[7:0]: Max total exposure for VS[31:24]
0x359	MAXTOTALEXP_VS_BYTE1	0x02	RW	Bit[7:0]: Max total exposure for VS[23:16]
0x35A	MAXTOTALEXP_VS_BYTE2	0x60	RW	Bit[7:0]: Max total exposure for VS[15:8]
0x35B	MAXTOTALEXP_VS_BYTE3	0x00	RW	Bit[7:0]: Max total exposure for VS[7:0]
0x35C	MINTOTALEXP_L_H	0x00	RW	Bit[7:0]: Min total exposure for long[15:8]
0x35D	MINTOTALEXP_L_L	0x20	RW	Bit[7:0]: Min total exposure for long[7:0]
0x35E	MINTOTALEXP_S_H	0x00	RW	Bit[7:0]: Min total exposure for short[15:8]
0x35F	MINTOTALEXP_S_L	0x20	RW	Bit[7:0]: Min total exposure for short[7:0]
0x360	MINTOTALEXP_VS_H	0x00	RW	Bit[7:0]: Min total exposure for VS[15:8]
0x361	MINTOTALEXP_VS_L	0x20	RW	Bit[7:0]: Min total exposure for VS[7:0]
0x366	TRAFFICMODEMINEXPOSURELINES_H	0x00	RW	Traffic Mode Minimum Exposure for Short Exposure High Byte
0x367	TRAFFICMODEMIN EXPOSURELINES_L	0x20	RW	Traffic Mode Minimum Exposure for Short Exposure Low Byte
0x369	BLCTRIGTEMPTHRE	0x02	RW	BLC Temperature Difference Trigger Threshold
0x36D	HTLIMITSTARTT	0x46	RW	Temperature Start Threshold in High Temperature BLC Function
0x36E	HTLIMITENDT	0x64	RW	Temperature End Threshold in High Temperature BLC Function
0x370	HTLIMITSTARTG_H	0x00	RW	Bit[7:0]: Analog gain start threshold[15:8] in high temperature BLC function
0x371	HTLIMITSTARTG_L	0xC0	RW	Bit[7:0]: Analog gain start threshold[7:0] in high temperature BLC function
0x372	HTLIMITENDG_H	0x01	RW	Bit[7:0]: Analog gain end threshold[15:8] in high temperature BLC function
0x373	HTLIMITENDG_L	0x80	RW	Bit[7:0]: Analog gain end threshold[7:0] in high temperature BLC function
0x374	ADDBLCOFFSETENABLE	0x02	RW	High Temperature BLC Target Offset Enable

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table 4-54 AEC firmware registers (sheet 8 of 8)

address offset	register name	default value	R/W	description
0x375	HTLIMITBLCTHREL	0x30	RW	BLC Offset for L Exposure in High Temperature BLC Function
0x376	HTLIMITBLCTHRES	0x30	RW	BLC Offset for S Exposure in High Temperature BLC Function
0x377	HTLIMITBLCTHREVS	0x30	RW	BLC Offset for VS Exposure in High Temperature BLC Function
0x378	HTLIMITGAMMAENABLE	0x01	RW	High Temperature BLC Limit Gamma Function Enable
0x379	HTLIMITMINGAMMATHRE	0x04	RW	High Temperature BLC Limit Minimum Gamma Threshold
0x37A	HTLIMITMAXGAMMATHRE	0x08	RW	High Temperature BLC Limit Maximum Gamma Threshold
0x38C	BLCBASEL_H	0x00	RW	Bit[7:0]: BLC target value[15:8] For L channel in normal temperature
0x38D	BLCBASEL_L	0x80	RW	Bit[7:0]: BLC target value[7:0] For L channel in normal temperature
0xAD8	MANUALAECENABLE	0x00	RW	Manual AEC Enable 0: Disable 1: Enable

table 4-55 LSC firmware registers (sheet 1 of 4)

address offset	register name	default value	R/W	description
0x3A4	LENSAUTOGAINENABLE	0x01	RW	Auto Gain Enable 0: Disable 1: Enable
0x3A5	LENSAUTOCTENABLE	0x01	RW	Auto CT Enable 0: Disable 1: Enable
0x3A6	LENSGAIN[0][0]_H	0x00	RW	Bit[7:0]: Lens gain 0[15:8] for long
0x3A7	LENSGAIN[0][0]_L	0x60	RW	Bit[7:0]: Lens gain 0[7:0] for long
0x3A8	LENSGAIN[0][1]_H	0x00	RW	Bit[7:0]: Lens gain 1[15:8] for long
0x3A9	LENSGAIN[0][1]_L	0xC0	RW	Bit[7:0]: Lens gain 1[7:0] for long

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table 4-55 LSC firmware registers (sheet 2 of 4)

address offset	register name	default value	R/W	description
0x3AA	LENSGAIN[1][0]_H	0x00	RW	Bit[7:0]: Lens gain 0[15:8] for short
0x3AB	LENSGAIN[1][0]_L	0x60	RW	Bit[7:0]: Lens gain 0[7:0] for short
0x3AC	LENSGAIN[1][1]_H	0x00	RW	Bit[7:0]: Lens gain 1[15:8] for short
0x3AD	LENSGAIN[1][1]_L	0xC0	RW	Bit[7:0]: Lens gain 1[7:0] for short
0x3AE	LENSGAIN[2][0]_H	0x00	RW	Bit[7:0]: Lens gain 0[15:8] for VS
0x3AF	LENSGAIN[2][0]_L	0x60	RW	Bit[7:0]: Lens gain 0[7:0] for VS
0x3B0	LENSGAIN[2][1]_H	0x00	RW	Bit[7:0]: Lens gain 1[15:8] for VS
0x3B1	LENSGAIN[2][1]_L	0xC0	RW	Bit[7:0]: Lens gain 1[7:0] for VS
0x3B2	LENSCTTHRE [0][0]_H	0x00	RW	Bit[7:0]: Lens CT threshold 0[15:8] for long
0x3B3	LENSCTTHRE [0][0]_L	0xE0	RW	Bit[7:0]: Lens CT threshold 0[7:0] for long
0x3B4	LENSCTTHRE [0][1]_H	0x00	RW	Bit[7:0]: Lens CT threshold 1[15:8] for long
0x3B5	LENSCTTHRE [0][1]_L	0xF0	RW	Bit[7:0]: Lens CT threshold 1[7:0] for long
0x3B6	LENSCTTHRE [0][2]_H	0x01	RW	Bit[7:0]: Lens CT threshold 2[15:8] for long
0x3B7	LENSCTTHRE [0][2]_L	0xB0	RW	Bit[7:0]: Lens CT threshold 2[7:0] for long
0x3B8	LENSCTTHRE [0][3]_H	0x01	RW	Bit[7:0]: Lens CT threshold 3[15:8] for long
0x3B9	LENSCTTHRE [0][3]_L	0xC0	RW	Bit[7:0]: Lens CT threshold 3[7:0] for long
0x3BA	LENSCTTHRE [1][0]_H	0x00	RW	Bit[7:0]: Lens CT threshold 0[15:8] for short
0x3BB	LENSCTTHRE [1][0]_L	0xE0	RW	Bit[7:0]: Lens CT threshold 0[7:0] for short
0x3BC	LENSCTTHRE [1][1]_H	0x00	RW	Bit[7:0]: Lens CT threshold 1[15:8] for short
0x3BD	LENSCTTHRE [1][1]_L	0xF0	RW	Bit[7:0]: Lens CT threshold 1[7:0] for short
0x3BE	LENSCTTHRE [1][2]_H	0x01	RW	Bit[7:0]: Lens CT threshold 2[15:8] for short
0x3BF	LENSCTTHRE [1][2]_L	0xB0	RW	Bit[7:0]: Lens CT threshold 2[7:0] for short
0x3C0	LENSCTTHRE [1][3]_H	0x01	RW	Bit[7:0]: Lens CT threshold 3[15:8] for short
0x3C1	LENSCTTHRE [1][3]_L	0xC0	RW	Bit[7:0]: Lens CT threshold 3[7:0] for short
0x3C2	LENSCTTHRE [2][0]_H	0x00	RW	Bit[7:0]: Lens CT threshold 0[15:8] for VS
0x3C3	LENSCTTHRE [2][0]_L	0xE0	RW	Bit[7:0]: Lens CT threshold 0[7:0] for VS
0x3C4	LENSCTTHRE [2][1]_H	0x00	RW	Bit[7:0]: Lens CT threshold 1[15:8] for VS
0x3C5	LENSCTTHRE [2][1]_L	0xF0	RW	Bit[7:0]: Lens CT threshold 1[7:0] for VS
0x3C6	LENSCTTHRE [2][2]_H	0x01	RW	Bit[7:0]: Lens CT threshold 2[15:8] for VS
0x3C7	LENSCTTHRE [2][2]_L	0xB0	RW	Bit[7:0]: Lens CT threshold 2[7:0] for VS

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table 4-55 LSC firmware registers (sheet 3 of 4)

address offset	register name	default value	R/W	description
0x3C8	LENSCTTHRE [2][3]_H	0x01	RW	Bit[7:0]: Lens CT threshold 3[15:8] for VS
0x3C9	LENSCTTHRE [2][3]_L	0xC0	RW	Bit[7:0]: Lens CT threshold 3[7:0] for VS
0x3CA	LENSMAXQ_0_H	0x00	RW	Bit[7:0]: Lens maxq[15:8] for long
0x3CB	LENSMAXQ_0_L	0x38	RW	Bit[7:0]: Lens maxq[7:0] for long
0x3CC	LENSMAXQ_1_H	0x00	RW	Bit[7:0]: Lens maxq[15:8] for short
0x3CD	LENSMAXQ_1_L	0x38	RW	Bit[7:0]: Lens maxq[7:0] for short
0x3CE	LENSMAXQ_2_H	0x00	RW	Bit[7:0]: Lens maxq[15:8] for VS
0x3CF	LENSMAXQ_2_L	0x38	RW	Bit[7:0]: Lens maxq[7:0] for VS
0x3D0	LENSMINQ_0_H	0x00	RW	Bit[7:0]: Lens minq[15:8] for long
0x3D1	LENSMINQ_0_L	0x28	RW	Bit[7:0]: Lens minq[7:0] for long
0x3D2	LENSMINQ_1_H	0x00	RW	Bit[7:0]: Lens minq[15:8] for short
0x3D3	LENSMINQ_1_L	0x28	RW	Bit[7:0]: Lens minq[7:0] for short
0x3D4	LENSMINQ_2_H	0x00	RW	Bit[7:0]: Lens minq[15:8] for VS
0x3D5	LENSMINQ_2_L	0x28	RW	Bit[7:0]: Lens minq[7:0] for VS
0x3D6	LENSMANUALCT_0_H	0x00	RW	Bit[7:0]: Lens manual CT[15:8] for long
0x3D7	LENSMANUALCT_0_L	0xA0	RW	Bit[7:0]: Lens manual CT[7:0] for long
0x3D8	LENSMANUALCT_1_H	0x00	RW	Bit[7:0]: Lens manual CT[15:8] for short
0x3D9	LENSMANUALCT_1_L	0xA0	RW	Bit[7:0]: Lens manual CT[7:0] for short
0x3DA	LENSMANUALCT_2_H	0x00	RW	Bit[7:0]: Lens manual CT[15:8] for VS
0x3DB	LENSMANUALCT_2_L	0xA0	RW	Bit[7:0]: Lens manual CT[7:0] for VS
0x3DC	LENSCPARRAY[0][0][]	0x0D	RW	Bit[7:0]: Lens control point array under Day light condition for long
0x49C	LENSCPARRAY[0][1][]	0x0E	RW	Bit[7:0]: Lens control point array under C light condition for long
0x55C	LENSCPARRAY[0][2][]	0x0E	RW	Bit[7:0]: Lens control point array under A light condition for long
0x61C	LENSCPARRAY[1][0][]	0x0D	RW	Bit[7:0]: Lens control point array under Day light condition for short
0x6DC	LENSCPARRAY[1][1][]	0x0D	RW	Bit[7:0]: Lens control point array under C light condition for short
0x79C	LENSCPARRAY[1][2][]	0x0C	RW	Bit[7:0]: Lens control point array under A light condition for short

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table 4-55 LSC firmware registers (sheet 4 of 4)

address offset	register name	default value	R/W	description
0x85C	MANUALLENCEN	0x00	RW	Lens Manual Control Enable 0: Disable 1: Enable

table 4-56 high temperature function firmware registers (sheet 1 of 2)

address offset	register name	default value	R/W	description
0x2D1	BLCBASES_H	0x00	RW	Bit[7:0]: BLC target value[15:8] for S channel in normal temperature
0x2D2	BLCBASES_L	0x88	RW	Bit[7:0]: BLC target value[7:0] for S channel in normal temperature
0x2D8	BLCBASEVS_H	0x00	RW	Bit[7:0]: BLC target value[15:8] for VS channel in normal temperature
0x2D9	BLCBASEVS_L	0x88	RW	Bit[7:0]: BLC target value[7:0] for VS channel in normal temperature
0x38C	BLCBASEL_H	0x00	RW	Bit[7:0]: BLC target value[15:8] for L channel in normal temperature
0x38D	BLCBASEL_L	0x80	RW	Bit[7:0]: BLC target value[7:0] for L channel in normal temperature
0x86C	BHTLIMITHDRGAINEN	0x01	RW	Bit[7:1]: Reserved Bit[0]: HTLimitHDRGainEn
0x86D	WEIGHTT	0x0C	RW	Bit[3:0]: Weight temp[3:0]
0x86E	NHTLIMITHDR_STARTTEMP	0x46	RW	Bit[7:0]: High temperature start
0x86F	HTLIMITHDR_ENDTEMP	0x64	RW	Bit[7:0]: High temperature end
0x870	HTLIMITHDR_STARTG HIGH	0x00	RW	Bit[7:0]: High temp HDR gain start value[15:8]
0x871	HTLIMITHDR_STARTG LOW	0x20	RW	Bit[7:0]: High temp HDR gain start value[7:0]
0x872	HTLIMITHDR_ENDG HIGH	0x01	RW	Bit[7:0]: High temp HDR gain end value[15:8]
0x873	HTLIMITHDR_ENDG LOW	0x00	RW	Bit[7:0]: High temp HDR gain end value[7:0]
0x876	HTHDRGAINTARGET	0x03	RW	Bit[7:0]: High temp HDR gain target value[15:8]

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table 4-56 high temperature function firmware registers (sheet 2 of 2)

address offset	register name	default value	R/W	description
0x877	HTHDRGAINTARGET	0x00	RW	Bit[7:0]: High temp HDR gain target value[7:0]
0x89C	HTLIMITSATURATIONEN	0x01	RW	Bit[7:1]: Reserved Bit[0]: HTLimitSaturationEn
0x89D	SATURATION_ORIGHIGH	0x38	RW	Bit[7:0]: Normal CMX maximum factor
0x89E	SATURATION_ORIGLOW	0x18	RW	Bit[7:0]: Normal CMX minimum factor
0x89F	SATURATION_TARGET HIGH	0x18	RW	Bit[7:0]: High temp CMX maximum factor
0x8A0	SATURATION_TARGETLOW	0x10	RW	Bit[7:0]: High temp CMX minimum factor
0x8A2	HTLIMITLENCEN	0x01	RW	Bit[7:1]: Reserved Bit[0]: HTLimitLenc enable
0x8A3	LENC_ORIGHIGH	0x38	RW	Bit[7:0]: Normal lens maximum factor
0x8A4	LENC_ORIGLOW	0x28	RW	Bit[7:0]: Normal lens minimum factor
0x8A5	LENC_TARGETHIGH	0x00	RW	Bit[7:0]: High temp maximum factor
0x8A6	LENC_TARGETLOW	0x00	RW	Bit[7:0]: High temp minimum factor

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5 operating specifications

5.1 absolute maximum ratings

table 5-1 absolute maximum ratings

parameter		absolute maximum rating[a]
supply voltage (with respect to ground)	MTXAVDD	3.6
	MRXAVDD	1.98V
	PLLAVDD	1.98V
	TSAVDD	3.6V
	CVDD	1.32V
	PADVDD	3.6V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to 3.6V
I/O current on any input or output pin		±200 mA
peak solder temperature (10 second dwell time)		260°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

5.2 functional temperature

table 5-2 functional temperature

parameter	range
operating temperature range	-40°C to +105°C ambient temperature

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5.3 DC characteristics

table 5-3 DC characteristics

symbol	parameter	condition	min	typ	max	unit
supply						
MTXAVDD	supply voltage (MIPI TX/DVP)		3	3.3	3.6	V
VRIA	regulator power input		1.62	1.8	3.6	V
VRIB	regulator power input		1.62	1.8	3.6	V
MRXAVDD	supply voltage (MIPI RX)		1.62	1.8	1.98	V
PLLAVDD	supply voltage (PLL)		1.62	1.8	1.98	V
TSAVDD	supply voltage (temperature sensor)		2.5	2.8	3.6	V
CVDD	supply voltage (digital core power)		1.08	1.2	1.32	V
PADVDD	supply voltage (digital I/O)		1.62	3.3	3.6	V
IDD-MTXAVDD[a]	active current			35		mA
IDD-MRXAVDD[b]	active current			8		mA
IDD-PLLAVDD	active current			0.5		mA
IDD-TSAVDD	active current			0.8		mA
IDD-CVDD[c]	active current			100		mA
IDD-PADVDD	active current			8		mA
IDDS-MTXAVDD	power down current			3		µA
IDDS-MRXAVDD	power down current			0.3		µA
IDDS-PLLAVDD	power down current			0.3		µA
IDDS-TSAVDD	power down current			0.6		µA
IDDS-CVDD	power down current			100		µA
IDDS-PADVDD	power down current			3		µA
digital inputs (typical conditions: PVDD =3.3V)						
V_{IH}	input voltage HIGH	CMOS	0.7×PVDD			V
V_{IL}	input voltage IOW	CMOS			0.3×PVDD	V
digital outputs (standard loading 25 pF, PVDD = 3.3V)						
V_{OH}	output voltage HIGH	CMOS	0.9×PVDD			V
V_{OL}	output voltage LOW	CMOS			0.1×PVDD	V

a. DVP output mode
b. MIPI input mode
c. DVP input and single channel

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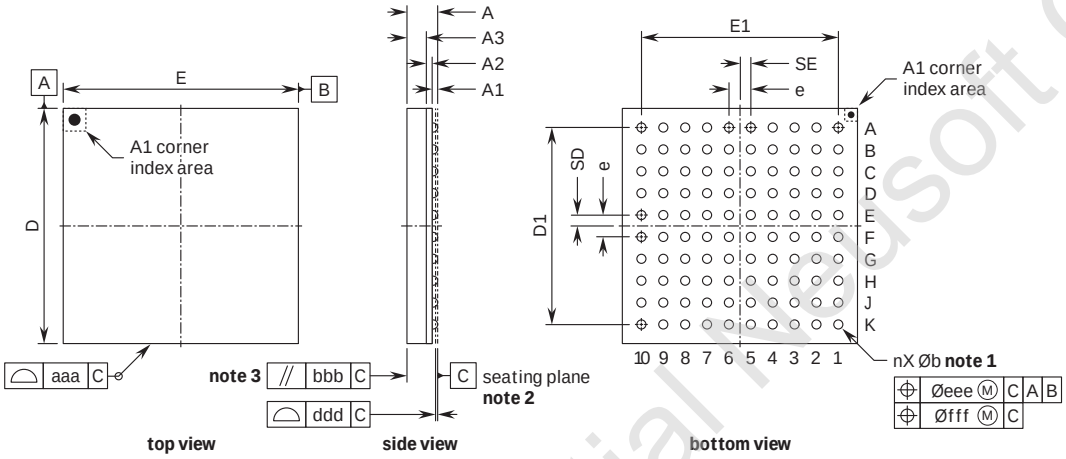
6 mechanical specifications

6.1 physical specifications

figure 6-1 package specifications



note 1 dimension b is measured at the maximum solder ball diameter, parallel to datum plane c

note 2 datum c (seating plane) is defined by the spherical crowns of the solder ball

note 3 parallelism measurement shall exclude any effect of mark on top surface of package

490_BDS_6_1

table 6-1 package dimensions (sheet 1 of 2)

parameter	symbol	min	typ	max	unit
total thickness	A			1.1	mm
stand off	A1	0.16		0.26	mm
substrate thickness	A2		0.26		mm
mold thickness	A3		0.54		mm
body size y-axis	D		7		mm
body size x-axis	E		7		mm
ball diameter			0.3		mm
ball opening			0.275		mm
ball width	b	0.27		0.37	mm
ball pitch	e		0.65		mm
ball count	n		100		

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table 6-1 package dimensions (sheet 2 of 2)

parameter	symbol	min	typ	max	unit
edge ball center to center (y-axis)	D1		5.85		mm
edge ball center to center (x-axis)	E1		5.85		mm
body center to contact ball	SD		0.325		mm
	SE		0.325		mm
package edge tolerance	aaa		0.1		mm
mold flatness	bbb		0.2		mm
coplanarity	ddd		0.08		mm
ball offset (package)	eee		0.15		mm
ball offset (ball)	fff		0.08		mm

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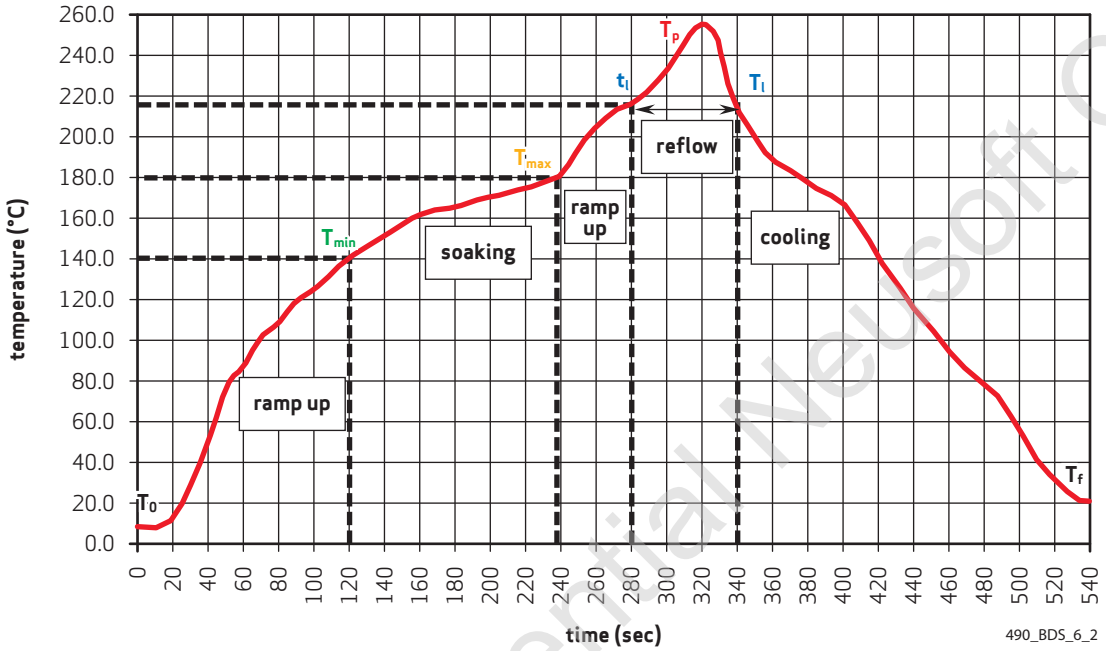
6.2 IR reflow specifications

figure 6-2 IR reflow ramp rate requirements



note
The OV490 uses a lead free package.

table 6-2 reflow conditions[ab]

zone	description	exposure
ramp up A (T_0 to T_{min})	heating from room temperature to 140°C	temperature slope ≤ 3°C per second
soaking	heating from 140°C to 180°C	90 ~ 150 seconds
ramp up B (t_l to T_P)	heating from 217°C to 260°C	temperature slope ≤ 3°C per second
peak temperature	maximum temperature in SMT	260°C +0/-5°C (duration max 30 sec)
reflow (t_l to T_l)	temperature higher than 217°C	30 ~ 120 seconds
ramp down A (T_P to T_l)	cooling from 260°C to 217°C	temperature slope ≤ 3°C per second
ramp down B (T_l to T_f)	cooling from 217°C to room temperature	temperature slope ≤ 6°C per second
T_0 to T_P	room temperature to peak temperature	≤ 8 minutes

a. maximum number of reflow cycles = 3

b. N2 gas reflow or control O2 gas PPM<500 as recommendation

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revision history

version 1.0 09.19.2013

- initial release

version 1.1 11.12.2013

- in table 1-1 and table 1-2, changed description of C3 pin from "3.3V MIPI TX analog power supply" to "3.3V analog power supply for MIPI TX in MIPI output mode and DVP supply in DVP output mode"
- in table 1-1 and table 1-2, changed description of D4 pin from "MIPI TX analog ground" to "MIPI TX analog ground in MIPI output mode and DVP analog ground in DVP output mode"
- in chapter 1, added table 1-3, power domain description
- in table 4-8, changed default value of register DVP CTRL0 (offset 0x00) from "0x00" to "0x04"
- in table 4-19, changed default value of register R_TMP_SLOPE_H (offset 0x00) from "0x04" to "0x4D"

version 2.0 04.10.2015

- changed datasheet from Preliminary specification to Product Specification
- major updates were completed throughout entire document
- in table 1-3, changed "I/O bank powered by M0RXAVDD18" to "I/O bank powered by PADVDD18"
- in table 2-2, added format "12 bits YUV422+12 bits RAW"
- in chapter 2, updated section 2-13 and section 2.22
- in chapter 2, updated figure 2-16
- in chapter 3, updated figure 3-7, figure 3-9, figure 3-20
- in chapter 3, removed section 3.16, UV DNS and updated entire section 3.12
- in chapter 3, updated all of section 3.19 and section 3.22
- in chapter 3, updated section 3.25
- in chapter 4, updated entire chapter

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OmniVision Technologies, Inc.

UNITED STATES

4275 Burton Drive
Santa Clara, CA 95054

tel: +1 408 567 3000

fax: +1 408 567 3001

email: sales@ovt.com

UNITED KINGDOM

Hook, Hampshire +44 1256 744 610

GERMANY

Munich +49 89 63 81 99 88

INDIA

Bangalore +91 80 4112 8966

CHINA

Beijing + 86 10 6580 1690

Shanghai + 86 21 6175 9888

+86 21 5774 9288

Shenzhen + 86 755 8384 9733

JAPAN

Yokohama +81 45 478 7977

Osaka +81 6 4964 2606

KOREA

Seoul + 82 2 3478 2812

SINGAPORE +65 6933 1933

TAIWAN

Taipei +886 2 2657 9800

Hsin-chu +886 3 5656688

website: www.ovt.com