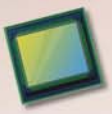
OmniVision



datasheet

PRELIMINARY SPECIFICATION

1/2.56" color CMOS 1.3 megapixel (1280 x 1080) high dynamic range (HDR) high definition (HD) image sensor

OV10640 (rev 1E)

color CMOS 1.3 megapixel (1280x1080) high dynamic range (HDR) high definition image sensor

datasheet (aCSP)
PRELIMINARY SPECIFICATION

version 1.1
may 2015

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- automotive
  - 360° surround view system
  - rear view camera
  - lane departure warning/ lane keep assist
  - blind spot detection
  - night vision
  - pedestrian detection
  - traffic sign recognition
  - occupant sensor
  - camera monitoring system
  - autonomous driving

ordering information

- **OV10640-N79Y-PE-Z** (color, lead-free) 78-pin aCSP™, rev 1E, with protective film, packed in tray
- **OV10640-N79Y-RE-Z** (color, lead-free) 78-pin aCSP™, rev 1E, with protective film, packed in tape & reel

note Since it is impossible to check compatibility with all displays, check the interoperability before committing to mass production.

features

- support for image size: 1280x1080, VGA, QVGA and any cropped size
- OmniHDR-S™ technology
- high sensitivity
- safety features
- low power consumption
- image sensor processor functions: automatic exposure/gain control, lens correction, defective pixel cancelation, HDR combination and tone mapping, automatic black level correction
- supported output formats: RAW
- horizontal and vertical sub-sampling
- serial camera control bus (SCCB) for register programming
- high speed serial data transfer with MIPI CSI-2
- external frame synchronization capability
- parallel 12-bit DVP output
- embedded temperature sensor
- one time programmable (OTP) memory

note To reduce image artifacts from Infrared light, and provide the best image quality, OmniVision recommends an IR cut filter

key specifications (typical)

- **active array size:** 1280 x 1080
- **power supply:**
  analog: 3.14 ~ 3.47V
  digital: 1.425 ~ 1.575V
  DOVDD: 1.7 ~ 1.9V
  AVDD: 1.7 ~ 1.9V
- **power requirements:**
  active: TBD
  standby: TBD
- **temperature range:**
  operating: -40°C to 105°C sensor ambient temperature and -40°C to 125°C junction temperature (see **table 9-2**)
- **output interfaces:** 12-bit DVP, MIPI/LVDS CSI-2
- **input clock frequency:** 6 ~ 27 MHz
- **lens size:** 1/2.56"
- **lens chief ray angle:** 9° (see **figure 11-2**)
- **output formats:** 20-bit combined RAW, 12-bit compressed combined RAW, separated 12-bit RAW, 2x12 bit compressed RAW, 16-bit log domain combined RAW, 3x12 bit uncompressed RAW
- **scan mode:** progressive
- **shutter:** rolling shutter
- **maximum image transfer rate:** 60 fps full resolution
- **sensitivity:** TBD
- **max S/N ratio:** TBD
- **dynamic range:** TBD
- **pixel size:** 4.2 µm x 4.2 µm
- **dark current:** TBD
- **image area:** 5410 µm x 4570 µm
- **package dimensions:** 7430 µm x 7190 µm

note OmniVision recommends aCSP packages use underfill as part of camera assembly process.

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1 application system

1.1 overview

The OV10640 color image sensor is a 1/2.56" optical format, 1280x1080 single-chip, low power CMOS, active-pixel digital high dynamic range sensor for both human vision and machine vision automotive applications.

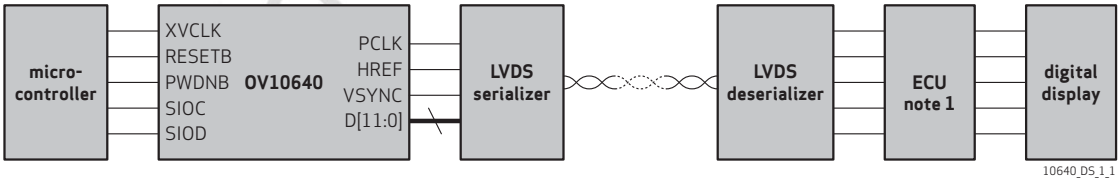
The OV10640 features OmniBSI™ technology to extend the dynamic range. The on-chip AEC/AGC automatically adjusts the ratio of the exposure and gain of the sub-pixels based on the dynamic range of the scene. The combined HDR RAW format is best suited for machine vision applications, while the tone mapped RAW output provides the HDR rendering for human vision applications.

The OV10640 performs sophisticated camera functions on-chip controlled via the Serial Camera Control Bus (SCCB) interface. These functions include lens shading correction, HDR combination, defect pixel correction, de-noise, and tone mapping. The OV10640 enables advanced HDR imaging in a simple, cost effective system.

1.1.1 typical OV10640 standalone camera

figure 1-1 is the block diagram of a standalone OV10640 camera for automotive applications. The micro-controller programs the register settings and controls the OV10640 based on the application requirements. The LVDS serializer and deserializer (SerDes) pair is for transferring video from the camera to the display unit over a long distance.

figure 1-1 standalone camera block diagram for automotive applications

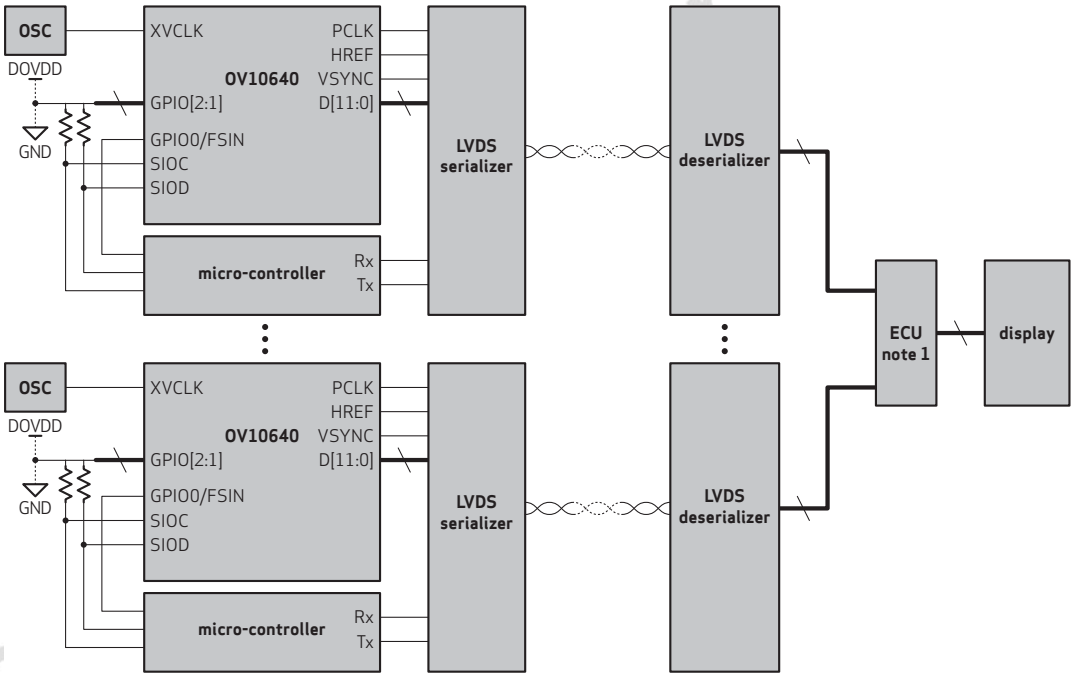


note 1 OV490 or similar ISP processor is required to generate YUV or RGB for digital display

1.1.2 typical OV10640 multi-camera system

The OV10640 features frame sync input to synchronize the video streaming timing between multiple sensors in a multi-camera system. Up to four SCCB IDs can be selected by GPIO2/1/0 in case a unique SCCB ID is required to access each sensor. **figure 1-2** shows the block diagram of a typical multi-camera system using the OV10640. The sensor registers are programmed by the Electronic Control Unit (ECU) from the LVDS back channel. There can also be a local micro-controller in each camera and the ECU can control the sensor via the micro-controller.

figure 1-2 multi-camera block diagram



note 1 OV490 or similar ISP processor is required to generate YUV or RGB for digital display

10640_DS_1_2

1.2 signal description and pin assignment

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV10640 image sensor. The package information is shown in **section 10**.

table 1-1 signal descriptions (sheet 1 of 3)

pin number	signal name	pin type	description
A1	DGND	ground	I/O ground
A2	DGND	ground	I/O ground
A3	DGND	ground	I/O ground
A4	DGND	ground	I/O ground
A5	DVDD	power	digital circuit power
A6	SVDD	power	sensor analog power
A7	DOVDD	power	I/O power (1.8V)
A8	DVDD	power	digital circuit power
A9	DGND	ground	I/O ground
A10	DGND	ground	I/O ground
B1	AGND	ground	analog ground
B2	AGND	ground	analog ground
B3	AVDD_LO	power	analog power (low power modules)
B4	VH1	analog I/O	analog reference
B5	AVDD	power	analog power
B6	**PCLK**	output	video output clock
B7	**HREF**	output	video output horizontal signal
B8	**VSYNC**	output	video output vertical signal
B9	AGND	ground	analog ground
B10	AGND	ground	analog ground
C1	SVDD_PIX	power	sensor power (pixel array)
C2	SVDD	power	sensor power (miscellaneous analog)
C3	AGND	ground	analog ground
C4	AGND	ground	analog ground
C5	ATEST	analog I/O	analog test I/O

table 1-1 signal descriptions (sheet 2 of 3)

pin number	signal name	pin type	description
C6	DOVDD	power	I/O power
C7	PLL DVDD	power	PLL digital power
C8	**XVCLK**	input	system clock input
C9	PLL AVSS	ground	PLL ground
C10	PLL AVDD	power	analog power for PLL
D1	DGND	ground	I/O ground
D2	AVDD	power	analog power
D3	AGND	ground	analog ground
D4	DOVDD	power	I/O power
D5	DOVDD	power	I/O power
D7	**MDP0/D4**	output	MIPI_LVDS data output/DVP data output
D8	MTXAVDD	power	MIPI TX analog power
D9	**MDP2/D2**	output	MIPI_LVDS data output/DVP data output
D10	**MDN2/D3**	output	MIPI_LVDS data output/DVP data output
E1	**BPREGD**	input	bypass DVDD regulator
E2	DGND	ground	I/O ground
E3	DVDD	power	digital circuit power
E4	DVDD	power	digital circuit power
E5	**PWDNB**	input	power down (active low with pull up resistor)
E6	MTXDVDD	power	MIPI TX digital power
E7	**MDN0/D5**	output	MIPI_LVDS data output/DVP data output
E8	**MCN/D7**	output	MIPI_LVDS clock output/DVP data output
E9	**MCP/D6**	output	MIPI_LVDS clock output/DVP data output
E10	MTXAVSS	ground	MIPI TX analog ground
F1	**GPIO2**	I/O	general purpose I/O
F2	**GPIO1**	I/O	general purpose I/O
F3	**GPIO0/FSIN**	I/O	general purpose I/O/frame sync input
F4	**SIOC**	input	SCCB interface input clock
F5	**RESETB**	input	reset/power down (active low with pull up resistor)
F6	**MDP1/D8**	output	MIPI_LVDS data output/DVP data output

table 1-1 signal descriptions (sheet 3 of 3)

pin number	signal name	pin type	description
F7	**MDN1/D9**	output	MIPI_LVDS data output/DVP data output
F8	**MDN3/D11**	output	MIPI_LVDS data output/DVP data output
F9	**MDP3/D10**	output	MIPI_LVDS data output/DVP data output
F10	MTXAVSS	ground	MIPI TX analog ground
G1	DGND	ground	I/O ground
G2	DGND	ground	I/O ground
G3	**SIOD**	I/O	SCCB interface data pin
G4	DOVDD	power	I/O power
G5	DVDD	power	digital circuit power
G6	**D1**	output	DVP data output
G7	**D0**	output	DVP data output
G8	**TM**	input	test mode (active high with pull down resistor)
G9	DGND	ground	I/O ground
G10	DGND	ground	I/O ground
H1	DGND	ground	I/O ground
H2	DGND	ground	I/O ground
H3	DGND	ground	I/O ground
H4	DGND	ground	I/O ground
H5	DGND	ground	I/O ground
H7	DOVDD	power	I/O power
H8	DVDD	power	digital circuit power
H9	DGND	ground	I/O ground
H10	DGND	ground	I/O ground

table 1-2 pin states under various conditions

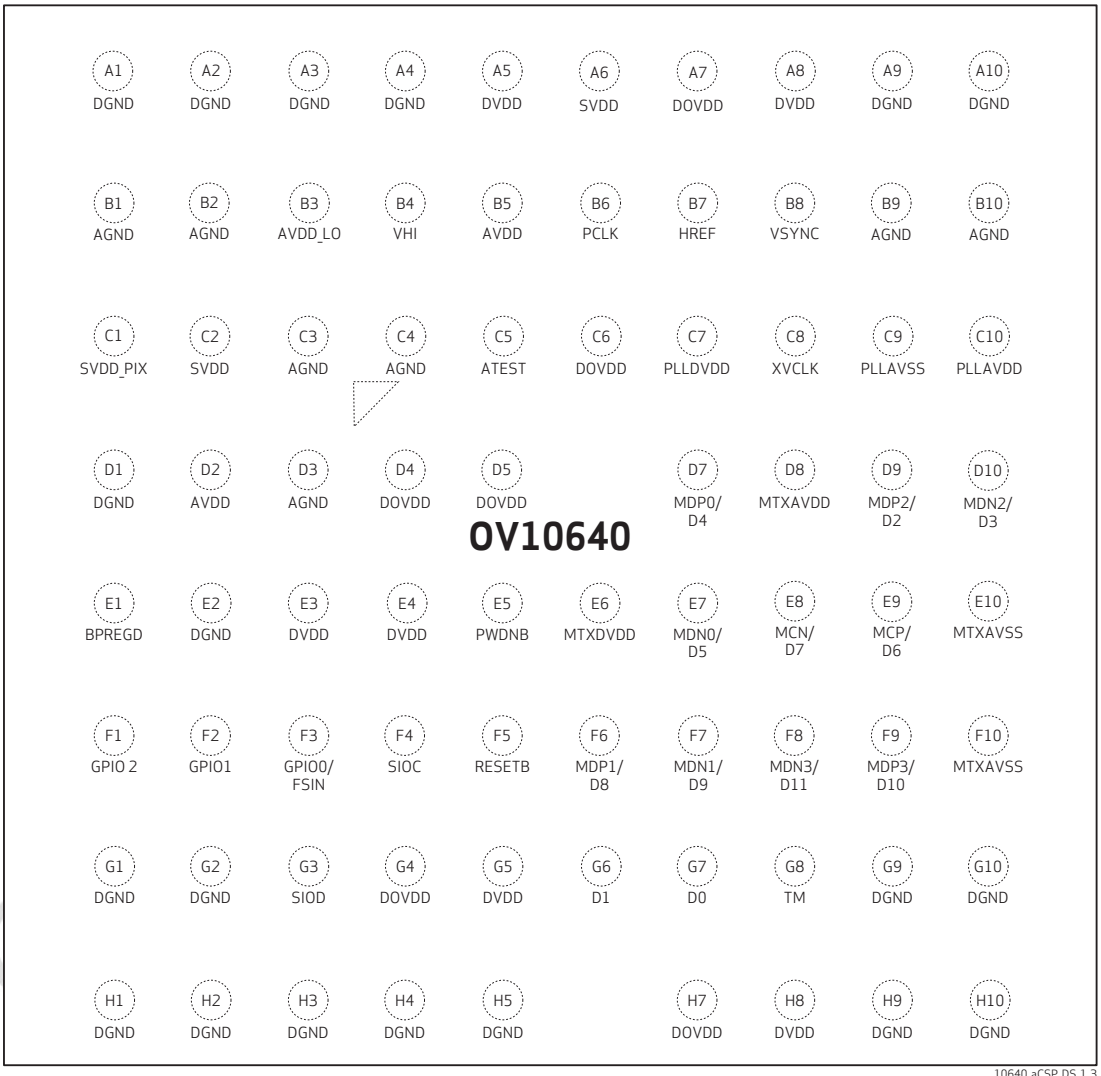
number	signal name	RESETB = 0	RESETB = 1 PWDNB = 1 stream/standby	RESETB = 1 PWDNB = 0 hardware standby/power down
B6	PCLK	output	output (configurable)[a]	output (configurable)[a]
B7	HREF	output	output (configurable)[a]	output (configurable)[a]
B8	VSYNC	output	output (configurable)[a]	output (configurable)[a]
C8	XVCLK	input	input	input
D7	MDP0/D4	output	output (configurable)[b]	output (configurable)[b]
D9	MDP2/D2	output	output (configurable)[b]	output (configurable)[b]
D10	MDN2/D3	output	output (configurable)[b]	output (configurable)[b]
E1	BPREGD	input	input	input
E5	PWDNB	input	input	input
E7	MDN0/D5	output	output (configurable)[b]	output (configurable)[b]
E8	MCN/D7	output	output (configurable)[b]	output (configurable)[b]
E9	MCP/D6	output	output (configurable)[b]	output (configurable)[b]
F1	GPIO2	input	input (configurable)[c]	input (configurable)[c]
F2	GPIO1	input	input (configurable)[c]	input (configurable)[c]
F3	GPIO0/FSIN	input	input (configurable)[c]	input (configurable)[c]
F4	SIOC	input	input	input
F5	RESETB	input	input	input
F6	MDP1/D8	output	output (configurable)[b]	output (configurable)[b]
F7	MDN1/D9	output	output (configurable)[b]	output (configurable)[b]
F8	MDN3/D11	output	output (configurable)[b]	output (configurable)[b]
F9	MDP3/D10	output	output (configurable)[b]	output (configurable)[b]
G3	SIOD	open-drain	open-drain	open-drain
G6	D1	output	output (configurable)[b]	output (configurable)[b]
G7	D0	output	output (configurable)[b]	output (configurable)[b]
G8	TM	input	input	input

a. 0x3023[3:0]: drive-strength

b. 0x3023[5]: drive-value, 0x3023[4]: drive enable

c. 0x3026[2]: input enable, 0x3026[1:0]: input drive strength, 0x3024[2:0] output enable

figure 1-3 pin diagram



top view
(bumps down)

table 1-3 pad equivalent circuit (sheet 1 of 2)

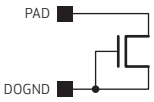
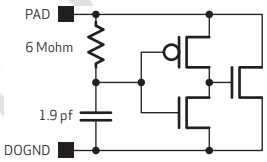
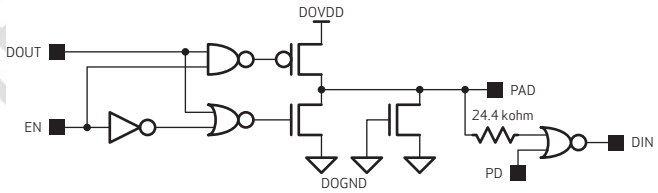
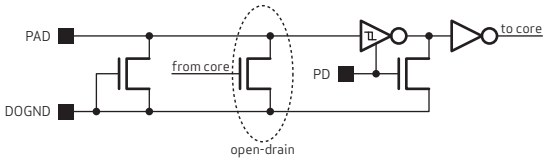
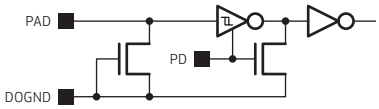
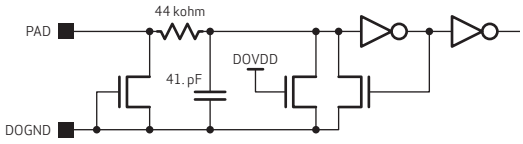
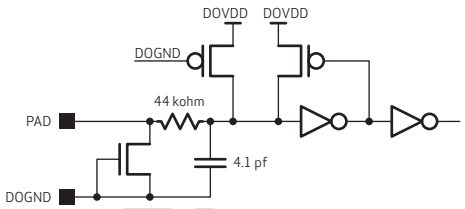
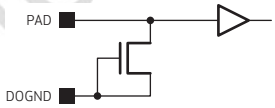
signal name	equivalent circuit
MTXAVSS, BPREGD, PLLAVSS, AGND, AVDD_LO, VHI, DGND, ATEST, MDP0/D4, MDP1/D8, MDP2/D2, MDP3/D10, MDN0/D5, MDN1/D9, MDN2/D3, MDN3/D11, MCN/D7, MCP/D6, SVDD_PIX	
MTXAVDD, DVDD, MTXDVDD, SVDD, DOVDD, AVDD, PLLAVDD	
PCLK, HREF, VSYNC, D0, D1, GPIO2, GPIO1, GPIO0/FSIN	
SIOD	
SIOC	
TM	

table 1-3 pad equivalent circuit (sheet 2 of 2)

signal name	equivalent circuit
RESETB, PWDNB	
XVCLK	

1.3 reference design

The silicon revision can be read from register 0x300D. **figure 1-4** shows the power supply and signal connection of the OV10640 when using MIPI interface.

figure 1-4 OV10640 MIPI reference schematic

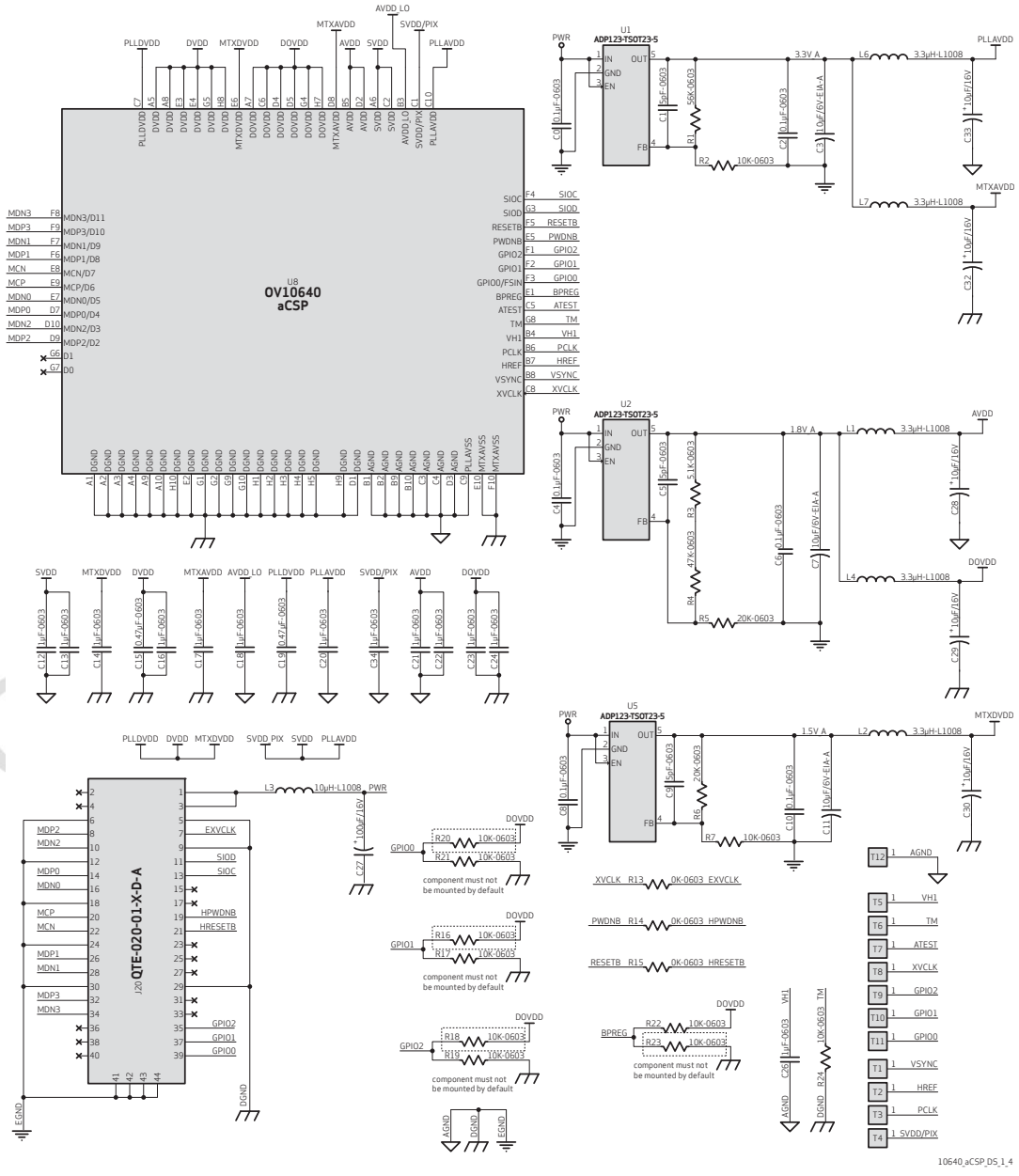
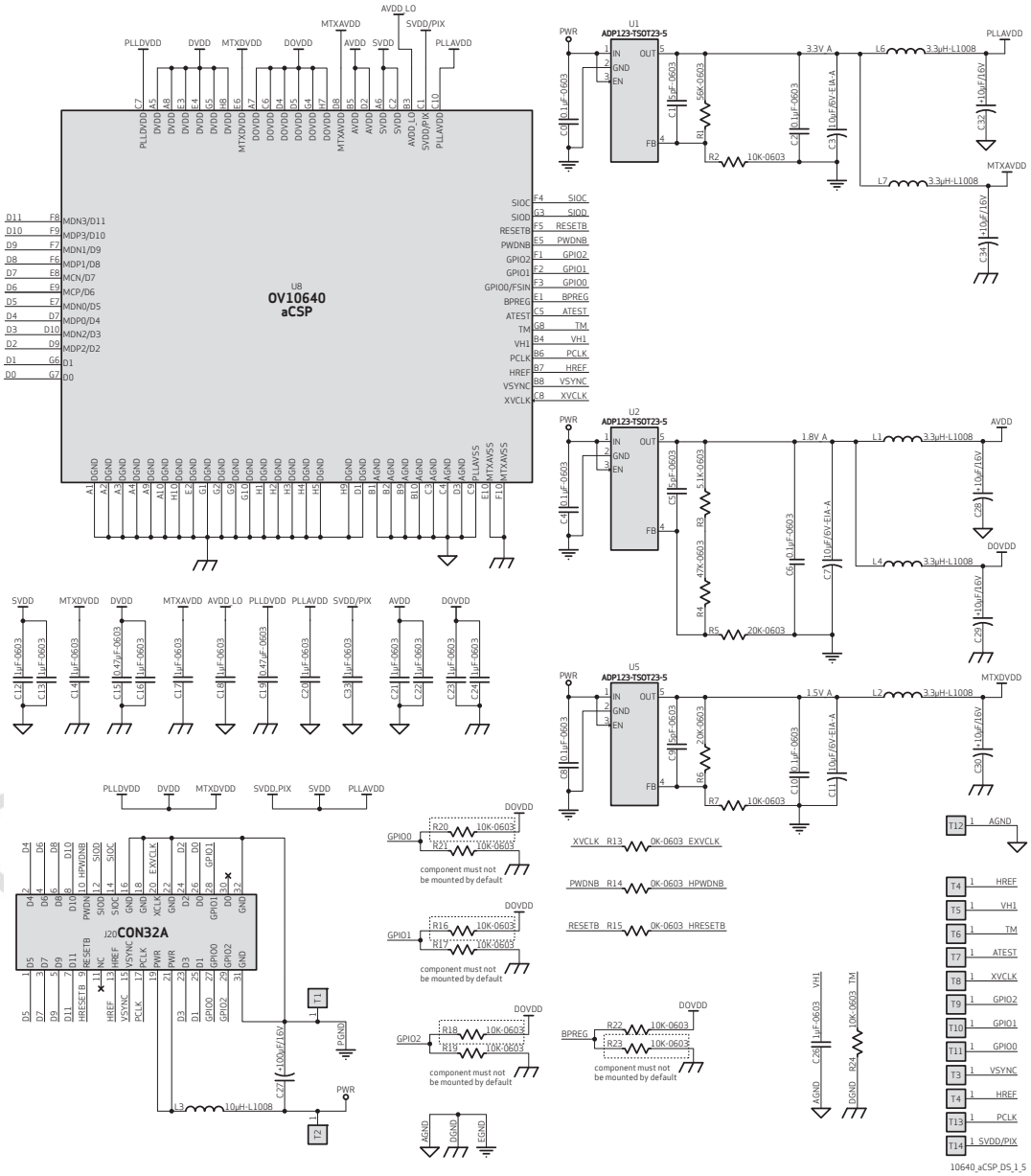


figure 1-5 shows the power supply and signal connection of the OV10640 when using DVP interface.

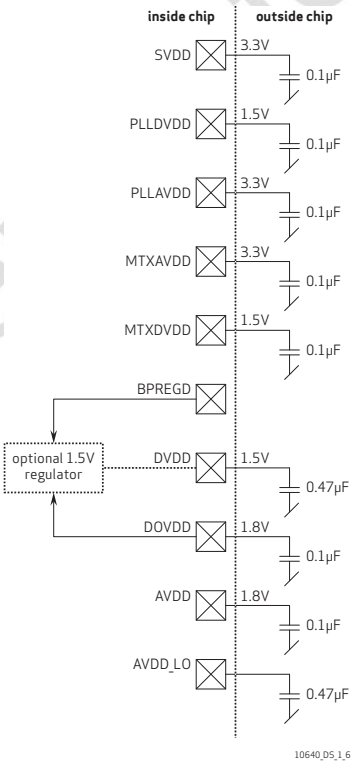
figure 1-5 OV10640 DVP reference schematic



1.3.1 external components

The pixel array is powered from 3.3V (SVDD). Analog supply is 1.8V (AVDD), except ADCs which operate on 1.5V (AVDD_LO) to save power and area. I/O pad power (DOVDD) is 1.8V. Core logic operates on 1.5V (DVDD). Optional embedded linear voltage regulator generates DVDD from DOVDD. The embedded DVDD regulator is selected when BPREGD is low, then the external 1.5V supply is not needed for DVDD. When BPREGD is high, 1.5V for DVDD must be supplied externally. The OV10640 must use external power de-coupling capacitors to reduce noise. The default capacitor value is 0.1µF, but for DVDD (when embedded voltage regulator is selected, BPREGH=low) and AVDD_LO, a capacitor of 0.47µF (ESR = 1Ω) is required. AVDD_LO should always be decoupled to ground via external capacitor. At power up, the power supplies should ramp up in 50 µs or more to avoid in-rush current during ramp-up.

figure 1-6 OV10640 power supplies and recommended external decoupling

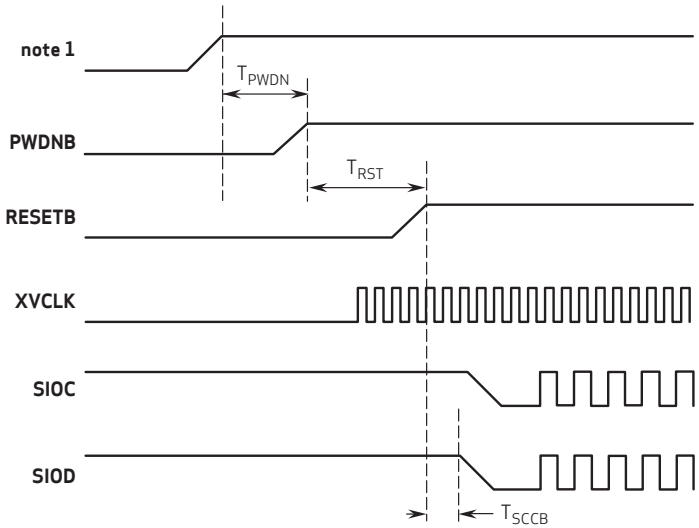


1.3.2 power on reset (POR) generation

The reset can be controlled from the external pin. However, inside this chip, there is a power on reset generation function to auto detect core power at stable state.

1.4 power up sequence/ boot sequence

figure 1-7 power on timing diagram



note 1 apply power in any sequence

note 2 T_{SCCB} = 255 + initialization time

10640_DS_1_7

When power is applied to the chip, the analog POR module keeps the chip in reset mode until the voltage is high enough to start operation. When the analog POR is released, an additional 255 XVCLK cycles are used to give some extra time for the system to stabilize. To extend this period, keep the RESETB pin low. The chip will then enter software reset state (SW_RESET). SW_RESET can also be reached by any other state by writing the software reset bit over SCCB.

T_{SCCB} starts from RESETB going high or when XVCLK is present, whichever is last. To ensure XVCLK is stable before reset mode is released, a minimum of 255 XVCLK cycles is waited before release. Then some additional initialization time will pass before standby state is entered and the sensor can be programmed over SCCB.

table 1-4 power on timing

parameter	min	max	unit
T_{AVDD}	0	n/a	ms
T_{DVDD}	0	10	ms
T_{PWDN}	1	n/a	ms
T_{RST}	0	n/a	ms
T_{SCCB}	255 + initialization time	n/a	XVCLK cycles

1.4.1 power down sequence

When in standby mode, power down mode can be entered by pulling the PWDNB pin low. In this state, all internal clocks are gated and the internal regulator is set in a power-saving low-power mode. When the regulator resumes from low power mode 255 XVCLK cycles are waited before turning on any clocks to ensure safe operation. The power down mode can only be entered from the standby mode. DVDD should be turned off before DOVDD because current can be conducted from DVDD to DOVDD through the regulator when DOVDD is not supplied.

1.4.2 operating modes

A software reset is required to reset all registers back to their default values. Set register 0x3013[0] and the sensor will be in standby mode after the software reset. It is highly recommended to wait 10ms before programming other registers after a software reset.

The OV10640 supports the following modes:

- reset mode
  - enabled when RESETB pin low
  - all modules brought to reset, including registers
  - IOs tri-stated
  - no active clocks
  - disabled SCCB
- power down mode (suspend mode)
  - enabled when PWDNB pin low
  - similar to reset mode, except register values are maintained
  - IOs de-activated (can be tri-stated or driven high or low by register control)
  - clock input is blocked to internal circuit logic control
  - internal clocks stopped
  - all sensor modules powered off, including SCCB
- standby mode
  - asserted after power-up and after SCCB command register 0x3013[0]=0
  - all modules powered ON
  - pads are active
  - PLL stopped (if early activation is not enabled)
- streaming mode
  - image capture and output streaming enabled

1.4.3 activation sequence

In standby mode, by setting register 0x3012[0]=1, the necessary analog modules and the PLLs are turned on. When the PLLs are stable after 4096 XVCLK cycles, the main clocks are switched from XVCLK to the faster PLL clock. When Tinit is done, streaming is activated.

1.4.4 deactivation sequence

In streaming mode, by clearing register 0x3012[0], the chip will enter standby after finishing the current frame (finish is signaled by VSYNC at the DVP-FIFO). The main clock is switched from PLL to XVCLK clock. If early activation is not set, PLLs and analog modules are turned off. To further reduce the power consumption from the standby state, the PWDNB pin can be pulled low. When this pin is low, the chip is not accessible through SCCB.

All registers are reset to default value by writing the software reset bit over SCCB. It is highly recommended to wait 10ms before programming other registers after a software reset.

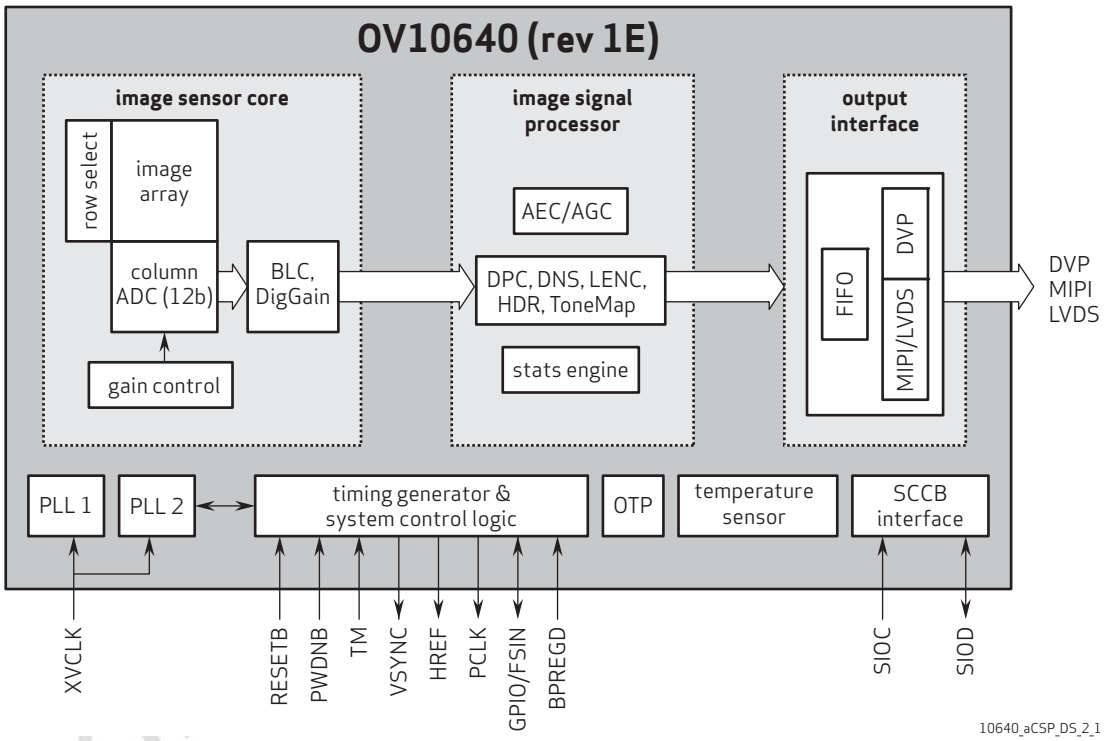
1.4.5 early activation

For faster activation, the user can choose to power up the analog modules and PLLs in standby mode. Since the PLLs are dependent on the analog to be powered up, register 0x3014[1] must be set to turn on the analog modules and for early PLL startup to work. Early PLL startup is enabled by setting register 0x3014[0].

2 sensor architecture

figure 2-3 shows the top level block diagram of the OV10640 sensor.

figure 2-1 OV10640 block diagram



The sensor consists of three major functional blocks: image sensor core, image signal processor, and output interface.

The image sensor core receives the photo signal which generates electrical charge collected by the pixel photo diodes (PDs). During readout, the accumulated charge is converted to a voltage signal in the pixel. This signal is then amplified and converted to a digital signal by the analog-to-digital converter (ADC). Dark current and circuit offsets are compensated by the black level correction circuit (BLC). The correction is implemented purely in the digital domain. Dark current increases exponentially with temperature and the BLC can be configured to automatically re-trigger with changes in junction temperature, in addition to changes in gain. The sensor core supports readout of three exposure values; long (L), short (S), and very short (VS), that can be used to process a high dynamic range (HDR) image. Each pixel consists of a large and small PD. The large PD (LPD) is used for the long and very short exposure channels, whereas the small PD (SPD) is used for the short exposure channel. The BLC runs separately on the three exposure channels.

The video stream from the image sensor core is applied to the image signal processor, which processes the data to generate the desired output format. Statistic data is calculated by the image processor and then applied to the automatic exposure control (AEC), automatic gain control (AGC), and automatic dynamic range control (ADRC) in order to control

the exposure time and gain of the long, short, and very short exposure channels. The output from the three exposure channels are combined to create an HDR output image. The image processor also supports lens correction (LENC), defect pixel correction (DPC), de-noise (DNS), and HDR global tone mapping (reversible).

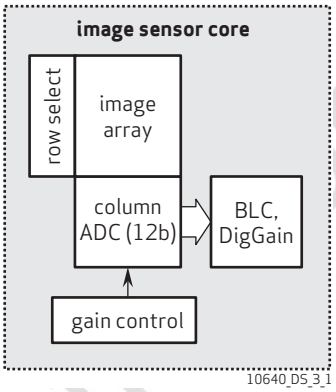
The processed image is formatted and output through the digital video port (DVP) interface or through the MIPI/LVDS interface. The supported output formats include combined 12/16/20-bit HDR, 2x12 bits compressed and 12-bit RAW data for each of the three exposure channels. Two on-chip phase lock loops (PLLs) generate the required clock signals for all blocks from the XVCLK input clock The timing generator generates the control signals for the pixel array to reset the PDs at the beginning of the exposure, to stop the exposure by reading out the accumulated charge, and also to generate the required control timing for the readout amplifier and ADC. In DVP mode, the horizontal synchronization reference (HREF), vertical synchronization (VSYNC), and pixel clock (PCLK) signals are also generated so the backend processor can receive the image data.

All functional blocks are controlled by registers. The host controller can program and read back through the Serial Camera Control Bus (SCCB) interface.

3 image sensor core

figure 3-1 shows the top level block diagram of the OV10640 image sensor core.

figure 3-1 sensor core block diagram

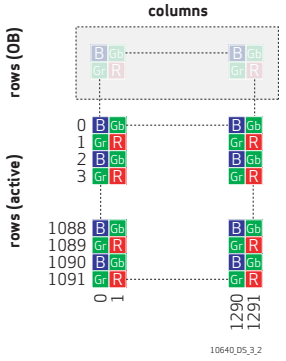


The image sensor core consists of the active pixel array, row access control circuit, column parallel ADC with gain control, and analog readout channel. A single analog readout channel is used for processing of the three exposure channels (L, S, VS). This provides optimal matching between the exposure channels. Gain and BLC are implemented in digital domain.

3.1 pixel array structure

The OV10640 sensor has an image array of 1292 columns by 1092 rows covered with color filters arranged in a Bayer pattern. **figure 3-2** shows the pixel array color filter layout. In addition to the active pixel rows, optical black (OB) pixel rows are embedded to serve as reference pixels for the black level correction (BLC). The OB rows are covered with a light shield (solid metal layer). In order to minimize non-ideal edge effects in the output image, it is not recommended to use the pixels at the lowest and highest row and column addresses.

figure 3-2 pixel array region color filter layout



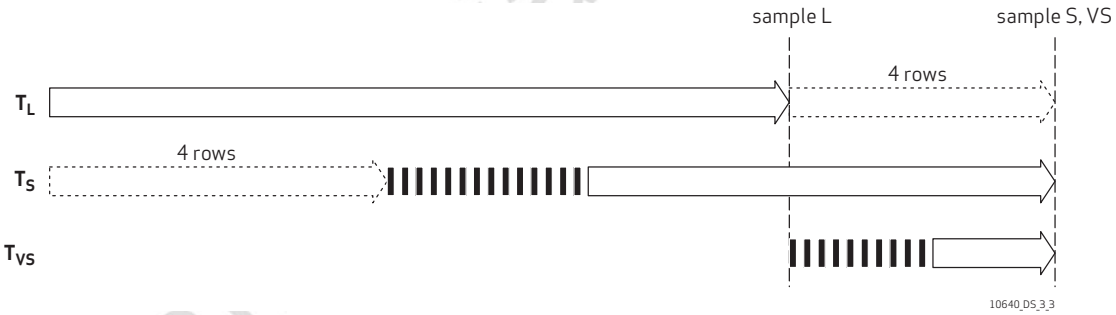
Each pixel has two photo diodes (PDs) with independent exposure and gain controls to extend the dynamic range. The two PDs also have different sizes to provide different sensitivity. The large PD (LPD) provides high sensitivity and the small PD (SPD) provides low sensitivity. The OV10640 supports triple exposure readout, with two exposures in spatial domain, and the shortest exposure in time domain:

- long exposure (L) using the large photodiode (LPD), also used in linear (non-HDR) mode
- short exposure (S) using the small photodiode (SPD) with an exposure time of equal or less than long exposure time
- very short (VS) using large photodiode (LPD), in the range of approximately 0.1 to 3.9 row time

The integration time for S (T_S) will always start four rows or later after integration time for L (T_L) start and finish four rows after T_L.

The integration time for VS (T_{VS}) will always start after (T_L) finish. The sampling point is four rows after, but the T_{VS} start can move from end of T_L to just before sampling of T_{VS} (see **figure 3-3**).

figure 3-3 integration time diagram



The OV10640 can operate according to five sensor exposure modes:

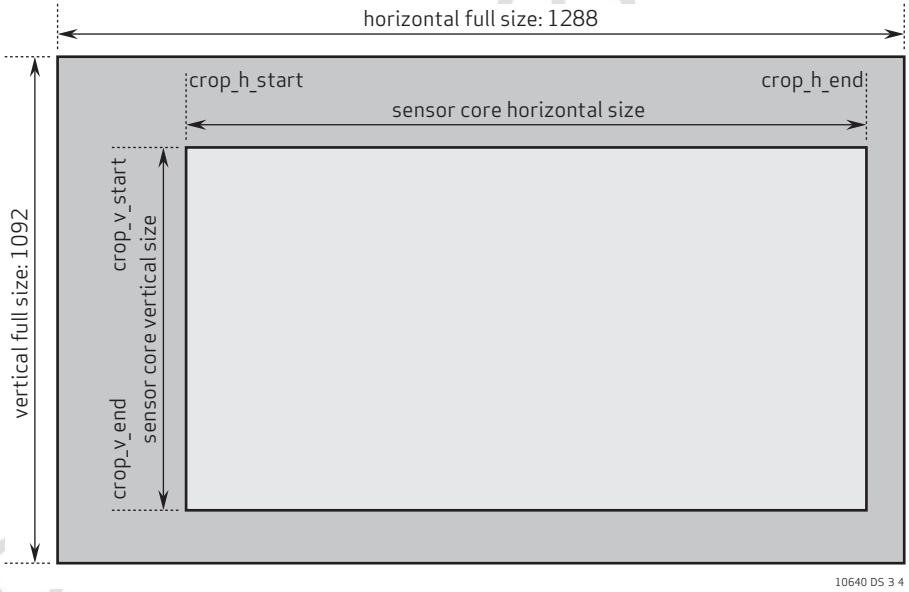
- three exposure mode: HDR mode with all three exposures valid
- L, S exposure mode: HDR mode with only long and short exposures valid
- L, VS exposure mode: HDR mode with only long and very short exposure valid
- L exposure mode: linear mode using only L exposure

Refer to **section 5,** HDR auto exposure control (AEC debug mode) for details.

3.2 pixel array access

The readout window is fully programmable from 256 to 1292 in steps of 4 (8 in sub-sampling) in the horizontal direction and 20 to 1092 in steps of 2 (4 in sub-sampling) in the vertical direction. Start address must be at an even row and column and end address must be at an odd row and column address in order to preserve the Bayer pattern order. The 'crop' address in registers 0x3074~0x307B programs the sensor core readout window and can be set freely within the pixel array. The crop window is programmed larger than the processed output image resolution because the ISP uses extra rows and columns for the image processing algorithms (e.g., defect pixel correction).

figure 3-4 pixel array access diagram



3.3 mirror and flip

The pixel array can be accessed in the reverse order in column and row directions (i.e., the image can be horizontally mirrored and vertically flipped) using register 0x3090[3:2]. Refer to **figure 3-5**. The sensor will not shift the start address in mirror and flip mode and color will be shifted in output. The ISP can shift the color and get the same Bayer pattern as non-mirrored 0x3291[2:1], to ensure correct ISP processing register 0x3128[1:0] must also be set. The DVP output size must be larger than the array crop size when using the ISP shift function and the output column size (DVP_h_size) must be reduced to closest multiple of 8.

figure 3-5 horizontal mirror and vertical flip samples

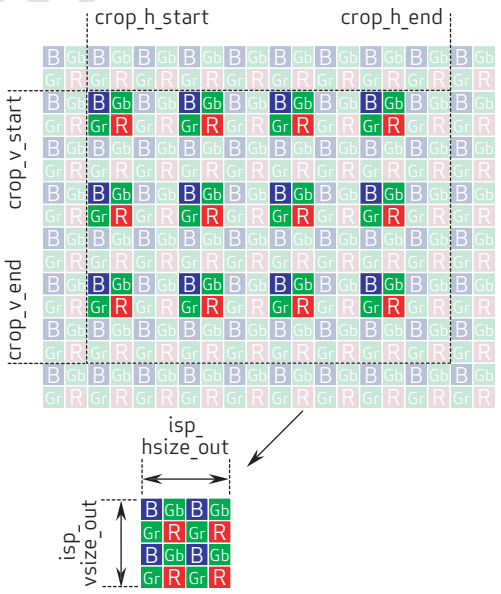
original image | mirrored image | flipped image | mirrored and flipped image

10640_DS_3_5

3.4 sub-sampling

The pixel array can be sub-sampled by a factor of 2 in both horizontal and vertical directions, controlled by register 0x308F[1:0]. The sub-sampling is done in the sensor core. The ISP processes the output from the sensor core as a continuous stream of pixel values and generates a lower resolution output image. The horizontal and vertical sub-sampling can be programmed independently. The vertical sub-sampling enables a higher frame rate since the number of rows per frame is reduced, whereas the horizontal sub-sampling will not enable a higher frame rate since the number of clock periods per row is not reduced when horizontal sub sampling is enabled.

figure 3-6 horizontal and vertical sub-sampling



note when using sub-sampling, the size (crop_h_end - crop_h_st+1) and (crop_v_end - crop_v_st + 1) must be multiple of four

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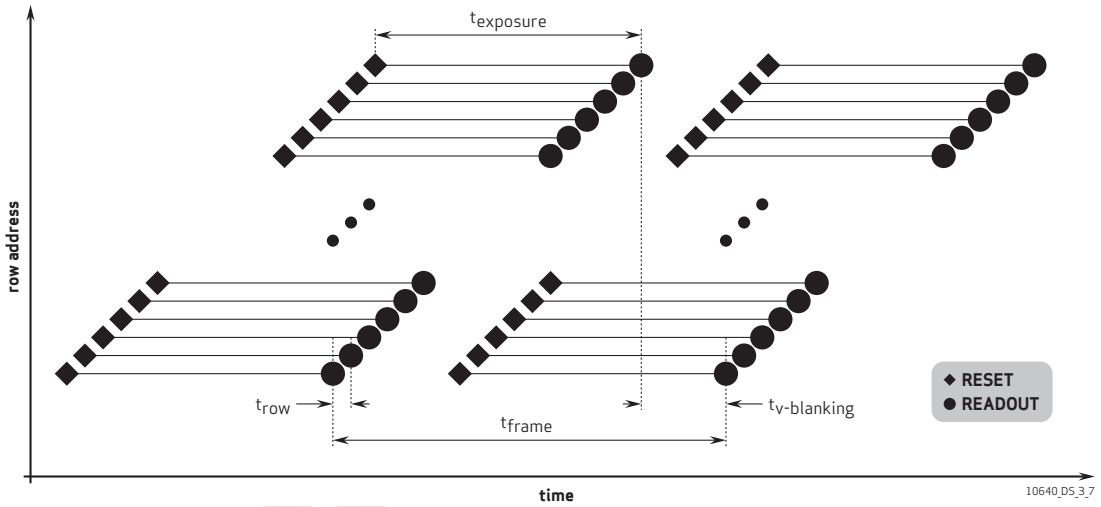
3.5 frame timing and maximum frame rate

The OV10640 employs an electronic rolling shutter (ERS) for exposure control (see **figure 3-7**). The pixel array is first reset row by row and when the exposure time has elapsed, the readout of the pixel array is done row by row.

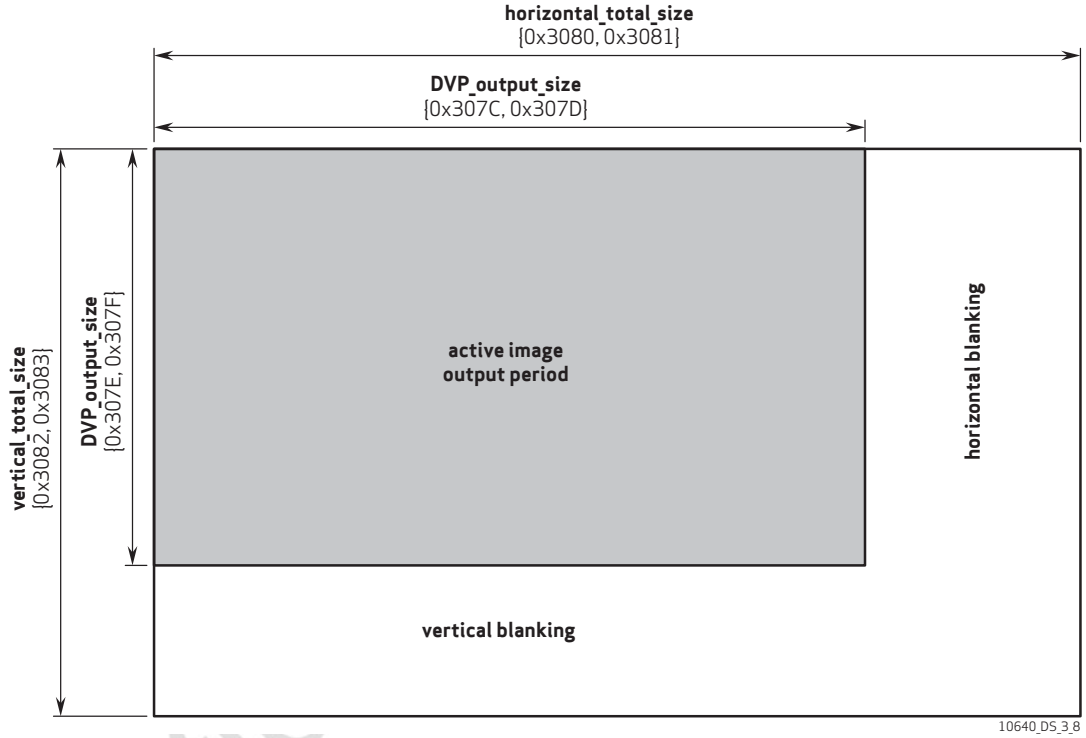
figure 3-7 row address versus time graph



The timing generator generates all the control signals based on a row counter and column counter. Refer to **figure 3-8** for the frame timing. The row period consists of an active output period and a horizontal blanking period. A vertical blanking period is also required to perform frame-based operation. The vertical blanking period seen by the backend processor is usually longer than the internal vertical blanking because the BLC is reading the optical black rows required to perform the correction.

A minimum number of clock periods are required to complete all the required operations per row (blanking time). Refer to **section 6** for details.

figure 3-8 frame output timing diagram



The maximum frame rate is determined by the maximum pixel clock, total number of pixels read out of the entire frame and minimum horizontal/vertical blanking time. The system clock and the minimum blanking time are usually fixed for a given design and the frame rate is dependent on the number of pixels read out. If the requested output image size (DVP output size) is smaller than the full pixel array, it is not necessary to read out the whole pixel array, thus; the frame rate can be increased by cropping and/or sub-sampling the pixel array (see **figure 3-3** and **figure 3-6**). **table 3-1** lists the most common image sizes and maximum frame rates that the sensor can achieve. Other image sizes are also possible by cropping and/or sub-sampling. Refer to **section 6** output interface for details.

table 3-1 supported output formats and frame rates (sheet 1 of 2)

output data format	maximum frame rate at full frame		comments
	MIPI/LVDS	DVP	
20b combined HDR value	60 fps (800 Mbps/lane)	30 fps (100 MHz)	
3x12b unprocessed (L, S, VS)	60 fps (800 Mbps/lane)	20 fps (100 MHz)	

table 3-1 supported output formats and frame rates (sheet 2 of 2)

output data format	maximum frame rate at full frame		comments
	MIPI/LVDS	DVP	
2x12b unprocessed compressed	60 fps (800 Mbps/lane)	30 fps (100 MHz)	compressed means 3x12b turned into 2x11b, see **section 6.1.1** for details
12b combined tone mapped	60 fps (800 Mbps/lane)	60 fps (100 MHz)	tone mapped means 20b combined value is mapped to 12b using global and fixed PWL mapping function which is reversible at receiving end
16b combined log domain	30 fps (800 Mbps/lane)	30 fps (100 MHz)	HDR combine outputs 16b log domain. Mapping function: PV_20b = 2^(PV_16b/2048), where PV is pixel value2x 8b, 2 clocks per pixel

table 3-2 timing control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3074	CROP_H_ST_H	0x00	RW	Start Address Horizontal High Byte
0x3075	CROP_H_ST_L	0x00	RW	Start Address Horizontal Low Byte
0x3076	CROP_V_ST_H	0x00	RW	Start Address Vertical High Byte
0x3077	CROP_V_ST_L	0x02	RW	Start Address Vertical Low Byte
0x3078	CROP_H_END_H	0x05	RW	End Address Horizontal High Byte
0x3079	CROP_H_END_L	0x07	RW	End Address Horizontal Low Byte
0x307A	CROP_V_END_H	0x04	RW	End Address Vertical High Byte
0x307B	CROP_V_END_L	0x41	RW	End Address Vertical Low Byte
0x307C	DVP_H_SIZE_H	0x05	RW	DVP Horizontal Size High Byte
0x307D	DVP_H_SIZE_L	0x08	RW	DVP Horizontal Size Low Byte
0x307E	DVP_V_SIZE_H	0x04	RW	DVP Vertical Size High Byte
0x307F	DVP_V_SIZE_L	0x44	RW	DVP Vertical Size Low Byte
0x308A	EXTRA_DELAY_H	0x00	RW	(fs_delay) Last Row can be Extended by this Number of Clocks High Byte
0x308B	EXTRA_DELAY_L	0x00	RW	(fs_delay) Last Row can be Extended by this Number of Clocks Low Byte

table 3-2 timing control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x308C	SENSOR_CTRL	0x01	RW	Bit[7]: use_r_rst_num Bit[6]: fsin_intr_en When high, external input can generate interrupt when FSIN arrives Bit[5]: fsin_retro_mode When high, makes FSIN logic work Bit[4]: fsin_en When high, FSIN mode is enabled Bit[3]: low_power_mode When high, sensor will not read exposures that are disabled (single or 2 expo) Bit[1]: adc_swap_en When high, enables swapping of ADCs Bit[0]: extra_ctrl When high, extra delays will be reset when used once
0x3090	READ_MODE	0x00	RW	Bit[7:5]: hdr_mode 000: hdr_3exp 001: s_2exp 010: lvs_2exp 011: l_1exp 100: Reserved Bit[3]: Flip Bit[2]: Mirror

3.6 black level calibration (BLC)

The black level correction (BLC) function is used to set the pixel output of a complete black object to a programmable pedestal value in all kinds of lightning conditions. Due to circuit offset and pixel dark current, the pixel output level of a black object is normally non-zero. The OV10640 calibrates the black level of the active pixel by subtracting the true optical black pixel output.

The target BLC pedestal value for long, short, and very short exposure channels are set by registers {0x30C3, 0x30C4}, {0x30C5, 0x30C6}, and {0x30C7, 0x30C8}, respectively. The pedestals are 12-bit values. The ISP will subtract the pedestal value early in the signal processing path.

Enabling the BLC is controlled by the register 0x30B9[4]. When the BLC is enabled, the active pixel output value will be limited to 0xFFF after subtracting the optical black pixel value. When the BLC is disabled, no black pixel subtraction is performed.

Optical black rows are used for BLC and are not output in the final image, but enabling show_dark_rows (0x30B9[0]) will output the black rows at the beginning of the output frame.

3.6.1 advanced operation of the BLC

The BLC is based on measuring the value at the center of the distribution of the optical black reference pixels and applying digital correction to bring the center to the predefined target value. The center of the pixel distribution is estimated from a combination of median and average filtering. The filtering for the BLC is based on the middle 896 columns of the 2, 4, or 8 optical dark rows. The selection of number of dark rows is performed in register 0x308D for timing control. Only the values closest to the horizontal center of each row are used in order to minimize influence from any edge effects in the array.

During normal operation, dark current is expected to change slowly with time. During slow changes, the BLC in the OV10640 will not change the correction value before a certain delta is measured. This triggering is configurable in the blc_trigger_threshold registers for long, short, and very short exposures in registers 0x30CA, 0x30CB, and 0x30CC, respectively. When one of these thresholds is crossed, the correction value is updated with an exponential moving average smoothing filter. The fractional smoothing factor is configurable in 0x30BA and affects the α in:

$correction_{FILTER} = correction_{LAST} + \alpha \times (correction_{NEW} - correction_{LAST}), 0 \leq \alpha \leq 1$

α is encoded as a 5-bit register value, so that α = (smoothing+1)/32. Setting smoothing to 0 means that no update is applied, while setting smoothing to 32 means that the new value is directly applied without smoothing.

While dark current changes slowly with time, when starting up, changing gain or exposure time, a rapid change will occur in the dark level. In the OV10640, this is handled as a hard trigger, where the newly measured dark level is used directly on the new frame. Slowly changing dark-level is handled through the smoothing filter when the BLC is soft-triggered through the trigger thresholds.

After a trigger, it is possible to have the BLC soft-triggered for a number of frames, configurable in 0x30CD. This can help average noise over multiple frames after a hard trigger.

It is possible to disable the threshold crossed triggers by writing the blc_trigger_threshold registers to 0xFF. It is also possible to handle the threshold crossed triggers as hard triggers by setting the 0x30C9[1] bit to 1.

Manual triggering is possible by writing a 1 to the 0x30C9[0] bit. Note that this bit must be manually cleared. To manually cause a hard-trigger, the 0x30C9[1] bit must also be set.

table 3-3 BLC control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x30B9	BLC_CTRL	0x22	RW	Bit[6]: show_dark_cols Bit[4]: blc_override_en Bit[3]: blc_cont_update_mode Bit[2]: blc_stretch_en Bit[1]: blc_dither_en Bit[0]: show_dark_rows
0x30BA	BLC_SMOOTHING	0x07	RW	Filter Coefficient Alpha=(smoothing+1)/32 If zero, new value is not used

table 3-3 BLC control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x30BB	D_VALUE_LARGE	0x00	RW	Signed Fractional (/64) Value Between -32/64 and 32/64 to adjust DL'=DL(1+D)
0x30BC	D_VALUE_SMALL	0x00	RW	d_value_small
0x30BD	BLC_OVERRIDE_L_H	0x00	RW	blc_override_l High Byte
0x30BE	BLC_OVERRIDE_L_L	0x00	RW	blc_override_l Low Byte
0x30BF	BLC_OVERRIDE_S_H	0x00	RW	blc_override_s High Byte
0x30C0	BLC_OVERRIDE_S_L	0x00	RW	blc_override_s Low Byte
0x30C1	BLC_OVERRIDE_VS_H	0x00	RW	blc_override_vs High Byte
0x30C2	BLC_OVERRIDE_VS_L	0x00	RW	blc_override_vs Low Byte
0x30C3	BLC_TARGET_L_H	0x00	RW	blc_target_l High Byte
0x30C4	BLC_TARGET_L_L	0x80	RW	blc_target_l Low Byte
0x30C5	BLC_TARGET_S_H	0x00	RW	blc_target_s High Byte
0x30C6	BLC_TARGET_S_L	0x80	RW	blc_target_s Low Byte
0x30C7	BLC_TARGET_VS_H	0x00	RW	blc_target_vs High Byte
0x30C8	BLC_TARGET_VS_L	0x80	RW	blc_target_vs Low Byte
0x30C9	BLC_TRIGGER	0x1C	RW	Bit[4]: blc_exp_changed_trig_en Bit[3]: blc_gain_changed_trig_en Bit[2]: blc_restart_frame_trig_en Bit[1]: blc_hard_trigger_en Bit[0]: blc_manual_trig
0x30CA	BLC_TRIGGER_ THRESHOLD_L	0x10	RW	blc_trigger_threshold_l
0x30CB	BLC_TRIGGER_ THRESHOLD_S	0x10	RW	blc_trigger_threshold_s
0x30CC	BLC_TRIGGER_ THRESHOLD_VS	0x10	RW	blc_trigger_threshold_vs
0x30CD	RESTART_FRAMES	0x01	RW	Number of Frames with Continuous Update After Restart
0x30CE	HOT_THRESHOLD	0x40	RW	Threshold for Setting the "Hot" Flag to Auto Exposure
0x30CF	AB_CTRL	0x00	RW	Bit[1]: Bframe Bit[0]: ab_mode
0x30D0	DARK_CURRENT_L_H	–	R	dark_current_l High Byte

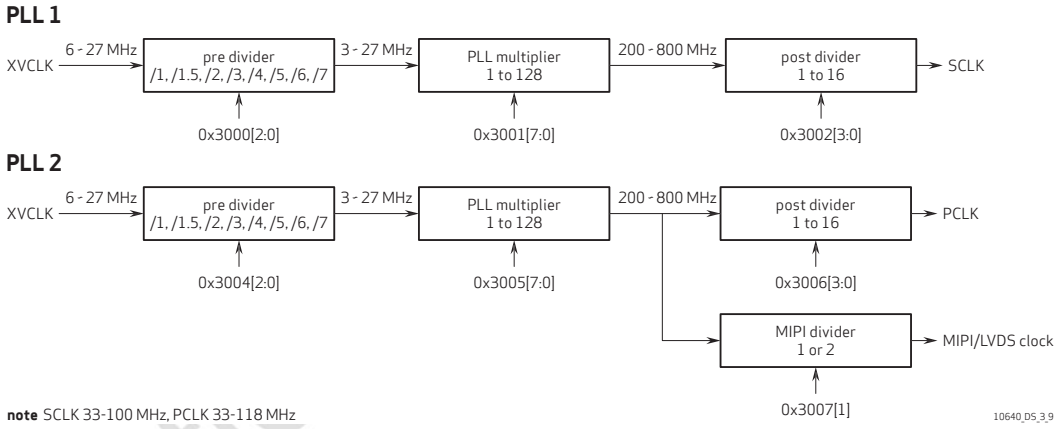
table 3-3 BLC control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x30D1	DARK_CURRENT_L_L	–	R	dark_current_l Low Byte
0x30D2	DARK_CURRENT_S_H	–	R	dark_current_s High Byte
0x30D3	DARK_CURRENT_S_L	–	R	dark_current_s Low Byte
0x30D4	DARK_CURRENT_VS_H	–	R	dark_current_v High Byte
0x30D5	DARK_CURRENT_VS_L	–	R	dark_current_vs Low Byte
0x30D6	ROW_AVERAGE_L_H	–	R	row_average_l High Byte
0x30D7	ROW_AVERAGE_L_L	–	R	row_average_l Low Byte
0x30D8	ROW_AVERAGE_S_H	–	R	row_average_s High Byte
0x30D9	ROW_AVERAGE_S_L	–	R	row_average_s Low Byte
0x30DA	ROW_AVERAGE_VS_H	–	R	row_average_vs High Byte
0x30DB	ROW_AVERAGE_VS_L	–	R	row_average_vs Low Byte
0x30DC	DIG_GAIN_L_H	–	R	Digital Gain for L Exposure High Byte
0x30DD	DIG_GAIN_L_L	–	R	Digital Gain for L Exposure Low Byte
0x30DE	DIG_GAIN_S_H	–	R	Digital Gain for S Exposure High Byte
0x30DF	DIG_GAIN_S_L	–	R	Digital Gain for S Exposure Low Byte
0x30E0	DIG_GAIN_VS_H	–	R	Digital Gain for VS Exposure High Byte
0x30E1	DIG_GAIN_VS_L	–	R	Digital Gain for VS Exposure Low Byte

3.7 PLL

The OV10640 implements two PLLs with both inputs connected to the XVCLK pin. One can support the MIPI/LVDS bit clock and output clock PCLK, while the other one can support internal SCLK. Two PLLs enable the internal clock (SCLK) to be separate from the output clock (PCLK). Additionally, the two PLLs, in MIPI/LVDS mode, can be used to optimize for EMC and/or minimize the required MIPI frequency. In DVP mode, they can be used to output data with PCLK = 2xSCLK (or 3xSCLK) when outputting 16b/20b (or 3x12b) per pixel. When using both PLLs, SCLK will come from PLL top (see **figure 3-9**). MIPI/LVDS bit clock and PCLK will come from PLL bottom. PLL input clock frequency range should be 6-27MHz.

figure 3-9 PLL control diagram



note PLL must be configured at standby mode

table 3-4 PLL control registers

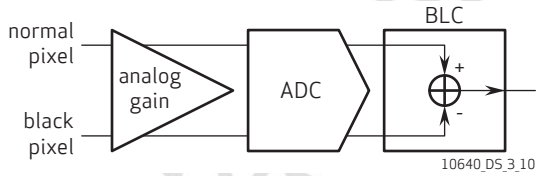
address	register name	default value	R/W	description
0x3000	SCLK_PLL_PRE	0x03	RW	SCLK PLL Pre Divider
0x3001	SCLK_PLL_MULT	0x62	RW	SCLK PLL Multiplier
0x3002	SCLK_PLL_POST	0x07	RW	SCLK PLL Post Divider (1-16)
0x3004	PCLK_PLL_PRE	0x03	RW	PCLK PLL Pre Divider
0x3005	PCLK_PLL_MULT	0x62	RW	PCLK PLL Multiplier (1-128)
0x3006	PCLK_PLL_POST	0x07	RW	PCLK PLL Post Divider (1-16)
0x3007	PCLK_PLL_CTRL	0x01	RW	Bit[2]: pclk_pll_mipi_dis Disable MIPI clock output Bit[1]: pclk_pll_mipidiv2 Divide frequency to MIPI/LVDS by 2 Bit[0]: pclk_pll_enable Enable PLL2

3.8 ADC range and minimum gain

The OV10640 implements a high precision low noise 12-bit ADC per column. The ADC range is maximized to leave room for dark current, and thus, is greater than pixel full well capacity (FWC), so a minimum gain must be applied to ensure that bright objects can always saturate and the pixel response is linear before saturation.

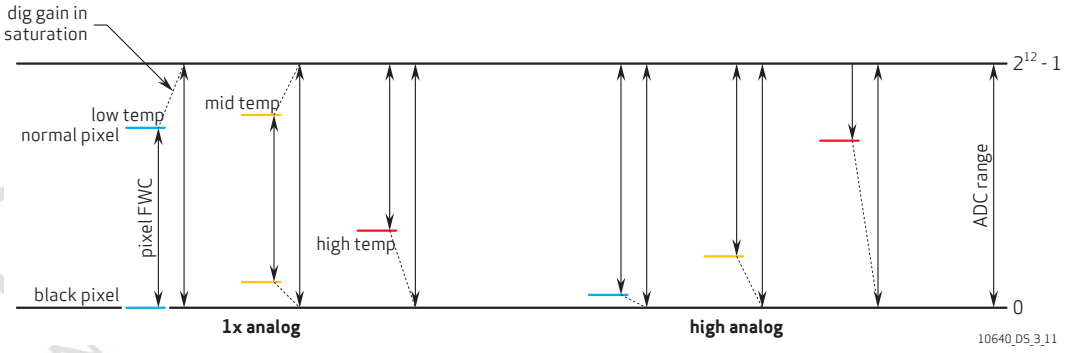
As shown in **figure 3-10**, the optical black pixel value is subtracted from the normal pixel in the black level calibration (BLC) block to keep black level consistent over temperature.

figure 3-10 ADC and BLC diagram



The black pixel's output value, y_Black, is not always 0 due to dark current. **figure 3-11** shows the black pixel value and the highest value of a normal pixel at different temperature and analog gain. A minimum (digital) gain must be applied after BLC to compensate the ADC range eaten by dark current.

figure 3-11 signal range, ADC range, and minimum gain



The minimum digital gain to stretch the remaining signal range to full ADC range is:

$$gain_{dig\_min} = \frac{4095 - C_{BLC}}{4095 - (y_{Black} + C_{ADC})}$$

where C_{BLC} is the black level pedestal, C_{ADC} is the ADC pedestal, y_{Black} is the black pixel output. y_{Black} is equal to dark current multiplied by analog gain.

$$y_{Black} = gain_{ana} \times y_{Dark}$$

where $gain_{ana}$ is analog gain and y_{Dark} is dark current. Dark current increases exponentially with temperature and linearly with exposure time. y_{Black} of L, S and VS channels can be read back from register {0x30D6, 0x30D7}, {0x30D8, 0x30D9} and {0x30DA, 0x30DB}, respectively.

$$y_{Black\_L} = register\ \{0x30D6, 0x30D7\}$$

$$y_{Black\_S} = register\ \{0x30D8, 0x30D9\}$$

$$y_{Black\_VS} = register\ \{0x30DA, 0x30DB\}$$

These registers are unsigned values. However, when y_{Black} is small, the calculation of y_{Black} may overflow and result in a big number (e.g., 0xFFE). In this case, the real y_{Black} can be calculated by subtracting 4096 from the register value. For example, 0xFFE means y_{Black} of -2. The dark current can be read back to distinguish real high y_{Black} from the overflowed value. When dark current is small, a big register value means y_{Black} is negative. The dark current of L, S and VS channels can be read back from registers {0x30D0, 0x30D1}, {0x30D2, 0x30D3}, and {0x30D4, 0x30D5}, respectively.

The ADC pedestal value, C_{ADC}, is also a function of analog gain. Please use following pedestal values to calculate the minimum digital gain (may change in the final setting). These values include the potential increase of y_{Black} before the next gain and exposure adjustment due to temperature change.

$$C_{ADC} = \begin{cases} 126, & when\ gain_{ana} = 1 \\ 312, & when\ gain_{ana} = 2 \\ 560, & when\ gain_{ana} = 4 \\ 1056, & when\ gain_{ana} = 8 \end{cases}$$

With minimum digital gain calculated following the above procedure, the max output of a normal pixel may be still less than 4095, so extra gain, preferably analog gain, is required. This gain can be calculated by the following formula:

$$gain_{extra\_min} = \frac{4095 - C_{BLC}}{y_{White} \times gain_{dig\_min}}$$

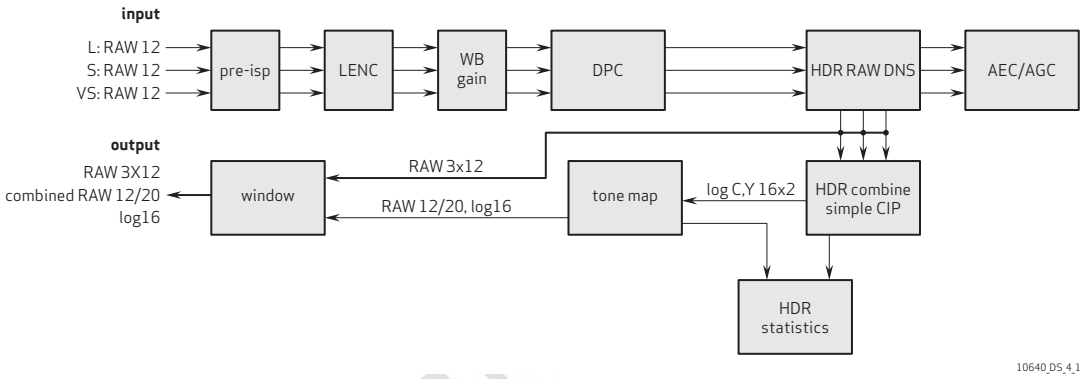
where y_{White} is the maximum value of normal pixel at 1x analog gain (i.e., the pixel FWC). For the OV10640, y_{White} is 3500 for L and VS, and 2048 for VS (may change for final production version). Please keep in mind that fractional analog gain is not supported and analog gain must be 1x, 2x, 4x or 8x.

In extremely strong illumination (e.g., the Sun or reflection from car body), the pixel reset level will drop quickly before the correlated double sampling (CDS) can result in a low readout value. This is known as black sun issue. The OV10640 has a built-in anti-Black Sun function. A minimum 1.4x digital gain is required for this circuit to operate properly. If the minimal digital gain calculated earlier is lower than 1.4x, the minimum gain must be set to 1.4x.

4 image processor

figure 4-1 shows the top level block diagram of the OV10640 image processor.

figure 4-1 image processor block diagram



The image processor pipeline (ISP) receives image data from the sensor core and includes modules for raw image processing. The video stream arrives as 12-bit parallel data separated in long exposure (L), short exposure (S) and very short exposure (VS) channels. Unused rows and columns are cut before further processing. After processing the data from the ISP, it is configured to the correct output format in the output interface.

One of the first processing steps in the ISP is to correct the shading caused by lens fall off (LENC). Digital gain is then applied to make the image white balanced (WB gain). Defect pixel and clusters (DPC) are corrected on-the-fly for each exposure channel and the de-noise filter (RAW DNS) reduces the noise in the raw image. RAW 12 for separated exposure channels can be output from here. Before the exposure channels are combined (HDR combine), a simple color interpolation (simple CIP) is applied. The image data in the dark area of the HDR image is from the L channel, while data in the bright area is from the S and VS channels. In the transition area, the data is linearly combined. The weighting used in the combination feeds back to the AEC/AGC and HDR combine to calculate the statistics.

4.1 test pattern

For testing purposes, the OV10640 offers analog and digital test patterns. The analog test pattern is a color bar as an overlay image (test pattern applied on pixel output to exercise the whole analog readout channel) and is enabled by setting register 0x305E[5]=1. The intensity of this color bar can be controlled by register 0x305F[3:0] and the order of colors can be swapped by setting register 0x305E[6]=1. The OV10640 also offers two digital effects for the test patterns: transparent effect and rolling bar effect. The digital test pattern function is enabled by register 0x3129[7] and the test pattern is selected by register 0x3129[6:0].

4.1.1 color bar

There are four types of color bars shown in **figure 4-2** selected from register 0x3129.

figure 4-2 color bar types

color bar (style 0) color bar (style 1)

color bar (style 2) color bar (style 3)

10640_DS_4_2

4.1.2 transparent effect

Transparent color bar image is selected by register 0x3129[5].

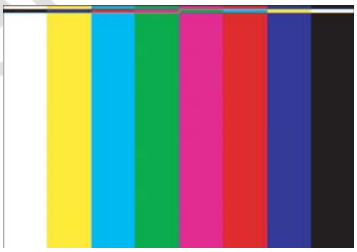
figure 4-3 transparent effect

10640_DS_4_3

4.1.3 rolling bar effect

Rolling bar on color bar image is selected by register 0x3129[6].

figure 4-4 rolling bar effect



10640_DS_4_4

Since digital test patterns pass through the pipeline, to get a consistent output pattern, a number of processing steps needs to be stopped before enabling the test pattern. Please contact your local OmniVision FAE to get a valid setting file.

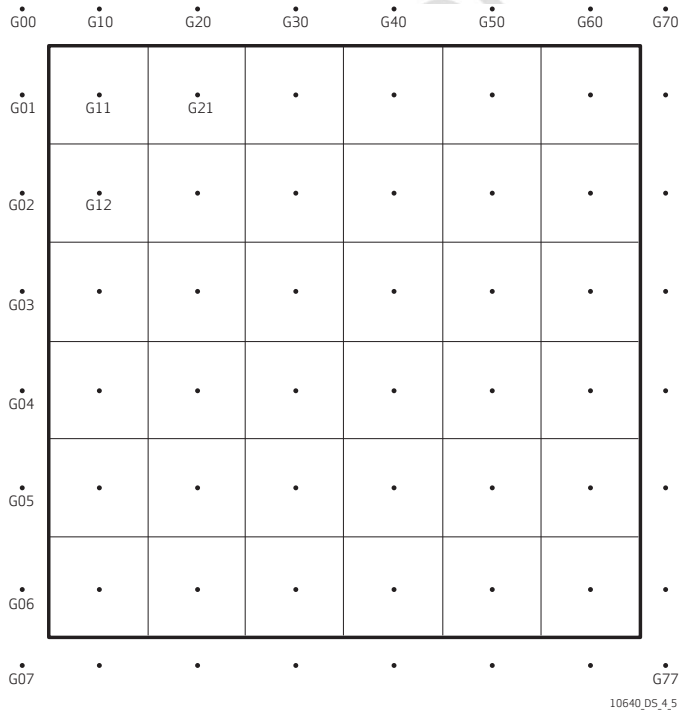
table 4-1 test pattern control registers

address	register name	default value	R/W	description
0x305E	ASP_REGA	0x16	RW	Bit[6]: Color bar overlay swap Bit[5]: Color bar overlay enable Bit[4:0]: Reserved
0x305F	ASP_REGB	0x18	RW	Bit[3:0]: Color bar intensity
0x3127	R_ISP_CTRL_0	0x7B	RW	Bit[6]: isp_crop_en (active high) ISP output window crop enable Bit[5]: hdr_dpc_en DPC enable Bit[4]: scip_en Simple interpolation enable Bit[3]: hdr_dns_en HDR RAW DNS enable Bit[2]: lenc_en LENC enable Bit[1]: awb_gain_en WB gain enable Bit[0]: isp_enable ISP enable
0x3129	R_PRE_CTRL0	0x00	RW	Bit[7]: test_mode_en Pre_ISP test mode enable Bit[6]: rolling_lines Pre_ISP rolling lines enable Bit[5]: transparent_mode Pre_ISP transparent mode enable Bit[4]: Reserved Bit[3:2]: color_bar Pre_ISP color bar style Bit[1:0]: img_sel Pre_ISP test image select

4.2 lens correction (LENC)

The first step in the image processing pipeline is to correct the shading due to light fall off in the edges and corner areas. The correction is done by multiplying each pixel with a gain based on the area where each pixel is located. The gain to apply is calculated from a 8x8 grid with control points for both luminance (G) and each color channel (B, R) separately. The control points are separated for LPD (L,VS) and SPD (S) (see registers 0x3296~0x3415). LENC is disabled by default and can be enabled by register 0x3127[2].

figure 4-5 LENC control points



The control points are selected according to the absolute coordinate of the input pixel in the sensor array. In other words, if y_offset and x_offset are bigger than 0 (0x3074~0x3077 values are bigger than 0), the control point (0,0) cannot be used, or if the image is flipped, control points will be selected from the back. The control points are located at the center of each sub-array and contain data on the lens artifacts in their respective locations in the pixel array.

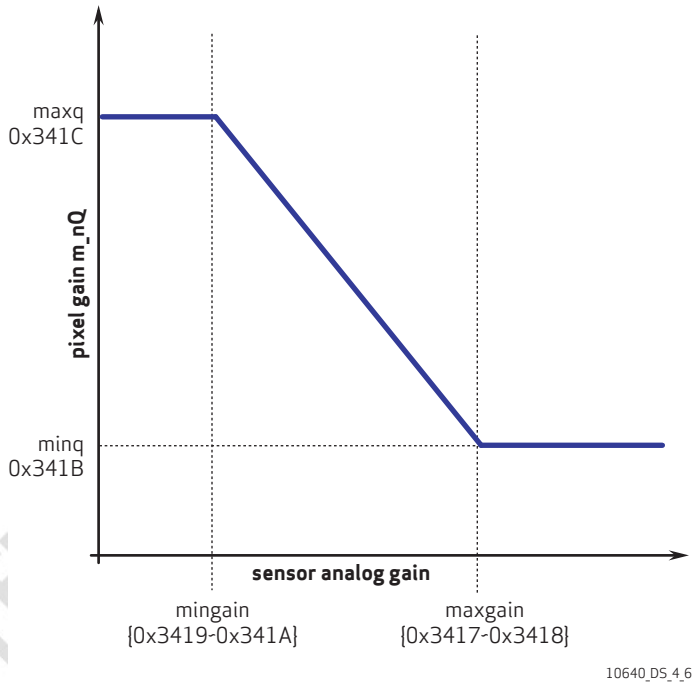
The OV10640 supports sub-sampling and flip in both horizontal and vertical directions while LENC is enabled.

The LENC control registers are separate for L, S and VS exposure. The following explanation is for L/VS.

Under dark conditions, the signal-to-noise ratio (SNR) drops in the corner areas. The noise can be significantly amplified by the lens correction gain and results in a brighter corner. The OV10640 can automatically adjust gain for the pixels to adapt to lighting conditions (m_nQ). This is accomplished by following the sensor analog gain and is enabled through register 0x3416[0] for LPD (enabled by default). If register 0x3416[0] is cleared, LENC gain will be fixed.

When scene brightness increases, the sensor analog gain decreases towards its minimum (mingain) and correspondingly, the LENC gain increases towards its maximum (maxq) (see **figure 4-6**). When scene brightness decreases, the sensor analog gain increases towards its maximum (maxgain) and the LENC gain decreases towards its minimum (minq).

figure 4-6 lens correction graph



Note that L/S/VS channels can share the same value of m_nQ calculated by L channel. The 8x8 control point matrix are, however, independent for L/VS (LPD) and S (SPD) channels, correspondingly.

By setting register 0x3416[3], the lens correction gain adjustments use the same luminance compensation level from L channel to apply on L,S and VS channels.

The luminance compensation levels used can be read from registers 0x342D~0x342F.

LENC control point parameters must be calibrated with a specific tool. Please contact your regional OmniVision FAE for assistance.

table 4-2 LENC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3416	LENC_CTRL10	0x0D	RW	Bit[3]: m_nq_option L/S/VS employ the same m_nq of L Bit[2]: less_1x_en_l (active high) Less than 1x gain enable for L/VS Bit[1]: rand_bit_en_l (active high) Add random enable for L/VS Bit[0]: auto_q_en_l (active high) Auto calculation Q enable for L/VS
0x3417	MAXGAIN_L_BYTE1	0x00	RW	Upper Gain Threshold for Auto Q for L/VS High Byte
0x3418	MAXGAIN_L_BYTE0	0x60	RW	Upper Gain Threshold for Auto Q for L/VS Low Byte
0x3419	MINGAIN_L_BYTE1	0x00	RW	Lower Gain Threshold for Auto Q for L/VS High Byte
0x341A	MINGAIN_L_BYTE0	0x20	RW	Lower Gain Threshold for Auto Q for L/VS Low Byte
0x341B	MINQ_L	0x18	RW	Minimum Q for Auto Q When Gain Larger Than Maxgain for L/VS
0x341C	MAXQ_L	0x40	RW	Maximum Q for Auto Q When Gain Smaller Than Mingain for L/VS
0x341D	BR_HSCALE_BYTE1	0x02	RW	H Scale for Blue/Red Channel, Same for All Exposures High Byte
0x341E	BR_HSCALE_BYTE0	0x0A	RW	H Scale for Blue/Red Channel, Same for All Exposures Low Byte
0x341F	BR_VSCALE_BYTE1	0x02	RW	V Scale for Blue/Red Channel, Same for All Exposures High Byte
0x3420	BR_VSCALE_BYTE0	0xF4	RW	V Scale for Blue/Red Channel, Same for All Exposures Low Byte
0x3421	G_HSCALE_BYTE1	0x02	RW	H Scale for Green Channel, Same for All Exposures High Byte
0x3422	G_HSCALE_BYTE0	0x0A	RW	H Scale for Green Channel, Same for All Exposures Low Byte
0x3423	G_VSCALE_BYTE1	0x01	RW	V Scale for Green Channel, Same for All Exposures High Byte
0x3424	G_VSCALE_BYTE0	0x0A	RW	V Scale for Green Channel, Same for All Exposures Low Byte

table 4-2 LENC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3425	LENC_CTRL11	0x05	RW	Bit[2]: less_1x_en_s (active high) Less than 1x gain enable for S Bit[1]: rand_bit_ en_s (active high) Add random enable for S Bit[0]: auto_q_en_s (active high) Auto calculation Q enable for S
0x3426	MAXGAIN_S_BYTE1	0x00	RW	Upper Gain Threshold for Auto Q for S High Byte
0x3427	MAXGAIN_S_BYTE0	0x60	RW	Upper Gain Threshold for Auto Q for S Low Byte
0x3428	MINGAIN_S_BYTE1	0x00	RW	Lower Gain Threshold for Auto Q for S High Byte
0x3429	MINGAIN_S_BYTE0	0x20	RW	Lower Gain Threshold for Auto Q for S Low Byte
0x342A	MINQ_S	0x18	RW	Minimum Q for Auto Q When Gain Larger Than Maxgain for S
0x342B	MAX_Q	0x40	RW	Maximum Q for Auto Q When Gain Larger Than Mingain for S

4.3 white balance gain (WB gain)

The next process in the pipeline is white balance. The RAW R, G and B values of a gray object vary with the light source spectrum and the pixel QE spectrum response. Light source spectrum is usually described by "color temperature", which is the surface temperature of a black body radiating equivalent spectrum. In the real world, the light color temperature ranges from very low (reddish) to very high (bluish) value. For example, the color temperature of an incandescent lamp is about 2850K, while the color temperature of an overcast day is about 6500K.

To make sure that a gray image is truly gray regardless of the light spectrum, the sensor needs to adjust the gain for each RGB channel according to color temperature. This process is called white balance (WB).

The OV10640 WB gain registers can be controlled by a separate ISP processor.

White balance gain is enabled/disabled in register 0x3127[1]. The applied WB gain can be read back from registers 0x31C3~0x31DA and offset values can be read back from registers 0x31D8~0x31FE.

table 4-3 WB control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x31C3	R_R_GAIN_L_I_H	0x01	RW	Gain for L Exposure Channel Red Component High Byte
0x31C4	R_R_GAIN_L_I_L	0x00	RW	Gain for L Exposure Channel Red Component Low Byte
0x31C5	R_GR_GAIN_L_I_H	0x01	RW	Gain for L Exposure Channel GreenR Component High Byte
0x31C6	R_GR_GAIN_L_I_L	0x00	RW	Gain for L Exposure Channel GreenR Component Low Byte
0x31C7	R_GB_GAIN_L_I_H	0x01	RW	Gain for L Exposure Channel GreenB Component High Byte
0x31C8	R_GB_GAIN_L_I_L	0x00	RW	Gain for L Exposure Channel GreenB Component Low Byte
0x31C9	R_B_GAIN_L_I_H	0x01	RW	Gain for L Exposure Channel Blue Component High Byte
0x31CA	R_B_GAIN_L_I_L	0x00	RW	Gain for L Exposure Channel Blue Component Low Byte
0x31CB	R_R_GAIN_S_I_H	0x01	RW	Gain for S Exposure Channel Red Component High Byte
0x31CC	R_R_GAIN_S_I_L	0x00	RW	Gain for S Exposure Channel Red Component Low Byte
0x31CD	R_GR_GAIN_S_I_H	0x01	RW	Gain for S Exposure Channel GreenR Component High Byte

table 4-3 WB control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x31CE	R_GR_GAIN_S_I_L	0x00	RW	Gain for S Exposure Channel GreenR Component Low Byte
0x31CF	R_GB_GAIN_S_I_H	0x01	RW	Gain for S Exposure Channel GreenB Component High Byte
0x31D0	R_GB_GAIN_S_I_L	0x00	RW	Gain for S Exposure Channel GreenB Component Low Byte
0x31D1	R_B_GAIN_S_I_H	0x01	RW	Gain for S Exposure Channel Blue Component High Byte
0x31D2	R_B_GAIN_S_I_L	0x00	RW	Gain for S Exposure Channel Blue Component Low Byte
0x31D3	R_R_GAIN_VS_I_H	0x01	RW	Gain for VS Exposure Channel Red Component High Byte
0x31D4	R_R_GAIN_VS_I_L	0x00	RW	Gain for VS Exposure Channel Red Component Low Byte
0x31D5	R_GR_GAIN_VS_I_H	0x01	RW	Gain for VS Exposure Channel GreenR Component High Byte
0x31D6	R_GR_GAIN_VS_I_L	0x00	RW	Gain for VS Exposure Channel GreenR Component Low Byte
0x31D7	R_GB_GAIN_VS_I_H	0x01	RW	Gain for VS Exposure Channel GreenB Component High Byte
0x31D8	R_GB_GAIN_VS_I_L	0x00	RW	Gain for VS Exposure Channel GreenB Component Low Byte
0x31D9	R_B_GAIN_VS_I_H	0x01	RW	Gain for VS Exposure Channel Blue Component High Byte
0x31DA	R_B_GAIN_VS_I_L	0x00	RW	Gain for VS Exposure Channel Blue Component Low Byte
0x31DB	R_R_OFFSET_L_I_H	0x00	RW	Offset for L Exposure Channel Red Component High Byte
0x31DC	R_R_OFFSET_L_I_M	0x00	RW	Offset for L Exposure Channel Red Component Middle Byte
0x31DD	R_R_OFFSET_L_I_L	0x00	RW	Offset for L Exposure Channel Red Component Low Byte
0x31DE	R_GR_OFFSET_L_I_H	0x00	RW	Offset for L Exposure Channel GreenR Component High Byte
0x31DF	R_GR_OFFSET_L_I_M	0x00	RW	Offset for L Exposure Channel GreenR Component Middle Byte
0x31E0	R_GR_OFFSET_L_I_L	0x00	RW	Offset for L Exposure Channel GreenR Component Low Byte

table 4-3 WB control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x31E1	R_GB_OFFSET_L_I_H	0x00	RW	Offset for L Exposure Channel GreenB Component High Byte
0x31E2	R_GB_OFFSET_L_I_M	0x00	RW	Offset for L Exposure Channel GreenB Component Middle Byte
0x31E3	R_GB_OFFSET_L_I_L	0x00	RW	Offset for L Exposure Channel GreenB Component Low Byte
0x31E4	R_B_OFFSET_L_I_H	0x00	RW	Offset for L Exposure Channel Blue Component High Byte
0x31E5	R_B_OFFSET_L_I_M	0x00	RW	Offset for L Exposure Channel Blue Component Middle Byte
0x31E6	R_B_OFFSET_L_I_L	0x00	RW	Offset for L Exposure Channel Blue Component Low Byte
0x31E7	R_R_OFFSET_S_I_H	0x00	RW	Offset for S Exposure Channel Red Component High Byte
0x31E8	R_R_OFFSET_S_I_M	0x00	RW	Offset for S Exposure Channel Red Component Middle Byte
0x31E9	R_R_OFFSET_S_I_L	0x00	RW	Offset for S Exposure Channel Red Component Low Byte
0x31EA	R_GR_OFFSET_S_I_H	0x00	RW	Offset for S Exposure Channel GreenR Component High Byte
0x31EB	R_GR_OFFSET_S_I_M	0x00	RW	Offset for S Exposure Channel GreenR Component Middle Byte
0x31EC	R_GR_OFFSET_S_I_L	0x00	RW	Offset for S Exposure Channel GreenR Component Low Byte
0x31ED	R_GB_OFFSET_S_I_H	0x00	RW	Offset for S Exposure Channel GreenB Component High Byte
0x31EE	R_GB_OFFSET_S_I_M	0x00	RW	Offset for S Exposure Channel GreenB Component Middle Byte
0x31EF	R_GB_OFFSET_S_I_L	0x00	RW	Offset for S Exposure Channel GreenB Component Low Byte
0x31F0	R_B_OFFSET_S_I_H	0x00	RW	Offset for S Exposure Channel Blue Component High Byte
0x31F1	R_B_OFFSET_S_I_M	0x00	RW	Offset for S Exposure Channel Blue Component Middle Byte
0x31F2	R_B_OFFSET_S_I_L	0x00	RW	Offset for S Exposure Channel Blue Component Low Byte
0x31F3	R_R_OFFSET_VS_I_H	0x00	RW	Offset for VS Exposure Channel Red Component High Byte

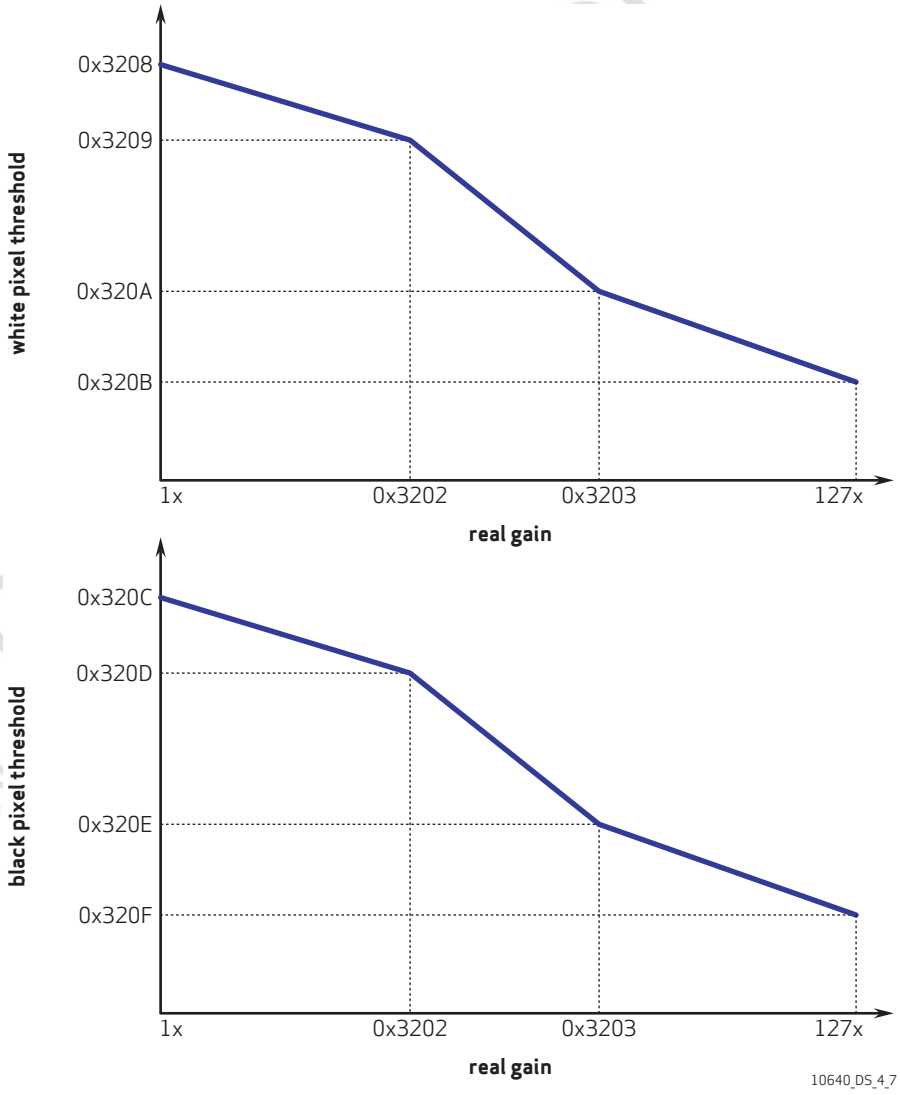
table 4-3 WB control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x31F4	R_R_OFFSET_VS_I_M	0x00	RW	Offset for VS Exposure Channel Red Component Middle Byte
0x31F5	R_R_OFFSET_VS_I_L	0x00	RW	Offset for VS Exposure Channel Red Component Low Byte
0x31F6	R_GR_OFFSET_VS_I_H	0x00	RW	Offset for VS Exposure Channel GreenR Component High Byte
0x31F7	R_GR_OFFSET_VS_I_M	0x00	RW	Offset for VS Exposure Channel GreenR Component Middle Byte
0x31F8	R_GR_OFFSET_VS_I_L	0x00	RW	Offset for VS Exposure Channel GreenR Component Low Byte
0x31F9	R_GB_OFFSET_VS_I_H	0x00	RW	Offset for VS Exposure Channel GreenB Component High Byte
0x31FA	R_GB_OFFSET_VS_I_M	0x00	RW	Offset for VS Exposure Channel GreenB Component Middle Byte
0x31FB	R_GB_OFFSET_VS_I_L	0x00	RW	Offset for VS Exposure Channel GreenB Component Low Byte
0x31FC	R_B_OFFSET_VS_I_H	0x00	RW	Offset for VS Exposure Channel Blue Component High Byte
0x31FD	R_B_OFFSET_VS_I_M	0x00	RW	Offset for VS Exposure Channel Blue Component Middle Byte
0x31FE	R_B_OFFSET_VS_I_L	0x00	RW	Offset for VS Exposure Channel Blue Component Low Byte

4.4 defect pixel correction (DPC)

The DPC function detects defect pixels/cluster by using a programmable threshold. The threshold can be automatically calculated based on real (analog gain × digital gain) from a programmable threshold gain curve or set manually by register 0x31FF[0]. Refer to **figure 4-7** for details, where the "channel" means L, S or VS channel. In the OV10640, DPC cannot be enabled/disabled (0x3127[5]) independently for L/S/VS exposure channels. All settings, such as white/black defect pixel process, can be set individually per exposure channel.

figure 4-7 threshold gain curve in auto threshold mode



The DPC can correct single defect pixels, couplets, cross types and tail types. The following figures illustrate defect patterns that can be detected. Refer to registers 0x31FF~0x3267 for more detailed information about DPC configuration.

figure 4-8 white defects

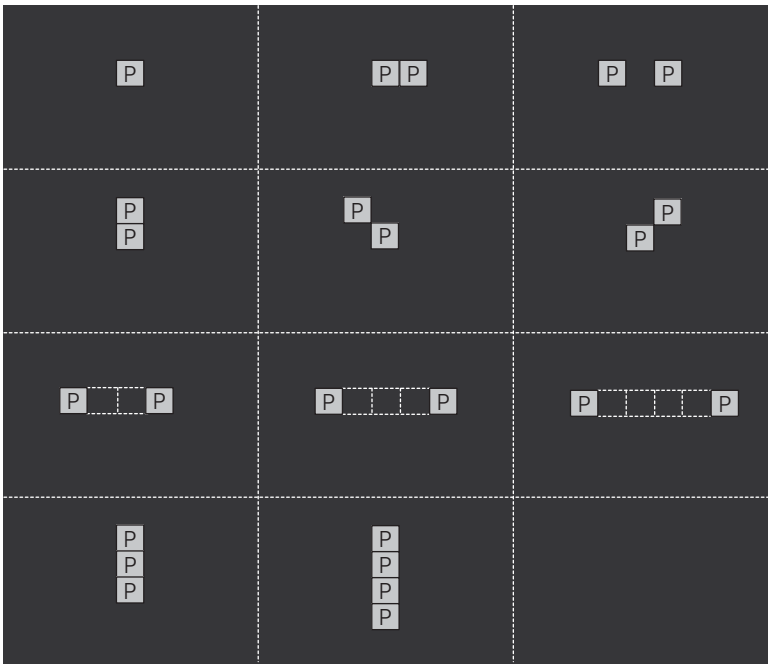


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figure 4-9 black defects

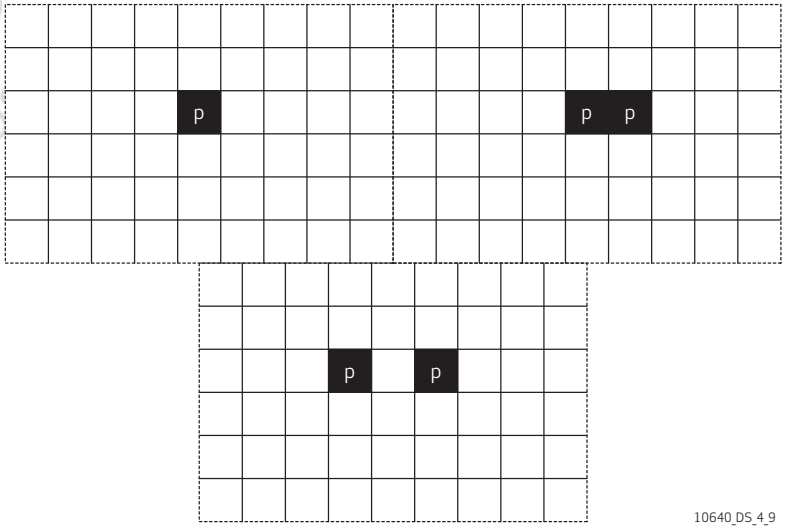

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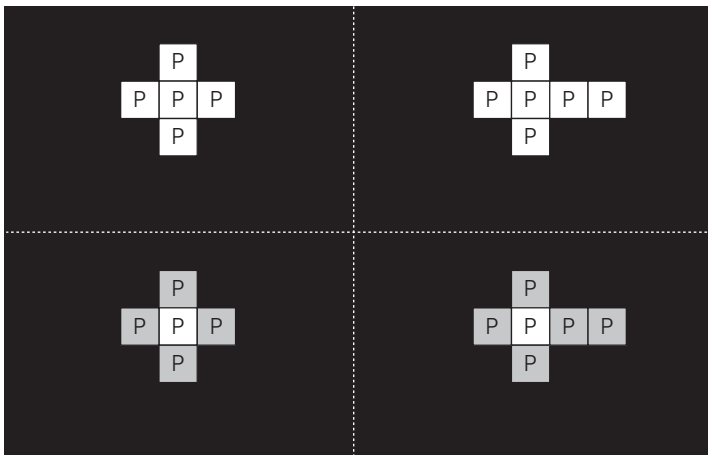
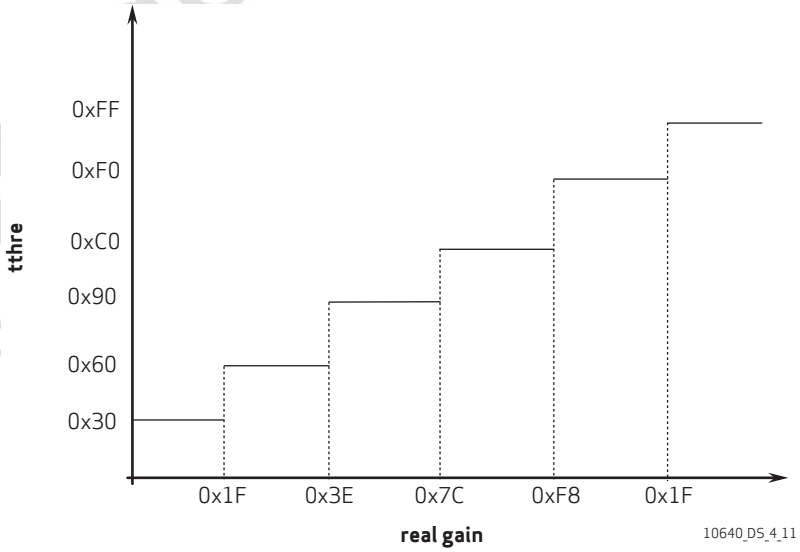
figure 4-10 cross and cross-tail



Threshold for T-cluster can be manually set (register 0x3200[7]) or changed automatically according to real gain (see **figure 4-11**).

figure 4-11 threshold for T-cluster diagram



If vertical black pixel detection is enabled (register 0x3200[5]), it is automatically activated by the relationship between sensor real gain and thresholds set by registers 0x3211 and 0x3212.

- activated if ({0x3211}+1)×16 is less than sensor real gain
- deactivated if ({0x3212}+1)×16 higher than sensor real gain

table 4-4 DPC control registers (sheet 1 of 12)

address	register name	default value	R/W	description
0x31FF	R_L_DPC_CTRL00	0x18	RW	For Long Exposure Channel Bit[7]: Tail type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: Saturation type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[5]: Cross cluster correction enable Bit[4]: Horizontal same color plane couplet correction enable 0: Disable 1: Enable Bit[3]: Horizontal couplet correction enable 0: Disable 1: Enable Bit[1]: r_bwsnr_en Bit[0]: Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on the analog gain 1: Manual mode in which defect pixel threshold is set manually by register

table 4-4 DPC control registers (sheet 2 of 12)

address	register name	default value	R/W	description
0x3200	R_L_DPC_CTRL01	0xDF	RW	For Long Exposure Channel Bit[7]: Set threshold for T-cluster 0: Automatically 1: Manually Bit[6]: r_comp_en Bit[5]: Vertical black pixel detection 0: Disable 1: Enable Bit[4]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[3]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable Bit[2]: T-cluster detection 0: Disable 1: Enable Bit[1:0]: Padding method of edge pixels 00: Pad with 0 01: Pad with 255 10: Pad with (255+1)/2 11: Pad with nearby same channel pixel This option will affect defect pixel detection of boundary pixels
0x3201	R_L_DPC_CTRL02	0xFF	RW	For Long Exposure Channel Bit[7]: White defect pixel detection 0: Disable 1: Enable Bit[6]: Black defect pixel detection 0: Disable 1: Enable Bit[5:4]: Pixel number threshold for detection of cross-cluster Bit[3:2]: Pixel number threshold for detection of T-cluster Bit[1:0]: Number of vertical connected white pixels removed 00: Remove the upper one white pixel 01: Remove two vertical white pixels 10: Remove three or less vertical connected white pixel

table 4-4 DPC control registers (sheet 3 of 12)

address	register name	default value	R/W	description
0x3202	R_L_WTHREGLIST1	0x08	RW	For Long Exposure Channel Bit[6:0]: Threshold value for detecting white pixel in manual. More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x3203	R_L_WTHREGLIST2	0x20	RW	For Long Exposure Channel Bit[6:0]: Threshold value for detecting black pixel in manual mode. More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x3204	R_L_THRE1	0x10	RW	For Long Exposure Channel Bit[6:0]: Threshold value used in recovery of defect pixel for long channel. The bigger the value, the more details retained, but the less effective of recovering defect
0x3205	R_L_THRE2	0x20	RW	For Long Exposure Channel Bit[6:0]: Threshold for registering defect pixel to detect cross cluster for long channel. The greater the threshold, the more defect pixels will be removed
0x3206	R_L_THRE3	0x10	RW	For Long Exposure Channel Bit[7:0]: Threshold to determine high frequency area where the DPC will keep the fine details for long channel. The greater the threshold, the more details will be removed by DPC
0x3207	R_L_THRE4	0x18	RW	For Long Exposure Channel Bit[6:0]: Threshold for detecting horizontal couplet for long channel. This threshold should be greater than the threshold for single white/black pixel
0x3208	R_L_WTHRE_LIST0	0x08	RW	For Long Exposure Channel Bit[6:0]: White pixel threshold 0 in auto mode

table 4-4 DPC control registers (sheet 4 of 12)

address	register name	default value	R/W	description
0x3209	R_L_WTHRE_LIST1	0x04	RW	For Long Exposure Channel Bit[6:0]: White pixel threshold 1 in auto mode
0x320A	R_L_WTHRE_LIST2	0x02	RW	For Long Exposure Channel Bit[6:0]: White pixel threshold 2 in auto mode
0x320B	R_L_WTHRE_LIST3	0x02	RW	For Long Exposure Channel Bit[6:0]: White pixel threshold 3 in auto mode
0x320C	R_L_BTHRE_LIST0	0x0C	RW	For Long Exposure Channel Bit[6:0]: Black pixel threshold 0 in auto mode
0x320D	R_L_BTHRE_LIST1	0x06	RW	For Long Exposure Channel Bit[6:0]: Black pixel threshold 1 in auto mode
0x320E	R_L_BTHRE_LIST2	0x02	RW	For Long Exposure Channel Bit[6:0]: Black pixel threshold 2 in auto mode
0x320F	R_L_BTHRE_LIST3	0x02	RW	For Long Exposure Channel Bit[6:0]: Black pixel threshold 3 in auto mode
0x3210	R_L_SAT	0xFF	RW	For Long Exposure Channel Bit[7:0]: Threshold of the center pixel for saturation type of cross cluster. To qualify a saturation type of cross cluster, the center pixel must be greater than this threshold
0x3211	R_L_VB_GAIN TH1	0x07	RW	For Long Exposure Channel Bit[6:0]: Vertical black pixel detection threshold 1
0x3212	R_L_VB_GAIN_TH2	0x03	RW	For Long Exposure Channel Bit[6:0]: Vertical black pixel detection threshold 2
0x3213	R_L_SMOOTH_GLIST0	0x03	RW	For Long Exposure Channel Bit[6:0]: Smooth gain list 0
0x3214	R_L_SMOOTH_GLIST1	0x07	RW	For Long Exposure Channel Bit[6:0]: Smooth gain list 1
0x3215	R_L_SMOOTH_GLIST2	0x0F	RW	For Long Exposure Channel Bit[6:0]: Smooth gain list 2

table 4-4 DPC control registers (sheet 5 of 12)

address	register name	default value	R/W	description
0x3216~ 0x3217	NOT USED	–	–	Not Used
0x3218	R_L_UNSAT	0xF0	RW	For Long Exposure Channel Bit[7:0]: Threshold of un-saturation level for detection of cross-cluster and T-cluster
0x3219	R_L_TTHRE	0x08	RW	For Long Exposure Channel Bit[7:0]: Threshold to determine a cross-cluster and T-cluster
0x321A	R_S_DPC_CTRL00	0x18	RW	For Short Exposure Channel Bit[7]: Tail type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: Saturation type cross cluster correction enable, works only when cross cluster correction is 0: Disable 1: Enable Bit[5]: Cross cluster correction enable Bit[4]: Horizontal same color plane couplet correction enable 0: Disable 1: Enable Bit[3]: Horizontal couplet correction enable 0: Disable 1: Enable Bit[1]: r_bwsnr_en Bit[0]: Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on the analog gain 1: Manual mode in which defect pixel threshold is set manually by register

table 4-4 DPC control registers (sheet 6 of 12)

address	register name	default value	R/W	description
0x321B	R_S_DPC_CTRL01	0xDF	RW	For Long Exposure Channel Bit[7]: Set threshold for T-cluster 0: Automatically 1: Manually Bit[6]: r_comp_en Bit[5]: Vertical black pixel detection 0: Disable 1: Enable Bit[4]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[3]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable Bit[2]: T-cluster detection 0: Disable 1: Enable Bit[1:0]: Padding method of edge pixels 00: Pad with 0 01: Pad with 255 10: Pad with (255+1)/2 11: Pad with nearby same channel pixel This option will affect defect pixel detection of boundary pixels
0x321C	R_S_DPC_CTRL02	0xFF	RW	For Short Exposure Channel Bit[7]: White defect pixel detection 0: Disable 1: Enable Bit[6]: Black defect pixel detection 0: Disable 1: Enable Bit[5:4]: Pixel number threshold for detection of cross-cluster Bit[3:2]: Pixel number threshold for detection of T-cluster Bit[1:0]: Number of vertical connected white pixels removed 00: Remove the upper one white pixel 01: Remove two vertical white pixels 10: Remove three or less vertical connected white pixel

table 4-4 DPC control registers (sheet 7 of 12)

address	register name	default value	R/W	description
0x321D	R_S_WTHREGLIST1	0x08	RW	For Short Exposure Channel Bit[6:0]: Threshold value for detecting white pixel in manual. More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x321E	R_S_WTHREGLIST2	0x20	RW	For Short Exposure Channel Bit[6:0]: Threshold value for detecting black pixel in manual mode. More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x321F	R_S_THRE1	0x10	RW	For Short Exposure Channel Bit[6:0]: Threshold value used in recovery of defect pixel for long channel. The bigger the value, the more details retained, but the less effective of recovering defect
0x3220	R_S_THRE2	0x20	RW	For Short Exposure Channel Bit[6:0]: Threshold for registering defect pixel to detect cross cluster for long channel. The greater the threshold, the more defect pixels will be removed
0x3221	R_S_THRE3	0x10	RW	For Short Exposure Channel Bit[7:0]: Threshold to determine high frequency area where the DPC will keep the fine details for long channel. The greater the threshold, the more details will be removed by DPC
0x3222	R_S_THRE4	0x18	RW	For Short Exposure Channel Bit[6:0]: Threshold for detecting horizontal couplet for long channel. This threshold should be greater than the threshold for single while/black pixel
0x3223	R_S_WTHRE_LIST0	0x08	RW	For Short Exposure Channel Bit[6:0]: White pixel threshold 0 in auto mode

table 4-4 DPC control registers (sheet 8 of 12)

address	register name	default value	R/W	description
0x3224	R_S_WTHRE_LIST1	0x04	RW	For Short Exposure Channel Bit[6:0]: White pixel threshold 1 in auto mode
0x3225	R_S_WTHRE_LIST2	0x02	RW	For Short Exposure Channel Bit[6:0]: White pixel threshold 2 in auto mode
0x3226	R_S_WTHRE_LIST3	0x02	RW	For Short Exposure Channel Bit[6:0]: White pixel threshold 3 in auto mode
0x3227	R_S_BTHRE_LIST0	0x0C	RW	For Short Exposure Channel Bit[6:0]: Black pixel threshold 0 in auto mode
0x3228	R_S_BTHRE_LIST1	0x06	RW	For Short Exposure Channel Bit[6:0]: Black pixel threshold 1 in auto mode
0x3229	R_S_BTHRE_LIST2	0x02	RW	For Short Exposure Channel Bit[6:0]: Black pixel threshold 2 in auto mode
0x322A	R_S_BTHRE_LIST3	0x02	RW	For Short Exposure Channel Bit[6:0]: Black pixel threshold 3 in auto mode
0x322B	R_S_SAT	0xFF	RW	For Short Exposure Channel Bit[7:0]: Threshold of the center pixel for saturation type of cross cluster. To qualify a saturation type of cross cluster, the center pixel must be greater than this threshold
0x322C	R_S_VB_GAIN_TH1	0x07	RW	For Short Exposure Channel Bit[6:0]: Vertical black pixel detection threshold 1
0x322D	R_S_VB_GAIN_TH2	0x03	RW	For Short Exposure Channel Bit[6:0]: Vertical black pixel detection threshold 2
0x322E	R_S_SMOOTH_GLIST0	0x03	RW	For Short Exposure Channel Bit[6:0]: Smooth gain list 0
0x322F	R_S_SMOOTH_GLIST1	0x07	RW	For Short Exposure Channel Bit[6:0]: Smooth gain list 1
0x3230	R_S_SMOOTH_GLIST2	0x0F	RW	For Short Exposure Channel Bit[6:0]: Smooth gain list 2

table 4-4 DPC control registers (sheet 9 of 12)

address	register name	default value	R/W	description
0x3231~ 0x3232	NOT USED	–	–	Not Used
0x3233	R_S_UNSAT	0xF0	RW	For Short Exposure Channel Bit[7:0]: Threshold of un-saturation level for detection of cross-cluster and T-cluster
0x3234	R_S_TTHRE	0x08	RW	For Short Exposure Channel Bit[7:0]: Threshold to determine a cross-cluster and T-cluster
0x3235	R_VS_DPC_CTRL00	0x18	RW	For Very Short Exposure Channel Bit[7]: Tail type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: Saturation type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[5]: Cross cluster correction enable Bit[4]: Horizontal same color plane couplet correction enable 0: Disable 1: Enable Bit[3]: Horizontal couplet correction enable 0: Disable 1: Enable Bit[1]: r_bwsnr_en Bit[0]: Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on the analog gain 1: Manual mode in which defect pixel threshold is set manually by register

table 4-4 DPC control registers (sheet 10 of 12)

address	register name	default value	R/W	description
0x3236	R_VS_DPC_CTRL01	0xDF	RW	For Very Short Exposure Channel Bit[7]: Manually set threshold for T-cluster Bit[6]: r_comp_en Bit[5]: Vertical black pixel detection 0: Disable 1: Enable Bit[4]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[3]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable Bit[2]: T-cluster detection 0: Disable 1: Enable Bit[1:0]: Padding method of edge pixels 00: Pad with 0 01: Pad with 255 10: Pad with (255+1)/2 11: Pad with nearby same channel pixel This option will affect defect pixel detection of boundary pixels
0x3237	R_VS_DPC_CTRL02	0xFF	RW	For Very Short Exposure Channel Bit[7]: White defect pixel detection 0: Disable 1: Enable Bit[6]: Black defect pixel detection 0: Disable 1: Enable Bit[5:4]: Pixel number threshold for detection of cross-cluster Bit[3:2]: Pixel number threshold for detection of T-cluster Bit[1:0]: Number of vertical connected white pixels removed 00: Remove the upper one white pixel 01: Remove two vertical white pixels 10: Remove three or less vertical connected white pixel

table 4-4 DPC control registers (sheet 11 of 12)

address	register name	default value	R/W	description
0x3238	R_VS_WTHREGLIST1	0x08	RW	For Very Short Exposure Channel Bit[6:0]: Threshold value for detecting white pixel in manual. More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x3239	R_VS_WTHREGLIST2	0x20	RW	For Very Short Exposure Channel Bit[6:0]: Threshold value for detecting black pixel in manual mode. More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x323A	R_VS_THRE1	0x10	RW	For Very Short Exposure Channel Bit[6:0]: Threshold value used in recovery of defect pixel for long channel. The bigger the value, the more details retained, but the less effective of recovering defect
0x323B	R_VS_THRE2	0x20	RW	For Very Short Exposure Channel Bit[6:0]: Threshold for registering defect pixel to detect cross cluster for long channel. The greater the threshold, the more defect pixels will be removed
0x323C	R_VS_THRE3	0x10	RW	For Very Short Exposure Channel Bit[7:0]: Threshold to determine high frequency area where the DPC will keep the fine details for long channel. The greater the threshold, the more details will be removed by DPC
0x323D	R_VS_THRE4	0x18	RW	For Very Short Exposure Channel Bit[6:0]: Threshold for detecting horizontal couplet for long channel. This threshold should be greater than the threshold for single while/black pixel
0x323E	R_VS_WTHRE_LIST0	0x08	RW	For Very Short Exposure Channel Bit[6:0]: White pixel threshold 0 in auto mode

table 4-4 DPC control registers (sheet 12 of 12)

address	register name	default value	R/W	description
0x323F	R_VS_WTHRE_LIST1	0x04	RW	For Very Short Exposure Channel Bit[6:0]: White pixel threshold 1 in auto mode
0x3240	R_VS_WTHRE_LIST2	0x02	RW	For Very Short Exposure Channel Bit[6:0]: White pixel threshold 2 in auto mode
0x3241	R_VS_WTHRE_LIST3	0x02	RW	For Very Short Exposure Channel Bit[6:0]: White pixel threshold 3 in auto mode
0x3242	R_VS_SAT	0xFF	RW	For Very Short Exposure Channel Bit[7:0]: Threshold of the center pixel for saturation type of cross cluster. To qualify a saturation type of cross cluster, the center pixel must be greater than this threshold
0x3243	R_VS_VB_GAIN_TH1	0x07	RW	For Very Short Exposure Channel Bit[6:0]: Vertical black pixel detection threshold 1
0x3244	R_VS_VB_GAIN_TH2	0x03	RW	For Very Short Exposure Channel Bit[6:0]: Vertical black pixel detection threshold 2
0x3245	R_VS_SMOOTH_GLIST0	0x03	RW	For Very Short Exposure Channel Bit[6:0]: Smooth gain list 0
0x3246	R_VS_SMOOTH_GLIST1	0x07	RW	For Very Short Exposure Channel Bit[6:0]: Smooth gain list 1
0x3247	R_VS_SMOOTH_GLIST2	0x0F	RW	For Very Short Exposure Channel Bit[6:0]: Smooth gain list 2
0x3248~ 0x3249	NOT USED	–	–	Not Used
0x324A	R_VS_UNSAT	0xF0	RW	For Very Short Exposure Channel Bit[7:0]: Threshold of un-saturation level for detection of cross-cluster and T-cluster
0x324B	R_VS_TTHRE	0x08	RW	For Very Short Exposure Channel Bit[7:0]: Threshold to determine a cross-cluster and T-cluster
0x324C~ 0x3267	RSVD	–	–	Reserved

4.5 HDR RAW de-noise (HDR RAW DNS)

RAWDNS will reduce noise in R/B channels before color interpolation, since WB gain may amplify the noise in R/B channels. It also supports noise reduction in green channel, but must be carefully applied as not remove too much detail, which may cause blurry images.

4.5.1 RAW DNS noise list

Noise level increases with sensor AGC gain, so DNS modules will also need to increase de-noise level with gain. DNS, an 8-step noise list, which defines the de-noise level, will be used when the sensor AGC gain is x1, x2, x4, x8, x16, x32, x64 or x128 (0x3268~0x326F for L). If the AGC gain is between two steps, the real de-noise level will be linearly interpolated between two steps.

4.5.2 RAWDNS configuration

In RAWDNS, except for the noise list, there are three parameters, which can influence image quality.

- green channel de-noising
  An option for choosing G position pixels to be involved in de-noise is enabled by registers 0x3270, 0x327B, and 0x3286 for L, S and VS, respectively. Note that enabling the green channel de-noising may remove image details and result in a blurry image. Unless the sensor noise level is very high, it is recommended to disable green channel de-noising.
- noise Y slop signal
  An option to increase the DNS level with the signal level is adjusted by registers 0x3271, 0x327C and 0x3287 for L, S and VS, respectively. In the linear domain, shot noise increases with signal level, so for a linear raw image, the dark tone has lower noise level than mid tone and light tone. A larger value will reduce more noise in light tone.
- maximum edge threshold
  An option to preserve color edges in low light conditions is adjusted by registers 0x3272, 0x327D and 0x3288 for L, S and VS, respectively. A smaller value will preserve color edges, but will also remove less noise in R/B channels.

table 4-5 HDR_RAW control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3268	R_NOISELIST0_L_I	0x04	RW	NoiseList0 for L Exposure Channel RAW Denoise
0x3269	R_NOISELIST1_L_I	0x08	RW	NoiseList1 for L Exposure Channel RAW Denoise
0x326A	R_NOISELIST2_L_I	0x10	RW	NoiseList2 for L Exposure Channel RAW Denoise
0x326B	R_NOISELIST3_L_I	0x18	RW	NoiseList3 for L Exposure Channel RAW Denoise
0x326C	R_NOISELIST4_L_I	0x20	RW	NoiseList4 for L Exposure Channel RAW Denoise

table 4-5 HDR_RAW control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x326D	R_NOISELIST5_L_I	0x30	RW	NoiseList5 for L Exposure Channel RAW Denoise
0x326E	R_NOISELIST6_L_I	0x40	RW	NoiseList6 for L Exposure Channel RAW Denoise
0x326F	R_NOISELIST7_L_I	0x40	RW	NoiseList7 for L Exposure Channel RAW Denoise
0x3270	R_G_DNS_EN_L_I	0x00	RW	Enable for Choosing G Position Pixels to be Involved in Denoise
0x3271	R_NOISE_YSLOP_L_I	0x04	RW	Noise YSlope Signal for L Exposure Channel Noise Calculation
0x3272	R_MAX_EDGE_THRE _L_I	0x3F	RW	Maximum Edge Threshold for L Exposure Channel Noise Calculation
0x3273	R_NOISELIST0_S_I	0x04	RW	NoiseList0 for S Exposure Channel RAW Denoise
0x3274	R_NOISELIST1_S_I	0x08	RW	NoiseList1 for S Exposure Channel RAW Denoise
0x3275	R_NOISELIST2_S_I	0x10	RW	NoiseList2 for S Exposure Channel RAW Denoise
0x3276	R_NOISELIST3_S_I	0x18	RW	NoiseList3 for S Exposure Channel RAW Denoise
0x3277	R_NOISELIST4_S_I	0x20	RW	NoiseList4 for S Exposure Channel RAW Denoise
0x3278	R_NOISELIST5_S_I	0x30	RW	NoiseList5 for S Exposure Channel RAW Denoise
0x3279	R_NOISELIST6_S_I	0x40	RW	NoiseList6 for S Exposure Channel RAW Denoise
0x327A	R_NOISELIST7_S_I	0x40	RW	NoiseList7 for S Exposure Channel RAW Denoise
0x327B	R_G_DNS_EN_S_I	0x00	RW	Enable for Choosing G Position Pixels to be Involved in Denoise
0x327C	R_NOISE_YSLOP_S_I	0x04	RW	Noise YSlope Signal for S Exposure Channel Noise Calculation
0x327D	R_MAX_EDGE_THRE _S_I	0x3F	RW	Maximum Edge Threshold for S Exposure Channel Noise Calculation
0x327E	R_NOISELIST0_V_I	0x04	RW	NoiseList0 for VS Exposure Channel RAW Denoise
0x327F	R_NOISELIST1_V_I	0x08	RW	NoiseList1 for VS Exposure Channel RAW Denoise

table 4-5 HDR_RAW control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3280	R_NOISELIST2_V_I	0x10	RW	NoiseList2 for VS Exposure Channel RAW Denoise
0x3281	R_NOISELIST3_V_I	0x18	RW	NoiseList3 for VS Exposure Channel RAW Denoise
0x3282	R_NOISELIST4_V_I	0x20	RW	NoiseList4 for VS Exposure Channel RAW Denoise
0x3283	R_NOISELIST5_V_I	0x30	RW	NoiseList5 for VS Exposure Channel RAW Denoise
0x3284	R_NOISELIST6_V_I	0x40	RW	NoiseList6 for VS Exposure Channel RAW Denoise
0x3285	R_NOISELIST7_V_I	0x40	RW	NoiseList7 for VS Exposure Channel RAW Denoise
0x3286	R_G_DNS_EN_V_I	0x00	RW	Enable for Choosing G Position Pixels to be Involved in Denoise
0x3287	R_NOISE_YSLOP_V_I	0x04	RW	Noise YSlope Signal for VS Exposure Channel Noise Calculation
0x3288	R_MAX_EDGE_THRE _V_I	0x3F	RW	Maximum Edge Threshold for VS Exposure Channel Noise Calculation

4.6 combine

The combine module will combine the L, S and VS channels to a single exposure channel with extended bit depth. Combine is automatically selected when enabling 20,16, or 12 comb in register 0x3119[2:0].

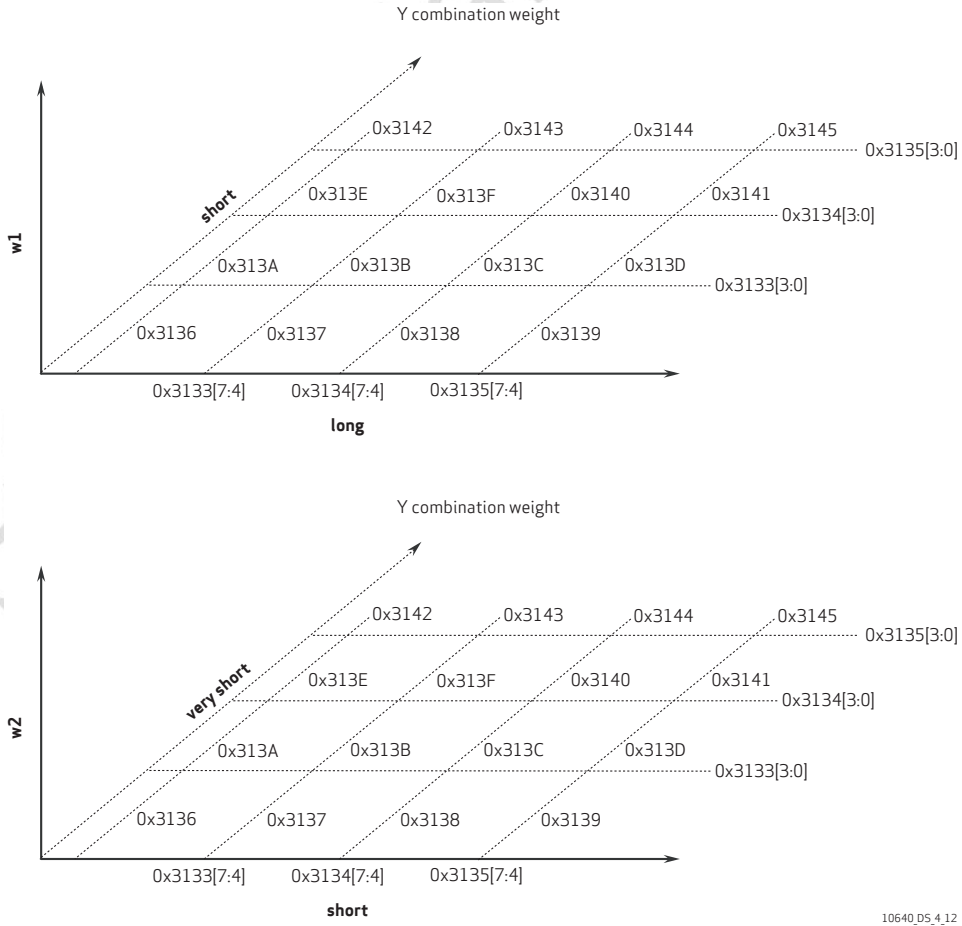
To prepare data for HDR processing, sensor RAW data is converted from Bayer pattern to RGBY format in a simple color interpolation procedure (simple CIP).

Y is calculated from BGR:

Y = (B+G×2+R)>>2

The combination is a combined weighted average of long, short and very short input. A linear blending method is used to combine the two exposures in the overlap range.

figure 4-12 combine graph diagram



The blending weight, w, is a 2D curve determined by the luminance of long, short and very short exposure channels. If the weight value is 0x80, it indicates w=1.

Three exposure mode:

$Y_C = Y_L \times W_1 + Y_S \times (1-W_1) \times W_2 + Y_{VS} \times (1-W_1)(1-W_2)$

W_1 is the weight between L and S

W_2 is the weight between S and VS

Y denotes the luminance data

The weighting varies from pixel to pixel and W1 and W2 is interpolated from a look up table. The two channels with the best SNR are combined for each pixel. So, the combination is either between L and S, or S and VS.

In order to cancel QE difference between long and short pixel, a color matrix correction may be applied to S channel before combination using register 0x3132[3].

table 4-6 combine control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3132	R_COMBINE_CTRL	0x3C	RW	Bit[7:5]: n_step Bit[4]: auto_ct_enable Bit[3]: S channel pre matrix enable Bit[2]: Compensate error enable Bit[1:0]: Combine work mode 00: HDRCombine enable 01: Not used 1x: Not used
0x3133	R_COMBINE_THRE_0	0x95	RW	Combine Threshold [0] Bit[7:4]: Long Bit[3:0]: Short
0x3134	R_COMBINE_THRE_1	0xA8	RW	Combine Threshold [1] Bit[7:4]: Long Bit[3:0]: Short
0x3135	R_COMBINE_THRE_2	0xAA	RW	Combine Threshold [2] Bit[7:4]: Long Bit[3:0]: Short
0x3136	R_COMBINE_WEIGHT_0_0	0x80	RW	Combine Weight [0][0]
0x3137	R_COMBINE_WEIGHT_0_1	0x80	RW	Combine Weight [0][1]
0x3138	R_COMBINE_WEIGHT_0_2	0x60	RW	Combine Weight [0][2]
0x3139	R_COMBINE_WEIGHT_0_3	0x40	RW	Combine Weight [0][3]
0x313A	R_COMBINE_WEIGHT_1_0	0x80	RW	Combine Weight [1][0]
0x313B	R_COMBINE_WEIGHT_1_1	0x80	RW	Combine Weight [1][1]

table 4-6 combine control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x313C	R_COMBINE_WEIGHT_1_2	0x40	RW	Combine Weight [1][2]
0x313D	R_COMBINE_WEIGHT_1_3	0x20	RW	Combine Weight [1][3]
0x313E	R_COMBINE_WEIGHT_2_0	0x80	RW	Combine Weight [2][0]
0x313F	R_COMBINE_WEIGHT_2_1	0x60	RW	Combine Weight [2][1]
0x3140	R_COMBINE_WEIGHT_2_2	0x00	RW	Combine Weight [2][2]
0x3141	R_COMBINE_WEIGHT_2_3	0x00	RW	Combine Weight [2][3]
0x3142	R_COMBINE_WEIGHT_3_0	0x80	RW	Combine Weight [3][0]
0x3143	R_COMBINE_WEIGHT_3_1	0x80	RW	Combine Weight [3][1]
0x3144	R_COMBINE_WEIGHT_3_2	0x00	RW	Combine Weight [3][2]
0x3145	R_COMBINE_WEIGHT_3_3	0x00	RW	Combine Weight [3][3]
0x3146	R_COMB_ERROR_CTRL_B2	0x02	RW	r_comb_error_ctrl High Byte
0x3147	R_COMB_ERROR_CTRL_B1	0x00	RW	r_comb_error_ctrl Middle Byte
0x3148	R_COMB_ERROR_CTRL_B0	0x00	RW	r_comb_error_ctrl Low Byte
0x3149	R_TRAFFIC_S_TH_H	0x28	RW	Traffic S Threshold High Byte
0x314A	NOT USED	–	–	Not Used
0x314B	R_TH_S_0H	0x10	RW	m_nThS[0] High Byte
0x314C	R_TH_S_0_L	0x00	RW	m_nThS[0] Low Byte
0x314D	R_TH_S_1_H	0x10	RW	m_nThS[1] High Byte
0x314E	R_TH_S_1_L	0x00	RW	m_nThS[1] Low Byte
0x314F	R_THS_DINV	0x20	RW	m_nThSDinv Equal to (2^16)/(m nThS[1]-m nThS[0])
0x3150	RSVD	–	–	Reserved

4.7 global tone mapping

The OV10640 is a high dynamic range (HDR) sensor, which combines three 12-bit captures with different sensitivities into one 20-bit linear output image. To reduce output data rate, a reversible tone mapping/compression function is provided to convert 20-bit values into 12 bits with minimum loss in signal/noise. The correct data output width must be selected in register 0x3119[2:0] for the 12 bit combined mode.

The piecewise linear (PWL) module is used to compress the 20-bit combined linear raw/Y to 12 bit linear raw/Y. A compress curve is used for the bit-convert.The 20bit-to-12bit mapping function is a PWL function with three knee-points defined in following section.

4.7.1 20b-to-12b mapping function

PV_20b: 20-bit linear pixel value (0...2^20-1),

PV_12b: 12-bit piecewise linear pixel value (0...2^14-1)

PV_20b ≤ 2^11	=> PV_12b = PV_20b/4	
2^11 ≤ PV_20b ≤ 2^14	=> PV_12b = (PV_20b+2^12+2^11) /16	(first knee-point)
2^14 ≤ PV_20b ≤ 2^16	=> PV_12b = (PV_20b+2^16+2^13) /64	(second knee-point)
2^16 ≤ PV_20b	=> PV_12b = (PV_20b+2^20) / 512	(third knee-point)

4.7.2 12b-to-20b mapping function

PV_12b ≤ 2^9	=> PV_20b = 4×PV_12b
2^9 ≤ PV_12b ≤ (2^14+2^12+2^11)/16	=> PV_20b = 16×PV_12B - 2^12 - 2^11
(2^14+2^12+2^11)/16 ≤ PV_12b ≤ (2^17+2^13)/64	=> PV_20b = 64×PV_12B - 2^16 - 2^13
(2^17+2^13)/64 ≤ PV_12b	=> PV_20b = 512×PV_12B - 2^20

The mapping error is always much smaller than the shot noise, which means that signal/noise ratio is maintained. In other words, the 20-bit-to-12-bit compression is virtually noiseless with no impact on final image quality.

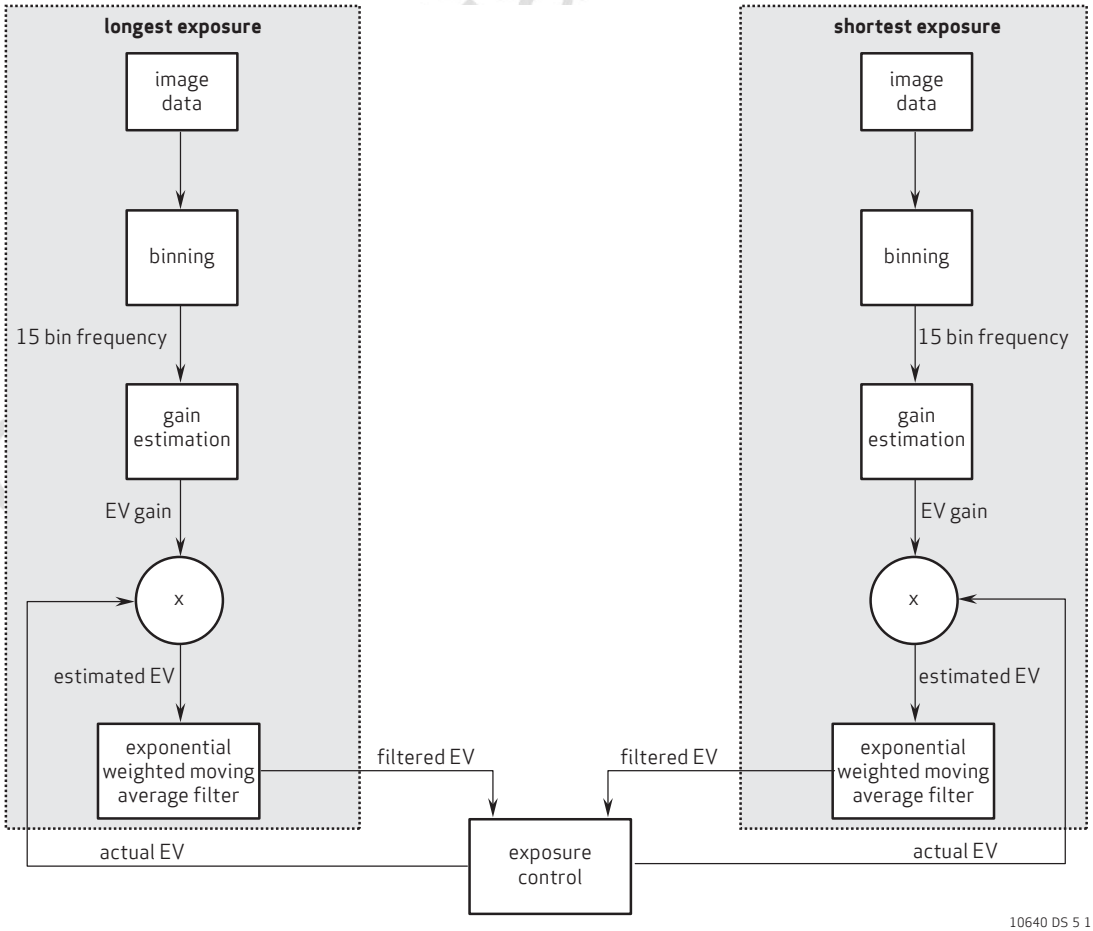
5 HDR auto exposure control (AEC debug mode)

5.1 exposure value (EV) estimation

The OV10640 high dynamic range (HDR) auto exposure control (AEC) operates by estimating exposure value (EV) to be applied in following frames. EV is the product of exposure time, analog gain, digital gain, conversion gain and pin diode ratio. The new EV is adjusted by a factor from current EV by comparing current EV to a target value.

There are three different exposure channels in the OV10640, L for long exposure, S for short exposure and VS for very short exposure. The OV10640 HDR AEC is specifically designed to work with the three exposure mode to maximize dynamic range, but will also work in single channel exposure mode. The AEC has two paths to estimate EV. The shortest exposure (VS) path will estimate an EV optimized to capture the brightest data of the scene, while the longest exposure (L) path will estimate an EV optimized to capture the darkest data of the same scene.

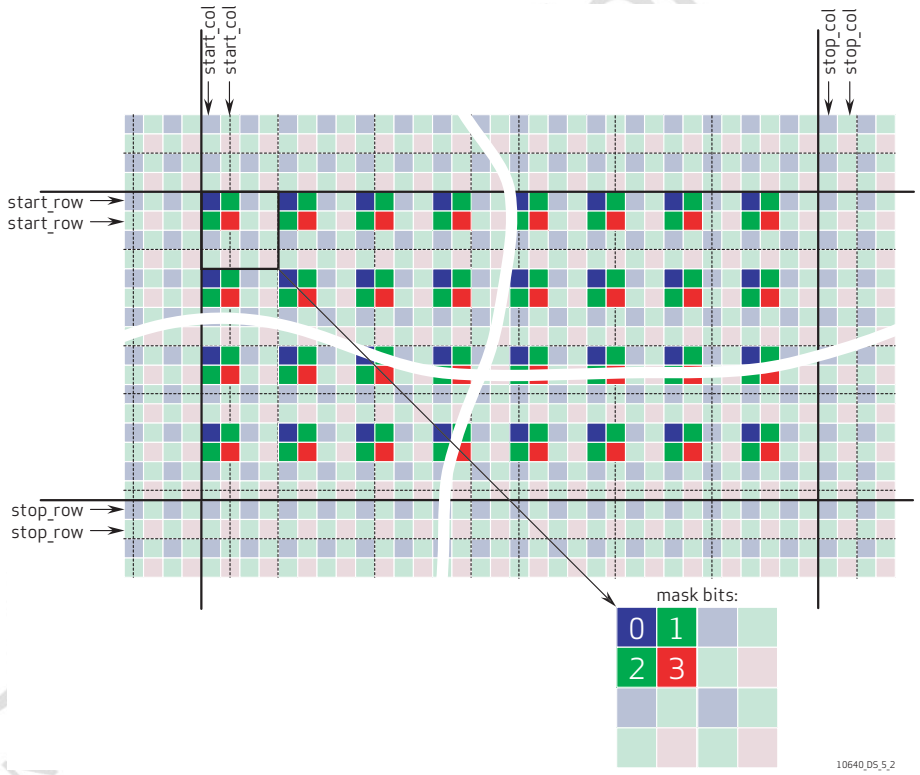
figure 5-1 HDR AEC overview diagram



In order to determine how far off the target the current EVs are, the pixel histogram is analyzed. To determine which pixels to include in the calculation, a region of interest (ROI) and a Bayer mask can be set by registers 0x30F2~0x30F9 and 0x30FA[3:0] (see **figure 5-2**).

In each of the two paths (longest and shortest exposure) (see **figure 5-2**), pixel values of the corresponding exposure are counted into bins. The bins are overlapping, so the aperture of bin #1 overlaps with bin #0, the aperture of bin #2 overlaps with bin #0 and bin #1, and so on. The binned pixel values are compared to a set of target values in order to calculate a factor with which the current image's actual EV is adjusted to give the estimated EV (see **figure 5-7**).

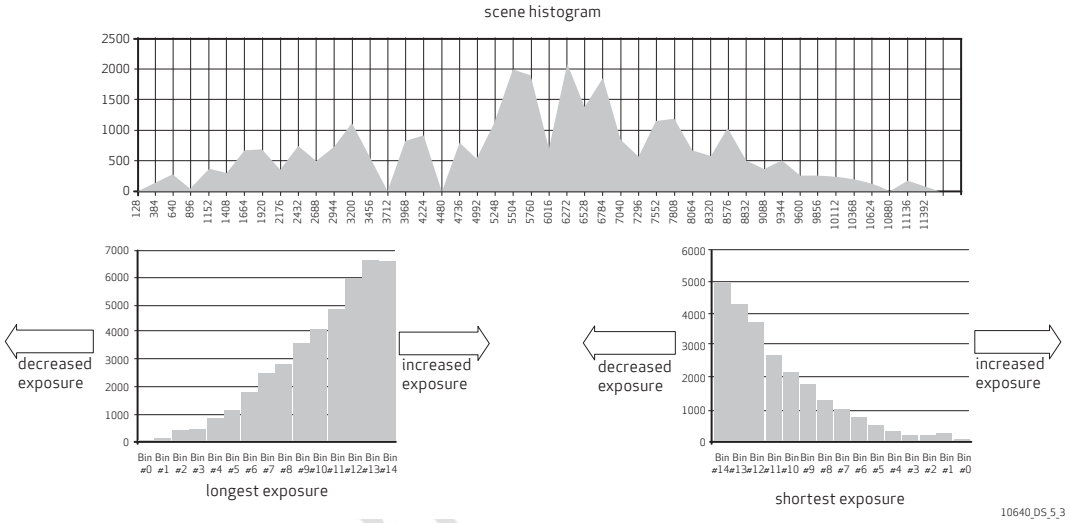
figure 5-2 region of interest (ROI) and Bayer mask bits diagram



The new EV is passed through a configurable exponentially weighted moving average filter (EWMA) (see **section 5.2.4**).

5.1.1 start of operation

figure 5-3 start of operation diagram



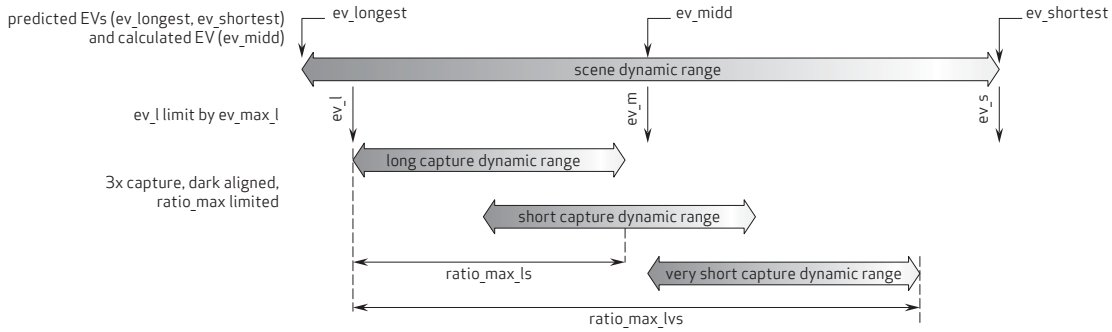
The AEC operation is performed by 'sliding' the bins left or right with respect to the scene histogram until the bin conditions match the target settings. The 'sliding' is performed by changing the EV for the respective exposure. Increasing EV will 'slide' the corresponding exposure right, while decreasing EV will 'slide' it left, see **figure 5-3**.

5.1.2 exposure control

The AEC will separate the EV into exposure time and gain values. Depending on mode of operation the longest and shortest EV will be applied to 1, 2 or 3 exposure channels. The individual exposure time and gain values may be enabled or disabled, or even automatically disabled at high temperature conditions (registers 0x7000, 0x7001 and 0x7003). If the EVs are outside the calculated limits, the exposure may be aligned to the brightest part or the darkest part (register 0x7002[1:0]). The limit calculations are based on configurable absolute limits and the capabilities of the individual exposure time and gain values set in registers 0x7040-0x70F3. If an exposure time and/or gain value is disabled in registers 0x7000, 0x7001 and 0x7003, it will be reflected in the limits.

The following figures show a few examples of how the exposure control will work in three exposure mode using dark alignment. Bright alignment will be similar but mirrored. If a minimum or maximum ratio is reached, the alignment will become asymmetrical; otherwise, it is approximately symmetrical (square root is an approximation).

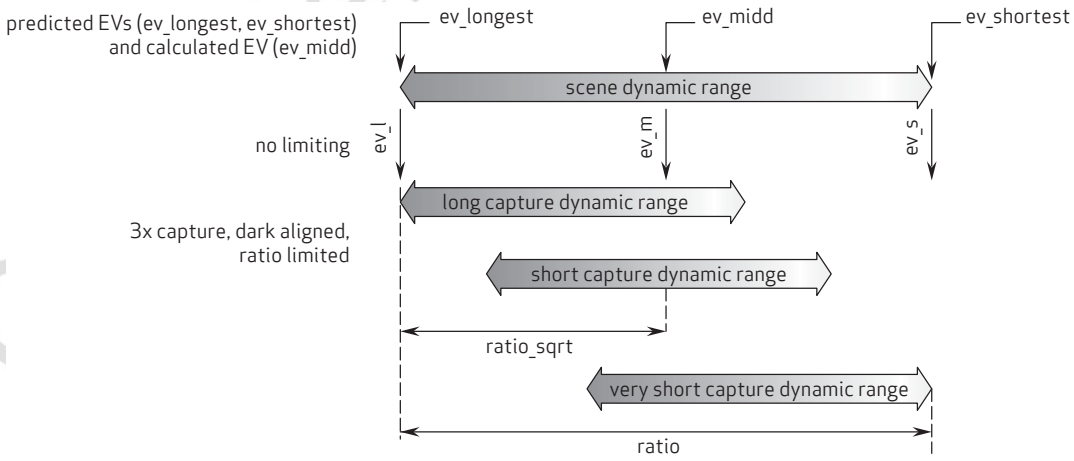
figure 5-4 exposure calculation example 1



note very high dynamic range scene captured in 3x-mode and dark aligned exposure calculation.
short and very short is determined by maximum long/short and long/very short ratios.

10640_DS_5_4

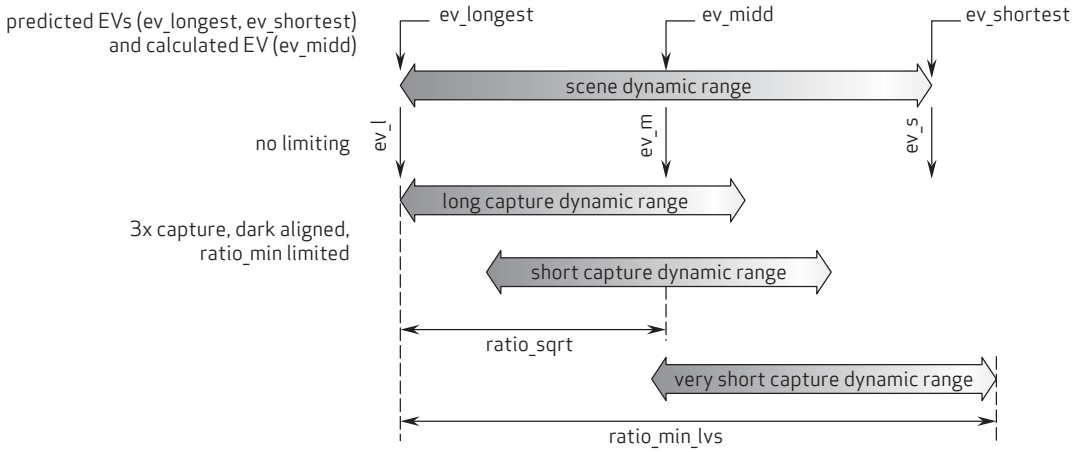
figure 5-5 exposure calculation example 2



note high dynamic range scene captured in 3x-mode and dark aligned exposure calculation.
very short is determined by actual ratio and short is aligned in geometrical middle of scene.

10640_DS_5_5

figure 5-6 exposure calculation example 3



note low dynamic range scene captured in 3x-mode and dark aligned exposure calculation.
very short is determined by minimum long/very short ratio and short is aligned in geometrical middle of scene. 10640_DS_5_6

5.2 configuration guide

5.2.1 auto exposure control

The auto exposure can be disabled or operated in one of two ways.

If 0x30FA[6] aec_enable is set, AEC is enabled and exposure parameters are controlled automatically.

If 0x30FA[5] ec_enable is set, all AEC components are enabled, except the new EV is not passed to the exposure control. It is, however, estimated just as in automatic mode and included in embedded data. The purpose of this mode is to enable host intervention. For example, in a surround view application, the host gets EVs from several sensors, but needs all the sensors to have the same exposure. The host may pick the lowest of the shortest EV and the highest of the longest EV and write it back to all sensors.

5.2.2 manual exposure

If 0x30FA[6:5]=0, AEC operation will be disabled. Exposure and gain parameters can then be set manually.

Exposure time for L and S exposure is adjusted in integer multiples of the row period. The row period is calculated as Trow = SCLK x HTS, where HTS is defined by registers 0x3080, 0x3081 and SCLK is the system clock (see **figure 3-9**) in MHz.

Subsequently, the exposure time is calculated in milliseconds as TexpL,S = ExpR × Trow, where ExpR is the exposure register value defined in registers 0x30E6, 0x30E7 for L exposure and registers 0x30E8, 0x30E9 for S exposure.

Exposure time for VS exposure is adjusted in fractions of 1/32 of the row period. The exposure time is calculated as TexpVS = ExpR/32 × Trow, where ExpR is the exposure register value defined in register 0x30EA for VS exposure.

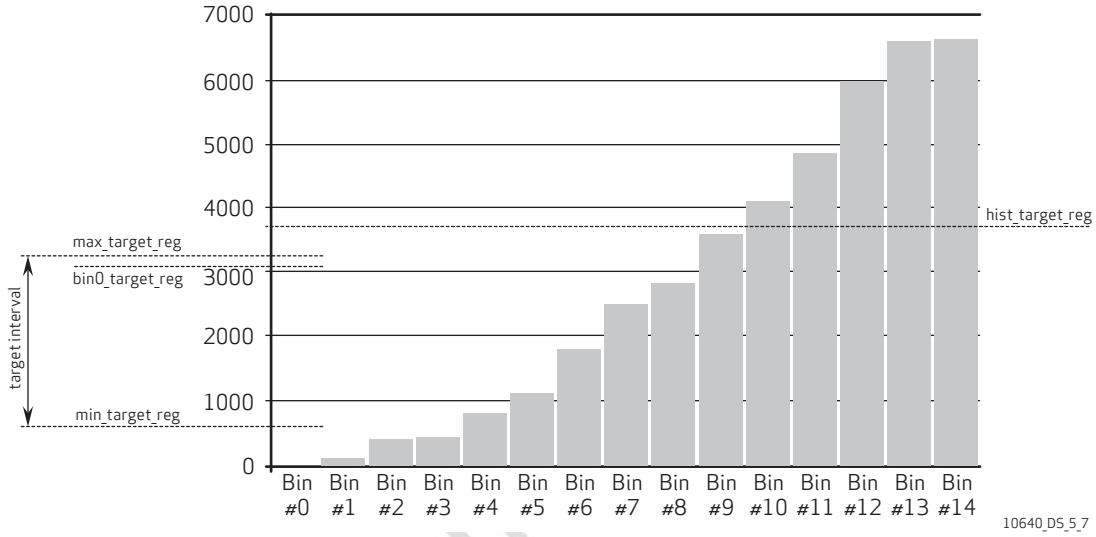
When writing analog gain and exposure time in frame n, it takes effect in frame n+2.

5.2.3 region of interest ROI

The AEC ROI together with the AEC mask bits (0x30FA[3:0]) selects which pixels will be counted by the binning. The ROI registers 0x30F2~0x30F9 set the start and stop row/column. The row setting must leave a 4-row margin minimum at the top and bottom with respect to the captured image (sensor core crop settings, see **figure 5-7**). Every odd row pair and odd column pair is skipped. The mask register selects which of the 4 Bayer pixels will be counted. By default, the two green pixels are included. The total number of pixels counted as follows:

No-of-pixels = ((aec_stop_row>>1) - (aec_start_row>>1) -1) × ((aec_stop_col>>1) (aec_start_col>>1) -1) / (4/N), where N is the number of set mask bits (default is N = 2). This is not same as pix cnt in registers 0x4011~0x4013 (see **section 5.3.5**)

figure 5-7 bins and related target values diagram



Minimum (0x7006~0x7007, min_target_reg) and maximum (0x7004~0x7005, max_target_reg) targets are both related to bin #0. Maximum target should be set to a small percentage of the total number of pixels no. of pixels as determined by ROI and mask settings), which is typically 1% to 5%. The minimum target must be set lower.

Bin #0 target (0x7008~0x7009, bin0_target_reg) will determine the factor with which EV is adjusted in case the count in bin #0 exceeds maximum target. To avoid flickering, this should be set to the same as max_target_reg.

Histogram target (0x700A~0x700B, hist_target_reg) will determine the factor with which EV is adjusted in case the count in bin #0 is less than minimum target. The factor is found by comparing bin counts in ascending order until a bin is found that reaches or exceeds the target value. The higher the bin number, the higher the factor. Typically, the histogram target is set at close to the maximum target or above (a value that is too high may cause overshoot).

5.2.4 EWMA filter

The filter is an exponentially weighted moving average EWMA:

$Out_t = Out_{t-1} + \alpha(In - Out_{t-1})/256$

α (0x700E~0x700F, ewma_alfa) can be 1 ~ 256 in steps of 1/256, where 1 is strongest filtering and 256 is no filtering.

5.2.5 exposure parameter limits

Exposure time, analog gain, digital gain and conversion gain of each exposure each have an absolute minimum and maximum register (registers 0x7040~0x70F3). The default values reflect the sensor capabilities and is not recommended to be changed.

5.2.6 exposure calculation control

The alignment of EVs can be set to bright or dark, (0x7002[1:0]). The alignment will only affect the result if the sensor's dynamic range is smaller or larger than the scene's dynamic range.

Automatic control of exposure time, analog gain, digital gain, and conversion gain of each exposure, can independently be enabled, disabled, or set to auto high temperature (freezing control in high temperature situations) (0x7000, 0x7001, 0x7003).

Furthermore, the priority (order in which EV is applied) for each exposure can be configured as follows (0x7002[7:2]):

- mode 0: conversion gain, analog gain, exposure time and digital gain
- mode 1: analog gain, conversion gain, exposure time and digital gain
- mode 2: exposure time, conversion gain, analog gain and digital gain (default)
- mode 3: exposure time, analog gain, conversion gain and digital gain

table 5-1 HDR_AEC control registers (sheet 1 of 15)

address	register name	default value	R/W	description
0x30E6	EXPO_L_H	0x00	RW	Long Exposure High Byte
0x30E7	EXPO_L_L	0x40	RW	Long Exposure Low Byte
0x30E8	EXPO_S_H	0x00	RW	Short Exposure High Byte
0x30E9	EXPO_S_L	0x40	RW	Short Exposure Low Byte
0x30EA	EXPO_VS	0x20	RW	Very Short Exposure Last five bits means fraction
0x30EB	CG_AGAIN	0x00	RW	Bit[7]: Very short CG 0: Low CG 1: High CG Bit[6]: Long CG 0: Low CG 1: High CG Bit[5:4]: Very short again 00: x1 01: x2 10: x4 11: x8 Bit[3:2]: Short again 00: x1 01: x2 10: x4 11: x8 Bit[1:0]: Long again 00: x1 01: x2 10: x4 11: x8
0x30EC	DGAIN_L_H	0x01	RW	Bit[5:0]: Long dgain[13:8] (integer)
0x30ED	DGAIN_L_L	0x00	RW	Bit[7:0]: Long dgain[7:0] (fraction)
0x30EE	DGAIN_S_H	0x01	RW	Bit[5:0]: Short dgain[13:8] (integer)

table 5-1 HDR_AEC control registers (sheet 2 of 15)

address	register name	default value	R/W	description
0x30EF	DGAIN_S_L	0x00	RW	Bit[7:0]: Short dgain[7:0] (fraction)
0x30F0	DGAIN_VS_H	0x01	RW	Bit[5:0]: Very short dgain[13:8] (integer)
0x30F1	DGAIN_VS_L	0x00	RW	Bit[7:0]: Very short dgain[7:0] (fraction)
0x30F2	AEC_ROW_START_H	0x00	RW	ROI Setting
0x30F3	AEC_ROW_START_L	0x04	RW	ROI Setting
0x30F4	AEC_COL_START_H	0x00	RW	ROI Setting
0x30F5	AEC_COL_START_L	0x00	RW	ROI Setting
0x30F6	AEC_ROW_STOP_H	0x04	RW	ROI Setting
0x30F7	AEC_ROW_STOP_L	0x30	RW	ROI Setting
0x30F8	AEC_COL_STOP_H	0x04	RW	ROI Setting
0x30F9	AEC_COL_STOP_L	0xFF	RW	ROI Setting
0x30FA	HDR_AEC_CTRL	0x06	RW	Bit[7]: data_select AEC data select 0: ISP input 1: DNS output Bit[6]: aec_enable AEC enable (automatic mode) Bit[5]: ec_enable EC enable (outputs EV and processes EV independently) Bit[4]: hdr_stats_en HDR/12-bit select Bit[3:0]: Bayer mask setting
0x30FB	PDRATIO_H	0x0E	RW	Pin Diode Ratio High Byte
0x30FC	PDRATIO_L	0x00	RW	Pin Diode Ratio Low Byte
0x30FD	CG_RATIO_H	0x08	RW	CG Ratio High Byte
0x30FE	CG_RATIO_L	0x00	RW	CG Ratio Low Byte
0x3105	REAL_GAIN_L_H	–	R	Long Digital × Analog Gain High Byte
0x3106	REAL_GAIN_L_L	–	R	Long Digital × Analog Gain Low Byte
0x3107	REAL_GAIN_S_H	–	R	Short Digital × Analog Gain High Byte
0x3108	REAL_GAIN_S_L	–	R	Short Digital × Analog Gain Low Byte
0x3109	REAL_GAIN_VS_H	–	R	Very Short Digital × Analog Gain High Byte
0x310A	REAL_GAIN_VS_L	–	R	Very Short Digital × Analog Gain Low Byte

table 5-1 HDR_AEC control registers (sheet 3 of 15)

address	register name	default value	R/W	description
0x310B	RATIO_LS_H	–	R	Long to Short Ratio High Byte
0x310C	RATIO_LS_L	–	R	Long to Short Ratio Low Byte
0x310D	RATIO_LVS_H	–	R	Long to Very Short Ratio High Byte
0x310E	RATIO_LVS_L	–	R	Long to Very Short Ratio Low Byte
0x310F	RATIO_SVS_H	–	R	Short to Very Short Ratio High Byte
0x3110	RATIO_SVS_L	–	R	Short to Very Short Ratio Low Byte
0x3111	D_EV_L_3	–	R	Longest EV Byte 3
0x3112	D_EV_L_2	–	R	Longest EV Byte 2
0x3113	D_EV_L_1	–	R	Longest EV Byte 1
0x3114	D_EV_L_0	–	R	Longest EV Byte 0
0x3115	D_EV_S_3	–	R	Shortest EV Byte 3
0x3116	D_EV_S_2	–	R	Shortest EV Byte 2
0x3117	D_EV_S_1	–	R	Shortest EV Byte 1
0x3118	D_EV_S_0	–	R	Shortest EV Byte 0
0x7000	EXPO_CALC_CTRL 1 HIGH BYTE	0x1F	RW	Bit[7:6]: cg_en_s Enable short CG 00: Off 01: On 10: Not used 11: Auto high_temp Bit[5:4]: dgain_en_s Enable short digital gain 00: Off 01: On 10: Not used 11: Auto high_temp Bit[3:2]: again_en_s Enable short analog gain 00: Off 01: On 10: Not used 11: Auto high_temp Bit[1:0]: expo_en_s Enable short exposure 00: Off 01: On 10: Not used 11: Auto high_temp

table 5-1 HDR_AEC control registers (sheet 4 of 15)

address	register name	default value	R/W	description
0x7001	EXPO_CALC_CTRL 1 LOW BYTE	0xDF	RW	Bit[7:6]: cg_en_l Enable long CG 00: Off 01: On 10: Not used 11: Auto high_temp Bit[5:4]: dgain_en_l Enable long digital gain 00: Off 01: On 10: Not used 11: Auto high_temp Bit[3:2]: again_en_l Enable long analog gain 00: Off 01: On 10: Not used 11: Auto high_temp Bit[1:0]: expo_en_l Enable long exposure 00: Off 01: On 10: Not used 11: Auto high_temp

table 5-1 HDR_AEC control registers (sheet 5 of 15)

address	register name	default value	R/W	description
0x7002	EXPO_CALC_CTRL 2 HIGH BYTE	0xAA	RW	Bit[7:6]: pri_mode_vs Very short priority 00: Conversion gain, analog gain, exposure time and digital gain 01: Analog gain, conversion gain, exposure time and digital gain 10: Exposure time, conversion gain, analog gain and digital gain (default) 11: Exposure time, analog gain, conversion gain and digital gain Bit[5:4]: pri_mode_s Short priority 00: Conversion gain, analog gain, exposure time and digital gain 01: Analog gain, conversion gain, exposure time and digital gain 10: Exposure time, conversion gain, analog gain and digital gain (default) 11: Exposure time, analog gain, conversion gain and digital gain Bit[3:2]: pri_mode_l Long priority 00: Conversion gain, analog gain, exposure time and digital gain 01: Analog gain, conversion gain, exposure time and digital gain 10: Exposure time, conversion gain, analog gain and digital gain (default) 11: Exposure time, analog gain, conversion gain and digital gain Bit[1:0]: Exposure alignment 00: Bright 01: Not used 10: Dark 11: Not used

table 5-1 HDR_AEC control registers (sheet 6 of 15)

address	register name	default value	R/W	description
0x7003	EXPO_CALC_CTRL 2 LOW BYTE	0xDF	RW	Bit[7:6]: cg_en_vs Enable very short CG 00: Off 01: On 10: Not used 11: Auto high_temp Bit[5:4]: dgain_en_vs Enable very short digital gain 00: Off 01: On 10: Not used 11: Auto high_temp Bit[3:2]: again_en_vs Enable very short analog gain 00: Off 01: On 10: Not used 11: Auto high_temp Bit[1:0]: expo_en_vs Enable very short exposure 00: Off 01: On 10: Not used 11: Auto high_temp
0x7004	MAX_TARGET_REG_L	0x13	RW	Longest Maximum Bin #0 Target Byte 1
0x7005	MAX_TARGET_REG_L	0xEC	RW	Longest Maximum Bin #0 Target Byte 0
0x7006	MIN_TARGET_REG_L	0x00	RW	Longest Minimum Bin #0 Target Byte 1
0x7007	MIN_TARGET_REG_L	0x64	RW	Longest Minimum Bin #0 Target Byte 0
0x7008	BIN0_TARGET_REG_L	0x13	RW	Longest Bin #0 Target Byte 1
0x7009	BIN0_TARGET_REG_L	0xEC	RW	Longest Bin #0 Target Byte 0
0x700A	HIST_TARGET_REG_L	0x12	RW	Longest Bin #1-14 Target Byte 1
0x700B	HIST_TARGET_REG_L	0xCA	RW	Longest Bin #1-14 Target Byte 0
0x700C	EV_GAIN_L	–	R	Longest Estimated EV Gain 8.8 Byte 1
0x700D	EV_GAIN_L	–	R	Longest Estimated EV Gain 8.8 Byte 0
0x700E	EWMA_L	0x00	RW	Longest EWMA Filter Value Bit[7]: Fine gain step (slower, more accurate) Bit[0]: Longest EWMA filter α value 1.8, max is 'h100 MSB

table 5-1 HDR_AEC control registers (sheet 7 of 15)

address	register name	default value	R/W	description
0x700F	EWMA_L	0x60	RW	Longest EWMA Filter Value Bit[7:0]: Longest EWMA filter α value 1.8, max is 'h100 8 LSBs
0x7010~ 0x7019	RSVD	–	–	Reserved
0x701A	MAX_TARGET_REG_S	0x13	RW	Shortest Maximum Bin #0 Target Byte 1
0x701B	MAX_TARGET_REG_S	0xEC	RW	Shortest Maximum Bin #0 Target Byte 0
0x701C	MIN_TARGET_REG_S	0x00	RW	Shortest Minimum Bin #0 Target Byte 1
0x701D	MIN_TARGET_REG_S	0x64	RW	Shortest Minimum Bin #0 Target Byte 0
0x701E	BIN0_TARGET_REG_S	0x13	RW	Shortest Bin #0 Target Byte 1
0x701F	BIN0_TARGET_REG_S	0xEC	RW	Shortest Bin #0 Target Byte 0
0x7020	HIST_TARGET_REG_S	0x12	RW	Shortest Bin #1-14 Target Byte 1
0x7021	HIST_TARGET_REG_S	0xCA	RW	Shortest Bin #1-14 Target Byte 0
0x7022	EV_GAIN_S	–	R	Shortest Estimated EV Gain 8.8 Byte 1
0x7023	EV_GAIN_S	–	R	Shortest Estimated EV Gain 8.8 Byte 0
0x7024	EWMA_S	0x00	RW	Shortest EWMA Filter Value Bit[7]: Fine gain step (slower, more accurate) Bit[0]: Shortest EWMA filter α value 1.8, max is 'h100 MSB
0x7025	EWMA_S	0x60	RW	Shortest EWMA Filter Value Bit[7:0]: Shortest EWMA filter α value 1.8, max is 'h100 8 LSBs
0x7026~ 0x703F	RSVD	–	–	Reserved
0x7040	D_EXPO_MAX_REG_L	0x3C	RW	Absolute Maximum Value for Exposure Time 24.8 Rows Byte 1
0x7041	D_EXPO_MAX_REG_L	0x00	RW	Absolute Maximum Value for Exposure Time 24.8 Rows Byte 0
0x7042	D_EXPO_MAX_REG_L	0x00	RW	Absolute Maximum Value for Exposure Time 24.8 Rows Byte 3
0x7043	D_EXPO_MAX_REG_L	0x04	RW	Absolute Maximum Value for Exposure Time 24.8 Rows Byte 2
0x7044	D_EXPO_MIN_REG_L	0x01	RW	Absolute Minimum Value for Exposure Time 24.8 Rows Byte 1

table 5-1 HDR_AEC control registers (sheet 8 of 15)

address	register name	default value	R/W	description
0x7045	D_EXPO_MIN_REG_L	0x00	RW	Absolute Minimum Value for Exposure Time 24.8 Rows Byte 0
0x7046	D_EXPO_MIN_REG_L	0x00	RW	Absolute Minimum Value for Exposure Time 24.8 Rows Byte 3
0x7047	D_EXPO_MIN_REG_L	0x00	RW	Absolute Minimum Value for Exposure Time 24.8 Rows Byte 2
0x7048	AGAIN_MIN_REG_L	0x00	RW	Bit[1:0]: Absolute maximum value[9:8] for analog gain 00: Unity 01: 2x 10: 4x 11: 8x
0x7049	AGAIN_MAX_REG_L	0x03	RW	Bit[1:0]: Absolute minimum value[9:8] for analog gain 00: Unity 01: 2x 10: 4x 11: 8x
0x704A	DGAIN_MAX_REG_L	0x01	RW	Absolute Maximum Value for Digital Gain 8.8 Byte 1
0x704B	DGAIN_MAX_REG_L	0x00	RW	Absolute Maximum Value for Digital Gain 8.8 Byte 0
0x704C	DGAIN_MIN_REG_L	0x00	RW	Absolute Minimum Value for Digital Gain 8.8 Byte 1
0x704D	DGAIN_MIN_REG_L	0x10	RW	Absolute Minimum Value for Digital Gain 8.8 Byte 0
0x704E	D_EV_MAX_L	–	R	Calculated Maximum EV 24.8 Byte 1
0x704F	D_EV_MAX_L	–	R	Calculated Maximum EV 24.8 Byte 0
0x7050	D_EV_MAX_L	–	R	Calculated Maximum EV 24.8 Byte 3
0x7051	D_EV_MAX_L	–	R	Calculated Maximum EV 24.8 Byte 2
0x7052	D_EV_MIN_L	–	R	Calculated Minimum EV 24.8 Byte 1
0x7053	D_EV_MIN_L	–	R	Calculated Minimum EV 24.8 Byte 0
0x7054	D_EV_MIN_L	–	R	Calculated Minimum EV 24.8 Byte 3
0x7055	D_EV_MIN_L	–	R	Calculated Minimum EV 24.8 Byte 2
0x7056	D_EXPO_MAX_L	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 1

table 5-1 HDR_AEC control registers (sheet 9 of 15)

address	register name	default value	R/W	description
0x7057	D_EXPO_MAX_L	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 0
0x7058	D_EXPO_MAX_L	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 3
0x7059	D_EXPO_MAX_L	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 2
0x705A	D_EXPO_MIN_L	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 1
0x705B	D_EXPO_MIN_L	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 0
0x705C	D_EXPO_MIN_L	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 3
0x705D	D_EXPO_MIN_L	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 2
0x705E	AGAIN_MAX_L	–	R	Calculated Maximum Analog Gain 8.8 Byte 1
0x705F	AGAIN_MAX_L	–	R	Calculated Maximum Analog Gain 8.8 Byte 0
0x7060	AGAIN_MIN_L	–	R	Calculated Minimum Analog Gain 8.8 Byte 1
0x7061	AGAIN_MIN_L	–	R	Calculated Minimum Analog Gain 8.8 Byte 0
0x7062	DGAIN_MAX_L	–	R	Calculated Maximum Digital Gain 8.8 Byte 1
0x7063	DGAIN_MAX_L	–	R	Calculated Maximum Digital Gain 8.8 Byte 0
0x7064	DGAIN_MIN_L	–	R	Calculated Minimum Digital Gain 8.8 Byte 1
0x7065	DGAIN_MIN_L	–	R	Calculated Minimum Digital Gain 8.8 Byte 0
0x7066	CG_MAX_L	–	R	Calculated Maximum CG 8.8 Byte 1
0x7067	CG_MAX_L	–	R	Calculated Maximum CG 8.8 Byte 0
0x7068	CG_MIN_L	–	R	Calculated Minimum CG 8.8 Byte 1
0x7069	CG_MIN_L	–	R	Calculated Minimum CG 8.8 Byte 0
0x706A~ 0x706B	RSVD	–	–	Reserved
0x706C 0x706F	D_ESTI_EV_S	–	R	Estimated EV Applied EV Gain to Actual
0x7070~ 0x707B	RSVD	–	–	Reserved
0x707C	D_EXPO_MAX_REG_S	0x3C	RW	Absolute Maximum Value for Exposure Time 24.8 Rows Byte 1

table 5-1 HDR_AEC control registers (sheet 10 of 15)

address	register name	default value	R/W	description
0x707D	D_EXPO_MAX_REG_S	0x00	RW	Absolute Maximum Value for Exposure Time 24.8 Rows Byte 0
0x707E	D_EXPO_MAX_REG_S	0x00	RW	Absolute Maximum Value for Exposure Time 24.8 Rows Byte 3
0x707F	D_EXPO_MAX_REG_S	0x04	RW	Absolute Maximum Value for Exposure Time 24.8 Rows Byte 2
0x7080	D_EXPO_MIN_REG_S	0x01	RW	Absolute Minimum Value for Exposure Time 24.8 Rows Byte 1
0x7081	D_EXPO_MIN_REG_S	0x00	RW	Absolute Minimum Value for Exposure Time 24.8 Rows Byte 0
0x7082	D_EXPO_MIN_REG_S	0x00	RW	Absolute Minimum Value for Exposure Time 24.8 Rows Byte 3
0x7083	D_EXPO_MIN_REG_S	0x00	RW	Absolute Minimum Value for Exposure Time 24.8 Rows Byte 2
0x7084	AGAIN_MIN_REG_S	0x00	RW	Bit[7]: Force long exposure[15] Bit[1:0]: Absolute minimum value[9:8] for analog gain 00: Unity 01: 2x 10: 4x 11: 8x
0x7085	AGAIN_MAX_REG_S	0x03	RW	Bit[1:0]: Absolute maximum value[9:8] for analog gain 00: Unity 01: 2x 10: 4x 11: 8x
0x7086	DGAIN_MAX_REG_S	0x3F	RW	Absolute Maximum Value for Digital Gain 8.8 Byte 1
0x7087	DGAIN_MAX_REG_S	0xFF	RW	Absolute Maximum Value for Digital Gain 8.8 Byte 0
0x7088	DGAIN_MIN_REG_S	0x00	RW	Absolute Minimum Value for Digital Gain 8.8 Byte 1
0x7089	DGAIN_MIN_REG_S	0x10	RW	Absolute Minimum Value for Digital Gain 8.8 Byte 0
0x708A	D_EV_MAX_S	–	R	Calculated Maximum EV 24.8 Byte 1
0x708B	D_EV_MAX_S	–	R	Calculated Maximum EV 24.8 Byte 0
0x708C	D_EV_MAX_S	–	R	Calculated Maximum EV 24.8 Byte 1
0x708D	D_EV_MAX_S	–	R	Calculated Maximum EV 24.8 Byte 0

table 5-1 HDR_AEC control registers (sheet 11 of 15)

address	register name	default value	R/W	description
0x708E	D_EV_MIN_S	–	R	Calculated Minimum EV 24.8 Byte 1
0x708F	D_EV_MIN_S	–	R	Calculated Minimum EV 24.8 Byte 0
0x7090	D_EV_MIN_S	–	R	Calculated Minimum EV 24.8 Byte 3
0x7091	D_EV_MIN_S	–	R	Calculated Minimum EV 24.8 Byte 2
0x7092	D_EXPO_MAX_S	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 1
0x7093	D_EXPO_MAX_S	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 0
0x7094	D_EXPO_MAX_S	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 3
0x7095	D_EXPO_MAX_S	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 2
0x7096	D_EXPO_MIN_S	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 1
0x7097	D_EXPO_MIN_S	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 0
0x7098	D_EXPO_MIN_S	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 3
0x7099	D_EXPO_MIN_S	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 2
0x709A	AGAIN_MAX_S	–	R	Calculated Maximum Analog Gain 8.8 Byte 1
0x709B	AGAIN_MAX_S	–	R	Calculated Maximum Analog Gain 8.8 Byte 0
0x709C	AGAIN_MIN_S	–	R	Calculated Minimum Analog Gain 8.8 Byte 1
0x709D	AGAIN_MIN_S	–	R	Calculated Minimum Analog Gain 8.8 Byte 0
0x709E	DGAIN_MAX_S	–	R	Calculated Maximum Digital Gain 8.8 Byte 1
0x709F	DGAIN_MAX_S	–	R	Calculated Maximum Digital Gain 8.8 Byte 0
0x70A0	DGAIN_MIN_S	–	R	Calculated Minimum Digital Gain 8.8 Byte 1
0x70A1	DGAIN_MIN_S	–	R	Calculated Minimum Digital Gain 8.8 Byte 0
0x70A2	CG_MAX_S	–	R	Calculated Maximum CG 8.8 Byte 1
0x70A3	CG_MAX_S	–	R	Calculated Maximum CG 8.8 Byte 0
0x70A4	CG_MIN_S	–	R	Calculated Minimum CG 8.8 Byte 1
0x70A5	CG_MIN_S	–	R	Calculated Minimum CG 8.8 Byte 0

table 5-1 HDR_AEC control registers (sheet 12 of 15)

address	register name	default value	R/W	description
0x70A6~ 0x70A7	RSVD	–	–	Reserved
0x70A8	D_ESTI_EV_VS	–	R	Estimated EV, Applied EV Gain to Actual Byte 1
0x70A9	D_ESTI_EV_VS	–	R	Estimated EV, Applied EV Gain to Actual Byte 0
0x70AA	D_ESTI_EV_VS	–	R	Estimated EV, Applied EV Gain to Actual Byte 3
0x70AB	D_ESTI_EV_VS	–	R	Estimated EV, Applied EV Gain to Actual Byte 2
0x70AC~ 0x70B7	RSVD	–	–	Reserved
0x70B8~ 0x70BB	D_EXPO_MAX_REG_ VS	–	–	Absolute Maximum Value for Exposure Time 24.8 Rows
0x70BC~ 0x70BF	D_EXPO_MIN_REG_ VS	–	–	Absolute Minimum Value for Exposure Time 24.8 Rows
0x70C0	AGAIN_MIN_REG_VS	0x00	RW	Bit[1:0]: Absolute minimum value[9:8] for analog gain 00: Unity 01: 2x 10: 4x 11: 8x
0x70C1	AGAIN_MAX_REG_VS	0x03	RW	Bit[1:0]: Absolute maximum value[9:8] for analog gain 00: Unity 01: 2x 10: 4x 11: 8x
0x70C2~ 0x70C3	DGAIN_MAX_REG_VS	–	–	Absolute Maximum Value for Digital Gain 8.8
0x70C4~ 0x40C5	DGAIN_MIN_REG_VS	–	–	Absolute Minimum Value for Digital Gain 8.8
0x70C6	D_EV_MAX_VS	–	R	Calculated Maximum EV 24.8 Byte 1
0x70C7	D_EV_MAX_VS	–	R	Calculated Maximum EV 24.8 Byte 0
0x70C8	D_EV_MAX_VS	–	R	Calculated Maximum EV 24.8 Byte 3
0x70C9	D_EV_MAX_VS	–	R	Calculated Maximum EV 24.8 Byte 2
0x70CA	D_EV_MIN_VS	–	R	Calculated Minimum EV 24.8 Byte 1
0x70CB	D_EV_MIN_VS	–	R	Calculated Minimum EV 24.8 Byte 0
0x70CC	D_EV_MIN_VS	–	R	Calculated Minimum EV 24.8 Byte 3
0x70CD	D_EV_MIN_VS	–	R	Calculated Minimum EV 24.8 Byte 2

table 5-1 HDR_AEC control registers (sheet 13 of 15)

address	register name	default value	R/W	description
0x70CE	D_EXPO_MAX_VS	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 1
0x70CF	D_EXPO_MAX_VS	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 0
0x70D0	D_EXPO_MAX_VS	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 3
0x70D1	D_EXPO_MAX_VS	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 2
0x70D2	D_EXPO_MIN_VS	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 1
0x70D3	D_EXPO_MIN_VS	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 0
0x70D4	D_EXPO_MIN_VS	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 3
0x70D5	D_EXPO_MIN_VS	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 2
0x70D6	AGAIN_MAX_VS	–	R	Calculated Maximum Analog Gain 8.8 Byte 1
0x70D7	AGAIN_MAX_VS	–	R	Calculated Maximum Analog Gain 8.8 Byte 0
0x70D8	AGAIN_MIN_VS	–	R	Calculated Minimum Analog Gain 8.8 Byte 1
0x70D9	AGAIN_MIN_VS	–	R	Calculated Minimum Analog Gain 8.8 Byte 0
0x70DA	DGAIN_MAX_VS	–	R	Calculated Maximum Digital Gain 8.8 Byte 1
0x70DB	DGAIN_MAX_VS	–	R	Calculated Maximum Digital Gain 8.8 Byte 0
0x70DC	DGAIN_MIN_VS	–	R	Calculated Minimum Digital Gain 8.8 Byte 1
0x70DD	DGAIN_MIN_VS	–	R	Calculated Minimum Digital Gain 8.8 Byte 0
0x70DE	CG_MAX_VS	–	R	Calculated Maximum CG 8.8 Byte 1
0x70DF	CG_MAX_VS	–	R	Calculated Maximum CG 8.8 Byte 0
0x70E0	CG_MIN_VS	–	R	Calculated Minimum CG 8.8 Byte 1
0x70E1	CG_MIN_VS	–	R	Calculated Minimum CG 8.8 Byte 0
0x70E2~ 0x70E3	RSVD	–	–	Reserved
0x70E4	D_RATIO_MAX_LS_ REG	0xFF	RW	Absolute Maximum Long/Short Ratio Byte 1
0x70E5	D_RATIO_MAX_LS_ REG	0xFF	RW	Absolute Maximum Long/Short Ratio Byte 0

table 5-1 HDR_AEC control registers (sheet 14 of 15)

address	register name	default value	R/W	description
0x70E6	D_RATIO_MAX_LS_REG	0x00	RW	Absolute Maximum Long/Short Ratio Byte 3
0x70E7	D_RATIO_MAX_LS_REG	0x03	RW	Absolute Maximum Long/Short Ratio Byte 2
0x70E8	D_RATIO_MIN_LS_REG	0x01	RW	Absolute Minimum Long/Short Ratio Byte 1
0x70E9	D_RATIO_MIN_LS_REG	0x00	RW	Absolute Minimum Long/Short Ratio Byte 0
0x70EA	D_RATIO_MIN_LS_REG	0x00	RW	Absolute Minimum Long/Short Ratio Byte 3
0x70EB	D_RATIO_MIN_LS_REG	0x00	RW	Absolute Minimum Long/Short Ratio Byte 2
0x70EC	D_RATIO_MAX_LVS_REG	0xFF	RW	Absolute Maximum Long/VShort Ratio Byte 1
0x70ED	D_RATIO_MAX_LVS_REG	0xFF	RW	Absolute Maximum Long/VShort Ratio Byte 0
0x70EE	D_RATIO_MAX_LVS_REG	0x00	RW	Absolute Maximum Long/VShort Ratio Byte 3
0x70EF	D_RATIO_MAX_LVS_REG	0x03	RW	Absolute Maximum Long/VShort Ratio Byte 2
0x70F0	D_RATIO_MIN_LVS_REG	0x01	RW	Absolute Minimum Long/VShort Ratio Byte 1
0x70F1	D_RATIO_MIN_LVS_REG	0x00	RW	Absolute Minimum Long/VShort Ratio Byte 0
0x70F2	D_RATIO_MIN_LVS_REG	0x00	RW	Absolute Minimum Long/VShort Ratio Byte 3
0x70F3	D_RATIO_MIN_LVS_REG	0x00	RW	Absolute Minimum Long/VShort Ratio Byte 2
0x70F4	D_RATIO_MAX_LS	–	R	Calculated Maximum Long/Short Ratio Byte 1
0x70F5	D_RATIO_MAX_LS	–	R	Calculated Maximum Long/Short Ratio Byte 0
0x70F6	D_RATIO_MAX_LS	–	R	Calculated Maximum Long/Short Ratio Byte 3
0x70F7	D_RATIO_MAX_LS	–	R	Calculated Maximum Long/Short Ratio Byte 2
0x70F8	D_RATIO_MIN_LS	–	R	Calculated Minimum Long/Short Ratio Byte 1
0x70F9	D_RATIO_MIN_LS	–	R	Calculated Minimum Long/Short Ratio Byte 0
0x70FA	D_RATIO_MIN_LS	–	R	Calculated Minimum Long/Short Ratio Byte 3

table 5-1 HDR_AEC control registers (sheet 15 of 15)

address	register name	default value	R/W	description
0x70FB	D_RATIO_MIN_LS	–	R	Calculated Minimum Long/Short Ratio Byte 2
0x70FC	D_RATIO_MAX_LVS	–	R	Calculated Maximum Long/VShort Ratio Byte 1
0x70FD	D_RATIO_MAX_LVS	–	R	Calculated Maximum Long/VShort Ratio Byte 0
0x70FE	D_RATIO_MAX_LVS	–	R	Calculated Maximum Long/VShort Ratio Byte 3
0x70FF	D_RATIO_MAX_LVS	–	R	Calculated Maximum Long/VShort Ratio Byte 2
0x7100	D_RATIO_MIN_LVS	–	R	Calculated Minimum Long/VShort Ratio Byte 1
0x7101	D_RATIO_MIN_LVS	–	R	Calculated Minimum Long/VShort Ratio Byte 0
0x7102	D_RATIO_MIN_LVS	–	R	Calculated Minimum Long/VShort Ratio Byte 3
0x7103	D_RATIO_MIN_LVS	–	R	Calculated Minimum Long/VShort Ratio Byte 2
0x7104	D_RATIO_SQRT	–	R	Square Root of Calculated Ratio Byte 1
0x7105	D_RATIO_SQRT	–	R	Square Root of Calculated Ratio Byte 0
0x7106	D_RATIO_SQRT	–	R	Square Root of Calculated Ratio Byte 3
0x7107	D_RATIO_SQRT	–	R	Square Root of Calculated Ratio Byte 2
0x7108	D_RATIO	–	R	Calculated Ratio Byte 1
0x7109	D_RATIO	–	R	Calculated Ratio Byte 0
0x710A	D_RATIO	–	R	Calculated Ratio Byte 3
0x710B	D_RATIO	–	R	Calculated Ratio Byte 2
0x710C~ 0x710F	RSVD	–	–	Reserved

5.3 statistics

The OV10640 can provide statistics from combined pixel data or separate histograms in three exposure mode. In latter configuration, the long and very short histograms will be provided by the auto exposure module, while the short histogram will be provided by the statistics engine. Hence, the auto exposure (AEC) must be enabled to guarantee that all histograms are available in embedded statistics data.

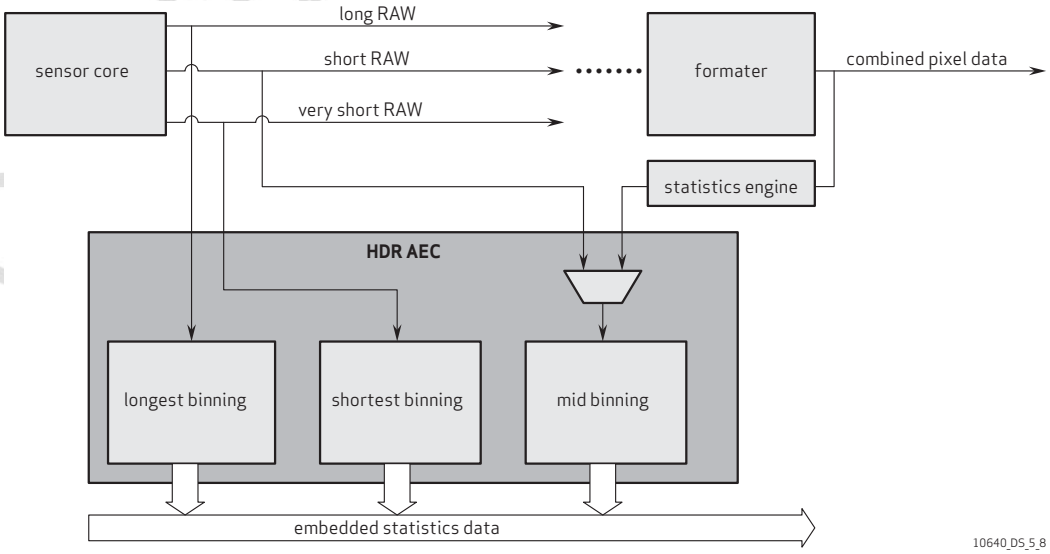
5.3.1 histogram binning

For the long (L) and very short (VS) histogram (registers 0x4053~0x4071 and 0x4014~0x4032), the binning module is a specialized 15 bin histogram. It decodes 4-bit data (16 codes). It differs from a standard histogram in two ways; bin #0 has higher capacity than the rest and bin #15 is missing.

For the combined or short histogram (in 3x12 mode), the core of the statistics engine is a simple 16-bin histogram (registers 0x4033~0x4052). To better cover all pixel codes for combined data, the decoding of combined pixel data to the histogram can be one of linear, binary logarithmic (Log2) or a hybrid of the two. Additionally, the linear decoded data is accumulated and averaged for each color. For short histogram only linear decoding is available.

The statistics engine is embedded in the auto exposure control module and the two functions share some controls. Therefore, there are some co-dependencies between these functions. The combined statistics will use stats ROI (0x4000~0x4007), while the separate histogram will use AEC ROI (0x30F2~0X30F9), and the AEC bayer mask (0x30FA[3:0]).

figure 5-8 statistics engines' relation to the system



5.3.2 combined histogram

The statistics ROI (0x4000~0x4007) defines the valid area of the pixel array. A 4-bit Bayer mask defines the valid pixels (0x30FA[3:0]).

The decoder will skip odd row/pixel pairs. The decoder will convert the incoming pixel data to a bin selector using one of three methods.

The binary logarithmic method will find the number of leading zeros (nlz) and calculate bin selector as follows:

Bin# = 15 - nlz(pixel); // number of leading zeros

The linear method will simply use the 4 MSBs as follows:

Bin# = pixel / 2^12;

The hybrid method will combine the two methods, as follows:

a = pixel / 2^5

b = 15 - nlz(pixel); // number of leading zeros

Bin# = a < 8 ? a : b;

When enabled, the histogram block counts codes in 16 bins. Each bin is 16 bit deep. In full frame and one Bayer color, the bin capacity is 80%. When the start-of-frame signal is received, bins are reset to zero. The bin scopes are shown in the following tables.

The combined histogram is presented in registers 0x4033~0x4052.

table 5-2 code range per bin with 20-bit data (sheet 1 of 2)

	Log2		hybrid		linear	
bin #	min	max	min	max	min	max
0	0	31	0	511	0	65535
1	32	63	512	1023	65536	131071
2	64	127	1024	1535	131072	196607
3	128	255	1536	2047	196608	262143
4	256	511	2048	2559	262144	327679
5	512	1023	2560	3071	327680	393215
6	1024	2047	3072	3583	393216	458751
7	2048	4095	3584	4095	458752	524287
8	4096	8191	4096	8191	524288	589823
9	8192	16383	8192	16383	589824	655359
10	16384	32767	16384	32767	655360	720895

table 5-2 code range per bin with 20-bit data (sheet 2 of 2)

bin #	Log2		hybrid		linear	
	min	max	min	max	min	max
11	32768	65535	32768	65535	720896	786431
12	65536	131071	65536	131071	786432	851967
13	131072	262143	131072	262143	851968	917503
14	262144	524287	262144	524287	917504	983039
15	524288	1048575	524288	1048575	983040	1048575

table 5-3 code range per bin with 16-bit data

bin #	Log2[a]		hybrid		linear	
	min	max	min	max	min	max
0	0	1	0	31	0	4095
1	2	3	32	63	4096	8191
2	4	7	64	95	8192	12287
3	8	15	96	127	12288	16383
4	16	31	128	159	16384	20479
5	32	63	160	191	20480	24575
6	64	127	192	223	24576	28671
7	128	255	224	255	28672	32767
8	256	511	256	511	32768	36863
9	512	1023	512	1023	36864	40959
10	1024	2047	1024	2047	40960	45055
11	2048	4095	2048	4095	45056	49151
12	4096	8191	4096	8191	49152	53247
13	8192	16383	8192	16383	53248	57343
14	16384	32767	16384	32767	57344	61439
15	32768	65535	32768	65535	61440	65535

a. although Log2 decoding is available in combined mode and 16-bit data, it is not recommended to be used.

table 5-4 code range per bin with 12-bit data

bin #	Log2[a]		hybrid[a]		linear	
	min	max	min	max	min	max
0	0	0	0	1	0	255
1	0	0	2	3	256	511
2	0	0	4	5	512	767
3	1	0	6	7	768	1023
4	1	1	8	9	1024	1279
5	2	3	10	11	1280	1535
6	4	7	12	13	1536	1791
7	8	15	14	15	1792	2047
8	16	31	16	31	2048	2303
9	32	63	32	63	2304	2559
10	64	127	64	127	2560	2815
11	128	255	128	255	2816	3071
12	256	511	256	511	3072	3327
13	512	1023	512	1023	3328	3583
14	1024	2047	1024	2047	3584	3839
15	2048	4095	2048	4095	3840	4095

a. although Log2 and hybrid decoding is available in combined mode, even if there is only 12-bit data, it is not recommended to be used

5.3.3 short histogram

The short histogram will be presented in registers 0x4033~0x4052 in same manner as linear method in **section 5.3.2**. One important difference is that short histogram will use AEC ROI (0x30F2~0X30F9) and not statistics ROI (0x4000~0x4007) to define the valid area of the pixel array. AEC bayer mask (0x30FA[3:0]) will apply.

5.3.4 long and very short histogram

The long histogram will be presented in registers 0x4053~0x4071 and very short histogram will be presented in registers 0x4014~0x4032. The long and very short histogram will use AEC ROI (0x30F2~0x30F9), and AEC bayer mask (0x30FA[3:0]).

The binning counts raw codes in 15 uniform bins, where one has higher capacity. Each bin covers 256 codes, thus the binning covers codes 0~3839 for longest exposure and codes 255~4095 for shortest exposure.

At readout, the bins are accumulated to form partially overlapping bins. When the start-of-frame signal is received, bins are reset to zero. The bin scopes are as follows:

table 5-5 bin scopes for aec_longest (L) and aec_shortest (VS)

bin #	codes (aec_longest)	codes (aec_shortest)
0	0~255	4095~3839
1	0~511	4095~3583
2	0~767	4095~3329
3	0~1023	4095~3071
4	0~1279	4095~2815
5	0 ~1535	4095~2579
6	0~1791	4095~2303
7	0~2047	4095~2047
8	0~2303	4095~1791
9	0~2559	4095~1535
10	0~2815	4095~1279
11	0~3071	4095~1023
12	0~3327	4095~767
13	0~3583	4095~511
14	0~3839	4095~255

The bin #1~14 size is 216-1, capable of counting a maximum of 20% of the full array if all pixels are selected or 80% if only one pixel is selected. Bin #0 size is 221-1.

The shortest binning (VS) instance has inversion set, while the longest binning (L) instance does not. In other words; bin #0 of shortest binning counts 0xF, while bin #0 of Longest Binning counts 0x0.

5.3.5 accumulator

The accumulator will use statistics ROI (0x4000~0x4007) and accumulate data for red, green and blue. For each color, the 16 MSBs are accumulated in a 16-bit register (registers 0x4009~0x4010). A register overflow will cause the register content to shift right one bit and a 5-bit shift value associated with the accumulator to increment by one. The results are available for each color (registers denoted …_acc_h and …_acc_l) and are in the format: xxxx_xxxx_xxxn_nnnn, where x is accumulator value and n is shift_value.

The pixel count is available as a 24-bit value in registers pix_cnt_2, pix_cnt_1 and pix_cnt_0 (registers 0x4011~0x4013).

No.-of-pixels = ((stop_row >> 1) - (start_row>>1) -1) x ((stop_col>>1 - (start_col>>1) - 1) / 4

The average can be calculated as:

For 12-bit compressed combined RAW and 20-bit combine RAW:

Average = [accumulator] × 2^[shift_value + 4] / (pix_cnt + 1)

For 16-bit log domain combined RAW:

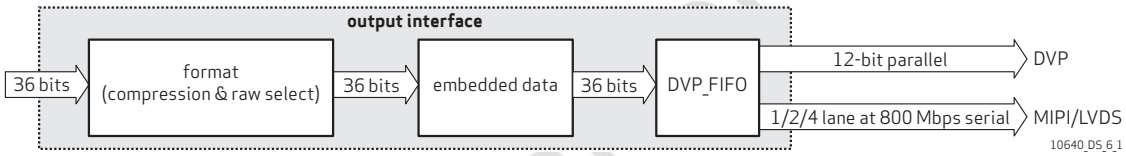
Average = [accumulator] × 2^[shift_value + 8] / (pix_cnt + 1)

6 image output interface

The video stream from the output interface (see **figure 6-1**) is formatted, compressed and output through the DVP or through the MIPI/LVDS interface. Embedded data and statistics are added pre-visible data and post-visible data.

The FIFO adapts the internal clock speed (SCLK) to the DVP/MIPI output speed (PCLK) and will start to read the FIFO after buffering enough data.

figure 6-1 output interface diagram



6.1 format

This module will configure and compress data from the ISP on the internal bus according to the sensor operation mode (3x12 RAW, 2x12 RAW compressed, 20 HDR, 16 HDR compressed and 12 HDR compressed), controlled by register 0x3119. Data will be MSB aligned except for special case 2x12 compressed format (see **section 6.1.1**). Note that compression from 20 HDR to 16 or 12 bits will be performed in ISP.

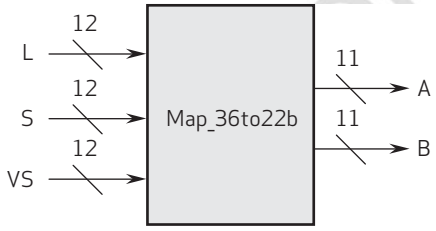
table 6-1 format control register

address	register name	default value	R/W	description
0x3119	INTERFACE_ CTRL	0x0C	RW	Bit[6]: no_comp When high, single 12-bit data is sent without compression Bit[5:4]: int_mode 00: DVP 01: MIPI 10: LVDS 11: Not used Bit[3]: auto_sel When data width in modes 12_l, 12_s and 12_vs, auto select (L versus VS) when in 2x12 mode 0: Normal mode 1: Auto select Bit[2:0]: data_width 000: 3x12 001: 2x12 010: 20 011: 16 100: 12 comb Others: Unprocessed L, S and VS

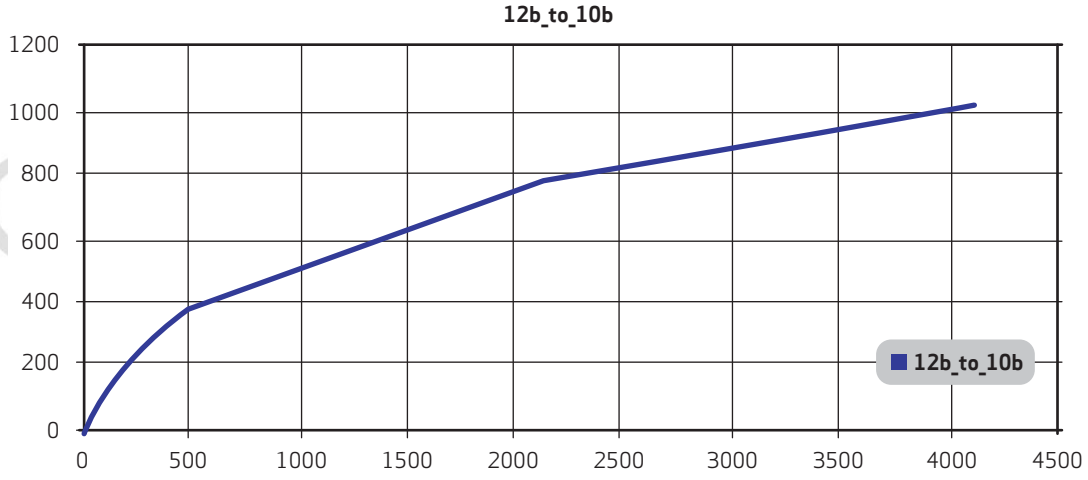
6.1.1 2x12 RAW compressed format

The OV10640 is a high dynamic range (HDR) sensor which captures three 12-bit values per pixel. A 2x12 bit/pixel format is supported, where the 11 bits data are LSB aligned and the 12th bit is forced to low, also referred to as 2x11 bit mode. **figure 6-2** illustrates what input parameters are needed to generate this output mode. Amongst the three input values {L, S, VS}, either {S, L} or {S, VS} is output depending on signal strength. If the pixel is dark, then {S, L} is output. If the pixel is bright, then {S, VS} is outputted. The omitted pixel value (i.e., VS in case of dark or L in case of bright) is assumed to have zero useful information since it is likely either saturated or zero.

figure 6-2 exposure processing diagram



A[9:0] = 10-bit value (L or VS) from 12bit-to-10bit mapping function (reference below)
A[10] = 0, if value is L
A[10] = 1, if value is VS
B[9:0] = 10-bit value (S) from 12bit-to-10bit mapping function
B[10] = debug
note: L and VS are captured with large PD, whereas S is captured with small PD



12bit-to-10bit mapping function:
if input <256 then output = input
else if input<512 then output = (input + 256)/2
else if input<2048 then output = (input + 1024)/4
else if output = (input + 4096)/8

10640 DS 6 2

6.2 digital video port (DVP)

The DVP provides a 12-bit parallel data output for the supported formats in **table 6-2**. The data bit arrangement on the DVP output is a default arrangement and can be rearranged through register 0x3124[6:4].

table 6-2 output formats

format	description	data bit arrangement		DVP output
RAW 12x3	data will be sent as 12-bit S, VS and L PCLK must be 3 times SCLK	cycle 1: cycle 2: cycle 3:	data1[11:0] data2[11:0] data3[11:0]	D[11:0]
RAW 12x2[a]	data will be sent as 12-bit B, A each component is 12 bits. 11 bits of data is in bit[10:0] PCLK must be 2 times SCLK	cycle 1(B): cycle 2(A):	{X, X, dataB[9:0]} {X, flag, dataA[9:0]}	D[11:0] D[11:0]
RAW 16[b]	data will be sent as H (high word) and L (low word) PCLK must be 2 times SCLK	cycle 1(H): cycle 2(L):	{data[15:4]} {D[3:0], D[7:0]} or {D[7:0], D[3:0]}[c]	D[11:0] D[11:0]
RAW 20[b]	data will be sent as 12-bit H (high word) and L (low word) PCLK must be 2 times SCLK	cycle 1(H): cycle 2(L):	{data[19:8]} {D[7:0], 4'bxxxx} or {D[9:0], 2'bxx}[c]	D[11:0] D[11:0]
RAW 12	HDR compressed (tone mapped) PCLK must be same frequency as SCLK		data[11:0]	D[11:0]

a. see **section 6.1.1** for details, flag = L/VS selection

b. RAW 16/20-bit data order has changed from silicon revision R1C

c. register 0x3123[3]=1

HREF, VSYNC and PCLK are configured as video output port by default as shown in **figure 6-3**. The leading edge of VSYNC is triggered by an internal SOF signal and the interval between the internal SOF signal and VSYNC is controlled by v_sync_delay (0x3120~0x3122 in unit of PCLK periods). VSYNC pulse width is set by registers 0x311C~0x311F as in the following formula:

VSYNC width = [VSYNC width line × t_{Row}] + [VSYNC width pixel × t_{PCLK}]

where:

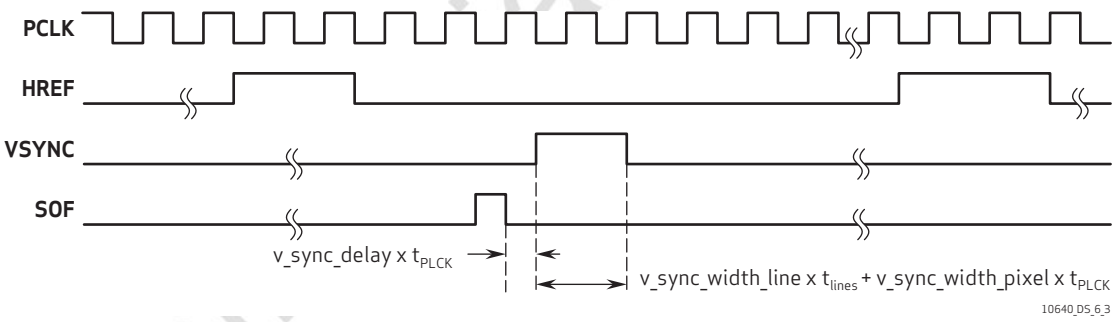
t_{Row} is row period,

t_{PCLK} is PCLK period.

VSYNC width line - {0x311C, 0x311D}

VSYNC width pixel - {0x311E, 0x311F}

figure 6-3 mode 1 diagram



The OV10640 supports walking one test pattern to test the connection between the sensor and the backend processor. The test pattern is enabled by register 0x3124[0]. By default, the image data bits are aligned with pins D[11:0].

The driver strength of the DVP can be configured by 0x3023[1:0]. **table 6-3** shows the DVP setup/hold time at 56 MHz PCLK with 1x drive current.

figure 6-4 DVP setup/hold time diagram

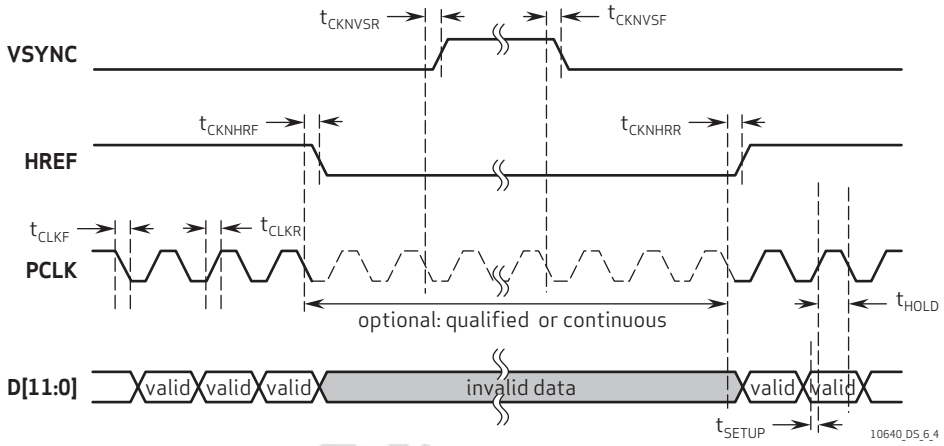


table 6-3 DVP setup/hold time[ab]

symbol	parameter	min	typ	max	unit
t_{CKNVSR}	PCLK falling edge to VSYNC rising edge delay	–	1.95	–	ns
t_{CKNVSF}	PCLK falling edge to VSYNC falling edge delay	–	1.76	–	ns
t_{CKNHRF}	PCLK falling edge to HREF falling edge delay	–	0.7	–	ns
t_{CKNHRR}	PCLK falling edge to HREF rising edge delay	–	0	–	ns
t_{CLKF}	PCLK fall time	0.29[c]	2.63[d]	1.69[e]	ns
t_{CLKR}	PLCK rise time	0.29[c]	2.77[d]	0.99[e]	ns
t_{SETUP}	data setup time	8.8	–	–	ns
t_{HOLD}	data hold time	7.6	–	–	ns

a. measured at 1.8V DOVDD and 100 MHz PCLK, with 2x drive strength

b. timing measurement shown at the beginning of the rising edge and/or of the falling edge signifies 10%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the beginning of the rising edge and/or of the falling edge signifies 90%

c. 4x driving strength

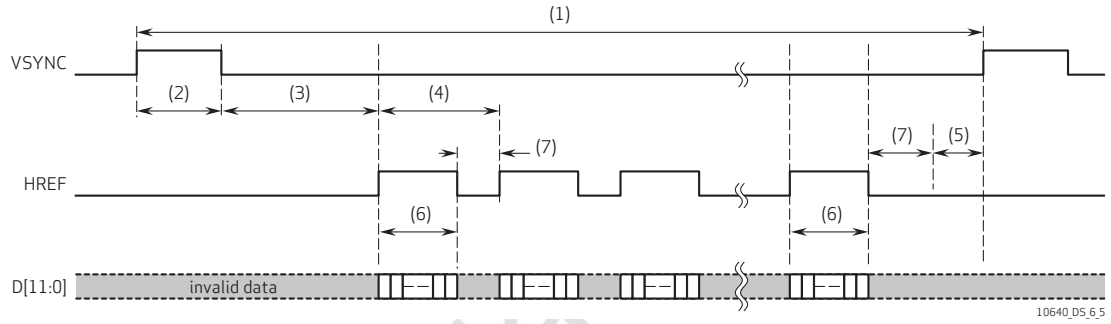
d. 2x driving strength

e. 1x driving strength

6.3 DVP timing

The DVP output is qualified by VSYNC and HREF and the timing is shown in **figure 6-5**.

figure 6-5 DVP timing diagram



(1) frame period

(2) VSYNC width

(3) VSYNC to HREF

(4) line period

(5) HREF to VSYNC

(6) active pixel

(7) horizontal blanking

(8) last horizontal blanking to VSYNC high

VSYNC pulse width is programmable from 1 CLK to 1 frame (high period = #lines + #pixels): registers 0x311C~0x311D: #lines, registers 0x311E~0x311F: #pixels

table 6-4 DVP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x311C	VSYNC_WIDTH_LINE_H	0x00	RW	Bit[7:0]: VSYNC width by line number[15:8]
0x311D	VSYNC_WIDTH_LINE_L	0x00	RW	Bit[7:0]: VSYNC width by line number[7:0]
0x311E	VSYNC_WIDTH_PIXEL_H	0x02	RW	Bit[7:0]: VSYNC width by pixel number[15:8]
0x311F	VSYNC_WIDTH_PIXEL_L	0x00	RW	Bit[7:0]: VSYNC width by pixel number[7:0]
0x3120	VSYNC_DELAY_H	0x00	RW	Bit[7:0]: VSYNC delay count[23:16]

table 6-4 DVP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3121	VSYNC_DELAY_M	0x01	RW	Bit[7:0]: VSYNC delay count[15:8]
0x3122	VSYNC_DELAY_L	0x00	RW	Bit[7:0]: VSYNC delay count[7:0]
0x3123	POLARITY_CTRL	0x00	RW	Bit[7]: Clock DDR mode enable Bit[6]: Reverse bit polarity Bit[5]: vsync_gate_clk_enable Bit[4]: href_gate_clk_enable Bit[3]: no_frst_for_fifo Bit[2]: href_polarity Bit[1]: vsync_polarity Bit[0]: pclk_polarity
0x3124	TEST_ORDER	0x00	RW	Bit[7]: fifo_bypass_mode Bit[6:4]: data_bit_swap 000: [11:0] 001: [0:11] 010: [2:11], [1:0] 011: [4:11], [3:0] 100: [9:0], [11:10] 101: [7:0], [11:8] 110: [1:0], [11:2] 111: [3:0], [11:4] Bit[3]: test_mode Bit[2]: test_bit10 Bit[1]: test_bit8 Bit[0]: test_enable
0x3125	BYP_SELECT	0x00	RW	Bit[6]: Bypass select Bit[5]: data_bit_shift Bit[4]: href_sel Bit[3:0]: bypass_sel
0x3126	R_FIFO	0x00	RW	Top Sync FIFO Control

6.4 mobile industry processor interface (MIPI)

The OV10640 MIPI uses a single uni-directional clock lane and one/two/four uni-directional data lanes to communicate to components supporting MIPI. The OV10640 follows MIPI specification D-PHY 1.00, CSI-2 V1, and supports all mandatory MIPI features.

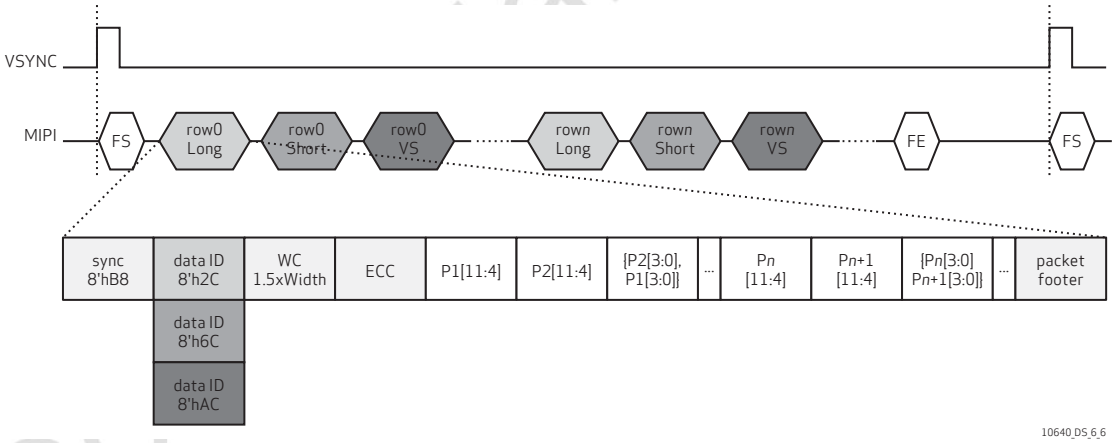
6.4.1 MIPI interface

The OV10640 supports up to 4 data lanes. The maximum data rate is 800Mbps per lane and the total bandwidth is about 3.2Gbps, which is able to output full resolution at 60 fps for any data format.

6.4.1.1 3x12b linear RAW format

L, S and VS are sent out via virtual channel 0, 1 and 2, respectively. For each exposure channel, every 2 pixels are packed into 3 bytes. **figure 6-6** illustrates the MIPI output packet.

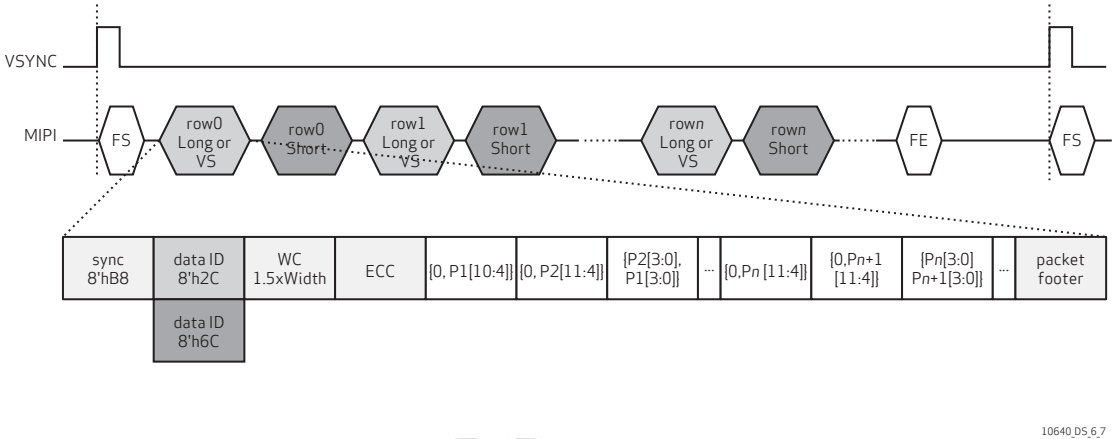
figure 6-6 3x12b linear RAW format MIPI output packet diagram



6.4.1.2 2x11b PWL RAW format

The 11b data is extended to 12b with MSB set to 0 and then sent out following CSI-2 raw12 format.

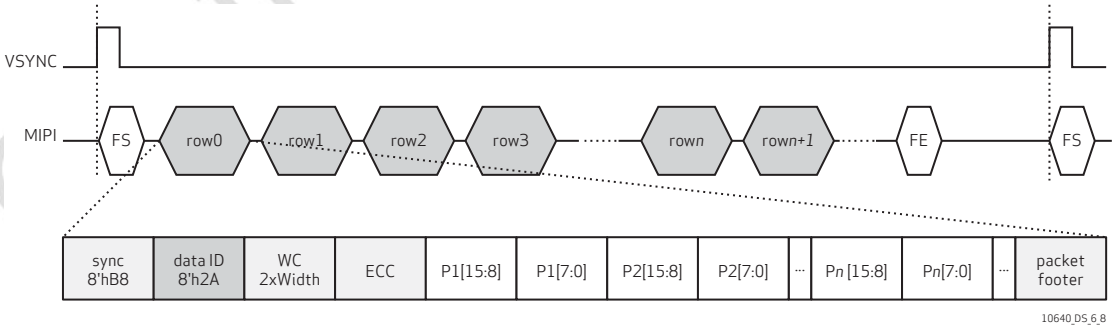
figure 6-7 2x11b PWL RAW format MIPI output packet diagram



6.4.1.3 16b log combined RAW format

16b log combined RAW is sent out following CSI-2 RAW 8 format. Every pixel is packed into 2 bytes. **figure 6-8** illustrates the MIPI output packet.

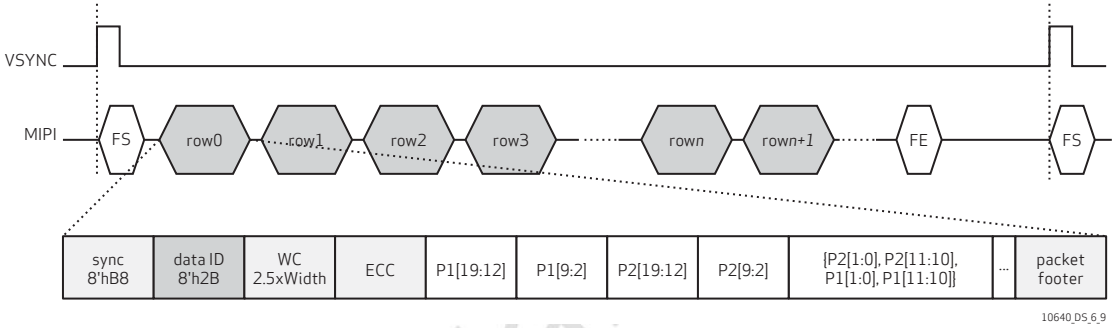
figure 6-8 16b log combined RAW format MIPI output packet diagram



6.4.1.4 20b linear combined RAW format

20b linear combined RAW is sent out following CSI-2 RAW 10 format. Every 2 pixels are packed into 5 bytes. **figure 6-9** illustrates the MIPI output packet.

figure 6-9 20b linear combined RAW format MIPI output packet diagram



6.4.1.5 12b PWL combined RAW format

20b linear combined RAW is sent out following CSI-2 RAW 10 format. Every 2 pixels are packed into 5 bytes. **figure 6-10** illustrate the MIPI output packet.

figure 6-10 12b PWL combined RAW format MIPI output packet diagram

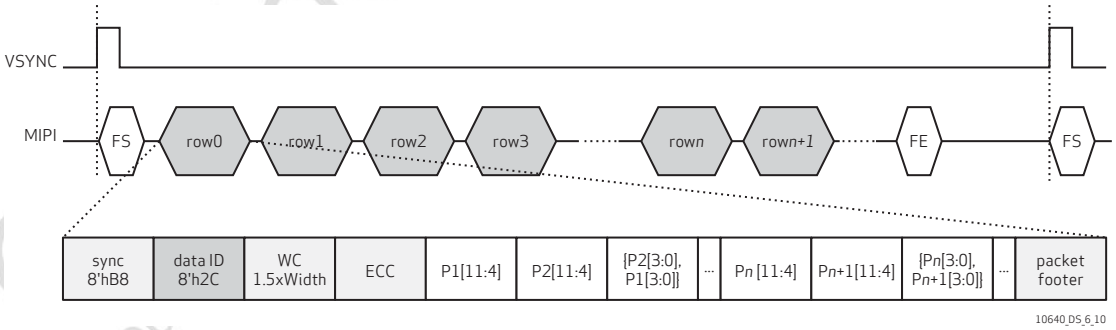


table 6-5 MIPI control registers (sheet 1 of 7)

address	register name	default value	R/W	description
0x3440	MIPI_CTRL00	0x04	RW	Bit[6]: vertical_en Bit[5]: gate_sc_en 0: Clock lane is free running 1: Gate clock lane when there is no packet to transmit Bit[4]: line_sync_en 0: Do not send line short packet for each line 1: Send line short packet for each line

table 6-5 MIPI control registers (sheet 2 of 7)

address	register name	default value	R/W	description
0x3441	MIPI_CTRL01	0x00	RW	Bit[6]: spkt_dt_sel Use dt_spkt as short packet data Bit[5]: first_bit Change clock lane first bit 0: Output 8'h55 1: Output 8'hAA Bit[1]: lpx_p_sel LPX select for pclk domain 0: Auto calculate lpx_p, unit pclk2x cycle 1: Use lpx_p min[7:0]
0x3442	MIPI_CTRL02	0x00	RW	Bit[7]: hs_prepare_s_el 0: Auto calculate T_hs_prepare, unit pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare_sel 0: Auto calculate T_clk_prepare, unit pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post_sel 0: Auto calculate T_clk_post, unit pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail_sel 0: Auto calculate T_clk_trail, unit pclk2x 1: Use clk_trail_min o[7:0] Bit[3]: hs_exit_sel 0: Auto calculate T_hs_exit, unit pclk2x 1: Use hs_exit_min o[7:0] Bit[2]: hs_zero_sel 0: Auto calculate T_hs_zero, unit pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail_sel 0: Auto calculate T_hs_trail, unit pclk2x 1: Use hs_trail_min_o[7:0] Bit[0]: clk_zero_sel 0: Auto calculate T_clk_zero, unit pclk2x 1: Use clk_zero_min_o[7:0]
0x3443	MIPI_CTRL03	0x00	RW	Bit[3]: manu_offset t_perio_manu offset SMIA Bit[2]: r_manu_half2one t_period_half to 1 SMIA Bit[1]: clk_pre_half Bit[0]: hs_pre_half

table 6-5 MIPI control registers (sheet 3 of 7)

address	register name	default value	R/W	description
0x3444	MIPI_CTRL04	0x48	RW	Bit[7:4]: lane_num_man Bit[3]: lane_num_man_en Bit[2]: lane4_6b_en_r 0: Not used 1: Support 4,7,8-lane 6-bit Bit[1]: Vsub_s 0: Valid in behind 1: Valid in front Bit[0]: vfifo_8x 0: Valid = 0 1: Valid = 8
0x3445	MIPI_CTRL05	0x00	RW	Bit[3]: lpda_retim_manu 0: Not used 1: Manual Bit[2]: lpda_retim_sel Bit[1]: lpck_retim_manu 0: Not used 1: Manual Bit[0]: lpck_retim_sel
0x3446	MIPI_CTRL06	0x10	RW	Bit[4]: pu_mark_en Power up mark1 enable Bit[3]: mipi_remot_rst Bit[2]: mipi_susp Bit[1]: smia_lane_ch_en Bit[0]: tx_lsb_first 0: High bit first 1: Low power transmit low bit first
0x3447	MIPI_CTRL07	0x03	RW	Bit[3:0]: sw_t_lpx
0x3448	MIPI_CTRL08	0x0A	RW	Bit[7:0]: wkup_dly Mark1 wakeup delay/2^10
0x3449	MIPI_CTRL10	0xFF	RW	Bit[7:0]: fcnt_max[15:8] High byte of maximum frame counter frame sync short packet
0x344A	MIPI_CTRL11	0xFF	RW	Bit[7:0]: fcnt max[7:0] Low byte of maximum frame counter of frame sync short packet
0x344B	MIPI_CTRL13	0x00	RW	Bit[2]: vc_sel_sel Bit[1:0]: Virtual channel ID
0x344C	MIPI_CTRL14	0x2A	RW	Bit[6]: lpkt_dt_sel 0: Use mipi_dt 1: Use dt_man_o as long packet data Bit[5:0]: dt_man

table 6-5 MIPI control registers (sheet 4 of 7)

address	register name	default value	R/W	description
0x344D	MIPI_CTRL15	0x00	RW	Bit[6]: pclk_inv 0: Use falling edge of mipi_pclk_o to generate MIPI bus to PHY 1: Use rising edge of mipi_pclk_o to generate MIPI bus to PHY Bit[5:0]: dt_spkt Data type for dummy line
0x344E	MIPI_CTRL16	0x52	RW	Bit[5:0]: emb_dt_manu Set embedded data type
0x3450	MIPI_CTRL18	0x00	RW	Bit[1:0]: hs_zero_min[9:8]
0x3451	MIPI_CTRL19	0x00	RW	Bit[7:0]: hs_zero_min[7:0]
0x3452	MIPI_CTRL1A	0x00	RW	Bit[1:0]: hs_trail_min[9:8]
0x3453	MIPI_CTRL1B	0x3C	RW	Bit[7:0]: hs_trail_min[7:0]
0x3454	MIPI_CTRL1C	0x01	RW	Bit[1:0]: clk_zero_min[9:8]
0x3455	MIPI_CTRL1D	0x2C	RW	Bit[7:0]: clk_zero_min[7:0]
0x3456	MIPI_CTRL1E	0x5F	RW	Bit[7:0]: clk_prepare_max Maximum value of clk_prepare, unit ns
0x3457	MIPI_CTRL1F	0x26	RW	Bit[7:0]: clk_prepare_min Minimum value of clk_prepare clk_prepare_real = clk_prepare_min_o + Tui*ui clk_prepare_min_o
0x3458	MIPI_CTRL20	0x00	RW	Bit[1:0]: clk_post_min[9:8] High byte of minimum value of clk_post, unit ns
0x3459	MIPI_CTRL21	0x3C	RW	Bit[7:0]: clk_post_min[7:0] Low byte of minimum value of clk_post clk_post_real = clk_post_min_o + Tui*ui clk_post_min_o
0x345A	MIPI_CTRL22	0x00	RW	Bit[1:0]: clk_trail_min[9:8] High byte of minimum value of clk_trail, unit ns
0x345B	MIPI_CTRL23	0x3C	RW	Bit[7:0]: clk_trail_min[7:0] Low byte of minimum value of clk_trail clk_trail_real = clk_trail_min o + Tui*ui clk_trail_min_o
0x345C	MIPI_CTRL24	0x00	RW	Bit[1:0]: lpx_p_min[9:8] High byte of minimum value of lpx_p, unit ns
0x345D	MIPI_CTRL25	0x32	RW	Bit[7:0]: lpx_p_min[7:0] Low byte of minimum value of lpx_p lpx_p_real = lpx_p_min_o + Tui*ui lpx_p_min_o

table 6-5 MIPI control registers (sheet 5 of 7)

address	register name	default value	R/W	description
0x345E	MIPI_CTRL26	0x28	RW	Bit[7:0]: hs_prepare_min Minimum value of hs_prepare, unit ns
0x345F	MIPI_CTRL27	0x55	RW	Bit[7:0]: hs_prepare_max Maximum value of hs_prepare hs_prepare_real = hs_prepare_max_o +Tui*ui hs_prepare_max_o
0x3460	MIPI_CTRL28	0x00	RW	Bit[1:0]: hs_exit_min[9:8]
0x3461	MIPI_CTRL29	0x64	RW	Bit[7:0]: hs_exit_min[7:0] Low byte of minimum value of hs_exit hs_exit_real = hs_exit_min_o
0x3462	MIPI_CTRL2A	0x0A	RW	Bit[5:0]: ui_hs_zero_min Minimum UI value of hs_zero, unit UI
0x3463	MIPI_CTRL2B	0x04	RW	Bit[5:0]: ui_hs_trail_min Minimum UI value of hs_trail, unit UI
0x3464	MIPI_CTRL2C	0x00	RW	Bit[5:0]: ui_clk_zero_min Minimum UI value of clk_zero, unit UI
0x3465	MIPI_CTRL2D	0x00	RW	Bit[7:4]: ui_clk_prepare_max Maximum UI value of clk_prepare, unit UI Bit[3:0]: ui_clk_prepare_min Minimum UI value of clk_prepare, unit UI
0x3466	MIPI_CTRL2E	0x34	RW	Bit[5:0]: ui_clk_post_min Minimum UI value of clk_post, unit UI
0x3467	MIPI_CTRL2F	0x00	RW	Bit[5:0]: ui_clk_trail_min Minimum UI value of clk_trail, unit UI
0x3468	MIPI_CTRL30	0x00	RW	Bit[5:0]: ui_lpx_p_min Minimum UI value of lpx_p, unit UI
0x3469	MIPI_CTRL31	0x64	RW	Bit[7:4]: ui_hs_prepare_max Maximum UI value of hs_prepare, unit UI Bit[3:0]: ui_hs_prepare_min Minimum UI value of hs_prepare, unit UI
0x346A	MIPI_CTRL32	0x00	RW	Bit[5:0]: ui_hs_exit_min Minimum UI value of hs_exit, unit UI
0x346B	MIPI_CTRL33	0x18	RW	Bit[5:0]: mipi_pkt_star_size
0x346C	MIPI_CTRL36	0x00	RW	Bit[0]: smia_cal_en
0x346D	MIPI_CTRL37	0x14	RW	Bit[7:0]: pclk_period Period of pclk2x, pclk_div=1 and 1-bit decimal

table 6-5 MIPI control registers (sheet 6 of 7)

address	register name	default value	R/W	description
0x346E	MIPI_CTRL38	0x00	RW	Bit[6]: lp_dir_man0 0: Output 1: Input Bit[5]: lp_p0 Lane 1 manual out p Bit[4]: lp_n0 Lane1 manual out n Bit[3]: lp_sel1 0: Auto generate mipi_lp_dir2_o 1: Use lp_dir_man2 o to be mipi_lp_dir2_o Bit[2]: lp_dir_man1 0: Output 1: Input Bit[1]: lp_p1 Lane 1 manual out p Bit[0]: lp_n1 Lane 1 manual out n
0x346F	MIPI_CTRL39	0x00	RW	Bit[7]: lp_sel2 0: Auto generate mipi_lp_dir1_o 1: Use lp_dir_man1_o to be mipi_lp_dir1_o Bit[6]: lp_dir_man2 0: Output 1: Input Bit[5]: lp_p2 Lane 2 manual out p Bit[4]: lp_n2 lane 2 manual out n Bit[3]: lp_sel3 0: Auto generate mipi_lp_dir2_o 1: Use lp_dir_man2_o to be mipi_lp__dir2_o Bit[2]: lp_dir_man3 0: Output 1: Input Bit[1]: lp_p3 Lane 3 manual out p Bit[0]: lp_n3 Lane 3 manual out n
0x3472	MIPI_CTRL3C	0x02	RW	Bit[3:0]: t_clk_pre

table 6-5 MIPI control registers (sheet 7 of 7)

address	register name	default value	R/W	description
0x3473	MIPI_CTRL3D	0x00	RW	Bit[7]: lp_ck_se0 0: Auto generate mipi_ck_lp_dir0_o 1: Use lp_ck_dir_man0 to be mipi_ck_lp_dir0_o Bit[6]: lp_ck_dir_man0 0: Input 1: Output Bit[5]: lp_ck_p0 Bit[4]: lp_ck_n0 Bit[3]: lp_ck_sel1 0: Auto generate mipi_ck_lp_dir1_o 1: Use p_ck_dir_man1 to be mipi_ck_lp_dir1_o Bit[2]: lp_ck_dir_man1 0: Input 1: Output Bit[1]: lp_ck_p1 Bit[0]: lp_ck_n1
0x3474	MIPI_CTRL4A	0x27	RW	Bit[5]: slp_lp_pon_man Set for power up Bit[4]: slp_lp_pon_da Bit[3]: slp_lp_pon_ck_da Bit[2]: mipi_slpst_man MIPI bus status manual control enable in sleep mode Bit[1]: slpst_clk_lane Bit[0]: slpst_data_lane
0x3475	MIPI_CTRL4B	0x07	RW	Bit[2]: line_st_sel 0: Line starts after HREF 1: Line starts after FIFO starts Bit[1]: clk_start_sel 0: Clock starts after SOF 1: Clock starts after reset Bit[0]: sof_sel 0: Frame starts after HREF 1: Frame starts after SOF
0x3476	MIPI_CTRL4C	0x03	RW	Bit[7]: sof_sel Bit[6]: smia_fcnt_sel Bit[5]: prbs_en Bit[4]: mipi_test MIPI high speed only test mode enable Bit[3]: fcnt_inact Set frame count to inactive mode (keep 0)
0x3477	MIPI_CTRL4D	0xB6	RW	Bit[7:0]: Pattern data lane
0x3478	MIPI_CTRL4E	0x10	RW	Bit[7:0]: r_fe_dly Last packet to frame end delay / 2
0x3479	MIPI_CTRL4F	0x55	RW	Bit[1:0]: ck_patten_data

6.5 low-voltage differential signaling (LVDS)

LVDS is a common differential signaling interface that has low power consumption, minimal EMI, and excellent noise immunity. LVDS supports 1/2/4 lane configurations. The maximum data rate for LVDS is 800 Mbps per lane. In case of multiple lanes, each data lane transmits one pixel serially from MSB to LSB using rising and falling edges of clock. Contact your local OmniVision FAE for more details.

Features include:

- supports 12-bit mode
- supports 1/2/4 lanes mode
- in 2- and 4-lane mode, supports 4 byte sync code per lane or split in every lane
- supports SAV first or EAV first switching
- supports manual setting sync code (can set different sync code for frame start/end and line start/end)
- supports manual setting dummy data in blanking duration
- supports bit swap or not to fit for different PHY
- supports PCLK inversion

6.5.1 LVDS sync mode

Set register bit 0x3430[0] to 1'b1 to enable synchronize code every lane mode. Each lane has 4 bytes of synchronizing.

```
Lane0: FF 00 00 SAV P0          ...       Pn-4 FF 00 00 00 EAV
Lane1: FF 00 00 SAV P1          ...       Pn-3 FF 00 00 00 EAV
Lane2: FF 00 00 SAV P2          ...       Pn-2 FF 00 00 00 EAV
Lane3: FF 00 00 SAV P3          ...       Pn-1 FF 00 00 00 EAV
```

6.5.2 split synchronize code

Set register bit 0x3430[0] to 1'b0 to enable split synchronize code mode. The lane amount differs for each lane amount and 4 bytes are inserted for different lane amounts.

```
four lane case
Lane0: FF P0 P4         ...       Pn-4 FF
Lane1: 00 P1 P5         ...       Pn-3 00
Lane2: 00 P2 P6         ...       Pn-2 00
Lane3: SAV P3 P7        ...       Pn-1 EAV
```

6.5.3 embedded channel ID in SAV or EAV

Set register bit 0x3430[3] to 1'b1 to enable the embedded channel ID mode. In normal mode, the sync code structure is:

```
SAV/EAV: 1'b1, F, V, H, V^H, F^H, F^V, F^V^H.
F: Field sync control by register 0x3430[2];
V: 1, vertical blank
H: 1, Horizontal blank.
For 8-bit mode : sync code = SAV/EAV
For 10-bit mode : sync code = SAV/EAV, 2'b00.
For 12-bit mode : sync code = SAV/EAV, 4'b0000.
```

But in embedded channel ID mode, the last 4 digits of SAV/EAV will be replaced by lane ID:

```
LANE0 : sync code = 1'b1, F, V, H, 4'b0000;
LANE1 : sync code = 1'b1, F, V, H, 4'b0001;
LANE2 : sync code = 1'b1, F, V, H, 4'b0010;
LANE3 : sync code = 1'b1, F, V, H, 4'b0011;
```

table 6-6 LVDS registers (sheet 1 of 2)

address	register name	default value	RW	description
0x3430	LVDS_R0	0x2A	RW	Bit[6]: r_syc_cod_man Sync code manual enable Bit[5]: r_syncd_en Bit[4]: lvds_pclk_inv Invert lvds_pclk_o Bit[3]: r_chid_en Channel ID enable in sync per lane mode Bit[2]: lvds_f CCIR parameter F Bit[1]: sav_first_en 0: EAV first 1: SAV first Bit[0]: sync_code_mod 0: Only one sync code 1: Sync code per lane
0x3431	LVDS_R2	0x00	RW	Dummy Data0 High Nibble
0x3432	LVDS_R3	0x80	RW	Dummy Data0 Low Byte
0x3433	LVDS_R4	0x00	RW	Dummy Data1 High Nibble
0x3434	LVDS_R5	0x10	RW	Dummy Data1 Low Byte

table 6-6 LVDS registers (sheet 2 of 2)

address	register name	default value	RW	description
0x3435	LVDS_R6	0xAA	RW	frame_st
0x3436	LVDS_R7	0x55	RW	frame_ed
0x3437	LVDS_R8	0x99	RW	line_st
0x3438	LVDS_R9	0x66	RW	line_ed
0x3439	LVDS_RA	0x08	RW	Bit[3]: r_bit_flip Bit[2]: r_hts_man_en Bit[1]: r_ln2_sel Bit[0]: r_chk_pcnt
0x343A	LVDS_RB	0x88	RW	Bit[7]: sleep_en Bit[5]: r_frame_rst_en Bit[4:0]: r_ln_end_dly
0x343B	LVDS_RC	0x00	RW	r_blk_time High Nibble
0x343C	LVDS_RD	0x02	RW	r_blk_time Low Byte
0x343D	LVDS_RE	0x00	RW	r_hts_man High Byte
0x343E	LVDS_RF	0x00	RW	r_hts_man Low Byte
0x343F	LVDS_LANE_NR	0x04	RW	Active LVDS Lanes

6.6 embedded data

Additional information about the set up and configuration of the sensor can be embedded in the video stream.The embedded data contains the values of a programmable list of registers to describe the current state of the sensor (e.g., frame counter, exposure time and gain, etc.), as well as the statistics data from the stats module. The embedded data can be added before the video stream, after the video data or both (2+2, 2+0, 0+2, 0+0). Embedded data can be displayed in the image by setting register 0x3091[3:2], and the output size must be increased by 4 to output 4 embedded rows.

The OV10640 can output the value from all of the registers before the video frame. All data fits inside the first row. The second row is empty.

The OV10640 can output the calculated statistics from the current frame data after the video frame. All data fits inside the first row. The second row is empty.

Embedded data will be read using a specific read bus from the registers. The normal register bus will not be used since it will be occupied.

6.6.1 embedded data format at output

Each register value is preceded by the tag 0xDA. When output data width is more than 8 bits, tag and register values will be MSB aligned (see **figure 6-12** for special case 2x12).

When more than one component per pixel is transmitted (e.g., 3x12 or 2x12), the same register value will be copied to all the components.

The number of registers transmitted is dependent on the register start and end address and might be one or two rows.The last four registers are CRC value (4 bytes) preceded with the tag value before each byte.

figure 6-11 3x12 RAW mode diagram

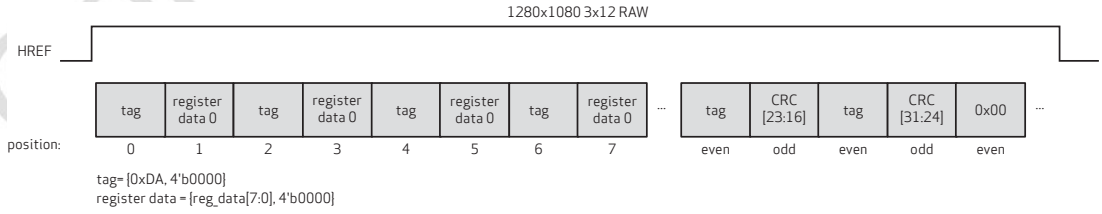


figure 6-12 2x12 (2x11) RAW mode diagram

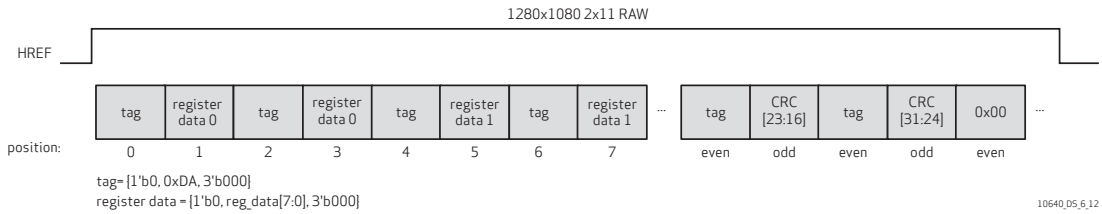


figure 6-13 1x12 RAW mode diagram

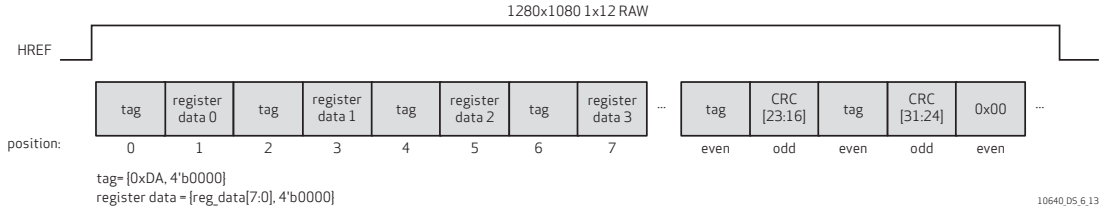
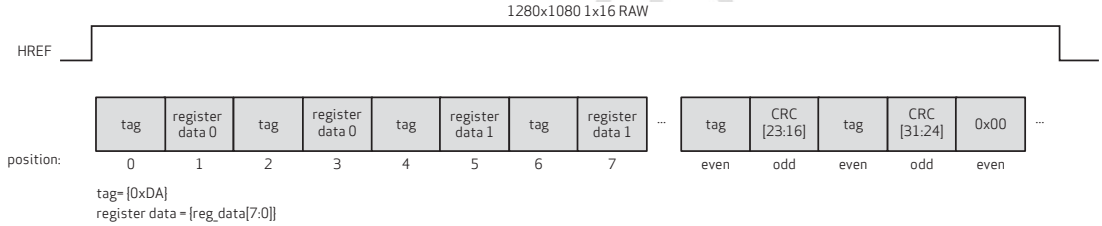
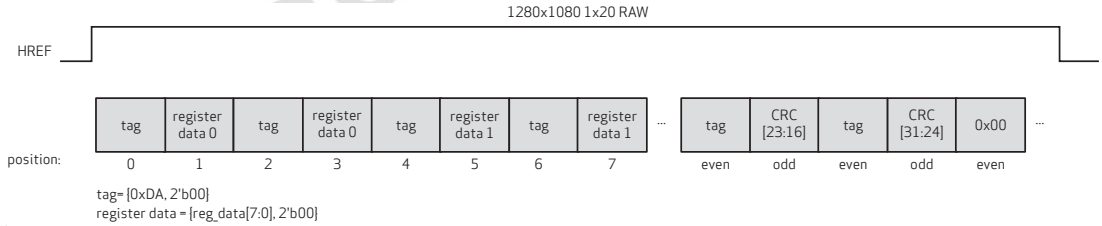


figure 6-14 1x16 RAW mode diagram



note 1 16-bit data is packed as 2x8 bits, such as {embedded data, repeat embedded data}.

figure 6-15 1x20 RAW mode diagram



note 1 20-bit data is packed as 2x10 bits, such as {embedded data, 2'b00, repeat embedded data, 2'b00}.

6.7 group hold

The OV10640 supports a group hold function where the register values are recorded in an internal buffer instead of writing to the register directly.

The OV10640 supports up to four groups. The number of entries for each group is set by registers 0x3028~0x302B. The total sum for the four groups is limited to 256 entries.

The group hold function is controlled through registers 0x302C~0x302F.

To program group hold, set 0x302F to 0x00 and select which group to program in 0x302C[3:2]. Then, specify the register to group hold by entering the register address and swap MSB (bit[15]) in address to 1. So, 0x3000 would be 0xB000, 0x30E6 would be 0xB0E6, etc.

To enable group hold, set register 0x302F[1:0] for 'single launch' to launch group settings once, or 'auto launch' to automatically switch between groups selected in 0x302C[3:0].

Example group hold:

```
  -  set group0
60 302f 00
60 302c 00 ;group0
60 B0eb 00 ;register 308b, hold function is bit 15 of address


  -  set group 1
60 302f 00
60 302c 04 group1
60 B0eb 01 ;register 308b, hold function is bit 15 of address


  -  set group 2
60 302f 00
60 302c 08 group2
60 B0eb 02 ;register 308b, hold function is bit 15 of address


  -  set group 3
60 302f 00
60 302c 0C group3
60 B0eb 03 ;register 308b, hold function is bit 15 of address
```

```
  -  single launch group0
60 302c 10 ;group0
60 302f 01 ;single launch

  -  single launch group1
60 302c 14 ;group1
60 302f 01 ;single launch

  -  single launch group2
60 302c 18 ;group2
60 302f 01 ;single launch

  -  single launch group3
60 302c 1C ; group3
60 302f 01 ;single launch

  -  auto switch between group0 and group1
60 302c 11 ; group0-1
60 302f 02 ; auto launch

  -  auto switch between group0 and group2
60 302c 12 ; group0-2
60 302f 02 ; auto launch

  -  auto switch between group2 and group3
60 302c 1B ; group2-3
60 302f 02 ; auto launch
```

table 6-7 group hold control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3028	GROUP_LENGTH0	0x40	RW	Number of Registers for Group 0 Total Sum of 4 Groups is Limited to 256
0x3029	GROUP_LENGTH1	0x40	RW	Number of Registers for Group 1
0x302A	GROUP_LENGTH2	0x40	RW	Number of Registers for Group 2
0x302B	GROUP_LENGTH3	0x40	RW	Number of Registers for Group 3
0x302C	GROUP_CTRL	0x03	RW	Bit[6]: launch_now Launch immediately, when single start is set Bit[5]: launch_pre_sof Launch before sensor core SOF, if single start is set Bit[4]: launch_post_sof Launch after sensor core SOF, if single start is set Bit[3:2]: first_grp_sel Main group select for hold and launch operation. Also used as the first group in auto mode. 00: Group select 0 01: Group select 1 10: Group select 2 11: Group select 3 Bit[1:0]: second_grp_sel Used as second group in auto mode
0x302D	FIRST_GRP_FRAMES	0x01	RW	Frames for Staying in Group Selected by First Grp Sel (Number of Frames = Register Value -1)
0x302E	SECOND_GRP_FRAMES	0x01	RW	Frames for Staying in Group Selected by Second Grp Sel (Number of Frames = Register Value -1)
0x302F	OPERATION_CTRL	0x02	RW	Bit[1]: auto_mode Switches automatically between first and second groups using frame counts Bit[0]: single_start Launch only once, reset by logic after done, overridden by auto_mode
0x3030	EMB_START_ADDR0_H	0x30	RW	Bit[7:0]: First embedded data range 0[15:8]
0x3031	EMB_START_ADDR0_L	0x00	RW	Bit[7:0]: First embedded data range 0[7:0]
0x3032	EMB_END_ADDR0_H	0x35	RW	Bit[7:0]: Last embedded data range 0[15:8]
0x3033	EMB_END_ADDR0_L	0x00	RW	Bit[7:0]: Last embedded data range 0[7:0]
0x3034	EMB_START_ADDR1_H	0x40	RW	Bit[7:0]: First embedded data range 1[15:8] Change to FF if not used

table 6-7 group hold control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3035	EMB_START_ADDR1_L	0x00	RW	Bit[7:0]: First embedded data range 1[7:0] Change to FF if not used
0x3036	EMB_END_ADDR1_H	0x42	RW	Bit[7:0]: Last embedded data range 1[15:8]
0x3037	EMB_END_ADDR1_L	0x00	RW	Bit[7:0]: Last embedded data range 1[7:0]
0x3038	ACTIVE_GROUP_NR	–	R	Indicates Which Group is Active
0x3039	FRAME_CNT_ACTIVE	–	R	Number of Frames with Current Group Valid Only in Auto Mode

7 serial camera control bus (SCCB) interface

The SCCB interface controls the image sensor operation. Refer to the *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for data transfer protocol and detailed usage of the serial control port.

7.1 SCCB timing

figure 7-1 SCCB interface timing

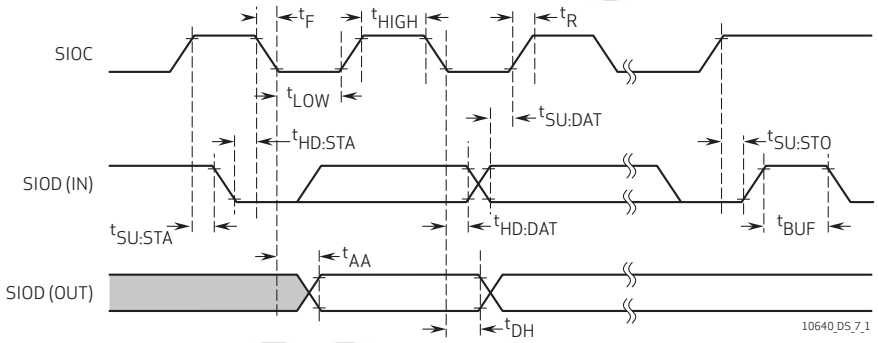


table 7-1 SCCB interface timing specifications[ab]

symbol	parameter	min	typ	max	unit
f_{SIOC}	clock frequency			400	kHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SIOC low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400kHz mode

b. timing measurement shown at the beginning of the rising edge or the end of the falling edge signifies 30%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the end of rising edge or the beginning of the falling edge signifies 70%

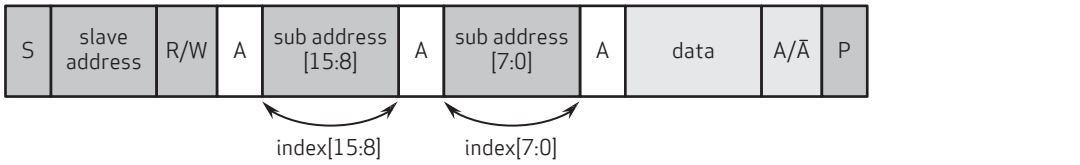
7.2 direct access mode

7.2.1 message format

The OV10640 supports the message format shown in **figure 7-2**. The repeated START (Sr) condition is shown in **figure 7-3** and **figure 7-5**.

figure 7-2 message type

message type: 16-bit sub-address, 8-bit data, and 7-bit slave address



from slave to master
from master to slave
direction depends on operation

S START condition
P STOP condition
Sr repeated START condition

A acknowledge
Ā negative acknowledge

10640_DS_7_2

7.2.2 read / write operation

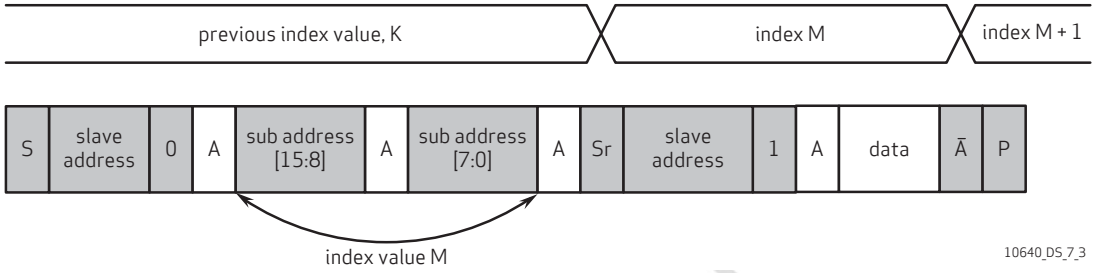
The OV10640 supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

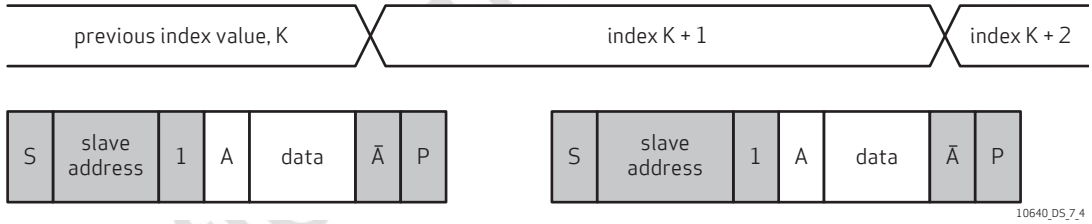
In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SIOD line as shown in **figure 7-3**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 7-3 SCCB single read from random location



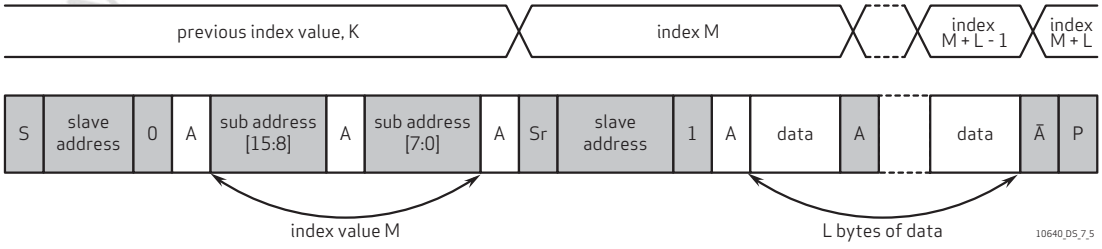
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SIOD line as shown in **figure 7-4**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 7-4 SCCB single read from current location



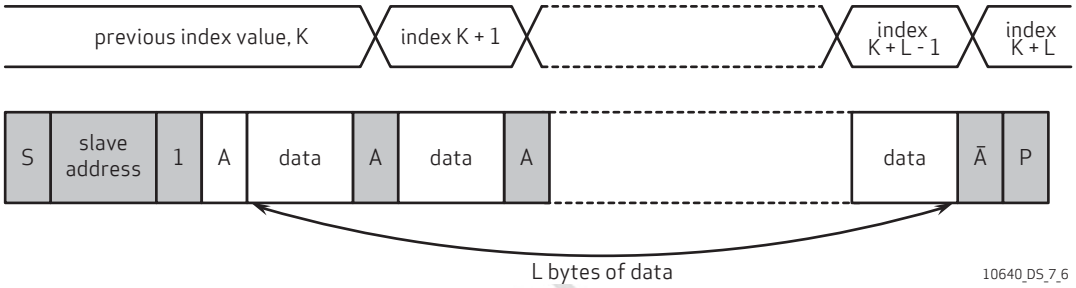
The sequential read from a random location is illustrated in **figure 7-5**. The master does a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 7-5 SCCB sequential read from random location



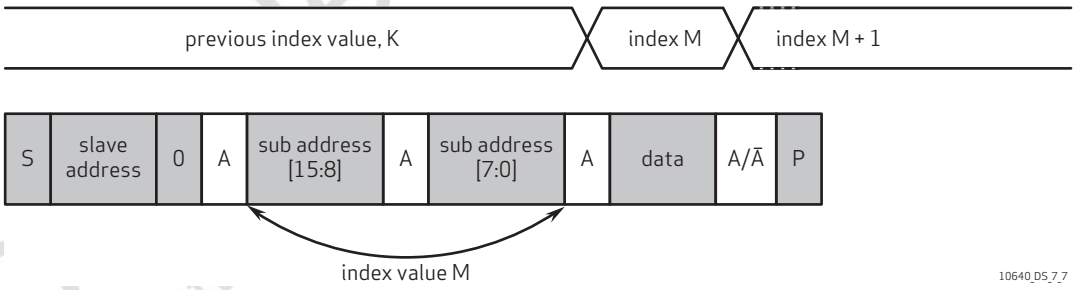
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation. as shown in **figure 7-6**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 7-6 SCCB sequential read from current location



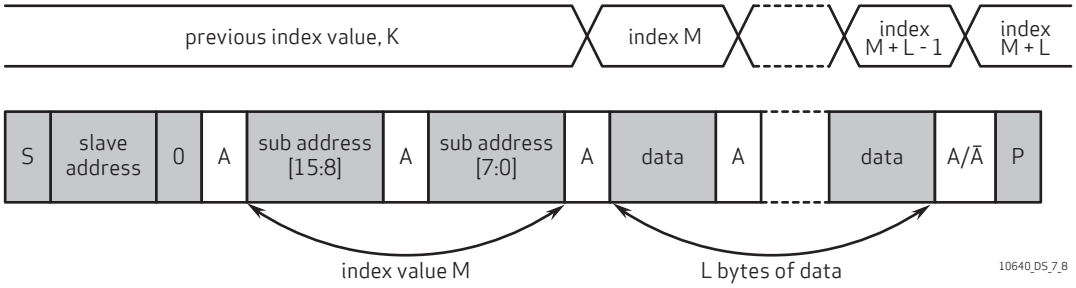
The write operation to a random location is illustrated in **figure 7-7**. The master issues a write operation to the slave, sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 7-7 SCCB single write to random location



The sequential write is illustrated in **figure 7-8**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 7-8 SCCB sequential write to random location

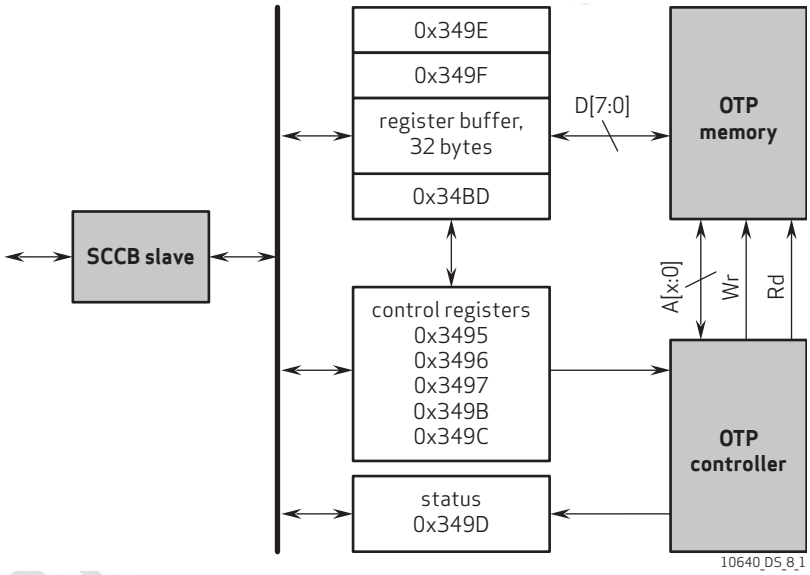


8 OTP memory and temperature sensor

8.1 OTP memory

The OV10640 has an embedded one-time-programmable (OTP) memory, see **figure 8-1**.

figure 8-1 OTP memory diagram



The OTP memory can be programmed through regular SCCB write and then read back through regular SCCB read. The OV10640 has a total of 32 bytes in two banks of OTP memory. Each bank can be accessed by 32 register buffers, 0x349E~0x34AD for bank0 and 0x34AE~0x34BD for bank1. The corresponding bank can be selected through 0x3495[0], where 0 means accessing bank 0, and 1 means accessing bank 1.

The OV10640 OTP memory can only be accessed manually. The manual read and write access is described in **section 8.1.2** and **section 8.1.3**. The manual start address is specified in 0x3496 and the manual end address is specified in 0x3497.

8.1.1 OTP memory access considerations

To guarantee reliable OTP programming, use the power requirements shown below:

- AVDD: 1.8V ± 10%
- DOVDD: 1.8V ± 10%
- PLLDVDD: 1.5V ± 10%
- PLLAVDD: 3.3V ± 200mV
- SVDD: 2.8 ~ 3.5V (used for programming efuse in the OTP)
- DVDD: 1.5V ± 10% (internal DVDD must be used)

All power supplies must be stable before OTP programming (power sequence is not critical in OTP programming stage).

OTP implies each memory bit can be programmed to '1' once only. However, multi-pass programming is allowed as long as NO any single bit is programmed twice.

Programming any bit more than one time may result in unexpected result, e.g. unstable read out value. It may also affect other OTP bits.

The OV10640 does not have auto load function of the OTP memory. The data in OTP memory must be read to register buffers and copied by OV490 or a similar backend processor chip to corresponding sensor register e.g. temperature calibration data, see **section 8.2**.

8.1.2 manual OTP memory read

The data stored in OTP memory can be manually read back though SCCB.

Procedure to read from OTP memory:

1. Clear register buffer 0x349E~0x34AD (Bank 0) or 0x34AE~0x34BD (Bank 1) to 0x00
2. Set 0x3496 to 0x00 and 0x3497 to 0x0F (manual register buffer address range, can be any address in between 0x00- 0x0F)
3. Set 0x3495[0] to 0 or 1 where specifying OTP bank 0 or 1
4. Set 0x349C to 0x01 (read strobe)
5. Wait 25 ms
6. Read OTP values from buffer 0x349E~0x34AD (Bank 0) or 0x34AE~0x34BD (Bank 1)

Example to read OTP memory bank 0:

```
60 349E 00; Clear Buffer, bank 0

60 349F 00

60 34A0 00

…

60 34AD 00

60 3496 00; Manual start buffer address, can be any address between 0x00-0x0F

60 3497 0F; Manual end buffer address, can be any address between 0x00-0x0F

60 3495 40; Manual read mode, specify OTP bank 0

60 349C 01; Read strobe (OTP values will be loaded to registers 0x349E~0x34AD)
```

Example to read memory bank 1:

```
60 34AE 00; Clear Buffer, bank 1

60 349F 00

60 34A0 00
```

…

```
60 34BD 00

60 3496 00; Manual start buffer address, can be any address between 0x00-0x0F

60 3497 0F; Manual end buffer address, can be any address between 0x00-0x0F

60 3495 41; Manual read mode, specify OTP bank 1

60 49C 01; Read strobe (OTP values will be loaded to registers 0x34AE~0x34BD)
```

8.1.3 manual OTP memory program

Data written to register buffer 0x349E~0x34AD will be burned into OTP memory bank 0, data written to register buffer 0x34AE~0x34BD will be burned into OTP memory bank 1. Register 0x3495[0] specifies the OTP memory bank.

Procedure to burn OTP memory content:

1. Follow procedure to read from OTP memory (see **section 8.1.2**) to make sure the OTP memory is empty
2. Write OTP values into register buffer 0x349E~0x34BD
3. Set 0x3496 to 0x00, and 0x3497 to 0x0F (manual register buffer address range, can be any address in between 0x00-0x0F)
4. Set 0x3495[0] to 0 or 1 where specifying OTP bank 0 or 1
5. Set 0x349B to 0x01 (program strobe)

Example to program OTP memory bank 0:

```
60 349E 00; Clear register buffer

60 349F 00

60 34A0 00

...

60 34AD 00

60 3496 00; Manual start buffer address, can be any address between 0x00-0x0F

60 3497 0F; Manual end buffer address, can be any address between 0x00-0x0F

60 3495 40; Manual read mode, specify OTP bank 0

60 349C 01; Read strobe (OTP values will be loaded to registers 0x349E~0x34AD)*

*make sure the buffer is clear, i.e. no data in the subsequent OTP memory

60 3495 00; Non-program state

60 349E 00; Write OTP data to register buffers

60 349F 01

60 34A0 02
```

```
...
60 34AD 0F
60 3496 00; Manual start buffer address, can be any address between 0x00-0x0F
60 3497 0F: Manual end buffer address, can be any address between 0x00-0x0F
60 3495 40; Manual read mode, specify OTP bank 0
60 349D 01; Program strobe
```

The underlined values above are the OTP data that will be programmed into OTP memory.

Example to program OTP memory bank 1:

```
60 34AE 00; Clear register buffer
60 34AF 00
60 34A0 00
...
60 34BD 00
60 3496 00; Manual start buffer address, can be any address between 0x00-0x0F
60 3497 0F; Manual end buffer address, can be any address between 0x00-0x0F
60 3495 41; Manual read mode, specify OTP bank 1
60 349C 01; Read strobe (OTP values will be loaded to registers 0x34AE~0x34BD)*
*make sure the register buffer is clear, i.e. no data in the subsequent OTP memory
60 3495 00; Non-program state
60 349E 00; Write OTP data to register buffers
60 349F 01
60 34A0 02
...
60 34AD 0F
60 3496 00; Manual start buffer address, can be any address between 0x00-0x0F
60 3497 0F: Manual end buffer address, can be any address between 0x00-0x0F
60 3495 41; Manual read mode, specify OTP bank 1
60 349D 01; Program strobe
```

The underlined values above are the OTP data that will be programmed into OTP memory.

8.1.4 OTP memory map

The OTP memory has 32 bytes in 2 banks. Each bank has byte address 0x00-0x0F and accessed through register buffer 0x349E~0x34BD. The OTP memory map is shown in **table 8-1**.

Bank 0 and byte 14 in bank1 is reserved for internal use. The reserved bits are usually used to store production information or used by internal functions.

Byte 0~13 and byte 15 in bank1 is fully user programmable. The programmable bits are usually used to store production tracking information, camera module calibration data, etc.

table 8-1 OTP memory structure

bank	byte address	register buffer	purpose
0	0x00~0x08	0x349E~0x34A6	reserved for OmniVision (9 byte ID)
0	0x09	0x34A7	reserved for OmniVision
0	0x0A	0x34A8	temperature sensor calibration data
0	0x0B	0x34A9	conversion gain
0	0x0C	0x34AA	long K factor
0	0x0D	0x34AB	short K factor
0	0x0E~0x0F	0x34AC~0x34AD	reserved for OmniVision
1	0x00~0x0D	0x34AE~0x34BB	customer area
1	0x0E	0x34BC	reserved for OmniVision
1	0x0F	0x34BD	customer area

table 8-2 OTP control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3493~ 0x3494	RSVD	–	–	Reserved
0x3495	R_MODE_CTRL	0x40	RW	Bit[7]: program_dis 1: Disable programming Bit[6]: mode_select 0: Auto mode 1: Manual mode Bit[5:0]: Memory select Used to choose the exact OTP bank 000000: Select memory 1 000001: Select memory 2 Others: Not used

table 8-2 OTP control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3496	R_START_ADDRESS	0x00	RW	Start Address for Manual Mode
0x3497	R_END_ADDRESS	0x0F	RW	End Address for Manual Mode
0x3498~ 0x349A	RSVD	–	–	Reserved
0x349B	OTP_PROGRAM	0x00	RW	Write 1 to Program Auto Reset
0x349C	OTP_READ	0x00	RW	Write 1 to Read Auto Reset
0x349D	R_OTP_STATUS	–	R	Bit[7:2]: Not used Bit[1]: r_otp_load_o 0: Not used 1: Loading time Bit[0]: r_otp_prog_o 0: Not used 1: Programing time
0x349E	DATA_0	0x00	RW	Register Buffer OTP data_0
0x349F	DATA_1	0x00	RW	Register Buffer OTP data_1
0x34A0	DATA_2	0x00	RW	Register Buffer OTP data_2
0x34A1	DATA_3	0x00	RW	Register Buffer OTP data_3
0x34A2	DATA_4	0x00	RW	Register Buffer OTP data_4
0x34A3	DATA_5	0x00	RW	Register Buffer OTP data_5
0x34A4	DATA_6	0x00	RW	Register Buffer OTP data_6
0x34A5	DATA_7	0x00	RW	Register Buffer OTP data_7
0x34A6	DATA_8	0x00	RW	Register Buffer OTP data_8
0x34A7	DATA_9	0x00	RW	Register Buffer OTP data_9
0x34A8	DATA_A	0x00	RW	Register Buffer OTP data_a
0x34A9	DATA_B	0x00	RW	Register Buffer OTP data_b
0x34AA	DATA_C	0x00	RW	Register Buffer OTP data_c
0x34AB	DATA_D	0x00	RW	Register Buffer OTP data_d
0x34AC	DATA_E	0x00	RW	Register Buffer OTP data_e
0x34AD	DATA_F	0x00	RW	Register Buffer OTP data_f
0x34AE	DATA_10	0x00	RW	Register Buffer OTP data_10
0x34AF	DATA_11	0x00	RW	Register Buffer OTP data_11
0x34B0	DATA_12	0x00	RW	Register Buffer OTP data_12

table 8-2 OTP control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x34B1	DATA_13	0x00	RW	Register Buffer OTP data_13
0x34B2	DATA_14	0x00	RW	Register Buffer OTP data_14
0x34B3	DATA_15	0x00	RW	Register Buffer OTP data_15
0x34B4	DATA_16	0x00	RW	Register Buffer OTP data_16
0x34B5	DATA_17	0x00	RW	Register Buffer OTP data_17
0x34B6	DATA_18	0x00	RW	Register Buffer OTP data_18
0x34B7	DATA_19	0x00	RW	Register Buffer OTP data_19
0x34B8	DATA_1A	0x00	RW	Register Buffer OTP data_1a
0x34B9	DATA_1B	0x00	RW	Register Buffer OTP data_1b
0x34BA	DATA_1C	0x00	RW	Register Buffer OTP data_1c
0x34BB	DATA_1D	0x00	RW	Register Buffer OTP data_1d
0x34BC	DATA_1E	0x00	RW	Register Buffer OTP data_1e
0x34BD	DATA_1F	0x00	RW	Register Buffer OTP data_1f

8.2 temperature sensor

The OV10640 has an embedded temperature sensor to measure junction temperature. This temperature sensor requires a 1-3 MHz clock divided from XVCLK. The temperature monitor is enabled by register 0x3046[4].

The temperature can be read back by register 0x304C. When the value is below 0xC0, the value is the temperature in degrees Celsius. When the value is greater than 0xC0, the temperature is (0x304C) - 0x100 in degrees Celsius.

The slope and offset of the temperature sensor is calibrated in an OmniVision production test and the calibration data is stored in the OTP memory. The calibrated offset value from OTP memory must be manually written to sensor register 0x303C~0x303F by following procedure:

1. The offset value must be loaded from OTP memory and read from register buffer 0x34A8 (see **section 8.1.2**).
2. The default offset value from sensor register 0x303C~0x303F must be read
3. Add the values from step 1 and step 2
4. The resulting calibrated offset value must be written back to sensor offset register 0x303C~0x303F.

After calibration, the accuracy of the temperature reading is ±5 degree Celsius over the operating temperature range. When the temperature is out of the operating temperature range, reading from the temperature sensor is not reliable and is for reference only.

table 8-3 temperature control registers

address	register name	default value	R/W	description
0x303A	TPM_SLOPE_H	0x01	RW	Temperature Slope High Byte
0x303B	TPM_SLOPE_L	0xDE	RW	Temperature Slope Low Byte
0x303C	TPM_OFFSET3	0xDE	RW	Temperature Offset Byte 3
0x303D	TPM_OFFSET2	0xDE	RW	Temperature Offset Byte 2
0x303E	TPM_OFFSET1	0xDE	RW	Temperature Offset Byte 1
0x303F	TPM_OFFSET0	0xDE	RW	Temperature Offset Byte 0
0x3040	TPM_CTRL0	0x71	RW	Bit[6:4]: cnt_bit Bit[3:0]: Clock divider
0x3041	RSVD	–	–	Reserved
0x3042	TPM_CTRL1	0xDE	RW	Bit[7]: mul_div_sel Bit[6]: div_sel Bit[4:0]: shift_bit

9 operating specifications

9.1 absolute maximum ratings

table 9-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-50°C to +125°C
supply voltage (analog)	$V_{DD-3.3}$	4.5V
supply voltage (digital circuit)	$V_{DD-1.5}$	2V
supply voltage (digital I/O + AVDD)	$V_{DD-1.8}$	3V
internal supply voltage (AVDD_LO)	$V_{DD-AVDD\_LO}$	2V
analog I/O (ATEST, VHI)		-0.3V to $V_{DD-3.3}$
all digital I/O		-0.3V to $V_{DD-1.8}$
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

9.2 functional temperature

table 9-2 functional temperature

parameter	range
operating temperature[a]	-40°C to +105°C sensor ambient temperature

a. sensor functions in the operating range; however, some image quality changes may be noticed at the temperature extremes

9.3 DC characteristics

table 9-3 DC characteristics (-40°C < T_J < 125°C)

symbol	parameter	min	typ	max	unit
supply					
$V_{DD-3.3}$	supply voltage (analog)	3.14	3.3	3.47	V
$V_{DD-1.5}$	supply voltage (digital circuit)	1.425	1.5	1.575	V
$V_{DD-1.8}$	supply voltage (digital I/O + AVDD)	1.7	1.8	1.9	V
$I_{DD-3.3}$	active (operating) current[a]		TBD	TBD	mA
$I_{DD-1.5}$			TBD	TBD	mA
$I_{DD-1.8}$			TBD	TBD	mA
$I_{DDS-PWDN-3.3}$[b]	standby current[c]		TBD		µA
$I_{DDS-PWDN-1.5}$			TBD		µA
$I_{DDS-PWDN-1.8}$			TBD		µA
digital inputs (typical conditions: AVDD = 1.8V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[d]	SIOC and SIOD	-0.5	0	.45	V
V_{IH}[c]	SIOC and SIOD	1.05	1.5	1.95	V

a. OmniVision recommends adding an external heat sink

b. standby current without input clock

c. standby current based on room temperature

d. based on DOVDD = 1.8V.

9.4 AC characteristics

table 9-4 AC characteristics (T_A = 25°C, V_{DD-A} = 3.3V, V_{DD-IO} = 1.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth	3		4	MHz
DLE	DC differential linearity error		<0.5		LSB
ILE	DC integral linearity error		<0.5		LSB
	settling time for software reset			<1	ms
	settling time for resolution mode change			1	ms
	settling time for register setting			32	ms

table 9-5 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)	6	24	27	MHz
t_r, t_f	clock input rise/fall time			5	ns

10 mechanical specifications

10.1 physical specifications

figure 10-1 package specifications

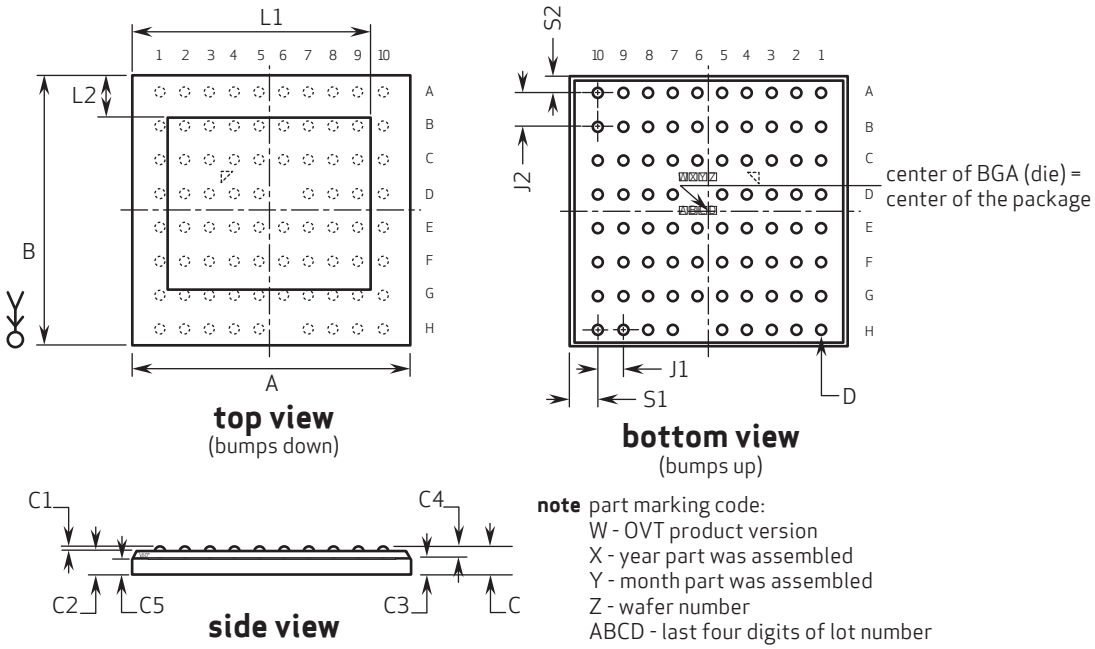


table 10-1 package dimensions (sheet 1 of 2)

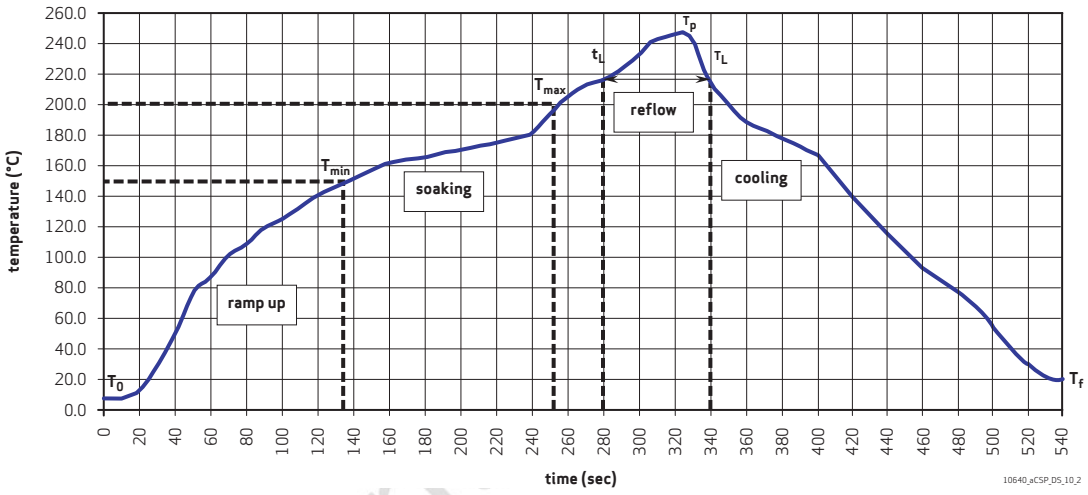
parameter	symbol	min	typ	max	unit
package body dimension x	A	7405	7430	7455	µm
package body dimension y	B	7165	7190	7215	µm
package height	C	700	760	820	µm
pixel to package edge dimension A	L1	6326.81	6361.81	6396.81	µm
pixel to package edge dimension B	L2	1090.155	1125.155	1160.155	µm
ball height	C1	100	130	160	µm
package body thickness	C2	585	630	675	µm
thickness of glass surface to wafer	C3	425	445	465	µm
image plane height	C4	260	315	370	µm

table 10-1 package dimensions (sheet 2 of 2)

parameter	symbol	min	typ	max	unit
glass thickness	C5	390	400	410	µm
ball diameter	D	220	250	280	µm
total pin count	N		78		
pin count x-axis	N1		10		
pin count y-axis	N2		8		
pins pitch x-axis	J1		660		µm
pins pitch y-axis	J2		900		µm
edge-to-pin center distance along x	S1	715	745	775	µm
edge-to-pin center distance along y	S2	415	445	475	µm
air gap between die and glass		40	45	50	µm
tilt between die and glass				0.2	degree
die rotation				0.1	degree

10.2 IR reflow specifications

figure 10-2 IR reflow ramp rate requirements



note
The OV10640 uses a lead free package.

table 10-2 reflow conditions[ab]

zone	description	exposure
ramp up A (T_0 to T_{min})	heating from room temperature to 150°C	temperature slope ≤ 3°C per second
soaking	heating from 150°C to 200°C	90 ~ 150 seconds
ramp up B (t_L to T_P)	heating from 217°C to 245°C	temperature slope ≤ 3°C per second
peak temperature	maximum temperature in SMT	245°C +0/-5°C (duration max 30 sec)
reflow (t_L to T_L)	temperature higher than 217°C	30 ~ 120 seconds
ramp down A (T_P to T_L)	cooling from 245°C to 217°C	temperature slope ≤ 3°C per second
ramp down B (T_L to T_f)	cooling from 217°C to room temperature	temperature slope ≤ 2°C per second
T_0 to T_P	room temperature to peak temperature	≤ 8 minutes

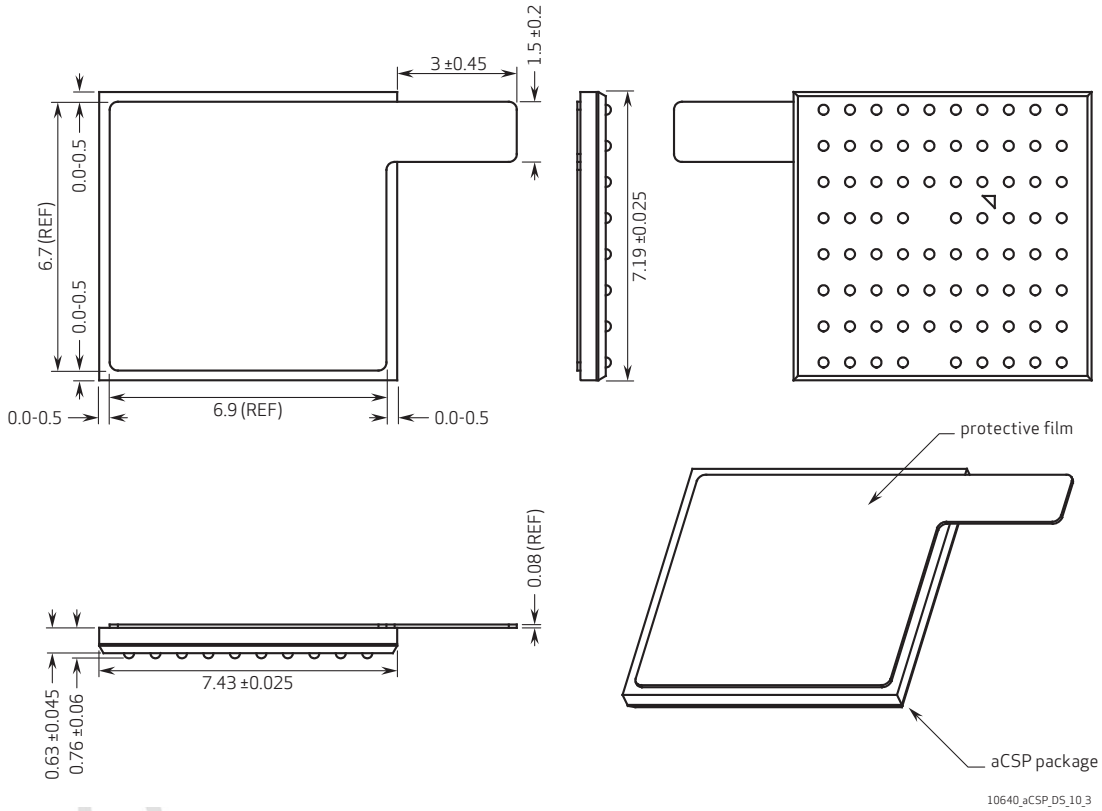
a. maximum number of reflow cycles = 3

b. N2 gas reflow or control O2 gas PPM<500 as recommendation

note
OmniVision recommends aCSP packages use underfill as part of camera assembly process.

10.3 protective film specifications

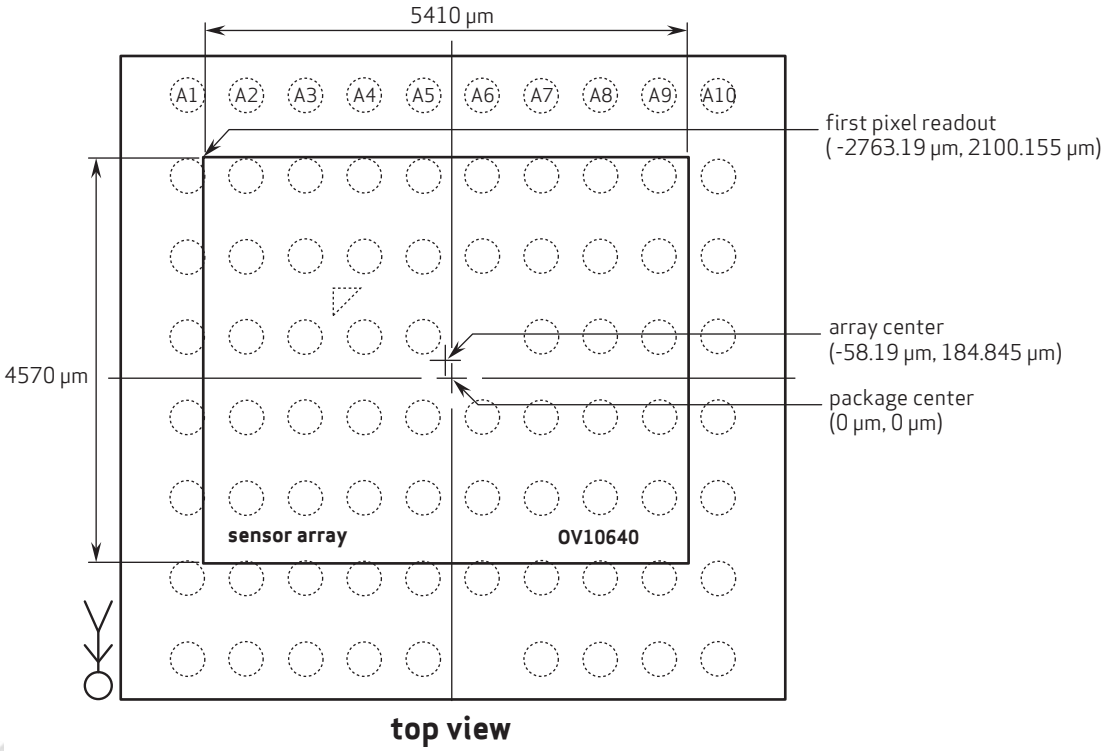
figure 10-3 protective film specifications



11 optical specifications

11.1 sensor array center

figure 11-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pin A1 oriented down on the PCB.

10640_aCSP_DS_11_1

11.2 lens chief ray angle (CRA)

figure 11-2 chief ray angle (CRA)

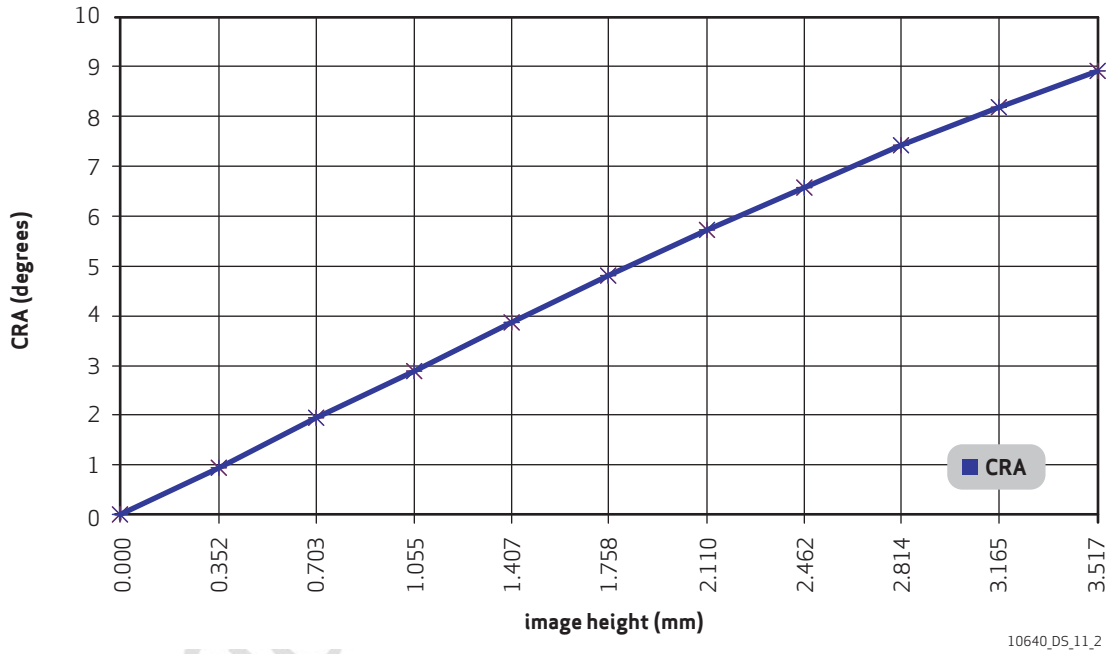


table 11-1 CRA versus image height plot

field (%)	image height (mm)	CRA (degrees)
0.00	0.000	0.00
0.10	0.352	0.99
0.20	0.703	1.98
0.30	1.055	2.95
0.40	1.407	3.91
0.50	1.758	4.85
0.60	2.110	5.76
0.70	2.462	6.63
0.80	2.814	7.46
0.90	3.165	8.24
1.00	3.517	8.95

appendix A register table

The following table provides a description of the device control registers contained in the OV10640. The 8-bit SCCB slave device address is 0x60, three bits in the device address can come from GPIO[2:0], which is controlled by 0x300C[0]. The address will be latched from GPIO on first clock after RESET goes high.

table A-1 sensor control registers (sheet 1 of 80)

address	register name	default value	R/W	description
0x3000	SCLK_PLL_PRE	0x03	RW	SCLK PLL Pre Divider
0x3001	SCLK_PLL_MULT	0x62	RW	SCLK PLL Multiplier
0x3002	SCLK_PLL_POST	0x07	RW	SCLK PLL Post Divider (1-16)
0x3003	SCLK_PLL_CONFIG	0x01	RW	Bit[7:3]: Not used Bit[2:0]: Charge pump current
0x3004	PCLK_PLL_PRE	0x03	RW	PCLK PLL Pre Divider
0x3005	PCLK_PLL_MULT	0x62	RW	PCLK PLL Multiplier (1-128)
0x3006	PCLK_PLL_POST	0x07	RW	PCLK PLL Post Divider (1-16)
0x3007	PCLK_PLL_CTRL	0x01	RW	Bit[7:3]: Not used Bit[2]: pclk_pll_mipi_dis Disable MIPI clock output Bit[1]: pclk_pll_mipidiv2 Divide frequency to MIPI/LVDS by 2 Bit[0]: pclk_pll_enable Enable PLL2
0x3008~ 0x3009	RSVD	–	–	Reserved
0x300A	CHIP_ID_H	0xA6	R	Chip ID High Byte
0x300B	CHIP_ID_L	0x40	R	Chip ID Low Byte
0x300C	SCCB_ID	0x60	RW	Bit[7:1]: sccb_id_n Bit[0]: sccb_id_sel 0: {sccb_id[7:4], gpio_i[3:1]} 1: sccb_id[7:1]
0x300D	SUB_ID	0xB4	RW	Bit[7:0]: Chip subversion ID
0x300E~ 0x300F	RSVD	–	–	Reserved
0x3010	MAN_ID_H	0x7F	R	Manufacturer ID
0x3011	MAN_ID_L	0xA2	R	Manufacturer ID

table A-1 sensor control registers (sheet 2 of 80)

address	register name	default value	R/W	description
0x3012	SOFTWARE_CTRL1	0x00	RW	Bit[7:1]: Reserved Bit[0]: sfw_stb 0: Software standby 1: Streaming
0x3013	SOFTWARE_CTRL2	0x00	RW	Bit[7:1]: Not used Bit[0]: Software reset
0x3014	PWUP_CTRL	0x00	RW	Bit[7:2]: Not used Bit[1]: early_ana 0: Turn analog off in software standby 1: Turn analog on in software standby Bit[0]: early_pl 0: Turn PLL off in software standby 1: Turn PLL on in software standby
0x3015~ 0x301D	RSVD	–	–	Reserved
0x301E	MIPI_CTRL1	0x00	RW	Bit[7:6]: skew_clk Bit[5]: Reserved Bit[4]: dis_clk_ane Bit[3:0]: dis_d_lane
0x301F	MIPI_D_SKEW	0x00	RW	Bit[7:6]: skew_d3 Bit[5:4]: skew_d2 Bit[3:2]: skew_d1 Bit[1:0]: skew_d0
0x3020	MIPI_CTRL2	0x00	RW	Bit[7:3]: Not used Bit[2:0]: slew_rate
0x3021	MIPI_CTRL3	0x00	RW	Bit[7:6]: Not used Bit[5:4]: Ictl IVREF input bias current control Bit[3:0]: bgr_vref
0x3022	RSVD	–	–	Reserved

table A-1 sensor control registers (sheet 3 of 80)

address	register name	default value	R/W	description
0x3023	DVP_PWR	0x00	RW	Bit[7:6]: Not used Bit[5]: pwdn_out Drive value during power down for D[11:0], HREF, VSYNC, and PCLK Bit[4]: pwdn_oe Drive enable during power down for D[11:0], HREF, VSYNC, and PCLK Bit[3:2]: pclk_pwr Drive strength for PCLK when active Bit[1:0]: d_pwr Drive strength for D[11:0], HREF, and VSYNC pins when active
0x3024	GPIO_OE	0x00	RW	GPIO Output Enable
0x3025	GPIO_OUT	0x00	RW	GPIO Output Value
0x3026	GPIO_CTRL	0x04	RW	Bit[7:3]: Not used Bit[2]: GPIO input enable Must be 1 for GPIO in to be valid Bit[1:0]: Power Driving strength for GPIO pads
0x3027	GPIO_IN	–	R	GPIO Input Value
0x3028	GROUP_LENGTH0	0x40	RW	Number of Registers for Group 0, Total Sum of Four Groups is Limited to 256
0x3029	GROUP_LENGTH1	0x40	RW	Number of Registers for Group 1
0x302A	GROUP_LENGTH2	0x40	RW	Number of Registers for Group 2
0x302B	GROUP_LENGTH3	0x40	RW	Number of Registers for Group 3

table A-1 sensor control registers (sheet 4 of 80)

address	register name	default value	R/W	description
0x302C	GROUP_CTRL	0x03	RW	Bit[7]: Not used Bit[6]: launch_now Launch immediately, when single start is set Bit[5]: launch_pre_sof Launch before sensor core SOF, if single start is set Bit[4]: launch_post_sof Launch after sensor core SOF, if single start is set Bit[3:2]: first_grp_sel Main group select for hold and launch operation. Also used as the first group in auto mode. 00: Group select 0 01: Group select 1 10: Group select 2 11: Group select 3 Bit[1:0]: second_grp_sel Used as second group in auto mode
0x302D	FIRST_GRP_FRAMES	0x01	RW	Frames for Staying in Group Selected by First Grp Sel (Number of Frames = Register Value -1)
0x302E	SECOND_GRP_FRAMES	0x01	RW	Frames for Staying in Group Selected by Second Grp Sel (Number of Frames = Register Value -1)
0x302F	OPERATION_CTRL	0x02	RW	Bit[7:2]: Not used Bit[1]: auto_mode Switches automatically between first and second groups using frame counts Bit[0]: single_start Launch only once, reset by logic after done, overridden by auto mode
0x3030	EMB_START_ADDR0_H	0x30	RW	Bit[7:0]: First embedded data range 0[15:8]
0x3031	EMB_START_ADDR0_L	0x00	RW	Bit[7:0]: First embedded data range 0[7:0]
0x3032	EMB_END_ADDR0_H	0x35	RW	Bit[7:0]: Last embedded data range 0[15:8]
0x3033	EMB_END_ADDR0_L	0x00	RW	Bit[7:0]: Last embedded data range 0[7:0]
0x3034	EMB_START_ADDR1_H	0x40	RW	Bit[7:0]: First embedded data range 1[15:8] Change to FF if not used
0x3035	EMB_START_ADDR1_L	0x00	RW	Bit[7:0]: First embedded data range 1[7:0] Change to FF if not used

table A-1 sensor control registers (sheet 5 of 80)

address	register name	default value	R/W	description
0x3036	EMB_END_ADDR1_H	0x42	RW	Bit[7:0]: Last embedded data range 1[15:8]
0x3037	EMB_END_ADDR1_L	0x00	RW	Bit[7:0]: Last embedded data range 1[7:0]
0x3038	ACTIVE_GROUP_NR	–	R	Indicates Which Group is Active
0x3039	FRAME_CNT_ACTIVE	–	R	Number of Frames with the Current Group Valid Only in Auto Mode
0x303A	TPM_SLOPE_H	0x01	RW	Temperature Slope High Byte
0x303B	TPM_SLOPE_L	0xDE	RW	Temperature Slope Low Byte
0x303C	TPM_OFFSET3	0xDE	RW	Temperature Offset Byte 3
0x303D	TPM_OFFSET2	0xDE	RW	Temperature Offset Byte 2
0x303E	TPM_OFFSET1	0xDE	RW	Temperature Offset Byte 1
0x303F	TPM_OFFSET0	0xDE	RW	Temperature Offset Byte 0
0x3040	TPM_CTRL0	0x71	RW	Bit[7]: Not used Bit[6:4]: cnt_bit Bit[3:0]: Clock divider
0x3041	RSVD	–	–	Reserved
0x3042	TPM_CTRL1	0xDE	RW	Bit[7]: mul_div_sel Bit[6]: div_sel Bit[5]: Not used Bit[4:0]: shift_bit
0x3043~ 0x3045	RSVD	–	–	Reserved
0x3046	A_TPM	0x00	RW	Bit[7:5]: Not used Bit[4]: a_tpm_en_n 0: Enables temperature monitor Bit[3:0]: Reserved
0x3047~ 0x304B	RSVD	–	–	Reserved
0x304C	TPM_02	–	R	Bit[7:0]: Sensor junction temperature <0xC0: (0x304C) >0xC0: (0x304C) - 0x100
0x304D~ 0x304E	RSVD	–	–	Reserved
0x305E	ASP_REGA	0x16	RW	Bit[7]: Not used Bit[6]: Color bar overlay swap Bit[5]: Color bar overlay enable Bit[4:0]: Reserved

table A-1 sensor control registers (sheet 6 of 80)

address	register name	default value	R/W	description
0x305F	ASP_REGB	0x18	RW	Bit[7:4]: Reserved Bit[3:0]: Color bar intensity
0x3074	CROP_H_ST_H	0x00	RW	Start Address Horizontal High Byte
0x3075	CROP_H_ST_L	0x00	RW	Start Address Horizontal Low Byte
0x3076	CROP_V_ST_H	0x00	RW	Start Address Vertical High Byte
0x3077	CROP_V_ST_L	0x02	RW	Start Address Vertical Low Byte
0x3078	CROP_H_END_H	0x05	RW	End Address Horizontal High Byte
0x3079	CROP_H_END_L	0x07	RW	End Address Horizontal Low Byte
0x307A	CROP_V_END_H	0x04	RW	End Address Vertical High Byte
0x307B	CROP_V_END_L	0x41	RW	End Address Vertical Low Byte
0x307C	DVP_H_SIZE_H	0x05	RW	DVP Horizontal Size High Byte
0x307D	DVP_H_SIZE_L	0x08	RW	DVP Horizontal Size Low Byte
0x307E	DVP_V_SIZE_H	0x04	RW	DVP Vertical Size High Byte
0x307F	DVP_V_SIZE_L	0x44	RW	DVP Vertical Size Low Byte
0x3080	HTS_H	0x05	RW	Line Length High Byte
0x3081	HTS_L	0xC4	RW	Line Length Low Byte
0x3082	VTS_H	0x04	RW	Frame Length High Byte
0x3083	VTS_L	0x52	RW	Frame Length Low Byte
0x3084	WIN_HOFFS_H	0x00	RW	win_hoffs High Byte
0x3085	WIN_HOFFS_L	0x00	RW	win_hoffs Low Byte
0x3086	WIN_VOFFS_H	0x00	RW	win_voffs High Byte
0x3087	WIN_VOFFS_L	0x00	RW	win_voffs Low Byte
0x308A	EXTRA_DELAY_H	0x00	RW	(fs_delay) Last Row can be Extended by this Number of Clocks High Byte
0x308B	EXTRA_DELAY_L	0x00	RW	(fs_delay) Last Row can be Extended by this Number of Clocks Low Byte

table A-1 sensor control registers (sheet 7 of 80)

address	register name	default value	R/W	description
0x308C	SENSOR_CTRL	0x01	RW	Bit[7]: use_r_rst_num Bit[6]: fsin_intr_en When high, external input can generate interrupt when FSIN arrives Bit[5]: fsin_retro_mode When high, makes FSIN logic work Bit[4]: fsin_en When high, FSIN mode is enabled Bit[3]: low_power_mode When high, sensor will not read exposures that are disabled (single or 2 expo) Bit[2]: Not used Bit[1]: adc_swap_en When high, enables swapping of ADCs Bit[0]: extra_ctrl When high, extra delays will be reset when used once
0x308D	ROW_ADDR_CTRL	0x92	RW	Bit[7:6]: row_black_count 00: 2 rows 01: 4 rows 10: 8 rows 11: Invalid Bit[4:0]: row_first_active Array row address of first active row
0x308E	COL_ADDR_END	0xFF	RW	End Address for Column Memory Read
0x308F	SKIP_CTRL	0x00	RW	Bit[7:4]: seq_var Sequencer program variation bits Bit[2]: Monochrome Monochrome readout mode Bit[1]: Vsub2 Skip 2/2 rows, or 1/1 rows in monochrome Bit[0]: Hsub2 Skip 2/2 columns, or 1/1 columns in monochrome

table A-1 sensor control registers (sheet 8 of 80)

address	register name	default value	R/W	description
0x3090	READ_MODE	0x00	RW	Bit[7:5]: hdr_mode 000: hdr_3exp 001: s_2exp 010: lvs_2exp 011: l_1exp 100: Reserved Others: Not used Bit[4]: Not used Bit[3]: Flip Bit[2]: Mirror Bit[1:0]: Not used
0x3091	READ_CTRL	0x0C	RW	Bit[7:5]: Reserved Bit[4]: unaligned_mode Bit[3]: show_stats_rows Bit[2]: show_embedded_rows Bit[1]: Reserved Bit[0]: Not used
0x3092~ 0x3095	RSVD	–	–	Reserved
0x3096	EXPOSURE_LONG_H	–	R	Frame Long Exposure (in Rows) High Byte
0x3097	EXPOSURE_LONG_L	–	R	Frame Long Exposure (in Rows) Low Byte
0x3098	EXPOSURE_SHORT_H	–	R	Frame Short Exposure (in Rows) High Byte
0x3099	EXPOSURE_SHORT_L	–	R	Frame Short Exposure (in Rows) Low Byte
0x309A	EXPOSURE_VERY_ SHORT	–	R	Frame Very Short Exposure (in Rows) Last five bits mean fraction
0x309B	CG_AGAIN_USE	–	R	Bit[7]: cg_vs 0: Short CG 1: Not used Bit[6]: cg_l 0: Long CG 1: Not used Bit[5:4]: again_vs 00: Very short again 01: Not used 1x: Not used Bit[3:2]: again_s 00: Short again 01: Not used 1x: Not used Bit[1:0]: again_l 00: Long again 01: Not used 1x: Not used

table A-1 sensor control registers (sheet 9 of 80)

address	register name	default value	R/W	description
0x309C	FCNT_3	–	R	fcnt Byte 3
0x309D	FCNT_2	–	R	fcnt Byte 2
0x309E	FCNT_1	–	R	fcnt Byte 1
0x309F	FCNT_0	–	R	fcnt Byte 0
0x30A0~ 0x30A3	RSVD	–	–	Reserved
0x30A4	EXTRA_VTS	0x00	RW	extra_vts
0x30A5~ 0x30B1	RSVD	–	–	Reserved
0x30B9	BLC_CTRL	0x22	RW	Bit[7]: Not used Bit[6]: show_dark_cols Bit[5]: Not used Bit[4]: blc_override_en Bit[3]: blc_cont_update_mode Bit[2]: blc_stretch_en Bit[1]: blc_dither_en Bit[0]: show_dark_rows
0x30BA	BLC_SMOOTHING	0x07	RW	Filter Coefficient Alpha = (smoothing+1)/32 If zero, new value is not used.
0x30BB	D_VALUE_LARGE	0x00	RW	Signed Fractional (/64) Value Between -32/64 and 32/64 to adjust DL'=DL(1+D)
0x30BC	D_VALUE_SMALL	0x00	RW	d_value_small
0x30BD	BLC_OVERRIDE_L_H	0x00	RW	blc_override_l High Byte
0x30BE	BLC_OVERRIDE_L_L	0x00	RW	blc_override_l Low Byte
0x30BF	BLC_OVERRIDE_S_H	0x00	RW	blc_override_s High Byte
0x30C0	BLC_OVERRIDE_S_L	0x00	RW	blc_override_s Low Byte
0x30C1	BLC_OVERRIDE_VS_H	0x00	RW	blc_override_vs High Byte
0x30C2	BLC_OVERRIDE_VS_L	0x00	RW	blc_override_vs Low Byte
0x30C3	BLC_TARGET_L_H	0x00	RW	blc_target_l High Byte
0x30C4	BLC_TARGET_L_L	0x80	RW	blc_target_l Low Byte
0x30C5	BLC_TARGET_S_H	0x00	RW	blc_target_s High Byte
0x30C6	BLC_TARGET_S_L	0x80	RW	blc_target_s Low Byte
0x30C7	BLC_TARGET_VS_H	0x00	RW	blc_target_vs High Byte

table A-1 sensor control registers (sheet 10 of 80)

address	register name	default value	R/W	description
0x30C8	BLC_TARGET_VS_L	0x80	RW	blc_target_vs Low Byte
0x30C9	BLC_TRIGGER	0x1C	RW	Bit[7:5]: Not used Bit[4]: blc_exp_changed_trig_en Bit[3]: blc_gain_changed_trig_en Bit[2]: blc_restart_frame_trig_en Bit[1]: blc_hard_trigger_en Bit[0]: blc_manual_trig
0x30CA	BLC_TRIGGER_ THRESHOLD_L	0x10	RW	blc_trigger_threshold_l
0x30CB	BLC_TRIGGER_ THRESHOLD_S	0x10	RW	blc_trigger_threshold_s
0x30CC	BLC_TRIGGER_ THRESHOLD_VS	0x10	RW	blc_trigger_threshold_vs
0x30CD	RESTART_FRAMES	0x01	RW	Number of Frames with Continuous Update After Restart
0x30CE	HOT_THRESHOLD	0x40	RW	Threshold for Setting the "Hot" Flag to Auto Exposure
0x30CF	AB_CTRL	0x00	RW	Bit[7:2]: Not used Bit[1]: Bframe Bit[0]: ab_mode
0x30D0	DARK_CURRENT_L_H	–	R	dark_current_l High Byte
0x30D1	DARK_CURRENT_L_L	–	R	dark_current_l Low Byte
0x30D2	DARK_CURRENT_S_H	–	R	dark_current_s High Byte
0x30D3	DARK_CURRENT_S_L	–	R	dark_current_s Low Byte
0x30D4	DARK_CURRENT_VS_H	–	R	dark_current_vs High Byte
0x30D5	DARK_CURRENT_VS_L	–	R	dark_current_vs Low Byte
0x30D6	ROW_AVERAGE_L_H	–	R	row_average_l High Byte
0x30D7	ROW_AVERAGE_L_L	–	R	row_average_l Low Byte
0x30D8	ROW_AVERAGE_S_H	–	R	row_average_s High Byte
0x30D9	ROW_AVERAGE_S_L	–	R	row_average_s Low Byte
0x30DA	ROW_AVERAGE_VS_H	–	R	row_average_vs High Byte
0x30DB	ROW_AVERAGE_VS_L	–	R	row_average_vs Low Byte
0x30DC	DIG_GAIN_L_H	–	R	Digital Gain for L Exposure High Byte
0x30DD	DIG_GAIN_L_L	–	R	Digital Gain for L Exposure Low Byte

table A-1 sensor control registers (sheet 11 of 80)

address	register name	default value	R/W	description
0x30DE	DIG_GAIN_S_H	–	R	Digital Gain for S Exposure High Byte
0x30DF	DIG_GAIN_S_L	–	R	Digital Gain for S Exposure Low Byte
0x30E0	DIG_GAIN_VS_H	–	R	Digital Gain for VS Exposure High Byte
0x30E1	DIG_GAIN_VS_L	–	R	Digital Gain for VS Exposure Low Byte
0x30E4~ 0x30E5	RSVD	–	–	Reserved
0x30E6	EXPO_L_H	0x00	RW	Long Exposure High Byte
0x30E7	EXPO_L_L	0x40	RW	Long Exposure Low Byte
0x30E8	EXPO_S_H	0x00	RW	Short Exposure High Byte
0x30E9	EXPO_S_L	0x40	RW	Short Exposure Low Byte
0x30EA	EXPO_VS	0x20	RW	Very Short Exposure Last five bits means fraction
0x30EB	CG_AGAIN	0x00	RW	Bit[7]: Very short CG 0: Low CG 1: High CG Bit[6]: Long CG 0: Low CG 1: High CG Bit[5:4]: Very short again 00: x1 01: x2 10: x4 11: x8 Bit[3:2]: Short again 00: x1 01: x2 10: x4 11: x8 Bit[1:0]: Long again 00: x1 01: x2 10: x4 11: x8
0x30EC	DGAIN_L_H	0x01	RW	Bit[7:6]: Not used Bit[5:0]: Long dgain[13:8] (integer)
0x30ED	DGAIN_L_L	0x00	RW	Bit[7:0]: Long dgain[7:0] (fraction)
0x30EE	DGAIN_S_H	0x01	RW	Bit[7:6]: Not used Bit[5:0]: Short dgain[13:8] (integer)
0x30EF	DGAIN_S_L	0x00	RW	Bit[7:0]: Short dgain[7:0] (fraction)

table A-1 sensor control registers (sheet 12 of 80)

address	register name	default value	R/W	description
0x30F0	DGAIN_VS_H	0x01	RW	Bit[7:6]: Not used Bit[5:0]: Very short dgain[13:8] (integer)
0x30F1	DGAIN_VS_L	0x00	RW	Bit[7:0]: Very short dgain[7:0] (fraction)
0x30F2	AEC_ROW_START_H	0x00	RW	ROI Setting
0x30F3	AEC_ROW_START_L	0x04	RW	ROI Setting
0x30F4	AEC_COL_START_H	0x00	RW	ROI Setting
0x30F5	AEC_COL_START_L	0x00	RW	ROI Setting
0x30F6	AEC_ROW_STOP_H	0x04	RW	ROI Setting
0x30F7	AEC_ROW_STOP_L	0x30	RW	ROI Setting
0x30F8	AEC_COL_STOP_H	0x04	RW	ROI Setting
0x30F9	AEC_COL_STOP_L	0xFF	RW	ROI Setting
0x30FA	HDR_AEC_CTRL	0x06	RW	Bit[7]: data_select AEC data select 0: ISP input 1: DNS output Bit[6]: aec_enable AEC enable (automatic mode) Bit[5]: ec_enable EC enable (outputs EV and processes EV independently) Bit[4]: hdr_stats_en HDR/12-bit select Bit[3:0]: Bayer mask setting
0x30FB	PDRATIO_H	0x0E	RW	Pin Diode Ratio High Byte
0x30FC	PDRATIO_L	0x00	RW	Pin Diode Ratio Low Byte
0x30FD	CG_RATIO_H	0x08	RW	CG Ratio High Byte
0x30FE	CG_RATIO_L	0x00	RW	CG Ratio Low Byte
0x30FF~ 0x3104	RSVD	–	–	Reserved
0x3105	REAL_GAIN_L_H	–	R	Long Digital × Analog Gain High Byte
0x3106	REAL_GAIN_L_L	–	R	Long Digital × Analog Gain Low Byte
0x3107	REAL_GAIN_S_H	–	R	Short Digital × Analog Gain High Byte
0x3108	REAL_GAIN_S_L	–	R	Short Digital × Analog Gain Low Byte
0x3109	REAL_GAIN_VS_H	–	R	Very Short Digital × Analog Gain High Byte

table A-1 sensor control registers (sheet 13 of 80)

address	register name	default value	R/W	description
0x310A	REAL_GAIN_VS_L	–	R	Very Short Digital × Analog Gain Low Byte
0x310B	RATIO_LS_H	–	R	Long to Short Ratio High Byte
0x310C	RATIO_LS_L	–	R	Long to Short Ratio Low Byte
0x310D	RATIO_LVS_H	–	R	Long to Very Short Ratio High Byte
0x310E	RATIO_LVS_L	–	R	Long to Very Short Ratio Low Byte
0x310F	RATIO_SVS_H	–	R	Short to Very Short Ratio High Byte
0x3110	RATIO_SVS_L	–	R	Short to Very Short Ratio Low Byte
0x3111	D_EV_L_3	–	R	Longest EV Byte 3
0x3112	D_EV_L_2	–	R	Longest EV Byte 2
0x3113	D_EV_L_1	–	R	Longest EV Byte 1
0x3114	D_EV_L_0	–	R	Longest EV Byte 0
0x3115	D_EV_S_3	–	R	Shortest EV Byte 3
0x3116	D_EV_S_2	–	R	Shortest EV Byte 2
0x3117	D_EV_S_1	–	R	Shortest EV Byte 1
0x3118	D_EV_S_0	–	R	Shortest EV Byte 0
0x3119	INTERFACE_CTRL	0x0C	RW	Bit[7]: Not used Bit[6]: no_comp When high, single 12-bit data are sent without compression Bit[5:4]: int_mode 00: DVP 01: MIPI 10: LVDS 11: Not used Bit[3]: auto_sel When data width in modes 12_l, 12_s and 12_vs, auto select (L versus VS) when in 2x12 mode 0: Normal mode 1: Auto select Bit[2:0]: data_width 000: 3x12 001: 2x12 010: 20 011: 16 100: 12 comb Others: Unprocessed L, S and VS

table A-1 sensor control registers (sheet 14 of 80)

address	register name	default value	R/W	description
0x311B	VFIFO_READ_LEVEL_L	0x10	RW	VFIFO Ready Level Low Byte
0x311C	VSYNC_WIDTH_LINE_H	0x00	RW	Bit[7:0]: VSYNC width by line number[15:8]
0x311D	VSYNC_WIDTH_LINE_L	0x00	RW	Bit[7:0]: VSYNC width by line number[7:0]
0x311E	VSYNC_WIDTH_PIXEL_H	0x02	RW	Bit[7:0]: VSYNC width by pixel number[15:8]
0x311F	VSYNC_WIDTH_PIXEL_L	0x00	RW	Bit[7:0]: VSYNC width by pixel number[7:0]
0x3120	VSYNC_DELAY_H	0x00	RW	Bit[7:0]: VSYNC delay count[23:16]
0x3121	VSYNC_DELAY_M	0x01	RW	Bit[7:0]: VSYNC delay count[15:8]
0x3122	VSYNC_DELAY_L	0x00	RW	Bit[7:0]: VSYNC delay count[7:0]
0x3123	POLARITY_CTRL	0x00	RW	Bit[7]: Clock DDR mode enable Bit[6]: Reverse bit polarity Bit[5]: vsync_gate_clk_enable Bit[4]: href_gate_clk_enable Bit[3]: no_frst_for_fifo Bit[2]: href_polarity Bit[1]: vsync_polarity Bit[0]: pclk_polarity
0x3124	TEST_ORDER	0x00	RW	Bit[7]: fifo_bypass_mode Bit[6:4]: data_bit_swap 000: [11:0] 001: [0:11] 010: [2:11], [1:0] 011: [4:11], [3:0] 100: [9:0], [11:10] 101: [7:0], [11:8] 110: [1:0], [11:2] 111: [3:0], [11:4] Bit[3]: test_mode Bit[2]: test_bit10 Bit[1]: test_bit8 Bit[0]: test_enable
0x3125	BYP_SELECT	0x00	RW	Bit[7]: Not used Bit[6]: Bypass select Bit[5]: data_bit_shift Bit[4]: href_sel Bit[3:0]: bypass_sel
0x3126	R_FIFO	0x00	RW	Top Sync FIFO Control

table A-1 sensor control registers (sheet 15 of 80)

address	register name	default value	R/W	description
0x3127	R_ISP_CTRL_0	0x7B	RW	Bit[7]: Not used Bit[6]: isp_crop_en (active high) ISP output window crop enable Bit[5]: hdr_dpc_en DPC enable Bit[4]: scip_en Simple interpolation enable Bit[3]: hdr_dns_en HDR RAW DNS enable Bit[2]: lenc_en LENC enable Bit[1]: awb_gain_en WB gain enable Bit[0]: isp_enable ISP enable
0x3128	R_ISP_CTRL_2	0x00	RW	Bit[7]: sram_man_ctrl_en HDR buffer manual control enable Bit[6]: sram_man_mode HDR buffer manual mode Bit[5:2]: Not used Bit[1:0]: cfa_pattern Used with mirror/flip offset register 0x3291[2:1] 00: No mirror/flip 01: Mirror 10: Flip 11: Mirror and flip
0x3129	R_PRE_CTRL0	0x00	RW	Bit[7]: test_mode_en Pre_ISP test mode enable Bit[6]: rolling_lines Pre_ISP rolling lines enable Bit[5]: transparent_mode Pre_ISP transparent mode enable Bit[4]: Reserved Bit[3:2]: color_bar Pre_ISP color bar style Bit[1:0]: img_sel Pre_ISP test image select
0x312A	R_PRE_CTRL1	0x11	RW	Bit[7:6]: Not used Bit[5:3]: ls_exp_ratio Pre_ISP long/short exposure pixel value ratio Bit[2:0]: svs_exp_ratio Pre_ISP short/vshort exposure pixel value ratio

table A-1 sensor control registers (sheet 16 of 80)

address	register name	default value	R/W	description
0x312B	R_PRE_CTRL2	0x01	RW	Bit[7]: Not used Bit[6]: reset_flag_sel Non-first frame flag reset select 0: Logic reset 1: Power on reset Bit[5]: Test Pre_ISP test, low byte to 0 Bit[4:0]: Reserved
0x312C	R_PRE_CTRL3	0x00	RW	Pre_ISP Line Interrupt Number High Byte
0x312D	R_PRE_CTRL4	0x13	RW	Pre_ISP Line Interrupt Number Low Byte
0x312E	R_PRE_CTRL5	–	R	Pre_ISP Read Out Actual Pixel Number of a Line High Byte
0x312F	R_PRE_CTRL6	–	R	Pre_ISP Read Out Actual Pixel Number of a Line Low Byte
0x3130	R_PRE_CTRL7	–	R	Pre_ISP Read Out Actual Line Number of a Frame High Byte
0x3131	R_PRE_CTRL8	–	R	Pre_ISP Read Out Actual Line Number of a Frame Low Byte
0x3132	R_COMBINE_CTRL	0x3C	RW	Bit[7:5]: n_step Bit[4]: auto_ct_enable Bit[3]: S channel pre matrix enable Bit[2]: Compensate error enable Bit[1:0]: Combine work mode 00: HDRCombine enable 01: Not used 1x: Not used
0x3133	R_COMBINE_THRE_0	0x95	RW	Combine Threshold [0] Bit[7:4]: Long Bit[3:0]: Short
0x3134	R_COMBINE_THRE_1	0xA8	RW	Combine Threshold [1] Bit[7:4]: Long Bit[3:0]: Short
0x3135	R_COMBINE_THRE_2	0xAA	RW	Combine Threshold [2] Bit[7:4]: Long Bit[3:0]: Short
0x3136	R_COMBINE_WEIGHT_0_0	0x80	RW	Combine Weight [0][0]
0x3137	R_COMBINE_WEIGHT_0_1	0x80	RW	Combine Weight [0][1]
0x3138	R_COMBINE_WEIGHT_0_2	0x60	RW	Combine Weight [0][2]

table A-1 sensor control registers (sheet 17 of 80)

address	register name	default value	R/W	description
0x3139	R_COMBINE_WEIGHT_0_3	0x40	RW	Combine Weight [0][3]
0x313A	R_COMBINE_WEIGHT_1_0	0x80	RW	Combine Weight [1][0]
0x313B	R_COMBINE_WEIGHT_1_1	0x80	RW	Combine Weight [1][1]
0x313C	R_COMBINE_WEIGHT_1_2	0x40	RW	Combine Weight [1][2]
0x313D	R_COMBINE_WEIGHT_1_3	0x20	RW	Combine Weight [1][3]
0x313E	R_COMBINE_WEIGHT_2_0	0x80	RW	Combine Weight [2][0]
0x313F	R_COMBINE_WEIGHT_2_1	0x60	RW	Combine Weight [2][1]
0x3140	R_COMBINE_WEIGHT_2_2	0x00	RW	Combine Weight [2][2]
0x3141	R_COMBINE_WEIGHT_2_3	0x00	RW	Combine Weight [2][3]
0x3142	R_COMBINE_WEIGHT_3_0	0x80	RW	Combine Weight [3][0]
0x3143	R_COMBINE_WEIGHT_3_1	0x80	RW	Combine Weight [3][1]
0x3144	R_COMBINE_WEIGHT_3_2	0x00	RW	Combine Weight [3][2]
0x3145	R_COMBINE_WEIGHT_3_3	0x00	RW	Combine Weight [3][3]
0x3146	R_COMB_ERROR_CTRL_B2	0x02	RW	r_comb_error_ctrl High Byte
0x3147	R_COMB_ERROR_CTRL_B1	0x00	RW	r_comb_error_ctrl Middle Byte
0x3148	R_COMB_ERROR_CTRL_B0	0x00	RW	r_comb_error_ctrl Low Byte
0x3149	R_TRAFFIC_S_TH_H	0x28	RW	Traffic S Threshold High Byte
0x314A	NOT USED	–	–	Not Used
0x314B	R_TH_S_0H	0x10	RW	m_nThS[0] High Byte
0x314C	R_TH_S_0_L	0x00	RW	m_nThS[0] Low Byte

table A-1 sensor control registers (sheet 18 of 80)

address	register name	default value	R/W	description
0x314D	R_TH_S_1_H	0x10	RW	m_nThS[1] High Byte
0x314E	R_TH_S_1_L	0x00	RW	m_nThS[1] Low Byte
0x314F	R_THS_DINV	0x20	RW	m_nThSDinv Equal to (2^16)/(m nThS[1]-m nThS[0])
0x3150~ 0x31C2	RSVD	–	–	Reserved
0x31C3	R_R_GAIN_L_I_H	0x01	RW	Gain for L Exposure Channel Red Component High Byte
0x31C4	R_R_GAIN_L_I_L	0x00	RW	Gain for L Exposure Channel Red Component Low Byte
0x31C5	R_GR_GAIN_L_I_H	0x01	RW	Gain for L Exposure Channel GreenR Component High Byte
0x31C6	R_GR_GAIN_L_I_L	0x00	RW	Gain for L Exposure Channel GreenR Component Low Byte
0x31C7	R_GB_GAIN_L_I_H	0x01	RW	Gain for L Exposure Channel GreenB Component High Byte
0x31C8	R_GB_GAIN_L_I_L	0x00	RW	Gain for L Exposure Channel GreenB Component Low Byte
0x31C9	R_B_GAIN_L_I_H	0x01	RW	Gain for L Exposure Channel Blue Component High Byte
0x31CA	R_B_GAIN_L_I_L	0x00	RW	Gain for L Exposure Channel Blue Component Low Byte
0x31CB	R_R_GAIN_S_I_H	0x01	RW	Gain for S Exposure Channel Red Component High Byte
0x31CC	R_R_GAIN_S_I_L	0x00	RW	Gain for S Exposure Channel Red Component Low Byte
0x31CD	R_GR_GAIN_S_I_H	0x01	RW	Gain for S Exposure Channel GreenR Component High Byte
0x31CE	R_GR_GAIN_S_I_L	0x00	RW	Gain for S Exposure Channel GreenR Component Low Byte
0x31CF	R_GB_GAIN_S_I_H	0x01	RW	Gain for S Exposure Channel GreenB Component High Byte
0x31D0	R_GB_GAIN_S_I_L	0x00	RW	Gain for S Exposure Channel GreenB Component Low Byte
0x31D1	R_B_GAIN_S_I_H	0x01	RW	Gain for S Exposure Channel Blue Component High Byte

table A-1 sensor control registers (sheet 19 of 80)

address	register name	default value	R/W	description
0x31D2	R_B_GAIN_S_I_L	0x00	RW	Gain for S Exposure Channel Blue Component Low Byte
0x31D3	R_R_GAIN_VS_I_H	0x01	RW	Gain for VS Exposure Channel Red Component High Byte
0x31D4	R_R_GAIN_VS_I_L	0x00	RW	Gain for VS Exposure Channel Red Component Low Byte
0x31D5	R_GR_GAIN_VS_I_H	0x01	RW	Gain for VS Exposure Channel GreenR Component High Byte
0x31D6	R_GR_GAIN_VS_I_L	0x00	RW	Gain for VS Exposure Channel GreenR Component Low Byte
0x31D7	R_GB_GAIN_VS_I_H	0x01	RW	Gain for VS Exposure Channel GreenB Component High Byte
0x31D8	R_GB_GAIN_VS_I_L	0x00	RW	Gain for VS Exposure Channel GreenB Component Low Byte
0x31D9	R_B_GAIN_VS_I_H	0x01	RW	Gain for VS Exposure Channel Blue Component High Byte
0x31DA	R_B_GAIN_VS_I_L	0x00	RW	Gain for VS Exposure Channel Blue Component Low Byte
0x31DB	R_R_OFFSET_L_I_H	0x00	RW	Offset for L Exposure Channel Red Component High Byte
0x31DC	R_R_OFFSET_L_I_M	0x00	RW	Offset for L Exposure Channel Red Component Middle Byte
0x31DD	R_R_OFFSET_L_I_L	0x00	RW	Offset for L Exposure Channel Red Component Low Byte
0x31DE	R_GR_OFFSET_L_I_H	0x00	RW	Offset for L Exposure Channel GreenR Component High Byte
0x31DF	R_GR_OFFSET_L_I_M	0x00	RW	Offset for L Exposure Channel GreenR Component Middle Byte
0x31E0	R_GR_OFFSET_L_I_L	0x00	RW	Offset for L Exposure Channel GreenR Component Low Byte
0x31E1	R_GB_OFFSET_L_I_H	0x00	RW	Offset for L Exposure Channel GreenB Component High Byte
0x31E2	R_GB_OFFSET_L_I_M	0x00	RW	Offset for L Exposure Channel GreenB Component Middle Byte
0x31E3	R_GB_OFFSET_L_I_L	0x00	RW	Offset for L Exposure Channel GreenB Component Low Byte
0x31E4	R_B_OFFSET_L_I_H	0x00	RW	Offset for L Exposure Channel Blue Component High Byte

table A-1 sensor control registers (sheet 20 of 80)

address	register name	default value	R/W	description
0x31E5	R_B_OFFSET_L_I_M	0x00	RW	Offset for L Exposure Channel Blue Component Middle Byte
0x31E6	R_B_OFFSET_L_I_L	0x00	RW	Offset for L Exposure Channel Blue Component Low Byte
0x31E7	R_R_OFFSET_S_I_H	0x00	RW	Offset for S Exposure Channel Red Component High Byte
0x31E8	R_R_OFFSET_S_I_M	0x00	RW	Offset for S Exposure Channel Red Component Middle Byte
0x31E9	R_R_OFFSET_S_I_L	0x00	RW	Offset for S Exposure Channel Red Component Low Byte
0x31EA	R_GR_OFFSET_S_I_H	0x00	RW	Offset for S Exposure Channel GreenR Component High Byte
0x31EB	R_GR_OFFSET_S_I_M	0x00	RW	Offset for S Exposure Channel GreenR Component Middle Byte
0x31EC	R_GR_OFFSET_S_I_L	0x00	RW	Offset for S Exposure Channel GreenR Component Low Byte
0x31ED	R_GB_OFFSET_S_I_H	0x00	RW	Offset for S Exposure Channel GreenB Component High Byte
0x31EE	R_GB_OFFSET_S_I_M	0x00	RW	Offset for S Exposure Channel GreenB Component Middle Byte
0x31EF	R_GB_OFFSET_S_I_L	0x00	RW	Offset for S Exposure Channel GreenB Component Low Byte
0x31F0	R_B_OFFSET_S_I_H	0x00	RW	Offset for S Exposure Channel Blue Component High Byte
0x31F1	R_B_OFFSET_S_I_M	0x00	RW	Offset for S Exposure Channel Blue Component Middle Byte
0x31F2	R_B_OFFSET_S_I_L	0x00	RW	Offset for S Exposure Channel Blue Component Low Byte
0x31F3	R_R_OFFSET_VS_I_H	0x00	RW	Offset for VS Exposure Channel Red Component High Byte
0x31F4	R_R_OFFSET_VS_I_M	0x00	RW	Offset for VS Exposure Channel Red Component Middle Byte
0x31F5	R_R_OFFSET_VS_I_L	0x00	RW	Offset for VS Exposure Channel Red Component Low Byte
0x31F6	R_GR_OFFSET_VS_I_H	0x00	RW	Offset for VS Exposure Channel GreenR Component High Byte
0x31F7	R_GR_OFFSET_VS_I_M	0x00	RW	Offset for VS Exposure Channel GreenR Component Middle Byte

table A-1 sensor control registers (sheet 21 of 80)

address	register name	default value	R/W	description
0x31F8	R_GR_OFFSET_VS_I_L	0x00	RW	Offset for VS Exposure Channel GreenR Component Low Byte
0x31F9	R_GB_OFFSET_VS_I_H	0x00	RW	Offset for VS Exposure Channel GreenB Component High Byte
0x31FA	R_GB_OFFSET_VS_I_M	0x00	RW	Offset for VS Exposure Channel GreenB Component Middle Byte
0x31FB	R_GB_OFFSET_VS_I_L	0x00	RW	Offset for VS Exposure Channel GreenB Component Low Byte
0x31FC	R_B_OFFSET_VS_I_H	0x00	RW	Offset for VS Exposure Channel Blue Component High Byte
0x31FD	R_B_OFFSET_VS_I_M	0x00	RW	Offset for VS Exposure Channel Blue Component Middle Byte
0x31FE	R_B_OFFSET_VS_I_L	0x00	RW	Offset for VS Exposure Channel Blue Component Low Byte
0x31FF	R_L_DPC_CTRL00	0x18	RW	For Long Exposure Channel Bit[7]: Tail type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: Saturation type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[5]: Cross cluster correction enable Bit[4]: Horizontal same color plane couplet correction enable 0: Disable 1: Enable Bit[3]: Horizontal couplet correction enable 0: Disable 1: Enable Bit[2]: Not used Bit[1]: r_bwsnr_en Bit[0]: Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on the analog gain 1: Manual mode in which defect pixel threshold is set manually by register

table A-1 sensor control registers (sheet 22 of 80)

address	register name	default value	R/W	description
0x3200	R_L_DPC_CTRL01	0xDF	RW	For Long Exposure Channel Bit[7]: Set threshold for T-cluster 0: Automatically 1: Manually Bit[6]: r_comp_en Bit[5]: Vertical black pixel detection 0: Disable 1: Enable Bit[4]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[3]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable Bit[2]: T-cluster detection 0: Disable 1: Enable Bit[1:0]: Padding method of edge pixels 00: Pad with 0 01: Pad with 255 10: Pad with (255+1)/2 11: Pad with nearby same channel pixel This option will affect defect pixel detection of boundary pixels
0x3201	R_L_DPC_CTRL02	0xFF	RW	For Long Exposure Channel Bit[7]: White defect pixel detection 0: Disable 1: Enable Bit[6]: Black defect pixel detection 0: Disable 1: Enable Bit[5:4]: Pixel number threshold for detection of cross-cluster Bit[3:2]: Pixel number threshold for detection of T-cluster Bit[1:0]: Number of vertical connected white pixels removed 00: Remove the upper one white pixel 01: Remove two vertical white pixels 10: Remove three or less vertical connected white pixel

table A-1 sensor control registers (sheet 23 of 80)

address	register name	default value	R/W	description
0x3202	R_L_WTHREGLIST1	0x08	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold value for detecting white pixel in manual. More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x3203	R_L_WTHREGLIST2	0x20	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold value for detecting black pixel in manual mode. More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x3204	R_L_THRE1	0x10	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold value used in recovery of defect pixel for long channel. The bigger the value, the more details retained, but the less effective of recovering defect
0x3205	R_L_THRE2	0x20	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold for registering defect pixel to detect cross cluster for long channel. The greater the threshold, the more defect pixels will be removed
0x3206	R_L_THRE3	0x10	RW	For Long Exposure Channel Bit[7:0]: Threshold to determine high frequency area where the DPC will keep the fine details for long channel. The greater the threshold, the more details will be removed by DPC
0x3207	R_L_THRE4	0x18	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold for detecting horizontal couplet for long channel. This threshold should be greater than the threshold for single white/black pixel

table A-1 sensor control registers (sheet 24 of 80)

address	register name	default value	R/W	description
0x3208	R_L_WTHRE_LIST0	0x08	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 0 in auto mode
0x3209	R_L_WTHRE_LIST1	0x04	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 1 in auto mode
0x320A	R_L_WTHRE_LIST2	0x02	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 2 in auto mode
0x320B	R_L_WTHRE_LIST3	0x02	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 3 in auto mode
0x320C	R_L_BTHRE_LIST0	0x0C	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 0 in auto mode
0x320D	R_L_BTHRE_LIST1	0x06	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 1 in auto mode
0x320E	R_L_BTHRE_LIST2	0x02	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 2 in auto mode
0x320F	R_L_BTHRE_LIST3	0x02	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 3 in auto mode
0x3210	R_L_SAT	0xFF	RW	For Long Exposure Channel Bit[7:0]: Threshold of the center pixel for saturation type of cross cluster. To qualify a saturation type of cross cluster, the center pixel must be greater than this threshold
0x3211	R_L_VB_GAIN TH1	0x07	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Vertical black pixel detection threshold 1

table A-1 sensor control registers (sheet 25 of 80)

address	register name	default value	R/W	description
0x3212	R_L_VB_GAIN_TH2	0x03	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Vertical black pixel detection threshold 2
0x3213	R_L_SMOOTH_GLIST0	0x03	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Smooth gain list 0
0x3214	R_L_SMOOTH_GLIST1	0x07	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Smooth gain list 1
0x3215	R_L_SMOOTH_GLIST2	0x0F	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Smooth gain list 2
0x3216~ 0x3217	NOT USED	–	–	Not Used
0x3218	R_L_UNSAT	0xF0	RW	For Long Exposure Channel Bit[7:0]: Threshold of un-saturation level for detection of cross-cluster and T-cluster
0x3219	R_L_TTHRE	0x08	RW	For Long Exposure Channel Bit[7:0]: Threshold to determine a cross-cluster and T-cluster

table A-1 sensor control registers (sheet 26 of 80)

address	register name	default value	R/W	description
0x321A	R_S_DPC_CTRL00	0x18	RW	For Short Exposure Channel Bit[7]: Tail type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: Saturation type cross cluster correction enable, works only when cross cluster correction is 0: Disable 1: Enable Bit[5]: Cross cluster correction enable Bit[4]: Horizontal same color plane couplet correction enable 0: Disable 1: Enable Bit[3]: Horizontal couplet correction enable 0: Disable 1: Enable Bit[2]: Not used Bit[1]: r_bwsnr_en Bit[0]: Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on the analog gain 1: Manual mode in which defect pixel threshold is set manually by register

table A-1 sensor control registers (sheet 27 of 80)

address	register name	default value	R/W	description
0x321B	R_S_DPC_CTRL01	0xDF	RW	For Long Exposure Channel Bit[7]: Set threshold for T-cluster 0: Automatically 1: Manually Bit[6]: r_comp_en Bit[5]: Vertical black pixel detection 0: Disable 1: Enable Bit[4]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[3]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable Bit[2]: T-cluster detection 0: Disable 1: Enable Bit[1:0]: Padding method of edge pixels 00: Pad with 0 01: Pad with 255 10: Pad with (255+1)/2 11: Pad with nearby same channel pixel This option will affect defect pixel detection of boundary pixels
0x321C	R_S_DPC_CTRL02	0xFF	RW	For Short Exposure Channel Bit[7]: White defect pixel detection 0: Disable 1: Enable Bit[6]: Black defect pixel detection 0: Disable 1: Enable Bit[5:4]: Pixel number threshold for detection of cross-cluster Bit[3:2]: Pixel number threshold for detection of T-cluster Bit[1:0]: Number of vertical connected white pixels removed 00: Remove the upper one white pixel 01: Remove two vertical white pixels 10: Remove three or less vertical connected white pixel

table A-1 sensor control registers (sheet 28 of 80)

address	register name	default value	R/W	description
0x321D	R_S_WTHREGLIST1	0x08	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold value for detecting white pixel in manual. More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x321E	R_S_WTHREGLIST2	0x20	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold value for detecting black pixel in manual mode. More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x321F	R_S_THRE1	0x10	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold value used in recovery of defect pixel for long channel. The bigger the value, the more details retained, but the less effective of recovering defect
0x3220	R_S_THRE2	0x20	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold for registering defect pixel to detect cross cluster for long channel. The greater the threshold, the more defect pixels will be removed
0x3221	R_S_THRE3	0x10	RW	For Short Exposure Channel Bit[7:0]: Threshold to determine high frequency area where the DPC will keep the fine details for long channel. The greater the threshold, the more details will be removed by DPC
0x3222	R_S_THRE4	0x18	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold for detecting horizontal couplet for long channel. This threshold should be greater than the threshold for single while/black pixel

table A-1 sensor control registers (sheet 29 of 80)

address	register name	default value	R/W	description
0x3223	R_S_WTHRE_LIST0	0x08	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 0 in auto mode
0x3224	R_S_WTHRE_LIST1	0x04	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 1 in auto mode
0x3225	R_S_WTHRE_LIST2	0x02	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 2 in auto mode
0x3226	R_S_WTHRE_LIST3	0x02	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 3 in auto mode
0x3227	R_S_BTHRE_LIST0	0x0C	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 0 in auto mode
0x3228	R_S_BTHRE_LIST1	0x06	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 1 in auto mode
0x3229	R_S_BTHRE_LIST2	0x02	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 2 in auto mode
0x322A	R_S_BTHRE_LIST3	0x02	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 3 in auto mode
0x322B	R_S_SAT	0xFF	RW	For Short Exposure Channel Bit[7:0]: Threshold of the center pixel for saturation type of cross cluster. To qualify a saturation type of cross cluster, the center pixel must be greater than this threshold
0x322C	R_S_VB_GAIN_TH1	0x07	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Vertical black pixel detection threshold 1

table A-1 sensor control registers (sheet 30 of 80)

address	register name	default value	R/W	description
0x322D	R_S_VB_GAIN_TH2	0x03	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Vertical black pixel detection threshold 2
0x322E	R_S_SMOOTH_GLIST0	0x03	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Smooth gain list 0
0x322F	R_S_SMOOTH_GLIST1	0x07	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Smooth gain list 1
0x3230	R_S_SMOOTH_GLIST2	0x0F	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Smooth gain list 2
0x3231~ 0x3232	NOT USED	–	–	Not Used
0x3233	R_S_UNSAT	0xF0	RW	For Short Exposure Channel Bit[7:0]: Threshold of un-saturation level for detection of cross-cluster and T-cluster
0x3234	R_S_TTHRE	0x08	RW	For Short Exposure Channel Bit[7:0]: Threshold to determine a cross-cluster and T-cluster

table A-1 sensor control registers (sheet 31 of 80)

address	register name	default value	R/W	description
0x3235	R_VS_DPC_CTRL00	0x18	RW	For Very Short Exposure Channel Bit[7]: Tail type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: Saturation type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[5]: Cross cluster correction enable Bit[4]: Horizontal same color plane couplet correction enable 0: Disable 1: Enable Bit[3]: Horizontal couplet correction enable 0: Disable 1: Enable Bit[2]: Not used Bit[1]: r_bwsnr_en Bit[0]: Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on the analog gain 1: Manual mode in which defect pixel threshold is set manually by register

table A-1 sensor control registers (sheet 32 of 80)

address	register name	default value	R/W	description
0x3236	R_VS_DPC_CTRL01	0xDF	RW	For Very Short Exposure Channel Bit[7]: Manually set threshold for T-cluster Bit[6]: r_comp_en Bit[5]: Vertical black pixel detection 0: Disable 1: Enable Bit[4]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[3]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable Bit[2]: T-cluster detection 0: Disable 1: Enable Bit[1:0]: Padding method of edge pixels 00: Pad with 0 01: Pad with 255 10: Pad with (255+1)/2 11: Pad with nearby same channel pixel This option will affect defect pixel detection of boundary pixels
0x3237	R_VS_DPC_CTRL02	0xFF	RW	For Very Short Exposure Channel Bit[7]: White defect pixel detection 0: Disable 1: Enable Bit[6]: Black defect pixel detection 0: Disable 1: Enable Bit[5:4]: Pixel number threshold for detection of cross-cluster Bit[3:2]: Pixel number threshold for detection of T-cluster Bit[1:0]: Number of vertical connected white pixels removed 00: Remove the upper one white pixel 01: Remove two vertical white pixels 10: Remove three or less vertical connected white pixel

table A-1 sensor control registers (sheet 33 of 80)

address	register name	default value	R/W	description
0x3238	R_VS_WTHREGLIST1	0x08	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold value for detecting white pixel in manual. More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x3239	R_VS_WTHREGLIST2	0x20	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold value for detecting black pixel in manual mode. More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x323A	R_VS_THRE1	0x10	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold value used in recovery of defect pixel for long channel. The bigger the value, the more details retained, but the less effective of recovering defect
0x323B	R_VS_THRE2	0x20	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold for registering defect pixel to detect cross cluster for long channel. The greater the threshold, the more defect pixels will be removed
0x323C	R_VS_THRE3	0x10	RW	For Very Short Exposure Channel Bit[7:0]: Threshold to determine high frequency area where the DPC will keep the fine details for long channel. The greater the threshold, the more details will be removed by DPC
0x323D	R_VS_THRE4	0x18	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold for detecting horizontal couplet for long channel. This threshold should be greater than the threshold for single while/black pixel

table A-1 sensor control registers (sheet 34 of 80)

address	register name	default value	R/W	description
0x323E	R_VS_WTHRE_LIST0	0x08	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 0 in auto mode
0x323F	R_VS_WTHRE_LIST1	0x04	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 1 in auto mode
0x3240	R_VS_WTHRE_LIST2	0x02	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 2 in auto mode
0x3241	R_VS_WTHRE_LIST3	0x02	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 3 in auto mode
0x3242	R_VS_SAT	0xFF	RW	For Very Short Exposure Channel Bit[7:0]: Threshold of the center pixel for saturation type of cross cluster. To qualify a saturation type of cross cluster, the center pixel must be greater than this threshold
0x3243	R_VS_VB_GAIN_TH1	0x07	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Vertical black pixel detection threshold 1
0x3244	R_VS_VB_GAIN_TH2	0x03	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Vertical black pixel detection threshold 2
0x3245	R_VS_SMOOTH_GLIST0	0x03	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Smooth gain list 0
0x3246	R_VS_SMOOTH_GLIST1	0x07	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Smooth gain list 1
0x3247	R_VS_SMOOTH_GLIST2	0x0F	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Smooth gain list 2
0x3248~ 0x3249	NOT USED	–	–	Not Used

table A-1 sensor control registers (sheet 35 of 80)

address	register name	default value	R/W	description
0x324A	R_VS_UNSAT	0xF0	RW	For Very Short Exposure Channel Bit[7:0]: Threshold of un-saturation level for detection of cross-cluster and T-cluster
0x324B	R_VS_TTHRE	0x08	RW	For Very Short Exposure Channel Bit[7:0]: Threshold to determine a cross-cluster and T-cluster
0x324C~ 0x3267	RSVD	–	–	Reserved
0x3268	R_NOISELIST0_L_I	0x04	RW	NoiseList0 for L Exposure Channel RAW Denoise
0x3269	R_NOISELIST1_L_I	0x08	RW	NoiseList1 for L Exposure Channel RAW Denoise
0x326A	R_NOISELIST2_L_I	0x10	RW	NoiseList2 for L Exposure Channel RAW Denoise
0x326B	R_NOISELIST3_L_I	0x18	RW	NoiseList3 for L Exposure Channel RAW Denoise
0x326C	R_NOISELIST4_L_I	0x20	RW	NoiseList4 for L Exposure Channel RAW Denoise
0x326D	R_NOISELIST5_L_I	0x30	RW	NoiseList5 for L Exposure Channel RAW Denoise
0x326E	R_NOISELIST6_L_I	0x40	RW	NoiseList6 for L Exposure Channel RAW Denoise
0x326F	R_NOISELIST7_L_I	0x40	RW	NoiseList7 for L Exposure Channel RAW Denoise
0x3270	R_G_DNS_EN_L_I	0x00	RW	Enable for Choosing G Position Pixels to be Involved in Denoise
0x3271	R_NOISE_YSLOP_L_I	0x04	RW	Noise YSlope Signal for L Exposure Channel Noise Calculation
0x3272	R_MAX_EDGE_THRE_L_I	0x3F	RW	Maximum Edge Threshold for L Exposure Channel Noise Calculation
0x3273	R_NOISELIST0_S_I	0x04	RW	NoiseList0 for S Exposure Channel RAW Denoise
0x3274	R_NOISELIST1_S_I	0x08	RW	NoiseList1 for S Exposure Channel RAW Denoise
0x3275	R_NOISELIST2_S_I	0x10	RW	NoiseList2 for S Exposure Channel RAW Denoise

table A-1 sensor control registers (sheet 36 of 80)

address	register name	default value	R/W	description
0x3276	R_NOISELIST3_S_I	0x18	RW	NoiseList3 for S Exposure Channel RAW Denoise
0x3277	R_NOISELIST4_S_I	0x20	RW	NoiseList4 for S Exposure Channel RAW Denoise
0x3278	R_NOISELIST5_S_I	0x30	RW	NoiseList5 for S Exposure Channel RAW Denoise
0x3279	R_NOISELIST6_S_I	0x40	RW	NoiseList6 for S Exposure Channel RAW Denoise
0x327A	R_NOISELIST7_S_I	0x40	RW	NoiseList7 for S Exposure Channel RAW Denoise
0x327B	R_G_DNS_EN_S_I	0x00	RW	Enable for Choosing G Position Pixels to Be Involved in Denoise
0x327C	R_NOISE_YSLOP_S_I	0x04	RW	Noise YSlope Signal for S Exposure Channel Noise Calculation
0x327D	R_MAX_EDGE_THRE_S_I	0x3F	RW	Maximum Edge Threshold for S Exposure Channel Noise Calculation
0x327E	R_NOISELIST0_V_I	0x04	RW	NoiseList0 for VS Exposure Channel RAW Denoise
0x327F	R_NOISELIST1_V_I	0x08	RW	NoiseList1 for VS Exposure Channel RAW Denoise
0x3280	R_NOISELIST2_V_I	0x10	RW	NoiseList2 for VS Exposure Channel RAW Denoise
0x3281	R_NOISELIST3_V_I	0x18	RW	NoiseList3 for VS Exposure Channel RAW Denoise
0x3282	R_NOISELIST4_V_I	0x20	RW	NoiseList4 for VS Exposure Channel RAW Denoise
0x3283	R_NOISELIST5_V_I	0x30	RW	NoiseList5 for VS Exposure Channel RAW Denoise
0x3284	R_NOISELIST6_V_I	0x40	RW	NoiseList6 for VS Exposure Channel RAW Denoise
0x3285	R_NOISELIST7_V_I	0x40	RW	NoiseList7 for VS Exposure Channel RAW Denoise
0x3286	R_G_DNS_EN_V_I	0x00	RW	Enable for Choosing G Position Pixels to be Involved in Denoise
0x3287	R_NOISE_YSLOP_V_I	0x04	RW	Noise YSlope Signal for VS Exposure Channel Noise Calculation
0x3288	R_MAX_EDGE_THRE_V_I	0x3F	RW	Maximum Edge Threshold for VS Exposure Channel Noise Calculation

table A-1 sensor control registers (sheet 37 of 80)

address	register name	default value	R/W	description
0x3289~ 0x3290	RSVD	–	–	Reserved
0x3291	R_CTRL08	0x00	RW	Bit[7:3]: Not used Bit[2]: Flip offset enable Bit[1]: Mirror offset enable Bit[0]: Reserved
0x3292~ 0x3295	RSVD	–	–	Reserved
0x3296	LENC_L_G00	0x00	RW	G00 of 8x8 G Control Point Array for L/VS
0x3297	LENC_L_G01	0x00	RW	G01 of 8x8 G Control Point Array for L/VS
0x3298	LENC_L_G02	0x00	RW	G02 of 8x8 G Control Point Array for L/VS
0x3299	LENC_L_G03	0x00	RW	G03 of 8x8 G Control Point Array for L/VS
0x329A	LENC_L_G04	0x00	RW	G04 of 8x8 G Control Point Array for L/VS
0x329B	LENC_L_G05	0x00	RW	G05 of 8x8 G Control Point Array for L/VS
0x329C	LENC_L_G06	0x00	RW	G06 of 8x8 G Control Point Array for L/VS
0x329D	LENC_L_G07	0x00	RW	G07 of 8x8 G Control Point Array for L/VS
0x329E	LENC_L_G10	0x00	RW	G10 of 8x8 G Control Point Array for L/VS
0x329F	LENC_L_G11	0x00	RW	G11 of 8x8 G Control Point Array for L/VS
0x32A0	LENC_L_G12	0x00	RW	G12 of 8x8 G Control Point Array for L/VS
0x32A1	LENC_L_G13	0x00	RW	G13 of 8x8 G Control Point Array for L/VS
0x32A2	LENC_L_G14	0x00	RW	G14 of 8x8 G Control Point Array for L/VS
0x32A3	LENC_L_G15	0x00	RW	G15 of 8x8 G Control Point Array for L/VS
0x32A4	LENC_L_G16	0x00	RW	G16 of 8x8 G Control Point Array for L/VS
0x32A5	LENC_L_G17	0x00	RW	G17 of 8x8 G Control Point Array for L/VS
0x32A6	LENC_L_G20	0x00	RW	G20 of 8x8 G Control Point Array for L/VS
0x32A7	LENC_L_G21	0x00	RW	G21 of 8x8 G Control Point Array for L/VS
0x32A8	LENC_L_G22	0x00	RW	G22 of 8x8 G Control Point Array for L/VS
0x32A9	LENC_L_G23	0x00	RW	G23 of 8x8 G Control Point Array for L/VS
0x32AA	LENC_L_G24	0x00	RW	G24 of 8x8 G Control Point Array for L/VS
0x32AB	LENC_L_G25	0x00	RW	G25 of 8x8 G Control Point Array for L/VS

table A-1 sensor control registers (sheet 38 of 80)

address	register name	default value	R/W	description
0x32AC	LENC_L_G26	0x00	RW	G26 of 8x8 G Control Point Array for L/VS
0x32AD	LENC_L_G27	0x00	RW	G27 of 8x8 G Control Point Array for L/VS
0x32AE	LENC_L_G30	0x00	RW	G30 of 8x8 G Control Point Array for L/VS
0x32AF	LENC_L_G31	0x00	RW	G31 of 8x8 G Control Point Array for L/VS
0x32B0	LENC_L_G32	0x00	RW	G32 of 8x8 G Control Point Array for L/VS
0x32B1	LENC_L_G33	0x00	RW	G33 of 8x8 G Control Point Array for L/VS
0x32B2	LENC_L_G34	0x00	RW	G34 of 8x8 G Control Point Array for L/VS
0x32B3	LENC_L_G35	0x00	RW	G35 of 8x8 G Control Point Array for L/VS
0x32B4	LENC_L_G36	0x00	RW	G36 of 8x8 G Control Point Array for L/VS
0x32B5	LENC_L_G37	0x00	RW	G37 of 8x8 G Control Point Array for L/VS
0x32B6	LENC_L_G40	0x00	RW	G40 of 8x8 G Control Point Array for L/VS
0x32B7	LENC_L_G41	0x00	RW	G41 of 8x8 G Control Point Array for L/VS
0x32B8	LENC_L_G42	0x00	RW	G42 of 8x8 G Control Point Array for L/VS
0x32B9	LENC_L_G43	0x00	RW	G43 of 8x8 G Control Point Array for L/VS
0x32BA	LENC_L_G44	0x00	RW	G44 of 8x8 G Control Point Array for L/VS
0x32BB	LENC_L_G45	0x00	RW	G45 of 8x8 G Control Point Array for L/VS
0x32BC	LENC_L_G46	0x00	RW	G46 of 8x8 G Control Point Array for L/VS
0x32BD	LENC_L_G47	0x00	RW	G47 of 8x8 G Control Point Array for L/VS
0x32BE	LENC_L_G50	0x00	RW	G50 of 8x8 G Control Point Array for L/VS
0x32BF	LENC_L_G51	0x00	RW	G51 of 8x8 G Control Point Array for L/VS
0x32C0	LENC_L_G52	0x00	RW	G52 of 8x8 G Control Point Array for L/VS
0x32C1	LENC_L_G53	0x00	RW	G53 of 8x8 G Control Point Array for L/VS
0x32C2	LENC_L_G54	0x00	RW	G54 of 8x8 G Control Point Array for L/VS
0x32C3	LENC_L_G55	0x00	RW	G55 of 8x8 G Control Point Array for L/VS
0x32C4	LENC_L_G56	0x00	RW	G56 of 8x8 G Control Point Array for L/VS
0x32C5	LENC_L_G57	0x00	RW	G57 of 8x8 G Control Point Array for L/VS
0x32C6	LENC_L_G60	0x00	RW	G60 of 8x8 G Control Point Array for L/VS
0x32C7	LENC_L_G61	0x00	RW	G61 of 8x8 G Control Point Array for L/VS

table A-1 sensor control registers (sheet 39 of 80)

address	register name	default value	R/W	description
0x32C8	LENC_L_G62	0x00	RW	G62 of 8x8 G Control Point Array for L/VS
0x32C9	LENC_L_G63	0x00	RW	G63 of 8x8 G Control Point Array for L/VS
0x32CA	LENC_L_G64	0x00	RW	G64 of 8x8 G Control Point Array for L/VS
0x32CB	LENC_L_G65	0x00	RW	G65 of 8x8 G Control Point Array for L/VS
0x32CC	LENC_L_G66	0x00	RW	G66 of 8x8 G Control Point Array for L/VS
0x32CD	LENC_L_G67	0x00	RW	G67 of 8x8 G Control Point Array for L/VS
0x32CE	LENC_L_G70	0x00	RW	G70 of 8x8 G Control Point Array for L/VS
0x32CF	LENC_L_G71	0x00	RW	G71 of 8x8 G Control Point Array for L/VS
0x32D0	LENC_L_G72	0x00	RW	G72 of 8x8 G Control Point Array for L/VS
0x32D1	LENC_L_G73	0x00	RW	G73 of 8x8 G Control Point Array for L/VS
0x32D2	LENC_L_G74	0x00	RW	G74 of 8x8 G Control Point Array for L/VS
0x32D3	LENC_L_G75	0x00	RW	G75 of 8x8 G Control Point Array for L/VS
0x32D4	LENC_L_G76	0x00	RW	G76 of 8x8 G Control Point Array for L/VS
0x32D5	LENC_L_G77	0x00	RW	G77 of 8x8 G Control Point Array for L/VS
0x32D6	LENC_L_B00	0x20	RW	B00 of 8x8 B Control Point Array for L/VS
0x32D7	LENC_L_B01	0x20	RW	B01 of 8x8 B Control Point Array for L/VS
0x32D8	LENC_L_B02	0x20	RW	B02 of 8x8 B Control Point Array for L/VS
0x32D9	LENC_L_B03	0x20	RW	B03 of 8x8 B Control Point Array for L/VS
0x32DA	LENC_L_B04	0x20	RW	B04 of 8x8 B Control Point Array for L/VS
0x32DB	LENC_L_B05	0x20	RW	B05 of 8x8 B Control Point Array for L/VS
0x32DC	LENC_L_B06	0x20	RW	B06 of 8x8 B Control Point Array for L/VS
0x32DD	LENC_L_B07	0x20	RW	B07 of 8x8 B Control Point Array for L/VS
0x32DE	LENC_L_B10	0x20	RW	B10 of 8x8 B Control Point Array for L/VS
0x32DF	LENC_L_B11	0x20	RW	B11 of 8x8 B Control Point Array for L/VS
0x32E0	LENC_L_B12	0x20	RW	B12 of 8x8 B Control Point Array for L/VS
0x32E1	LENC_L_B13	0x20	RW	B13 of 8x8 B Control Point Array for L/VS
0x32E2	LENC_L_B14	0x20	RW	B14 of 8x8 B Control Point Array for L/VS
0x32E3	LENC_L_B15	0x20	RW	B15 of 8x8 B Control Point Array for L/VS

table A-1 sensor control registers (sheet 40 of 80)

address	register name	default value	R/W	description
0x32E4	LENC_L_B16	0x20	RW	B16 of 8x8 B Control Point Array for L/VS
0x32E5	LENC_L_B17	0x20	RW	B17 of 8x8 B Control Point Array for L/VS
0x32E6	LENC_L_B20	0x20	RW	B20 of 8x8 B Control Point Array for L/VS
0x32E7	LENC_L_B21	0x20	RW	B21 of 8x8 B Control Point Array for L/VS
0x32E8	LENC_L_B22	0x20	RW	B22 of 8x8 B Control Point Array for L/VS
0x32E9	LENC_L_B23	0x20	RW	B23 of 8x8 B Control Point Array for L/VS
0x32EA	LENC_L_B24	0x20	RW	B24 of 8x8 B Control Point Array for L/VS
0x32EB	LENC_L_B25	0x20	RW	B25 of 8x8 B Control Point Array for L/VS
0x32EC	LENC_L_B26	0x20	RW	B26 of 8x8 B Control Point Array for L/VS
0x32ED	LENC_L_B27	0x20	RW	B27 of 8x8 B Control Point Array for L/VS
0x32EE	LENC_L_B30	0x20	RW	B30 of 8x8 B Control Point Array for L/VS
0x32EF	LENC_L_B31	0x20	RW	B31 of 8x8 B Control Point Array for L/VS
0x32F0	LENC_L_B32	0x20	RW	B32 of 8x8 B Control Point Array for L/VS
0x32F1	LENC_L_B33	0x20	RW	B33 of 8x8 B Control Point Array for L/VS
0x32F2	LENC_L_B34	0x20	RW	B34 of 8x8 B Control Point Array for L/VS
0x32F3	LENC_L_B35	0x20	RW	B35 of 8x8 B Control Point Array for L/VS
0x32F4	LENC_L_B36	0x20	RW	B36 of 8x8 B Control Point Array for L/VS
0x32F5	LENC_L_B37	0x20	RW	B37 of 8x8 B Control Point Array for L/VS
0x32F6	LENC_L_B40	0x20	RW	B40 of 8x8 B Control Point Array for L/VS
0x32F7	LENC_L_B41	0x20	RW	B41 of 8x8 B Control Point Array for L/VS
0x32F8	LENC_L_B42	0x20	RW	B42 of 8x8 B Control Point Array for L/VS
0x32F9	LENC_L_B43	0x20	RW	B43 of 8x8 B Control Point Array for L/VS
0x32FA	LENC_L_B44	0x20	RW	B44 of 8x8 B Control Point Array for L/VS
0x32FB	LENC_L_B45	0x20	RW	B45 of 8x8 B Control Point Array for L/VS
0x32FC	LENC_L_B46	0x20	RW	B46 of 8x8 B Control Point Array for L/VS
0x32FD	LENC_L_B47	0x20	RW	B47 of 8x8 B Control Point Array for L/VS
0x32FE	LENC_L_B50	0x20	RW	B50 of 8x8 B Control Point Array for L/VS
0x32FF	LENC_L_B51	0x20	RW	B51 of 8x8 B Control Point Array for L/VS

table A-1 sensor control registers (sheet 41 of 80)

address	register name	default value	R/W	description
0x3300	LENC_L_B52	0x20	RW	B52 of 8x8 B Control Point Array for L/VS
0x3301	LENC_L_B53	0x20	RW	B53 of 8x8 B Control Point Array for L/VS
0x3302	LENC_L_B54	0x20	RW	B54 of 8x8 B Control Point Array for L/VS
0x3303	LENC_L_B55	0x20	RW	B55 of 8x8 B Control Point Array for L/VS
0x3304	LENC_L_B56	0x20	RW	B56 of 8x8 B Control Point Array for L/VS
0x3305	LENC_L_B57	0x20	RW	B57 of 8x8 B Control Point Array for L/VS
0x3306	LENC_L_B60	0x20	RW	B60 of 8x8 B Control Point Array for L/VS
0x3307	LENC_L_B61	0x20	RW	B61 of 8x8 B Control Point Array for L/VS
0x3308	LENC_L_B62	0x20	RW	B62 of 8x8 B Control Point Array for L/VS
0x3309	LENC_L_B63	0x20	RW	B63 of 8x8 B Control Point Array for L/VS
0x330A	LENC_L_B64	0x20	RW	B64 of 8x8 B Control Point Array for L/VS
0x330B	LENC_L_B65	0x20	RW	B65 of 8x8 B Control Point Array for L/VS
0x330C	LENC_L_B66	0x20	RW	B66 of 8x8 B Control Point Array for L/VS
0x330D	LENC_L_B67	0x20	RW	B67 of 8x8 B Control Point Array for L/VS
0x330E	LENC_L_B70	0x20	RW	B70 of 8x8 B Control Point Array for L/VS
0x330F	LENC_L_B71	0x20	RW	B71 of 8x8 B Control Point Array for L/VS
0x3310	LENC_L_B72	0x20	RW	B72 of 8x8 B Control Point Array for L/VS
0x3311	LENC_L_B73	0x20	RW	B73 of 8x8 B Control Point Array for L/VS
0x3312	LENC_L_B74	0x20	RW	B74 of 8x8 B Control Point Array for L/VS
0x3313	LENC_L_B75	0x20	RW	B75 of 8x8 B Control Point Array for L/VS
0x3314	LENC_L_B76	0x20	RW	B76 of 8x8 B Control Point Array for L/VS
0x3315	LENC_L_B77	0x20	RW	B77 of 8x8 B Control Point Array for L/VS
0x3316	LENC_L_R00	0x20	RW	R00 of 8x8 R Control Point Array for L/VS
0x3317	LENC_L_R01	0x20	RW	R01 of 8x8 R Control Point Array for L/VS
0x3318	LENC_L_R02	0x20	RW	R02 of 8x8 R Control Point Array for L/VS
0x3319	LENC_L_R03	0x20	RW	R03 of 8x8 R Control Point Array for L/VS
0x331A	LENC_L_R04	0x20	RW	R04 of 8x8 R Control Point Array for L/VS
0x331B	LENC_L_R05	0x20	RW	R05 of 8x8 R Control Point Array for L/VS

table A-1 sensor control registers (sheet 42 of 80)

address	register name	default value	R/W	description
0x331C	LENC_L_R06	0x20	RW	R06 of 8x8 R Control Point Array for L/VS
0x331D	LENC_L_R07	0x20	RW	R07 of 8x8 R Control Point Array for L/VS
0x331E	LENC_L_R10	0x20	RW	R10 of 8x8 R Control Point Array for L/VS
0x331F	LENC_L_R11	0x20	RW	R11 of 8x8 R Control Point Array for L/VS
0x3320	LENC_L_R12	0x20	RW	R12 of 8x8 R Control Point Array for L/VS
0x3321	LENC_L_R13	0x20	RW	R13 of 8x8 R control point array for L/VS
0x3322	LENC_L_R14	0x20	RW	R14 of 8x8 R control point array for L/VS
0x3323	LENC_L_R15	0x20	RW	R15 of 8x8 R control point array for L/VS
0x3324	LENC_L_R16	0x20	RW	R16 of 8x8 R control point array for L/VS
0x3325	LENC_L_R17	0x20	RW	R17 of 8x8 R control point array for L/VS
0x3326	LENC_L_R20	0x20	RW	R20 of 8x8 R control point array for L/VS
0x3327	LENC_L_R21	0x20	RW	R21 of 8x8 R control point array for L/VS
0x3328	LENC_L_R22	0x20	RW	R22 of 8x8 R control point array for L/VS
0x3329	LENC_L_R23	0x20	RW	R23 of 8x8 R control point array for L/VS
0x332A	LENC_L_R24	0x20	RW	R24 of 8x8 R control point array for L/VS
0x332B	LENC_L_R25	0x20	RW	R25 of 8x8 R control point array for L/VS
0x332C	LENC_L_R26	0x20	RW	R26 of 8x8 R control point array for L/VS
0x332D	LENC_L_R27	0x20	RW	R27 of 8x8 R control point array for L/VS
0x332E	LENC_L_R30	0x20	RW	R30 of 8x8 R control point array for L/VS
0x332F	LENC_L_R31	0x20	RW	R31 of 8x8 R control point array for L/VS
0x3330	LENC_L_R32	0x20	RW	R32 of 8x8 R control point array for L/VS
0x3331	LENC_L_R33	0x20	RW	R33 of 8x8 R control point array for L/VS
0x3332	LENC_L_R34	0x20	RW	R34 of 8x8 R control point array for L/VS
0x3333	LENC_L_R35	0x20	RW	R35 of 8x8 R control point array for L/VS
0x3334	LENC_L_R36	0x20	RW	R36 of 8x8 R control point array for L/VS
0x3335	LENC_L_R37	0x20	RW	R37 of 8x8 R control point array for L/VS
0x3336	LENC_L_R40	0x20	RW	R40 of 8x8 R control point array for L/VS
0x3337	LENC_L_ R41	0x20	RW	R41 of 8x8 R control point array for L/VS

table A-1 sensor control registers (sheet 43 of 80)

address	register name	default value	R/W	description
0x3338	LENC_L_R42	0x20	RW	R42 of 8x8 R control point array for L/VS
0x3339	LENC_L_R43	0x20	RW	R43 of 8x8 R control point array for L/VS
0x333A	LENC_L_R44	0x20	RW	R44 of 8x8 R control point array for L/VS
0x333B	LENC_L_R45	0x20	RW	R45 of 8x8 R control point array for L/VS
0x333C	LENC_L_R46	0x20	RW	R46 of 8x8 R control point array for L/VS
0x333D	LENC_L_R47	0x20	RW	R47 of 8x8 R control point array for L/VS
0x333E	LENC_L_R50	0x20	RW	R50 of 8x8 R control point array for L/VS
0x333F	LENC_L_R51	0x20	RW	R51 of 8x8 R control point array for L/VS
0x3340	LENC_L_R52	0x20	RW	R52 of 8x8 R control point array for L/VS
0x3341	LENC_L_R53	0x20	RW	R53 of 8x8 R control point array for L/VS
0x3342	LENC_L_R54	0x20	RW	R54 of 8x8 R control point array for L/VS
0x3343	LENC_L_R55	0x20	RW	R55 of 8x8 R control point array for L/VS
0x3344	LENC_L_R56	0x20	RW	R56 of 8x8 R control point array for L/VS
0x3345	LENC_L_R57	0x20	RW	R57 of 8x8 R control point array for L/VS
0x3346	LENC_L_R60	0x20	RW	R60 of 8x8 R control point array for L/VS
0x3347	LENC_L_R61	0x20	RW	R61 of 8x8 R control point array for L/VS
0x3348	LENC_L_R62	0x20	RW	R62 of 8x8 R control point array for L/VS
0x3349	LENC_L_R63	0x20	RW	R63 of 8x8 R control point array for L/VS
0x334A	LENC_L_R64	0x20	RW	R64 of 8x8 R control point array for L/VS
0x334B	LENC_L_R65	0x20	RW	R65 of 8x8 R control point array for L/VS
0x334C	LENC_L_R66	0x20	RW	R66 of 8x8 R control point array for L/VS
0x334D	LENC_L_R67	0x20	RW	R67 of 8x8 R control point array for L/VS
0x334E	LENC_L_R70	0x20	RW	R70 of 8x8 R control point array for L/VS
0x334F	LENC_L_R71	0x20	RW	R71 of 8x8 R control point array for L/VS
0x3350	LENC_L_R72	0x20	RW	R72 of 8x8 R control point array for L/VS
0x3351	LENC_L_R73	0x20	RW	R73 of 8x8 R control point array for L/VS
0x3352	LENC_L_R74	0x20	RW	R74 of 8x8 R control point array for L/VS
0x3353	LENC_L_R75	0x20	RW	R75 of 8x8 R control point array for L/VS

table A-1 sensor control registers (sheet 44 of 80)

address	register name	default value	R/W	description
0x3354	LENC_L_R76	0x20	RW	R76 of 8x8 R control point array for L/VS
0x3355	LENC_L_R77	0x20	RW	R77 of 8x8 R control point array for L/VS
0x3356	LENC_S_G00	0x00	RW	G00 of 8x8 G Control Point Array for S
0x3357	LENC_S_G01	0x00	RW	G01 of 8x8 G Control Point Array for S
0x3358	LENC_S_G02	0x00	RW	G02 of 8x8 G Control Point Array for S
0x3359	LENC_S_G03	0x00	RW	G03 of 8x8 G Control Point Array for S
0x335A	LENC_S_G04	0x00	RW	G04 of 8x8 G Control Point Array for S
0x335B	LENC_S_G05	0x00	RW	G05 of 8x8 G Control Point Array for S
0x335C	LENC_S_G06	0x00	RW	G06 of 8x8 G Control Point Array for S
0x335D	LENC_S_G07	0x00	RW	G07 of 8x8 G Control Point Array for S
0x335E	LENC_S_G10	0x00	RW	G10 of 8x8 G Control Point Array for S
0x335F	LENC_S_G11	0x00	RW	G11 of 8x8 G Control Point Array for S
0x3360	LENC_S_G12	0x00	RW	G12 of 8x8 G Control Point Array for S
0x3361	LENC_S_G13	0x00	RW	G13 of 8x8 G Control Point Array for S
0x3362	LENC_S_G14	0x00	RW	G14 of 8x8 G Control Point Array for S
0x3363	LENC_S_G15	0x00	RW	G15 of 8x8 G Control Point Array for S
0x3364	LENC_S_G16	0x00	RW	G16 of 8x8 G Control Point Array for S
0x3365	LENC_S_G17	0x00	RW	G17 of 8x8 G Control Point Array for S
0x3366	LENC_S_G20	0x00	RW	G20 of 8x8 G Control Point Array for S
0x3367	LENC_S_G21	0x00	RW	G21 of 8x8 G Control Point Array for S
0x3368	LENC_S_G22	0x00	RW	G22 of 8x8 G Control Point Array for S
0x3369	LENC_S_G23	0x00	RW	G23 of 8x8 G Control Point Array for S
0x336A	LENC_S_G24	0x00	RW	G24 of 8x8 G Control Point Array for S
0x336B	LENC_S_G25	0x00	RW	G25 of 8x8 G Control Point Array for S
0x336C	LENC_S_G26	0x00	RW	G26 of 8x8 G Control Point Array for S
0x336D	LENC_S_G27	0x00	RW	G27 of 8x8 G Control Point Array for S
0x336E	LENC_S_G30	0x00	RW	G30 of 8x8 G Control Point Array for S
0x336F	LENC_S_G31	0x00	RW	G31 of 8x8 G Control Point Array for S

table A-1 sensor control registers (sheet 45 of 80)

address	register name	default value	R/W	description
0x3370	LENC_S_G32	0x00	RW	G32 of 8x8 G Control Point Array for S
0x3371	LENC_S_G33	0x00	RW	G33 of 8x8 G Control Point Array for S
0x3372	LENC_S_G34	0x00	RW	G34 of 8x8 G Control Point Array for S
0x3373	LENC_S_G35	0x00	RW	G35 of 8x8 G Control Point Array for S
0x3374	LENC_S_G36	0x00	RW	G36 of 8x8 G Control Point Array for S
0x3375	LENC_S_G37	0x00	RW	G37 of 8x8 G Control Point Array for S
0x3376	LENC_S_G40	0x00	RW	G40 of 8x8 G Control Point Array for S
0x3377	LENC_S_G41	0x00	RW	G41 of 8x8 G Control Point Array for S
0x3378	LENC_S_G42	0x00	RW	G42 of 8x8 G Control Point Array for S
0x3379	LENC_S_G43	0x00	RW	G43 of 8x8 G Control Point Array for S
0x337A	LENC_S_G44	0x00	RW	G44 of 8x8 G Control Point Array for S
0x337B	LENC_S_G45	0x00	RW	G45 of 8x8 G Control Point Array for S
0x337C	LENC_S_G46	0x00	RW	G46 of 8x8 G Control Point Array for S
0x337D	LENC_S_G47	0x00	RW	G47 of 8x8 G Control Point Array for S
0x337E	LENC_S_G50	0x00	RW	G50 of 8x8 G Control Point Array for S
0x337F	LENC_S_G51	0x00	RW	G51 of 8x8 G Control Point Array for S
0x3380	LENC_S_G52	0x00	RW	G52 of 8x8 G Control Point Array for S
0x3381	LENC_S_G53	0x00	RW	G53 of 8x8 G Control Point Array for S
0x3382	LENC_S_G54	0x00	RW	G54 of 8x8 G Control Point Array for S
0x3383	LENC_S_G55	0x00	RW	G55 of 8x8 G Control Point Array for S
0x3384	LENC_S_G56	0x00	RW	G56 of 8x8 G Control Point Array for S
0x3385	LENC_S_G57	0x00	RW	G57 of 8x8 G Control Point Array for S
0x3386	LENC_S_G60	0x00	RW	G60 of 8x8 G Control Point Array for S
0x3387	LENC_S_G61	0x00	RW	G61 of 8x8 G Control Point Array for S
0x3388	LENC_S_G62	0x00	RW	G62 of 8x8 G Control Point Array for S
0x3389	LENC_S_G63	0x00	RW	G63 of 8x8 G Control Point Array for S
0x338A	LENC_S_G64	0x00	RW	G64 of 8x8 G Control Point Array for S
0x338B	LENC_S_G65	0x00	RW	G65 of 8x8 G Control Point Array for S

table A-1 sensor control registers (sheet 46 of 80)

address	register name	default value	R/W	description
0x338C	LENC_S_G66	0x00	RW	G66 of 8x8 G Control Point Array for S
0x338D	LENC_S_G67	0x00	RW	G67 of 8x8 G Control Point Array for S
0x338E	LENC_S_G70	0x00	RW	G70 of 8x8 G Control Point Array for S
0x338F	LENC_S_G71	0x00	RW	G71 of 8x8 G Control Point Array for S
0x3390	LENC_S_G72	0x00	RW	G72 of 8x8 G Control Point Array for S
0x3391	LENC_S_G73	0x00	RW	G73 of 8x8 G Control Point Array for S
0x3392	LENC_S_G74	0x00	RW	G74 of 8x8 G Control Point Array for S
0x3393	LENC_S_G75	0x00	RW	G75 of 8x8 G Control Point Array for S
0x3394	LENC_S_G76	0x00	RW	G76 of 8x8 G Control Point Array for S
0x3395	LENC_S_G77	0x00	RW	G77 of 8x8 G Control Point Array for S
0x3396	LENC_S_B00	0x20	RW	B00 of 8x8 B Control Point Array for S
0x3397	LENC_S_B01	0x20	RW	B01 of 8x8 B Control Point Array for S
0x3398	LENC_S_B02	0x20	RW	B02 of 8x8 B Control Point Array for S
0x3399	LENC_S_B03	0x20	RW	B03 of 8x8 B Control Point Array for S
0x339A	LENC_S_B04	0x20	RW	B04 of 8x8 B Control Point Array for S
0x339B	LENC_S_B05	0x20	RW	B05 of 8x8 B Control Point Array for S
0x339C	LENC_S_B06	0x20	RW	B06 of 8x8 B Control Point Array for S
0x339D	LENC_S_B07	0x20	RW	B07 of 8x8 B Control Point Array for S
0x339E	LENC_S_B10	0x20	RW	B10 of 8x8 B Control Point Array for S
0x339F	LENC_S_B11	0x20	RW	B11 of 8x8 B Control Point Array for S
0x33A0	LENC_S_B12	0x20	RW	B12 of 8x8 B Control Point Array for S
0x33A1	LENC_S_B13	0x20	RW	B13 of 8x8 B Control Point Array for S
0x33A2	LENC_S_B14	0x20	RW	B14 of 8x8 B Control Point Array for S
0x33A3	LENC_S_B15	0x20	RW	B15 of 8x8 B Control Point Array for S
0x33A4	LENC_S_B16	0x20	RW	B16 of 8x8 B Control Point Array for S
0x33A5	LENC_S_B17	0x20	RW	B17 of 8x8 B Control Point Array for S
0x33A6	LENC_S_B20	0x20	RW	B20 of 8x8 B Control Point Array for S
0x33A7	LENC_S_B21	0x20	RW	B21 of 8x8 B Control Point Array for S

table A-1 sensor control registers (sheet 47 of 80)

address	register name	default value	R/W	description
0x33A8	LENC_S_B22	0x20	RW	B22 of 8x8 B Control Point Array for S
0x33A9	LENC_S_B23	0x20	RW	B23 of 8x8 B Control Point Array for S
0x33AA	LENC_S_B24	0x20	RW	B24 of 8x8 B Control Point Array for S
0x33AB	LENC_S_B25	0x20	RW	B25 of 8x8 B Control Point Array for S
0x33AC	LENC_S_B26	0x20	RW	B26 of 8x8 B Control Point Array for S
0x33AD	LENC_S_B27	0x20	RW	B27 of 8x8 B Control Point Array for S
0x33AE	LENC_S_B30	0x20	RW	B30 of 8x8 B Control Point Array for S
0x33AF	LENC_S_B31	0x20	RW	B31 of 8x8 B Control Point Array for S
0x33B0	LENC_S_B32	0x20	RW	B32 of 8x8 B Control Point Array for S
0x33B1	LENC_S_B33	0x20	RW	B33 of 8x8 B Control Point Array for S
0x33B2	LENC_S_B34	0x20	RW	B34 of 8x8 B Control Point Array for S
0x33B3	LENC_S_B35	0x20	RW	B35 of 8x8 B Control Point Array for S
0x33B4	LENC_S_B36	0x20	RW	B36 of 8x8 B Control Point Array for S
0x33B5	LENC_S_B37	0x20	RW	B37 of 8x8 B Control Point Array for S
0x33B6	LENC_S_B40	0x20	RW	B40 of 8x8 B Control Point Array for S
0x33B7	LENC_S_B41	0x20	RW	B41 of 8x8 B Control Point Array for S
0x33B8	LENC_S_B42	0x20	RW	B42 of 8x8 B Control Point Array for S
0x33B9	LENC_S_B43	0x20	RW	B43 of 8x8 B Control Point Array for S
0x33BA	LENC_S_B44	0x20	RW	B44 of 8x8 B Control Point Array for S
0x33BB	LENC_S_B45	0x20	RW	B45 of 8x8 B Control Point Array for S
0x33BC	LENC_S_B46	0x20	RW	B46 of 8x8 B Control Point Array for S
0x33BD	LENC_S_B47	0x20	RW	B47 of 8x8 B Control Point Array for S
0x33BE	LENC_S_B50	0x20	RW	B50 of 8x8 B Control Point Array for S
0x33BF	LENC_S_B51	0x20	RW	B51 of 8x8 B Control Point Array for S
0x33C0	LENC_S_B52	0x20	RW	B52 of 8x8 B Control Point Array for S
0x33C1	LENC_S_B53	0x20	RW	B53 of 8x8 B Control Point Array for S
0x33C2	LENC_S_B54	0x20	RW	B54 of 8x8 B Control Point Array for S
0x33C3	LENC_S_B55	0x20	RW	B55 of 8x8 B Control Point Array for S

table A-1 sensor control registers (sheet 48 of 80)

address	register name	default value	R/W	description
0x33C4	LENC_S_B56	0x20	RW	B56 of 8x8 B Control Point Array for S
0x33C5	LENC_S_B57	0x20	RW	B57 of 8x8 B Control Point Array for S
0x33C6	LENC_S_B60	0x20	RW	B60 of 8x8 B Control Point Array for S
0x33C7	LENC_S_B61	0x20	RW	B61 of 8x8 B Control Point Array for S
0x33C8	LENC_S_B62	0x20	RW	B62 of 8x8 B Control Point Array for S
0x33C9	LENC_S_B63	0x20	RW	B63 of 8x8 B Control Point Array for S
0x33CA	LENC_S_B64	0x20	RW	B64 of 8x8 B Control Point Array for S
0x33CB	LENC_S_B65	0x20	RW	B65 of 8x8 B Control Point Array for S
0x33CC	LENC_S_B66	0x20	RW	B66 of 8x8 B Control Point Array for S
0x33CD	LENC_S_B67	0x20	RW	B67 of 8x8 B Control Point Array for S
0x33CE	LENC_S_B70	0x20	RW	B70 of 8x8 B Control Point Array for S
0x33CF	LENC_S_B71	0x20	RW	B71 of 8x8 B Control Point Array for S
0x33D0	LENC_S_B72	0x20	RW	B72 of 8x8 B Control Point Array for S
0x33D1	LENC_S_B73	0x20	RW	B73 of 8x8 B Control Point Array for S
0x33D2	LENC_S_B74	0x20	RW	B74 of 8x8 B Control Point Array for S
0x33D3	LENC_S_B75	0x20	RW	B75 of 8x8 B Control Point Array for S
0x33D4	LENC_S_B76	0x20	RW	B76 of 8x8 B Control Point Array for S
0x33D5	LENC_S_B77	0x20	RW	B77 of 8x8 B Control Point Array for S
0x33D6	LENC_S_R00	0x20	RW	R00 of 8x8 B Control Point Array for S
0x33D7	LENC_S_R01	0x20	RW	R01 of 8x8 B Control Point Array for S
0x33D8	LENC_S_R02	0x20	RW	R02 of 8x8 B Control Point Array for S
0x33D9	LENC_S_R03	0x20	RW	R03 of 8x8 B Control Point Array for S
0x33DA	LENC_S_R04	0x20	RW	R04 of 8x8 B Control Point Array for S
0x33DB	LENC_S_R05	0x20	RW	R05 of 8x8 B Control Point Array for S
0x33DC	LENC_S_R06	0x20	RW	R06 of 8x8 B Control Point Array for S
0x33DD	LENC_S_R07	0x20	RW	R07 of 8x8 B Control Point Array for S
0x33DE	LENC_S_R10	0x20	RW	R10 of 8x8 B Control Point Array for S
0x33DF	LENC_S_R11	0x20	RW	R11 of 8x8 B Control Point Array for S

table A-1 sensor control registers (sheet 49 of 80)

address	register name	default value	R/W	description
0x33E0	LENC_S_R12	0x20	RW	R12 of 8x8 B Control Point Array for S
0x33E1	LENC_S_R13	0x20	RW	R13 of 8x8 B Control Point Array for S
0x33E2	LENC_S_R14	0x20	RW	R14 of 8x8 B Control Point Array for S
0x33E3	LENC_S_R15	0x20	RW	R15 of 8x8 B Control Point Array for S
0x33E4	LENC_S_R16	0x20	RW	R16 of 8x8 B Control Point Array for S
0x33E5	LENC_S_R17	0x20	RW	R17 of 8x8 B Control Point Array for S
0x33E6	LENC_S_R20	0x20	RW	R20 of 8x8 R Control Point Array for S
0x33E7	LENC_S_R21	0x20	RW	R21 of 8x8 R Control Point Array for S
0x33E8	LENC_S_R22	0x20	RW	R22 of 8x8 R Control Point Array for S
0x33E9	LENC_S_R23	0x20	RW	R23 of 8x8 R Control Point Array for S
0x33EA	LENC_S_R24	0x20	RW	R24 of 8x8 R Control Point Array for S
0x33EB	LENC_S_R25	0x20	RW	R25 of 8x8 R Control Point Array for S
0x33EC	LENC_S_R26	0x20	RW	R26 of 8x8 R Control Point Array for S
0x33ED	LENC_S_R27	0x20	RW	R27 of 8x8 R Control Point Array for S
0x33EE	LENC_S_R30	0x20	RW	R30 of 8x8 R Control Point Array for S
0x33EF	LENC_S_R31	0x20	RW	R31 of 8x8 R Control Point Array for S
0x33F0	LENC_S_R32	0x20	RW	R32 of 8x8 R Control Point Array for S
0x33F1	LENC_S_R33	0x20	RW	R33 of 8x8 R Control Point Array for S
0x33F2	LENC_S_R34	0x20	RW	R34 of 8x8 R Control Point Array for S
0x33F3	LENC_S_R35	0x20	RW	R35 of 8x8 R Control Point Array for S
0x33F4	LENC_S_R36	0x20	RW	R36 of 8x8 R Control Point Array for S
0x33F5	LENC_S_R37	0x20	RW	R37 of 8x8 R Control Point Array for S
0x33F6	LENC_S_R40	0x20	RW	R40 of 8x8 R Control Point Array for S
0x33F7	LENC_S_R41	0x20	RW	R41 of 8x8 R Control Point Array for S
0x33F8	LENC_S_R42	0x20	RW	R42 of 8x8 R Control Point Array for S
0x33F9	LENC_S_R43	0x20	RW	R43 of 8x8 R Control Point Array for S
0x33FA	LENC_S_R44	0x20	RW	R44 of 8x8 R Control Point Array for S
0x33FB	LENC_S_R45	0x20	RW	R45 of 8x8 R Control Point Array for S

table A-1 sensor control registers (sheet 50 of 80)

address	register name	default value	R/W	description
0x33FC	LENC_S_R46	0x20	RW	R46 of 8x8 R Control Point Array for S
0x33FD	LENC_S_R47	0x20	RW	R47 of 8x8 R Control Point Array for S
0x33FE	LENC_S_R50	0x20	RW	R50 of 8x8 R Control Point Array for S
0x33FF	LENC_S_R51	0x20	RW	R51 of 8x8 R Control Point Array for S
0x3400	LENC_S_R52	0x20	RW	R52 of 8x8 R Control Point Array for S
0x3401	LENC_S_R53	0x20	RW	R53 of 8x8 R Control Point Array for S
0x3402	LENC_S_R54	0x20	RW	R54 of 8x8 R Control Point Array for S
0x3403	LENC_S_R55	0x20	RW	R55 of 8x8 R Control Point Array for S
0x3404	LENC_S_R56	0x20	RW	R56 of 8x8 R Control Point Array for S
0x3405	LENC_S_R57	0x20	RW	R57 of 8x8 R Control Point Array for S
0x3406	LENC_S_R60	0x20	RW	R60 of 8x8 R Control Point Array for S
0x3407	LENC_S_R61	0x20	RW	R61 of 8x8 R Control Point Array for S
0x3408	LENC_S_R62	0x20	RW	R62 of 8x8 R Control Point Array for S
0x3409	LENC_S_R63	0x20	RW	R63 of 8x8 R Control Point Array for S
0x340A	LENC_S_R64	0x20	RW	R64 of 8x8 R Control Point Array for S
0x340B	LENC_S_R65	0x20	RW	R65 of 8x8 R Control Point Array for S
0x340C	LENC_S_R66	0x20	RW	R66 of 8x8 R Control Point Array for S
0x340D	LENC_S_R67	0x20	RW	R67 of 8x8 R Control Point Array for S
0x340E	LENC_S_R70	0x20	RW	R70 of 8x8 R Control Point Array for S
0x340F	LENC_S_R71	0x20	RW	R71 of 8x8 R Control Point Array for S
0x3410	LENC_S_R72	0x20	RW	R72 of 8x8 R Control Point Array for S
0x3411	LENC_S_R73	0x20	RW	R73 of 8x8 R Control Point Array for S
0x3412	LENC_S_R74	0x20	RW	R74 of 8x8 R Control Point Array for S
0x3413	LENC_S_R75	0x20	RW	R75 of 8x8 R Control Point Array for S
0x3414	LENC_S_R76	0x20	RW	R76 of 8x8 R Control Point Array for S
0x3415	LENC_S_R77	0x20	RW	R77 of 8x8 R Control Point Array for S

table A-1 sensor control registers (sheet 51 of 80)

address	register name	default value	R/W	description
0x3416	LENC_CTRL10	0x0D	RW	Bit[7:4]: Not used Bit[3]: m_nq_option L/S/VS employ the same m_nq of L Bit[2]: less_1x_en_l (active high) Less than 1x gain enable for L/VS Bit[1]: rand_bit_en_l (active high) Add random enable for L/VS Bit[0]: auto_q_en_l (active high) Auto calculation Q enable for L/VS
0x3417	MAXGAIN_L_BYTE1	0x00	RW	Upper Gain Threshold for Auto Q for L/VS High Byte
0x3418	MAXGAIN_L_BYTE0	0x60	RW	Upper Gain Threshold for Auto Q for L/VS Low Byte
0x3419	MINGAIN_L_BYTE1	0x00	RW	Lower Gain Threshold for Auto Q for L/VS High Byte
0x341A	MINGAIN_L_BYTE0	0x20	RW	Lower Gain Threshold for Auto Q for L/VS Low Byte
0x341B	MINQ_L	0x18	RW	Minimum Q for Auto Q When Gain Larger Than Maxgain for L/VS
0x341C	MAXQ_L	0x40	RW	Maximum Q for Auto Q When Gain Smaller Than Mingain for L/VS
0x341D	BR_HSCALE_BYTE1	0x02	RW	H Scale for Blue/Red Channel, Same for All Exposures High Byte
0x341E	BR_HSCALE_BYTE0	0x0A	RW	H Scale for Blue/Red Channel, Same for All Exposures Low Byte
0x341F	BR_VSCALE_BYTE1	0x02	RW	V Scale for Blue/Red Channel, Same for All Exposures High Byte
0x3420	BR_VSCALE_BYTE0	0xF4	RW	V Scale for Blue/Red Channel, Same for All Exposures Low Byte
0x3421	G_HSCALE_BYTE1	0x02	RW	H Scale for Green Channel, Same for All Exposures High Byte
0x3422	G_HSCALE_BYTE0	0x0A	RW	H Scale for Green Channel, Same for All Exposures Low Byte
0x3423	G_VSCALE_BYTE1	0x01	RW	V Scale for Green Channel, Same for All Exposures High Byte
0x3424	G_VSCALE_BYTE0	0x0A	RW	V Scale for Green Channel, Same for All Exposures Low Byte

table A-1 sensor control registers (sheet 52 of 80)

address	register name	default value	R/W	description
0x3425	LENC_CTRL11	0x05	RW	Bit[7:3]: Not used Bit[2]: less_1x_en_s (active high) Less than 1x gain enable for S Bit[1]: rand_bit_en_s (active high) Add random enable for S Bit[0]: auto_q_en_s (active high) Auto calculation Q enable for S
0x3426	MAXGAIN_S_BYTE1	0x00	RW	Upper Gain Threshold for Auto Q for S High Byte
0x3427	MAXGAIN_S_BYTE0	0x60	RW	Upper Gain Threshold for Auto Q for S Low Byte
0x3428	MINGAIN_S_BYTE1	0x00	RW	Lower Gain Threshold for Auto Q for S High Byte
0x3429	MINGAIN_S_BYTE0	0x20	RW	Lower Gain Threshold for Auto Q for S Low Byte
0x342A	MINQ_S	0x18	RW	Minimum Q for Auto Q When Gain Larger Than Maxgain for S
0x342B	MAX_Q	0x40	RW	Maximum Q for Auto Q When Gain Larger Than Mingain for S
0x3430	LVDS_R0	0x2A	RW	Bit[7]: Not used Bit[6]: r_syc_cod_man Sync code manual enable Bit[5]: r_syncd_en Bit[4]: lvds_pclk_inv Invert lvds_pclk_o Bit[3]: r_chid_en Channel ID enable in sync per lane mode Bit[2]: lvds_f CCIR parameter F Bit[1]: sav_first_en 0: EAV first 1: SAV first Bit[0]: sync_code_mod 0: Only one sync code 1: Sync code per lane
0x3431	LVDS_R2	0x00	RW	Dummy Data0 High Nibble
0x3432	LVDS_R3	0x80	RW	Dummy Data0 Low Byte
0x3433	LVDS_R4	0x00	RW	Dummy Data1 High Nibble
0x3434	LVDS_R5	0x10	RW	Dummy Data1 Low Byte
0x3435	LVDS_R6	0xAA	RW	frame_st
0x3436	LVDS_R7	0x55	RW	frame_ed

table A-1 sensor control registers (sheet 53 of 80)

address	register name	default value	R/W	description
0x3437	LVDS_R8	0x99	RW	line_st
0x3438	LVDS_R9	0x66	RW	line_ed
0x3439	LVDS_RA	0x08	RW	Bit[7:4]: Not used Bit[3]: r_bit_flip Bit[2]: r_hts_man_en Bit[1]: r_ln2_sel Bit[0]: r_chk_pcnt
0x343A	LVDS_RB	0x88	RW	Bit[7]: sleep_en Bit[6]: Not used Bit[5]: r_frame_rst_en Bit[4:0]: r_ln_end_dly
0x343B	LVDS_RC	0x00	RW	r_blk_time High Nibble
0x343C	LVDS_RD	0x02	RW	r_blk_time Low Byte
0x343D	LVDS_RE	0x00	RW	r_hts_man High Byte
0x343E	LVDS_RF	0x00	RW	r_hts_man Low Byte
0x343F	LVDS_LANE_NR	0x04	RW	Active LVDS Lanes
0x3440	MIPI_CTRL00	0x04	RW	Bit[7]: Not used Bit[6]: vertical_en Bit[5]: gate_sc_en 0: Clock lane is free running 1: Gate clock lane when there is no packet to transmit Bit[4]: line_sync_en 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3:0]: Not used
0x3441	MIPI_CTRL01	0x00	RW	Bit[7]: Not used Bit[6]: spkt_dt_sel Use dt_spkt as short packet data Bit[5]: first_bit Change clock lane first bit 0: Output 8'h55 1: Output 8'hAA Bit[4:2]: Not used Bit[1]: lpx_p_sel LPX select for pclk domain 0: Auto calculate lpx_p, unit pclk2x cycle 1: Use lpx_p min[7:0] Bit[0]: Not used

table A-1 sensor control registers (sheet 54 of 80)

address	register name	default value	R/W	description
0x3442	MIPI_CTRL02	0x00	RW	Bit[7]: hs_prepare_s_el 0: Auto calculate T_hs_prepare, unit pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare_sel 0: Auto calculate T_clk_prepare, unit pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post_sel 0: Auto calculate T_clk_post, unit pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail_sel 0: Auto calculate T_clk_trail, unit pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: hs_exit_sel 0: Auto calculate T_hs_exit, unit pclk2x 1: Use hs_exit_min_o[7:0] Bit[2]: hs_zero_sel 0: Auto calculate T_hs_zero, unit pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail_sel 0: Auto calculate T_hs_trail, unit pclk2x 1: Use hs_trail_min_o[7:0] Bit[0]: clk_zero_sel 0: Auto calculate T_clk_zero, unit pclk2x 1: Use clk_zero_min_o[7:0]
0x3443	MIPI_CTRL03	0x00	RW	Bit[7:4]: Not used Bit[3]: manu_offset t_perio_manu offset SMIA Bit[2]: r_manu_half2one t_period_half to 1 SMIA Bit[1]: clk_pre_half Bit[0]: hs_pre_half

table A-1 sensor control registers (sheet 55 of 80)

address	register name	default value	R/W	description
0x3444	MIPI_CTRL04	0x48	RW	Bit[7:4]: lane_num_man Bit[3]: lane_num_man_en Bit[2]: lane4_6b_en_r 0: Not used 1: Support 4,7,8-lane 6-bit Bit[1]: Vsub_s 0: Valid in behind 1: Valid in front Bit[0]: vfifo_8x 0: Valid = 0 1: Valid = 8
0x3445	MIPI_CTRL05	0x00	RW	Bit[7:4]: Not used Bit[3]: lpda_retim_manu 0: Not used 1: Manual Bit[2]: lpda_retim_sel Bit[1]: lpck_retim_manu 0: Not used 1: Manual Bit[0]: lpck_retim_sel
0x3446	MIPI_CTRL06	0x10	RW	Bit[7:5]: Not used Bit[4]: pu_mark_en Power up mark1 enable Bit[3]: mipi_remot_rst Bit[2]: mipi_susp Bit[1]: smia_lane_ch_en Bit[0]: tx_lsb_first 0: High bit first 1: Low power transmit low bit first
0x3447	MIPI_CTRL07	0x03	RW	Bit[7:4]: Not used Bit[3:0]: sw_t_lpx
0x3448	MIPI_CTRL08	0x0A	RW	Bit[7:0]: wkup_dly Mark1 wakeup delay/2^10
0x3449	MIPI_CTRL10	0xFF	RW	Bit[7:0]: fcnt_max[15:8] High byte of maximum frame counter frame sync short packet
0x344A	MIPI_CTRL11	0xFF	RW	Bit[7:0]: fcnt max[7:0] Low byte of maximum frame counter of frame sync short packet
0x344B	MIPI_CTRL13	0x00	RW	Bit[7:3]: Not used Bit[2]: vc_sel_sel Bit[1:0]: Virtual channel ID

table A-1 sensor control registers (sheet 56 of 80)

address	register name	default value	R/W	description
0x344C	MIPI_CTRL14	0x2A	RW	Bit[7]: Not used Bit[6]: lpkt_dt_sel 0: Use mipi_dt 1: Use dt_man_o as long packet data Bit[5:0]: dt_man
0x344D	MIPI_CTRL15	0x00	RW	Bit[7]: Not used Bit[6]: pclk_inv 0: Use falling edge of mipi_pclk_o to generate MIPI bus to PHY 1: Use rising edge of mipi_pclk_o to generate MIPI bus to PHY Bit[5:0]: dt_spkt Data type for dummy line
0x344E	MIPI_CTRL16	0x52	RW	Bit[7:6]: Not used Bit[5:0]: emb_dt_manu Set embedded data type
0x344F	RSVD	–	–	Reserved
0x3450	MIPI_CTRL18	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_zero_min[9:8]
0x3451	MIPI_CTRL19	0x00	RW	Bit[7:0]: hs_zero_min[7:0]
0x3452	MIPI_CTRL1A	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_trail_min[9:8]
0x3453	MIPI_CTRL1B	0x3C	RW	Bit[7:0]: hs_trail_min[7:0]
0x3454	MIPI_CTRL1C	0x01	RW	Bit[7:2]: Not used Bit[1:0]: clk_zero_min[9:8]
0x3455	MIPI_CTRL1D	0x2C	RW	Bit[7:0]: clk_zero_min[7:0]
0x3456	MIPI_CTRL1E	0x5F	RW	Bit[7:0]: clk_prepare_max Maximum value of clk_prepare, unit ns
0x3457	MIPI_CTRL1F	0x26	RW	Bit[7:0]: clk_prepare_min Minimum value of clk_prepare clk_prepare_real = clk_prepare_min_o + Tui*ui clk_prepare_min_o
0x3458	MIPI_CTRL20	0x00	RW	Bit[7:2]: Not used Bit[1:0]: clk_post_min[9:8] High byte of minimum value of clk_post, unit ns

table A-1 sensor control registers (sheet 57 of 80)

address	register name	default value	R/W	description
0x3459	MIPI_CTRL21	0x3C	RW	Bit[7:0]: clk_post_min[7:0] Low byte of minimum value of clk_post clk_post_real = clk_post_min_o + Tui*ui clk_post_min_o
0x345A	MIPI_CTRL22	0x00	RW	Bit[7:2]: Not used Bit[1:0]: clk_trail_min[9:8] High byte of minimum value of clk_trail, unit ns
0x345B	MIPI_CTRL23	0x3C	RW	Bit[7:0]: clk_trail_min[7:0] Low byte of minimum value of clk_trail clk_trail_real = clk_trail_min o + Tui*ui clk_trail_min_o
0x345C	MIPI_CTRL24	0x00	RW	Bit[7:2]: Not used Bit[1:0]: lpx_p_min[9:8] High byte of minimum value of lpx_p, unit ns
0x345D	MIPI_CTRL25	0x32	RW	Bit[7:0]: lpx_p_min[7:0] Low byte of minimum value of lpx_p lpx_p_real = lpx_p_min_o + Tui*ui lpx_p_min_o
0x345E	MIPI_CTRL26	0x28	RW	Bit[7:0]: hs_prepare_min Minimum value of hs_prepare, unit ns
0x345F	MIPI_CTRL27	0x55	RW	Bit[7:0]: hs_prepare_max Maximum value of hs_prepare hs_prepare_real = hs_prepare_max_o +Tui*ui hs_prepare_max_o
0x3460	MIPI_CTRL28	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_exit_min[9:8]
0x3461	MIPI_CTRL29	0x64	RW	Bit[7:0]: hs_exit_min[7:0] Low byte of minimum value of hs_exit hs_exit_real = hs_exit_min_o
0x3462	MIPI_CTRL2A	0x0A	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_zero_min Minimum UI value of hs_zero, unit UI

table A-1 sensor control registers (sheet 58 of 80)

address	register name	default value	R/W	description
0x3463	MIPI_CTRL2B	0x04	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_trail_min Minimum UI value of hs_trail, unit UI
0x3464	MIPI_CTRL2C	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_zero_min Minimum UI value of clk_zero, unit UI
0x3465	MIPI_CTRL2D	0x00	RW	Bit[7:4]: ui_clk_prepare_max Maximum UI value of clk_prepare, unit UI Bit[3:0]: ui_clk_prepare_min Minimum UI value of clk_prepare, unit UI
0x3466	MIPI_CTRL2E	0x34	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_post_min Minimum UI value of clk_post, unit UI
0x3467	MIPI_CTRL2F	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_trail_min Minimum UI value of clk_trail, unit UI
0x3468	MIPI_CTRL30	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_lpx_p_min Minimum UI value of lpx_p, unit UI
0x3469	MIPI_CTRL31	0x64	RW	Bit[7:4]: ui_hs_prepare_max Maximum UI value of hs_prepare, unit UI Bit[3:0]: ui_hs_prepare_min Minimum UI value of hs_prepare, unit UI
0x346A	MIPI_CTRL32	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_exit_min Minimum UI value of hs_exit, unit UI
0x346B	MIPI_CTRL33	0x18	RW	Bit[7:6]: Not used Bit[5:0]: mipi_pkt_star_size
0x346C	MIPI_CTRL36	0x00	RW	Bit[7:1]: Not used Bit[0]: smia_cal_en
0x346D	MIPI_CTRL37	0x14	RW	Bit[7:0]: pclk_period Period of pclk2x, pclk_div=1 and 1-bit decimal

table A-1 sensor control registers (sheet 59 of 80)

address	register name	default value	R/W	description
0x346E	MIPI_CTRL38	0x00	RW	Bit[7]: Not used Bit[6]: lp_dir_man0 0: Output 1: Input Bit[5]: lp_p0 Lane 1 manual out p Bit[4]: lp_n0 Lane1 manual out n Bit[3]: lp_sel1 0: Auto generate mipi_lp_dir2_o 1: Use lp_dir_man2_o to be mipi_lp_dir2_o Bit[2]: lp_dir_man1 0: Output 1: Input Bit[1]: lp_p1 Lane 1 manual out p Bit[0]: lp_n1 Lane 1 manual out n
0x346F	MIPI_CTRL39	0x00	RW	Bit[7]: lp_sel2 0: Auto generate mipi_lp_dir1_o 1: Use lp_dir_man1_o to be mipi_lp_dir1_o Bit[6]: lp_dir_man2 0: Output 1: Input Bit[5]: lp_p2 Lane 2 manual out p Bit[4]: lp_n2 lane 2 manual out n Bit[3]: lp_sel3 0: Auto generate mipi_lp_dir2_o 1: Use lp_dir_man2_o to be mipi_lp__dir2_o Bit[2]: lp_dir_man3 0: Output 1: Input Bit[1]: lp_p3 Lane 3 manual out p Bit[0]: lp_n3 Lane 3 manual out n
0x3472	MIPI_CTRL3C	0x02	RW	Bit[7:4]: Not used Bit[3:0]: t_clk_pre

table A-1 sensor control registers (sheet 60 of 80)

address	register name	default value	R/W	description
0x3473	MIPI_CTRL3D	0x00	RW	Bit[7]: lp_ck_se0 0: Auto generate mipi_ck_lp_dir0_o 1: Use lp_ck_dir_man0 to be mipi_ck_lp_dir0_o Bit[6]: lp_ck_dir_man0 0: Input 1: Output Bit[5]: lp_ck_p0 Bit[4]: lp_ck_n0 Bit[3]: lp_ck_sel1 0: Auto generate mipi_ck_lp_dir1_o 1: Use p_ck_dir_man1 to be mipi_ck_lp_dir1_o Bit[2]: lp_ck_dir_man1 0: Input 1: Output Bit[1]: lp_ck_p1 Bit[0]: lp_ck_n1
0x3474	MIPI_CTRL4A	0x27	RW	Bit[7:6]: Not used Bit[5]: slp_lp_pon_man Set for power up Bit[4]: slp_lp_pon_da Bit[3]: slp_lp_pon_ck_da Bit[2]: mipi_slpst_man MIPI bus status manual control enable in sleep mode Bit[1]: slpst_clk_lane Bit[0]: slpst_data_lane
0x3475	MIPI_CTRL4B	0x07	RW	Bit[7:3]: Not used Bit[2]: line_st_sel 0: Line starts after HREF 1: Line starts after FIFO starts Bit[1]: clk_start_sel 0: Clock starts after SOF 1: Clock starts after reset Bit[0]: sof_sel 0: Frame starts after HREF 1: Frame starts after SOF

table A-1 sensor control registers (sheet 61 of 80)

address	register name	default value	R/W	description
0x3476	MIPI_CTRL4C	0x03	RW	Bit[7]: sof_sel Bit[6]: smia_fcnt_sel Bit[5]: prbs_en Bit[4]: mipi_test MIPI high speed only test mode enable Bit[3]: fcnt_inact Set frame count to inactive mode (keep 0) Bit[2:0]: Not used
0x3477	MIPI_CTRL4D	0xB6	RW	Bit[7:0]: Pattern data lane
0x3478	MIPI_CTRL4E	0x10	RW	Bit[7:0]: r_fe_dly Last packet to frame end delay / 2
0x3479	MIPI_CTRL4F	0x55	RW	Bit[7:2]: Not used Bit[1:0]: ck_patten_data
0x3493~ 0x3494	RSVD	–	–	Reserved
0x3495	R_MODE_CTRL	0x40	RW	Bit[7]: program_dis 1: Disable programming Bit[6]: mode_select 0: Auto mode 1: Manual mode Bit[5:0]: Memory select Used to choose exact OTP bank 000000: Select memory 1 000001: Select memory 2 Others: Not used
0x3496	R_START_ADDRESS	0x00	RW	Start Address for Manual Mode
0x3497	R_END_ADDRESS	0x0F	RW	End Address for Manual Mode
0x3498	R_PS2CS	0x03	RW	PS to CSB Time Control by Sclk
0x3499	LD_WR_GAP	0x01	RW	Load Write Register Gap
0x349A	LOAD_CTRL	0x01	RW	OTP Load Setting Enable
0x349B	OTP_PROGRAM	0x00	RW	Write 1 to Program Auto Reset
0x349C	OTP_READ	0x00	RW	Write 1 to Read Auto Reset

table A-1 sensor control registers (sheet 62 of 80)

address	register name	default value	R/W	description
0x349D	R_OTP_STATUS	–	R	Bit[7:2]: Not used Bit[1]: r_otp_load_o 0: Not used 1: Loading time Bit[0]: r_otp_prog_o 0: Not used 1: Programing time
0x349E	DATA_0	0x00	RW	Register Buffer OTP data_0
0x349F	DATA_1	0x00	RW	Register Buffer OTP data_1
0x34A0	DATA_2	0x00	RW	Register Buffer OTP data_2
0x34A1	DATA_3	0x00	RW	Register Buffer OTP data_3
0x34A2	DATA_4	0x00	RW	Register Buffer OTP data_4
0x34A3	DATA_5	0x00	RW	Register Buffer OTP data_5
0x34A4	DATA_6	0x00	RW	Register Buffer OTP data_6
0x34A5	DATA_7	0x00	RW	Register Buffer OTP data_7
0x34A6	DATA_8	0x00	RW	Register Buffer OTP data_8
0x34A7	DATA_9	0x00	RW	Register Buffer OTP data_9
0x34A8	DATA_A	0x00	RW	Register Buffer OTP data_a
0x34A9	DATA_B	0x00	RW	Register Buffer OTP data_b
0x34AA	DATA_C	0x00	RW	Register Buffer OTP data_c
0x34AB	DATA_D	0x00	RW	Register Buffer OTP data_d
0x34AC	DATA_E	0x00	RW	Register Buffer OTP data_e
0x34AD	DATA_F	0x00	RW	Register Buffer OTP data_f
0x34AE	DATA_10	0x00	RW	Register Buffer OTP data_10
0x34AF	DATA_11	0x00	RW	Register Buffer OTP data_11
0x34B0	DATA_12	0x00	RW	Register Buffer OTP data_12
0x34B1	DATA_13	0x00	RW	Register Buffer OTP data_13
0x34B2	DATA_14	0x00	RW	Register Buffer OTP data_14
0x34B3	DATA_15	0x00	RW	Register Buffer OTP data_15
0x34B4	DATA_16	0x00	RW	Register Buffer OTP data_16
0x34B5	DATA_17	0x00	RW	Register Buffer OTP data_17
0x34B6	DATA_18	0x00	RW	Register Buffer OTP data_18

table A-1 sensor control registers (sheet 63 of 80)

address	register name	default value	R/W	description
0x34B7	DATA_19	0x00	RW	Register Buffer OTP data_19
0x34B8	DATA_1A	0x00	RW	Register Buffer OTP data_1a
0x34B9	DATA_1B	0x00	RW	Register Buffer OTP data_1b
0x34BA	DATA_1C	0x00	RW	Register Buffer OTP data_1c
0x34BB	DATA_1D	0x00	RW	Register Buffer OTP data_1d
0x34BC	DATA_1E	0x00	RW	Register Buffer OTP data_1e
0x34BD	DATA_1F	0x00	RW	Register Buffer OTP data_1f
0x4000	STATS_ROW_START_H	0x00	RW	ROI setting
0x4001	STATS_ROW_START_L	0x04	RW	ROI setting
0x4002	STATS_COL_START_H	0x00	RW	ROI setting
0x4003	STATS_COL_START_L	0x04	RW	ROI setting
0x4004	STATS_ROW_STOP_H	0x04	RW	ROI setting
0x4005	STATS_ROW_STOP_L	0x30	RW	ROI setting
0x4006	STATS_COL_STOP_H	0x04	RW	ROI setting
0x4007	STATS_COL_STOP_L	0xFF	RW	ROI setting
0x4008	STATS_CTRL	–	R	Bit[7:6]: Not used Bit[5:4]: mode 00: Linear mode 01: Mixed mode 10: Binary log 11: Not used Bit[3:0]: Bayer mask setting
0x4009	RED_ACC_H	–	R	Red Accumulated Pixel Value High Byte of xxxx xxxx xxx.n nnnn Where x*2^n (see register **0x400A** for low byte)
0x400A	RED_ACC_L	–	R	Red Accumulated Pixel Value Low Byte
0x400B	GR1_ACC_H	–	R	Green 1 Accumulated Pixel Value High Byte of xxxx xxxx xxx.n nnnn Where x*2^n
0x400C	GR1_ACC_L	–	R	Green 1 Accumulated Pixel Value Low Byte
0x400D	GR2_ACC_H	–	R	Green 2 Accumulated Pixel Value High Byte of xxxx xxxx xxx.n nnnn Where x*2^n
0x400E	GR2_ACC_L	–	R	Green 2 Accumulated Pixel Value Low Byte
0x400F	BLU_ACC_H	–	R	Blue Accumulated Pixel Value High Byte of xxxx xxxx xxx.n nnnn Where x*2^n

table A-1 sensor control registers (sheet 64 of 80)

address	register name	default value	R/W	description
0x4010	BLU_ACC_L	–	R	Blue Accumulated Pixel Value Low Byte
0x4011	PIX_CNT_2	–	R	Valid Pixel Count High Byte
0x4012	PIX_CNT_1	–	R	Valid Pixel Count Middle Byte
0x4013	PIX_CNT_0	–	R	Valid Pixel Count Low Byte
0x4014	BIN_00_2_SHORTEST	–	R	Bin 0 of Shortest Histogram High Byte
0x4015	BIN_00_1_SHORTEST	–	R	Bin 0 of Shortest Histogram Middle Byte
0x4016	BIN_00_0_SHORTEST	–	R	Bin 0 of Shortest Histogram Low Byte
0x4017	BIN_01_H_SHORTEST	–	R	Bin 1 of Shortest Histogram High Byte
0x4018	BIN_01_L_SHORTEST	–	R	Bin 1 of Shortest Histogram Low Byte
0x4019	BIN_02_H_SHORTEST	–	R	Bin 2 of Shortest Histogram High Byte
0x401A	BIN_02_L_SHORTEST	–	R	Bin 2 of Shortest Histogram Low Byte
0x401B	BIN_03_H_SHORTEST	–	R	Bin 3 of Shortest Histogram High Byte
0x401C	BIN_03_L_SHORTEST	–	R	Bin 3 of Shortest Histogram Low Byte
0x401D	BIN_04_H_SHORTEST	–	R	Bin 4 of Shortest Histogram High Byte
0x401E	BIN_04_L_SHORTEST	–	R	Bin 4 of Shortest Histogram Low Byte
0x401F	BIN_05_H_SHORTEST	–	R	Bin 5 of Shortest Histogram High Byte
0x4020	BIN_05_L_SHORTEST	–	R	Bin 5 of Shortest Histogram Low Byte
0x4021	BIN_06_H_SHORTEST	–	R	Bin 6 of Shortest Histogram High Byte
0x4022	BIN_06_L_SHORTEST	–	R	Bin 6 of Shortest Histogram Low Byte
0x4023	BIN_07_H_SHORTEST	–	R	Bin 7 of Shortest Histogram High Byte
0x4024	BIN_07_L_SHORTEST	–	R	Bin 7 of Shortest Histogram Low Byte
0x4025	BIN_08_H_SHORTEST	–	R	Bin 8 of Shortest Histogram High Byte
0x4026	BIN_08_L_SHORTEST	–	R	Bin 8 of Shortest Histogram Low Byte
0x4027	BIN_09_H_SHORTEST	–	R	Bin 9 of Shortest Histogram High Byte
0x4028	BIN_09_L_SHORTEST	–	R	Bin 9 of Shortest Histogram Low Byte
0x4029	BIN_10_H_SHORTEST	–	R	Bin 10 of Shortest Histogram High Byte
0x402A	BIN_10_L_SHORTEST	–	R	Bin 10 of Shortest Histogram Low Byte
0x402B	BIN_11_H_SHORTEST	–	R	Bin 11 of Shortest Histogram High Byte

table A-1 sensor control registers (sheet 65 of 80)

address	register name	default value	R/W	description
0x402C	BIN_11_L_SHORTEST	–	R	Bin 11 of Shortest Histogram Low Byte
0x402D	BIN_12_H_SHORTEST	–	R	Bin 12 of Shortest Histogram High Byte
0x402E	BIN_12_L_SHORTEST	–	R	Bin 12 of Shortest Histogram Low Byte
0x402F	BIN_13_H_SHORTEST	–	R	Bin 13 of Shortest Histogram High Byte
0x4030	BIN_13_L_SHORTEST	–	R	Bin 13 of Shortest Histogram Low Byte
0x4031	BIN_14_H_SHORTEST	–	R	Bin 14 of Shortest Histogram High Byte
0x4032	BIN_14_L_SHORTEST	–	R	Bin 14 of Shortest Histogram Low Byte
0x4033	BIN_00_H_MID	–	R	Bin 0 of Mid Histogram High Byte
0x4034	BIN_00_L_MID	–	R	Bin 0 of Mid Histogram Low Byte
0x4035	BIN_01_H_MID	–	R	Bin 1 of Mid Histogram High Byte
0x4036	BIN_01_L_MID	–	R	Bin 1 of Mid Histogram Low Byte
0x4037	BIN_02_H_MID	–	R	Bin 2 of Mid Histogram High Byte
0x4038	BIN_02_L_MID	–	R	Bin 2 of Mid Histogram Low Byte
0x4039	BIN_03_H_MID	–	R	Bin 3 of Mid Histogram High Byte
0x403A	BIN_03_L_MID	–	R	Bin 3 of Mid Histogram Low Byte
0x403B	BIN_04_H_MID	–	R	Bin 4 of Mid Histogram High Byte
0x403C	BIN_04_L_MID	–	R	Bin 4 of Mid Histogram Low Byte
0x403D	BIN_05_H_MID	–	R	Bin 5 of Mid Histogram High Byte
0x403E	BIN_05_L_MID	–	R	Bin 5 of Mid Histogram Low Byte
0x403F	BIN_06_H_MID	–	R	Bin 6 of Mid Histogram High Byte
0x4040	BIN_06_L_MID	–	R	Bin 6 of Mid Histogram Low Byte
0x4041	BIN_07_H_MID	–	R	Bin 7 of Mid Histogram High Byte
0x4042	BIN_07_L_MID	–	R	Bin 7 of Mid Histogram Low Byte
0x4043	BIN_08_H_MID	–	R	Bin 8 of Mid Histogram High Byte
0x4044	BIN_08_L_MID	–	R	Bin 8 of Mid Histogram Low Byte
0x4045	BIN_09_H_MID	–	R	Bin 9 of Mid Histogram High Byte
0x4046	BIN_09_L_MID	–	R	Bin 9 of Mid Histogram Low Byte
0x4047	BIN_10_H_MID	–	R	Bin 10 of Mid Histogram High Byte

table A-1 sensor control registers (sheet 66 of 80)

address	register name	default value	R/W	description
0x4048	BIN_10_L_MID	–	R	Bin 10 of Mid Histogram Low Byte
0x4049	BIN_11_H_MID	–	R	Bin 11 of Mid Histogram High Byte
0x404A	BIN_11_L_MID	–	R	Bin 11 of Mid Histogram Low Byte
0x404B	BIN_12_H_MID	–	R	Bin 12 of Mid Histogram High Byte
0x404C	BIN_12_L_MID	–	R	Bin 12 of Mid Histogram Low Byte
0x404D	BIN_13_H_MID	–	R	Bin 13 of Mid Histogram High Byte
0x404E	BIN_13_L_MID	–	R	Bin 13 of Mid Histogram Low Byte
0x404F	BIN_14_H_MID	–	R	Bin 14 of Mid Histogram High Byte
0x4050	BIN_14_L_MID	–	R	Bin 14 of Mid Histogram Low Byte
0x4051	BIN_15_H_MID	–	R	Bin 15 of Mid Histogram High Byte
0x4052	BIN_15_L_MID	–	R	Bin 15 of Mid Histogram Low Byte
0x4053	BIN_00_2_LONGEST	–	R	Bin 0 of Longest Histogram High Byte
0x4054	BIN_00_1_LONGEST	–	R	Bin 0 of Longest Histogram Middle Byte
0x4055	BIN_00_0_LONGEST	–	R	Bin 0 of Longest Histogram Low Byte
0x4056	BIN_01_H_LONGEST	–	R	Bin 1 of Longest Histogram High Byte
0x4057	BIN_01_L_LONGEST	–	R	Bin 1 of Longest Histogram Low Byte
0x4058	BIN_02_H_LONGEST	–	R	Bin 2 of Longest Histogram High byte
0x4059	BIN_02_L_LONGEST	–	R	Bin 2 of Longest Histogram Low Byte
0x405A	BIN_03_H_LONGEST	–	R	Bin 3 of Longest Histogram High Byte
0x405B	BIN_03_L_LONGEST	–	R	Bin 3 of Longest Histogram Low Byte
0x405C	BIN_04_H_ LONGEST	–	R	Bin 4 of Longest Histogram High Byte
0x405D	BIN_04_L_LONGEST	–	R	Bin 4 of Longest Histogram Low Byte
0x405E	BIN_05_H_LONGEST	–	R	Bin 5 of Longest Histogram High Byte
0x405F	BIN_05_L_LONGEST	–	R	Bin 5 of Longest Histogram Low Byte
0x4060	BIN_06_H_LONGEST	–	R	Bin 6 of Longest Histogram High Byte
0x4061	BIN_06_L_LONGEST	–	R	Bin 6 of Longest Histogram Low Byte
0x4062	BIN_07_H_LONGEST	–	R	Bin 7 of Longest Histogram High Byte
0x4063	BIN_07_L_LONGEST	–	R	Bin 7 of Longest Histogram Low Byte

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address	register name	default value	R/W	description
0x4064	BIN_08_H_LONGEST	–	R	Bin 8 of Longest Histogram High Byte
0x4065	BIN_08_L_LONGEST	–	R	Bin 8 of Longest Histogram Low Byte
0x4066	BIN_09_H_LONGEST	–	R	Bin 9 of Longest Histogram High Byte
0x4067	BIN_09_L_LONGEST	–	R	Bin 9 of Longest Histogram Low Byte
0x4068	BIN_10_H_LONGEST	–	R	Bin 10 of Longest Histogram High Byte
0x4069	BIN_10_L_LONGEST	–	R	Bin 10 of Longest Histogram Low Byte
0x406A	BIN_11_H_LONGEST	–	R	Bin 11 of Longest Histogram High Byte
0x406B	BIN_11_L_LONGEST	–	R	Bin 11 of Longest Histogram Low Byte
0x406C	BIN_12_H_LONGEST	–	R	Bin 12 of Longest Histogram High Byte
0x406D	BIN_12_L_LONGEST	–	R	Bin 12 of Longest Histogram Low Byte
0x406E	BIN_13_H_LONGEST	–	R	Bin 13 of Longest Histogram High Byte
0x406F	BIN_13_L_LONGEST	–	R	Bin 13 of Longest Histogram Low Byte
0x4070	BIN_14_H_LONGEST	–	R	Bin 14 of Longest Histogram High Byte
0x4071	BIN_14_L_LONGEST	–	R	Bin 14 of Longest Histogram Low Byte
0x7000	EXPO_CALC_CTRL 1 HIGH BYTE	0x1F	RW	Bit[7:6]: cg_en_s Enable short CG 00: Off 01: On 10: Not used 11: Auto high_temp Bit[5:4]: dgain_en_s Enable short digital gain 00: Off 01: On 10: Not used 11: Auto high_temp Bit[3:2]: again_en_s Enable short analog gain 00: Off 01: On 10: Not used 11: Auto high_temp Bit[1:0]: expo_en_s Enable short exposure 00: Off 01: On 10: Not used 11: Auto high_temp

table A-1 sensor control registers (sheet 68 of 80)

address	register name	default value	R/W	description
0x7001	EXPO_CALC_CTRL 1 LOW BYTE	0xDF	RW	Bit[7:6]: cg_en_l Enable long CG 00: Off 01: On 10: Not used 11: Auto high_temp Bit[5:4]: dgain_en_l Enable long digital gain 00: Off 01: On 10: Not used 11: Auto high_temp Bit[3:2]: again_en_l Enable long analog gain 00: Off 01: On 10: Not used 11: Auto high_temp Bit[1:0]: expo_en_l Enable long exposure 00: Off 01: On 10: Not used 11: Auto high_temp

table A-1 sensor control registers (sheet 69 of 80)

address	register name	default value	R/W	description
0x7002	EXPO_CALC_CTRL 2 HIGH BYTE	0xAA	RW	Bit[7:6]: pri_mode_vs Very short priority 00: Conversion gain, analog gain, exposure time and digital gain 01: Analog gain, conversion gain, exposure time and digital gain 10: Exposure time, conversion gain, analog gain and digital gain (default) 11: Exposure time, analog gain, conversion gain and digital gain Bit[5:4]: pri_mode_s Short priority 00: Conversion gain, analog gain, exposure time and digital gain 01: Analog gain, conversion gain, exposure time and digital gain 10: Exposure time, conversion gain, analog gain and digital gain (default) 11: Exposure time, analog gain, conversion gain and digital gain Bit[3:2]: pri_mode_l Long priority 00: Conversion gain, analog gain, exposure time and digital gain 01: Analog gain, conversion gain, exposure time and digital gain 10: Exposure time, conversion gain, analog gain and digital gain (default) 11: Exposure time, analog gain, conversion gain and digital gain Bit[1:0]: Exposure alignment 00: Bright 01: Not used 10: Dark 11: Not used

table A-1 sensor control registers (sheet 70 of 80)

address	register name	default value	R/W	description
0x7003	EXPO_CALC_CTRL 2 LOW BYTE	0xDF	RW	Bit[7:6]: cg_en_vs Enable very short CG 00: Off 01: On 10: Not used 11: Auto high_temp Bit[5:4]: dgain_en_vs Enable very short digital gain 00: Off 01: On 10: Not used 11: Auto high_temp Bit[3:2]: again_en_vs Enable very short analog gain 00: Off 01: On 10: Not used 11: Auto high_temp Bit[1:0]: expo_en_vs Enable very short exposure 00: Off 01: On 10: Not used 11: Auto high_temp
0x7004	MAX_TARGET_REG_L	0x13	RW	Longest Maximum Bin #0 Target Byte 1
0x7005	MAX_TARGET_REG_L	0xEC	RW	Longest Maximum Bin #0 Target Byte 0
0x7006	MIN_TARGET_REG_L	0x00	RW	Longest Minimum Bin #0 Target Byte 1
0x7007	MIN_TARGET_REG_L	0x64	RW	Longest Minimum Bin #0 Target Byte 0
0x7008	BIN0_TARGET_REG_L	0x13	RW	Longest Bin #0 Target Byte 1
0x7009	BIN0_TARGET_REG_L	0xEC	RW	Longest Bin #0 Target Byte 0
0x700A	HIST_TARGET_REG_L	0x12	RW	Longest Bin #1-14 Target Byte 1
0x700B	HIST_TARGET_REG_L	0xCA	RW	Longest Bin #1-14 Target Byte 0
0x700C	EV_GAIN_L	–	R	Longest Estimated EV Gain 8.8 Byte 1
0x700D	EV_GAIN_L	–	R	Longest Estimated EV Gain 8.8 Byte 0

table A-1 sensor control registers (sheet 71 of 80)

address	register name	default value	R/W	description
0x700E	EWMA_L	0x00	RW	Longest EWMA Filter Value Bit[7]: Fine gain step (slower, more accurate) Bit[6:1]: Not used Bit[0]: Longest EWMA filter α value 1.8, max is 'h100 MSB
0x700F	EWMA_L	0x60	RW	Longest EWMA Filter Value Bit[7:0]: Longest EWMA filter α value 1.8, max is 'h100 8 LSBs
0x7010~ 0x7019	RSVD	–	–	Reserved
0x701A	MAX_TARGET_REG_S	0x13	RW	Shortest Maximum Bin #0 Target Byte 1
0x701B	MAX_TARGET_REG_S	0xEC	RW	Shortest Maximum Bin #0 Target Byte 0
0x701C	MIN_TARGET_REG_S	0x00	RW	Shortest Minimum Bin #0 Target Byte 1
0x701D	MIN_TARGET_REG_S	0x64	RW	Shortest Minimum Bin #0 Target Byte 0
0x701E	BIN0_TARGET_REG_S	0x13	RW	Shortest Bin #0 Target Byte 1
0x701F	BIN0_TARGET_REG_S	0xEC	RW	Shortest Bin #0 Target Byte 0
0x7020	HIST_TARGET_REG_S	0x12	RW	Shortest Bin #1-14 Target Byte 1
0x7021	HIST_TARGET_REG_S	0xCA	RW	Shortest Bin #1-14 Target Byte 0
0x7022	EV_GAIN_S	–	R	Shortest Estimated EV Gain 8.8 Byte 1
0x7023	EV_GAIN_S	–	R	Shortest Estimated EV Gain 8.8 Byte 0
0x7024	EWMA_S	0x00	RW	Shortest EWMA Filter Value Bit[7]: Fine gain step (slower, more accurate) Bit[6:1]: Not used Bit[0]: Shortest EWMA filter α value 1.8, max is 'h100 MSB
0x7025	EWMA_S	0x60	RW	Shortest EWMA Filter Value Bit[7:0]: Shortest EWMA filter α value 1.8, max is 'h100 8 LSBs
0x7026~ 0x703F	RSVD	–	–	Reserved

table A-1 sensor control registers (sheet 72 of 80)

address	register name	default value	R/W	description
0x7040	D_EXPO_MAX_REG_L	0x3C	RW	Absolute Maximum Value for Exposure Time 24.8 Rows Byte 1
0x7041	D_EXPO_MAX_REG_L	0x00	RW	Absolute Maximum Value for Exposure Time 24.8 Rows Byte 0
0x7042	D_EXPO_MAX_REG_L	0x00	RW	Absolute Maximum Value for Exposure Time 24.8 Rows Byte 3
0x7043	D_EXPO_MAX_REG_L	0x04	RW	Absolute Maximum Value for Exposure Time 24.8 Rows Byte 2
0x7044	D_EXPO_MIN_REG_L	0x01	RW	Absolute Minimum Value for Exposure Time 24.8 Rows Byte 1
0x7045	D_EXPO_MIN_REG_L	0x00	RW	Absolute Minimum Value for Exposure Time 24.8 Rows Byte 0
0x7046	D_EXPO_MIN_REG_L	0x00	RW	Absolute Minimum Value for Exposure Time 24.8 Rows Byte 3
0x7047	D_EXPO_MIN_REG_L	0x00	RW	Absolute Minimum Value for Exposure Time 24.8 Rows Byte 2
0x7048	AGAIN_MIN_REG_L	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Absolute maximum value[9:8] for analog gain 00: Unity 01: 2x 10: 4x 11: 8x
0x7049	AGAIN_MAX_REG_L	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Absolute minimum value[9:8] for analog gain 00: Unity 01: 2x 10: 4x 11: 8x
0x704A	DGAIN_MAX_REG_L	0x01	RW	Absolute Maximum Value for Digital Gain 8.8 Byte 1
0x704B	DGAIN_MAX_REG_L	0x00	RW	Absolute Maximum Value for Digital Gain 8.8 Byte 0
0x704C	DGAIN_MIN_REG_L	0x00	RW	Absolute Minimum Value for Digital Gain 8.8 Byte 1
0x704D	DGAIN_MIN_REG_L	0x10	RW	Absolute Minimum Value for Digital Gain 8.8 Byte 0
0x704E	D_EV_MAX_L	–	R	Calculated Maximum EV 24.8 Byte 1

table A-1 sensor control registers (sheet 73 of 80)

address	register name	default value	R/W	description
0x704F	D_EV_MAX_L	–	R	Calculated Maximum EV 24.8 Byte 0
0x7050	D_EV_MAX_L	–	R	Calculated Maximum EV 24.8 Byte 3
0x7051	D_EV_MAX_L	–	R	Calculated Maximum EV 24.8 Byte 2
0x7052	D_EV_MIN_L	–	R	Calculated Minimum EV 24.8 Byte 1
0x7053	D_EV_MIN_L	–	R	Calculated Minimum EV 24.8 Byte 0
0x7054	D_EV_MIN_L	–	R	Calculated Minimum EV 24.8 Byte 3
0x7055	D_EV_MIN_L	–	R	Calculated Minimum EV 24.8 Byte 2
0x7056	D_EXPO_MAX_L	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 1
0x7057	D_EXPO_MAX_L	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 0
0x7058	D_EXPO_MAX_L	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 3
0x7059	D_EXPO_MAX_L	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 2
0x705A	D_EXPO_MIN_L	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 1
0x705B	D_EXPO_MIN_L	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 0
0x705C	D_EXPO_MIN_L	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 3
0x705D	D_EXPO_MIN_L	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 2
0x705E	AGAIN_MAX_L	–	R	Calculated Maximum Analog Gain 8.8 Byte 1
0x705F	AGAIN_MAX_L	–	R	Calculated Maximum Analog Gain 8.8 Byte 0
0x7060	AGAIN_MIN_L	–	R	Calculated Minimum Analog Gain 8.8 Byte 1
0x7061	AGAIN_MIN_L	–	R	Calculated Minimum Analog Gain 8.8 Byte 0
0x7062	DGAIN_MAX_L	–	R	Calculated Maximum Digital Gain 8.8 Byte 1
0x7063	DGAIN_MAX_L	–	R	Calculated Maximum Digital Gain 8.8 Byte 0
0x7064	DGAIN_MIN_L	–	R	Calculated Minimum Digital Gain 8.8 Byte 1
0x7065	DGAIN_MIN_L	–	R	Calculated Minimum Digital Gain 8.8 Byte 0
0x7066	CG_MAX_L	–	R	Calculated Maximum CG 8.8 Byte 1

table A-1 sensor control registers (sheet 74 of 80)

address	register name	default value	R/W	description
0x7067	CG_MAX_L	–	R	Calculated Maximum CG 8.8 Byte 0
0x7068	CG_MIN_L	–	R	Calculated Minimum CG 8.8 Byte 1
0x7069	CG_MIN_L	–	R	Calculated Minimum CG 8.8 Byte 0
0x706A~ 0x706B	RSVD	–	–	Reserved
0x706C 0x706F	SHORT_SHORT_D_ESTI_ EV	–	R	Estimated EV Applied EV Gain to Actual
0x7070~ 0x707B	RSVD	–	–	Reserved
0x707C	D_EXPO_MAX_REG_ S	0x3C	RW	Absolute Maximum Value for Exposure Time 24.8 Rows Byte 1
0x707D	D_EXPO_MAX_REG_ S	0x00	RW	Absolute Maximum Value for Exposure Time 24.8 Rows Byte 0
0x707E	D_EXPO_MAX_REG_ S	0x00	RW	Absolute Maximum Value for Exposure Time 24.8 Rows Byte 3
0x707F	D_EXPO_MAX_REG_ S	0x04	RW	Absolute Maximum Value for Exposure Time 24.8 Rows Byte 2
0x7080	D_EXPO_MIN_REG_S	0x01	RW	Absolute Minimum Value for Exposure Time 24.8 Rows Byte 1
0x7081	D_EXPO_MIN_REG_S	0x00	RW	Absolute Minimum Value for Exposure Time 24.8 Rows Byte 0
0x7082	D_EXPO_MIN_REG_S	0x00	RW	Absolute Minimum Value for Exposure Time 24.8 Rows Byte 3
0x7083	D_EXPO_MIN_REG_S	0x00	RW	Absolute Minimum Value for Exposure Time 24.8 Rows Byte 2
0x7084	AGAIN_MIN_REG_S	0x00	RW	Bit[7]: Force long exposure[15] Bit[6:2]: Not used Bit[1:0]: Absolute minimum value[9:8] for analog gain 00: Unity 01: 2x 10: 4x 11: 8x

table A-1 sensor control registers (sheet 75 of 80)

address	register name	default value	R/W	description
0x7085	AGAIN_MAX_REG_S	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Absolute maximum value[9:8] for analog gain 00: Unity 01: 2x 10: 4x 11: 8x
0x7086	DGAIN_MAX_REG_S	0x3F	RW	Absolute Maximum Value for Digital Gain 8.8 Byte 1
0x7087	DGAIN_MAX_REG_S	0xFF	RW	Absolute Maximum Value for Digital Gain 8.8 Byte 0
0x7088	DGAIN_MIN_REG_S	0x00	RW	Absolute Minimum Value for Digital Gain 8.8 Byte 1
0x7089	DGAIN_MIN_REG_S	0x10	RW	Absolute Minimum Value for Digital Gain 8.8 Byte 0
0x708A	D_EV_MAX_S	–	R	Calculated Maximum EV 24.8 Byte 1
0x708B	D_EV_MAX_S	–	R	Calculated Maximum EV 24.8 Byte 0
0x708C	D_EV_MAX_S	–	R	Calculated Maximum EV 24.8 Byte 1
0x708D	D_EV_MAX_S	–	R	Calculated Maximum EV 24.8 Byte 0
0x708E	D_EV_MIN_S	–	R	Calculated Minimum EV 24.8 Byte 1
0x708F	D_EV_MIN_S	–	R	Calculated Minimum EV 24.8 Byte 0
0x7090	D_EV_MIN_S	–	R	Calculated Minimum EV 24.8 Byte 3
0x7091	D_EV_MIN_S	–	R	Calculated Minimum EV 24.8 Byte 2
0x7092	D_EXPO_MAX_S	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 1
0x7093	D_EXPO_MAX_S	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 0
0x7094	D_EXPO_MAX_S	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 3
0x7095	D_EXPO_MAX_S	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 2
0x7096	D_EXPO_MIN_S	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 1
0x7097	D_EXPO_MIN_S	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 0

table A-1 sensor control registers (sheet 76 of 80)

address	register name	default value	R/W	description
0x7098	D_EXPO_MIN_S	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 3
0x7099	D_EXPO_MIN_S	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 2
0x709A	AGAIN_MAX_S	–	R	Calculated Maximum Analog Gain 8.8 Byte 1
0x709B	AGAIN_MAX_S	–	R	Calculated Maximum Analog Gain 8.8 Byte 0
0x709C	AGAIN_MIN_S	–	R	Calculated Minimum Analog Gain 8.8 Byte 1
0x709D	AGAIN_MIN_S	–	R	Calculated Minimum Analog Gain 8.8 Byte 0
0x709E	DGAIN_MAX_S	–	R	Calculated Maximum Digital Gain 8.8 Byte 1
0x709F	DGAIN_MAX_S	–	R	Calculated Maximum Digital Gain 8.8 Byte 0
0x70A0	DGAIN_MIN_S	–	R	Calculated Minimum Digital Gain 8.8 Byte 1
0x70A1	DGAIN_MIN_S	–	R	Calculated Minimum Digital Gain 8.8 Byte 0
0x70A2	CG_MAX_S	–	R	Calculated Maximum CG 8.8 Byte 1
0x70A3	CG_MAX_S	–	R	Calculated Maximum CG 8.8 Byte 0
0x70A4	CG_MIN_S	–	R	Calculated Minimum CG 8.8 Byte 1
0x70A5	CG_MIN_S	–	R	Calculated Minimum CG 8.8 Byte 0
0x70A6~ 0x70A7	RSVD	–	–	Reserved
0x70A8	D_ESTI_EV_VS	–	R	Estimated EV, Applied EV Gain to Actual Byte 1
0x70A9	D_ESTI_EV_VS	–	R	Estimated EV, Applied EV Gain to Actual Byte 0
0x70AA	D_ESTI_EV_VS	–	R	Estimated EV, Applied EV Gain to Actual Byte 3
0x70AB	D_ESTI_EV_VS	–	R	Estimated EV, Applied EV Gain to Actual Byte 2
0x70AC~ 0x70B7	RSVD	–	–	Reserved
0x70B8~ 0x70BB	D_EXPO_MAX_REG_ VS	–	–	Absolute Maximum Value for Exposure Time 24.8 Rows
0x70BC~ 0x70BF	D_EXPO_MIN_REG_ VS	–	–	Absolute Minimum Value for Exposure Time 24.8 Rows

table A-1 sensor control registers (sheet 77 of 80)

address	register name	default value	R/W	description
0x70C0	AGAIN_MIN_REG_VS	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Absolute minimum value[9:8] for analog gain 00: Unity 01: 2x 10: 4x 11: 8x
0x70C1	AGAIN_MAX_REG_VS	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Absolute maximum value[9:8] for analog gain 00: Unity 01: 2x 10: 4x 11: 8x
0x70C2~ 0x70C3	DGAIN_MAX_REG_VS	–	–	Absolute Maximum Value for Digital Gain 8.8
0x70C4~ 0x40C5	DGAIN_MIN_REG_VS	–	–	Absolute Minimum Value for Digital Gain 8.8
0x70C6	D_EV_MAX_VS	–	R	Calculated Maximum EV 24.8 Byte 1
0x70C7	D_EV_MAX_VS	–	R	Calculated Maximum EV 24.8 Byte 0
0x70C8	D_EV_MAX_VS	–	R	Calculated Maximum EV 24.8 Byte 3
0x70C9	D_EV_MAX_VS	–	R	Calculated Maximum EV 24.8 Byte 2
0x70CA	D_EV_MIN_VS	–	R	Calculated Minimum EV 24.8 Byte 1
0x70CB	D_EV_MIN_VS	–	R	Calculated Minimum EV 24.8 Byte 0
0x70CC	D_EV_MIN_VS	–	R	Calculated Minimum EV 24.8 Byte 3
0x70CD	D_EV_MIN_VS	–	R	Calculated Minimum EV 24.8 Byte 2
0x70CE	D_EXPO_MAX_VS	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 1
0x70CF	D_EXPO_MAX_VS	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 0
0x70D0	D_EXPO_MAX_VS	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 3
0x70D1	D_EXPO_MAX_VS	–	R	Calculated Maximum Exposure Time 24.8 Rows Byte 2
0x70D2	D_EXPO_MIN_VS	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 1

table A-1 sensor control registers (sheet 78 of 80)

address	register name	default value	R/W	description
0x70D3	D_EXPO_MIN_VS	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 0
0x70D4	D_EXPO_MIN_VS	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 3
0x70D5	D_EXPO_MIN_VS	–	R	Calculated Minimum Exposure Time 24.8 Rows Byte 2
0x70D6	AGAIN_MAX_VS	–	R	Calculated Maximum Analog Gain 8.8 Byte 1
0x70D7	AGAIN_MAX_VS	–	R	Calculated Maximum Analog Gain 8.8 Byte 0
0x70D8	AGAIN_MIN_VS	–	R	Calculated Minimum Analog Gain 8.8 Byte 1
0x70D9	AGAIN_MIN_VS	–	R	Calculated Minimum Analog Gain 8.8 Byte 0
0x70DA	DGAIN_MAX_VS	–	R	Calculated Maximum Digital Gain 8.8 Byte 1
0x70DB	DGAIN_MAX_VS	–	R	Calculated Maximum Digital Gain 8.8 Byte 0
0x70DC	DGAIN_MIN_VS	–	R	Calculated Minimum Digital Gain 8.8 Byte 1
0x70DD	DGAIN_MIN_VS	–	R	Calculated Minimum Digital Gain 8.8 Byte 0
0x70DE	CG_MAX_VS	–	R	Calculated Maximum CG 8.8 Byte 1
0x70DF	CG_MAX_VS	–	R	Calculated Maximum CG 8.8 Byte 0
0x70E0	CG_MIN_VS	–	R	Calculated Minimum CG 8.8 Byte 1
0x70E1	CG_MIN_VS	–	R	Calculated Minimum CG 8.8 Byte 0
0x70E2~ 0x70E3	RSVD	–	–	Reserved
0x70E4	D_RATIO_MAX_LS_ REG	0xFF	RW	Absolute Maximum Long/Short Ratio Byte 1
0x70E5	D_RATIO_MAX_LS_ REG	0xFF	RW	Absolute Maximum Long/Short Ratio Byte 0
0x70E6	D_RATIO_MAX_LS_ REG	0x00	RW	Absolute Maximum Long/Short Ratio Byte 3
0x70E7	D_RATIO_MAX_LS_ REG	0x03	RW	Absolute Maximum Long/Short Ratio Byte 2
0x70E8	D_RATIO_MIN_LS_ REG	0x01	RW	Absolute Minimum Long/Short Ratio Byte 1
0x70E9	D_RATIO_MIN_LS_ REG	0x00	RW	Absolute Minimum Long/Short Ratio Byte 0
0x70EA	D_RATIO_MIN_LS_ REG	0x00	RW	Absolute Minimum Long/Short Ratio Byte 3

table A-1 sensor control registers (sheet 79 of 80)

address	register name	default value	R/W	description
0x70EB	D_RATIO_MIN_LS_ REG	0x00	RW	Absolute Minimum Long/Short Ratio Byte 2
0x70EC	D_RATIO_MAX_LVS_ REG	0xFF	RW	Absolute Maximum Long/VShort Ratio Byte 1
0x70ED	D_RATIO_MAX_LVS_ REG	0xFF	RW	Absolute Maximum Long/VShort Ratio Byte 0
0x70EE	D_RATIO_MAX_LVS_ REG	0x00	RW	Absolute Maximum Long/VShort Ratio Byte 3
0x70EF	D_RATIO_MAX_LVS_ REG	0x03	RW	Absolute Maximum Long/VShort Ratio Byte 2
0x70F0	D_RATIO_MIN_LVS_ REG	0x01	RW	Absolute Minimum Long/VShort Ratio Byte 1
0x70F1	D_RATIO_MIN_LVS_ REG	0x00	RW	Absolute Minimum Long/VShort Ratio Byte 0
0x70F2	D_RATIO_MIN_LVS_ REG	0x00	RW	Absolute Minimum Long/VShort Ratio Byte 3
0x70F3	D_RATIO_MIN_LVS_ REG	0x00	RW	Absolute Minimum Long/VShort Ratio Byte 2
0x70F4	D_RATIO_MAX_LS	–	R	Calculated Maximum Long/Short Ratio Byte 1
0x70F5	D_RATIO_MAX_LS	–	R	Calculated Maximum Long/Short Ratio Byte 0
0x70F6	D_RATIO_MAX_LS	–	R	Calculated Maximum Long/Short Ratio Byte 3
0x70F7	D_RATIO_MAX_LS	–	R	Calculated Maximum Long/Short Ratio Byte 2
0x70F8	D_RATIO_MIN_LS	–	R	Calculated Minimum Long/Short Ratio Byte 1
0x70F9	D_RATIO_MIN_LS	–	R	Calculated Minimum Long/Short Ratio Byte 0
0x70FA	D_RATIO_MIN_LS	–	R	Calculated Minimum Long/Short Ratio Byte 3
0x70FB	D_RATIO_MIN_LS	–	R	Calculated Minimum Long/Short Ratio Byte 2
0x70FC	D_RATIO_MAX_LVS	–	R	Calculated Maximum Long/VShort Ratio Byte 1
0x70FD	D_RATIO_MAX_LVS	–	R	Calculated Maximum Long/VShort Ratio Byte 0
0x70FE	D_RATIO_MAX_LVS	–	R	Calculated Maximum Long/VShort Ratio Byte 3
0x70FF	D_RATIO_MAX_LVS	–	R	Calculated Maximum Long/VShort Ratio Byte 2
0x7100	D_RATIO_MIN_LVS	–	R	Calculated Minimum Long/VShort Ratio Byte 1
0x7101	D_RATIO_MIN_LVS	–	R	Calculated Minimum Long/VShort Ratio Byte 0
0x7102	D_RATIO_MIN_LVS	–	R	Calculated Minimum Long/VShort Ratio Byte 3

table A-1 sensor control registers (sheet 80 of 80)

address	register name	default value	R/W	description
0x7103	D_RATIO_MIN_LVS	–	R	Calculated Minimum Long/VShort Ratio Byte 2
0x7104	D_RATIO_SQRT	–	R	Square Root of Calculated Ratio Byte 1
0x7105	D_RATIO_SQRT	–	R	Square Root of Calculated Ratio Byte 0
0x7106	D_RATIO_SQRT	–	R	Square Root of Calculated Ratio Byte 3
0x7107	D_RATIO_SQRT	–	R	Square Root of Calculated Ratio Byte 2
0x7108	D_RATIO	–	R	Calculated Ratio Byte 1
0x7109	D_RATIO	–	R	Calculated Ratio Byte 0
0x710A	D_RATIO	–	R	Calculated Ratio Byte 3
0x710B	D_RATIO	–	R	Calculated Ratio Byte 2
0x710C~ 0x710F	RSVD	–	–	Reserved

revision history

version 1.0 03.24.2015

- initial release

version 1.1 05.08.2015

- in sub-section 1.3.1, changed second to last sentence of section description to "'AVDD_LO should always be decoupled to ground via external capacitor."
- in table 4-4, replaced bit descriptions for registers 0x31FF~0x3267 with new information
- in chapter 6, updated figure 6-1
- in sub-section 6.4.1, removed "In MIPI mode, L, S and VS are sent out via different virtual channel,...." from sub-section description
- in section 6.5, added sub-sections 6.5.1, 6.5.2, and 6.5.3
- in table A-1, replaced bit descriptions for registers 0x31FF~0x3267 with new information, changed register addresses from 0x332A~0x33E5 to 0x331A~0x33D5, changed register name for register 0x3365 to "LENC_S_G17", and added registers 0x33D6~0x33E5

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