MAX9286

Quad 1.5Gbps GMSL Deserializer with Coax or STP Input and CSI-2 Output

General Description

The MAX9286 Gigabit multimedia serial link (GMSL) deserializer receives data from up to four GMSL serializers over 50Ω coax or 100Ω shielded twisted pair (STP) cables and output data on four CSI-2 lanes. Each serial link has an embedded control channel operating from 9.6kbps to 1Mbps in UART-UART, UART-I²C, and I²C-I²C mode. Using the control channel, a µC can program the serializers, deserializer, and peripheral device registers at any time, independent of video timing. A maskable broadcast write speeds programming of image sensor registers.

For use with longer cables, the deserializer has a programmable cable equalizer and programmable error detection and correction. The serial input meets ISO 10605 and IEC 61000-4-2 ESD standards. The core supply is 1.7V to 1.9V and the I/O supply is 1.7V to 3.6V.

The device is available in lead(Pb)-free, 56-pin, 8mm x 8mm QFND and TQFN packages with exposed pad and 0.5mm lead pitch.

Applications

- Surround View Camera Systems
- Machine Vision Systems
- 3D Camera Systems

***Ordering Information** appears at end of data sheet.*

Benefits and Features

- Ideal for Multicamera Stream Applications
  - Works with Low-Cost 50Ω Coax Cable and FAKRA Connectors or 100Ω STP
  - Data from Image Sensors Are Synchronized to the Same Pixel
  - Automatic Internal/External Generation of Camera Sync
  - Equalization Allows 15m Length Cable Operation at Full Speed
- Multiple Input/Output Features for System Flexibility
  - 1 to 4 Lane CSI-2 Output with 80Mbps to 1200Mbps Per Lane
  - Swappable/Selectable Serial Input/Output with Swappable Polarity
  - 9.6kbps to 1Mbps Control Channel in UART, Mixed UART/I²C, or I²C Mode with Clock Stretch Capability
- Peripheral Features for System Power-Up and Verification
  - Built-In PRBS Tester for BER Testing of the Serial Link
  - Programmable Choice of Nine Default Device Addresses
  - Two Dedicated GPIO Ports
  - High-Immunity Mode for Maximum Control-Channel Noise Rejection
- Meets Rigorous Automotive and Industrial Requirements
  - -40°C to +105°C Operating Temperature
  - ±8kV Contact, ±20kV Air ISO 10605 and ±8kV Contact, ±12kV EC 61000-4-2 ESD Protection

19-7456; Rev 0; 1/15

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TABLE OF CONTENTS

TABLE OF CONTENTS (CONTINUED)

LIST OF FIGURES

LIST OF FIGURES (CONTINUED)

LIST OF TABLES

Absolute Maximum Ratings (Note 1)

AVDD to EP ..... -0.5V to +1.9V
DVDD to EP ..... -0.5V to +1.9V
MAVDD to EP ..... -0.5V to +1.9V
IOVDD to EP ..... -0.5V to +3.9V
IN_+, IN_- to EP ..... -0.5V to +1.9V
DOUT_+, DOUT_-, CLK+, CLK- to EP ..... -0.5V to +1.9V
MON+, MON- to EP ..... -0.5V to +1.9V
LMN_ to EP (15mA current limit) ..... -0.5V to +3.9V
All Other Pins to EP ..... -0.5V to +(V_{IOVDD} + 0.5V)
IN+, IN- Short Circuit to Ground or Supply ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
QFND (derate 42.7 mW/°C above +70°C) 3418mW
TQFN (derate 47.6mW/°C above +70°C) 3809.5mW
Operating Temperature Range ..... -40°C to +105°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Note 1: EP connected to PCB ground.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

QFND
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 1.6°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 23.4°C/W

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 1°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 21°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = V_{MAVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ±1% (single-ended), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{MAVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (CX/TP, HIM, I2CSEL, MS, $\overline{PWDN}$, FRSYNC/GPI)						
High-Level Input Voltage	V_{IH1}		0.65 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL1}				0.35 x V_{IOVDD}	V
Input Current	I_{IN1}		-20		+20	µA
THREE-LEVEL LOGIC INPUTS (ADD0, ADD1, BWS)						
High-Level Input Voltage	V_{IH}		0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{IOVDD}	V
Mid-Level Input Current	I_{INM}	Open or connected to a driver with output in high impedance (Note 4)	-10		+10	µA
Input Current	I_{IN}	High or low	-150		+150	µA

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{MAVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ±1% (single-ended), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{MAVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE- ENDED-OUTPUTS (FRSYNC/GPI)							
High-Level Output Voltage	V_{OH}	I_{OH} = -2mA		V_{IOVDD} - 0.2			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 2mA				0.2	V
Output Short-Circuit Current	I_{OS}	V_O = 0V	V_{IOVDD} = 3.0V to 3.6V	16	35	64	mA
			V_{IOVDD} = 1.7V to 1.9V	3	12	21	
OPEN-DRAIN INPUT/OUTPUTS (GPIO0, GPIO1, RX/SDA, TX/SCL)							
High-Level Input Voltage	V_{IH2}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}					0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	V_{IN} = 0V to V_{IOVDD} (Note 5)	RX/SDA, TX/SCL	-110		5	µA
			GPIO_	-80		5	
Low-Level Output Voltage	V_{OL2}	I_{OUT} = 3mA	V_{IOVDD} = 1.7V to 1.9V			0.4	V
			V_{IOVDD} = 3.0V to 3.6V			0.3	
Input Capacitance	C_{IN}	Each pin (Note 6)				10	pF
OPEN-DRAIN OUTPUTS ($\overline{CCBSY}$, $\overline{ERR}$, $\overline{LFLT}$, $\overline{LMO}$, LOCK)							
Low-Level Output Voltage	V_{OL3}	I_{OUT} = 3mA	V_{IOVDD} = 1.7V to 1.9V			0.4	V
			V_{IOVDD} = 3.0V to 3.6V			0.3	
Input Current	I_{IN3}	(Note 5)		-80		5	µA
OUTPUTS FOR REVERSE CONTROL CHANNEL (IN+, IN-)							
Differential High Output Peak Voltage, (V_{IN+} - V_{IN-})	V_{RODH}	Forward channel disabled (Figure 1)	Legacy reverse control channel mode	30		60	mV
			High-immunity mode	50		100	
Differential Low Output Peak Voltage, (V_{IN+} - V_{IN-})	V_{RODL}	Forward channel disabled (Figure 1)	Legacy reverse control channel mode	-60		-30	mV
			High-immunity mode	-100		-50	
Single-Ended High Output Peak Voltage	V_{ROSH}	Forward channel disabled (Figure 1)	Legacy reverse control channel mode	30		60	mV
			High-immunity mode	50		100	
Single-Ended Low Output Peak Voltage	V_{ROSL}	Forward channel disabled (Figure 1)	Legacy reverse control channel mode	-60		-30	mV
			High-immunity mode	-100		-50	

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{MAVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ±1% (single-ended), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{MAVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIFFERENTIAL INPUTS (IN_+, IN_-) (STP MODE)							
Differential High Input Threshold (Peak) Voltage, (V_{IN+} - V_{IN-})	$V_{IDH(P)}$	Figure 2	Activity detector medium threshold (0x3C D[6:5] = 01)			60	mV
			Activity detector low threshold (0x3C D[6:5] = 00)			49	
Differential Low Input Threshold (Peak) Voltage, (V_{IN+} - V_{IN-})	$V_{IDL(P)}$	Figure 2	Activity detector medium threshold (0x3C D[6:5] = 01)	-60			mV
			Activity detector low threshold (0x3C D[6:5] = 00)	-49			
Input Common-Mode Voltage ((V_{IN+}) + (V_{IN-}))/2	V_{CMR}			1	1.3	1.6	V
Differential Input Resistance (Internal)	R_I			80	100	130	Ω
CSI-2 OUTPUTS, HIGH-SPEED DIFFERENTIAL MODE (DOUT[3:0]_, CLK_)							
Transmit Static Common Mode Voltage	V_{CMTX}			150		250	mV
V_{CMTX} Mismatch When Output is Differential 1 or 0	$\lvert\Delta V_{CMTX}\rvert$	(Note 7)				5	mV
Transmit Differential Voltage	$\lvert V_{OD}\rvert$			140		270	mV
V_{OD} Mismatch When Output is Differential 1 or 0	$\lvert\Delta V_{OD}\rvert$					14	mV
Output High Voltage	V_{OHHS}					360	mV
Single-Ended Output Impedance	Z_{OS}			40	50	62.5	Ω
Single-Ended Output Impedance Mismatch	$\lvert\Delta Z_{OS}\rvert$	Mismatch of the single-ended output impedance between DOUT_+ and DOUT_-				10	%
CSI-2 OUTPUTS, LOW-SPEED SINGLE-ENDED MODE (DOUT[3:0]_, CLK_)							
Thevenin Output High	V_{OH}			1.05	1.2	1.3	V
Thevenin Output Low	V_{OL}			-50	5	+50	mV
Output Impedance of Low Power Transmitter	Z_{OLP}			110			Ω

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{MAVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ±1% (single-ended), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{MAVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MONITOR OUTPUTS (MON+, MON-) (COAX MODE)							
Differential Output Voltage	V_{OD}				200		mV
Change in V_{OD} Between Complementary Output States	ΔV_{OD}				0		mV
Output Offset Voltage (V_{OUT+} + V_{OUT-})/2 = V_{OS}	V_{OS}	(Note 7)			1.6		V
Change in V_{OS} Between Complementary Output States	V_{OS}				0		mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V			-35		mA
		V_{OUT+} or V_{OUT-} = V_{AVDD}			7.5		
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0V			3.7		mA
Output Termination Resistance (Internal)	R_O	From OUT+ or OUT- to AVDD			57		Ω
SINGLE-ENDED INPUTS (IN_+, IN-)							
Single-Ended High Input Threshold (Peak) Voltage	$V_{ISH(P)}$	Figure 3	Activity detector medium threshold (0x3C D[6:5] = 01)			43	mV
			Activity detector low threshold (0x3C D[6:5] = 00)			36	
Single-Ended Low Input Threshold (Peak) Voltage	$V_{ISL(P)}$	Figure 3	Activity detector medium threshold (0x3C D[6:5] = 01)	-43			mV
			Activity detector low threshold (0x2C D[6:5] = 00)	-36			
Input Resistance (Internal)	R_I			40	50	65	Ω
LINE-FAULT DETECTION INPUTS (LMN0, LMN1, LMN2, LMN3)							
Short-to-GND Threshold	V_{TG}	Figure 4				0.3	V
Normal Threshold	V_{TN}	Figure 4		0.57		1.07	V
Open Threshold	V_{TO}	Figure 4		1.45		V_{IO} + 0.06	V
Open Input Voltage	V_{IO}	Figure 4		1.47		1.75	V
Short-to-Battery Threshold	V_{TB}	Figure 4		2.47			V

DC Electrical Characteristics (continued)

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Current (Worst-Case Pattern) (Note 8, Figure 5)	I_{WCS}	4 input channels at 1.5Gbps/channel, 4 CSI-2 output lanes at 1.2Gbps/lane	AVDD + DVDD + MAVDD (1.9V)		330	430	mA
			IOVDD (3.6V)		0.5	1.0	
			IOVDD (1.9V)		0.3	0.5	
		4 input channels at 750Mbps/channel, 2 CSI-2 output lanes at 1.2Gbps/lane	AVDD + DVDD + MAVDD (1.9V)		240	320	
			IOVDD (3.6V)		0.5	1.0	
			IOVDD (1.9V)		0.3	0.5	
		2 input channels at 1.5Gbps/channel, 2 CSI-2 output lanes at 1.2Gbps/lane	AVDD + DVDD + MAVDD (1.9V)		200	270	
			IOVDD (3.6V)		0.5	1.0	
			IOVDD (1.9V)		0.3	0.5	
Sleep Mode Supply Current	I_{CCS}	Remote wake-up receivers enabled			220	1050	0.5
		Remote wake-up receivers disabled			35	800	
Power-Down Current	I_{CCZ}	$\overline{PWDN}$ = EP-			35	800	µA
ESD PROTECTION							
IN_+, IN_- (Note 9)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF			±8		kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF	Contact discharge		±8		
			Air discharge		±12		
		ISO 10605, R_D = 2kΩ, C_S = 330pF	Contact discharge		±8		
			Air discharge		±20		
All Other Pins	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF (Note 10)			±4.5		kV
		Machine Model			200		V

AC Electrical Characteristics

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
I²C/UART PORT TIMING							
I²C/UART Bit Rate	BR			9.6		1000	kbps
Output Rise Time	t_R	0.3 x V_{IOVDD} to 0.7 x V_{IOVDD}, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}		20		150	ns
Output Fall Time	t_F	0.7 x V_{IOVDD} to 0.3 x V_{IOVDD}, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}		20		150	ns
I²C TIMING (Figure 6)							
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range: (I2CMSTBT = 010, I2CSLVSH = 10)		9.6		100	kHz
		Mid f_{SCL} range: (I2CMSTBT = 101, I2CSLVSH = 01)		> 100		400	
		High f_{SCL} range: (I2CMSTBT = 111, I2CSLVSH = 00)		> 400		1000	
START Condition Hold Time	$t_{HD:STA}$	f_{SCL} range	Low	4.0			µs
			Mid	0.6			
			High	0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range	Low	4.7			µs
			Mid	1.3			
			High	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range	Low	4.0			µs
			Mid	0.6			
			High	0.26			
Repeated START Condition Setup Time	$t_{SU:STA}$	f_{SCL} range	Low	4.7			µs
			Mid	0.6			
			High	0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range	Low	0			µs
			Mid	0			
			High	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range	Low	250			ns
			Mid	100			
			High	50			
Setup Time for STOP Condition	$t_{SU:STO}$	f_{SCL} range	Low	4.0			µs
			Mid	0.6			
			High	0.26			

AC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{MAVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ±1% (single-ended), EP connected to PCB ground, T_A = -40°C to + 105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{MAVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Bus Free Time	t_{BUF}	f_{SCL} range	Low	4.7			µs
			Mid	1.3			
			High	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range	Low			3.45	µs
			Mid			0.9	
			High			0.45	
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range	Low			3.45	µs
			Mid			0.9	
			High			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range	Low			50	ns
			Mid			50	
			High			50	
Capacitive Load Each Bus Line	C_B	(Note 6)				100	pF
SWITCHING CHARACTERISTICS (Note 7)							
Deserializer Delay	t_{SD}	(Figure 7, Note 11)		0.5		4	t_{HS}
Reverse Control Channel Output Rise Time	t_R	Forward-channel disabled (Figure 1), 20% to 80%, V_{OD} ≥ 400mV, R_L = 100Ω, serial bit rate = 1.5Gbps		180		400	ns
Reverse Control Channel Output Fall Time	t_F	Forward-channel disabled (Figure 1), 20% to 80%, V_{OD} ≥ 400mV, R_L = 100Ω, serial bit rate = 1.5Gbps		180		400	ns
FRSYNC/GPI to GPO Delay	t_{GPOD}	FSYNC/GPI to serializer GPO (cable delay not included) Figure 8)		220		360	µs
FRSYNC/GPI to GPO Skew	t_{GPOS}	FSYNC/GPI to serializer GPO skew (Figure 8)				0.5	µs
Lock Time	t_{LOCK}	All channels locked (Figure 9)				4	ms
Camera Sync Time	t_{CAMS}	Default settings in full automatic mode (Figure 9, Note 12)				$6t_{VS}$ + 1	ms
Power-Up Time	t_{PU}	(Figure 10)				7	ms
CSI-2 OUTPUTS, HIGH-SPEED DIFFERENTIAL MODE (DOUT[3:0]_, CLK_) (Note 7)							
20% to 80% Rise and Fall Time	t_R, t_F	Bit time ≤ 1Gbps				0.30	UI
		Bit time > 1Gbps				0.35	UI
				100			ps
UI Instantaneous	UI_{IN}			0.794		12.5	ns
Data-to-Clock Skew	t_{SKEW}	Bit time ≤ 1Gbps		-0.15		+0.15	UI
		Bit time > 1Gbps		-0.2		+0.2	

AC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{MAVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ±1% (single-ended), EP connected to PCB ground, T_A = -40°C to + 105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{MAVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UI Variation	ΔUI	Bit time ≤ 1Gbps	-5		+5	%
		Bit time > 1Gbps	-10		+10	
Common Mode Variation	ΔV_{CM}	> 450MHz			15	mV_{PEAK}
		50MHz ≤ $f_{CLK\_}$ ≤ 450MHz			25	
CSI-2 OUTPUTS, LOW-SPEED DIFFERENTIAL MODE (DOUT[3:0]_, CLK_) (Note 7)						
15% to 85% Rise and Fall Time	t_{RLP}, t_{FLP}				25	ns
30% to 85% Rise and Fall Time Transition from HS to LP	t_{REOP}				35	ns
GENERAL CSI-2 TIMING (Figure 11, Note 7)						
Start of Transmission: Clock Preparation Time	$t_{CLK-PREP}$	Time that the transmitter drives the clock lane LP-00 line state immediately before HS-0 line state starting the HS transition	38		95	ns
End of Transmission: Clock Trail Time	$t_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst	60			ns
Clock Start of Transmission Time	$t_{CLK-PREP}$ + $t_{CLK-ZERO}$	$t_{CLK-PREP}$ + time that the transmitter drives the HS-0 state prior to starting the clock	300			ns
Clock End of Transmission Time	t_{EOT}	Transmitted time interval from the start of $t_{HS-TRAIL}$ or $t_{CLK-TRAIL}$ to start of the LP-11 state following an HS burst			105 + 12UI	ns
HS Exit Time	$t_{HS-EXIT}$	Time that the transmitter drives LP-11 following an HS burst	100			ns
Start of Transmission: Data Preparation Time	$t_{HS-PREP}$	Time that the transmitter drives the data lane LP-00 line state immediately before the HS-0 line state starting the HS transmission	40 + 4UI		85 + 6UI	ns
Start of Transition Time	$t_{HS-PREP}$+ t_{HSZERO}	$t_{HS-PREP}$ + time that the transmitter drives the HS-0 state prior to transmitting the sync sequence	145 + 10 UI			ns
End of Transmission: Data Trail Time	$t_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after the last payload data bit of an HS transmission burst	MAX(8UI, 60ns + 4UI)			ns
LP Transmit Time	t_{LPTX}	Transmitted length of any low power state period	50			ns

AC Electrical Characteristics (continued)

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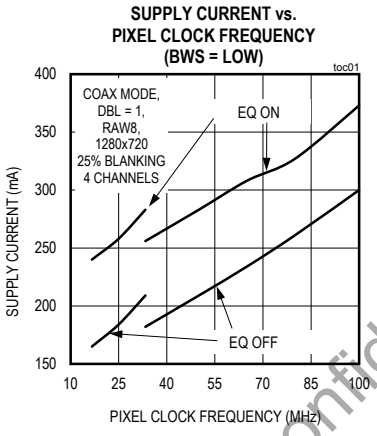
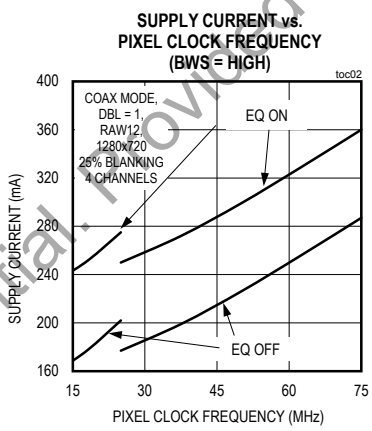
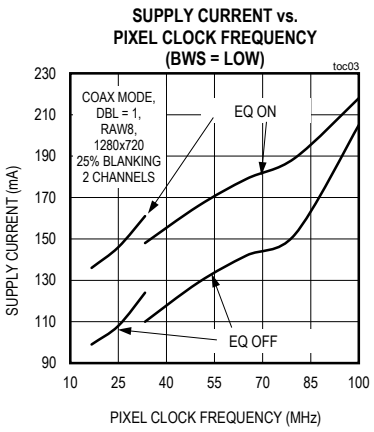
Note 3: Limits are 100% production tested at T_A = +105°C. Limits over the operating temperature range are guaranteed by design and characterization, unless otherwise noted.
Note 4: To provide a mid-level voltage, leave the input open, or, if driven, put the driver in high-impedance state. High-impedance leakage current must be less than ±10µA.
Note 5: I_{IN} min is due to voltage drop across the internal pullup resistor.
Note 6: Not production tested. Guaranteed by design.
Note 7: Not production tested. Guaranteed by characterization.
Note 8: IOVDD current is not production tested.
Note 9: Specified pin to ground.
Note 10: Specified pin to all supply/ground.
Note 11: t_{HS} is the line (HSYNC) period.
Note 12: t_{VS} is the frame (VSYNC) period.

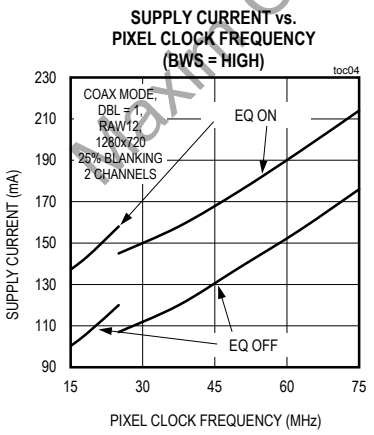
Typical Operating Characteristics

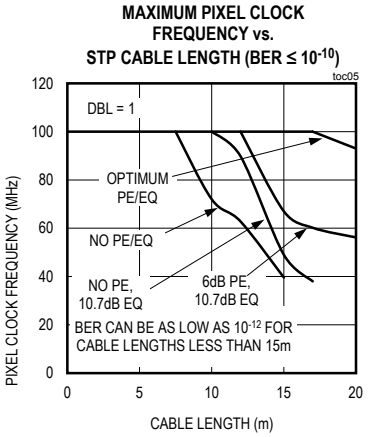
(V_{DVDD} = V_{MAVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C, unless otherwise noted.)

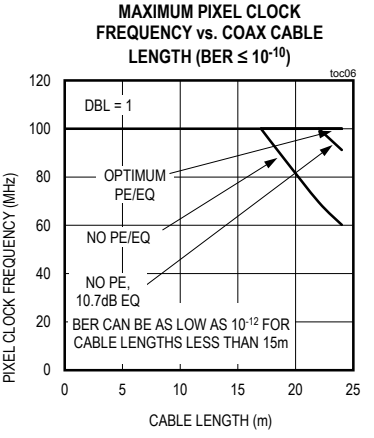








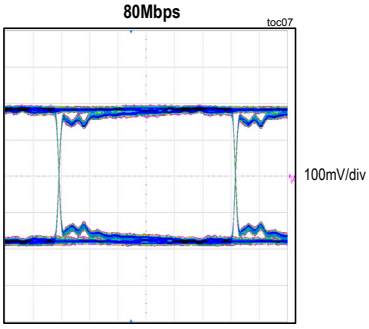




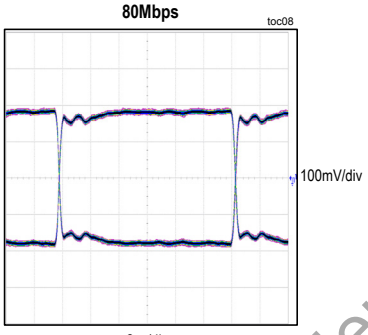
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{MAVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C, unless otherwise noted.)

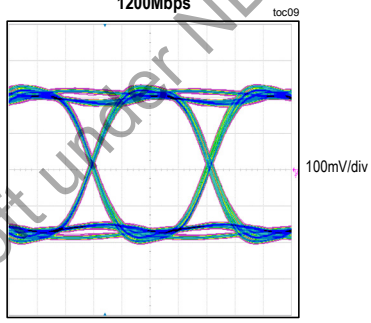
MIPI DATA EYE PATTERN
80Mbps



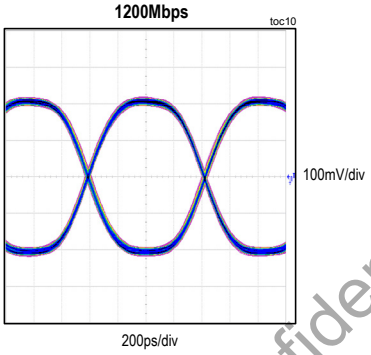
MIPI CLOCK EYE PATTERN
80Mbps



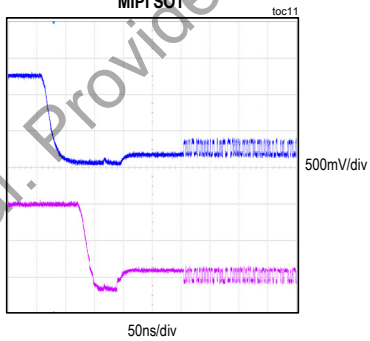
MIPI DATA EYE PATTERN
1200Mbps



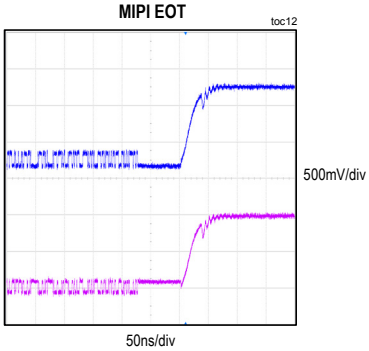
MIPI CLOCK EYE PATTERN
1200Mbps



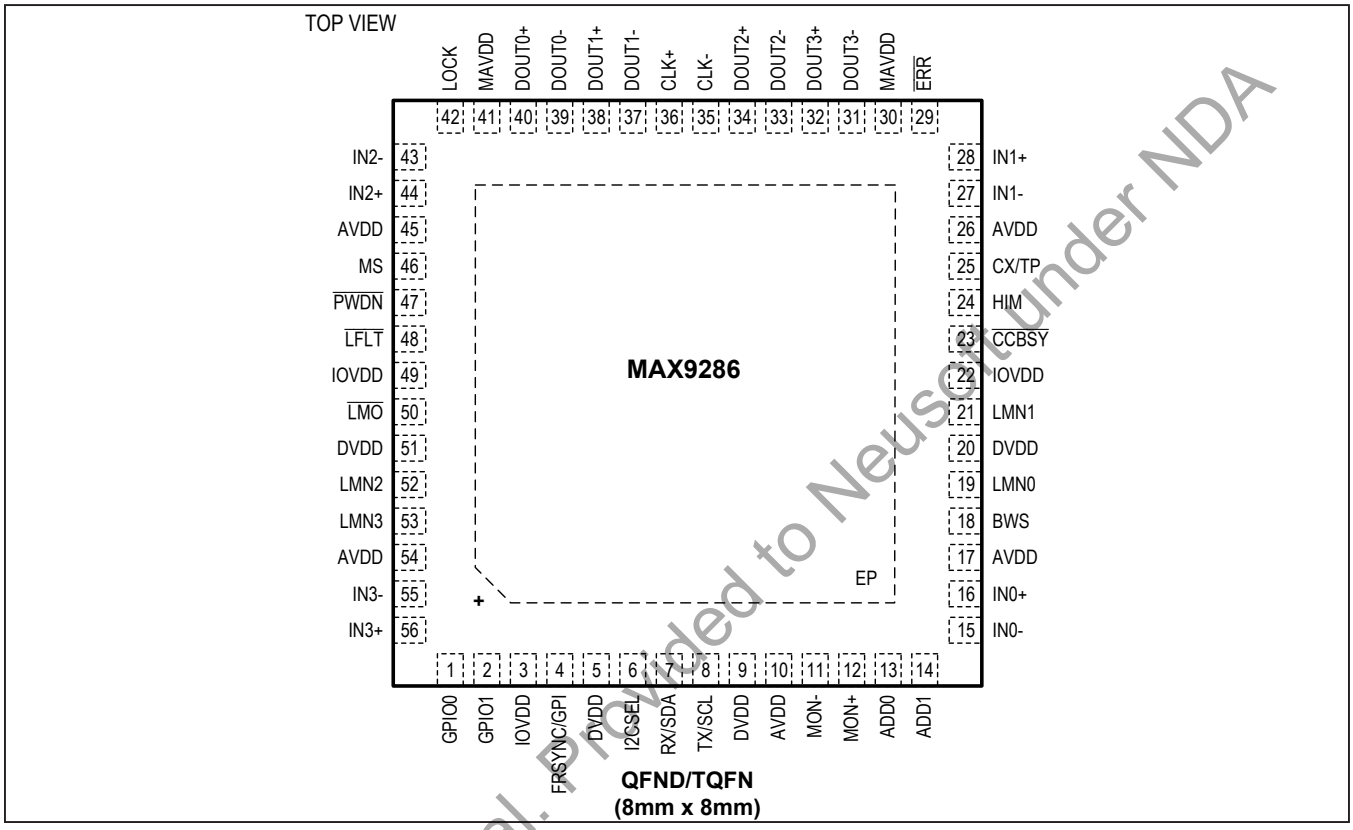
MIPI SOT



MIPI EOT



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	GPIO0	Open-Drain, General-Purpose Input/Output with Internal 60kΩ Pullup to IOVDD
2	GPIO1	Open-Drain, General-Purpose Input/Output with Internal 60kΩ Pullup to IOVDD
3, 22, 49	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to IOVDD.
4	FRSYNC/GPI	Frame Sync/General-Purpose Input/Output with Internal Pulldown to EP. **Set to high impedance at power-up.** Frame Sync: operating mode is determined by the FSYNCMODE register bits (see Table 27). GPI: The serializer's GPO (or INT) outputs follow GPI (when FSYNCMODE = 11).
5, 9, 20, 51	DVDD	1.8V Digital Power Supply. Bypass DVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
6	I2CSEL	I^2C Select. Control channel interface protocol select input with internal pulldown to EP. Set I2CSEL = high to select I^2C-to-I^2C interface. Set I2CSEL = low to select UART/UART or UART/I^2C interface.

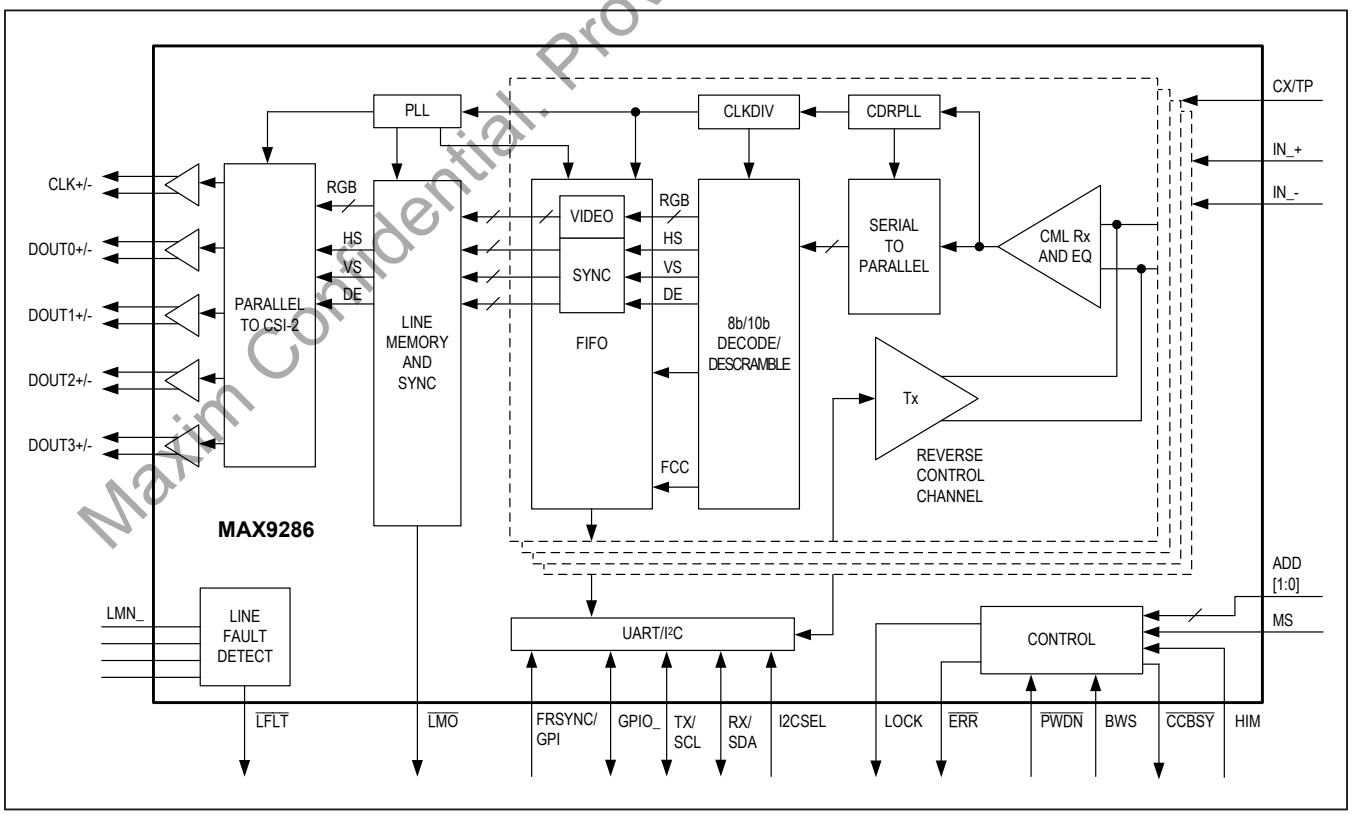
Pin Description (continued)

PIN	NAME	FUNCTION
7	RX/SDA	UART Receive/I²C Serial Data Input/Output with Internal 30kΩ Pullup to IOVDD. Function is determined by the state of I2CSEL at power-up. RX/SDA has an open-drain driver and requires a pullup resistor. RX: Input of the deserializer's UART. SDA: Data output/input of the deserializer's I²C master/slave.
8	TX/SCL	UART Transmit/I²C Serial Clock Input/Output with Internal 30kΩ Pullup to IOVDD. Function is determined by the state of I2CSEL at power-up. TX/SCL has an open-drain driver and requires a pullup resistor. TX: Output of the deserializer's UART. SCL: Clock output/input of the deserializer's I²C master/slave.
10, 17, 26, 45, 54	AVDD	1.8V Analog Power Supply. Bypass AVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
11, 12	MON-, MON+	CML Monitor Output. Outputs the signal after equalization from Link 0
13	ADD0	Three-Level Address Selection Input. The state of ADD0 latches at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). See Table 1 for details.
14	ADD1	Three-Level Address Selection Input. The state of ADD1 latches at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). See Table 1 for details.
15	IN0-	Channel 0 Inverting Coax/Twisted-Pair Serial Input. Polarity is programmable (see Table 27).
16	IN0+	Channel 0 Noninverting Coax/Twisted-Pair Serial Input. Polarity is programmable (see Table 27).
18	BWS	Three-Level Bus Width Select Input. Set BWS to the same level on both sides of the serial link. Set BWS = low for 24-bit mode. Set BWS = high for 32-bit mode. Set BWS = open for high-bandwidth mode (MAX9275-MAX9281 only).
19	LMN0	Line-Fault Monitor Input for Channel 0. See Figure 4.
21	LMN1	Line-Fault Monitor Input for Channel 1. See Figure 4.
23	$\overline{CCBSY}$	Active low Control Channel Busy Output. Open-drain indicator of control channel activity with Internal 60kΩ pullup to IOVDD. $\overline{CCBSY}$ = low indicates that the control channel is currently in use.
24	HIM	High-Immunity Mode Input with Internal Pulldown to EP. Default HIGHIMM bit value is latched at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low) and is active-high. HIGHIMM can be programmed to a different value after power-up. HIGHIMM in the serializer must be set to the same value. High-immunity mode must be supported by the serializer (MAX9275-MAX9281 only).
25	CX/TP	Coax/Twisted Pair Select Input with internal pulldown to EP. Set CX/TP high to select coax input. Set CX/TP low for STP input. Input cable type can be programmed to a different value after power-up.
27	IN1-	Channel 1 Inverting Coax/Twisted Pair Serial Input. Polarity is programmable (see Table 27).
28	IN1+	Channel 1 Noninverting Coax/Twisted Pair Serial Input. Polarity is programmable (see Table 27).
29	$\overline{ERR}$	Active Low Error Output. Open-drain data error detection and/or correction indication output with internal 60kΩ pullup to IOVDD. ERR is high when PWDN is low.
30, 41	MAVDD	1.8V MIPI CSI-2 Power Supply. Bypass MAVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to MAVDD.
31–34, 37–40	DOUT_-, DOUT_+	CSI-2 Data Output
35, 36	CLK-, CLK+	CSI-2 Clock Output
42	LOCK	Open-Drain Lock Output with Internal 60kΩ Pullup to IOVDD. LOCK = high indicates that PLLs are locked with correct serial-word-boundary alignment. LOCK = low indicates that PLLs are not locked or an incorrect serial-word-boundary alignment. LOCK is high when $\overline{PWDN}$ = low.

Pin Description (continued)

PIN	NAME	FUNCTION
43	IN2-	Channel 2 Inverting Coax/Twisted-Pair Serial Input. Polarity is programmable (see Table 27).
44	IN2+	Channel 2 Noninverting Coax/Twisted-Pair Serial Input. Polarity is programmable (see Table 27).
46	MS	Mode Select Input with Internal Pulldown to EP. Mode selection is only used in UART-to-UART and UART-to-I²C mode. Set MS = low to select base mode. Set MS = high to select bypass mode.
47	$\overline{PWDN}$	Active-Low, Power-Down Input with Internal Pulldown to EP. Set $\overline{PWDN}$ low to enter power-down mode to reduce power consumption.
48	$\overline{LFLT}$	Active Low Open-Drain Line-Fault Output. $\overline{LFLT}$ has a 60kΩ pullup to IOVDD. $\overline{LFLT}$ = low indicates a line fault. LFLT is output high when $\overline{PWDN}$ is low.
50	$\overline{LMO}$	Line Memory Overflow Output. $\overline{LMO}$ has a 60kΩ pullup to IOVDD. $\overline{LMO}$ = low when the serial data overflows the line memory.
52	LMN2	Line-Fault Monitor Input for Channel 2. See Figure 4.
53	LMN3	Line-Fault Monitor Input for Channel 3. See Figure 4.
55	IN3-	Channel 3 Inverting Coax/Twisted Pair Serial Input. Polarity is programmable (see Table 27).
56	IN3+	Channel 3 Noninverting Coax/Twisted Pair Serial Input. Polarity is programmable (see Table 27).
—	EP	Exposed Pad. EP is internally connected to device ground. EP **must** be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Functional Diagram



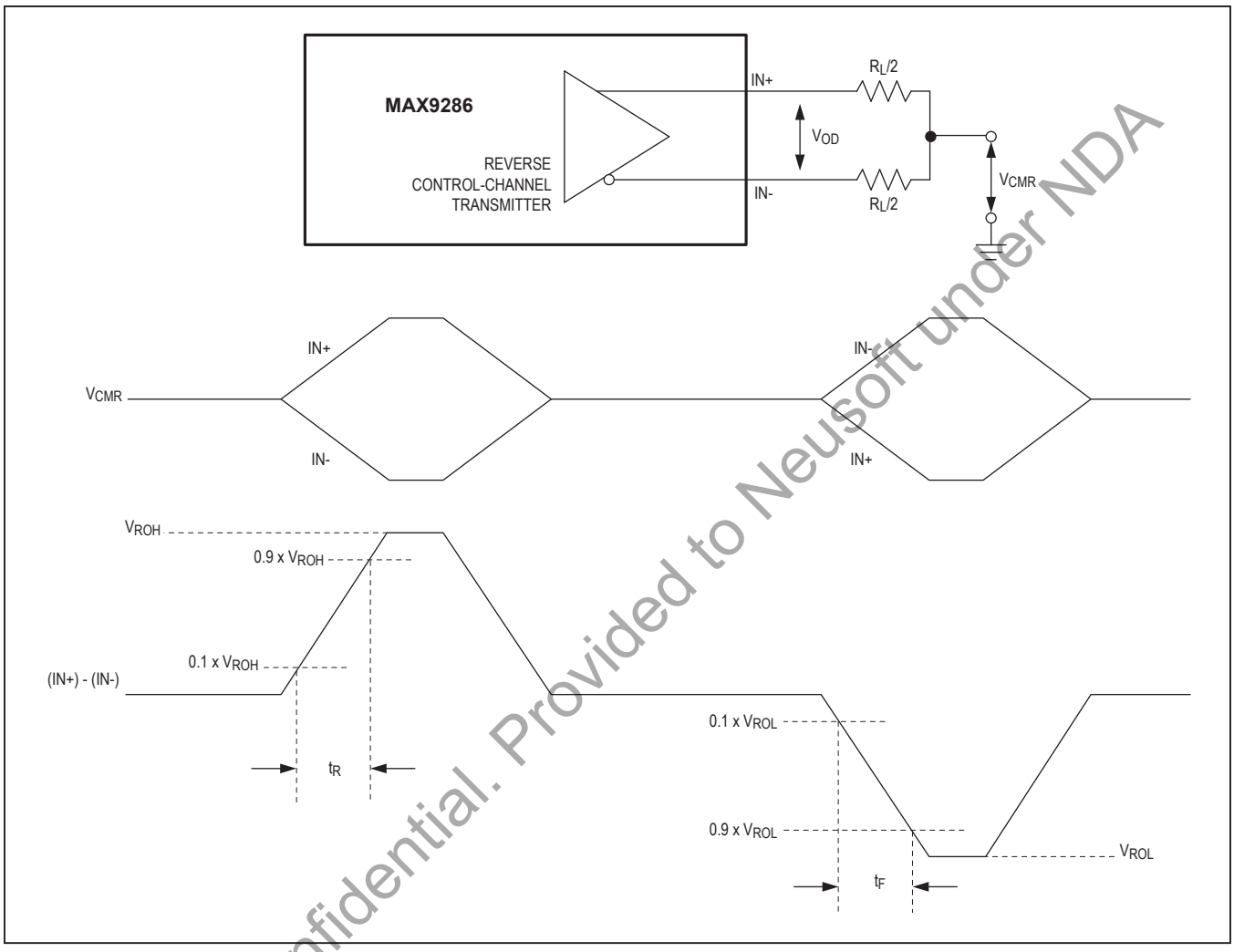


Figure 1. Reverse Control Channel Output Parameters

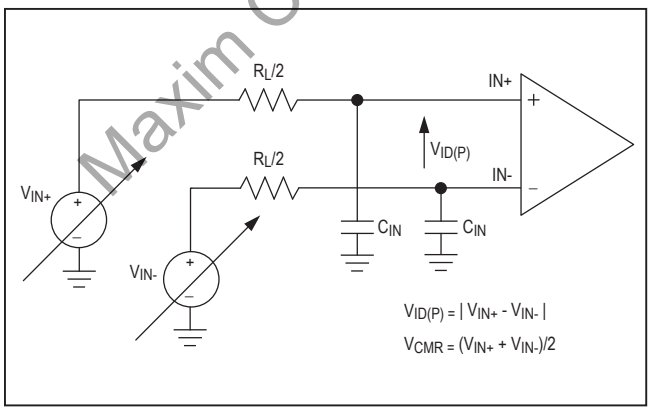


Figure 2. Test Circuit for Differential Input Measurement

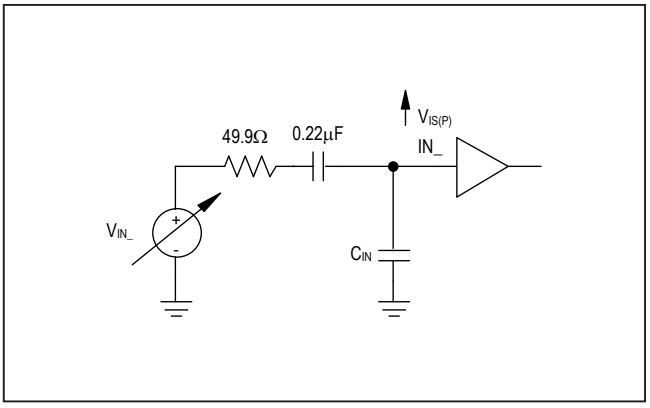


Figure 3. Test Circuit for Single-Ended Input Measurement

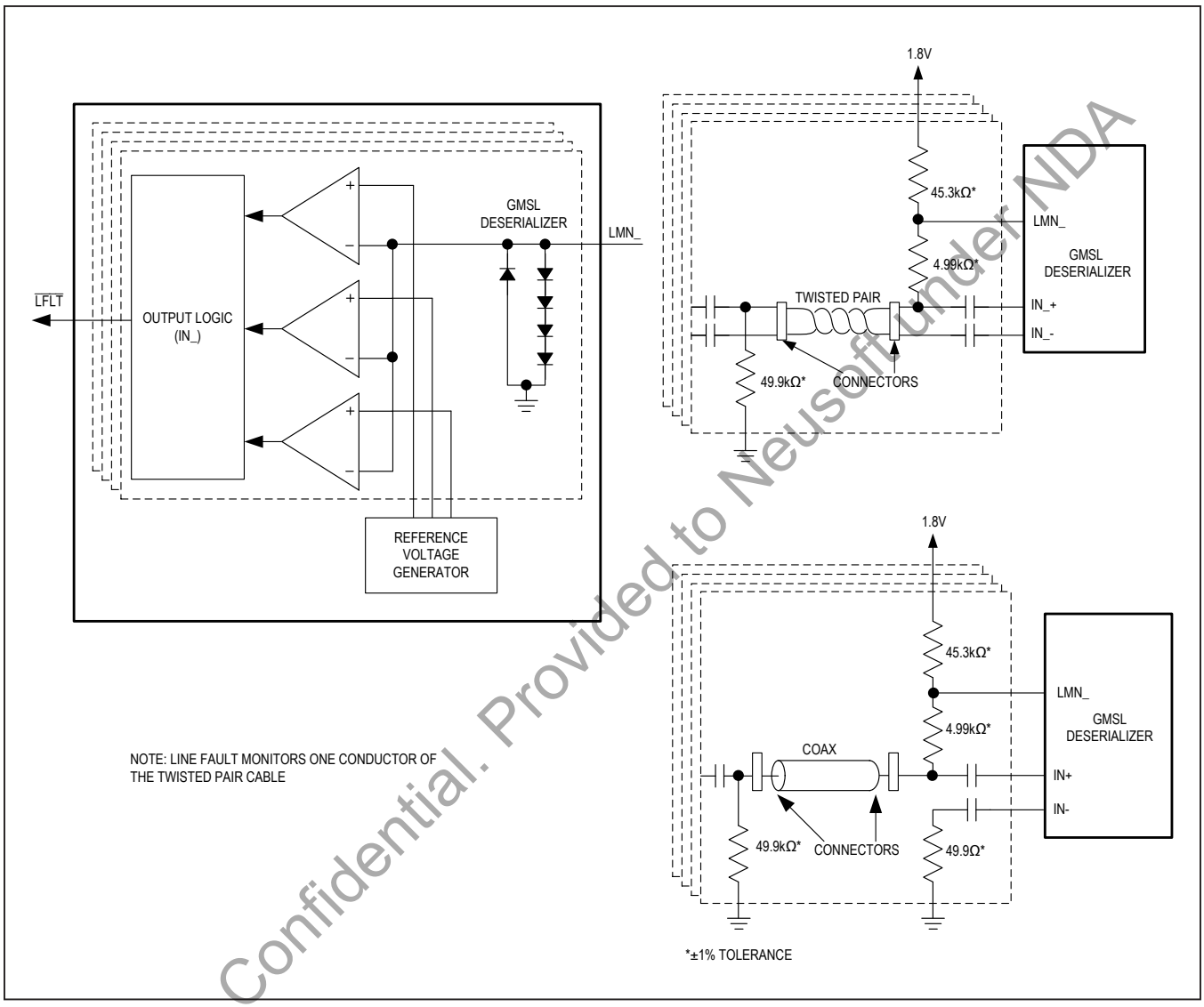


Figure 4. Line Fault

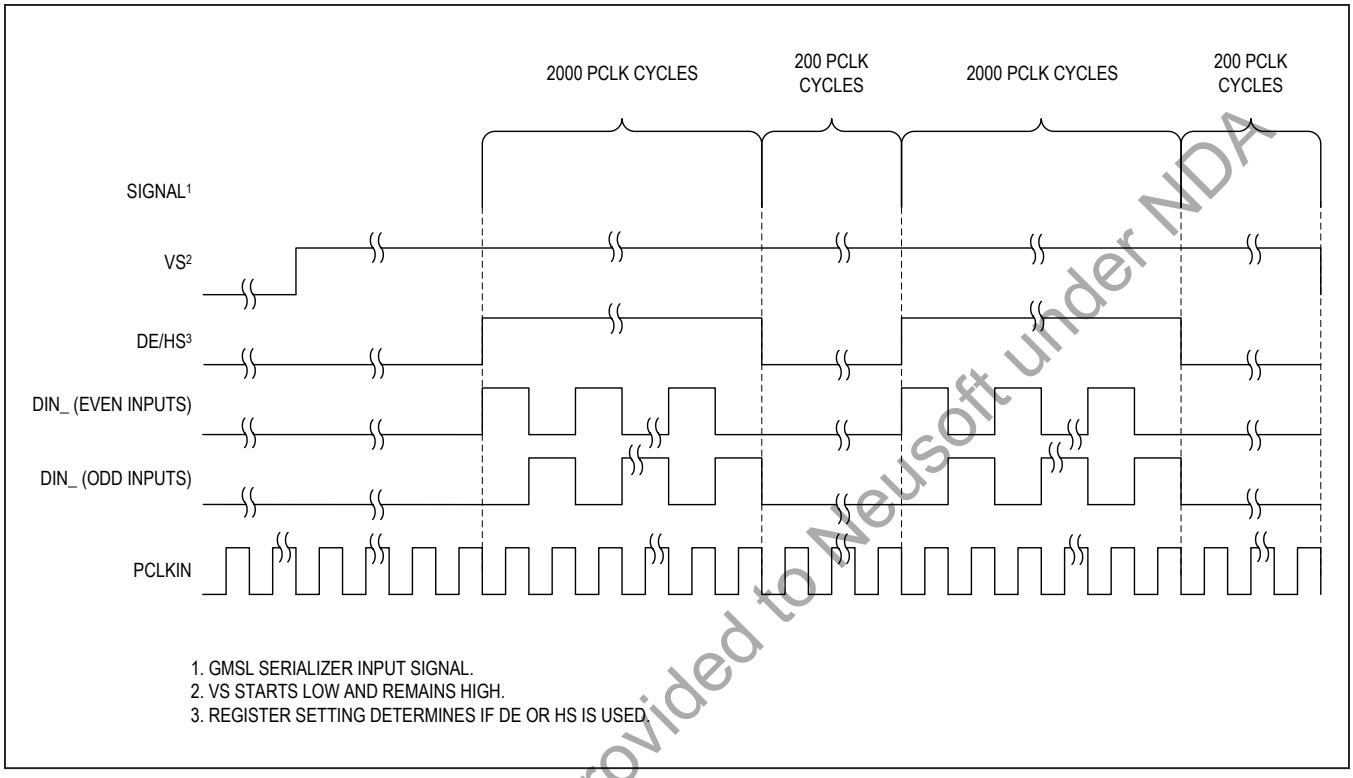


Figure 5. Worst-Case Pattern Output

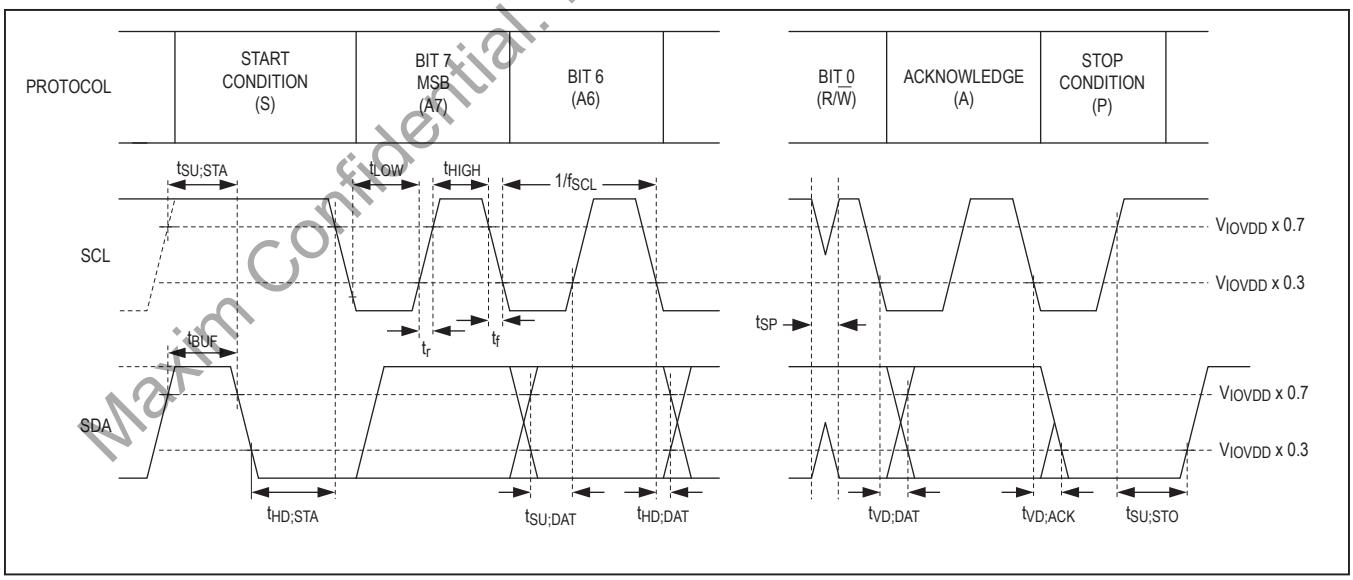


Figure 6. I²C Timing Parameters

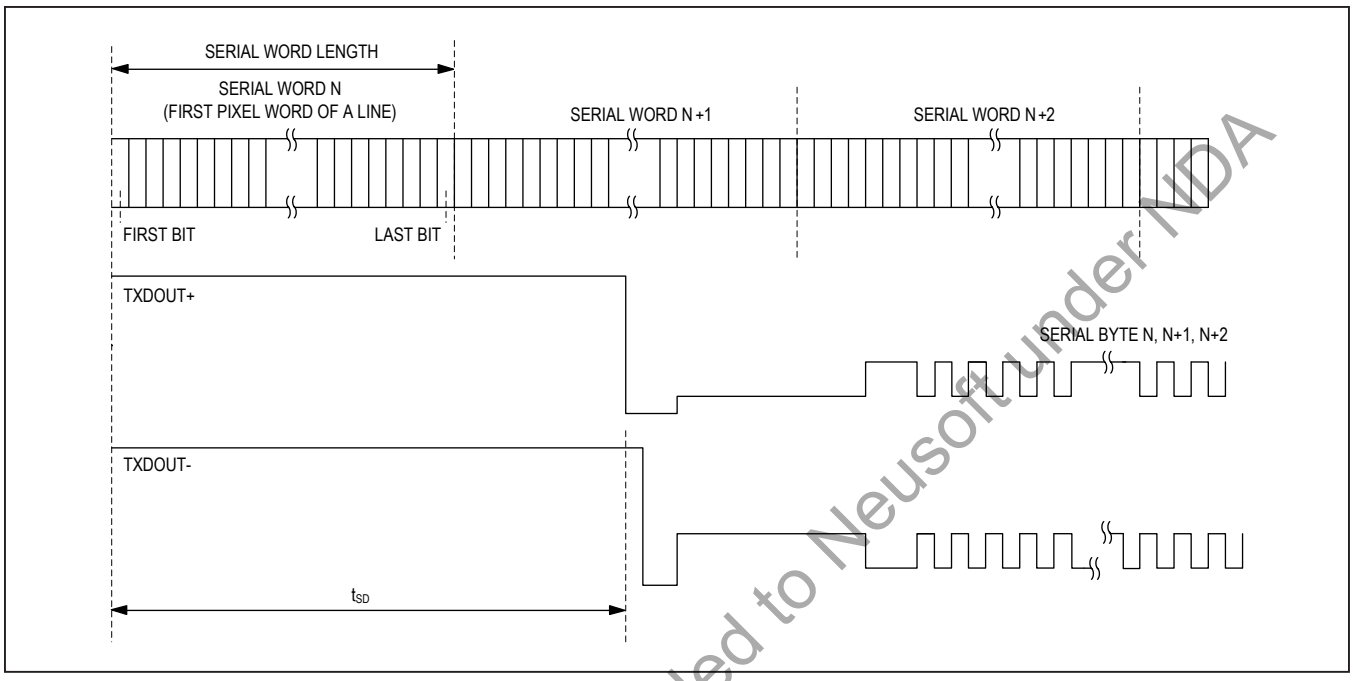


Figure 7. Deserializer Delay

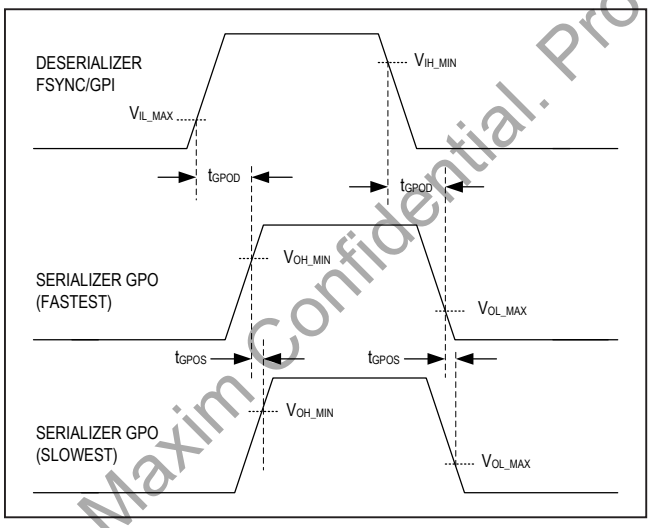


Figure 8. GPI-to-GPO Delay

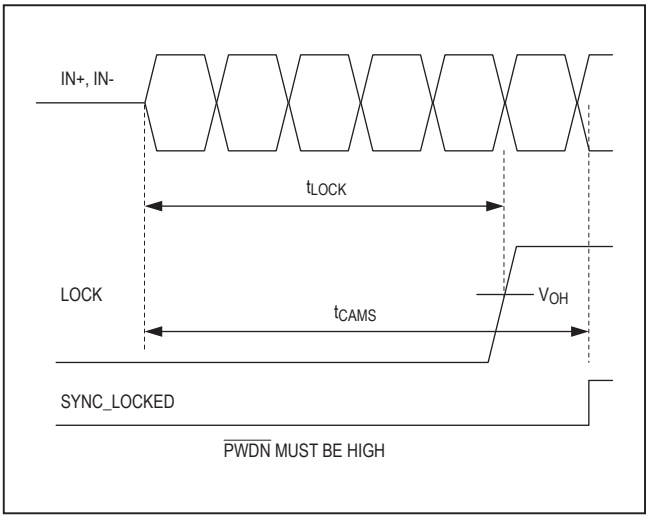


Figure 9. Lock and Camera Sync Time

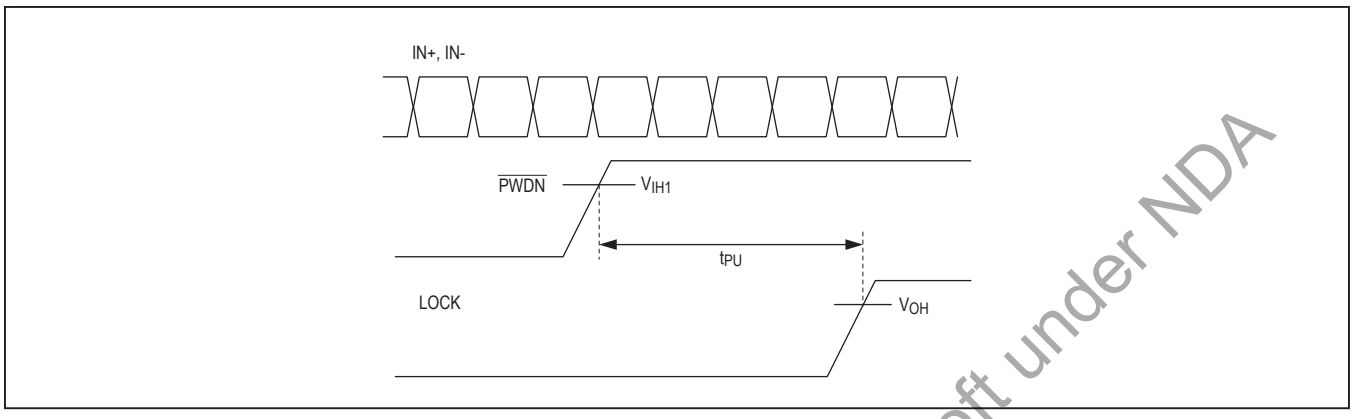


Figure 10. Power-Up Delay

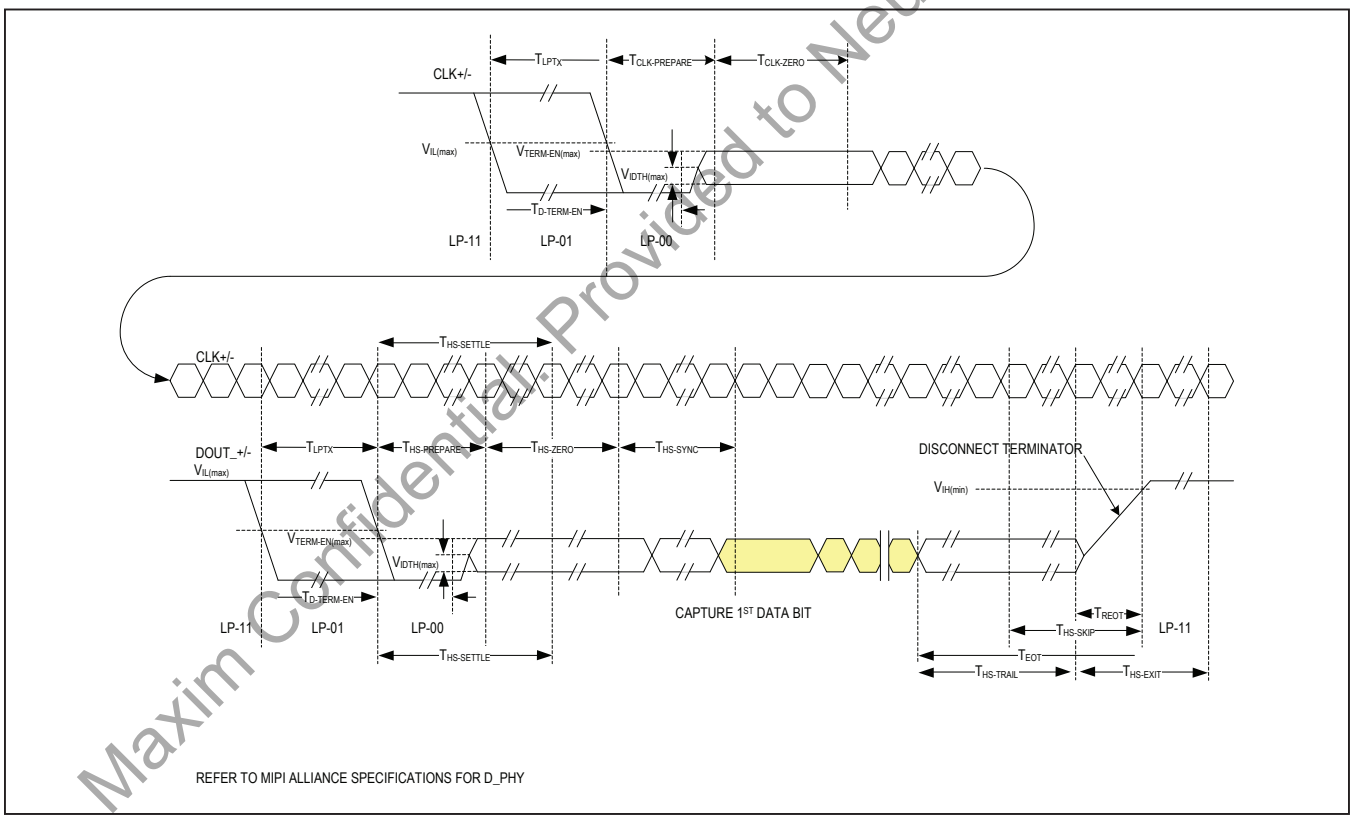


Figure 11. MIPI Output Timing Parameters

Detailed Description

The MAX9286 deserializer, when paired with the MAX9271/MAX9273 serializers, provides the full set of operating features, but is backward compatible with the MAX9249–MAX9281 family of Gigabit multimedia serial link (GMSL) devices and has basic functionality when paired with any GMSL device.

The deserializer synchronizes data from up to four serializers. The each link has a maximum serial-bit rate of 1.5Gbps per link for up to 15m of cable and operates up to a maximum pixel clock of 100MHz (up to 12 bits), or 75MHz (up to 15 bits). This bit rate and output flexibility support a wide range of megapixel image sensors. Input equalization, combined with GMSL serializer pre/deemphasis, and error correction/detection extend the cable length and enhance link reliability.

Two control channel modes send data across the serial link. I^2C-to-I^2C and UART-to-I^2C mode allow a microcontroller's UART or I^2C port to program the deserialzer, serializer(s), and remote I^2C peripherals. Individual link controls and address translation enable the deserializer to manage communication to individual devices, as well as broadcast commands to several links.

The serial input complies with ISO 10605 and IEC 61000-4-2 ESD protection standards.

Register Mapping

Registers set the operating conditions of the deserializers and are programmed using the control channel in base mode (Table 27). The MAX9286 holds its own device address and the device addresses used by address translation. Similarly, the serializer holds its own device address and the address of the MAX9286. Whenever the deserializer device address is changed be sure to write the new address to both devices. The default device address of the deserializer is set by the ADD[1:0] inputs (see Table 1). Register 0x09 holds the device address.

Table 1. Device Address Defaults (Register 0x09)

PIN		DEVICE ADDRESS (BIN)								DESERIALIZER DEVICE ADDRESS (hex)
ADD1	ADD0	D7	D6	D5	D4	D3	D2	D1	D0	
Low	Low	1	0	0	X*	0	0	0	R/$\overline{W}$	90
Low	High	1	0	0	X*	0	1	0	R/$\overline{W}$	94
Low	Open	1	0	0	X*	1	0	0	R/$\overline{W}$	98
High	Low	1	1	0	X*	0	0	0	R/$\overline{W}$	D0
High	High	1	1	0	X*	0	1	0	R/$\overline{W}$	D4
High	Open	1	1	0	X*	1	0	0	R/$\overline{W}$	D8
Open	Low	0	1	0	X*	0	0	0	R/$\overline{W}$	50
Open	High	0	1	0	X*	0	1	0	R/$\overline{W}$	54
Open	Open	0	1	0	X*	1	0	0	R/$\overline{W}$	58

**X = 0 for the serializer address, X = 1 for the deserializer address.*

Frame Combination

The deserializer receives serialized data from up to four input links. The maximum active frame width accepted is 1280 pixels. The input frames are synchronized, and combined in to a single (4 x W) x H or W x (4 x H) frame (Figure 12). The output data rate is N times the input data rate where N is the number of active serial links.

Serial Link Signaling and Data Format

The serializer uses differential CML signaling to drive twisted-pair cable and single-ended CML to drive coaxial cable with programmable pre/deemphasis and AC-coupling. The deserializer uses AC-coupling and programmable channel equalization.

GMSL uses three different serial link modes controlled by the BWS bit/pin: 24-bit mode (BWS = low), 32-bit mode (BWS = high), and a 27-bit high-bandwidth mode (BWS = open). Input data is scrambled and then 8b/10b coded (9b10b in high-bandwidth mode). The deserializer recovers the embedded serial clock, then samples, decodes, and descrambles the data. Two bits are reserved for the embedded forward control channel and the parity bit of the serial word (see Figure 13, Figure 14, and Figure 15). An additional 6 bits are reserved if error detection/correction is used (EDC). The remaining bits are either a single video word (DBL = 0), or as two half-width video words (DBL = 1). The total bit width of the video word depends on BWS, EDC, and DBL.

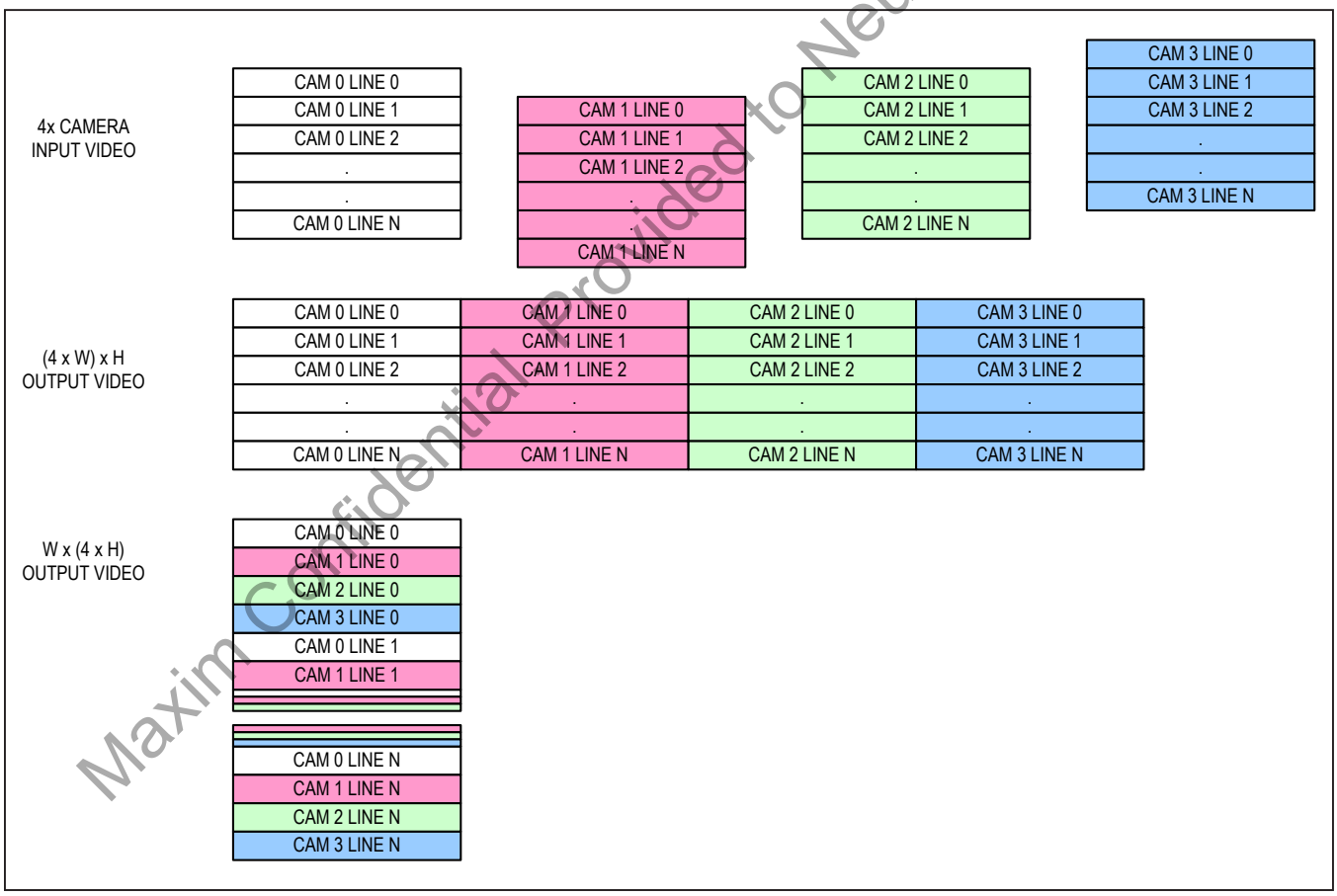


Figure 12. Frame Combination

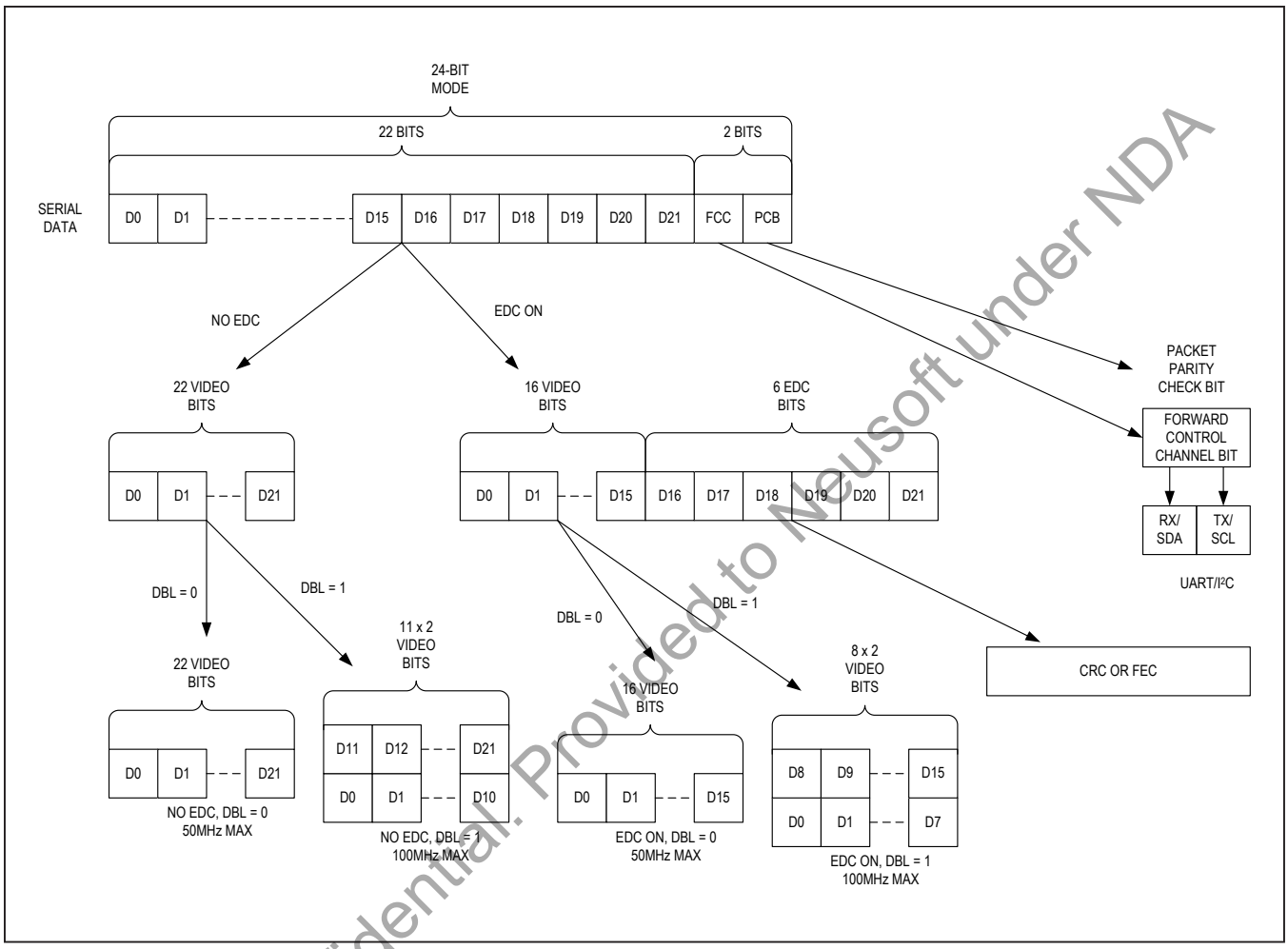


Figure 13. 24-Bit Mode Serial Data Format

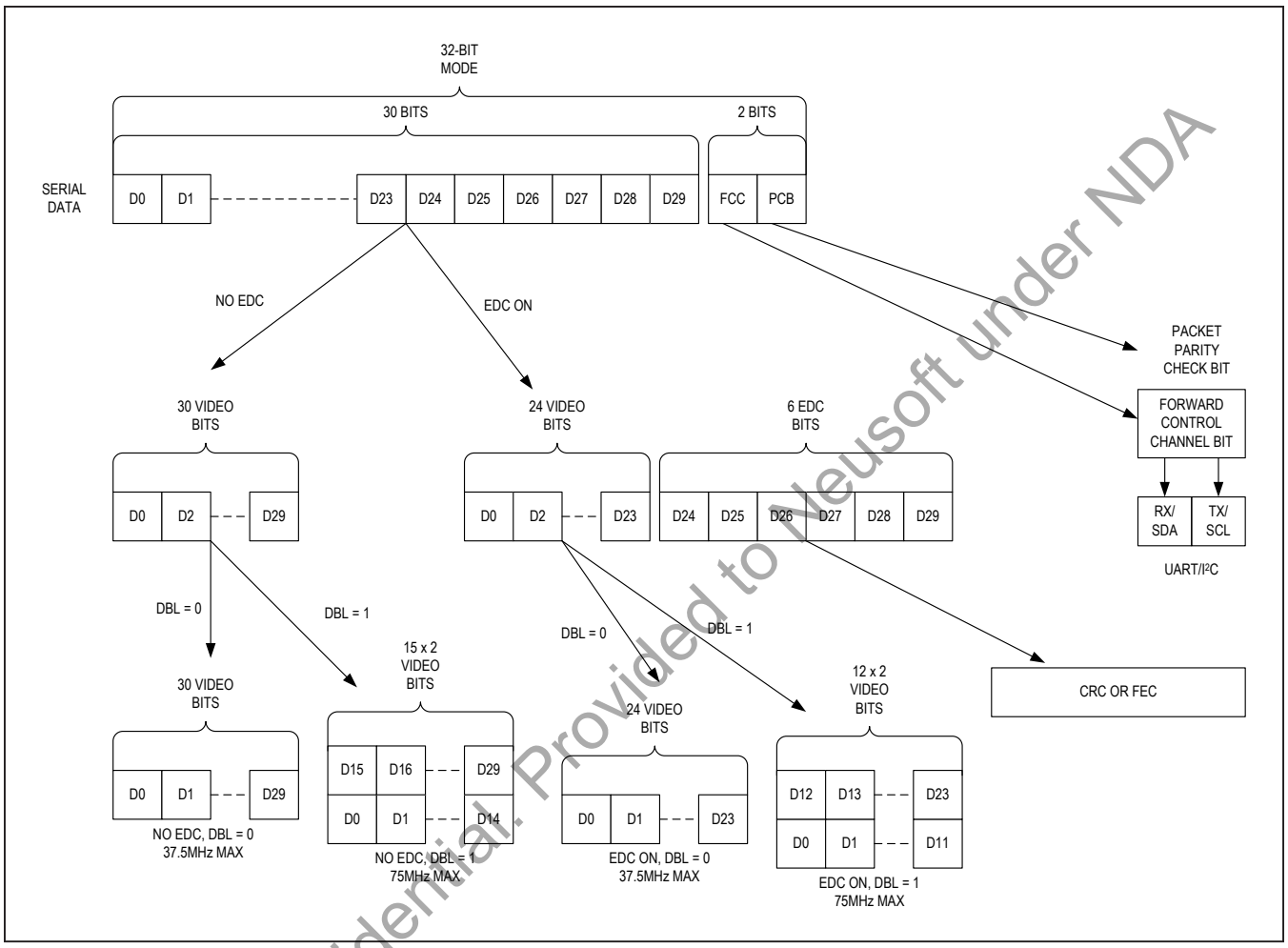


Figure 14. 32-Bit Mode Serial Data Format

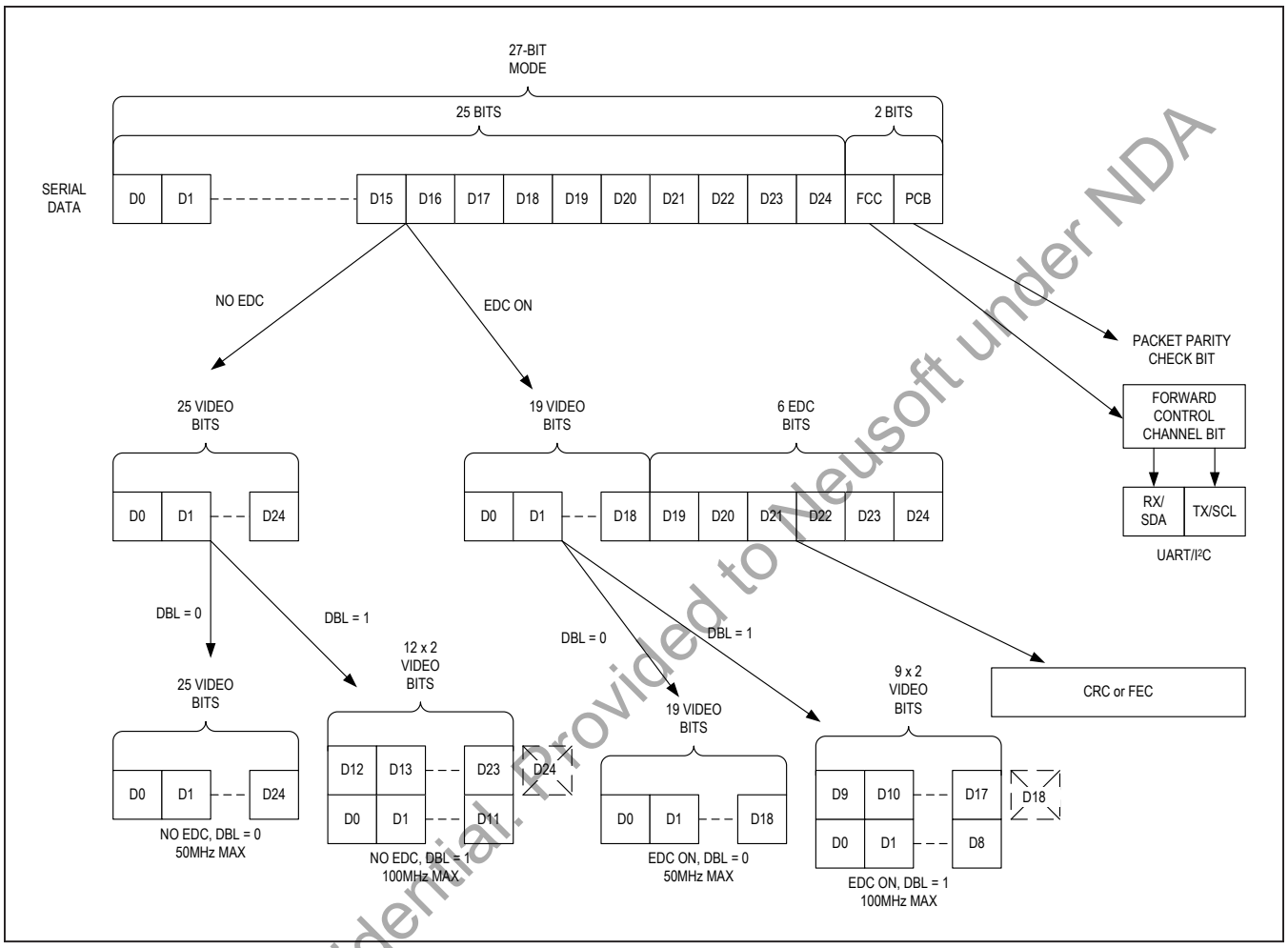


Figure 15. 27-Bit High-Bandwidth Mode Serial Data Format

Maximum Input/Output Data Rate

The input/output bit width, CSI-2 format, and GMSL settings such as error detection/correction (EDC) determine the usable data rate ranges. Table 2 lists the maximum serializer input clock rates for various CSI-2 formats.

Data Formats and Configuration

Table 3 to Table 18 list the required settings and input pixel clock ranges for various input formats. Figure 16 to Figure 31 list the input and output map.

Table 2. Maximum Serializer Input Clock Rates

DEVICE	MAX SERIALIZER INPUT CLOCK RATE (MHz)							
	RAW							
	8	10	11 x 2†	12	12 x 2†	14	16†	20†
MAX9271	100	100[1]	75	75	75	75[2]	100	100[1]
MAX9273	100	100[1]	75	75	75	75[2]	100	100[1]
OTHER GMSL*	50	50	50	50	50	50	50	50

DEVICE	MAX SERIALIZER INPUT CLOCK RATE (MHz)							
	YUV			RGB			USER-DEFINED 24-BIT	USER-DEFINED 8-BIT
	8†	10†	12	565	666	888		
MAX9271	100	100[1]	N/A	N/A	N/A	N/A	N/A	100
MAX9273	100	100[1]	N/A	50	50[3]	N/A	N/A	100
OTHER GMSL*	50	50	37.5	50	50	50	37.5	50

**EDC not supported.*

†Two clocked words per pixel.

1 *Pixel rate is 75MHz if EDC is used.*

2 *Pixel rate is 50MHz if EDC is used.*

3 *Pixel rate is 37.5MHz if EDC is used.*

Table 3. Data Rate and Config Selection Table (RAW8)

DEVICE	EDC	HVEN	BWS	DBL	PCLK RATE* (MHz)
9271/ 9273	No	X	0	1	33.33 to 100
	Yes	0	1	1	25 to 75
		1	0	1	33.33 to 100
Other	—	—	0	—	16.66 to 50

X = Don't care.

**If a lower clock rate is needed and DBL = 1, set DBL = 0 to half the all frequencies. After setting DBL = 0, or if double mode is not supported, set DRS = 1 to further divide all frequencies in half.*

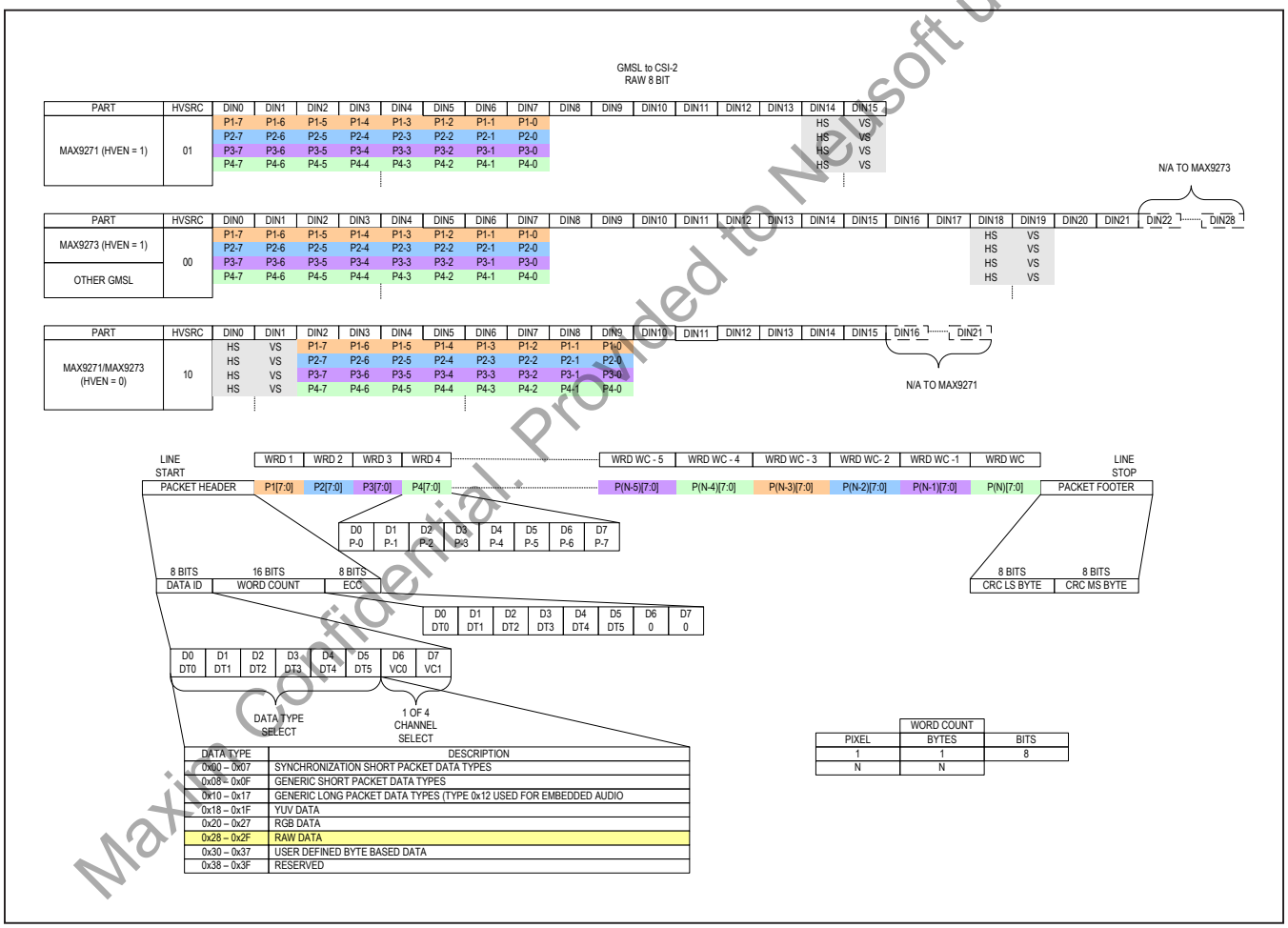


Figure 16. RAW8 Input Map

Table 4. Data Rate and Config Selection Table (RAW10)

DEVICE	EDC	HVEN	BWS	DBL	PCLK RATE* (MHz)
9271/ 9273	No	0	1	1	25 to 75
		1	0	1	33.33 to 100
	Yes	X	1	1	25 to 75
Other	—	—	0	—	16.66 to 50

X = Don't care.

**If a lower clock rate is needed and DBL = 1, set DBL = 0 to half the all frequencies. After setting DBL = 0, or if double mode is not supported, set DRS = 1 to further divide all frequencies in half.*

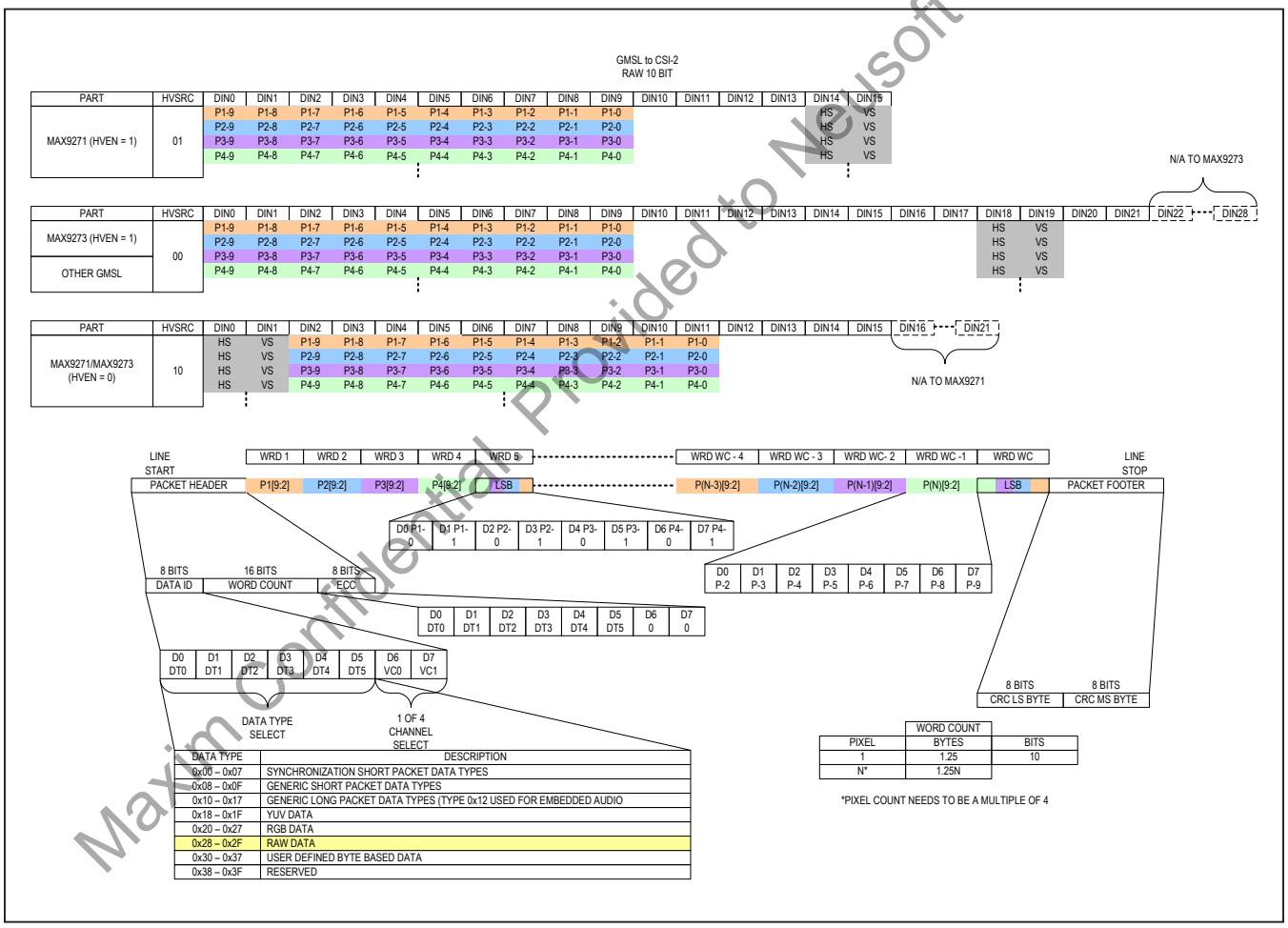


Figure 17. RAW10 Input Map

Table 5. Data Rate and Config Selection Table (RAW11x2)

DEVICE	EDC	HVEN	BWS	DBL	SERIALIZER INPUT CLOCK RATE* (MHz)
9271/ 9273	No	X	1	1	25 to 75
	Yes	0	0	0	16.66 to 50
		1	1	1	25 to 75
Other	—	—	0	—	16.66 to 50

X = Don't care.

**If a lower clock rate is needed and DBL = 1, set DBL = 0 to half the all frequencies. After setting DBL = 0, or if double mode is not supported, set DRS = 1 to further divide all frequencies in half.*

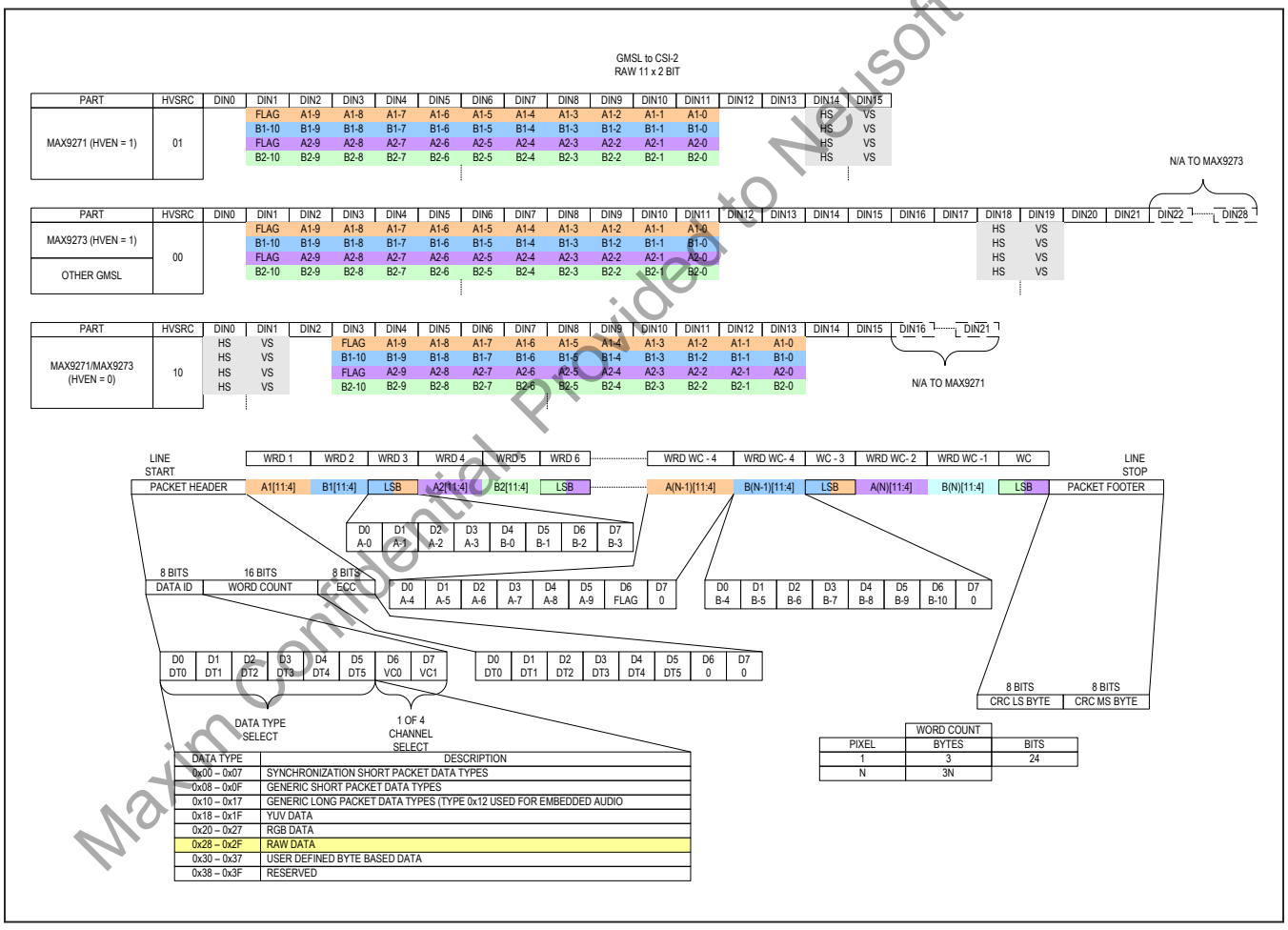


Figure 18. RAW11x2 Input Map

Table 6. Data Rate and Config Selection Table (RAW12)

DEVICE	EDC	HVEN	BWS	DBL	SERIALIZER INPUT CLOCK RATE* (MHz)
9271/ 9273	No	X	1	1	25 to 75
	Yes	0	0	0	16.66 to 50
		1	1	1	25 to 75
Other	—	—	0	—	16.66 to 50

X = Don't care.

**If a lower clock rate is needed and DBL = 1, set DBL = 0 to half the all frequencies. After setting DBL = 0, or if double mode is not supported, set DRS = 1 to further divide all frequencies in half.*

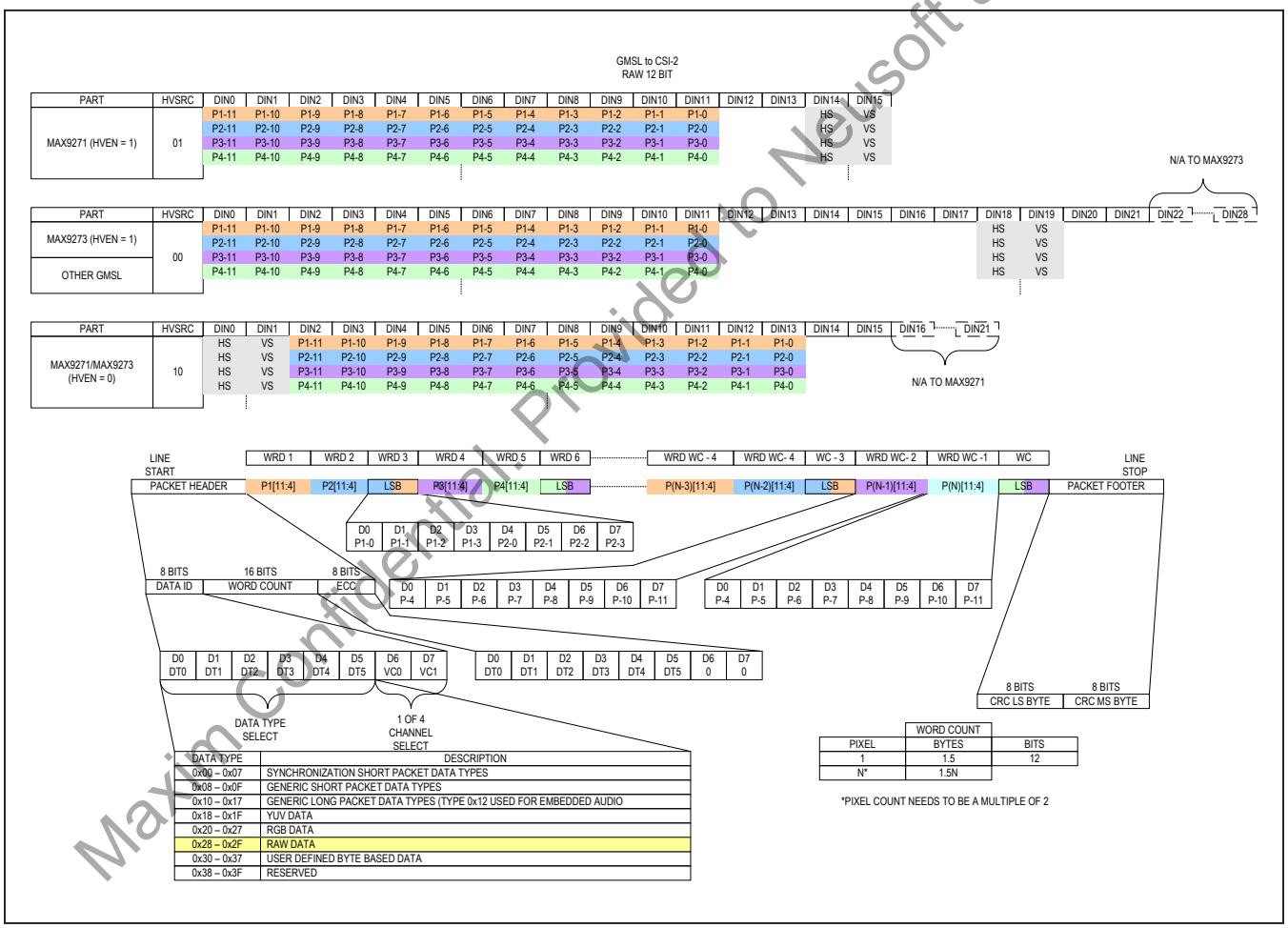


Figure 19. RAW12 Input Map

Table 7. Data Rate and Config Selection Table (RAW12x2)

DEVICE	EDC	HVEN	BWS	DBL	SERIALIZER INPUT CLOCK RATE* (MHz)
9271/ 9273	No	X	1	1	25 to 75
	Yes	0	0	0	16.66 to 50
		1	1	1	25 to 75
Other	—	—	0	—	16.66 to 50

X = Don't care.

**If a lower clock rate is needed and DBL = 1, set DBL = 0 to half the all frequencies. After setting DBL = 0, or if double mode is not supported, set DRS = 1 to further divide all frequencies in half.*

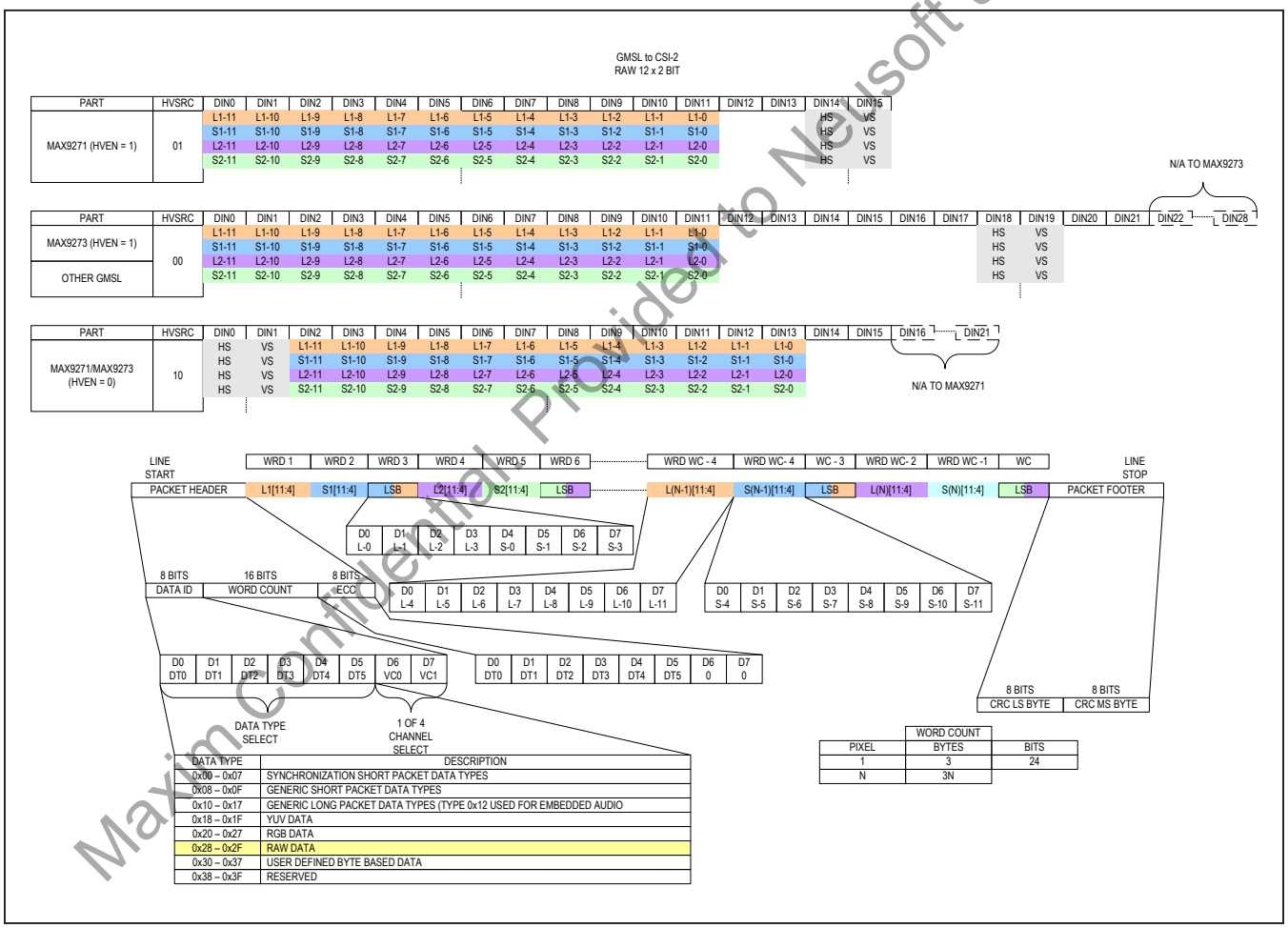


Figure 20. RAW12x2 Input Map

Table 8. Data Rate and Config Selection Table (RAW14)

DEVICE	EDC	HVEN	BWS	DBL	SERIALIZER INPUT CLOCK RATE* (MHz)
9271/ 9273	X	X	0	0	16.66 to 50
Other	—	—	0	—	16.66 to 50

X = Don't care.

**If a lower clock rate is needed and DBL = 1, set DBL = 0 to half the all frequencies. After setting DBL = 0, or if double mode is not supported, set DRS = 1 to further divide all frequencies in half.*

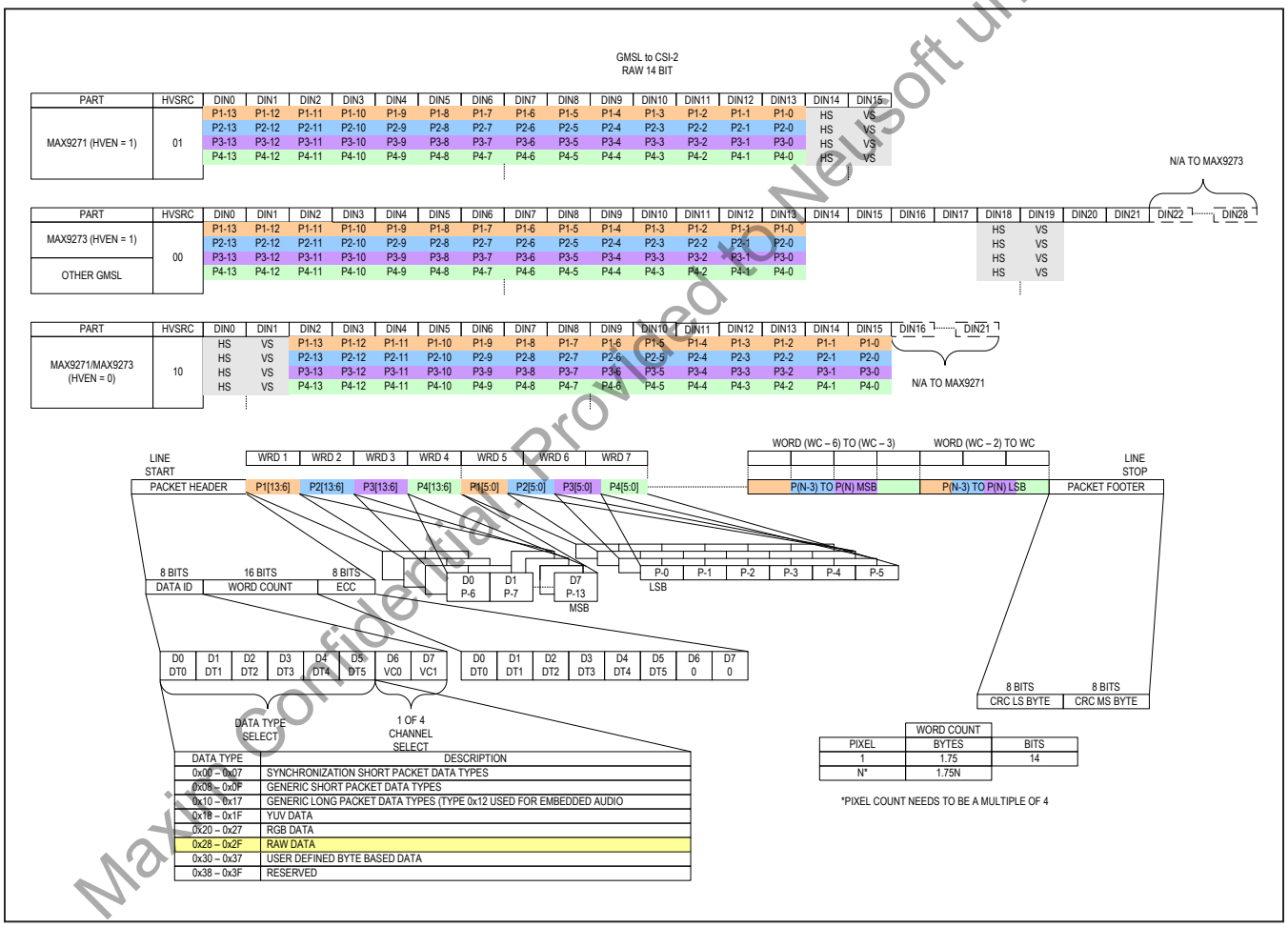


Figure 21. RAW14 Input Map

Table 9. Data Rate and Config Selection Table (RAW16)

DEVICE	EDC	HVEN	BWS	DBL	SERIALIZER INPUT CLOCK RATE* (MHz)
9271/ 9273	No	X	0	1	33.33 to 100
	Yes	0	1	1	25 to 75
		1	0	1	33.33 to 100
Other	—	—	0	—	16.66 to 50

X = Don't care.

**If a lower clock rate is needed and DBL = 1, set DBL = 0 to half the all frequencies. After setting DBL = 0, or if double mode is not supported, set DRS = 1 to further divide all frequencies in half.*

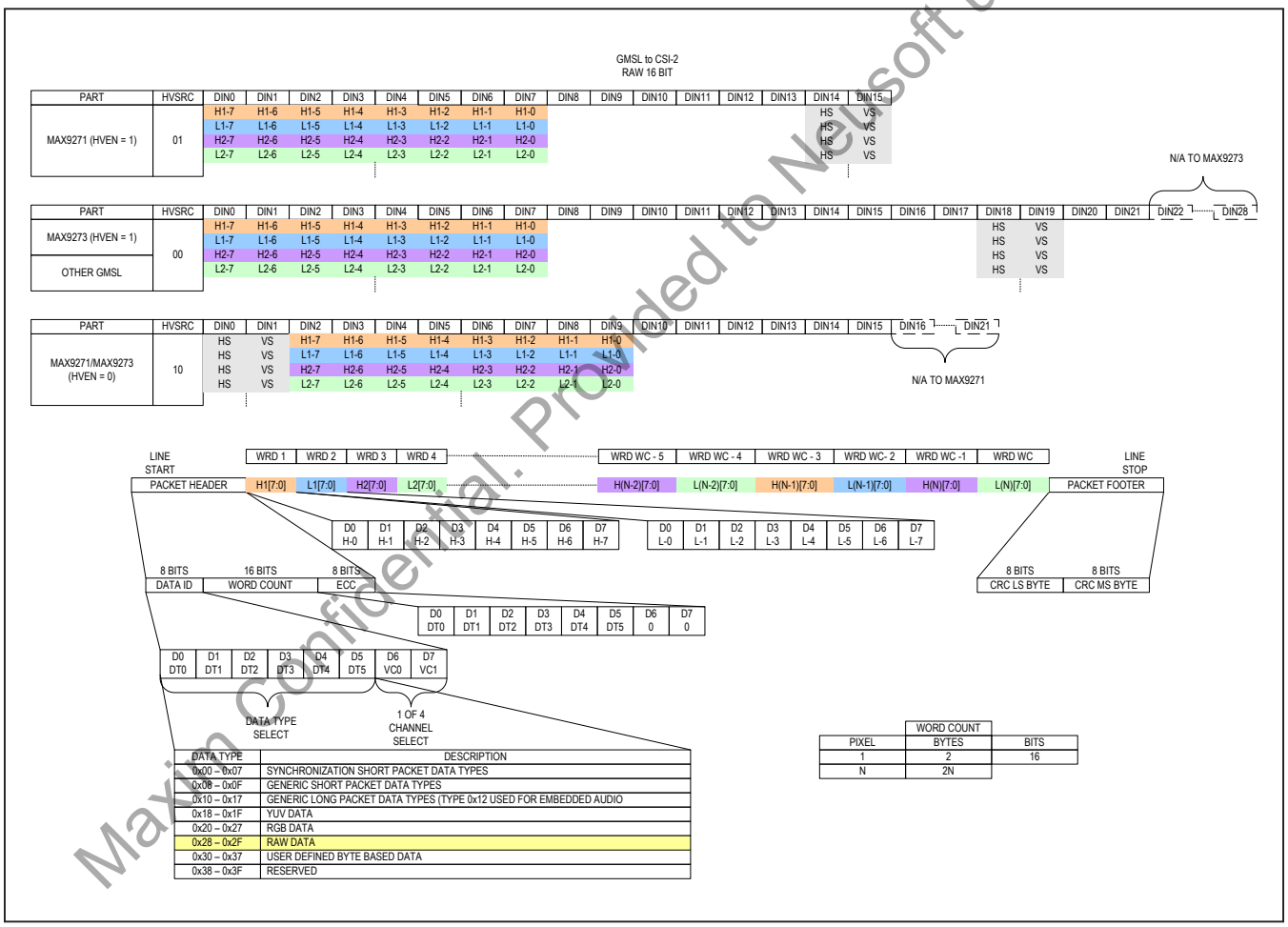


Figure 22. RAW16 Input Map

Table 10. Data Rate and Config Selection Table (RAW20)

DEVICE	EDC	HVEN	BWS	DBL	SERIALIZER INPUT CLOCK RATE* (MHz)
9271/ 9273	No	0	1	1	25 to 75
		1	0	1	33.33 to 100
	Yes	X	1	1	25 to 75
Other	—	—	0	—	16.66 to 50

X = Don't care.

**If a lower clock rate is needed and DBL = 1, set DBL = 0 to half the all frequencies. After setting DBL = 0, or if double mode is not supported, set DRS = 1 to further divide all frequencies in half.*

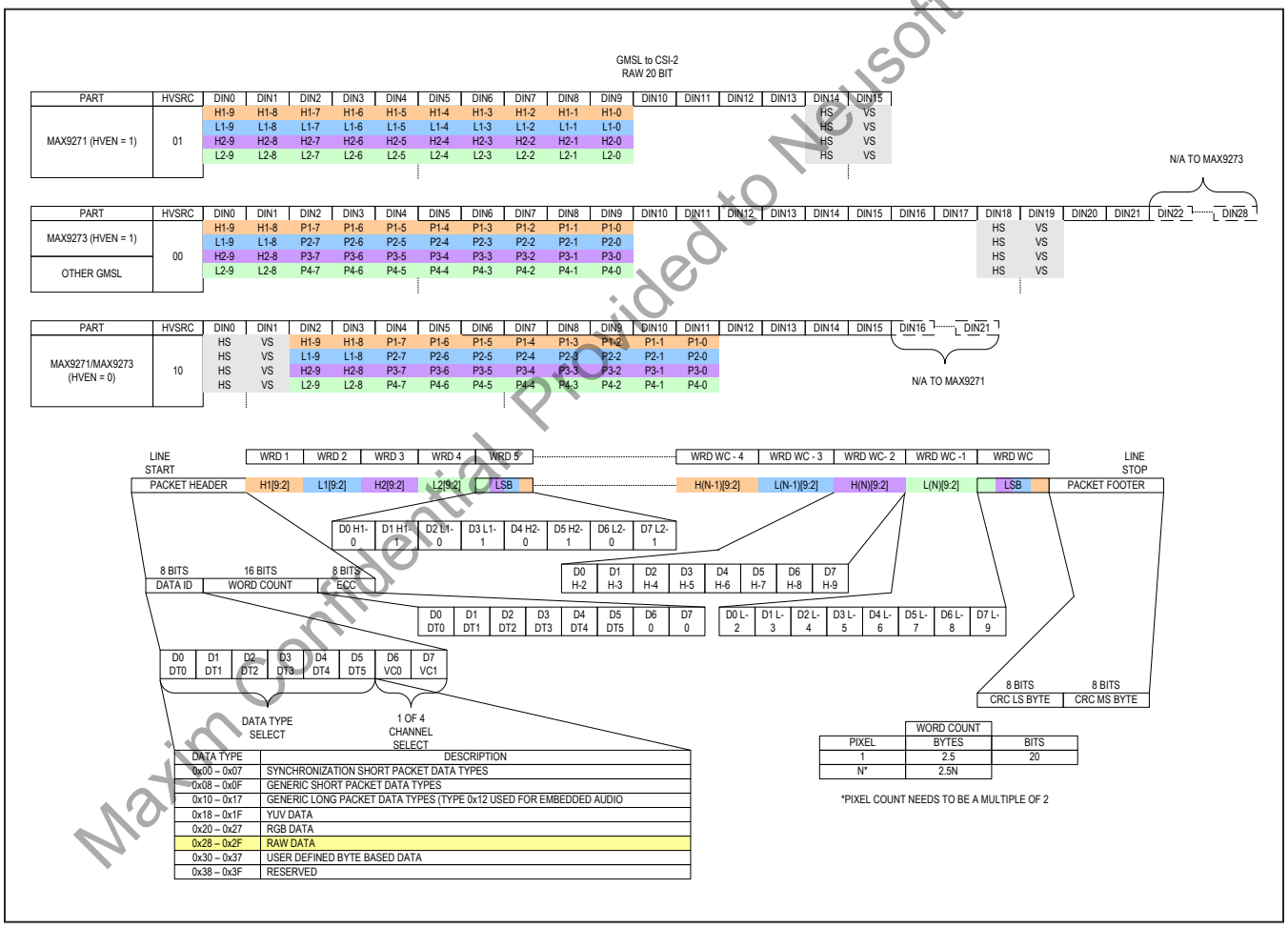


Figure 23. RAW20 Input Map

Table 11. Data Rate and Config Selection Table (YUV8)

DEVICE	EDC	HVEN	BWS	DBL	SERIALIZER INPUT CLOCK RATE* (MHz)
9271/ 9273	No	X	0	1	33.33 to 100
	Yes	0	1	1	25 to 75
		1	0	1	33.33 to 100
Other	—	—	0	—	16.66 to 50

X = Don't care.

**If a lower clock rate is needed and DBL = 1, set DBL = 0 to half the all frequencies. After setting DBL = 0, or if double mode is not supported, set DRS = 1 to further divide all frequencies in half.*

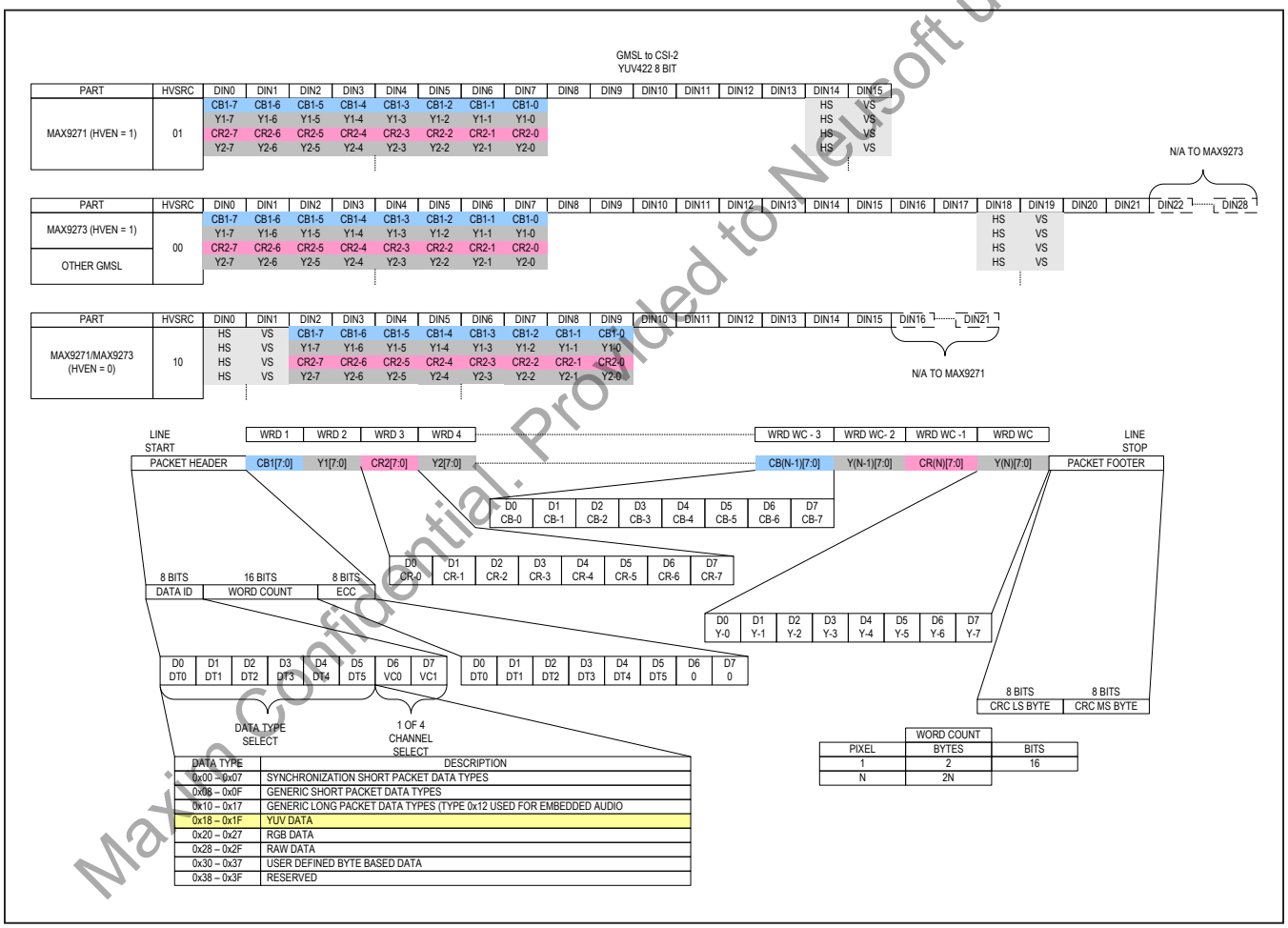


Figure 24. YUV8 Input Map

Table 12. Data Rate and Config Selection Table (YUV10)

DEVICE	EDC	HVEN	BWS	DBL	SERIALIZER INPUT CLOCK RATE* (MHz)
9271/ 9273	No	0	1	1	25 to 75
		1	0	1	33.33 to 100
	Yes	X	1	1	25 to 75
Other	—	—	0	—	16.66 to 50

X = Don't care.

**If a lower clock rate is needed and DBL = 1, set DBL = 0 to half the all frequencies. After setting DBL = 0, or if double mode is not supported, set DRS = 1 to further divide all frequencies in half.*

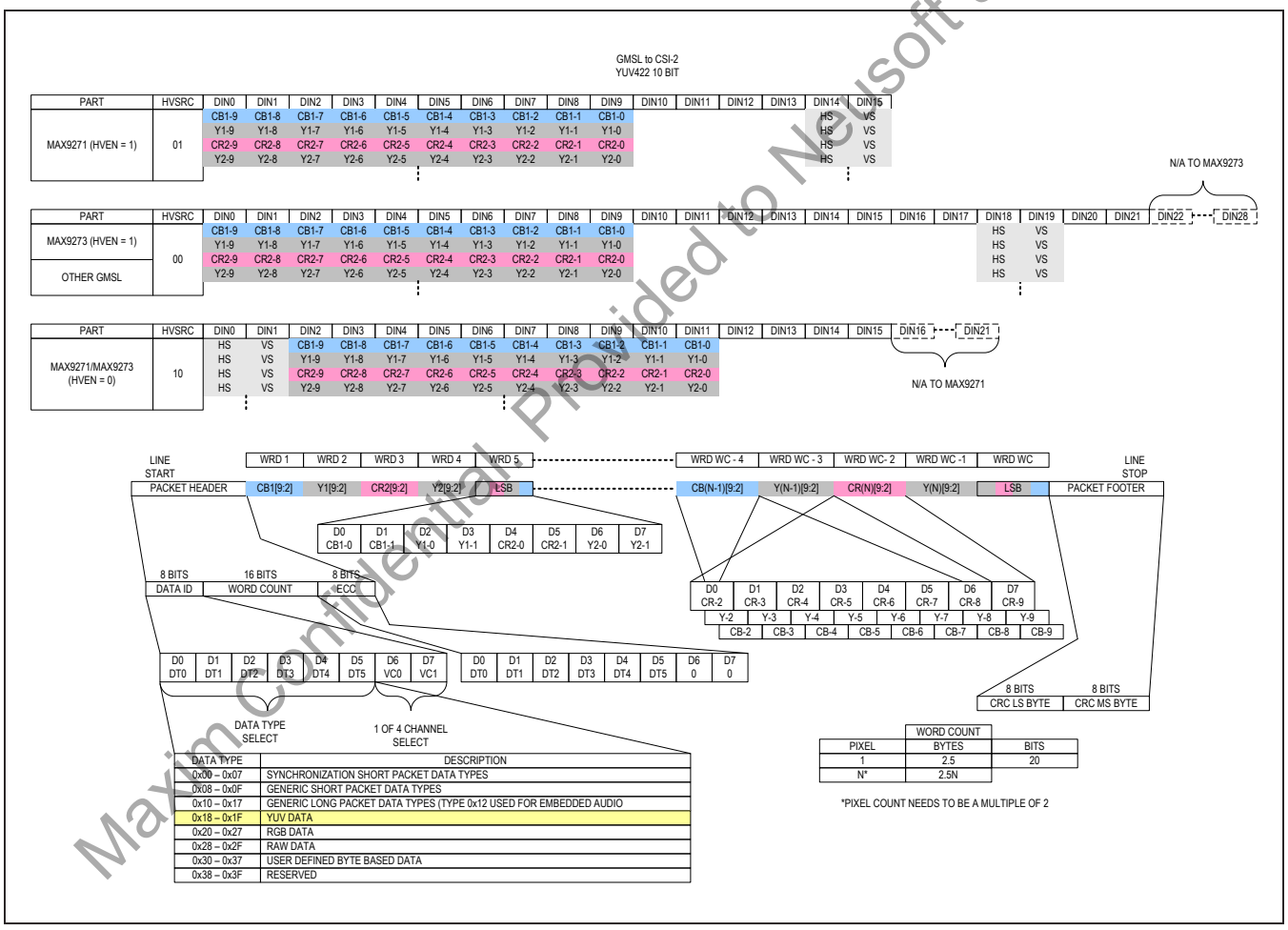


Figure 25. YUV10 Input Map

Table 13. Data Rate and Config Selection Table (YUV12)

DEVICE	EDC	HVEN	BWS	DBL	SERIALIZER INPUT CLOCK RATE* (MHz)
9271/ 9273	No	0	0	0	16.66 to 50
		1	1	1	25 to 75
	Yes	0	0	0	16.66 to 50
		1	1	1	25 to 75
Other	—	—	0	—	16.66 to 50

X = Don't care.

**If a lower clock rate is needed and DBL = 1, set DBL = 0 to half the all frequencies. After setting DBL = 0, or if double mode is not supported, set DRS = 1 to further divide all frequencies in half.*

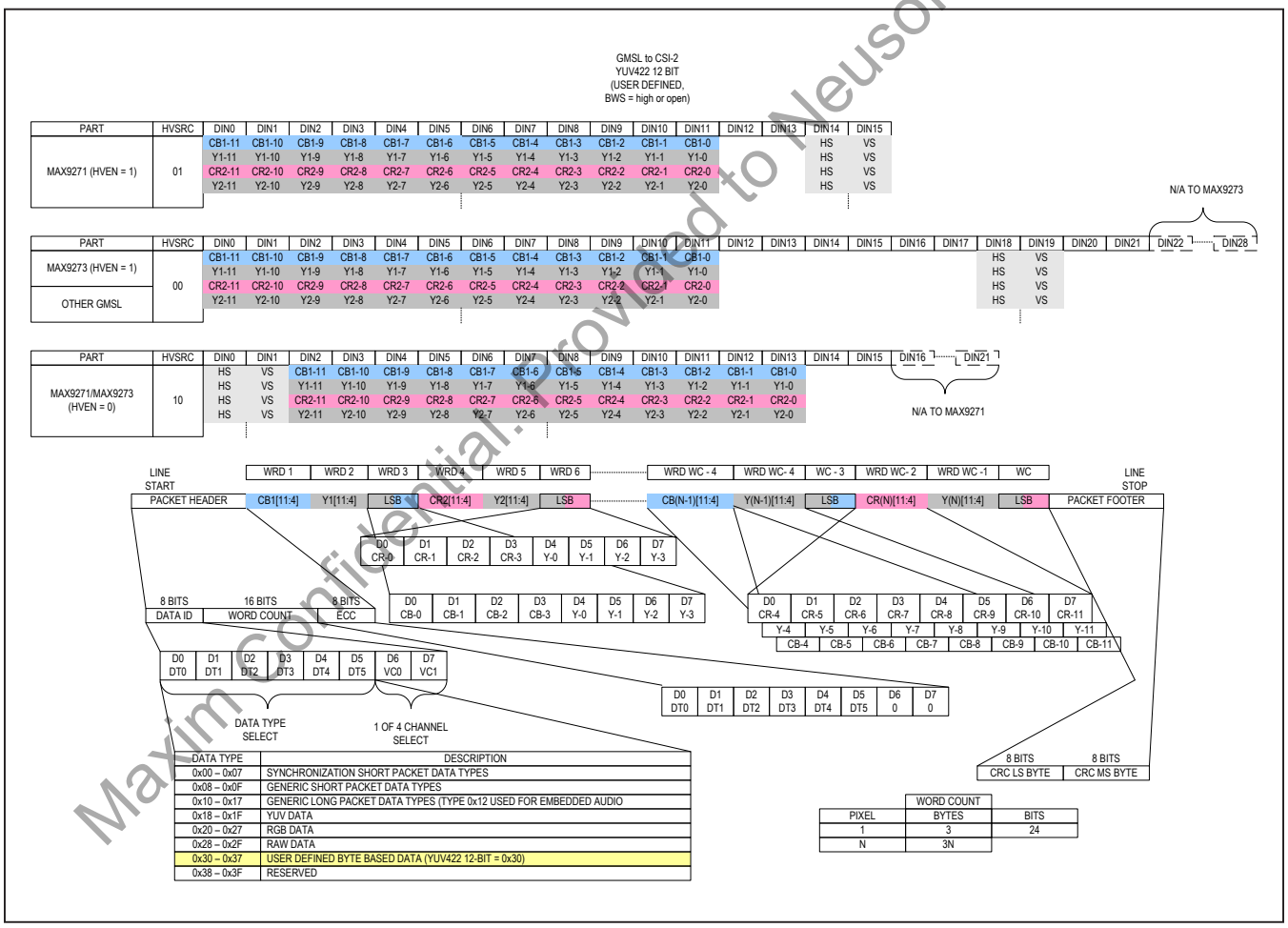


Figure 26. YUV12 Input Map

Table 14. Data Rate and Config Selection Table (RGB565)

DEVICE	EDC	HVEN	BWS	DBL	SERIALIZER INPUT CLOCK RATE* (MHz)
9271	N/A	N/A	N/A	N/A	Not capable
9273	No	X	0	0	16.66 to 50
	Yes	0	1	0	12.5 to 37.5
		1	0	0	16.66 to 50
Other	—	—	0	—	16.66 to 50

X = Don't care.

**If a lower clock rate is needed, set DRS = 1 to divide PCLK in half.*

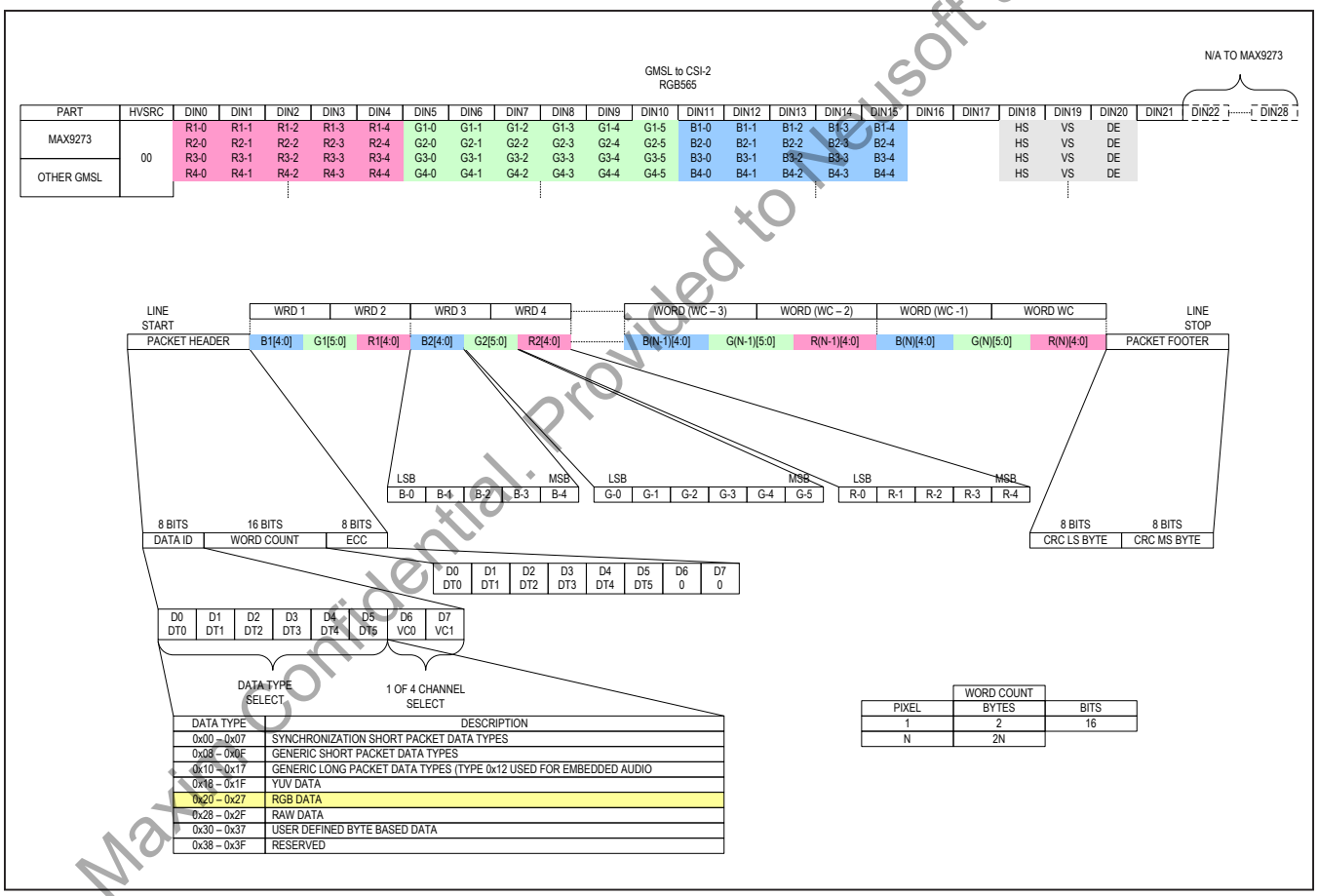


Figure 27. RGB565 Input Map

Table 15. Data Rate and Config Selection Table (RGB666)

DEVICE	EDC	HVEN	BWS	DBL	SERIALIZER INPUT CLOCK RATE* (MHz)
9271	N/A	N/A	N/A	N/A	Not capable
9273	No	X	0	0	16.66 to 50
	Yes	X	1	0	12.5 to 37.5
Other	—	—	0	—	16.66 to 50

X = Don't care.

**If a lower clock rate is needed, set DRS = 1 to divide PCLK in half.*

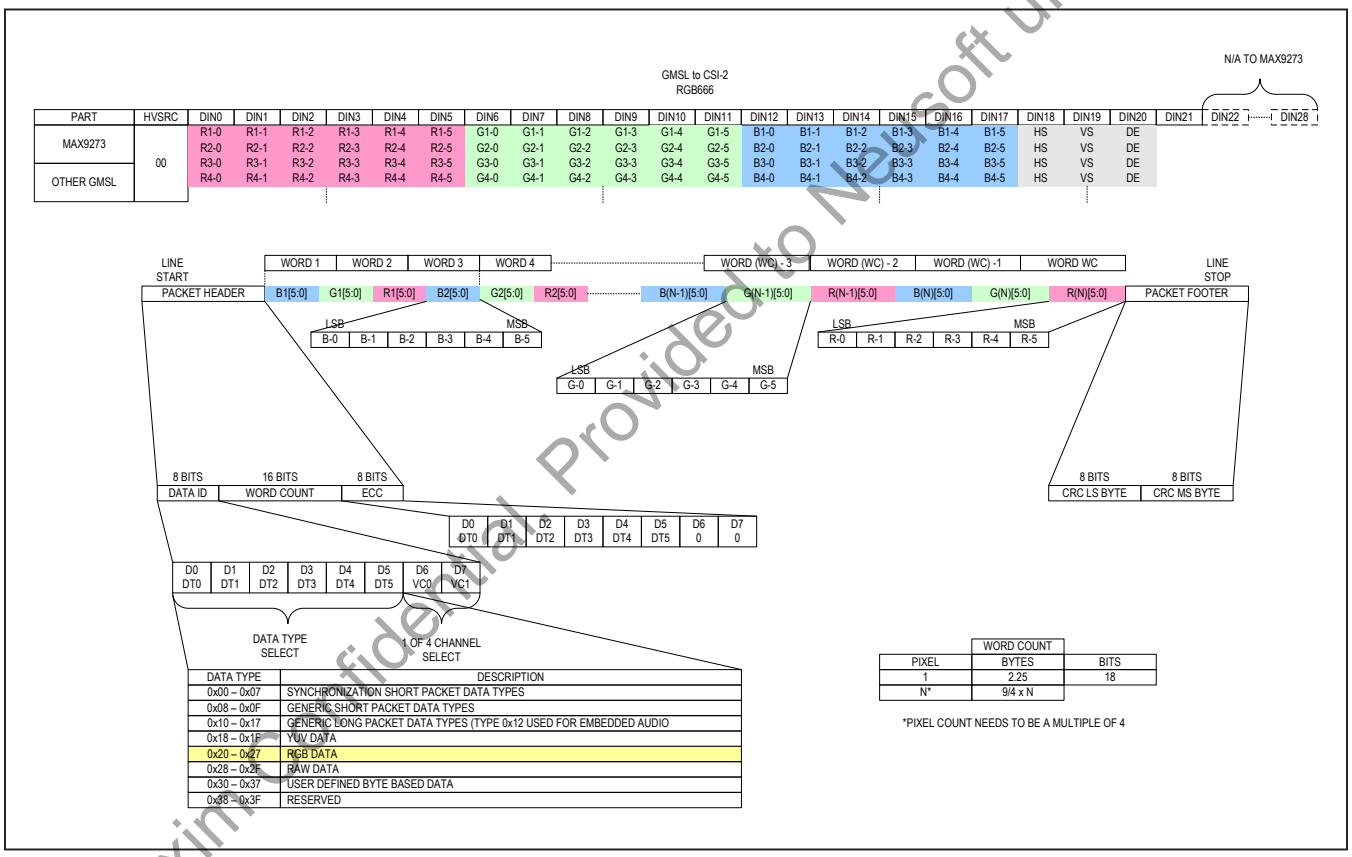


Figure 28. RGB666 Input Map

Table 16. Data Rate and Config Selection Table (RGB888)

DEVICE	BWS	SERIALIZER INPUT CLOCK RATE* (MHz)
9271/ 9273	N/A	Not capable
Other	Open†	36.66 to 50
	1	12.5 to 37.5

X = Don't care.

**If a lower clock rate is needed, set DRS = 1 to divide PCLK in half.*

†*If high bandwidth mode is not supported, use BWS = 1.*

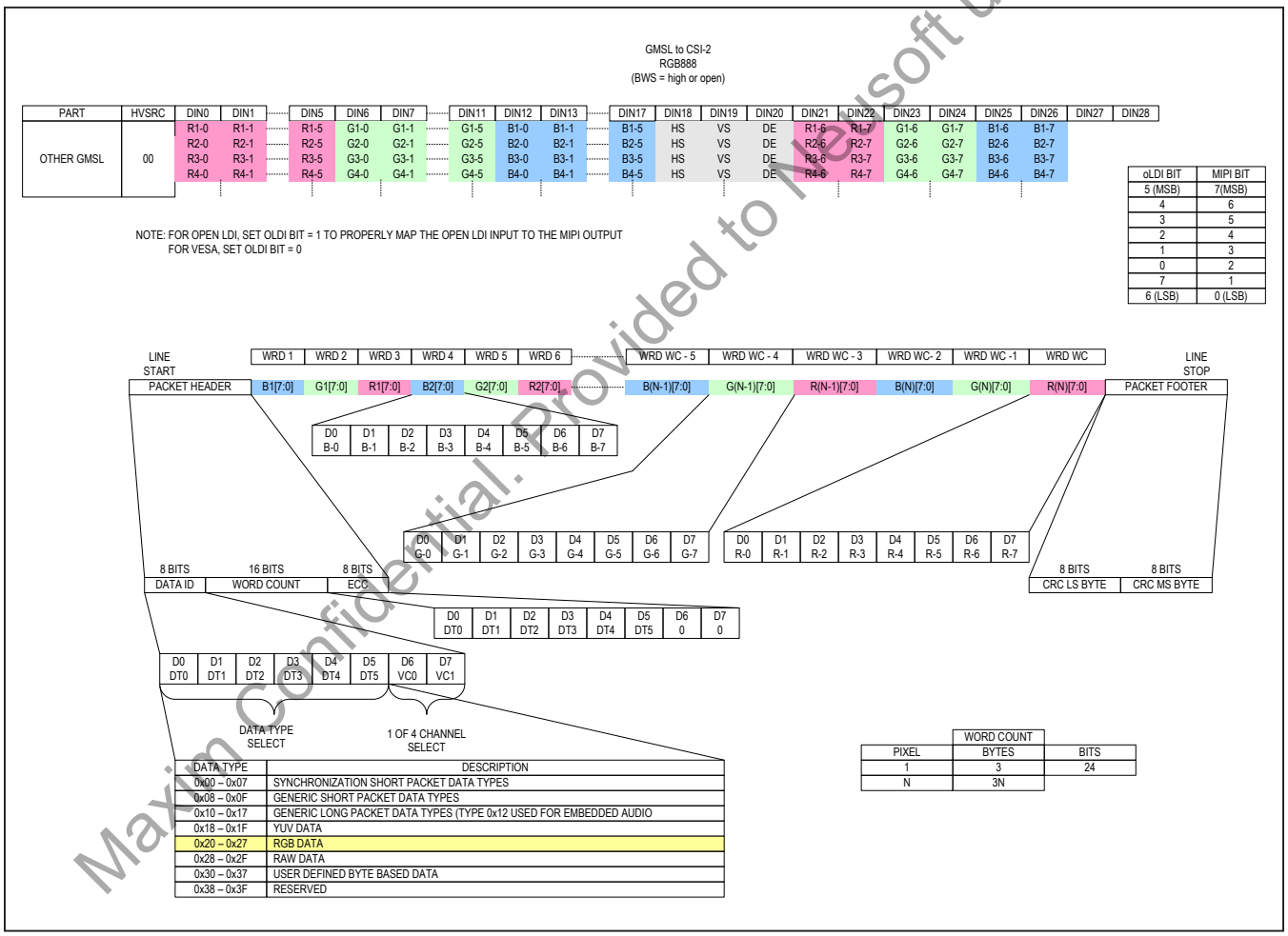


Figure 29. RGB888 Input Map

Table 17. Data Rate and Config Selection Table (User-Defined 8-Bit)

DEVICE	EDC	HVEN	BWS	DBL	PCLK RATE* (MHz)
9271/ 9273	No	X	0	1	33.33 to 100
	Yes	0	1	1	25 to 75
		1	0	1	33.33 to 100
Other	—	—	0	—	16.66 to 50

X = Don't care.

**If a lower clock rate is needed and DBL = 1, set DBL = 0 to half the all frequencies. After setting DBL = 0, or if double mode is not supported, set DRS = 1 to further divide all frequencies in half.*

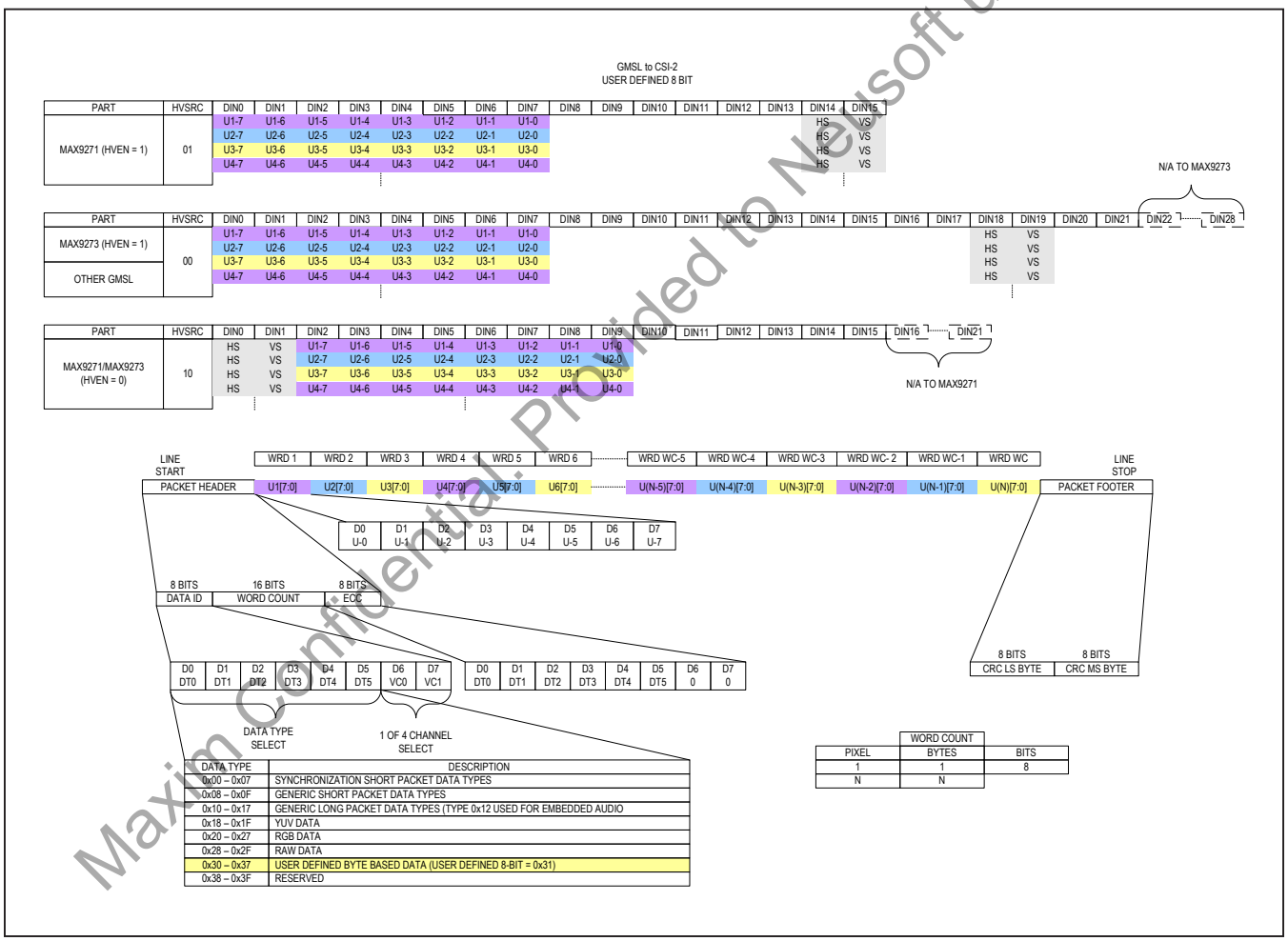


Figure 30. User-Defined 8-Bit Input Map

Table 18. Data Rate and Config Selection Table (User-Defined 24-Bit)

DEVICE	BWS	SERIALIZER INPUT CLOCK RATE* (MHz)
9271/ 9273	N/A	Not capable
Other	Open†	36.66 to 50
	1	12.5 to 37.5

X = Don't care.

**If a lower clock rate is needed, set DRS = 1 to divide PCLK in half.*

†*If high bandwidth mode is not supported, use BWS = 1.*

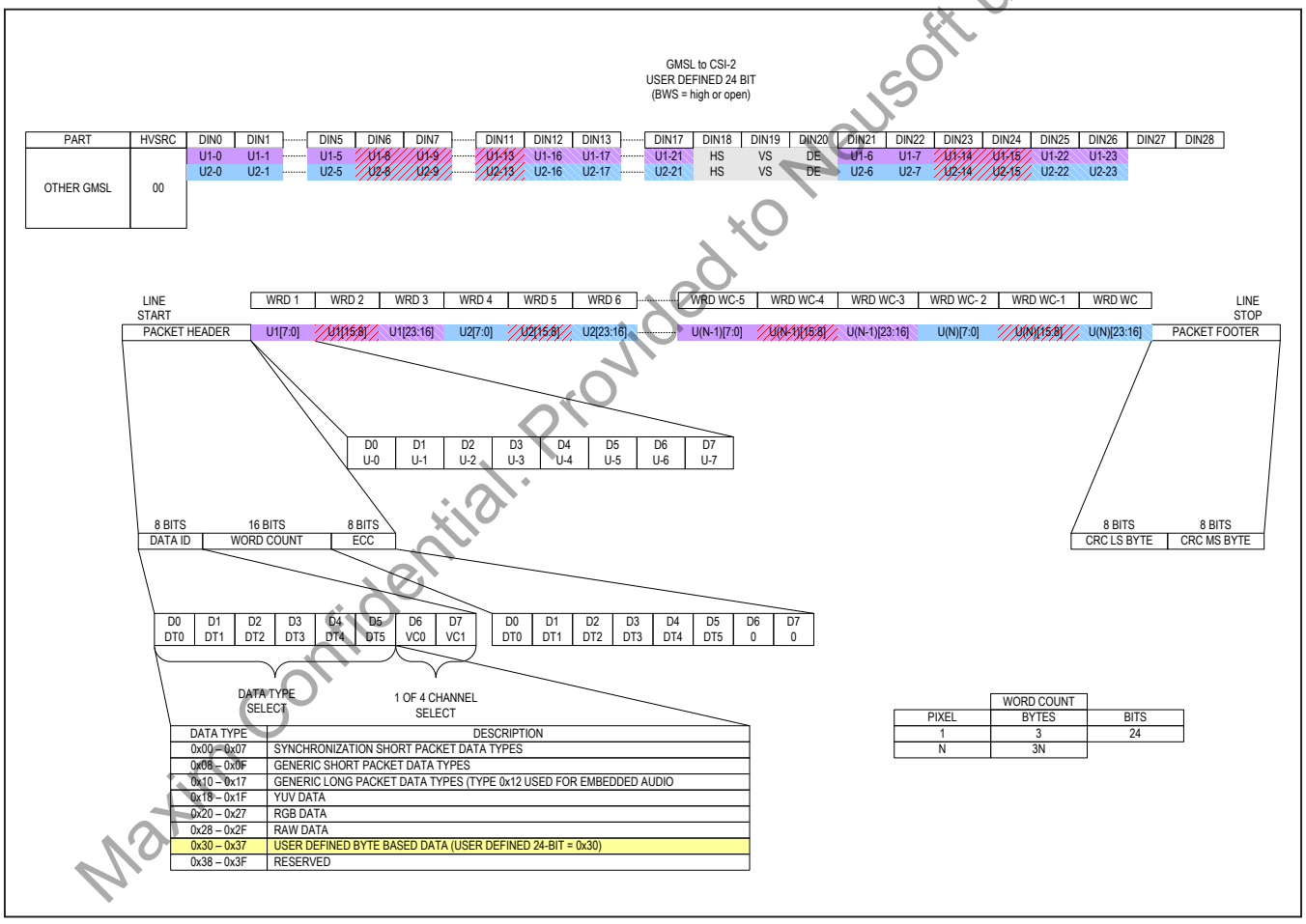


Figure 31. User-Defined 24-Bit Input Map

Supported Data Rates

Two factors limit the available data rate range in the deserializer: the serial link bit rate range of 500Mbps to 1500Mbps per link and the CSI-2 bit rate range of 80Mbps to 1200Mbps per lane. These bit rates relate to the serializer input rate as follows:

$$f_{GMSL} = f_{PCLK} \times \frac{10 \times (3 + BWS) \times (1 + DRS)}{1 + DBL}$$

$$f_{CSI-2} = f_{PCLK} \times \frac{(WIDTH) \times (CHANNELS)}{LANES}$$

where:

f_{GMSL} = Serial link actual bit rate (including overhead)

f_{PCLK} = Serializer input word rate

f_{CSI-2} = CSI-2 output bit rate (per lane)

BWS = BWS pin/bit value (high = 1, low or open = 0)

DRS = DRS pin/bit value (high = 1, low = 0)

DBL = DBL pin/bit value (high = 1, low or not supported = 0)

WIDTH = Pixel format bit width per word shown in Table 19

CHANNELS = Number of input channels used

LANES = Number of CSI-2 Lanes operational

Taking the above two limitations, the available PCLK range (from $f_{PCLKMIN}$ to $f_{PCLKMAX}$) is as follows:

$$f_{PCLKMAX} = \min\left(\left[150 \times \frac{1 + DBL}{(3 + BWS) \times (1 + DRS)}\right], \left[1200 \times \frac{LANES}{(WIDTH) \times (CHANNELS)}\right]\right)$$

$$f_{PCLKMIN(BWS = 0 \text{ OR } 1)} = \max\left(\left[50 \times \frac{1 + DBL}{(3 + BWS) \times (1 + DRS)}\right], \left[80 \times \frac{LANES}{(WIDTH) \times (CHANNELS)}\right]\right)$$

$$f_{PCLKMIN(BWS = OPEN)} = \max\left(\left[36.6 \times \frac{1 + DBL}{1 + DRS}\right], \left[80 \times \frac{LANES}{(WIDTH) \times (CHANNELS)}\right]\right)$$

where:

DBL = DBL pin/bit value (high = 1, low or not supported = 0)

BWS = BWS pin/bit value (high = 1, low or open = 0)

DRS = DRS pin/bit value (high = 1, low = 0)

LANES = Number of CSI-2 lanes operational

WIDTH = Pixel format bit width per word shown in Table 19

CHANNELS = Number of input channels used

Reverse Control Channel

The serializer uses the reverse control channel to receive I²C/UART and GPO signals from the deserializer in the opposite direction of the video stream. The reverse control channel and forward video data coexist on the same serial cable forming a bidirectional link. The reverse control channel operates independently from the forward control channel. The reverse control channel is available 2ms after power-up. The serializer temporarily disables the reverse control channel for 500µs after starting/stopping the forward serial link.

Control Channel and Register Programming

The control channel is available for the µC to send and receive control data over the serial link simultaneously with the high-speed data. The µC controls the link from either the serializer or the deserializer side to support video-display or image-sensing applications. The control channel between the µC and serializer or deserializer runs in base mode or bypass mode according to the mode selection (MS) input of the device connected to the µC. Base mode is a half-duplex control channel and the

Table 19. Data Word Bitwidth

FORMAT	WIDTH
RAW8	8
RAW10	10
RAW12	12
RAW14	14
RAW16*	8
RAW20*	10
RGB565	16
RGB666	18
RGB888	24
USER8	8
USER24	24
YUV8*	8
YUV10*	10
YUV12	24

**Two clocked words per pixel.*

bypass mode is a full-duplex control channel. The total maximum forward or reverse control channel delay is 2µs (UART) or 2-bit times (I^2C) from the input of one device to the output of the other. I^2C delay is measured from a START condition to START condition.

UART Interface

In base mode, the µC is the host and can access the registers of both the serializer and deserializer from either side of the link using the GMSL UART protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the serializer or deserializer, with the UART packets converted to I^2C by the device on the remote side of the link. The µC communicates with a UART peripheral in base mode (through INTTYPE register settings), using the half-duplex default GMSL UART protocol of the serializer/deserializer. The device addresses of the serializer and deserializer in base mode are programmable.

When the peripheral interface is I^2C, the serializer/deserializer converts UART packets to I^2C that have device addresses different from those of the serializer or deserializer. The converted I^2C bit rate is the same as the original UART bit rate.

The deserializer uses differential line coding to send signals over the reverse channel to the serializer. The bit rate of the control channel is 9.6kbps to 1Mbps in both directions. The serializer and deserializer automatically detect the control-channel bit rate in base mode. Packet bit rate changes can be made in steps of up to 3.5 times higher or lower than the previous bit rate. See the *Changing the Clock Frequency* section for more information on changing the control channel bit rate.

Figure 32 shows the UART protocol for writing and reading in base mode between the µC and the serializer/deserializer.

Figure 33 shows the UART data format. Even parity is used. Figure 34 and Figure 35 detail the formats of the SYNC byte (0x79) and the ACK byte (0xC3). The µC and the connected slave chip generate the SYNC byte and ACK byte, respectively. Events such as device wake-up and GPI generate transitions on the control channel that can be ignored by the µC. Data written to the deserializer registers do not take effect until after the acknowledge byte is sent. This allows the µC to verify that write commands are received without error, even if the result of the write command directly affects the serial link. The slave uses the SYNC byte to synchronize with the host UART's data rate. If the GPI or MS inputs of the deserializer toggle while there is control-channel communication, or if a line fault occurs, the control-channel communication will be corrupted. In the event of a missed or delayed acknowledge (~1ms due to control channel timeout), the µC should assume there was an error in the packet transmission or response. In base mode, the µC must keep the UART Tx/Rx lines high no more than four bit-times between bytes in a packet. Keep the UART Tx/Rx lines high for at least 16 bit times before starting to send a new packet.

As shown in Figure 36, the remote-side device converts packets going to or coming from the peripherals from UART format to I^2C format and vice versa. The remote device removes the byte number count and adds or receives the ACK between the data bytes of I^2C. The I^2C bit rate is the same as the UART bit rate.

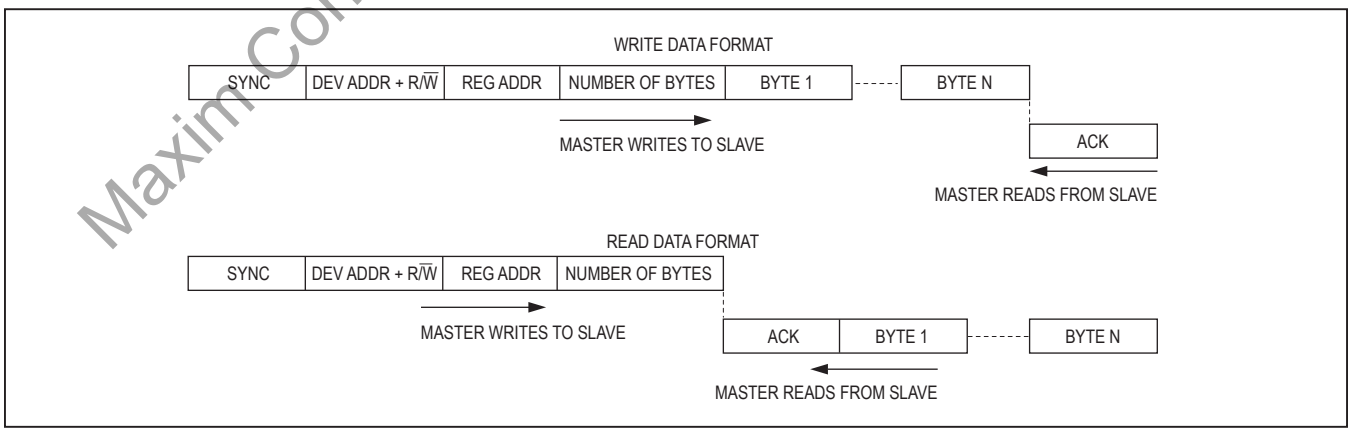


Figure 32. GMSL UART Protocol for Base Mode

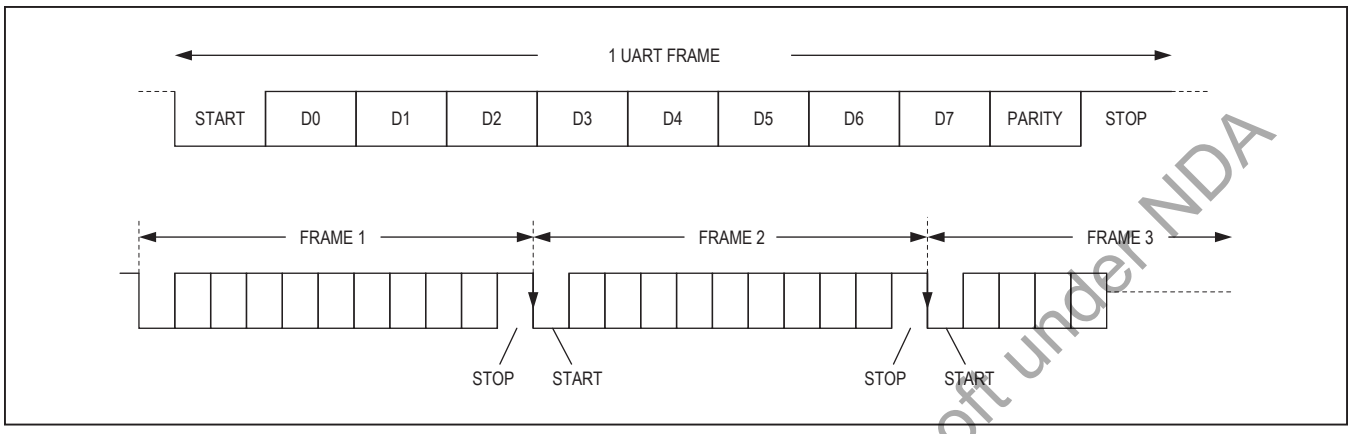


Figure 33. GMSL UART Data Format for Base Mode

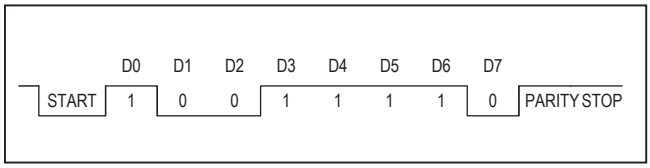


Figure 34. Sync Byte (0x79)

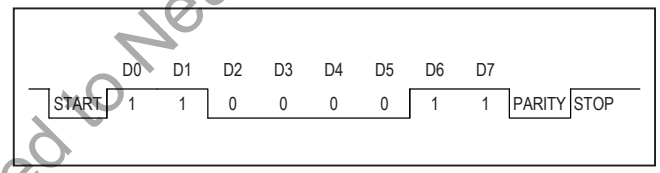


Figure 35. ACK Byte (0xC3)

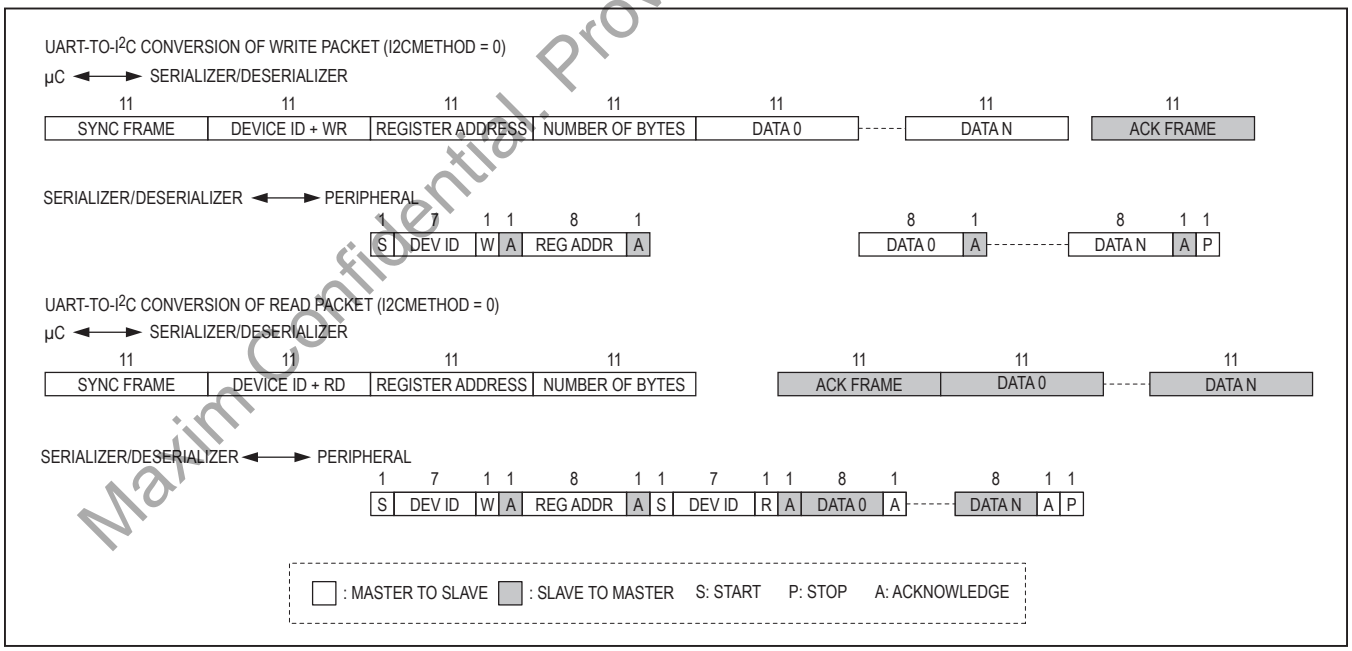


Figure 36. Format Conversion Between GMSL UART and I²C with Register Address (I2CMETHOD = 0)

Interfacing Command-Byte-Only I²C Devices with UART

The deserializer's UART-to-I²C conversion can interface with devices that do not require register addresses, such as the MAX7324 GPIO expander. In this mode, the I²C master ignores the register address byte and directly reads/writes the subsequent data bytes (Figure 37). Change the communication method of the I²C master using the I2CMETHOD bit. I2CMETHOD = 1 sets command-byte-only mode, while I2CMETHOD = 0 sets normal mode where the first byte in the data stream is the register address.

UART Bypass Mode

In bypass mode, the deserializers ignore UART commands from the µC and the µC communicates with the peripherals directly using its own defined UART protocol. The µC cannot access the serializer/deserializer's registers in this mode. Peripherals accessed through the forward control channel using the UART interface need to handle at least one TXCLKOUT period ±10ns of jitter due to the asynchronous sampling of the UART signal by TXCLKOUT. Set MS/HVEN = high to put the control channel into bypass mode. For applications with the µC connected to the deserializer, there is a 1ms wait time between setting MS high and the bypass control channel being active. There is no delay time when switching to bypass mode when the µC is connected to the serializer. Do not send a logic-low value longer than 100µs to ensure proper GPO functionality. Bypass mode accepts bit rates down to 10kbps in either direction. See the *GPO/GPI Control* section for GPI functionality limitations. The control-channel data pattern should not be held low longer than 100µs if GPI control is used.

I²C Interface

In I²C-to-I²C mode, the deserializer's control channel interface sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master and slave(s). A µC master initiates all data transfers to and from the device and generates the SCL clock that synchronizes the data transfer. When an I²C transaction starts on the local side device's control channel port, the remote side device's control channel port becomes an I²C master that interfaces with remote side I²C peripherals. The I²C master must accept clock stretching, which is imposed by the deserializer (holding SCL low) The SDA and SCL lines operate as both an input and an open-drain output. Pullup resistors are required on SDA and SCL. Each transmission consists of a START condition (Figure 6) sent by a master, followed by the device's 7-bit slave address plus a R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP condition.

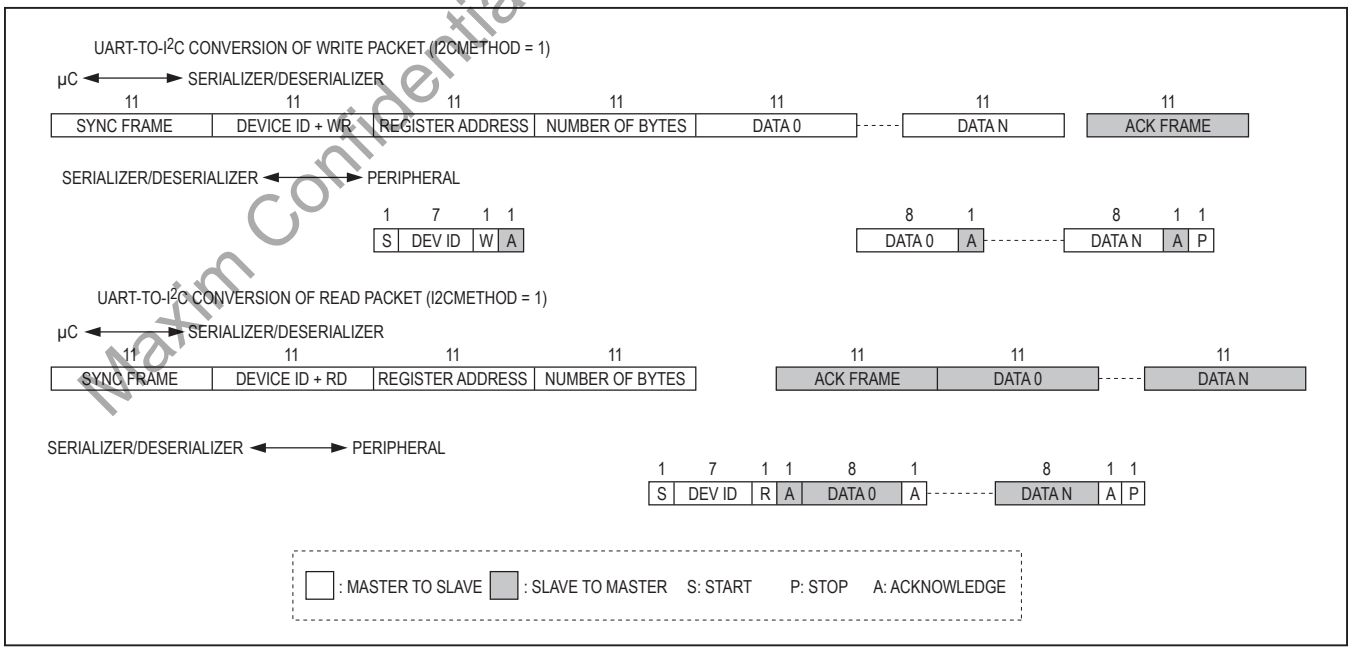


Figure 37. Format Conversion Between GMSL UART and I²C Without Register Address (I2CMETHOD = 1)

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high (see Figure 38). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock pulse (Figure 39). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data (Figure 40). Thus, each byte transferred effectively requires nine bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the slave device, the slave device generates the acknowledge bit because the slave device is the recipient. When the slave device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. The device generates an acknowledge even when the forward control channel is not active. To prevent acknowledge generation when the forward control channel is not active, set the I2CLOCACK bit low.

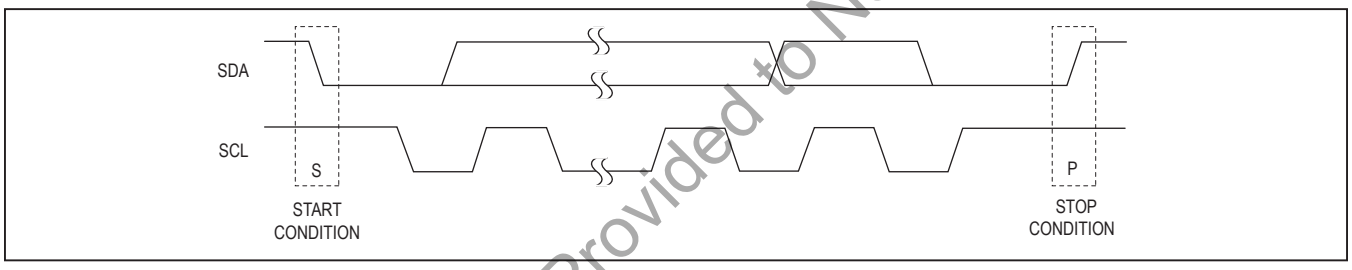


Figure 38. START and STOP Conditions

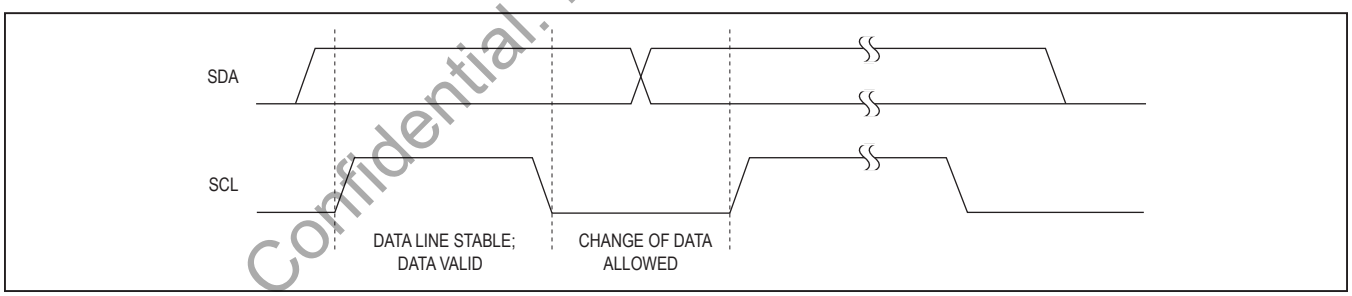


Figure 39. Bit Transfer

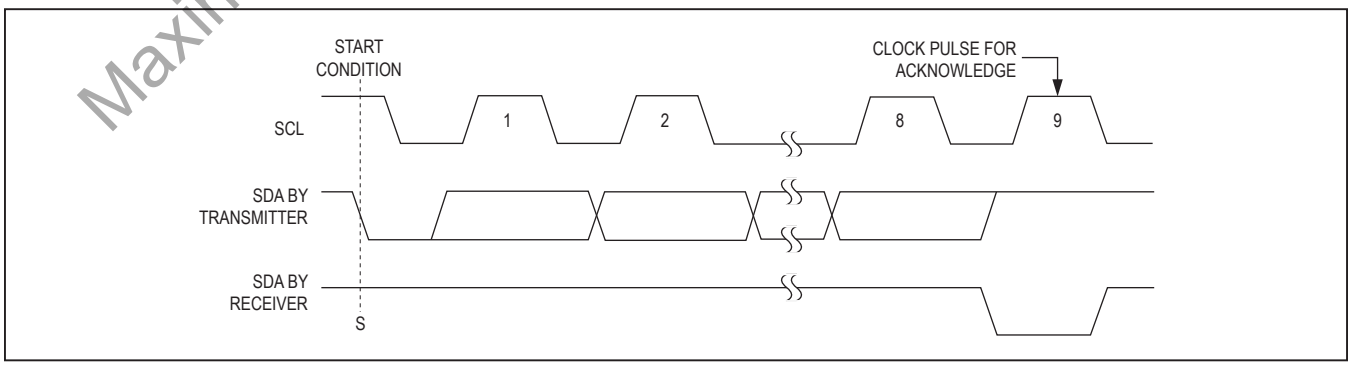


Figure 40. Acknowledge

Slave Address

The deserializers have 7-bit long slave addresses. The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. The slave address for the deserializer is XX01XXX1 for read commands and XX01XXX0 for write commands. See Figure 41.

Bus Reset

The device resets the bus with the I²C START condition for reads. When the R/$\overline{W}$ bit is set to 1, the deserializers transmit data to the master, thus the master is reading from the device.

Format for Writing

Writes to the deserializers comprise the transmission of the slave address with the R/$\overline{W}$ bit set to zero, followed by at least one byte of information. The first byte of information is the register address or command byte. The register address determines which register of the device is to be written by the next byte, if received. If a STOP (P) condition is detected after the register address is received, the device takes no further action beyond storing the register address (Figure 42). Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address, and subsequent data bytes go into subsequent registers (Figure 43). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register addresses autoincrements.

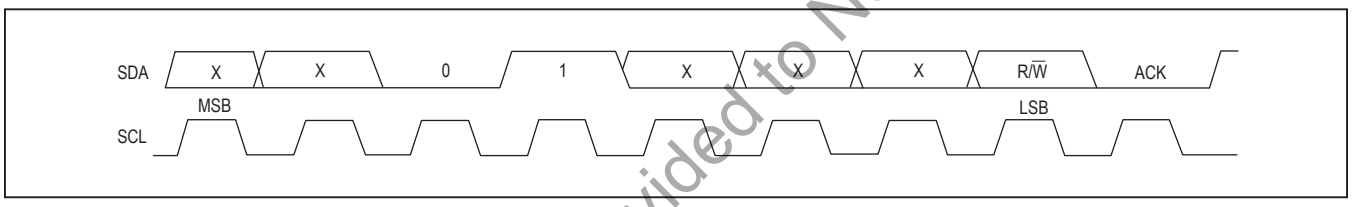


Figure 41. Slave Address

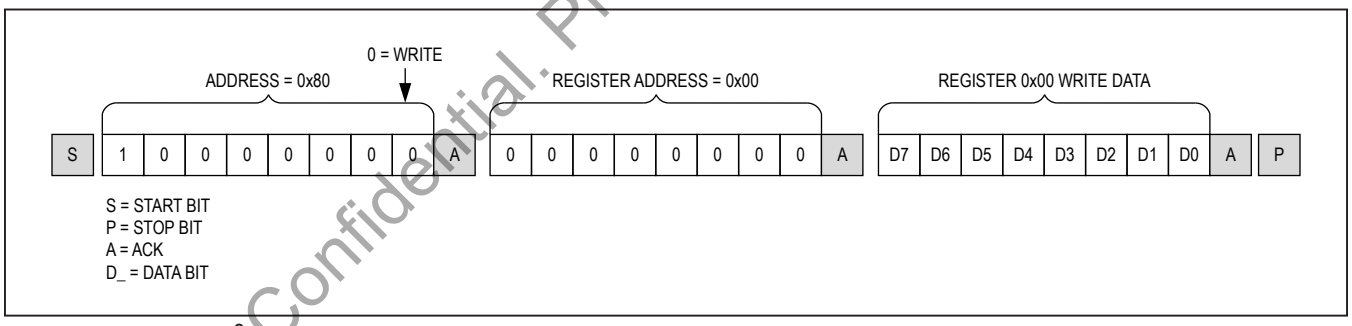


Figure 42. Format for I²C write

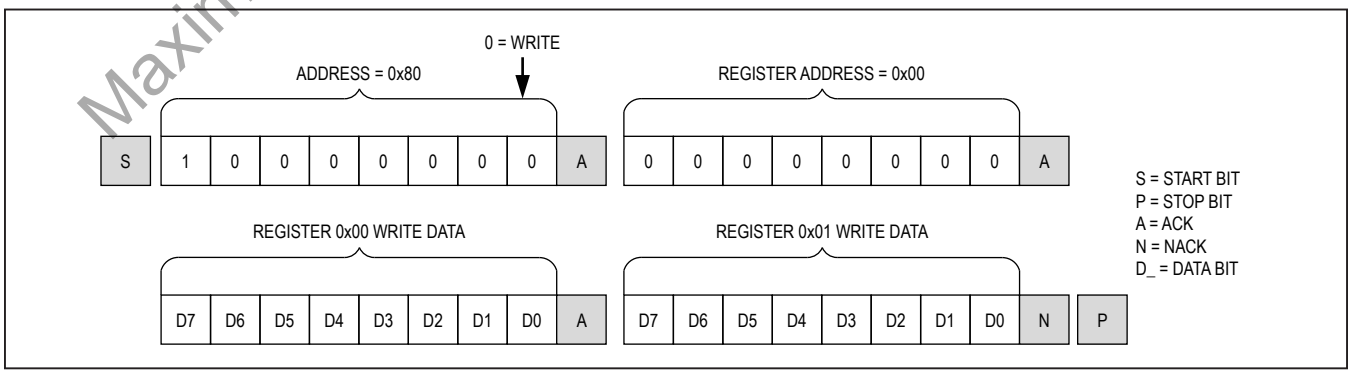


Figure 43. Format for I²C Write to Multiple Registers

Format for Reading

The deserializers are read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the register address by performing a write (Figure 44). The master can now read consecutive bytes from the device, with the first data byte being read from the register address pointed by the previously written register address. Once the master sends a NACK, the device stops sending valid data.

I²C Communication with Remote Side Devices

The deserializers support I²C communication with a peripheral on the remote side of the communication link using SCL clock stretching. While multiple masters can reside on either side of the communication link, arbitration is not provided. The connected masters need to support SCL clock stretching. The remote side I²C bit rate range must be set according to the local side I²C bit rate. Supported remote side bit rates can be found in Table 20. Set the I2CMSTBT (register 0x34) to set the remote I²C bit rate. If using a bit rate different from 400kbps, local and remote side I²C setup and hold times should be adjusted by setting the I2CSLVSH register settings on both sides.

UART/I²C Device Address Translation

GMSL supports UART/I²C device address translation for up to two remote device addresses. Use address translation to assign unique device addresses to remote peripherals with limited UART/I²C addresses. When the µC is connected to the serializer, program the MAX9286 to translate the deserializer (and/or peripheral) addresses. When the µC is connected to the MAX9286, program the serializer(s) to translate the serializer (and/or peripheral) addresses.

In a multilink situation where there are multiple serializers and/or peripheral devices connected to the deserializer, the serializers support broadcast commands to control these multiple devices. Select an unused device address to use as a broadcast device address. Program all the remote side serializer devices to translate the broadcast device address (source address stored in serializer's registers 0x0F, 0x11) to the peripheral's address (destination address stored in serializer's registers 0x10, 0x12). Any commands sent to the broadcast address (selected unused address) will be sent to all deserializers and/or peripheral devices connected to the deserializers whose addresses match the translated broadcast address.

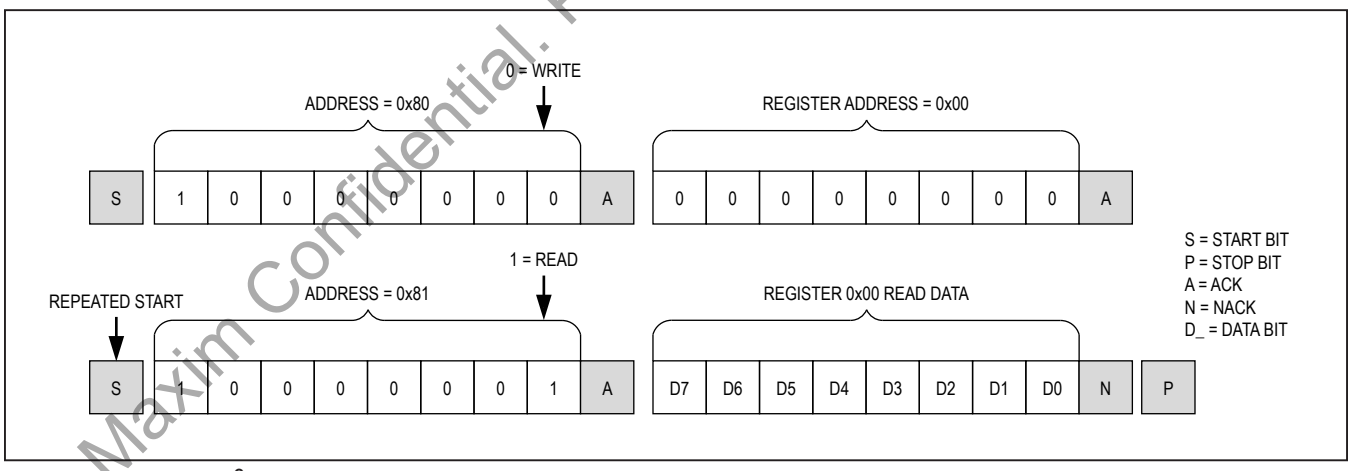


Figure 44. Format for I²C Read

Table 20. I²C Bit Rate Ranges

LOCAL BIT RATE	REMOTE BIT RATE RANGE	I2CMSTBT SETTING
f > 50kbps	Up to 1Mbps	Any
20kbps < f < 50kbps	Up to 400kbps	Up to 110
f < 20kbps	Up to 10kbps	000

Line Equalizers

The deserializer includes line equalizers to compensate cable attenuation at high frequencies. The cable equalizers have 11 selectable levels of compensation from 2.1dB to 13dB (Table 21). Each link boost setting can be individually set to account for differing lengths and cable types. Use equalization in the deserializer, together with preemphasis in the serializer, to create the most reliable link for any given cable. The device powers up with the equalization disabled.

HS/DE Tracking

The deserializer has tracking to filter out HS bit or packet errors. Set/clear HSTRACK (D3 of register 0x0D) to enable/disable HS/DE tracking.

Cable Type Configuration

The device can receive serial data from two kinds of cable: 100Ω twisted pair and 50Ω coax. (Contact the factory for devices compatible with 75Ω cables). CX/TP determine the power-up state of the serial input. CX/TP = high selects coax mode, while CX/TP = low selects twisted pair mode. After power up, set the CXTP_ bits to select coax or twisted pair mode. CXSEL_ selects whether the IN_+ or IN_- port is used in coax mode. To simplify signal routing requirements, SWITCHIN_ can swap the IN_+ and IN_- inputs to accommodate various connector orientations.

High-Immunity Reverse Control Channel Mode

The deserializer contains a high-immunity reverse control channel mode, which has increased robustness at half the bit rate over the standard GMSL reverse control channel link (Table 22). Set HIM = high on the serializer and deserializer to use high-immunity mode at power-up. Set the HIGHIMM bit high in both the serializer and deserializer to enable high-immunity mode at any time after power-up. Set the HIGHIMM bit low in both the serializer and deserializer to use the legacy reverse control channel mode. The deserializer reverse channel mode is not available for 500µs/1.92ms after the reverse control channel mode is changed through the serializer/deserializer's HIGHIMM bit setting, respectively. The user must set HIM and GPO/HIM or the HIGHIMM bits to the same value for proper reverse control channel communication.

In high-immunity mode, Set HPFTUNE = 00 in the equalizer, if the serial bit rate = [TXCLKOUT x 30 (BWS = low or open) or 40 (BWS = high)] is larger than 1Gbps when BWS is low or high. In addition, use 47nF AC-coupling capacitors. Note that legacy reverse-control channel mode may not function when using 47nF AC-coupling capacitors.

By default, high-immunity mode has a 500kbps max bitrate. Set REVFAST = 1 in both devices to use a 1Mbps bit rate. Fast high-immunity mode requires 24 or 32-bit mode (BWS = low, high) and a serial data rate greater than 1.25Gbps.

Table 21. Cable Equalizer Boost Levels

BOOST SETTING (REGISTER 0x32, 0x33)	TYPICAL BOOST GAIN (dB)
0000	2.1
0001	2.8
0010	3.4
0011	4.2
0100	5.2
0101	6.2
0110	7
0111	8.2
1000	9.4
1001	10.7 **Power-up default***
1010	11.7
1011	13

**The equalizer is disabled at power-up.*

Table 22. Reverse Control Channel Modes

HIGHIMM BIT OR HIM PIN SETTING	REVFAST BIT	REVERSE CONTROL CHANNEL MODE	MAX UART/I²C BIT RATE (kbps)
LOW (0)	X	Legacy reverse control channel mode (compatible with all GMSL devices)	1000
HIGH (1)	0	High-immunity mode	500
	1	Fast high-immunity mode (requires BWS = low or high, serial data rate >1.25Gbps)	1000

X = Don't care.

Sleep Mode

The deserializer has a sleep mode to reduce power consumption. The devices enter or exit sleep mode by a command from a µC using the control channel. Set the SLEEP bit to 1 to initiate sleep mode. The deserializer sleeps after serial link inactivity or 8ms (whichever arrives first) after setting its SLEEP = 1. See the *Link Startup Procedure* section for details on waking up the device for different µC and starting conditions.

To wake up from the local side, send an arbitrary control channel command to deserializer, wait for 5ms for the chip to power up and then write 0 to SLEEP register bit to make the wake-up permanent. To wake up from the remote side, enable serialization. The deserializer will detect the activity on serial link and then when it locks, it will automatically set its SLEEP register bit to 0.

Power-Down Mode

The deserializers have a power-down mode that further reduces power consumption compared to sleep mode. Set $\overline{PWDN}$ low to enter power-down mode. In power-down, the CMOS outputs remain high impedance. Entering power-down resets the device's registers. Upon exiting power-down, the state of external pins ADD[2:0], CX/TP, I2CSEL, HIM, and BWS are latched.

Frame Sync

The GPI/GPO provide a simple solution for camera applications that require a frame sync signal from the ECU (e.g. surround view systems). Connect each serializer's GPO output to the camera frame sync input. Frame sync timing can be generated internally, or supplied by the ECU.

Internal Frame Sync (FSYNCMODE = 0X)

When the deserializer generates the frame sync signals, it can run in one of three modes: manual, automatic, and semi-automatic.

- Manual Mode (FSYNCMETH = 00)

  FSYNCPERIOD bits (registers 0x06 to 0x08) manually set the frame sync period. Manual mode allows a frame sync period up to 2^{24} PCLK cycles (~16.8 million).

- Automatic Mode (FSYNCMETH = 1X) (Figure 45)

  The deserializer sends frame sync after counting VSYNC pulses (determined by FSYNCPERDIV) on the slowest link (auto mode) or master link (semi-auto mode). After the last VSYNC pulse, and timing margins adjustments (set by KVAL and PVAL), the deserializer sends frame sync. FSYNC is locked when all VSYNCs are aligned (within the margin DIFF) and FSYNC occurs within the timing margin (KVAL, PVAL) for two consecutive VSYNC cycles. PVAL is specified in PCLK cycles while KVAL is specified in absolute time units.

- Semi-Automatic Mode (FSYNCMETH = 01)

  The device operates similar to automatic mode with the following differences: The deserializer does not check the skew between different serial links (DIFF). Timing margins adjustments (KVAL, PVAL) are measured from the master link (as opposed to the slowest link).

Frame sync generation requires an active-high VSYNC. If active-low VSYNC is used, set the INVVSYNC in the serializer and deserializer to invert the incoming and outgoing VSYNC signal.

External Frame Sync (FSYNCMODE = 1X)

When set for External frame sync, all frame sync timing comes from the FSYNC/GPI pin. Connect the ECU Frame Sync signal to GPI. When FSYNCMODE = 10, Any transition on FSYNC/GPI triggers a frame sync packet.

GPO/GPI Control

When not used for frame synchronization, GPO on the serializers follow GPI transitions on the deserializer. The GPI to GPO delay is 0.35ms max. Keep time between GPI transitions to a minimum 0.35ms. Bit D6 of register 0x27 in the deserializer stores the GPI input state. GPO is low after power-up. The µC can also set GPO by writing to the SETGPO register bit. Do not send a logic-low value on the deserializer RX/SDA input (UART mode) longer than 100µs in either base or bypass mode to ensure proper GPO/GPI functionality.

Configuration Link

The control channel can operate in a low-speed mode called configuration link in the absence of a clock input. This allows a microprocessor to program configuration registers before starting the video link. An internal oscillator provides the clock for the configuration link. Set CLINKEN = 1 on the serializer to enable configuration link. Configuration link is active until the video link is enabled. The video link overrides the configuration link and attempts to lock when SEREN = 1.

Link Masking

When link masking is enabled (MASKLINK_ = 1) the deserializer ignores all input on the respective serial link. Frame and line synchronization is derived from all other unmasked links. Masking a link keeps the frame combiner running when the input data is corrupted or missing by

replacing the corrupted frame with a blank screen (disabling the link causes the link to disappear, altering the frame size) set AUTOMASKEN bit high to automatically mask links if a video link is lost. Set AUTOCOMBACKEN to unmask a link when a video link is reestablished.

Link Startup Procedure

Table 23 lists the startup procedure. The control channel is available after the video link or the configuration link is established. If the deserializer powers up after the serializer, the control channel becomes unavailable for 2ms after power-up.

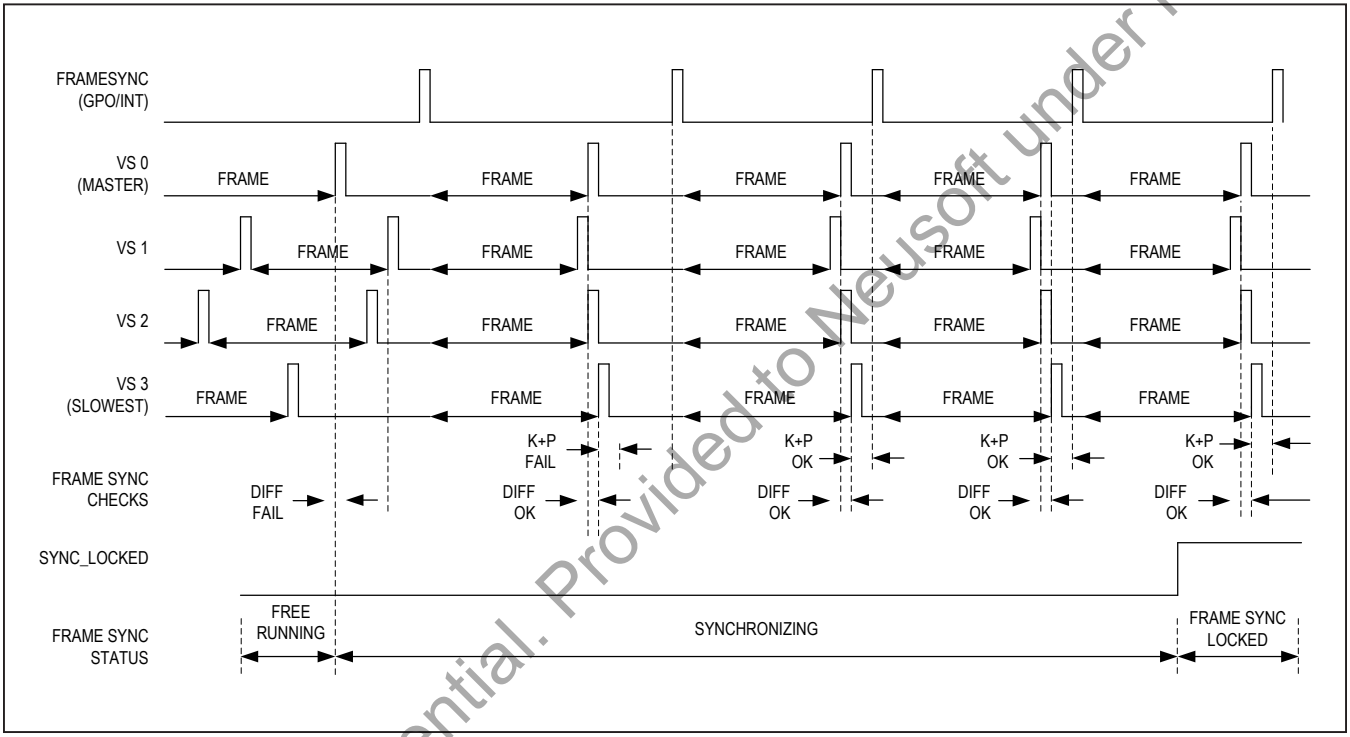


Figure 45. Example Frame Sync Operation (Automatic Mode)

Table 23. Startup Procedure (see Figure 46)

NO.	µC	SERIALIZERS		DESERIALIZER
		(AUTOSTART ENABLED)	(AUTOSTART DISABLED)	
—	µC connected to deserializer.	Set all configuration inputs	Set all configuration inputs	Set all configuration inputs
1	Powers up.	Powers up and loads default settings. Establishes video link when valid PCLK available.	Powers up and loads default settings. Goes to sleep after 8ms.	Powers up and loads default settings. Locks to video link signal if available.
2	Set FWDCCEN_ and REVCCEN_ bits to Enable control channel of link zero only. Waits ~5m for serial link to be established if autostart enabled (LOCK = 1).			Enables link 0 only.

Table 23. Startup Procedure (see Figure 46) (continued)

NO.	µC	SERIALIZERS		DESERIALIZER
		(AUTOSTART ENABLED)	(AUTOSTART DISABLED)	
2a	If serializer is asleep (autostart disabled), wakes up the serializer by sending dummy packet, then writing SLEEP = 0 after 5 to 8ms. May not get an acknowledge (or gets a dummy acknowledge) if not locked.		Serializer 0 wakes up.	Forwards commands from µC to serializer 0.
3	Set SEREN = 0 and CLINKEN = 1 to disable the video channel and enable the control channel. May not get an acknowledge (or gets a dummy acknowledge). Waits ~5m for configuration link to be established.	Serialzer 0 switches to control channel mode.		Forwards commands from µC to serializer 0. Link 0 locks to control channel.
4	Change serializer 0 device address to unique address. Setup address translation (camera/peripherals, and broadcast) for serializer 0.	Serializer 0 configuration changed from default settings.		Forwards commands from µC to serializer 0.
5	Repeat steps 2 to 4 with the other links.	All serializers awake, device addresses set.		Enables links individually and forwards commands from µC.
6	Set all FWDCCEN_ and REVCCEN_ bits = 1 to Enable control channel of all links. Waits ~5m for configuration links to be established.			Enables all links.
7	Writes rest of serializer/deserializer configuration bits. Bits that need to be set on both sides of the link (EDC, BWS, etc.) should be set in the serializer first.	Configuration changed from default settings		Forwards commands from µC to serializers. Configuration changed from default settings.
8	Writes camera/peripheral configuration bits.	Forwards commands from serializers to cameras/ peripherals.		Forwards commands from µC to serializers
9	When valid PCLK available, sets SEREN = 1 to serializers. Gets an acknowledge and waits~5m for all serial links to be established (LOCK = 1).	Establishes video link.		Locks to video link signals.
9a	If not already enabled, Send commands to cameras to begin sending video data.	Serializes video data. Forwards frame sync commands from deserializer to cameras.		Deserializes video data. Sends frame sync command to serializers.
10	Wait ~6 VSYNC cycles for cameras to synchronize (FSYNCLOCKED = 1).			Combines incoming video streams into a single video output.
11	Sets CSIOUTEN = 1 to enable CSI-2 output.			Outputs video data on CSI-2 outputs.

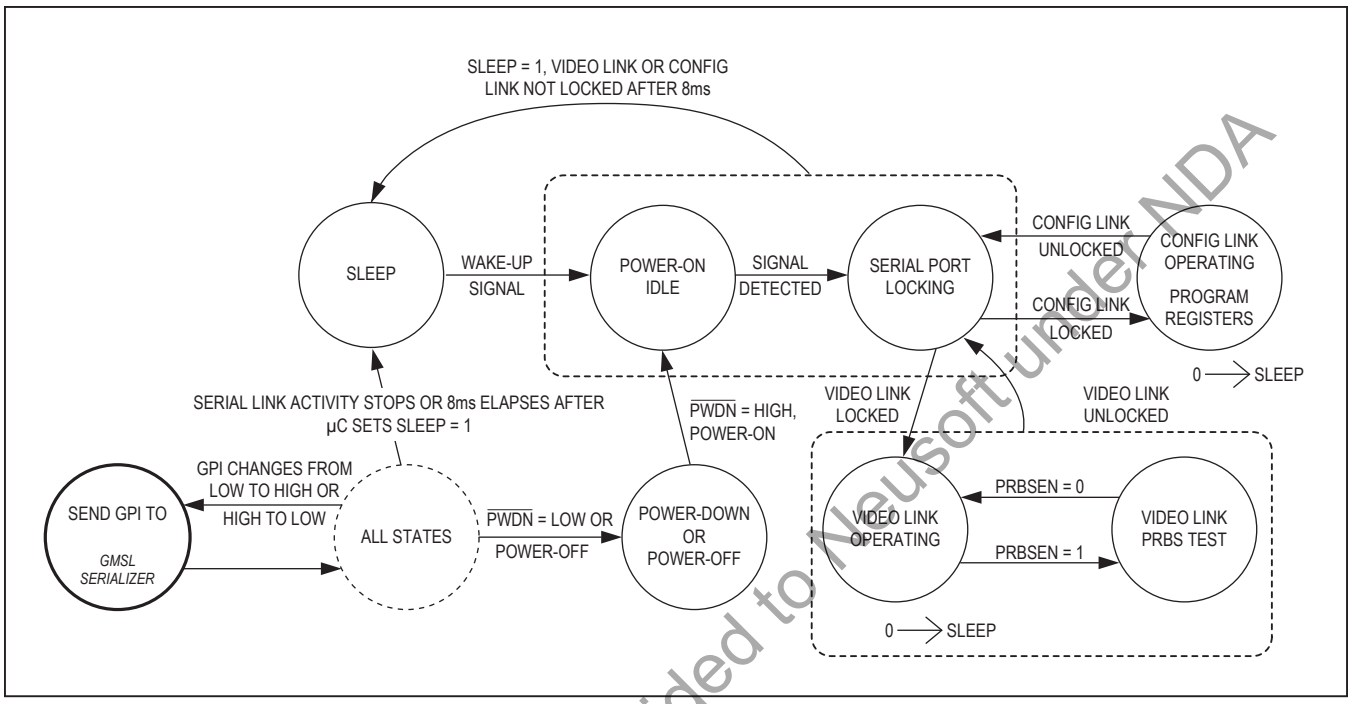


Figure 46. State Diagram

Applications Information

Self-PRBS Test

The serializers include a PRBS pattern generator that works with bit-error verification in the deserializer. Before running the PRBS test, first set ENHSFILT and ENVSFILT, to 0, to disable glitch filtering in the deserializer. For MAX9271-MAX9273 serializers set PRBSEN_ = 1 in the deserializer and then set PRBSEN = 1 (0x04, D5) in the serializer. For all other GMSL serializers, set PRBSTYPE = 0 in the deserializer. Then set PRBSEN = 1 (0x04, D5) in the serializer and then set PRBSEN_ = 1 in the deserializer.

For the MAX9271-MAX9273 set PRBSEN = 0 (0x04, D5) in the serializer to exit the PRBS test. For all other GMSL serializers, set PRBSEN_ = 0 (0x0E, D4) in the deserializer and then set PRBSEN = 0 (0x04, D5) in the serializer. to exit the PRBS test.

Error Checking

The deserializer checks each serial link for errors and stores the number of detected and corrected errors in the 8-bit registers, DETERR_ (0x28–0x2B) and CORRERR (0x2C–0x2F). If a large number of 8b/10b errors are detected on a serial link within a short duration (error rate = 1/4), the deserializer loses that serial link's lock and stops the error counter. The deserializer then attempts to relock to the serial data. DETERR_ and CORRERR_ reset upon successful video link lock, successful readout of their respective registers (through µC), or whenever autoerror reset is enabled. The deserializer uses a separate PRBS register during the internal PRBS test, and DETERR_ and CORRERR_ are reset to 0x00.

$\overline{\text{ERR}}$ Output

The deserializer has an open-drain $\overline{\text{ERR}}$ output. This output asserts low whenever the number of detected/corrected errors exceeds the error thresholds during normal operation, or when at least 1 PRBS error is detected during PRBS test. $\overline{\text{ERR}}$ reasserts high whenever DETERR_ and CORRERR_ resets, due to DETERR/CORRERR readout, video link lock, or auto error reset.

Auto Error Reset

The default method to reset errors is to read the respective error registers in the deserializers (0x028–0x2F). Auto error reset clears the error counters DETERR_, CORERR_, and the $\overline{\text{ERR}}$ output ~1µs after $\overline{\text{ERR}}$ goes low. Auto error reset is disabled on power-up. Enable auto error reset through AUTORST (0x0F, D5). Auto error reset does not run when the device is in PRBS test mode.

Changing the Clock Frequency

It is recommended that the serial link be enabled after the video clock (f_{PCLK}) and the control-channel clock (f_{UART}/f_{I2C}) are stable. When changing the clock frequency, stop the video clock for 5µs, apply the clock at the new frequency, then restart the serial link or toggle SEREN. On-the-fly changes in clock frequency are possible if the new frequency is immediately stable and without glitches. The reverse control channel remains unavailable for 500µs after serial link start or stop. When using the UART interface, limit on-the-fly changes in f_{UART} to factors of less than 3.5 at a time to ensure that the device recognizes the UART sync pattern. For example, when lowering the UART frequency from 1Mbps to 100kbps, first send data at 333kbps and then at 100kbps for reduction ratios of 3 and 3.333, respectively.

Software Programming of the Device Addresses

The serializers and deserializers have programmable device addresses. This allows multiple GMSL devices, along with I²C peripherals, to coexist on the same control channel. The serializer device address is in register 0x00 of the serializer, while the deserializer device address is in register 0x01 of the serializer and register 0x09 of the MAX9286. To change a device address, write to register 0x00 of the serializer for serializer device address change, or register 0x09 of the deserializer for deserializer device address change. When changing the deserialzer address, write the same address into register 0x01 of the serializers). When changing the serializer address, use the FWDCCEN_ and REVCCEN_ bits (register 0x0A) to select individual serializers.

3-Level Configuration Inputs

ADD[1:0] are 3-level inputs that control the serial interface configuration and power-up defaults. Connect 3-level inputs through a pullup resistor to IOVDD to set a high level, a pulldown resistor to GND to set a low level, or open to set a mid level. For digital control, use three-state logic to drive the 3-level logic input.

Configuration Blocking

The deserializers can block changes to registers. Set CFGBLOCK to make all registers read only. Once set, the registers remain blocked until the supplies are removed or until $\overline{PWDN}$ is low.

Compatibility with Other GMSL Devices

The deserializers are designed to pair with the MAX9271–MAX9281 serializers but interoperates with any GMSL serializers. See Table 24 for operating limitations

HS/VS Inversion

The deserializer uses an active-high HS and VS for HS/VS encoding and GMSL to CSI-2 conversion. Set INVHSYNC, and INVVSYNC the serializers and deserializers to invert active-low signals for use with the GMSL devices.

GPIOs

The deserializers have two open-drain GPIOs available, GPIO1OUT and GPIO0OUT (0x0F, D[1:0]) set the output state of the GPIOs. Setting the GPIO output bits to ‘0’ low pulls the output low, while setting the bits to 1 leaves the output undriven, and pulled high through internal/external pullup resistors. The GPIO input buffers are always enabled. The input states are stored in GPIO1 and GPIO0 (0x27, D[5:4]). Set GPIO1OUT/GPIO0OUT to 1 when using GPIO1/GPIO0 as an input.

Internal Input Pulldowns

The control and configuration inputs (except 3-level inputs) include a pulldown resistor to GND. External pulldown resistors are not needed.

Table 24. MAX9286 Feature Compatibility

MAX9286 FEATURE	GMSL SERIALIZER
HSYNC/VSYNC encoding	Do not use if feature is not supported in the serializer.
I²C to I²C	If feature not supported in serializer, must use UART to I²C or UART to UART.
Coax	If feature not supported in serializer, must connect unused serial input through 200nF and 50Ω in series to V_{DD} and set the reverse control channel amplitude to 100mV.
High-immunity control channel	If feature not supported in serializer, must use the legacy reverse control channel mode.
High-bandwidth mode	If feature not supported in serializer, must use 24-bit or 32-bit mode.
Error correction/detection	If feature not supported in serializer, must use default parity error detection only.

Choosing I²C/UART Pullup Resistors

I²C and UART open-drain lines require a pullup resistor to provide a logic-high level. There are tradeoffs between power dissipation and speed, and a compromise may be required when choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. I²C specifies 300ns rise times (30% to 70%) for fast mode, which is defined for data rates up to 400kbps (see the I²C specifications in the *AC Electrical Characteristics* table for details). To meet the fast-mode rise-time requirement, choose the pullup resistors so that rise time t_R = 0.85 x R_{PULLUP} x C_{BUS} < 300ns. The waveforms are not recognized if the transition time becomes too slow. The device supports I²C/UART rates up to 1Mbps.

AC-Coupling

AC-coupling isolates the receiver from DC voltages up to the voltage rating of the capacitor. Capacitors at the serializer output and at the deserializer input are needed for proper link operation and to provide protection if either end of the cable is shorted to a battery. AC-coupling blocks low-frequency ground shifts and low-frequency common-mode noise.

Selection of AC-Coupling Capacitors

Voltage droop and the digital sum variation (DSV) of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is fixed, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level. The RC network for an AC-coupled link consists of the CML/coax receiver termination resistor (R_{TR}), the CML/coax driver termination resistor (R_{TD}), and the series AC-coupling capacitors (C). The RC time constant for four equal-value series capacitors is (C x (R_{TD} + R_{TR}))/4. R_{TD} and R_{TR} are required to match the transmission line impedance (usually 100Ω differential, 50Ω single ended). This leaves the capacitor selection to change the system time constant. Use at least 0.22µF (using legacy reverse control channel), 47nF (using high-immunity reverse control channel), or larger high-frequency surface-mount ceramic capacitors, with sufficient voltage rating to withstand a short to battery, to pass the lower speed reverse control-channel signal. Use capacitors with a case size less than 3.2mm x 1.6mm to have lower parasitic effects to the high-speed signal.

Selection of Camera Frequency References

To ensure proper operation, the reference frequencies of the cameras should be within a 100ppm tolerance, to reduce the drift between frame sync signals. The frame combiner can handle a skew of up to 2 horizontal lines between cameras. Table 25 lists some common sensors and configurations.

Power-Supply Circuits and Bypassing

The deserializers use an V_{AVDD}, V_{DVDD}, and V_{MAVDD} of 1.7V to 1.9V. All single-ended inputs and outputs except for the serial input derive power from an IOVDD of 1.7V to 3.6V, which scale with IOVDD. Proper voltage-supply bypassing is essential for high-frequency circuit stability.

Cables and Connectors

Interconnect for CML and MIPI typically have a differential impedance of 100Ω. Use cables and connectors

Table 25. Suggested Sensor Configurations for GMSL

SENSOR	CONFIGURATION
OV10635	30Hz, 1280x800p (1905 x 840 with blanking), 10-bit YUV, 96MHz
OV10640	30Hz, 1280 x 1080p (1476 x 1106 with blanking), 12-bit RAW/12-bit HDR, 75MHz
	60Hz, 1280 x 1080p (1476 x 1106 with blanking), 12-bit RAW, 100MHz
AR0132	45Hz, 1280 x 960p (1650 x 990) with blanking, 12-bit RAW data type, 74.25MHz

that have matched differential impedance to minimize impedance discontinuities. Coax cables typically have a characteristic impedance of 50Ω, (contact the factory for 75Ω operation). Table 26 lists the suggested cables and connectors used in the GMSL link.

Board Layout

Separate LVCMOS logic signals MIPI, and CML/coax high-speed signals to prevent crosstalk. Use a four-layer PCB with separate layers for power, ground, CML/coax, and MIPI/LVCMOS logic signals. Layout PCB traces close to each other for a 100Ω differential characteristic impedance for STP. The trace dimensions depend on the type of trace used (microstrip or stripline). Note that two 50Ω PCB traces do not have 100Ω differential impedance when brought close together—the impedance goes down when the traces are brought closer. Use a 50Ω trace for the single-ended output when driving coax. Route the PCB traces for differential CML channel in parallel to maintain the differential characteristic impedance.

Avoid vias. Keep PCB traces that make up a differential pair equal length to avoid skew within the differential pair.

ESD Protection

ESD tolerance is rated for Human Body Model, IEC 61000-4-2, and ISO 10605. The ISO 10605 and IEC 61000-4-2 standards specify ESD tolerance for electronic systems. The serial link inputs are rated for ISO 10605 ESD protection and IEC 61000-4-2 ESD protection. All pins are tested for the Human Body Model. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 47). The IEC 61000-4-2 discharge components are C_S = 150pF and R_D = 330Ω (Figure 48). The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 49).

Table 26. Suggested Connectors and Cables for GMSL

VENDOR	CONNECTOR	CABLE	TYPE
Rosenberger	59S2AX-400A5-Y	RG174	Coax
Rosenberger	D4S10A-40ML5-Z	Dacar 538	STP
Nissei	GT11L-2S	F-2WME AWG28	STP
JAE	MX38-FF	A-BW-Lxxxxx	STP

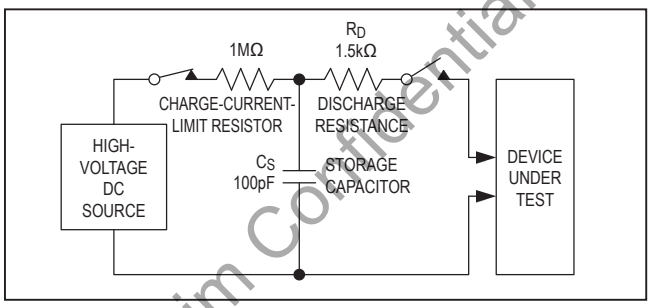


Figure 47. Human Body Model ESD Test Circuit

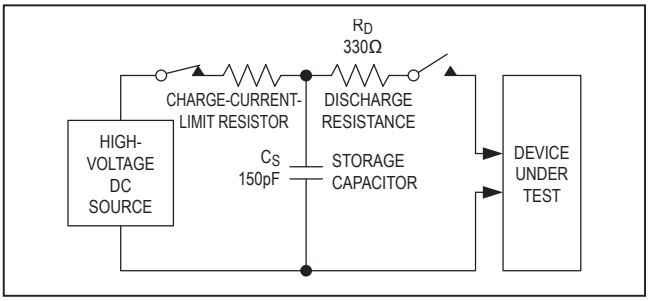


Figure 48. IEC 61000-4-2 Contact Discharge ESD Test Circuit

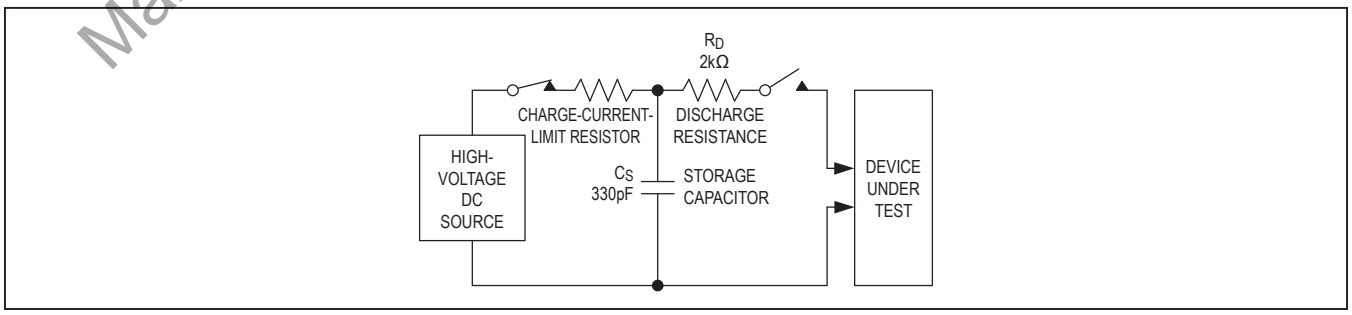


Figure 49. ISO 10605 Contact Discharge ESD Test Circuit

Table 27. Register Table

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x00	D[7:5]	MSTLINKSEL	000	Use link 0 for CSI clock source	111
			001	Use link 1 for CSI clock source	
			010	Use link 2 for CSI clock source	
			011	Use link 3 for CSI clock source	
			1XX	Auto detect link used for CSI clock source	
	D4	EN_VS_GEN	0	Disable Internal VSYNC generation (VSYNC comes from camera)	0
			1	Enable Internal VS generation (when FSYNCMODE not set to 11)	
	D3	LINKEN3	0	Disable input link 3 (IN3+, IN3-)	1
			1	Enable input link 3 (IN3+, IN3-)	
	D2	LINKEN2	0	Disable input link 2 (IN2+, IN2-)	1
			1	Enable input link 2 (IN2+, IN2-)	
	D1	LINKEN1	0	Disable input link 1 (IN1+, IN1-)	1
			1	Enable input link 1 (IN1+, IN1-)	
	D0	LINKEN0	0	Disable input link 0 (IN0+, IN0-)	1
			1	Enable input link 0 (IN0+, IN0-)	
0x01	D[7:6]	FSYNCMODE	00	Internally generate frame sync, FSYNC/GPI is high impedance	00
			01	Internally generate frame sync, FSYNC/GPI outputs frame sync	
			10	Receive external frame sync from another MAX9286. FSYNC/GPI is external frame sync input	
			11	Receive external frame sync from ECU. FSYNC/GPI is a general purpose input	
	D5	GPIEN*	0	Disable GPI-to-GPO transmission	1
			1	Enable GPI-to-GPO transmission (when FSYNCMODE = 0x11)	
	D[4:3]	—	00	Reserved	00
	D2	ENLMO RSTFSYNC	0	Line memory overflow does not reset frame synchronization	0
			1	Line memory overflow resets frame synchronization	
	D[1:0]	FSYNCMETH	00	Internal frame sync uses manual mode (when FSYNCMODE = 0X)	10
			01	Internal frames sync uses semi-automatic mode (when FSYNCMODE = 0X)	
			1X	Internal frame sync uses automatic mode (when FSYNCMODE = 0X)	

Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x02	D[7:4]	FSYNC PERDIV	0000	Frame sync transmission period is 1 VSYNC period	0000
			0001	Frame sync period is 2 VSYNC periods	
			0010	Frame sync period is 4 VSYNC periods	
			0011	Frame sync period is 6 VSYNC periods	
			0100	Frame sync period is 8 VSYNC periods	
			0101	Frame sync period is 10 VSYNC periods	
			0110	Frame sync period is 12 VSYNC periods	
			0111	Frame sync period is 16 VSYNC periods	
			1000	Frame sync period is 20 VSYNC periods	
			1001	Frame sync period is 24 VSYNC periods	
			1010	Frame sync period is 32 VSYNC periods	
			1011	Frame sync period is 48 VSYNC periods	
			1100	Frame sync period is 64 VSYNC periods	
			1101	Frame sync period is 80 VSYNC periods	
			1110	Frame sync period is 96 VSYNC periods	
			1111	Frame sync period is 128 VSYNC periods	
	D[3:0]	—	0000	Reserved	0000
0x03	D[7:5]	—	000	Reserved	000
	D4	KVALSIGN	0	Positive KVAL value	0
			1	Negative KVAL value	
	D[3:0]	KVAL	0000	1µs desired margin with respect to rising edge of VSYNC of the master link (semi-auto mode) or the slowest link (auto mode)	0001
			0001	2µs desired margin	
			0010	3µs desired margin	
			0011	4µs desired margin	
			0100	5µs desired margin	
			0101	6µs desired margin	
			0110	7µs desired margin	
			0111	8µs desired margin	
			1000	10µs desired margin	
			1001	12µs desired margin	
			1010	14µs desired margin	
			1011	16µs desired margin	
			1100	20µs desired margin	
			1101	24µs desired margin	
			1110	28µs desired margin	
			1111	32µs desired margin	
0x04	D[7:0]	PVALL	XXXXXXXX	Low byte of desired margin (in PCLK cycles) with respect to rising edge of VSYNC of the master link (semi-auto mode) or the slowest link (auto mode)	00000000

Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x05	D[7:6]	—	00	Reserved	00
	D5	PVALSIGN	0	Positive desired margin value (PVAL)	0
			1	Negative desired margin (PVAL)	
	D[4:0]	PVALH	XXXXXXX	High byte of desired margin (in PCLK cycles) with respect to rising edge of VSYNC of the master link (semi-auto mode) or the slowest link (auto mode)	00000
0x06	D[7:0]	FSYNC PERIODL*	XXXXXXXX	Manual mode low byte of internally generated frame sync period in terms of PCLK cycles (effective when FSYNCMETH = 00 and FSYNCMODE = 0X)	00000000
0x07	D[7:0]	FSYNC PERIODM*	XXXXXXXX	Manual mode middle byte of internally generated frame sync period in terms of PCLK cycles (effective when FSYNCMETH = 00 and FSYNCMODE = 0X)	00000000
0x08	D[7:0]	FSYNC PERIODH*	XXXXXXXX	Manual mode high byte of internally generated frame sync period in terms of PCLK cycles (effective when FSYNCMETH = 00 and FSYNCMODE = 0X)	00000000
0x09	D[7:1]	DESADDR	XXXXXXX	Deserializer device address (power-up default value depends on latched address pin level)	XX01XXX
	D0	CFGBLOCK	0	Normal operation	0
			1	Registers 0x00 to 0x1F are read only	
0x0A	D7	FWDCCEN3	0	Disable link 3 forward control channel from serializer (receiving)	1
			1	Enable link 3 forward control channel from serializer (receiving)	
	D6	FWDCCEN2	0	Disable link 2 forward control channel from serializer (receiving)	1
			1	Enable link 2 forward control channel from serializer (receiving)	
	D5	FWDCCEN1	0	Disable link 1 forward control channel from serializer (receiving)	1
			1	Enable link 1 forward control channel from serializer (receiving)	
	D4	FWDCCEN0	0	Disable link 0 forward control channel from serializer (receiving)	1
			1	Enable link 0 forward control channel from serializer (receiving)	
	D3	REVCCEN3	0	Disable link 3 reverse control channel to serializer (sending)	1
			1	Enable link 3 reverse control channel to serializer (sending)	
	D2	REVCCEN2	0	Disable link 2 reverse control channel to serializer (sending)	1
			1	Enable link 2 reverse control channel to serializer (sending)	
	D1	REVCCEN1	0	Disable link 1 reverse control channel to serializer (sending)	1
			1	Enable link 1 reverse control channel to serializer (sending)	
	D0	REVCCEN0	0	Disable link 0 reverse control channel to serializer (sending)	1
			1	Enable link 0 reverse control channel to serializer (sending)	

Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x0B	D[7:6]	LINK3 OUTORD	00	Link 3 is first in the CSI-2 output order (assign each link a unique position in the output order)	11
			01	Link 3 is second in the CSI-2 output order	
			10	Link 3 is third in the CSI-2 output order	
			11	Link 3 is fourth in the CSI-2 output order	
	D[5:4]	LINK2 OUTORD	00	Link 2 is first in the CSI-2 output order (assign each link a unique position in the output order)	10
			01	Link 2 is second in the CSI-2 output order	
			10	Link 2 is third in the CSI-2 output order	
			11	Link 2 is fourth in the CSI-2 output order	
	D[3:2]	LINK1 OUTORD	00	Link 1 is first in the CSI-2 output order (assign each link a unique position in the output order)	01
			01	Link 1 is second in the CSI-2 output order	
			10	Link 1 is third in the CSI-2 output order	
			11	Link 1 is fourth in the CSI-2 output order	
	D[1:0]	LINK0 OUTORD	00	Link 0 is first in the CSI-2 output order (assign each link a unique position in the output order)	00
			01	Link 0 is second in the CSI-2 output order	
			10	Link 0 is third in the CSI-2 output order	
			11	Link 0 is fourth in the CSI-2 output order	
0x0C	D7	HVEN	0	Do not use HS/VS encoding	1
			1	Use HS/VS encoding (set this bit when the **MAX9271/MAX9273** uses HV encoding) Keep HS/VS high or low for at least 8 pixel clock cycles	
	D[6:5]	EDC	00	Use 1-bit parity error detection (compatible with all GMSL serializers)	00
			01	Use 6-bit CRC error detection (use when the **MAX9271/ MAX9273** uses CRC)	
			10	Use 6-bit Hamming code (single bit-error correct, double bit-error detect) and 16-word interleaving (use when the **MAX9271/ MAX9273** uses Hamming)	
			11	Do not use	
	D4	DESEL	0	Use DE as line valid source (when HVEN = 0 and DBL = 0)	1
			1	Use HS as line valid source (when HVEN = 0 and DBL = 0)	
	D3	INVVS	0	Do not invert VSYNC polarity	1
			1	Invert VSYNC polarity	
	D2	INVHS	0	Do not invert HSYNC polarity	0
			1	Invert HSYNC polarity	
	D[1:0]	HVSRC	00	Use D18. D19 for HSYNC/VSYNC	01
			01	Use D14/D15 for HSYNC/VSYNC (D[19:16] shifted to D[17:14]). For use with the **MAX9271** when DBL = 0 or when HVEN = 1.	
			1X	Use D0/D1 for HSYNC/VSYNC (D[19:2] shifted to D[17:0]). For use with the **MAX9271/MAX9273** when DBL = 1 and HVEN = 0.	

Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x0D	D7	LFLTEN3	0	Line fault monitor for Link 3 disabled	1
			1	Line fault monitor for Link 3 enable	
	D6	LFLTEN2	0	Line fault monitor for Link 2 disabled	1
			1	Line fault monitor for Link 2 enable	
	D5	LFLTEN1	0	Line fault monitor for Link 1 disabled	1
			1	Line fault monitor for Link 1 enable	
	D4	LFLTEN0	0	Line fault monitor for Link 0 disabled	1
			1	Line fault monitor for Link 0 enable	
	D3	—	0	Reserved	0
	D2	HSTRACK	0	Disable HSYNC/line valid tracking	0
			1	Enable HSYNC/line valid tracking	
	D1	ENHSFILT	0	Disable HSYNC glitch filtering (power up default when BWS = open)	X
			1	Enable HSYNC glitch filtering (power up default when BWS = low, high)	
	D0	ENVSFILT	0	Disable VSYNC glitch filtering (power up default when BWS = open)	X
			1	Enable VSYNC glitch filtering (power up default when BWS = low, high)	
0x0E	D7	SLEEP	0	Normal mode	0
			1	Activate sleep mode	
	D6	DISRWAKE	0	Enable remote wake-up from serializer	1
			1	Disable remote wake-up from serializer	
	D5	DRS	0	High data rate mode	0
			1	Low data rate mode	
	D4	PRBSTYPE	0	Use MAX9249, MAX9259-MAX9265 and MAX9275-MAX9293 compatible PRBS test	1
			1	Use MAX9273/MAX9271 compatible PRBS test (**Power-up default)**	
	D3	PRBSEN3	0	Enable PRBS test for Link 3	0
			1	Disable PRBS test for Link 3	
	D2	PRBSEN2	0	Enable PRBS test for Link 2	0
			1	Disable PRBS test for Link 2	
	D1	PRBSEN1	0	Enable PRBS test for Link 1	0
			1	Disable PRBS test for Link 1	
	D0	PRBSEN0	0	Enable PRBS test for Link 0	0
			1	Disable PRBS test for Link 0	

Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x0F	D[7:6]	ERRSEL	00	Assert $\overline{ERR}$ when DETERR > DETTHR	00
			01	Assert $\overline{ERR}$ when CORRERR > CORRTHR	
			1x	Assert $\overline{ERR}$ when DETERR > DETTHR or CORRERR > CORRTHR	
	D5	ERRRST	0	Do not automatically reset error registers and outputs	0
			1	Automatically reset DETERR and CORRERR registers 1µs after $\overline{ERR}$ asserts	
	D[4:2]	—	010	Reserved	010
	D1	GPIO1OUT	0	Set GPIO1 to low	1
			1	Set GPIO1 to high	
	D0	GPIO0OUT	0	Set GPIO0 to low	1
			1	Set GPIO0 to high	
0x10	D[7:0]	DETTHR	XXXXXXXX	Error threshold for detected errors	00000000
0x11	D[7:0]	CORRTHR	XXXXXXXX	Error threshold for corrected errors	00000000
0x12	D[7:6]	CSILANECNT	00	Enable CSI data lane D0	11
			01	Enable CSI data lanes D0, D1	
			10	Enable CSI data lanes D0-D2	
			11	Enable CSI data lanes D0-D3	
	D5	CSIDBL	0	RAW8/10/12 mode uses single load. YUV422-8b/10b uses muxed mode (clear this bit when DBL = 0)	1
			1	RAW8/10/12 mode uses double load. YUV422-8b/10b uses normal mode (Set this bit when DBL = 1)	
	D4	DBL	0	Use single input mode. (clear this bit when the serializer uses single input mode)	1
			1	Use double input mode (set this bit when the **MAX9271/ MAX9273** uses double input mode)	
	D[3:0]	DATATYPE	0000	CSI-2 Output uses RGB888	0100
			0001	CSI-2 Output uses RGB565	
			0010	CSI-2 Output uses RGB666	
			0011	CSI-2 Output uses YUV 422 8-bit	
			0100	CSI-2 Output uses YUV 422 10-bit **(Power-on default)**	
			0101	CSI-2 Output uses RAW8/RAW16	
			0110	CSI-2 Output uses RAW10/RAW20	
			0111	CSI-2 Output uses RAW11/RAW12	
			1000	CSI-2 Output uses RAW14	
			1001	CSI-2 Output uses user defined generic 24-bit	
			1010	CSI-2 Output uses user defined YUV422 12-bit	
			1011	CSI-2 Output uses user defined generic 8-bit	

Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x13	D[7:4]	—	0000	Reserved	0000
	D3	OLDI	0	RGB888 uses VESA format	1
			1	RGB888 uses oLDI format	
	D[2:0]	DPHYRNG	000	80Mbps to 125Mbps D-PHY data rate	111
			001	125Mbps to 250Mbps D-PHY data rate	
			010	250Mbps to 500Mbps D-PHY data rate	
			011	500Mbps to 1200Mbps D-PHY data rate	
			1XX	Auto-detect D-PHY data rate range	
0x14	D[7:6]	CSILAN E3MAP	00	Map lane 3 data to CSI output lane 0 (data mapping should be exclusive)	11
			01	Map lane 3 data to CSI output lane 1	
			10	Map lane 3 data to CSI output lane 2	
			11	Map lane 3 data to CSI output lane 3	
	D[5:4]	CSILAN E2MAP	00	Map lane 2 data to CSI output lane 0 (data mapping should be exclusive)	10
			01	Map lane 2 data to CSI output lane 1	
			10	Map lane 2 data to CSI output lane 2	
			11	Map lane 2 data to CSI output lane 3	
	D[3:2]	CSILAN E1MAP	00	Map lane 1 data to CSI output lane 0 (data mapping should be exclusive)	01
			01	Map lane 1 data to CSI output lane 1	
			10	Map lane 1 data to CSI output lane 2	
			11	Map lane 1 data to CSI output lane 3	
	D[1:0]	CSILAN E0MAP	00	Map lane 0 data to CSI output lane 0 (data mapping should be exclusive)	00
			01	Map lane 0 data to CSI output lane 1	
			10	Map lane 0 data to CSI output lane 2	
			1	Map lane 0 data to CSI output lane 3	
0x15	D7	—	0	Reserved	0
	D[6:5]	VC	00	CSI-2 outputs on virtual channel 0 (when VCITYPE = 0)	00
			01	CSI-2 outputs on virtual channel 1 (when VCITYPE = 0)	
			10	CSI-2 outputs on virtual channel 2 (when VCITYPE = 0)	
			11	CSI-2 outputs on virtual channel 3 (when VCITYPE = 0)	
	D4	VCTYPE	0	Set virtual channel manually with VC bits (see above)	0
			1	Set virtual channel according to the link number	
	D3	CSIOUTEN	0	Disable CSI-2 output. (in external FSYNC mode, keep this bit low until frame sync is achieved)	1
			1	Enable CSI-2 output	
	D[2:0]	—	011	Reserved	011

Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x16	D[7:0]	CSIFRM CNTPERL	XXXXXXXX	Low byte of CSI-2 frame counter period	00000000
0x17	D[7:0]	CSIFRM CNTPERH	XXXXXXXX	High byte of CSI-2 frame counter period	00000001
0x18	D[7:6]	TCLK PREPARE	00	Drive clock lane LP00 for 64ns before starting HS transmission	00
			01	Drive clock lane LP00 for 72ns before starting HS transmission	
			10	Drive clock lane LP00 for 80ns before starting HS transmission	
			11	Drive clock lane LP00 for 88ns before starting HS transmission	
	D[5:4]	TCLKZERO	00	Drive HS0 state for 360ns + 16-24UI before starting the clock	00
			01	Drive HS0 state for 720ns + 16-24UI before starting the clock	
			10	Drive HS0 state for 1.08µs + 16-24UI before starting the clock	
			11	Drive HS0 state for 1.44µs + 16-24UI before starting the clock	
	D[3:0]	—	0000	Reserved	000
0x19	D[7:6]	THS PREPARE	00	Drive data lane LP00 for 64ns +4UI before starting HS transmission	00
			01	Drive data lane LP00 for 72ns + 4UI before starting HS transmission	
			10	Drive data lane LP00 for 80ns + 4UI before starting HS transmission	
			11	Drive data lane LP00 for 88ns + 4UI before starting HS transmission	
	D[5:4]	THSZERO	00	Drive HS0 state for 160ns + 24 - 32UI before transmitting the sync sequence	00
			01	Drive HS0 state for 176ns + 24 - 32UI before transmitting the sync sequence	
			10	Drive HS0 state for 200ns + 24 - 32UI before transmitting the sync sequence	
			11	Drive HS0 state for 240ns + 24 - 32UI before transmitting the sync sequence	
	D[3:2]	THSTRAIL	00	Drive HSTRAIL state for 64ns + 8UI after the last payload data bit of a HS transmission burst.	00
			01	Drive HSTRAIL state for 80ns + 8UI after the last payload data bit of a HS transmission burst.	
			10	Drive HSTRAIL state for 96ns + 8UI after the last payload data bit of a HS transmission burst.	
			11	Drive HSTRAIL state for 120ns + 8UI after the last payload data bit of a HS transmission burst.	
	D[1:0]	TLPX	00	64ns LPTX period length	00
			01	128ns LPTX period length	
			10	192ns LPTX period length	
			11	256ns LPTX period length	

Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x1A	D7	—	0	Reserved	0
	D[6:5]	SRNG	00	0.5 to 1Gbps serial data rate	11
			01	1 to 1.5Gbps serial data rate	
			1X	Automatically detect serial data rate	
	D4	SWITCHCLK	0	Do not switch CLK+ and CLK- output pins	0
			1	Switch CLK+ and CLK- output pins	
	D3	SWITCHDO3	0	Do not switch DOUT3+ and DOUT3- output pins	0
			1	Switch DOUT3+ and DOUT3- output pins	
	D2	SWITCHDO2	0	Do not switch DOUT2+ and DOUT2- output pins	0
			1	Switch DOUT2+ and DOUT2- output pins	
	D1	SWITCHDO1	0	Do not switch DOUT1+ and DOUT1- output pins	0
			1	Switch DOUT1+ and DOUT1- output pins	
	D0	SWITCHDO0	0	Do not switch DOUT0+ and DOUT0- output pins	0
			1	Switch DOUT0+ and DOUT0- output pins	
0x1B	D7	SWITCHIN3	0	Do not switch IN3+ and IN3- input pins	0
			1	Switch IN3+ and IN3- input pins	
	D6	SWITCHIN2	0	Do not switch IN2+ and IN2- input pins	0
			1	Switch IN2+ and IN2- input pins	
	D5	SWITCHIN1	0	Do not switch IN1+ and IN1- input pins	0
			1	Switch IN1+ and IN1- input pins	
	D4	SWITCHIN0	0	Do not switch IN0+ and IN0- input pins	0
			1	Switch IN0+ and IN0- input pins	
	D3	ENEQ3	0	Disable link 3 equalizer. **Power-up default**	0
			1	Enable link 3 equalizer	
	D2	ENEQ2	0	Disable link 2 equalizer. **Power-up default.**	0
			1	Enable link 2 equalizer	
	D1	ENEQ1	0	Disable link 1 equalizer. **Power-up default.**	0
			1	Enable link 1 equalizer	
	D0	ENEQ0	0	Disable link 0 equalizer. **Power-up default.**	0
			1	Enable link 0 equalizer	

Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x1C	D7	HIGHIMM3	0	Use legacy reverse control channel mode for link 3 (power-up default value when HIM = low)	X
			1	Use high immunity reverse control channel mode for link 3 (power-up default when HIM = high). **Compatible with the MAX9275-MAX9293 only**.	
	D6	HIGHIMM2	0	Use legacy reverse control channel mode for link 2 (power-up default value when HIM = low)	X
			1	Use high immunity reverse control channel mode for link 2 (power-up default when HIM = high). **Compatible with the MAX9275-MAX9293 only**.	
	D5	HIGHIMM1	0	Use legacy reverse control channel mode for link 1 (power-up default value when HIM = low)	X
			1	Use high immunity reverse control channel mode for link 1 (power-up default when HIM = high). **Compatible with the MAX9275-MAX9293 only**.	
	D4	HIGHIMM0	0	Use legacy reverse control channel mode for link 0 (power-up default value when HIM = low)	X
			1	Use high immunity reverse control channel mode for link 0 (power-up default when HIM = high). **Compatible with the MAX9275-MAX9293 only**.	
	D[3:0]	—	0XXX	Reserved	0XXX
0x1D	D[7:4]	—	1111	Reserved	1111
	D3	CXTP3	0	Use twisted pair input for link 3 (power-up default value when CX/TP = low)	X
			1	Use coax input for link 3 (power-up default when CX/TP = high or open. **Compatible with the MAX9271-MAX9293 only.**	
	D2	CXTP2	0	Use twisted pair input for link 2 (power-up default value when CX/TP = low)	X
			1	Use coax input for link 2 (power-up default when CX/TP = high or open. **Compatible with the MAX9271-MAX9293 only.**	
	D1	CXTP1	0	Use twisted pair input for link 1 (power-up default value when CX/TP = low)	X
			1	Use coax input for link 1 (power-up default when CX/TP = high or open. **Compatible with the MAX9271-MAX9293 only.**	
	D0	CXTP0	0	Use twisted pair input for link 0 (power-up default value when CX/TP = low)	X
			1	Use coax input for link 0 (power-up default when CX/TP = high or open. **Compatible with the MAX9271-MAX9293 only.**	
0x1E	D[7:0]	ID	01000000	Device identifier (MAX9286 = 0x40)	01000000 (Read only)
0x1F	D[7:5]	—	000	Reserved	000 (Read only)
	D4	CAPS	0	Not HDCP capable (MAX9286)	0 (Read only)
	D[3:0]	REVISION	XXXX	Device revision	(Read only)

Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x20	D[7:6]	LF3	00	Line connected to LMN3 is shorted to battery	10 (Read only)
			01	Line connected to LMN3 is shorted to ground	
			10	Line connected to LMN3 is normal	
			11	Line connected to LMN3 is open	
	D[5:4]	LF2	00	Line connected to LMN2 is shorted to battery	10 (Read only)
			01	Line connected to LMN2 is shorted to ground	
			10	Line connected to LMN2 is normal	
			11	Line connected to LMN2 is open	
	D[3:2]	LF1	00	Line connected to LMN1 is shorted to battery	10 (Read only)
			01	Line connected to LMN1 is shorted to ground	
			10	Line connected to LMN1 is normal	
			11	Line connected to LMN1 is open	
	D[1:0]	LF0	00	Line connected to LMN0 is shorted to battery	10 (Read only)
			01	Line connected to LMN0 is shorted to ground	
			10	Line connected to LMN0 is normal	
			11	Line connected to LMN0 is open	
0x21	D7	PRBSOK3	0	Link 3 MAX9271/MAX9273 compatible test not completed, or completed with abnormalities	0 (Read only)
			1	Link 3 MAX9271/MAX9273 compatible test completed without abnormalities. Check PRBSERR3 for the number of PRBS errors	
	D6	PRBSOK2	0	Link 2 MAX9271/MAX9273 compatible test not completed, or completed with abnormalities	0 (Read only)
			1	Link 2 MAX9271/MAX9273 compatible test completed without abnormalities. Check PRBSERR3 for the number of PRBS errors.	
	D5	PRBSOK1	0	Link 1 MAX9271/MAX9273 compatible test not completed, or completed with abnormalities	0 (Read only)
			1	Link 1 MAX9271/MAX9273 compatible test completed without abnormalities. Check PRBSERR3 for the number of PRBS errors.	
	D4	PRBSOK0	0	Link 0 MAX9271/MAX9273 compatible test not completed, or completed with abnormalities	0 (Read only)
			1	Link 0 MAX9271/MAX9273 compatible test completed without abnormalities. Check PRBSERR3 for the number of PRBS errors.	
	D3	HLOCKED3	0	Line tracking for link 3 is locked	0 (Read only)
			1	Line tracking for link 3 is not locked	
	D2	HLOCKED2	0	Line tracking for link 2 is locked	0 (Read only)
			1	Line tracking for link 2 is not locked	
	D1	HLOCKED1	0	Line tracking for link 1 is locked	0 (Read only)
			1	Line tracking for link 1 is not locked	
	D0	HLOCKED0	0	Line tracking for link 0 is locked	0 (Read only)
			1	Line tracking for link 0 is not locked	

Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x22	D7	LINBUFFOF3	0	Line buffer for link 3 is normal	0 (Read only)
			1	Line buffer for link 3 is overflowed	
	D6	LINBUFFOF2	0	Line buffer for link 2 is normal	0 (Read only)
			1	Line buffer for link 2 is overflowed	
	D5	LINBUFFOF1	0	Line buffer for link 1 is normal	0 (Read only)
			1	Line buffer for link 1 is overflowed	
	D4	LINBUFFOF0	0	Line buffer for link 0 is normal	0 (Read only)
			1	Line buffer for link 0 is overflowed	
	D3	LENGTH ERR3	0	Link 3 is normal	0 (Read only)
			1	Link 3 has a line error detected	
	D2	LENGTH ERR2	0	Link 2 is normal	0 (Read only)
			1	Link 2 has a line error detected	
	D1	LENGTH ERR1	0	Link 1 is normal	0 (Read only)
			1	Link 1 has a line error detected	
	D0	LENGTH ERR0	0	Link 0 is normal	0 (Read only)
			1	Link 0 has a line error detected	
0x23	D[7:0]	PRBSERR0	XXXXXXXX	PRBS error counter for link 0. Counter resets to zero when read	00000000 (Read only)
0x24	D[7:0]	PRBSERR1	XXXXXXXX	PRBS error counter for link 1. Counter resets to zero when read	00000000 (Read only)
0x25	D[7:0]	PRBSERR2	XXXXXXXX	PRBS error counter for link 2. Counter resets to zero when read	00000000 (Read only)
0x26	D[7:0]	PRBSERR3	XXXXXXXX	PRBS error counter for link 3. Counter resets to zero when read	00000000 (Read only)

Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x27	D7	LOCKED	0	One or more enabled input links are not locked (LOCK = low)	0 (Read only)
			1	All enabled input links are locked (LOCK = high)	
	D6	GPIIN	0	GPI input is low	(Read only)
			1	GPI input is high	
	D5	GPIO1IN	0	GPIO1 input is low	(Read only)
			1	GPIO1 input is high	
	D4	GPIO0IN	0	GPIO0 input is low	(Read only)
			1	GPIO0 input is high	
	D3	VSYNCDET3	0	No rising edge VSYNC on link 3 detected	0 (Read only)
			1	Rising edge VSYNC on link 3 detected (cleared when read or no VSYNC is detected for 100ms)	
	D2	VSYNCDET2	0	No rising edge VSYNC on link 2 detected	0 (Read only)
			1	Rising edge VSYNC on link 2 detected (cleared when read or no VSYNC is detected for 100ms)	
	D1	VSYNCDET1	0	No rising edge VSYNC on link 1 detected	0 (Read only)
			1	Rising edge VSYNC on link 1 detected (cleared when read or no VSYNC is detected for 100ms)	
	D0	VSYNCDET0	0	No rising edge VSYNC on link 0 detected	0 (Read only)
			1	Rising edge VSYNC on link 0 detected (cleared when read or no VSYNC is detected for 100ms)	
0x28	D[7:0]	DETERR0	XXXXXXXX	Detected error counter for link 0. Counter resets to zero when read, or when the device locks to an incoming serial bit stream,	00000000 (Read only)
0x29	D[7:0]	DETERR1	XXXXXXXX	Detected error counter for link 1. Counter resets to zero when read, or when the device locks to an incoming serial bit stream,	00000000 (Read only)
0x2A	D[7:0]	DETERR2	XXXXXXXX	Detected error counter for link 2. Counter resets to zero when read, or when the device locks to an incoming serial bit stream,	00000000 (Read only)
0x2B	D[7:0]	DETERR3	XXXXXXXX	Detected error counter for link 3. Counter resets to zero when read, or when the device locks to an incoming serial bit stream,	00000000 (Read only)
0x2C	D[7:0]	CORRERR0	XXXXXXXX	Corrected error counter for link 0. Counter resets to zero when read, or when the device locks to an incoming serial bit stream,	00000000 (Read only)
0x2D	D[7:0]	CORRERR1	XXXXXXXX	Corrected error counter for link 1. Counter resets to zero when read, or when the device locks to an incoming serial bit stream,	00000000 (Read only)
0x2E	D[7:0]	CORRERR2	XXXXXXXX	Corrected error counter for link 2. Counter resets to zero when read, or when the device locks to an incoming serial bit stream,	00000000 (Read only)
0x2F	D[7:0]	CORRERR3	XXXXXXXX	Corrected error counter for link 3. Counter resets to zero when read, or when the device locks to an incoming serial bit stream,	00000000 (Read only)
0x30	D[7:0]	FRMDIFFL	XXXXXXXX	Low byte of the difference between the fastest and slowest frame (in master PCLK cycles)	00000000 (Read only)

Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x31	D7	FSYNCLOSS OFLOCK	0	No loss-of-lock has occurred	0 (Read only)
			1	Loss-of-lock has occurred (cleared when read)	
	D6	FSYNC LOCKED	0	Frame synchronization is not locked	0 (Read only)
			1	Frame synchronization is locked	
	D[5:0]	FRMDIFFH	XXXXXXXX	High byte of the difference between the fastest and slowest frame (in master PCLK cycles)	000000 (Read only)
0x32	D[7:4]	EQTUNE0*	0000	Link 0 uses 2.1dB equalizer boost gain	1001
			0001	Link 0 uses 2.8dB equalizer boost gain	
			0010	Link 0 uses 3.4dB equalizer boost gain	
			0011	Link 0 uses 4.2dB equalizer boost gain	
			0100	Link 0 uses 5.2dB equalizer boost gain.	
			0101	Link 0 uses 6.2dB equalizer boost gain	
			0110	Link 0 uses 7dB equalizer boost gain	
			0111	Link 0 uses 8.2dB equalizer boost gain	
			1000	Link 0 uses 9.4dB equalizer boost gain	
			1001	Link 0 uses 10.7dB equalizer boost gain. **Power-up default,**	
			1010	Link 0 uses 11.7dB equalizer boost gain	
			1011	Link 0 uses 13dB equalizer boost gain	
			11XX	Do not use	
	D[3:0]	EQTUNE1*	0000	Link 1 uses 2.1dB equalizer boost gain	1001
			0001	Link 1 uses 2.8dB equalizer boost gain	
			0010	Link 1 uses 3.4dB equalizer boost gain	
			0011	Link 1 uses 4.2dB equalizer boost gain	
			0100	Link 1 uses 5.2dB equalizer boost gain.	
			0101	Link 1 uses 6.2dB equalizer boost gain	
			0110	Link 1 uses 7dB equalizer boost gain	
			0111	Link 1 uses 8.2dB equalizer boost gain	
			1000	Link 1 uses 9.4dB equalizer boost gain	
			1001	Link 1 uses 10.7dB equalizer boost gain. **Power-up default,**	
			1010	Link 1 uses 11.7dB equalizer boost gain	
			1011	Link 1 uses 13dB equalizer boost gain	
			11XX	Do not use	

Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x33	D[7:4]	EQTUNE2*	0000	Link 2 uses 2.1dB equalizer boost gain	1001
			0001	Link 2 uses 2.8dB equalizer boost gain	
			0010	Link 2 uses 3.4dB equalizer boost gain	
			0011	Link 2 uses 4.2dB equalizer boost gain	
			0100	Link 2 uses 5.2dB equalizer boost gain.	
			0101	Link 2 uses 6.2dB equalizer boost gain	
			0110	Link 2 uses 7dB equalizer boost gain	
			0111	Link 2 uses 8.2dB equalizer boost gain	
			1000	Link 2 uses 9.4dB equalizer boost gain	
			1001	Link 2 uses 10.7dB equalizer boost gain. **Power-up default,**	
			1010	Link 2 uses 11.7dB equalizer boost gain	
			1011	Link 2 uses 13dB equalizer boost gain	
			11XX	Do not use	
	D[3:0]	EQTUNE3*	0000	Link 3 uses 2.1dB equalizer boost gain	1001
			0001	Link 3 uses 2.8dB equalizer boost gain	
			0010	Link 3 uses 3.4dB equalizer boost gain	
			0011	Link 3 uses 4.2dB equalizer boost gain	
			0100	Link 3 uses 5.2dB equalizer boost gain.	
			0101	Link 3 uses 6.2dB equalizer boost gain	
			0110	Link 3 uses 7dB equalizer boost gain	
			0111	Link 3 uses 8.2dB equalizer boost gain	
			1000	Link 3 uses 9.4dB equalizer boost gain	
			1001	Link 3 uses 10.7dB equalizer boost gain. **Power-up default,**	
			1010	Link 3 uses 11.7dB equalizer boost gain	
			1011	Link 3 uses 13dB equalizer boost gain	
			11XX	Do not use	

Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x34	D7	I2CLOCACK	0	Acknowledge not generated when forward channel is not available	1
			1	I²C to I²C-slave generates local acknowledge when forward channel is not available	
	D[6:5]	I2CSLVSH	00	352ns/117ns I²C setup/hold time	01
			01	469ns/234ns I²C setup/hold time	
			10	938ns/352ns I²C setup/hold time	
			11	1046ns/469ns I²C setup/hold time	
	D[4:2]	I2CMSTBT	000	8.47kbps (typ) I²C to I²C-master bit rate setting (Set the serializer I2CMSTBT setting to the same value)	101
			001	28.3kbps (typ) I²C to I²C-master bit rate setting	
			010	84.7kbps (typ) I²C to I²C-master bit rate setting	
			011	105kbps (typ) I²C to I²C-master bit rate setting	
			100	173kbps (typ) I²C to I²C-master bit rate setting	
			101	339kbps (typ) I²C to I²C-master bit rate setting	
			110	533kbps (typ) I²C to I²C-master bit rate setting	
			111	837kbps (typ) I²C to I²C-master bit rate setting	
	D[1:0]	I2CSLVTO	00	64µs (typ) I²C to I²C-slave remote timeout	10
			01	256µs (typ) I²C to I²C-slave remote timeout	
			10	1024µs (typ) I²C to I²C-slave remote timeout	
			11	No I²C to I²C-slave remote timeout	
0x35	D[7:0]	—	00000000	Reserved	00000000
0x36	D[7:0]	—	00000000	Reserved	00000000
0x37	D[7:0]	—	00000000	Reserved	00000000
0x38	D[7:0]	—	00000000	Reserved	00000000
0x39	D[7:0]	—	00000000	Reserved	00000000
0x3A	D[7:0]	—	00000000	Reserved	00000000
0x3B	D[7:0]	—	0010XXX0	Reserved	0010XXX0
0x3C	D[7:0]	—	00100100	Reserved	00100100
0x3D	D[7:0]	—	01010100	Reserved	01010100
0x3E	D[7:0]	—	11001000	Reserved	11001000
0x3F	D[7:0]	—	00100010	Reserved	00100010
0x40	D[7:0]	—	01011010	Reserved	01011010
0x41	D[7:0]	—	X0010000	Reserved	00010000
0x42	D[7:0]	—	00000000	Reserved	00000000
0x43	D[7:0]	—	10X00000	Reserved	10X00000
0x44	D[7:0]	—	00000000	Reserved	00000000

Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x45	D[7:0]	—	00000000	Reserved	00000000
0x46	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x47	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x48	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x49	D7	CONFIGDET3	0	No configuration link detected for link 3	(Read only)
			1	Configuration link detected for link 3	
	D6	CONFIGDET2	0	No configuration link detected for link 2	(Read only)
			1	Configuration link detected for link 2	
	D5	CONFIGDET1	0	No configuration link detected for link 1	(Read only)
			1	Configuration link detected for link 1	
	D4	CONFIGDET0	0	No configuration link detected for link 0	(Read only)
			1	Configuration link detected for link 0	
	D3	VIDEODET3	0	No video link detected for link 3	(Read only)
			1	Video link detected for link 3	
	D2	VIDEODET2	0	No video link detected for link 2	(Read only)
			1	Video link detected for link 2	
	D1	VIDEODET1	0	No video link detected for link 1	(Read only)
			1	Video link detected for link 1	
	D0	VIDEODET0	0	No video link detected for link 0	(Read only)
			1	Video link detected for link 0	
0x4A	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x4B	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x4C	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x4D	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x4E	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x4F	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x50	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x51	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x52	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)

Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x53	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x54	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x55	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x56	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x57	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x58	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x59	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x5A	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX (Read only)
0x5B	D[7:0]	CALCFRM LENL	XXXXXXXX	Low byte of calculated VS period (in pixel clock cycles) of master link in auto synchronization mode (Use when FSYNCMETH = 10 and FSYNCMODE = 0x)	XXXXXXXX (Read only)
0x5C	D[7:0]	CALCFRM LENM	XXXXXXXX	Mid byte of calculated VS period (in pixel clock cycles) of master link in auto synchronization mode (Use when FSYNCMETH = 10 and FSYNCMODE = 0x)	XXXXXXXX (Read only)
0x5D	D[7:0]	CALCFRM LENH	XXXXXXXX	High byte of calculated VS period (in pixel clock cycles) of master link in auto synchronization mode (Use when FSYNCMETH = 10 and FSYNCMODE = 0x)	XXXXXXXX (Read only)
0x5E	D[7:0]	FRMSYNC ERRCNT	XXXXXXXX	Frame sync error counter (reset to zero when read)	XXXXXXXX (Read only)
0x5F	D[7:0]	FRMSYNC ERRTHR	XXXXXXXX	Frame sync error threshold	00000000
0x60	D[7:3]	—	01000	Reserved	01000
	D2	ENSYNC LMOB	0	Disable FSYNCLOSSOFLOCK bit to drive $\overline{LMO}$	1
			1	Enable FSYNCLOSSOFLOCK bit to drive $\overline{LMO}$	
	D1	SYNCERR RST	0	SYNCERRCNT does not automatically reset	0
				Automatically reset SYNCERRCNT register 1µs after $\overline{ERR}$ pin is asserted	
	D0	ENSYNCERR	0	Do not assert $\overline{ERR}$ when FRMSYNCERRCNT > FRMSYNCERRTHR	1
			1	Assert $\overline{ERR}$ when FRMSYNCERRCNT > FRMSYNCERRTHR	
0x61	D[7:0]	FRMDIFF ERRTHRL	XXXXXXXX	Low byte of error threshold between the earliest and latest VSYNC (in pixel clock cycles). Disabled if all 13 bits are zero.	00000000

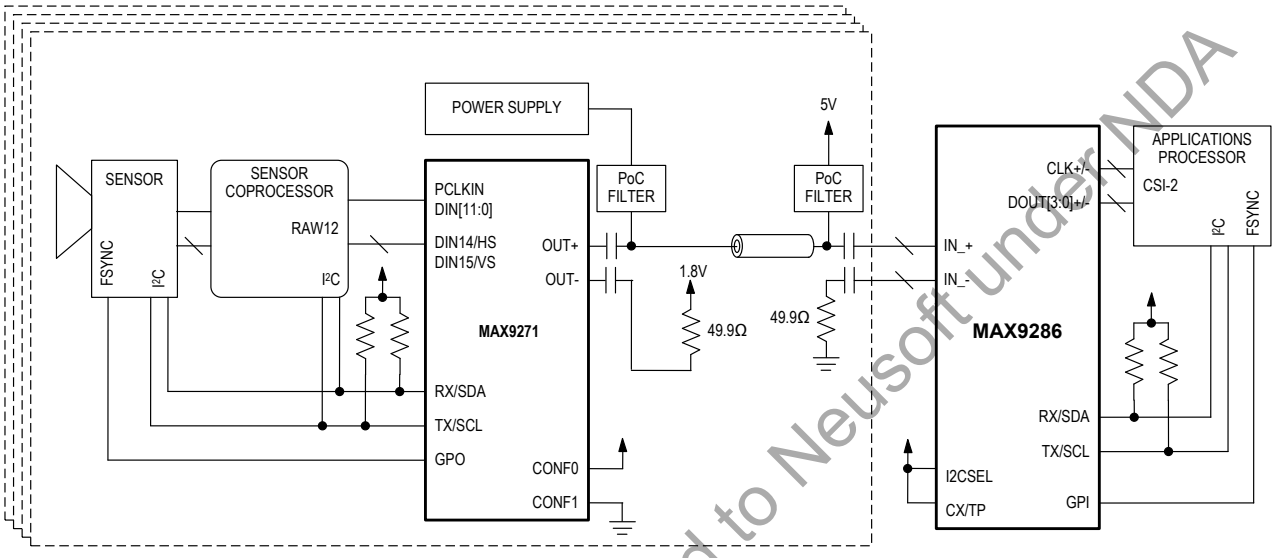
Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x62	D[7:5]	—	000	Reserved	000
	D[4:0]	FRMDIFF ERRTHRH	XXXXX	High byte of error threshold between the earliest and latest VSYNC (in pixel clock cycles). Disabled if all 13 bits are zero.	01111
0x63	D[7:0]	OVLP WINDOWL	XXXXXXXX	Low byte of overlap window (in pixel clock cycles). Disabled if all 13 bits are zero.	10000000
0x64	D[7:6]	—	00	Reserved	00
	D5	ENFSINLAST	0	FSIN occurs anytime between VS rising edges	0
			1	FSIN occurs after all VS rising edges	
	D[4:0]	OVLP WINDOWH	XXXXX	High byte of overlap window (in pixel clock cycles). Disabled if all 13 bits are zero.	10110
0x65	D[7:0]	—	00010010	Reserved	00010010
0x66	D[7:0]	—	10010110	Reserved	10010110
0x67	D[7:2]	—	000000	Reserved	000000
	D1	CCARBEN	0	Disable UART forward channel arbitration	0
			1	Enable UART forward channel arbitration	
	D0	CCARBTO*	0	256µs forward channel arbitration timeout	0
			1	4ms forward channel arbitration timeout	
0x68	D[7:1]	—	0100000	Reserved	0101000
	D0	ENMONOUT	0	Disable serial link monitor output	0
			1	Enable serial link monitor output	
0x69	D7	LFLTBMON MASKED	0	$\overline{\text{LFLT}}$ pin reflects the status of enabled and unmasked links	0
			1	$\overline{\text{LFLT}}$ pin reflects the status of all enabled links	
	D6	LOCKMON MASKED	0	LOCK pin reflects the status of enabled and unmasked links	0
			1	LOCK pin reflects the status of all enabled links	
	D5	AUTO COMBACKEN	0	Auto comeback disabled (see the *Link Masking* section)	0
			1	Auto comeback enabled (see the *Link Masking* section)	
	D4	AUTOMASK EN	0	Auto mask disabled (see the *Link Masking* section)	0
			1	Auto mask enabled (see the *Link Masking* section)	
	D3	MASKLINK3	0	Do not mask link 3	0
			1	Mask link 3	
	D2	MASKLINK2	0	Do not mask link 2	0
			1	Mask link 2	
	D1	MASKLINK1	0	Do not mask link 1	0
			1	Mask link 1	
	D0	MASKLINK0	0	Do not mask link 0	0
			1	Mask link 0	

Table 27. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x70	D7	I2CACK RECVED3	0	No I²C response received for last packet from remote side of link 3	(Read only)
			1	I²C response received for last packet from remote side of link 3	
	D6	I2CACK RECVED2	0	No I²C response received for last packet from remote side of link 2	(Read only)
			1	I²C response received for last packet from remote side of link 2	
	D5	I2CACK RECVED1	0	No I²C response received for last packet from remote side of link 1	(Read only)
			1	I²C response received for last packet from remote side of link 1	
	D4	I2CACK RECVED0	0	No I²C response received for last packet from remote side of link 0	(Read only)
			1	I²C response received for last packet from remote side of link 0	
	D3	I2CACKED3	0	I²C ack bit was low (ACK) at remote side of link 3	(Read only)
			1	I²C ack bit was high (NACK) at remote side of link 3	
	D2	I2CACKED2	0	I²C ack bit was low (ACK) at remote side of link 2	(Read only)
			1	I²C ack bit was high (NACK) at remote side of link 2	
	D1	I2CACKED1	0	I²C ack bit was low (ACK) at remote side of link 1	(Read only)
			1	I²C ack bit was high (NACK) at remote side of link 1	
	D0	I2CACKED0	0	I²C ack bit was low (ACK) at remote side of link 0	(Read only)
			1	I²C ack bit was high (NACK) at remote side of link 0	
0x71	D[7:6]	—	00	Reserved	00 (Read only)
	D[5:4]	SELECTED MSTLINK	00	Link 0 selected as master link	(Read only)
			01	Link 1 selected as master link	
			10	Link 2 selected as master link	
			11	Link 3 selected as master link	
	D[3:0]	—	XXXX	Reserved	(Read only)
0xFC	D[7:0]	—	00000000	Reserved	00000000
0xFD	D[7:0]	—	00000000	Reserved	00000000
0xFE	D[7:0]	—	00000000	Reserved	00000000
0xFF	D[7:0]	—	0000XXXX	Reserved	0000XXXX (Read only)

Typical Application Circuit



NOTE: NOT ALL PULLUP/PULLDOWN RESISTORS ARE SHOWN. SEE PIN DESCRIPTION FOR DETAILS.

4x CAMERA APPLICATION

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9286GGN/VY+*	-40°C to +105°C	56 QFND-EP**
MAX9286GTN+	-40°C to +105°C	56 TQFN-EP**
MAX9286GTN/V+*	-40°C to +105°C	56 TQFN-EP**

/V denotes an automotive qualified product.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**Future product—Contact factory for availability.*
***EP = Exposed pad.*

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
56 QFND-EP	G5688Y+1	21-0704	90-0423
56 TQFN-EP	T5688+2	21-0135	90-0046

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/15	Initial release	—

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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