Digital Systems Track	Course Code: CND 212 Digital Testing and Verification	Project #1

Supervisor:

Dr. Khaled Salah

Project Title: A Generic Migration from Verilog to SystemVerilog

In this project, students will convert their previous Verilog course project into SystemVerilog for design and build a SystemVerilog testbench for it. This will involve updating the design code to SystemVerilog syntax and incorporating new features offered by SystemVerilog such as interfaces, classes, constrained-random stimulus generation, and coverage-driven verification methodologies.

Number of Students:

Group of 2-6 students

Assessment Criteria:

- **Conversion Accuracy**: How accurately and effectively the Verilog code was converted to SystemVerilog.
- **Utilization of SystemVerilog Features**: Evaluation of the usage of SystemVerilog constructs like interfaces, classes, randomization, assertions, and coverage.
- **Testbench Completeness**: Assessing the comprehensiveness and effectiveness of the SystemVerilog testbench in verifying the functionality of the design.
- **Functional Verification**: How well the testbench verifies the functionality of the design under different scenarios.
- **Simulation Results and Coverage**: Analysis of simulation results and coverage metrics to ensure thorough testing.

Best of Luck!

Digital Systems Track	Course Code: CND 212 Digital Testing and Verification	Project #2

Supervisor:

Dr. Omar Eldash

Project Title: Verification of SPI slave IP with systemVerilog

In this project, students will test an SPI slave IP using systemVerilog. This will involve using an actual IP or an abstract model as the test will assume a black box approach. The testing will be incorporating new features offered by SystemVerilog such as interfaces, classes, constrained-random stimulus generation, and coverage-driven verification methodologies. You will be required to show different test scenarios for the Slave IP showing modularity and reusability of the test environment.

Number of Students:

Group of 2-6 students

Assessment Criteria:

- Utilization of SystemVerilog Features: Evaluation of the usage of SystemVerilog constructs like interfaces, classes, randomization, assertions, and coverage.
- Testbench Completeness: Assessing the comprehensiveness and effectiveness of the SystemVerilog testbench in verifying the functionality of the design.
- Functional Verification: How well the testbench verifies the functionality of the design under different scenarios.
- Simulation Results and Coverage: Analysis of simulation results and coverage metrics to ensure thorough testing.

Best of Luck!

Digital Systems Track	Course Code: CND 212 Digital Testing and Verification	Project #3

Supervisor:

Eng. Randa Aboudeif, Dr. Ahmed Saeed

Project Title: UVM Verification of ALU Design

The main aim of this project is to take the trainee through the complete verification flow to generate a working UVM testbench for a simple IP using the UVM (Universal Verification Methodology) Framework.

Project Requirements:

In this project, the trainees are required to build a complete UVM and SystemVerilog testbench using Synopsys tools for the open-source ALU design available at: https://shorturl.at/lvwX6 through the following steps:

1. Verification plan
   - The design specification and testbench architecture.
   - Design under test (DUT) interface with the testbench.
   - The testing scenarios and Coverpoints in functional coverage.
2. SystemVerilog code for the UVM Testbench with constrained random stimulus generation.
3. Functional coverage analysis.
4. Code coverage reporting.
5. Simulation results for different testing scenarios.

Number of Students:

Group of 2-5 students

Assessment Criteria:

- Understanding the design specifications and planning for features to be verified (20%)
- Testbench Development using UVM and SystemVerilog capabilities such as TLM, constrained randomization, coverage features, DUT integration. (40%)
- Testbench and testing scenarios efficiency for verifying the design functionality. (25%)
- Simulation results analysis including UVM reports, functional, and code coverage. (15%)

Best of Luck!