嵌入式系统

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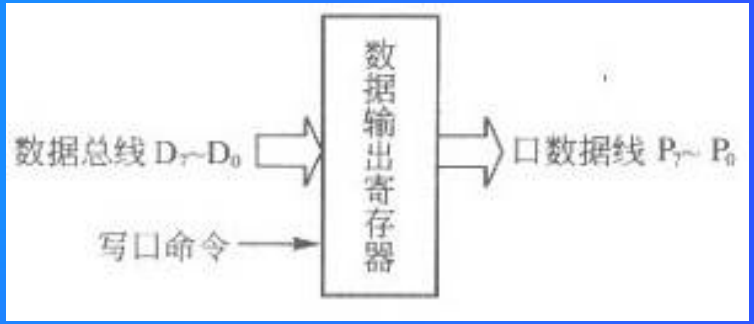
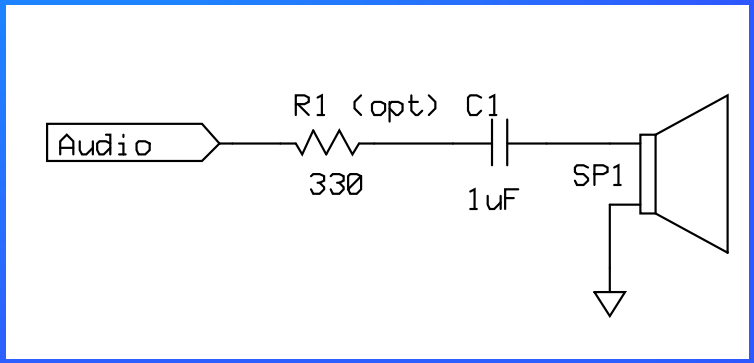
General Purpose IOs

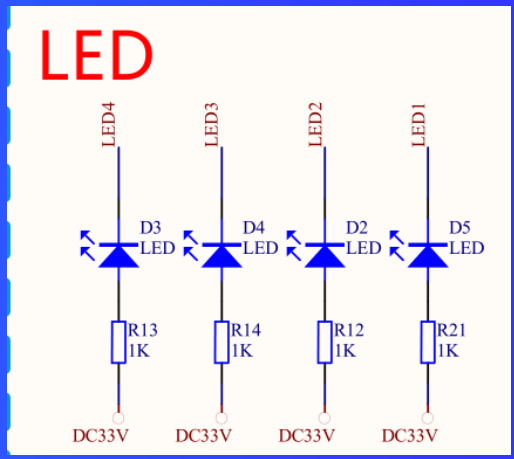
通用并行I/O接口

并行传输及其接口

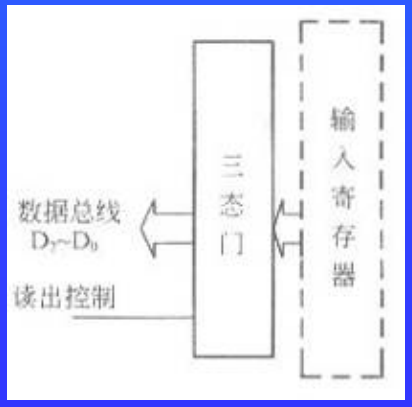
- 简单并行口
  - 简单输出口

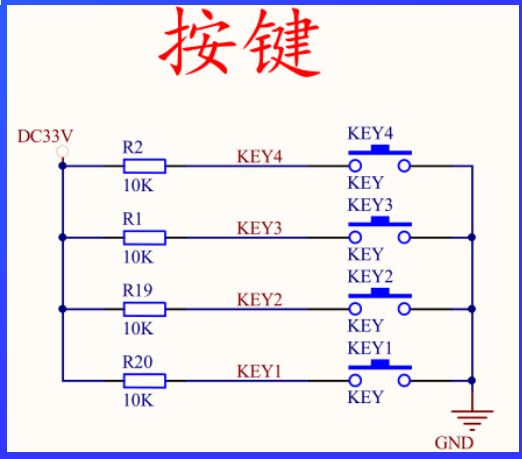






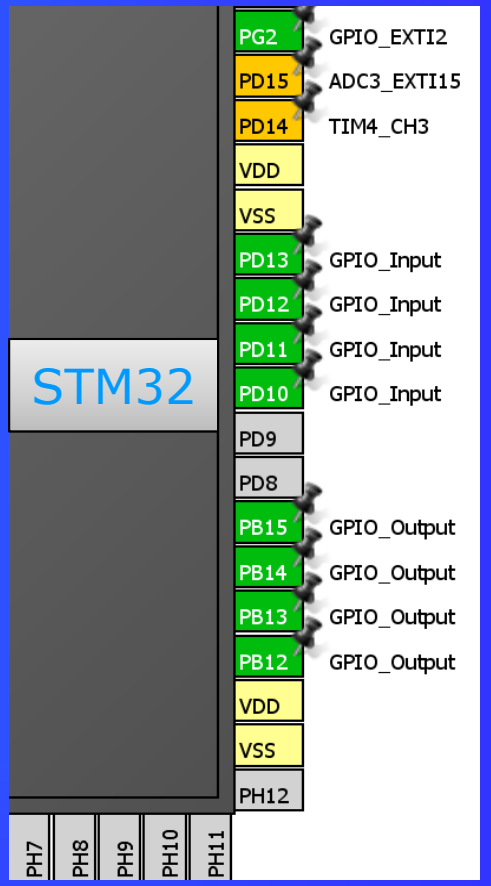
  - 简单输入口





STM32的GPIO接口

- 通用输入输出接口GPIO
  - 用户可以通过编程灵活的对接口进行控制
- GPIO被分成多组，每组最多有16个引脚
  - STM32F407IGT6：
    - GPIOA、GPIOB、GPIOC至GPIOI共9个GPIO端口（port）
    - 所有GPIO引脚都有：
      - 基本的输入输出功能
      - 可选功能（alternate function）



GPIO main features

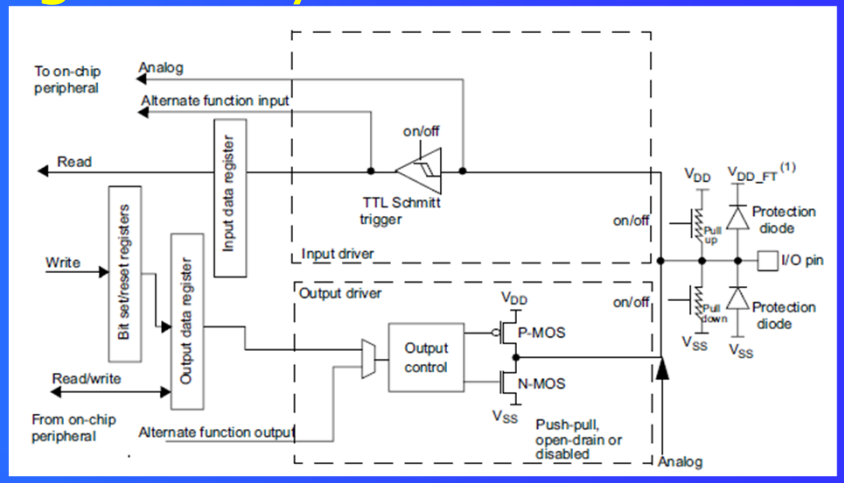
- 最多16个可控I/O管脚
  - 多路复用技术，I/O管脚可以用作GPIO或多种外设功能管脚之一
  - Alternate function input/output selection registers (at most 16 AFs per I/O)
  - 支持模拟功能
- 输出
  - 状态:
    - 推挽（push-pull）
    - 开漏（open drain） + 上拉/下拉（pull-up/down）
  - 通过output data register （GPIOx_ODR）或外设（alternate function output）输出数据
- 输入
  - 状态
    - 悬空（floating）
    - 上拉/下拉（pull-up/down）
    - 模拟（analog）
  - 通过input data register（GPIOx_IDR）或外设（alternate function input）输入数据

GPIO main features

- 对GPIOx_ODR的位写入操作
  - 位置位和位复位寄存器（Bit set and reset register, GPIOx_BSRR）用于
- 锁定机制（GPIOx_LCKR寄存器）可以冻结I/O配置
- 每个I/O管脚可以选择支持的速率
- 高速切换，每两个时钟周期改变状态

GPIO工作模式

- Each port bit of the general-purpose I/O (GPIO) ports can be individually configured by software in several modes:
  - Input floating 输入浮空
  - Input pull-up 输入上拉
  - Input-pull-down 输入下拉
  - Analog 模拟输入



- Output open-drain with pull-up or pull-down capability
- Output push-pull with pull-up or pull-down capability
- Alternate function push-pull with pull-up or pull-down capability
- Alternate function open-drain with pull-up or pull-down capability

开漏输出 推挽复用功能

推挽输出 开漏复用功能

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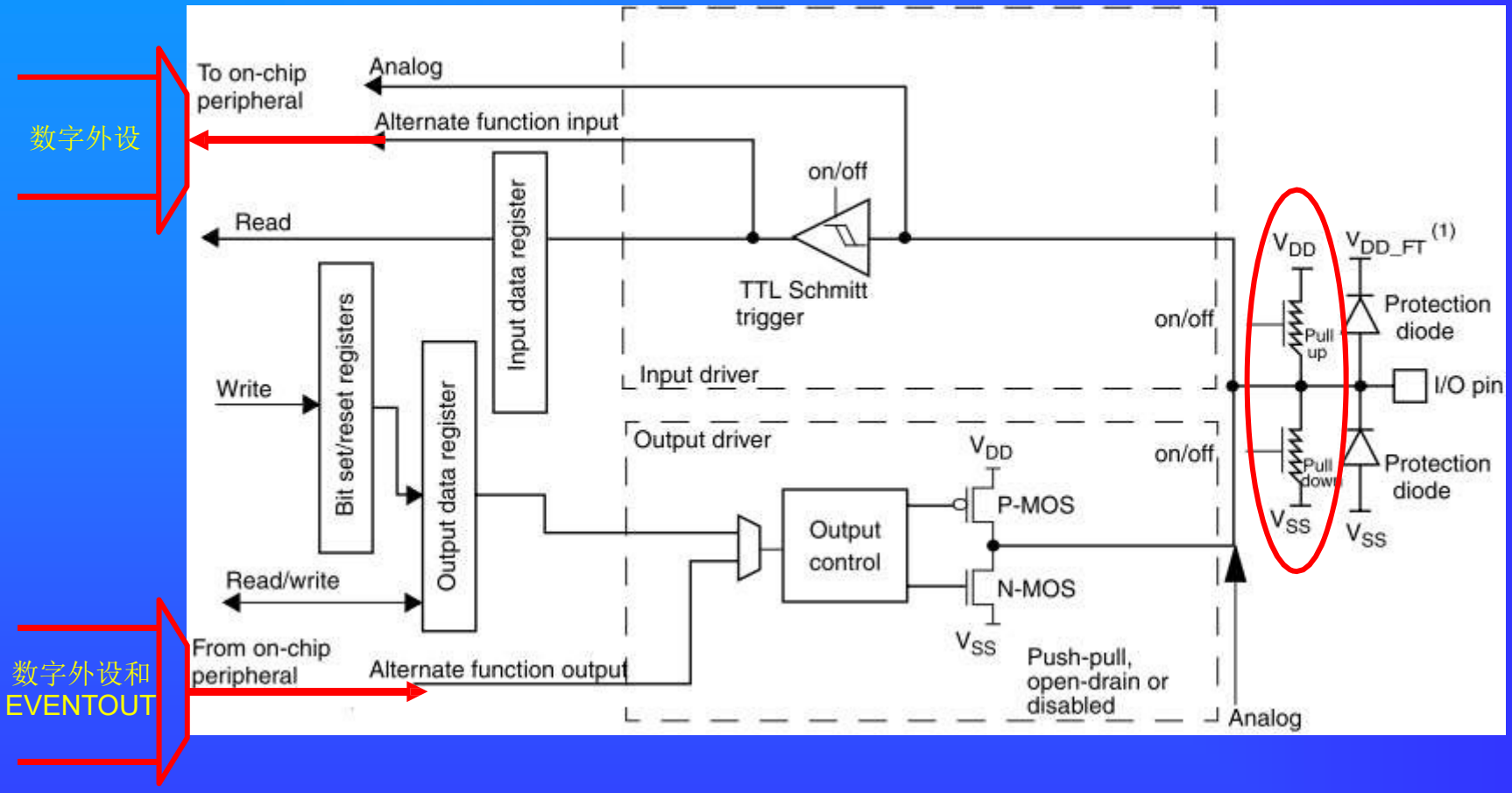
GPIO结构框图



复位之后，JTAG引脚是“输入上/下拉”模式，其他I/O引脚默认是“浮空输入”模式

GPIO寄存器

- Each general-purpose I/O port has:
  - four 32-bit configuration registers
    - GPIOx_MODER: mode register
    - GPIOx_OTYPER: output type register
    - GPIOx_OSPEEDR: output speed register
    - GPIOx_PUPDR: pull-up/pull-down register
  - two 32-bit data registers
    - GPIOx_IDR: input data register
    - GPIOx_ODR: output data register

GPIO寄存器

- Each general-purpose I/O port has:
  - four 32-bit configuration registers
  - two 32-bit data registers
  - a 32-bit set/reset register
    - GPIOx_BSRR: bit set/reset register
  - a 32-bit locking register
    - GPIOx_LCKR
  - two 32-bit alternate function selection register
    - GPIOx_AFRH: alternate function high register
    - GPIOx_AFRL: alternate function low register

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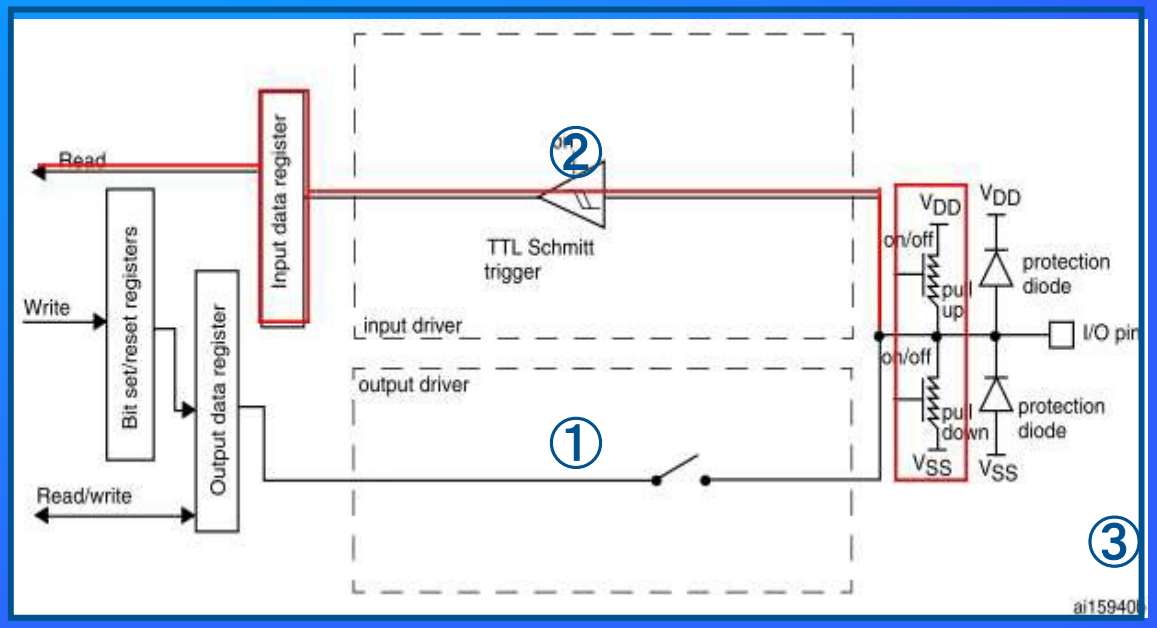
输入模式（MODER=00）



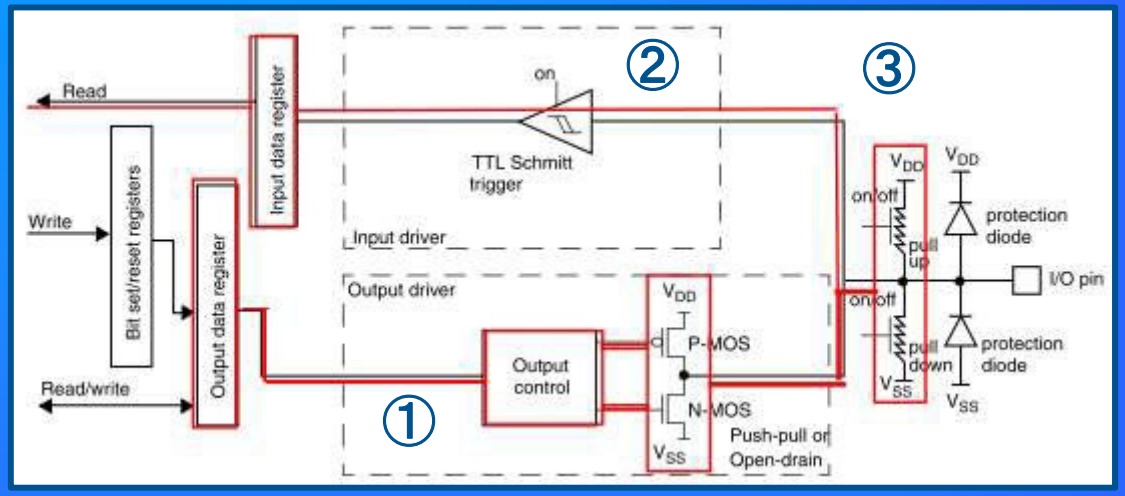
① 输出驱动关闭

② Schmit触发输入激活

③上/下拉电阻是否激活取决于GPIOx_PUPDR

- 根据上下拉电阻是否激活，可以分为
  - 浮空输入、上拉输入、下拉输入
- GPIO模块在AHB1总线上，每个AHB1时钟周期，采样一次I/O引脚上的电平，送入输入数据寄存器
  - 读取GPIO_IDR可得到引脚上的电平状态

GPIO输出模式（MODER=01）



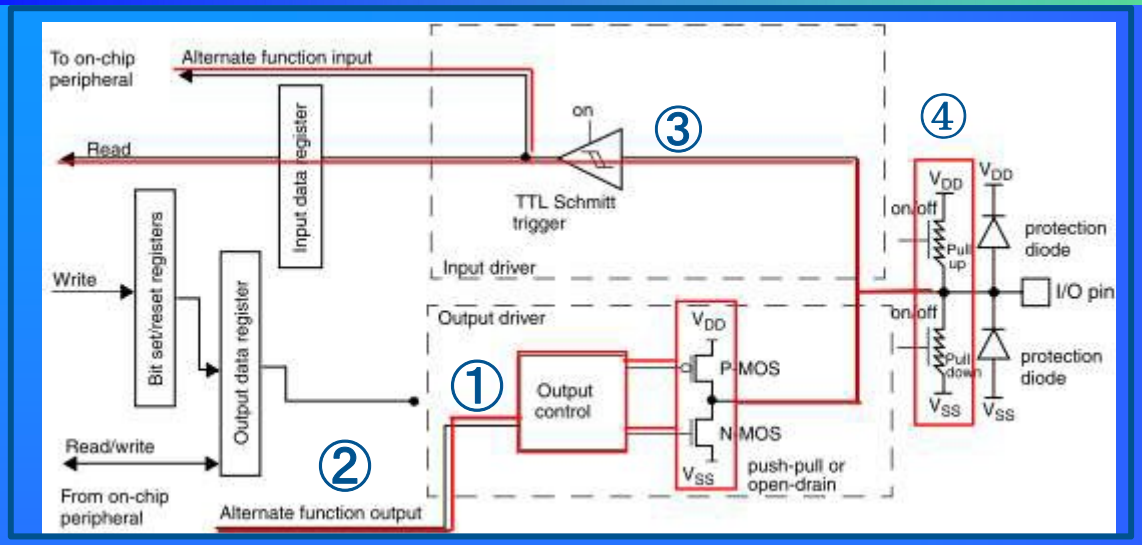
① 输出驱动打开，推挽/开漏取决于GPIOx_OTYPER

② Schmit触发输入激活

③上/下拉电阻是否激活取决于GPIOx_PUPDR

- 根据P-MOS是否激活，可分为
  - 推挽输出、开漏输出
- 每个AHB1时钟周期，采样一次I/O引脚上的电平，送入输入数据寄存器
  - 读取GPIO_IDR可得到引脚的当前电平
- 读取输出数据寄存器GPIO_ODR只能得到上次在推挽模式下输出的值
  - 开漏模式下软件写1，I/O引脚电平取决于外部电路

可选功能模式（MODER=10）



① 输出驱动打开，推挽/开漏取决于GPIOx_OTYPER

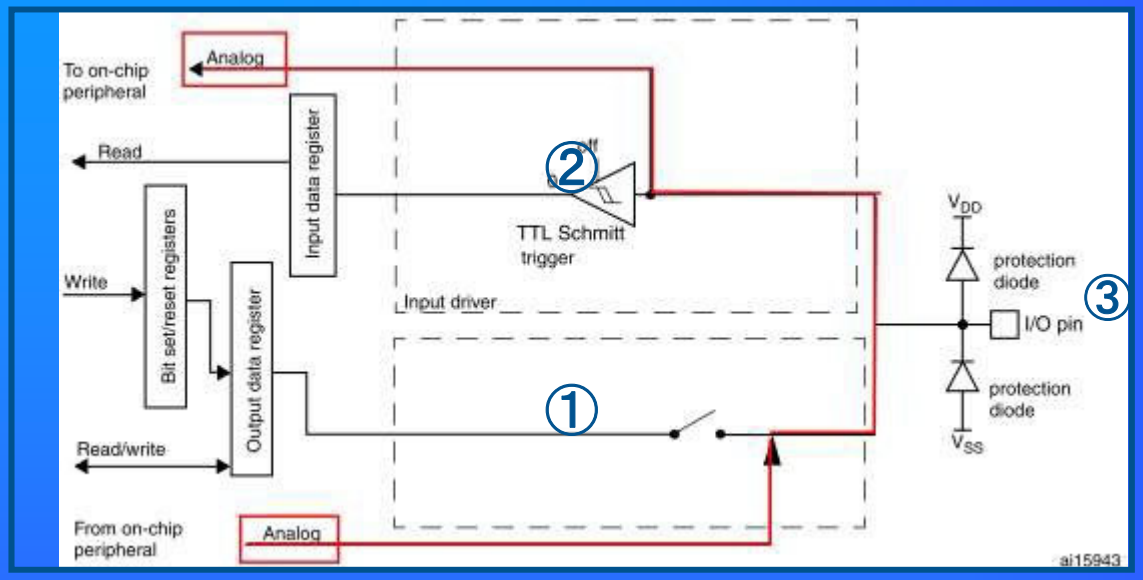
② 输出电路由片上外设驱动

③ Schmit触发输入激活

④上/下拉电阻是否激活取决于GPIOx_PUPDR

- 输出信号仅来自片上数字外设，根据P-MOS是否激活可分为
  - 推挽输出、开漏输出
- I/O引脚上的信号可以输入到片上数字外设和GPIO_IDR
  - 每个AHB1时钟周期采样一次I/O引脚上的电平，送入输入数据寄存器
  - 读取GPIO_IDR可得到引脚上的电平状态

模拟功能模式（MODER=11）



① 输出驱动关闭

② Schmit触发输入关闭

③上/下拉电阻被禁止

- Schmitt触发器关闭
  - 该引脚功耗为0
  - 触发器输出强制为常数0
- 读取输入数据寄存器始终得到”0”
- 模拟功能配置下，I/O引脚不是5V友好的

GPIO引脚模式小结

	MODER	输出信号来自…		引脚电平信息输入到…	施密特触发器	PU/PDR
		OTYPER：配置推挽输出或开漏输出	OSPEEDR：配置GPIO输出带宽			
输入模式	00			GPIO_IDR	激活	配置内部弱上拉、弱下拉或浮空
输出模式	01	GPIO_ODR		GPIO_IDR		
可选功能模式	10	片上数字外设		外设和GPIO_IDR		
模拟功能	11	片上模拟外设：ADC/DAC		ADC/DAC	关闭	关闭

- 橘黄色框：对应寄存器无效
- 红色框：芯片以AHB1时钟频率采样引脚电平状态，送入输入数据寄存器
- 蓝色框：只有这两个模式输出驱动被打开，输出信号分别来自输出数据寄存器和片上数字外设
  - 需要配置：
    - 推挽或开漏输出
    - 输出带宽(2MHz、25MHz、50MHz和100MHz)

GPIO Configuration Modes

MODER(i) [1:0]	OTYPER(i)	PUPDR(i) [1:0]		I/O configuration
01	0	0	0	Output Push Pull
		0	1	Output Push Pull with Pull-up
		1	0	Output Push Pull with Pull-down
	1	0	0	Output Open Drain
		0	1	Output Open Drain with Pull-up
		1	0	Output Open Drain with Pull-down
10	0	0	0	Alternate Function Push Pull
		0	1	Alternate Function PP Pull-up
		1	0	Alternate Function PP Pull-down
	1	0	0	Alternate Function Open Drain
		0	1	Alternate Function OD Pull-up
		1	0	Alternate Function OD Pull-down
00	x	0	0	Input floating
		0	1	Input with Pull-up
		1	0	Input with Pull-down
11	x	x		**Analog mode**

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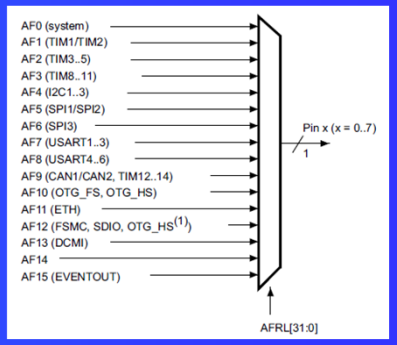
* In output mode, the I/O speed is configurable through OSPEEDR register: 2MHz, 10MHz or 50MHz

可选功能多路选择器

- 每个引脚都有一个多路复用选择器，决定哪一个外设功能连到该引脚
- 每个多路选择器有16路输入可供选择
  - AF0：系统功能（复位后复用选择器的默认连接）
    - JTAG/SWD，MCO1/2，RTC_50Hz
  - AF1~13：各种数字外设功能
  - AF14：保留
  - AF15：Cortex-M4 EVENTOUT



- 每个数字外设功能可以映射到多个I/O引脚
  - 具体映射关系参考数据手册(可编程功能映射表)
  - 映射以单个引脚为单位

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Alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/I2S2/I2S2ext	SPI3/I2Sext/I2S3	USART1/2/3/I2S3ext	UART4/5/USART6	CAN1/2 TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/OTG_FS	DCMI		
Port A	PA0	-	TIM2_CH1_ETR	TIM 5_CH1	TIM8_ETR	-	-	-	USART2_CTS	UART4_TX	-	-	ETH_MII_CRS	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS	UART4_RX	-	-	ETH_MII_RX_CLK ETH_RMII__REF_CLK	-	-	-	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_TX	-	-	-	ETH_MDIO	-	-	-	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	USART2_RX	-	-	OTG_HS_ULPI_D0	ETH _MII_COL	-	-	-	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK	-	-	-	-	OTG_HS_SOF	DCMI_HSYNC	-	EVENTOUT
	PA5	-	TIM2_CH1_ETR	-	TIM8_CH1N	-	SPI1_SCK	-	-	-	-	OTG_HS_ULPI_CK	-	-	-	-	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	-	-	TIM13_CH1	-	-	-	DCMI_PIXCK	-	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI	-	-	-	TIM14_CH1	-	ETH_MII_RX_DV ETH_RMII_CRS_DV	-	-	-	EVENTOUT
	PA8	MCO1	TIM1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	-	-	-	-	EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	-	-	USART1_TX	-	-	-	-	-	DCMI_D0	-	EVENTOUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX	-	-	OTG_FS_ID	-	-	DCMI_D1	-	EVENTOUT
	PA11	-	TIM1_CH4	-	-	-	-	-	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	-	EVENTOUT
	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS	-	CAN1_TX	OTG_FS_DP	-	-	-	-	EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM 2_CH1 TIM 2_ETR	-	-	-	SPI1_NSS	SPI3_NSS/I2S3_WS	-	-	-	-	-	-	-	-	EVENTOUT

Alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/I2S2/I2S2ext	SPI3/I2Sext/I2S3	USART1/2/3/I2S3ext	UART4/5/USART6	CAN1/2 TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/OTG_FS	DCMI		
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-	-	-	OTG_HS_ULPI_D1	ETH _MII_RXD2	-	-	-	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N		-	-	-	-	-	OTG_HS_ULPI_D2	ETH _MII_RXD3	-	-	-	EVENTOUT
	PB2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB3	JTDO/TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK I2S3_CK	-	-	-	-	-	-	-	-	EVENTOUT
	PB4	NJTRST	-	TIM3_CH1		-	SPI1_MISO	SPI3_MISO	I2S3ext_SD	-	-	-	-	-	-	-	EVENTOUT
	PB5	-	-	TIM3_CH2		I2C1_SMBA	SPI1_MOSI	SPI3_MOSI I2S3_SD		-	CAN2_RX	OTG_HS_ULPI_D7	ETH _PPS_OUT	-	DCMI_D10	-	EVENTOUT
	PB6	-	-	TIM4_CH1		I2C1_SCL	-	-	USART1_TX	-	CAN2_TX	-	-	-	DCMI_D5	-	EVENTOUT
	PB7	-	-	TIM4_CH2		I2C1_SDA	-	-	USART1_RX	-	-	-	-	FSMC_NL	DCMI_VSYNC	-	EVENTOUT
	PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	-	-	-	CAN1_RX	-	ETH _MII_TXD3	SDIO_D4	DCMI_D6	-	EVENTOUT
	PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS I2S2_WS	-	-	-	CAN1_TX	-	-	SDIO_D5	DCMI_D7	-	EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK I2S2_CK	-	USART3_TX	-	-	OTG_HS_ULPI_D3	ETH_ MII_RX_ER	-	-	-	EVENTOUT
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH _MII_TX_EN ETH _RMII_TX_EN	-	-	-	EVENTOUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS I2S2_WS	-	USART3_CK	-	CAN2_RX	OTG_HS_ULPI_D5	ETH _MII_TXD0 ETH _RMII_TXD0	OTG_HS_ID	-	-	EVENTOUT
	PB13	-	TIM1_CH1N	-	-	-	SPI2_SCK I2S2_CK	-	USART3_CTS	-	CAN2_TX	OTG_HS_ULPI_D6	ETH _MII_TXD1 ETH _RMII_TXD1	-	-	-	EVENTOUT
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	-	SPI2_MISO	I2S2ext_SD	USART3_RTS	-	TIM12_CH1	-	-	OTG_HS_DM	-	-	EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI I2S2_SD	-	-	-	TIM12_CH2	-	-	OTG_HS_DP	-	-	EVENTOUT

Alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/I2S2/I2S2ext	SPI3/I2Sext/I2S3	USART1/2/3/I2S3ext	UART4/5/USART6	CAN1/2 TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/OTG_FS	DCMI		
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS I2S2_WS	-	-	-	-	-	-	-	DCMI_D13	-	EVENTOUT
	PI1	-	-	-	-	-	SPI2_SCK I2S2_CK	-	-	-	-	-	-	-	DCMI_D8	-	EVENTOUT
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	I2S2ext_SD	-	-	-	-	-	-	DCMI_D9	-	EVENTOUT
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI I2S2_SD	-	-	-	-	-	-	-	DCMI_D10	-	EVENTOUT
	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	-	-	DCMI_D5	-	EVENTOUT
	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	-	-	-	DCMI_VSYNC	-	EVENTOUT
	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	-	-	-	DCMI_D6	-	EVENTOUT
	PI7	-	-	-	TIM8_CH3	-	-	-	-	-	-	-	-	-	DCMI_D7	-	EVENTOUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PI9	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	-	-	-	EVENTOUT
	PI10	-	-	-	-	-	-	-	-	-	-	-	ETH _MII_RX_ER	-	-	-	EVENTOUT
	PI11	-	-	-	-	-	-	-	-	-	-	OTG_HS_ULPI_DIR	-	-	-	-	EVENTOUT

I/O引脚的使用：GPIO

- 配置方向
  - 输入方向
    - GPIOx_MODER = 00
  - 输出方向
    - GPIOx_MODER = 01
- 输入管脚
  - 配置上/下拉电阻
    - GPIOx_PUPDR
- 输出管脚
  - 选择推挽/开漏、上/下拉和输出速度
    - GPIOx_OTYPER、GPIOx_PUPDR、GPIOx_OSPEEDER

MODER(i) [1:0]	OTYPER(i)	OSPEEDR(i) [B:A]		PUPDR(i) [1:0]		I/O configuration	
01	0	SPEED [B:A]		0	0	GP output	PP
	0			0	1	GP output	PP + PU
	0			1	0	GP output	PP + PD
	0			1	1	Reserved	
	1			0	0	GP output	OD
	1			0	1	GP output	OD + PU
	1			1	0	GP output	OD + PD
	1			1	1	Reserved (GP output OD)	
00	x	x	x	0	0	Input	Floating
	x	x	x	0	1	Input	PU
	x	x	x	1	0	Input	PD
	x	x	x	1	1	Reserved (input floating)	

I/O引脚的使用：外设功能

- 模拟外设ADC/DAC
  - 配置成模拟模式
    - GPIOx_MODER = 11
  - 关闭上/下拉电阻
    - GPIOx_PUPDR = 00

MODER(i) [1:0]	OTYPER(i)	OSPEEDR(i) [B:A]		PUPDR(i) [1:0]		I/O configuration	
10	0	SPEED [B:A]		0	0	AF	PP
	0			0	1	AF	PP + PU
	0			1	0	AF	PP + PD
	0			1	1	Reserved	
	1			0	0	AF	OD
	1			0	1	AF	OD + PU
	1			1	0	AF	OD + PD
	1			1	1	Reserved	
11	x	x	x	0	0	Input/output	Analog
	x	x	x	0	1	Reserved	
	x	x	x	1	0		
	x	x	x	1	1		

- 数字外设
  - 配置成可选功能模式
    - GPIOx_MODER = 10
  - 选择推挽/开漏、上/下拉和输出速度
    - GPIOx_OTYPER、GPIOx_PUPDR、GPIOx_OSPEEDER
  - 配置多路选择器，把使用到的外设连到对应引脚
    - GPIOx_AFRL或者GPIOx_AFRH

I/Os special considerations

- 上电复位过程及复位之后：
  - 可选功能未激活，I/O端口均配置为输入浮空模式
  - debug pins （JTAG/SWD) are in AF pull-up/pull-down after reset:
    - PA13: JTMS/SWDIO
    - PA14: JTCK/SWCLK
    - PA15: JTDI
    - PB3: JTDO
    - PB4: NJTRST

GPIO引脚分布

	R(64pin)	V(100pin)	Z(144pin)	I(176pin)
PortA (16)	3	5	7	9
PortB (16)				
PortC (16)				
PortD (16)	PD.2			
PortE (16)				
PortF (16)				
PortG (16)				
PortH (16)	PH0/1(OSC)	PH0/1(OSC)	PH0/1(OSC)	
PortI (12)				
总共引脚数目	48+1+2=51	80+2=82	112+2=114	128+12=140

GPIO占芯片所有引脚的**80%**左右

GPIO寄存器

- Each general-purpose I/O port has:
  - four 32-bit configuration registers
    - GPIOx_MODER: mode register
    - GPIOx_OTYPER: output type register
    - GPIOx_OSPEEDR: output speed register
    - GPIOx_PUPDR: pull-up/pull-down register
  - two 32-bit data registers
    - GPIOx_IDR: input data register
    - GPIOx_ODR: output data register
  - a 32-bit set/reset register
    - GPIOx_BSRR: bit set/reset register
  - a 32-bit locking register
    - GPIOx_LCKR
  - two 32-bit alternate function selection register
    - GPIOx_AFRH: alternate function high register
    - GPIOx_AFRL: alternate function low register

GPIO寄存器MODER（mode register）

- GPIO端口模式寄存器 (GPIOx_MODER) (x = A..I)
  - 偏移地址：0x00
  - 复位值： 0xA800 0000（端口 A）；0x0000 0280（端口 B）；0x0000 0000（其它端口）
  - Bits 2y:2y+1 MODERy[1:0]
    - Port x configuration bits y (y= 0..15)
      - 00: Input (reset state)
      - 01: General purpose output mode
      - 10: Alternate function mode
      - 11: Analog mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODER15[1:0]		MODER14[1:0]		MODER13[1:0]		MODER12[1:0]		MODER11[1:0]		MODER10[1:0]		MODER9[1:0]		MODER8[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODER7[1:0]		MODER6[1:0]		MODER5[1:0]		MODER4[1:0]		MODER3[1:0]		MODER2[1:0]		MODER1[1:0]		MODER0[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

GPIO寄存器OTYPER（output type register）

- GPIO端口输出类型寄存器 (GPIOx_OTYPER) (x = A..I)
  - 偏移地址： 0x04
  - 复位值： 0x0000 0000
  - Bits 31:16: Reserved
  - Bits 15:0: OTy
    - Port x configuration bits y (y = 0..15)
      - 0: Output push-pull 推挽输出(reset state)
      - 1: Output open-drain开漏输出

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OT15	OT14	OT13	OT12	OT11	OT10	OT9	OT8	OT7	OT6	OT5	OT4	OT3	OT2	OT1	OT0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

GPIO寄存器OSPEEDR（output speed register）

- GPIO端口输出速度寄存器 (GPIOx_OSPEEDR) (x = A..I/)
  - 偏移地址：0x08
  - 复位值：0x0C00 0000（端口A）；0x0000 00C0（端口 B）;0x0000 0000（其它端口）
  - Bits 2y:2y+1:OSPEEDRy[1:0]
    - Port x configuration bits y (y = 0..15)
      - 00: Low speed：一般情况下选用，如LED、按键等
      - 01: Medium speed
      - 10: High speed
      - 11: Very high speed

输出速度：I/O口驱动电路的响应速度
不是输出信号的速度
输出信号的速度：取决于软件程序

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OSPEEDR15[1:0]		OSPEEDR14[1:0]		OSPEEDR13[1:0]		OSPEEDR12[1:0]		OSPEEDR11[1:0]		OSPEEDR10[1:0]		OSPEEDR9[1:0]		OSPEEDR8[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OSPEEDR7[1:0]		OSPEEDR6[1:0]		OSPEEDR5[1:0]		OSPEEDR4[1:0]		OSPEEDR3[1:0]		OSPEEDR2[1:0]		OSPEEDR1[1:0]		OSPEEDR0[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

GPIO寄存器PUPDR（pull-up/pull-down register）

- GPIO端口上拉/下拉寄存器 (GPIOx_PUPDR) (x = A..I/)
  - 偏移地址：0x0C
  - 复位值：0x6400 0000（端口 A）;0x0000 0100（端口 B）;0x0000 0000（其它端口）
  - Bits 2y:2y+1: PUPDRy[1:0]
    - Port x configuration bits y (y = 0..15)
      - 00: No pull-up, pull-down
      - 01: Pull-up
      - 10: Pull-down
      - 11: Reserved

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PUPDR15[1:0]		PUPDR14[1:0]		PUPDR13[1:0]		PUPDR12[1:0]		PUPDR11[1:0]		PUPDR10[1:0]		PUPDR9[1:0]		PUPDR8[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PUPDR7[1:0]		PUPDR6[1:0]		PUPDR5[1:0]		PUPDR4[1:0]		PUPDR3[1:0]		PUPDR2[1:0]		PUPDR1[1:0]		PUPDR0[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

GPIO寄存器IDR（input data register）

- GPIO端口输入数据寄存器 (GPIOx_IDR) (x = A..I)
  - 偏移地址：0x10
  - 复位值：0x0000 XXXX（ X 表示未定义）
  - Bits 31:16 Reserved, must be kept at reset value.
  - Bits 15:0 IDRy
    - Port input data y (y = 0..15)
    - 只读，仅能通过字模式访问
    - 映射相应I/O管脚的输入电平

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDR15	IDR14	IDR13	IDR12	IDR11	IDR10	IDR9	IDR8	IDR7	IDR6	IDR5	IDR4	IDR3	IDR2	IDR1	IDR0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

GPIO寄存器ODR（output data register）

- GPIO端口输出数据寄存器 (GPIOx_ODR) (x = A..I)
  - 偏移地址：0x14
  - 复位值：0x0000 0000
  - Bits 31:16 Reserved, must be kept at reset value.
  - Bits 15:0 ODRy
    - Port output data (y = 0..15)
    - can be read and written by software

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ODR15	ODR14	ODR13	ODR12	ODR11	ODR10	ODR9	ODR8	ODR7	ODR6	ODR5	ODR4	ODR3	ODR2	ODR1	ODR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

GPIO寄存器BSRR（bit set/reset register）

- GPIO端口置位/复位寄存器 (GPIOx_BSRR) (x = A..I)
  - 偏移地址：0x18；复位值：0x0000 0000
  - Bits 31:16 BRy: Port x reset bit y (y = 0..15)
    - 0: 不改变相应ODRx位的值
    - 1: 相应ODRx位复位（清零）
    - 只写，可以通过字、半字或字节模式方式
      - 读操作始终返回0x0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BR15	BR14	BR13	BR12	BR11	BR10	BR9	BR8	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BS15	BS14	BS13	BS12	BS11	BS10	BS9	BS8	BS7	BS6	BS5	BS4	BS3	BS2	BS1	BS0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

GPIO寄存器BSRR（bit set/reset register）

- GPIO端口置位/复位寄存器 (GPIOx_BSRR) (x = A..I)
  - 偏移地址：0x18；复位值：0x0000 0000
  - Bits 31:16 BRy: Port x reset bit y (y = 0..15)
  - Bits 15:0 BSy: Port x set bit y (y= 0..15)
    - 0: 不改变相应ODRx位的值
    - 1: 相应ODRx位置位（置1）
    - 只写，可以通过字、半字或字节模式方式
      - 读操作始终返回0x0000
  - BSx和BRx同时为1时，BSx优先

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BR15	BR14	BR13	BR12	BR11	BR10	BR9	BR8	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BS15	BS14	BS13	BS12	BS11	BS10	BS9	BS8	BS7	BS6	BS5	BS4	BS3	BS2	BS1	BS0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

GPIO寄存器AFRL（alternate function low register）

- GPIO可选功能低寄存器 (GPIOx_AFRL) (x = A..I)
  - 偏移地址：0x20
  - 复位值：0x0000 0000
  - Bits 31:0 AFRLy
    - Alternate function selection for port x bit y (y = 0..7)
    - AFRLy selection:
      - 0000: AF0; 0001: AF1; 0010: AF2; 0011: AF3
      - 0100: AF4; 0101: AF5; 0110: AF6; 0111: AF7
      - 1000: AF8; 1001: AF9; 1010: AF10; 1011: AF11
      - 1100: AF12; 1101: AF13; 1110: AF14; 1111: AF15

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AFRL7[3:0]				AFRL6[3:0]				AFRL5[3:0]				AFRL4[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFRL3[3:0]				AFRL2[3:0]				AFRL1[3:0]				AFRL0[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

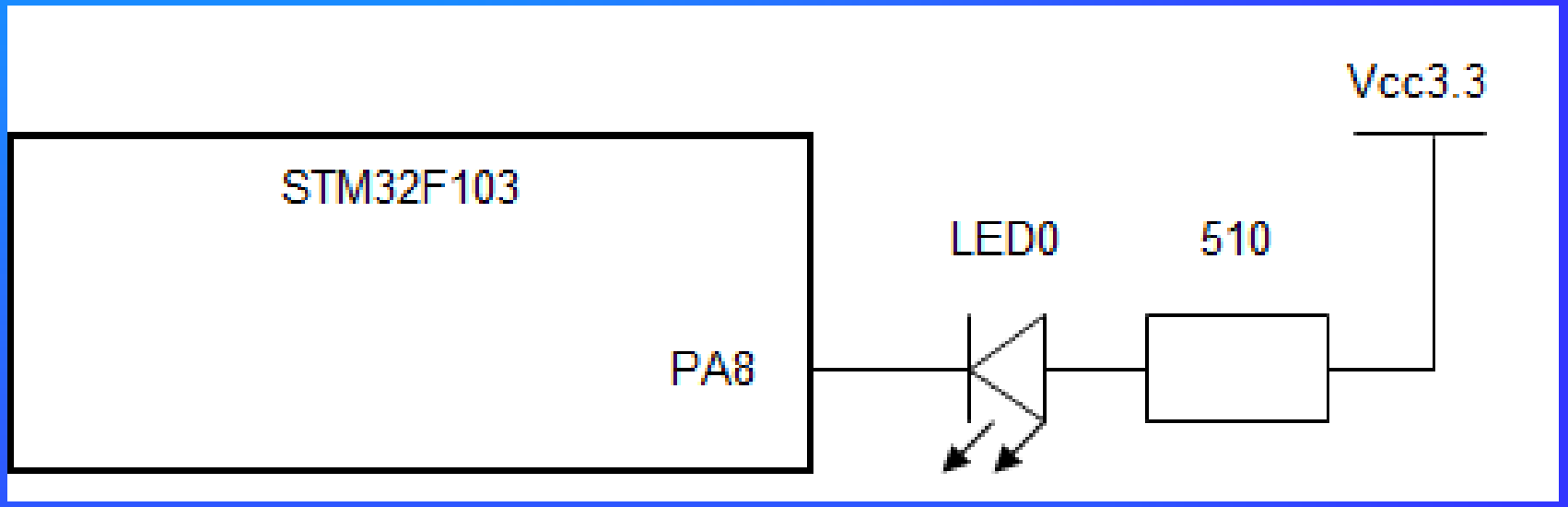
GPIO寄存器AFRH（alternate function high register）

- GPIO可选功能高寄存器 (GPIOx_AFRH) (x = A..I)
  - 偏移地址：0x24
  - 复位值：0x0000 0000
  - Bits 31:0 AFRHy
    - Alternate function selection for port x bit y (y = 8..15)
    - AFRHy selection:
      - 0000: AF0; 0001: AF1; 0010: AF2; 0011: AF3
      - 0100: AF4; 0101: AF5; 0110: AF6; 0111: AF7
      - 1000: AF8; 1001: AF9; 1010: AF10; 1011: AF11
      - 1100: AF12; 1101: AF13; 1110: AF14; 1111: AF15

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AFRH15[3:0]				AFRH14[3:0]				AFRH13[3:0]				AFRH12[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFRH11[3:0]				AFRH10[3:0]				AFRH9[3:0]				AFRH8[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

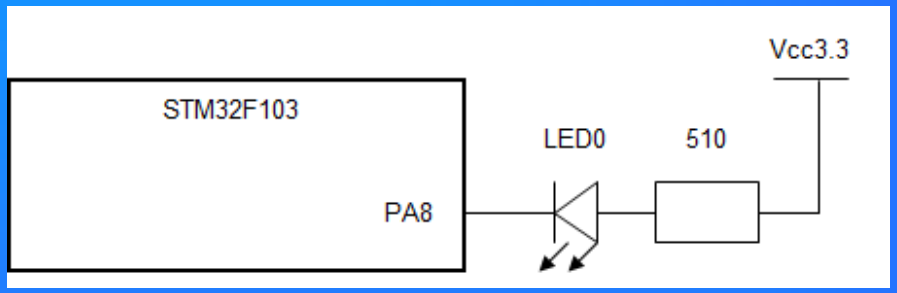
STM32F103—GPIO应用实例1

- LED闪烁

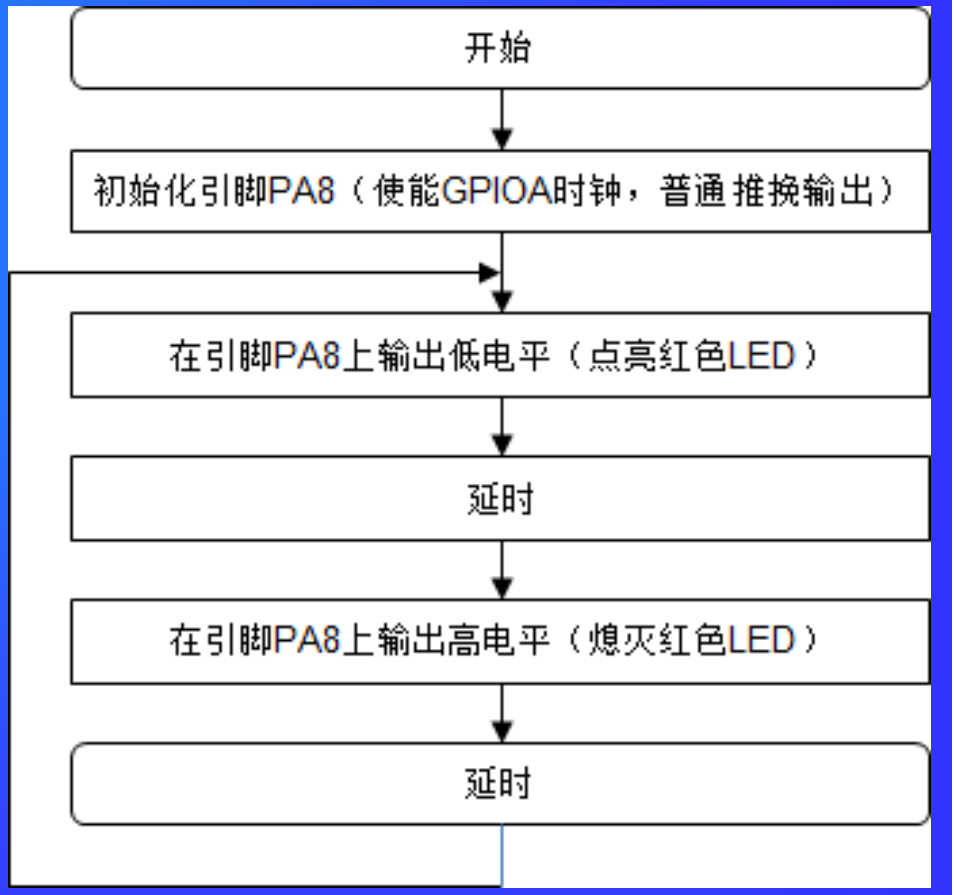


STM32F103—GPIO应用实例

LED闪烁

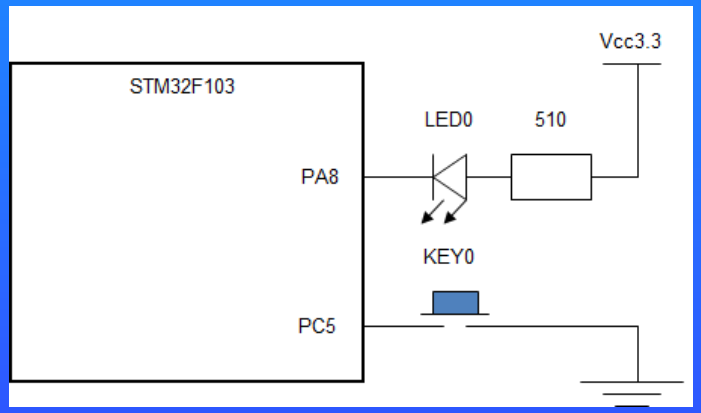


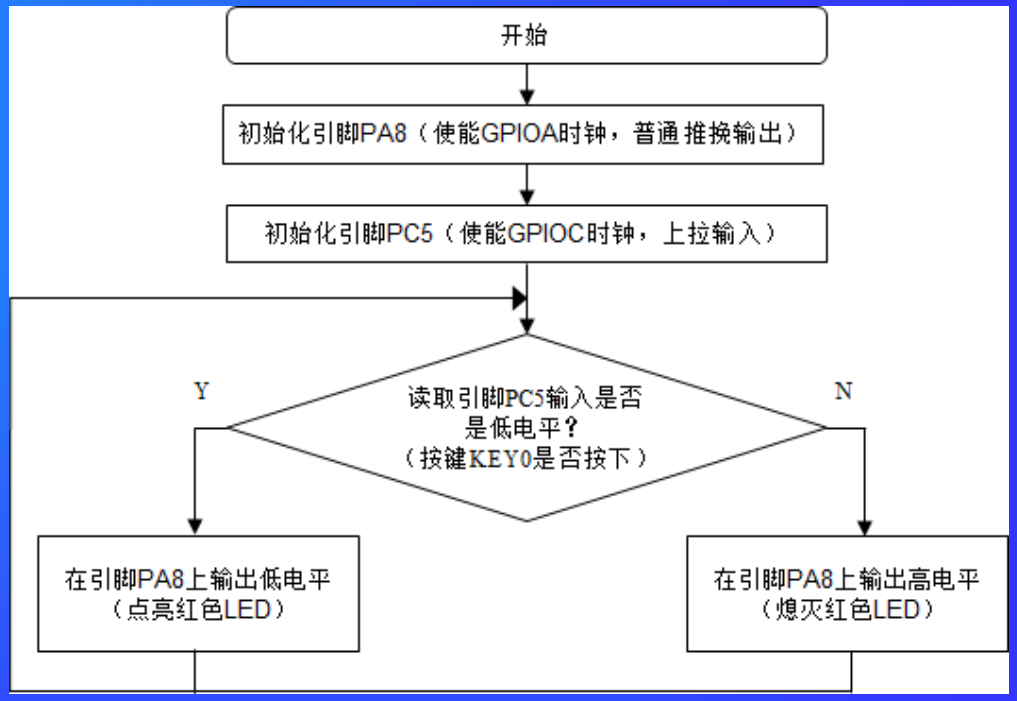
- 所有GPIO引脚，使用前必须先打开其所属端口时钟
  - 为降低功耗，每个外设都对应一个时钟，在上电时处于关闭状态
  - 所有GPIO都挂载到AHB1总线上，其时钟由AHB1外设时钟使能寄存器（RCC_AHB1ENR）控制



STM32F103—GPIO应用实例

- 按键控制LED亮灭





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