8255 Programmable Peripheral Interface
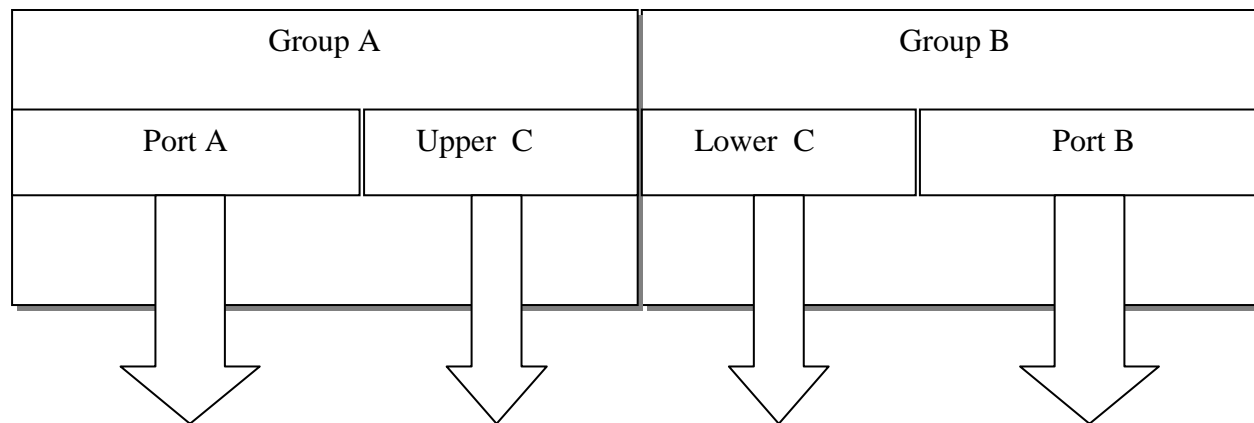
Programmable Peripheral Interface

- The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel microcomputer systems.

- Its function is to Interface peripheral equipment to the microcomputer system bus.
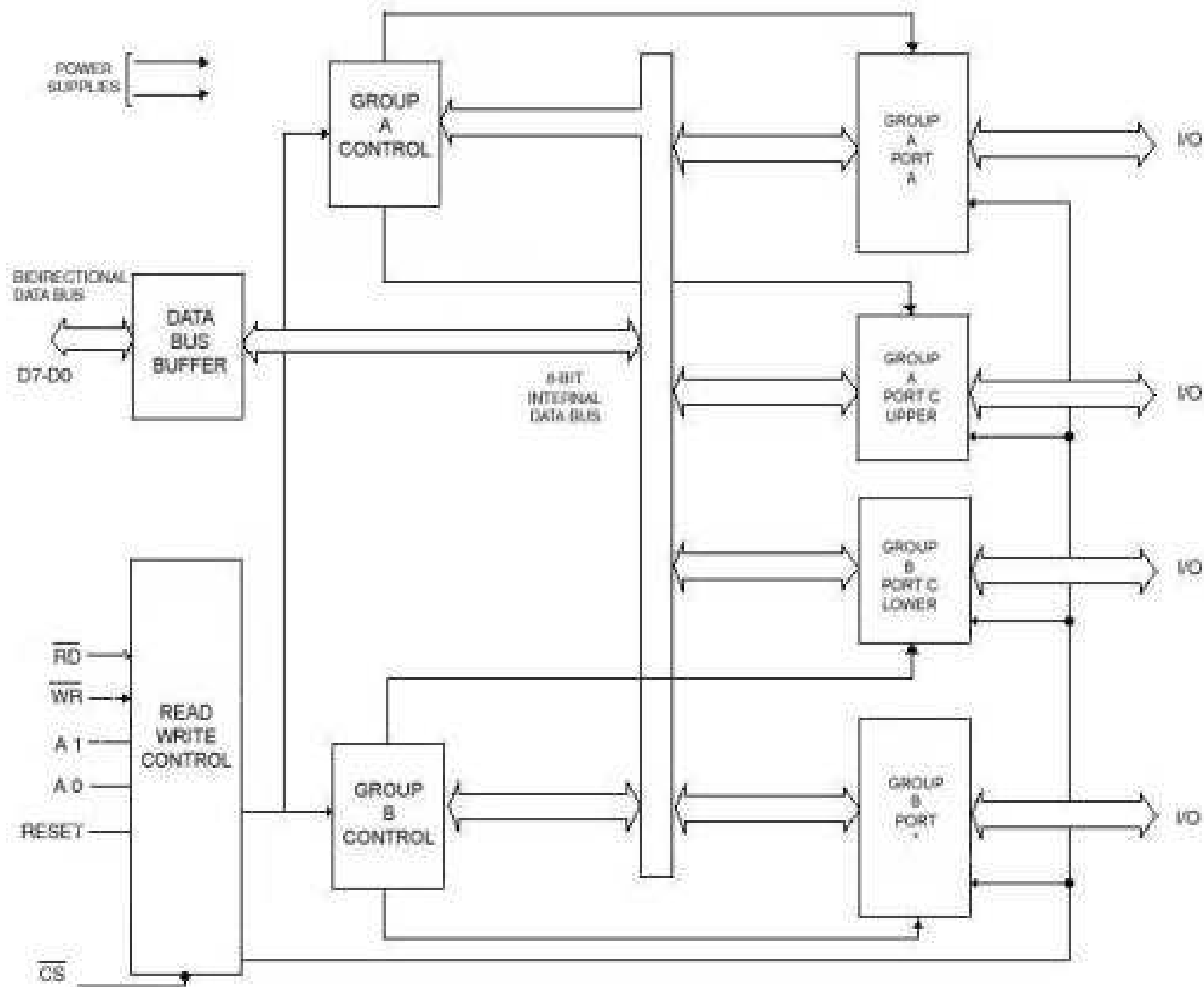
Programmable Peripheral Interface

- Intel 8255 has three 8-bit ports: Port A, B and C
- Ports A and B can be programmed as either input or output.
- Ports A and C can be used as bidirectional
- Port C can be programmed as a pair of 4-bit bidirectional control ports or individual lines can be set or reset

PPI cont…

- Control register controls the overall operation of 8255
- All three ports A, B and C are grouped into two

Group A		Group B	
Port A	Upper C	Lower C	Port B

POWER SUPPLIES

GROUP A CONTROL

GROUP A PORT A

I/O

BIDIRECTIONAL DATA BUS

D7-D0

DATA BUS BUFFER

8-BIT INTERNAL DATA BUS

GROUP A PORT C UPPER

I/O

GROUP B PORT C LOWER

I/O

RD

WR

A 1

A 0

RESET

READ WRITE CONTROL

GROUP B CONTROL

GROUP B PORT

I/O

CS

8255 PPI Chip Pinout

PA3 ☐ 1	40 ☐ PA4
PA2 ☐ 2	39 ☐ PA5
PA1 ☐ 3	38 ☐ PA6
PA0 ☐ 4	37 ☐ PA7
$\overline{RD}$ ☐ 5	36 ☐ $\overline{WR}$
$\overline{CS}$ ☐ 6	35 ☐ RESET
GND ☐ 7	34 ☐ D0
A1 ☐ 8	33 ☐ D1
A0 ☐ 9	32 ☐ D2
PC7 ☐ 10	31 ☐ D3
PC6 ☐ 11	30 ☐ D4
PC5 ☐ 12	29 ☐ D5
PC4 ☐ 13	28 ☐ D6
PC0 ☐ 14	27 ☐ D7
PC1 ☐ 15	26 ☐ Vcc
PC2 ☐ 16	25 ☐ PB7
PC3 ☐ 17	24 ☐ PB6
PB0 ☐ 18	23 ☐ PB5
PB1 ☐ 19	22 ☐ PB4
PB2 ☐ 20	21 ☐ PB3

8 2 5 5 A

Figure 4-4. 8255 PPI Chip

- D7 – D0 - DATA BUS
- RESET- RESET INPUT
- CS - CHIP SELECT
- RD - READ INPUT
- WR - WRITE INPUT
- A0 – A1 - PORT ADDRESS
- PA 7 - PA 0 :PORT A (BIT)
- PB 7 - PB 0: PORT B (BIT)
- PC 7 - PC 0: PORT C (BIT)
- Vcc - 5 VOLTS
- GND

8255 Port Selection

Table 4-1: 8255 Port Selection

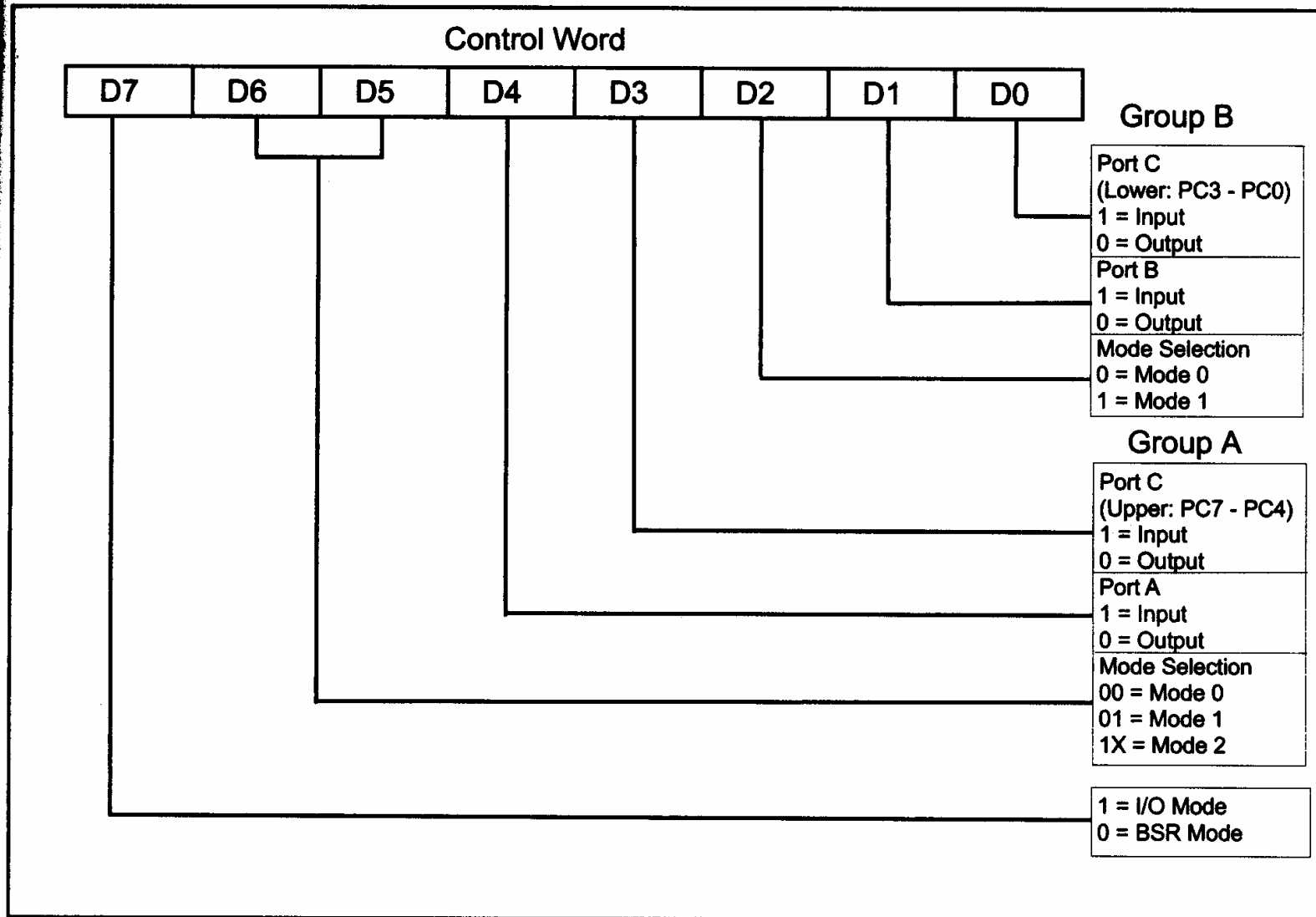| CS*	A1	A0	Selects:
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control register
1	x	x	8255 is not selected

8255 Control Word

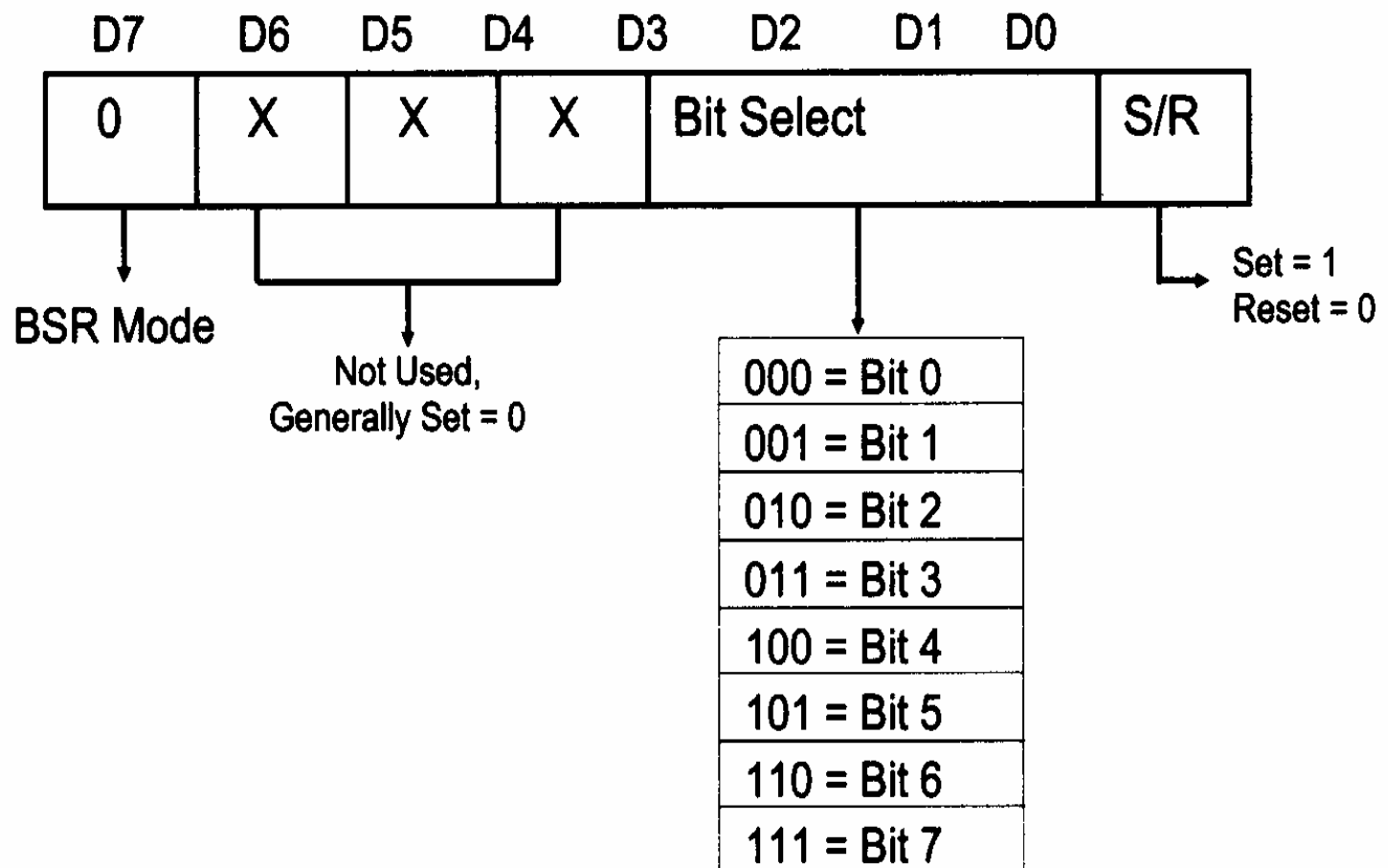**Figure 4-5. 8255 Control Word Format (I/O Mode)**
(Reprinted by permission of Intel Corporation, Copyright Intel Corp. 1983)

BSR Mode

D7	D6	D5	D4	D3	D2	D1	D0
0	X	X	X	Bit Select			S/R

BSR Mode

Not Used,
Generally Set = 0

Set = 1
Reset = 0

000 = Bit 0
001 = Bit 1
010 = Bit 2
011 = Bit 3
100 = Bit 4
101 = Bit 5
110 = Bit 6
111 = Bit 7

8255 Mode selection

Mode selection of the 8255A

While ports A, B, and C are used for I/O data, it is the control register that must be programmed to select the operation mode of the three ports A, B, and C. The ports of the 8255 can be programmed in any of the following modes.

1. Mode 0, simple I/O mode. In this mode, any of the ports A, B, CL, and CU can be programmed as input or output. In this mode, all bits are out or all are in. In other words, there is no control of individual bits.
2. Mode 1. In this mode, ports A and B can be used as input or output ports with handshaking capabilities. Handshaking signals are provided by the bits of port C.
3. Mode 2. In this mode, port A can be used as a bidirectional I/O port with handshaking capabilities whose signals are provided by port C. Port B can be used either in simple I/O mode or handshake mode 1.
4. BSR (bit set/reset) mode. In this mode, only the individual bits of port C can be programmed.

The 8255 chip is programmed in any of the above modes by sending a byte (Intel calls it control word) to the control register of the 8255. See Figure 4-5. Next we discuss the programming and usage of each mode.
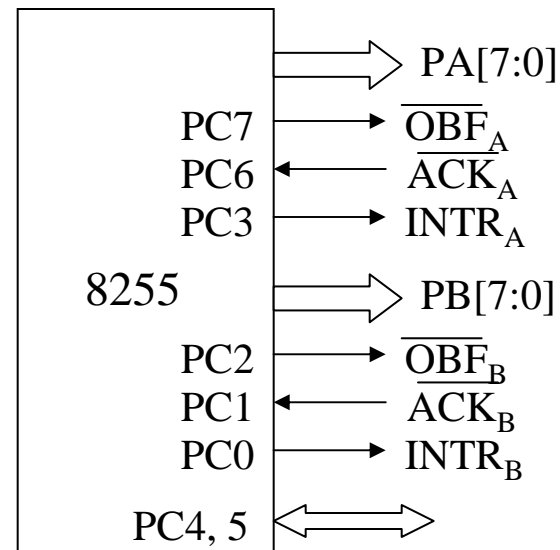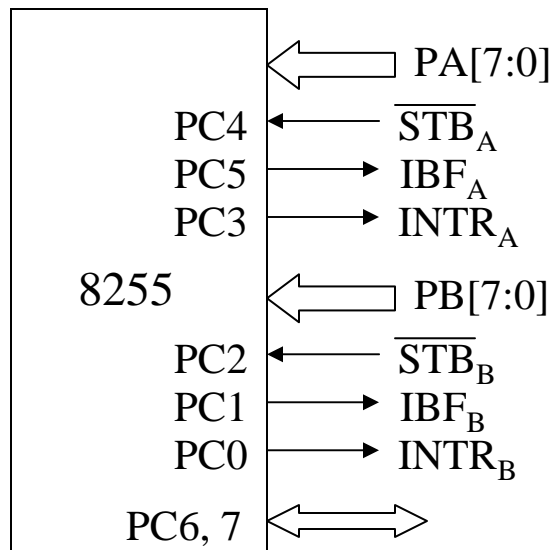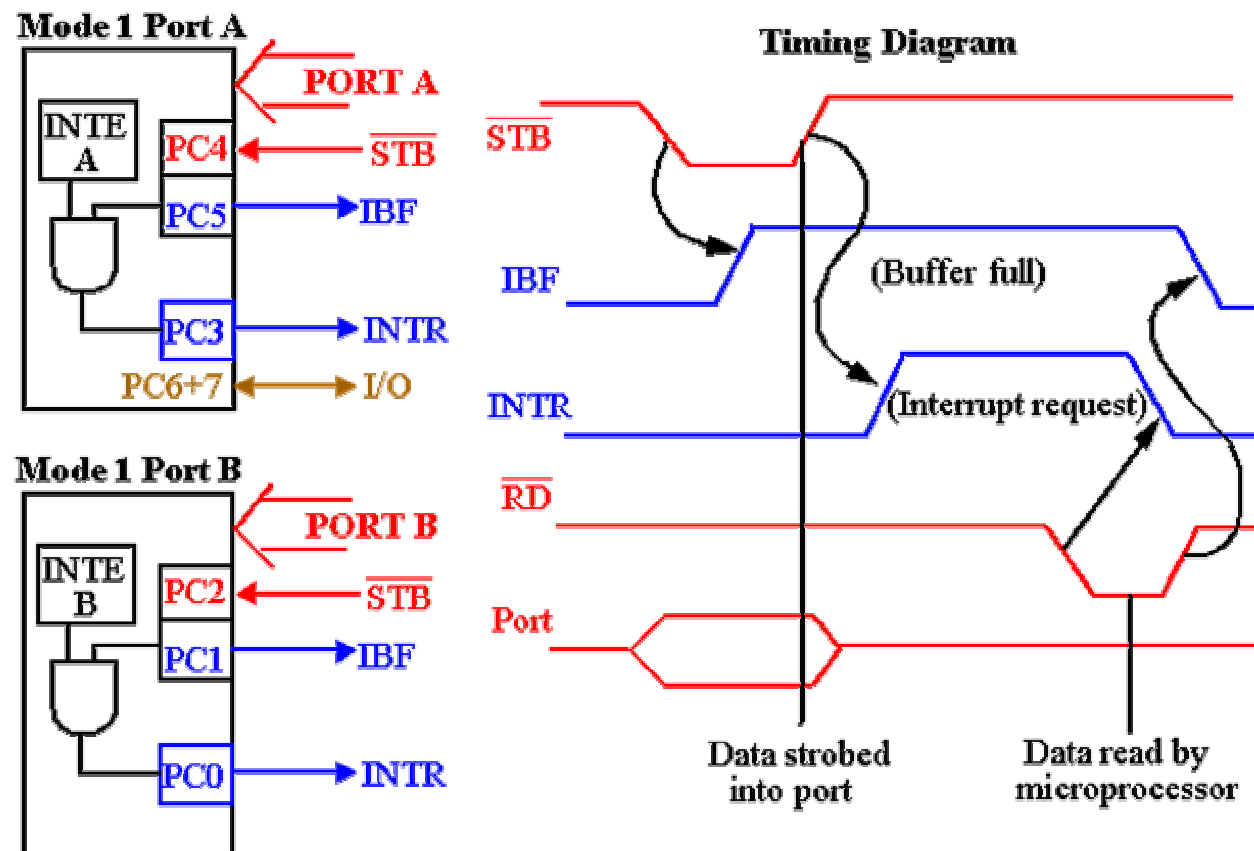
Programming 8255

❑ Mode 0:

    — Ports A, B, and C can be individually programmed as input or output ports
    — Port C is divided into two 4-bit ports which are independent from each other

❑ Mode 1:

    — Ports A and B are programmed as input or output ports
    — Port C is used for handshaking

Left diagram:

```
                      ⇐═══  PA[7:0]
         PC4  ←──  STB_A
         PC5  ──→  IBF_A
         PC3  ──→  INTR_A
  8255
                      ⇐═══  PB[7:0]
         PC2  ←──  STB_B
         PC1  ──→  IBF_B
         PC0  ──→  INTR_B

      PC6, 7  ⇔═══
```

Right diagram:

```
                      ═══⇒  PA[7:0]
         PC7  ──→  OBF_A
         PC6  ←──  ACK_A
         PC3  ──→  INTR_A
  8255
                      ═══⇒  PB[7:0]
         PC2  ──→  OBF_B
         PC1  ←──  ACK_B
         PC0  ──→  INTR_B

      PC4, 5  ⇔═══
```

$\overline{\text{STB}}$ The strobe input loads data into the port latch on a 0-to-1 transition

IFB   **Input buffer full** is an output indicating that the input latch
          contain   information

INTR   **Interrupt request** is an output that requests an interrupt

INTE   The **interrupt enable signal** is neither an input nor an output; it is an
          internal bit programmed via the PC4(port A) or PC2(port B) bits.

PC7,PC6   The port C pins 7 and 6 are general-purpose I/O pins that are
          available for any purpose.

Mode 1 Port A

INTE A

PC4 ← $\overline{\text{STB}}$
PC5 → IBF
PC3 → INTR
PC6+7 ↔ I/O

PORT A

Mode 1 Port B

INTE B

PC2 ← $\overline{\text{STB}}$
PC1 → IBF
PC0 → INTR

PORT B

Timing Diagram

$\overline{\text{STB}}$

IBF   (Buffer full)

INTR   (Interrupt request)

$\overline{\text{RD}}$

Port

Data strobed   Data read by
into port   microprocessor

$\overline{\text{OBF}}$ **Output buffer full** is an output that goes low when data is latched in either port A or port B. Goes low on $\overline{\text{ACK}}$.

$\overline{\text{ACK}}$ The **acknowledge** signal causes the $\overline{\text{OBF}}$ pin to return to 0. This is a response from an external device.

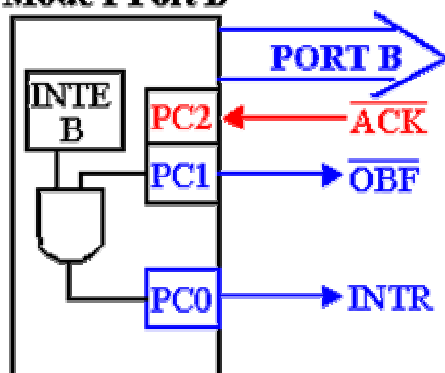INTR **Interrupt request** is an output that requests an interrupt

INTE The **interrupt enable signal** is neither an input nor an output; it is an internal bit programmed via the PC6(port A) or PC2(port B) bits.

PC5,PC4 The port C pins 5 and 4 are general-purpose I/O pins that are available for any purpose.
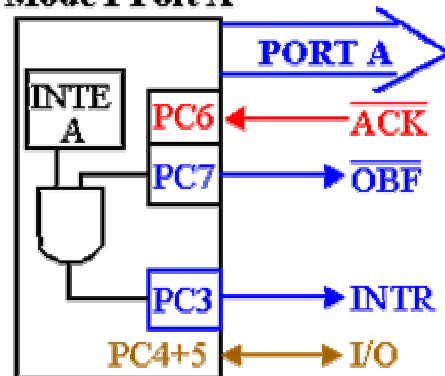
Mode 1 Port A

Timing Diagram

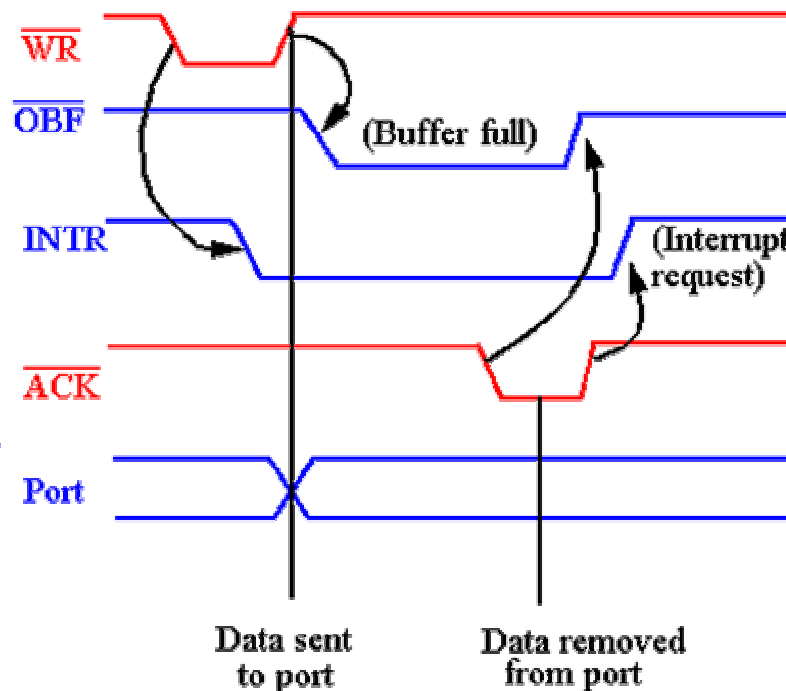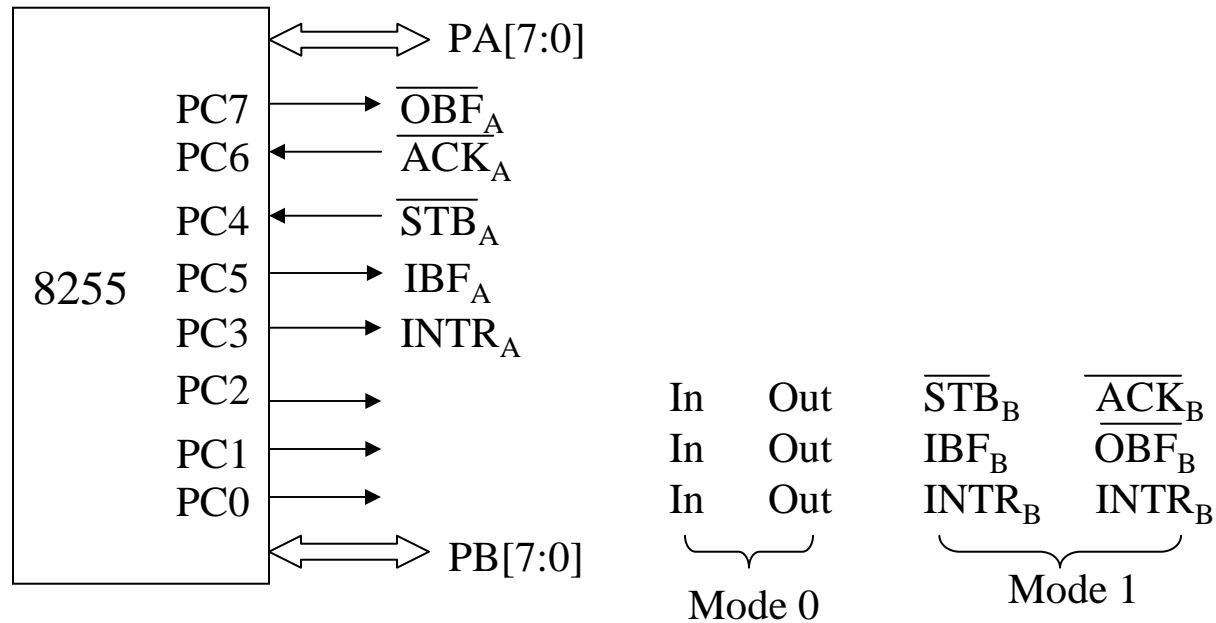**Mode 1 Port B**

Programming 8255

□ Mode 2:

— Port A is programmed to be bi-directional
— Port C is for handshaking
— Port B can be either input or output in mode 0 or mode 1

1.   Write the instructions that set 8255 into mode 0, port A as input, port B as output, PC0-PC3 as input, PC4-PC7 as output ?

INTR — Interrupt request is an output that requests an interrupt

$\overline{\text{OBF}}$ — Output buffer full is an output indicating that the output buffer contains data for the bi-directional bus

$\overline{\text{ACK}}$ — Acknowledge is an input that enables tri-state buffers which are otherwise in their high-impedance state

$\overline{\text{STB}}$ — The strobe input loads data into the port A latch

IFB — Input buffer full is an output indicating that the input latch contains information for the external bi-directional bus

INTE — Interrupt enable are internal bits that enable the INTR pin. Bit PC6(INTE1) and PC4(INTE2)

PC2,PC1 and PC0 — Theses port C pins are general-purpose I/O pins that are available for any purpose.

Timing diagram is a combination of the Mode 1 Strobed Input and Mode 1 Strobed Output Timing diagrams.