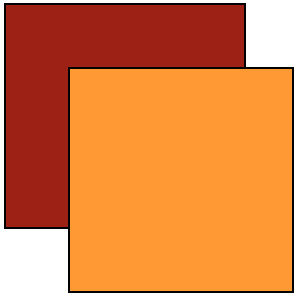


# Multiprocessor Configurations

## Multiprocessor Configurations

If a microprocessor system contains more components that can execute instructions independently, then the system is called multiprocessor system.

2 basic multiprocessor configurations:

1. Closely coupled
2. Loosely coupled

## *Advantages*

- Improves performance ratio of the systems.
- Several processors may be combined to fit the need of an application.
- Task are divided among the modules.
- If failure occurs, it is easier to find and replace the malfunctioning processor.

***Issues***

- Bus contention
- Interprocessor  communication
- Resource sharing

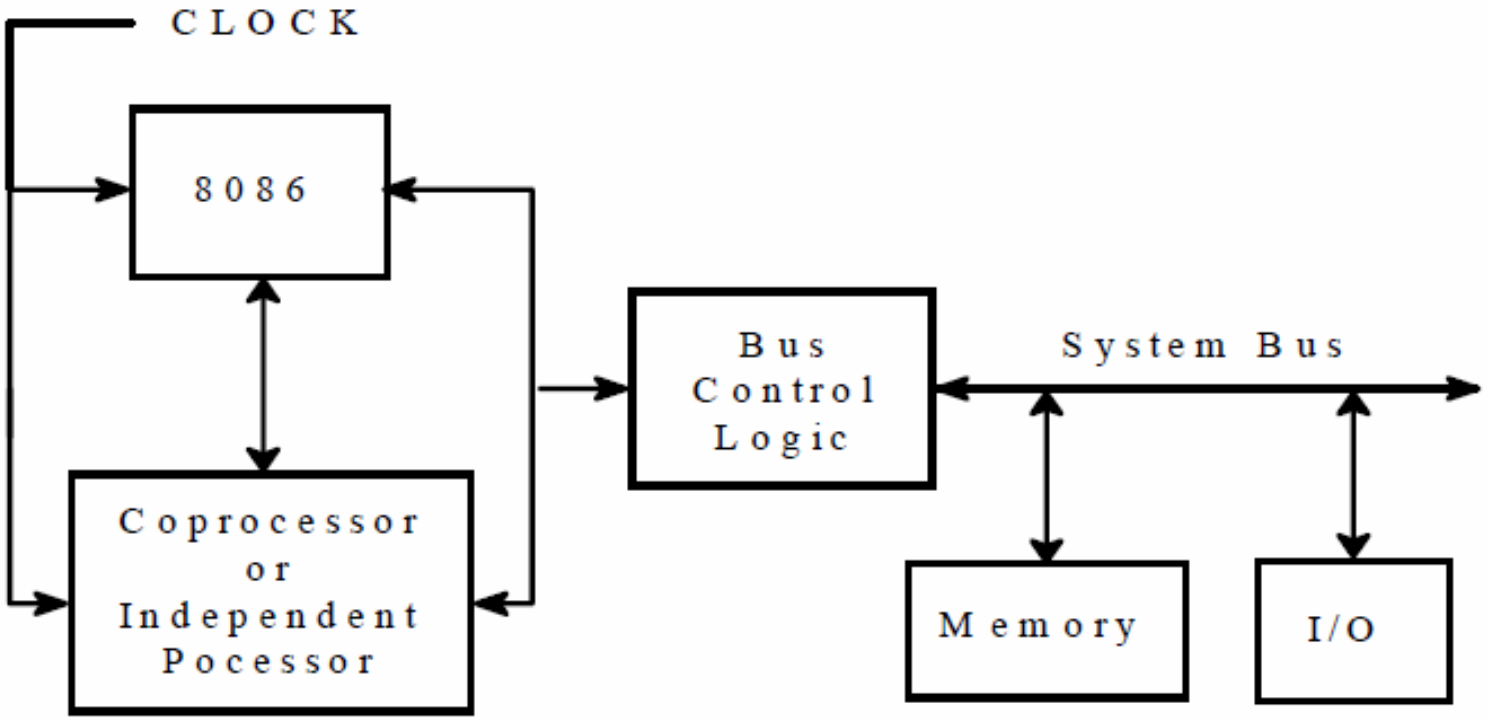
# Closely coupled configuration

In Closely coupled configurations, both the CPU and the external processor share:

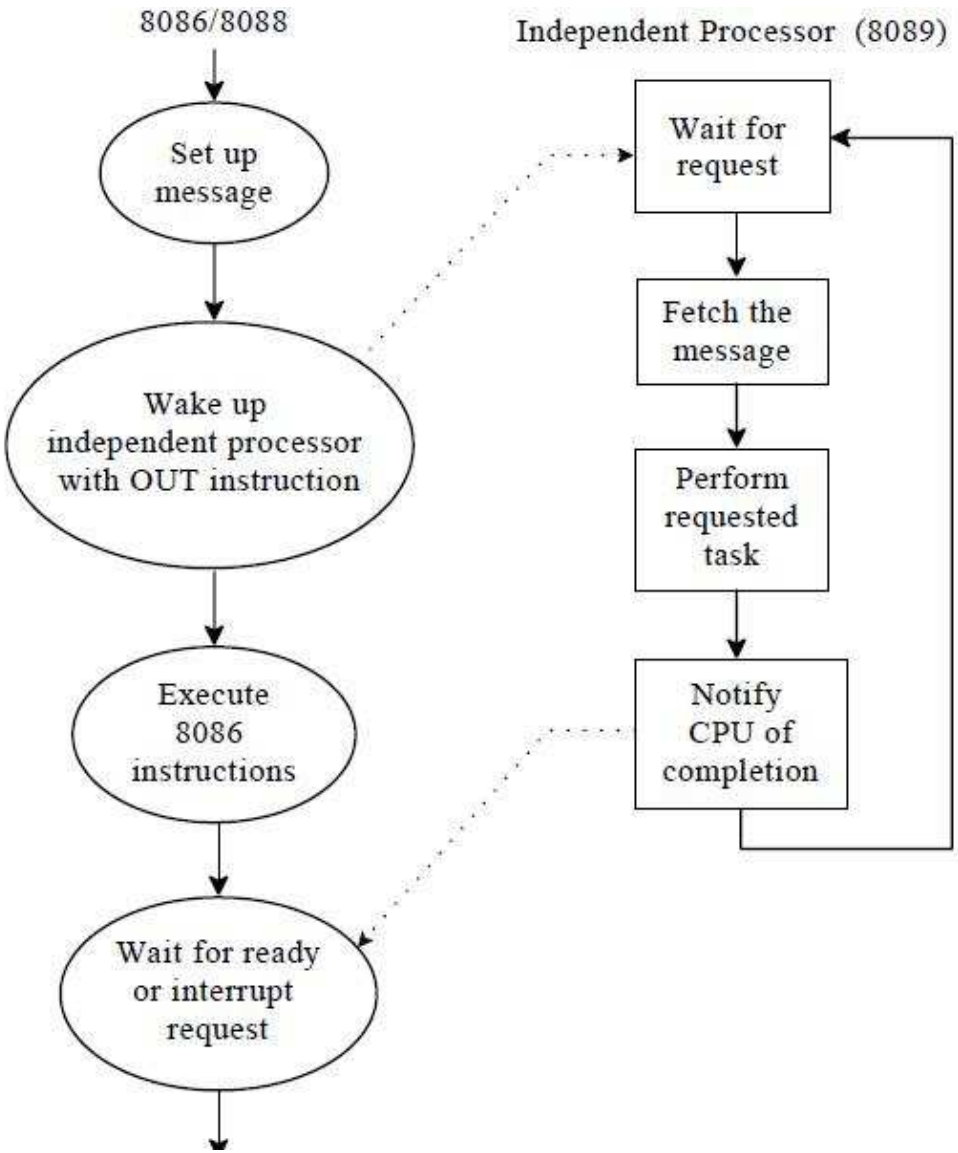
- Memory
- I/O system
- Bus & bus control logic
- Clock generator

# Closely coupled configuration

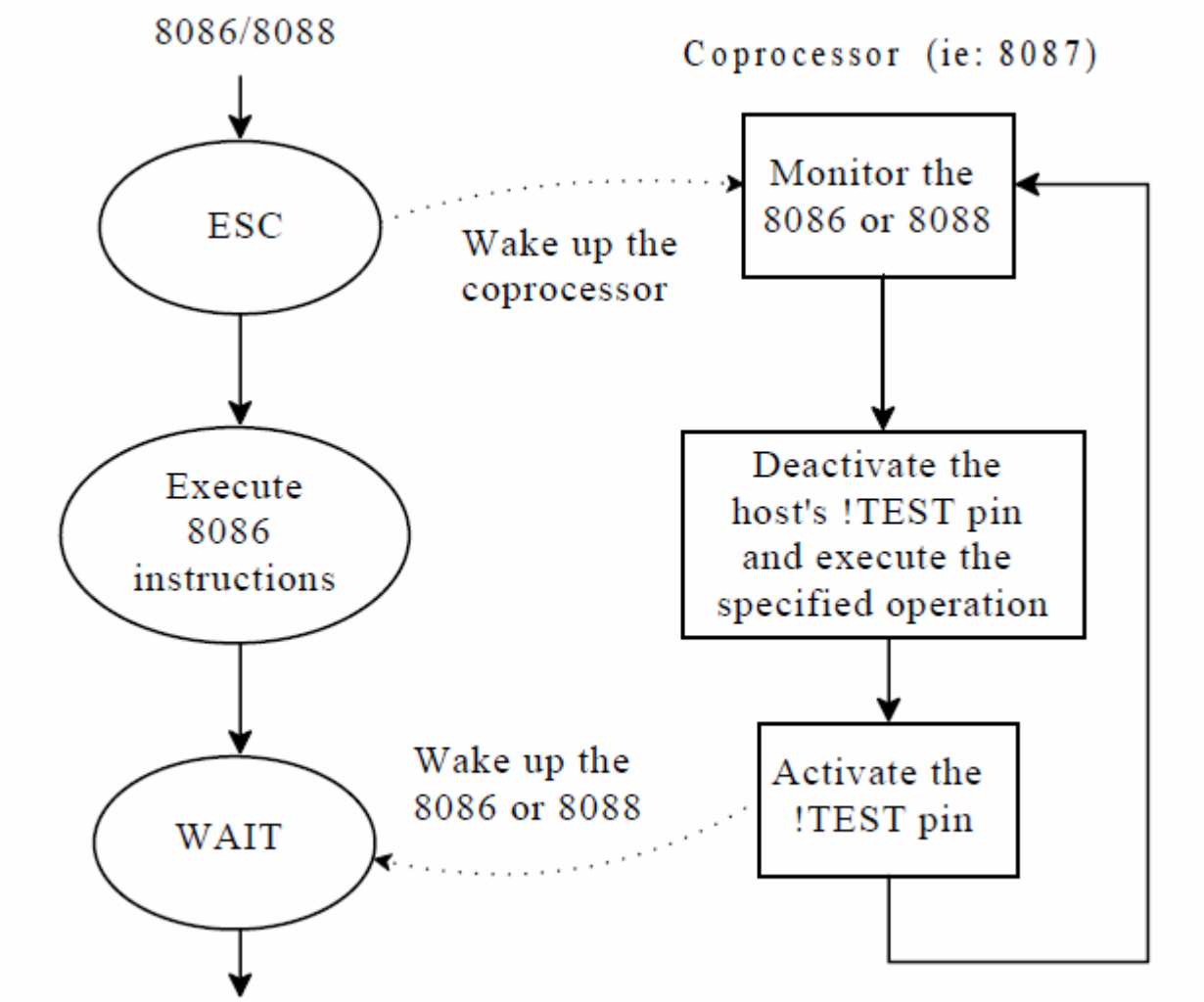
**Closely Coupled Configuration:**



# Closely coupled configuration



# Closely coupled configuration



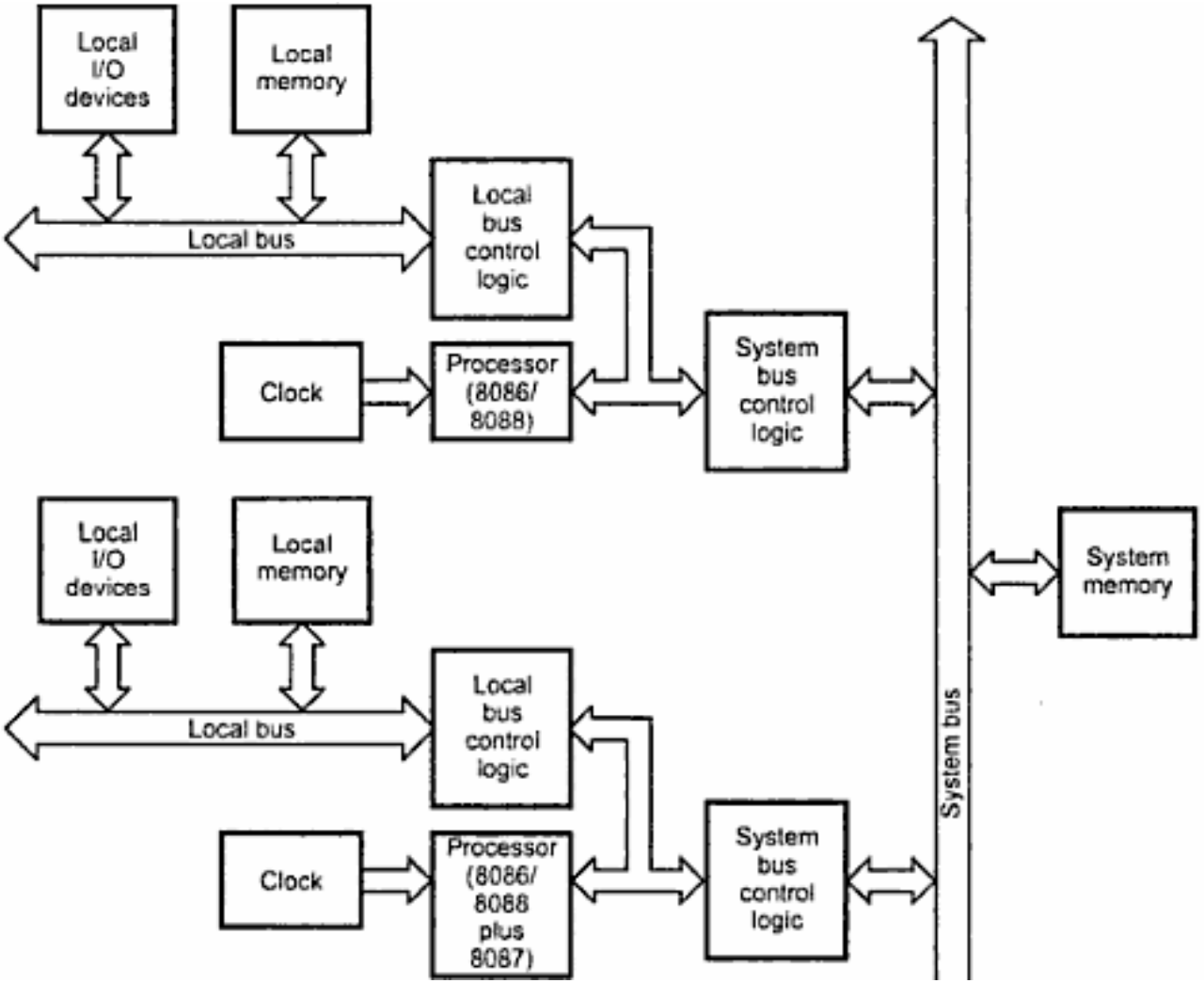
**Loosely Coupled Configuration:**

- has shared system bus, system memory, and system I/O

- each processor has its own clock as well as its own memory (in addition to access to the system resources, such as the system clock)

-clocks are of similar frequency, but asynchronous towards each other

# Loosely coupled configuration



## Bus Allocation Schemes

- Daisy Chaining

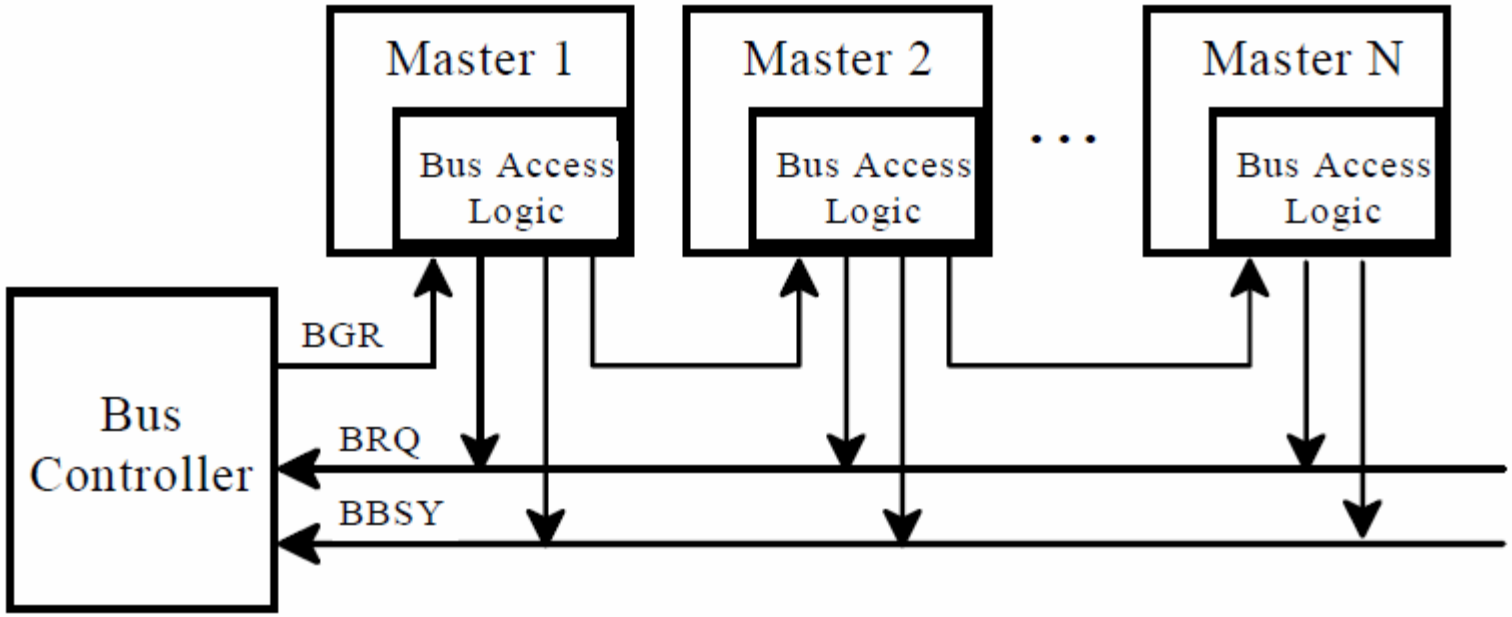
- Polling

-Independent Priority

***Daisy Chaining:***

- Need a bus controller to monitor bus busy and bus request signals
- Sends a bus grant to a Master , each Master either keeps the service or passes it on
- Master releases the Bus Busy signal when finished

# Daisy Chaining



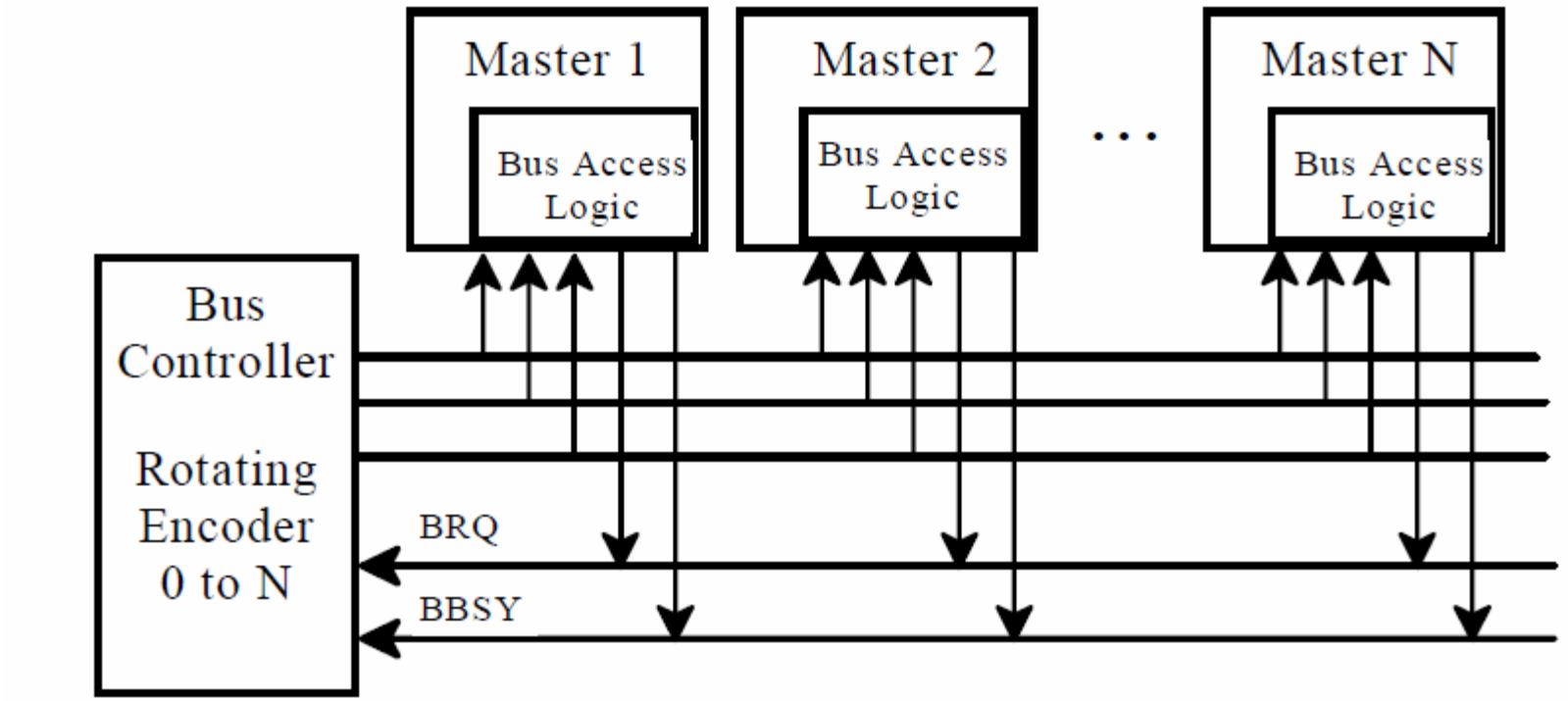
## Advantages

- It is simpler and cheaper method
- It requires the least number of lines and this number is independent of the number of masters in the system

## Disadvantages

- Propagation delay is proportional to the number of masters
- The priority of the master is fixed by its physical location
- Failure of one system causes the whole system to fail

Polling


Master 1
Bus Access Logic
Master 2
Bus Access Logic
Master N
Bus Access Logic
Bus Controller
Rotating Encoder 0 to N
BRQ
BBSY

***Polling:***

- A set of address lines are driven by controller to address the masters
- When a bus request is received from a device, controller generates the addresses on the address lines.
- When the requesting master recognizes its address, it activates the BUSY line.
- Once the busy line is activated , the controller stops generating further addresses

Advantages

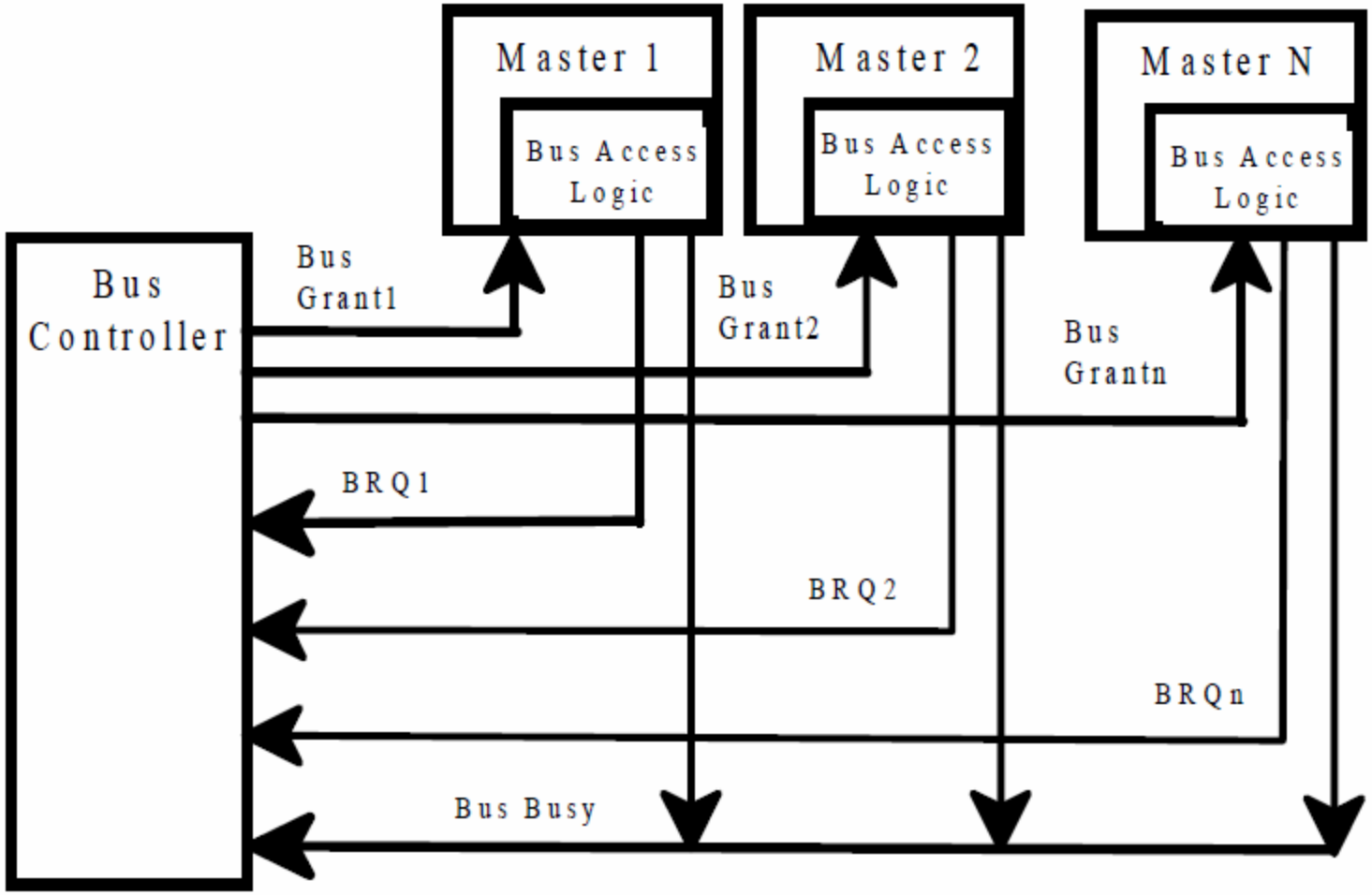
- The priority can be changed by altering the polling sequence stored in the controller

- If one module fails entire system does not fail

## Independent Priority

- Each master has a separate pair of bus request and bus grant line
- Each pair has priority assigned to it.
- Fixed priority or rotating priority can be given.

# Independent Priority



## Advantages

- Due to separate pairs of bus request and bus grant signals, arbitration is fast and is independent of the number of masters in the system

## Disadvantages

- It requires more bus request and grant signals(2*n signals for n modules).