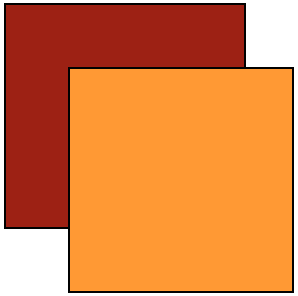
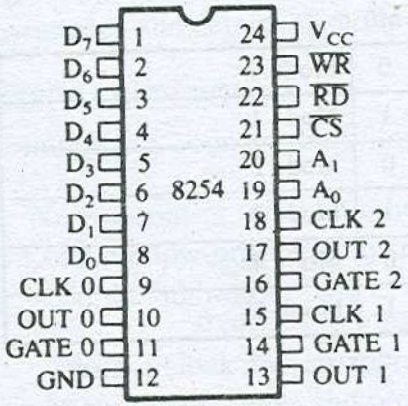


8254 – Programmable Interval Timer

8254 – Programmable Interval Timer : Block Diagram

Pin Configuration



Pin Names

D_7–D_0	Data Bus (8 Bit)
CLK N	Counter Clock Inputs
GATE N	Counter Gate Inputs
OUT N	Counter Outputs
$\overline{RD}$	Read Counter
$\overline{WR}$	Write Command or Data
$\overline{CS}$	Chip Select
A_0–A_1	Counter Select
V_{CC}	+5 Volts
GND	Ground

Block Diagram

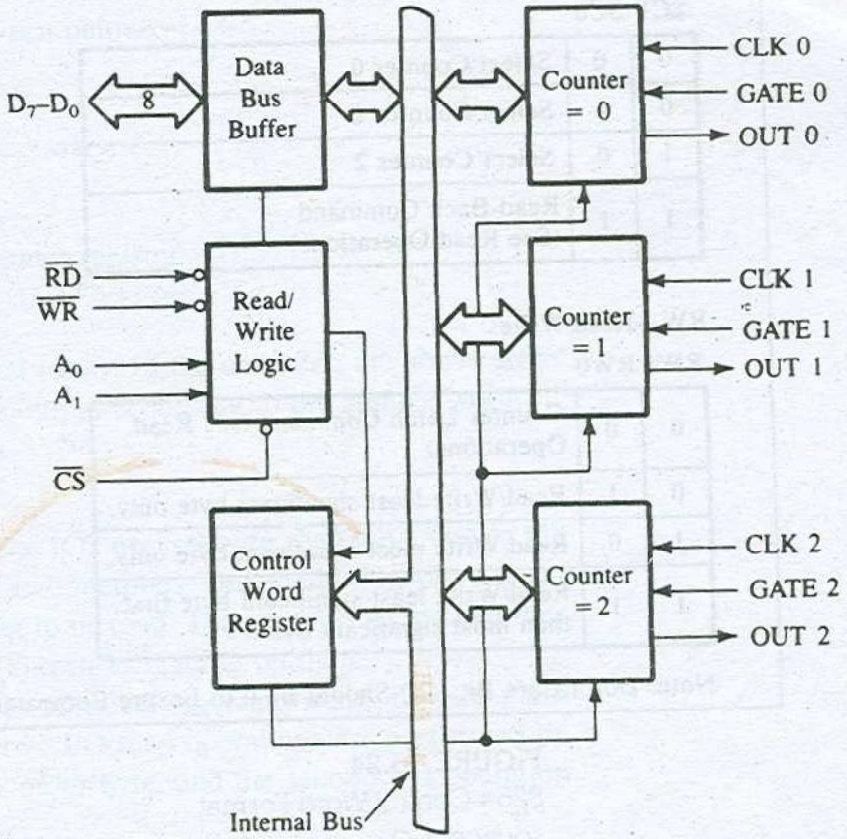
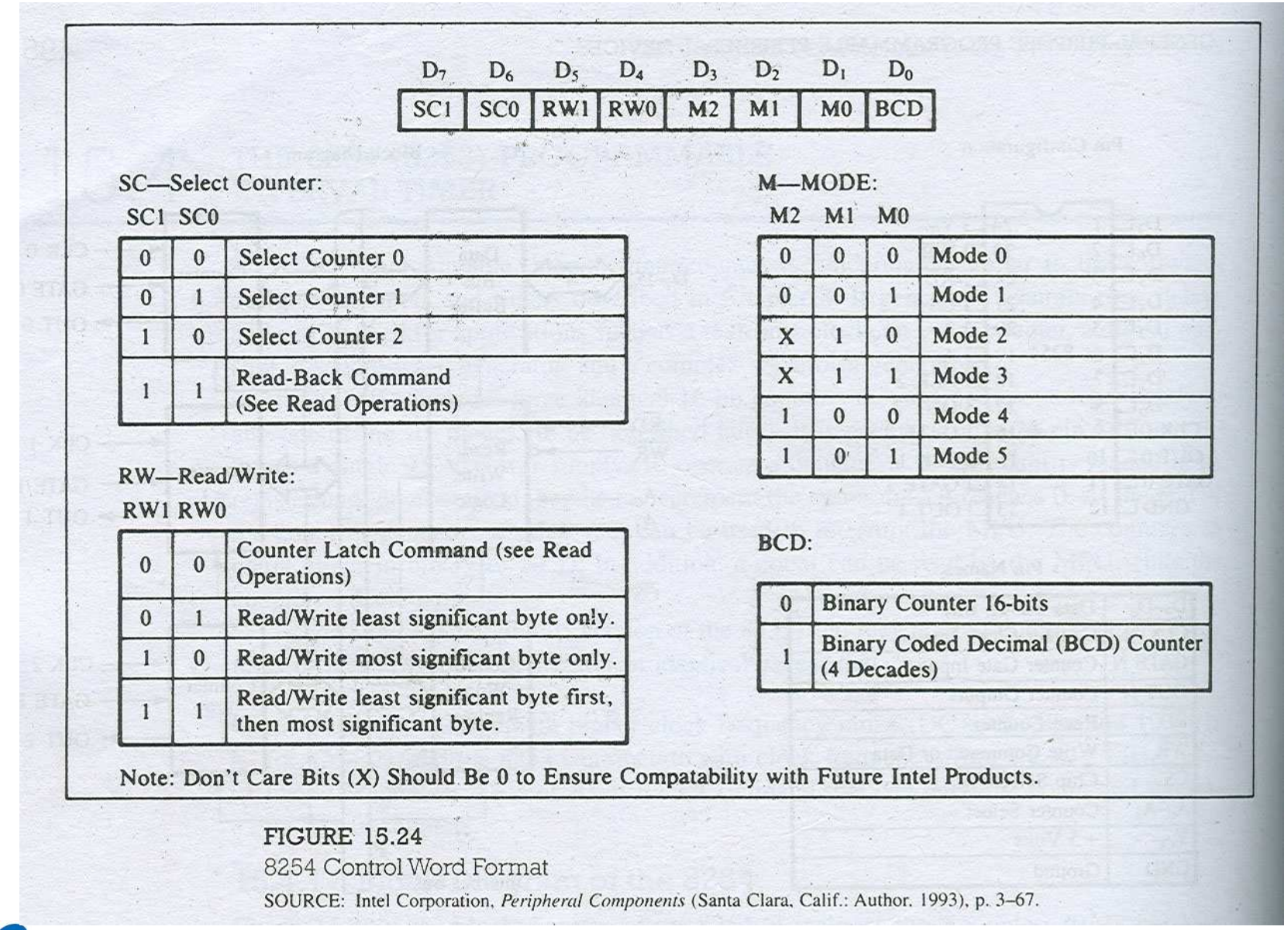


FIGURE 15.23
8254 Block Diagram

SOURCE: Intel Corporation, *Peripheral Components* (Santa Clara, Calif.: Author, 1993), p. 3–62.

8254 – Programmable Interval Timer : Control Word



D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC—Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

M—MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW—Read/Write:

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Note: Don't Care Bits (X) Should Be 0 to Ensure Compatability with Future Intel Products.

FIGURE 15.24
8254 Control Word Format

SOURCE: Intel Corporation, *Peripheral Components* (Santa Clara, Calif.: Author, 1993), p. 3–67.

8254 – Programmable Interval Timer : Modes

6 modes

Mode 0 – Interrupt on terminal count

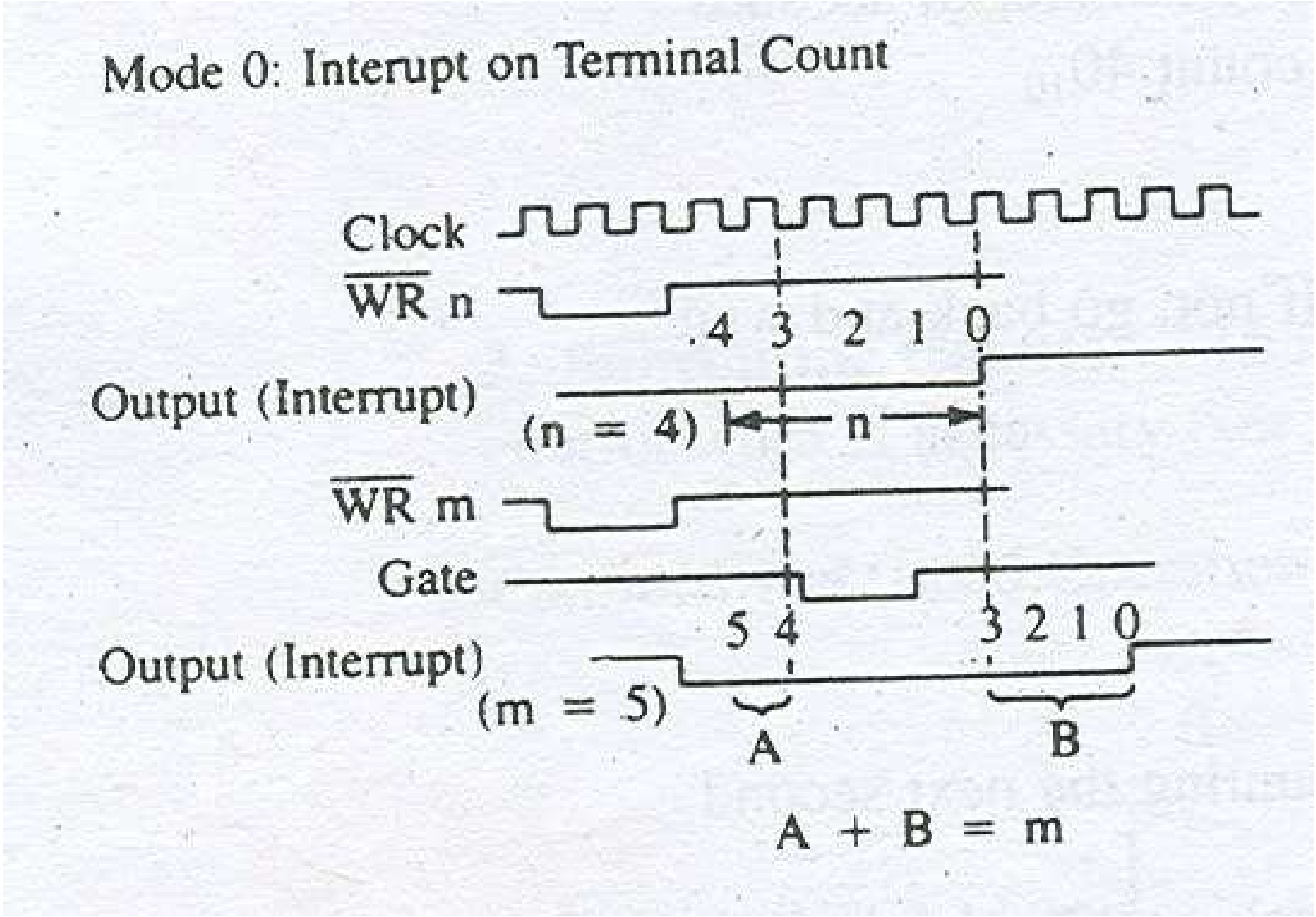
Mode 1 – Retriggerable one shot (programmable one shot)

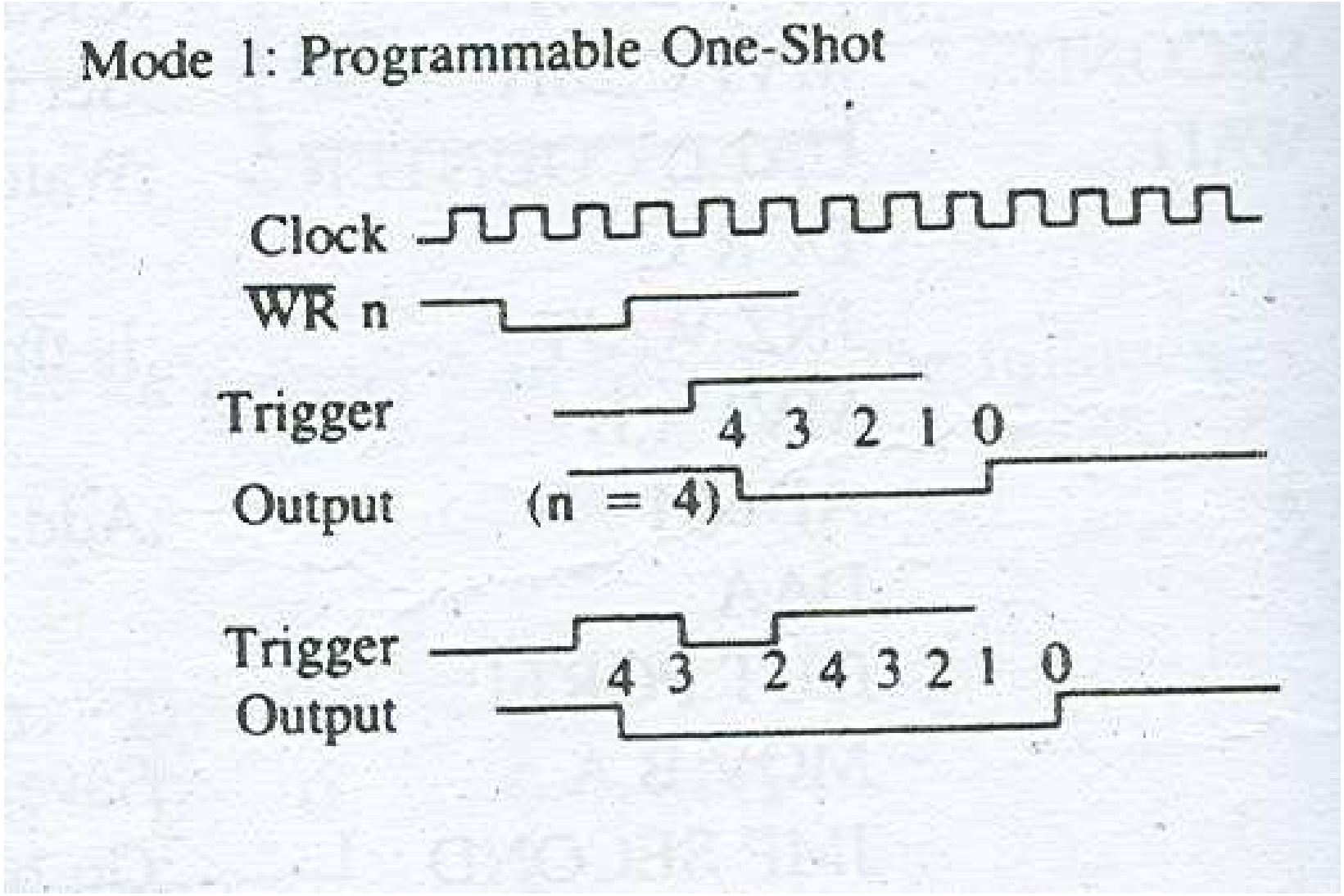
Mode 2 – Rate generator clock

Mode 3 – Square wave generator

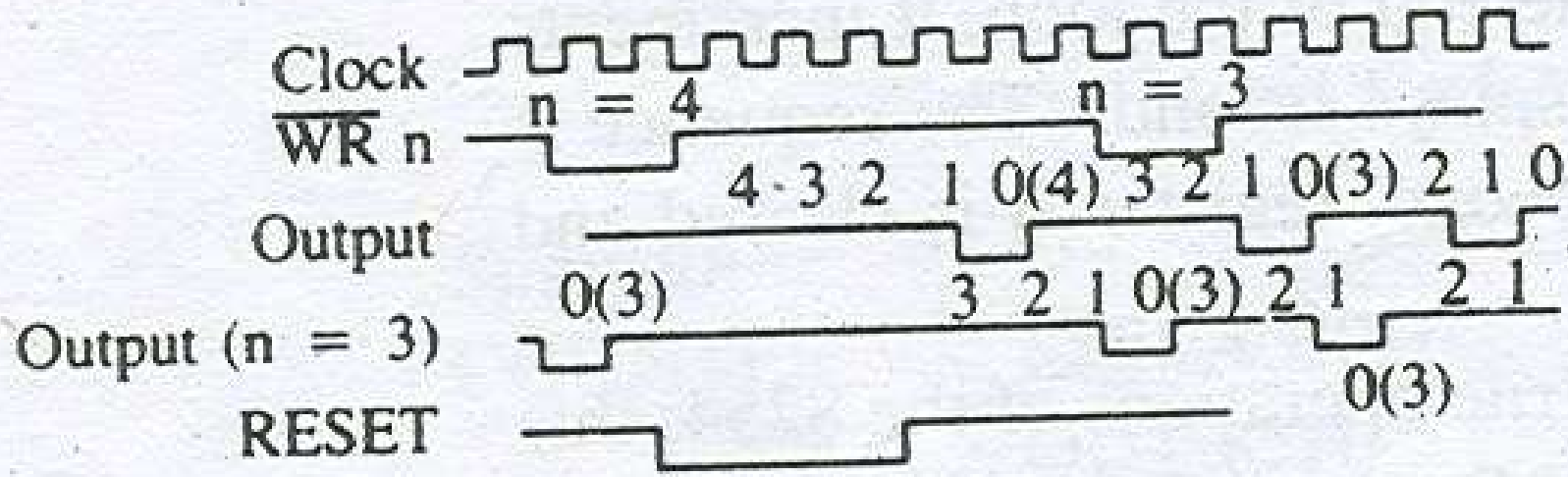
Mode 4 – S/W triggered strobe

Mode 5 – H/W triggered strobe

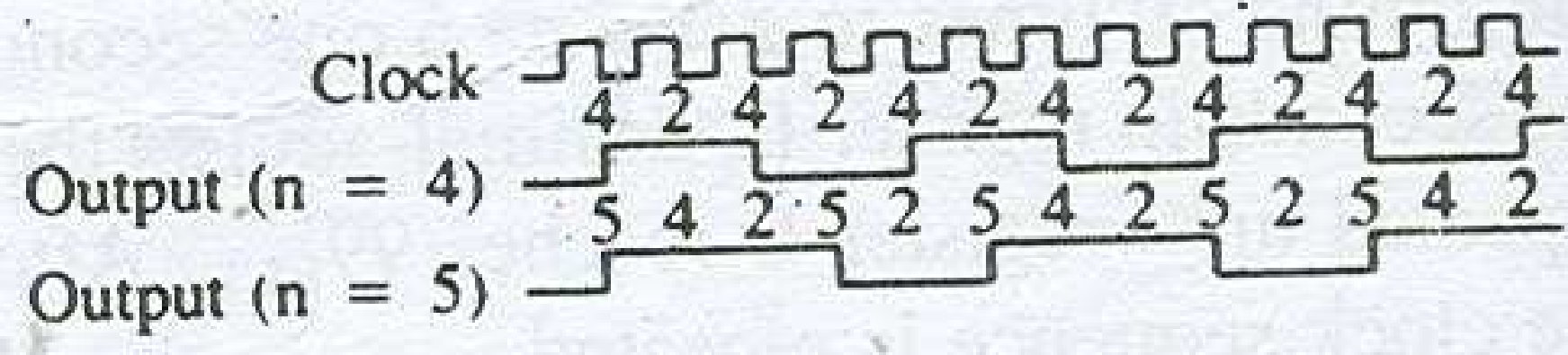

Mode 0: Interupt on Terminal Count
Clock
WR n
.4 3 2 1 0
Output (Interrupt)
(n = 4)
n
WR m
Gate
5 4
3 2 1 0
Output (Interrupt)
(m = 5)
A
B
A + B = m


Mode 1: Programmable One-Shot
Clock
WR n
Trigger
4 3 2 1 0
Output
(n = 4)
Trigger
4 3 2 4 3 2 1 0
Output

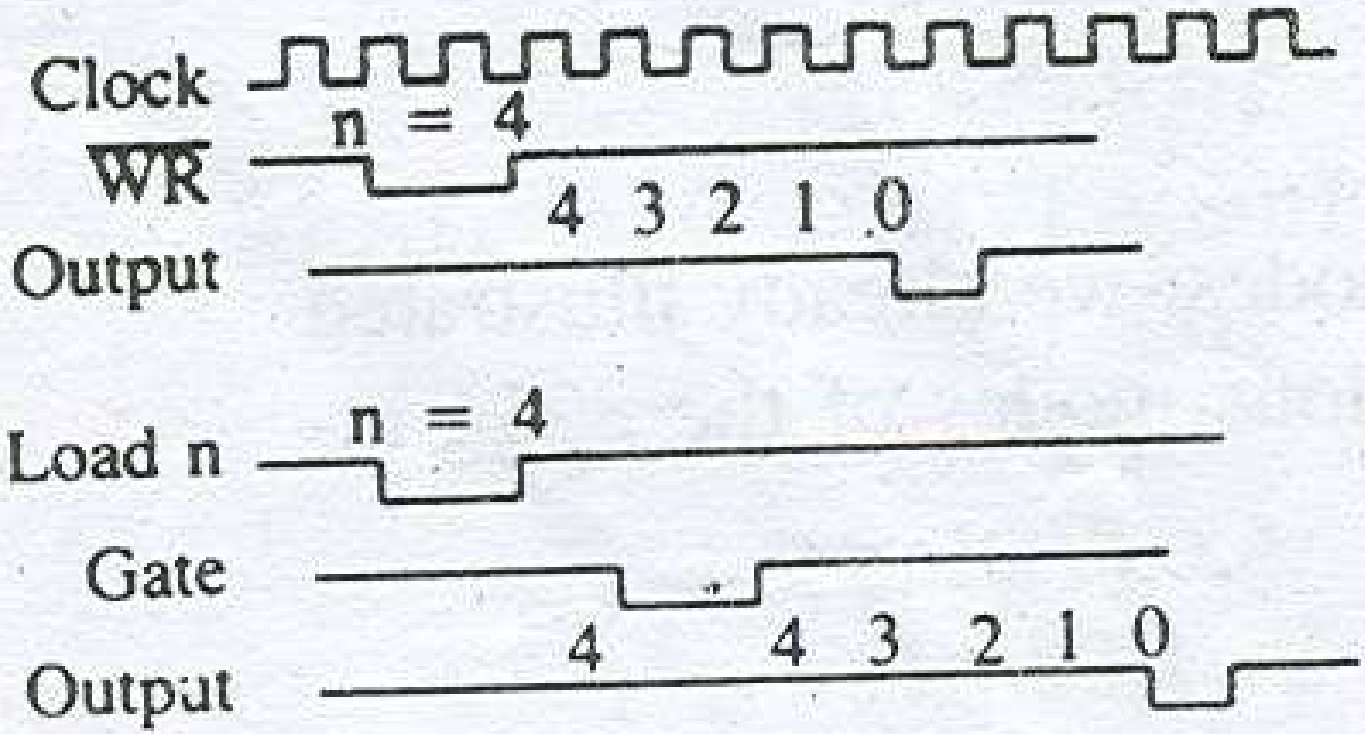
Mode 2: Rate Generator Clock

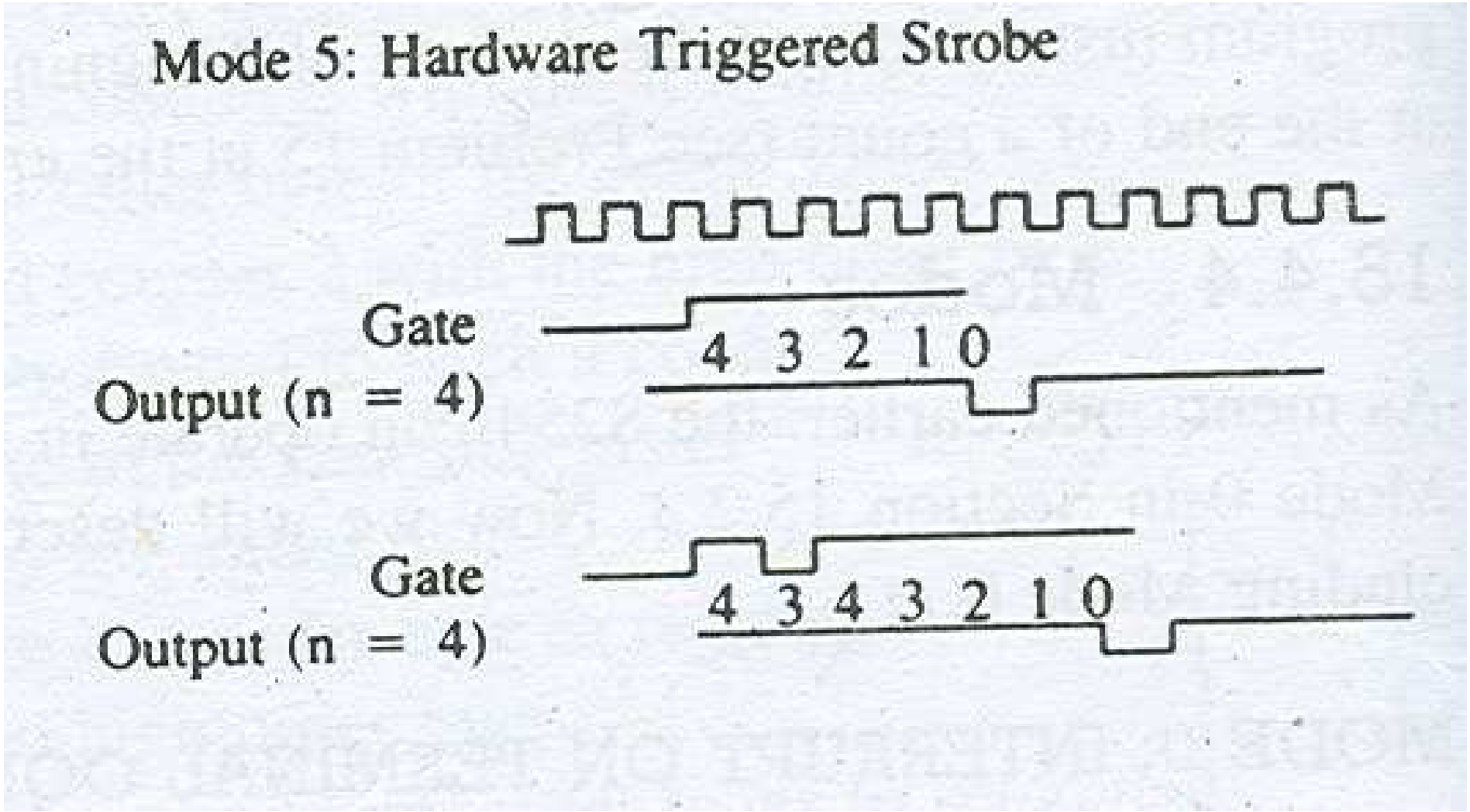


Mode 3: Square Wave Generator



Mode 4: Software Triggered Strobe




Mode 5: Hardware Triggered Strobe
Gate
4 3 2 1 0
Output (n = 4)
Gate
4 3 4 3 2 1 0
Output (n = 4)

8254 – Programmable Interval Timer : Effect of gate in different modes

Modes \ Signal Status	Low or Going Low	Rising	High
0	Disables counting	—	Enables counting
1	—	(1) Initiates counting (2) Resets output after next clock	—
2	(1) Disables counting (2) Sets output immediately high	(1) Reloads counter (2) Initiates counting	Enables counting
3	(1) Disables counting (2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	—	Enables counting
5	—	Initiates counting	—

FIGURE 15.25
Gate Settings of a Counter

SOURCE: Intel Corporation, *Peripheral Components* (Santa Clara, Calif.: Author, 1993), p. 3–78.

8254 – Programmable Interval Timer : Read Back Command

(a) Read-Back Command Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	$\overline{\text{COUNT}}$	$\overline{\text{STATUS}}$	CNT 2	CNT 1	CNT 0	0

D_5: 0 = Latch Count of Selected Counter(s)
D_4: 0 = Latch Status of Selected Counter(s)
D_3: 1 = Select Counter 2
D_2: 1 = Select Counter 1
D_1: 1 = Select Counter 0
D_0: Reserved for Future Expansion; Must Be 0

$A_0, A_1 = 11$
$\overline{CS} = 0$
$\overline{RD} = 1$
$\overline{WR} = 0$

8254 – Programmable Interval Timer : Status Byte

(b) Status Byte

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OUTPUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D_7: 1 = Out Pin is 1
: 0 = Out Pin is 0
D_6: 1 = Null Count
: 0 = Count Available for Reading
D_5-D_0: Counter Programmed Mode