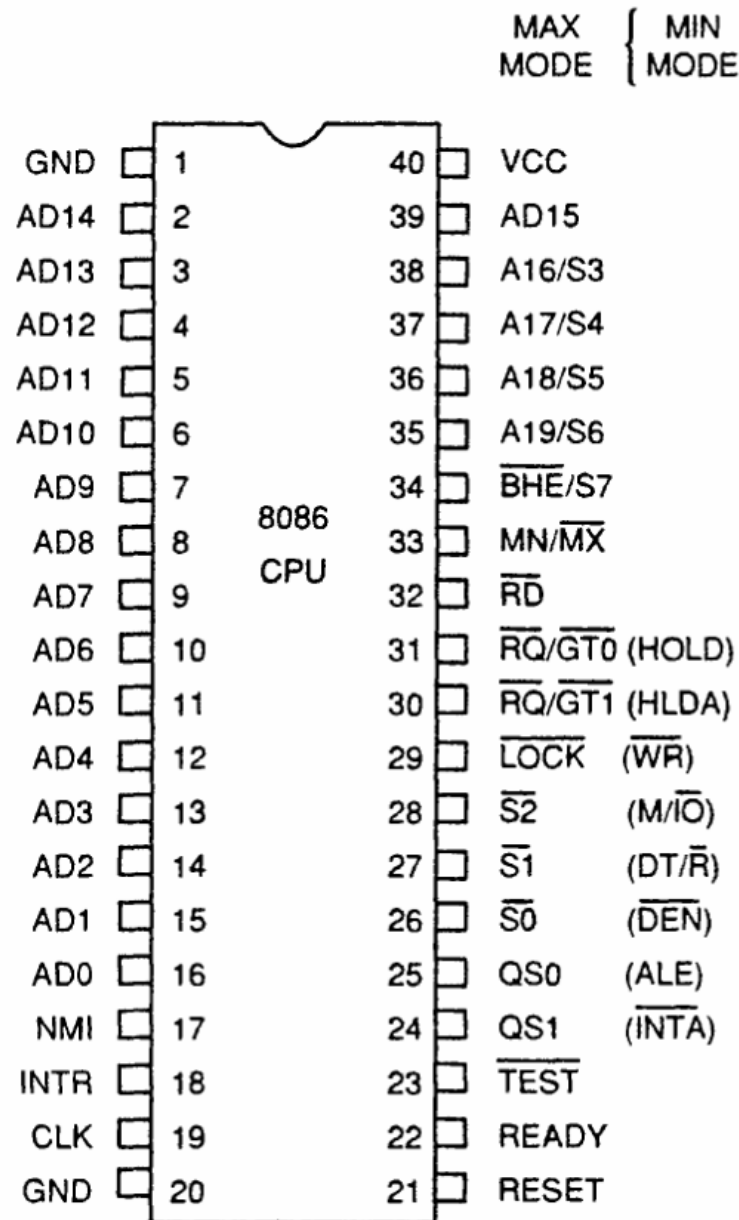
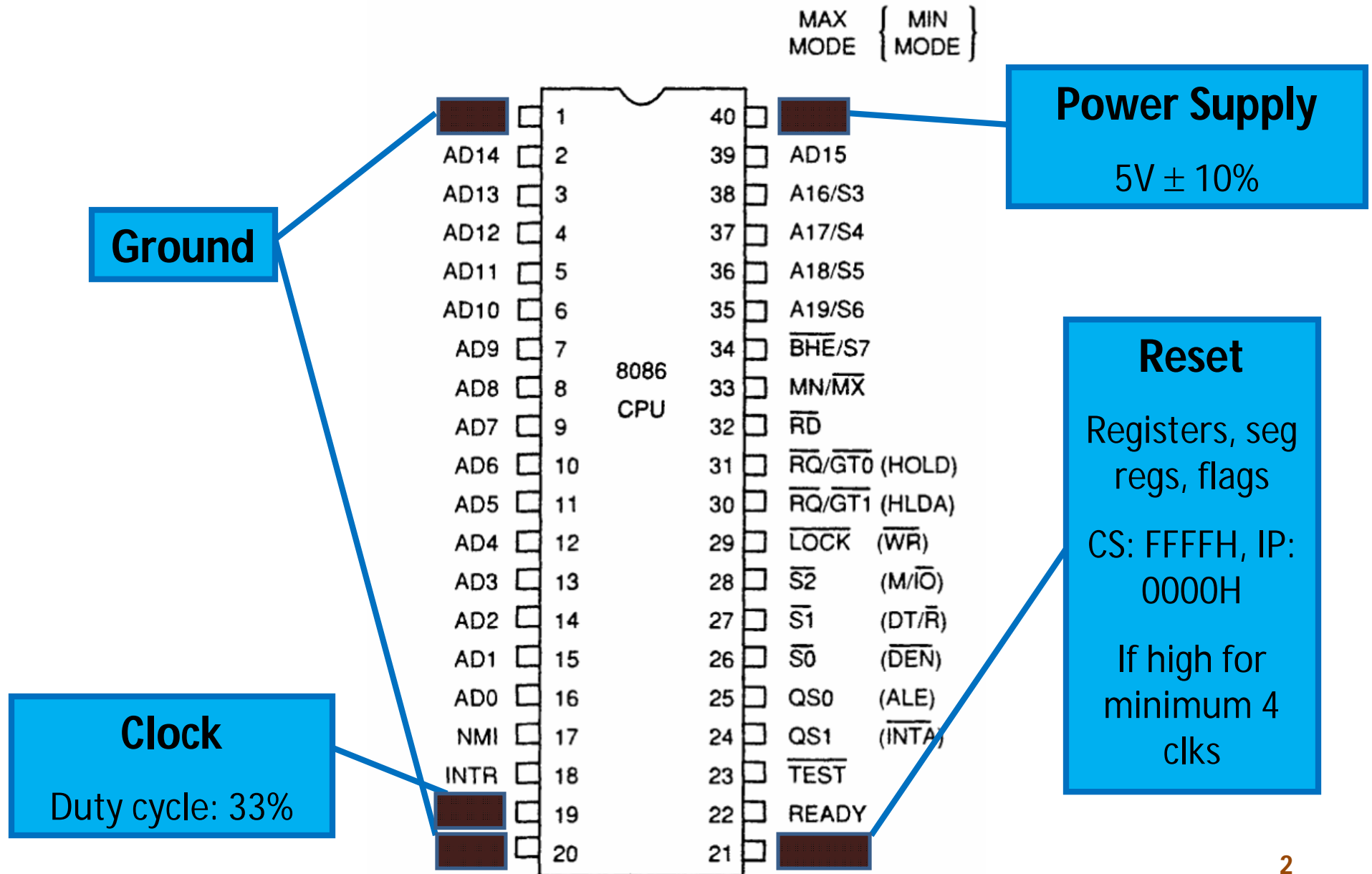


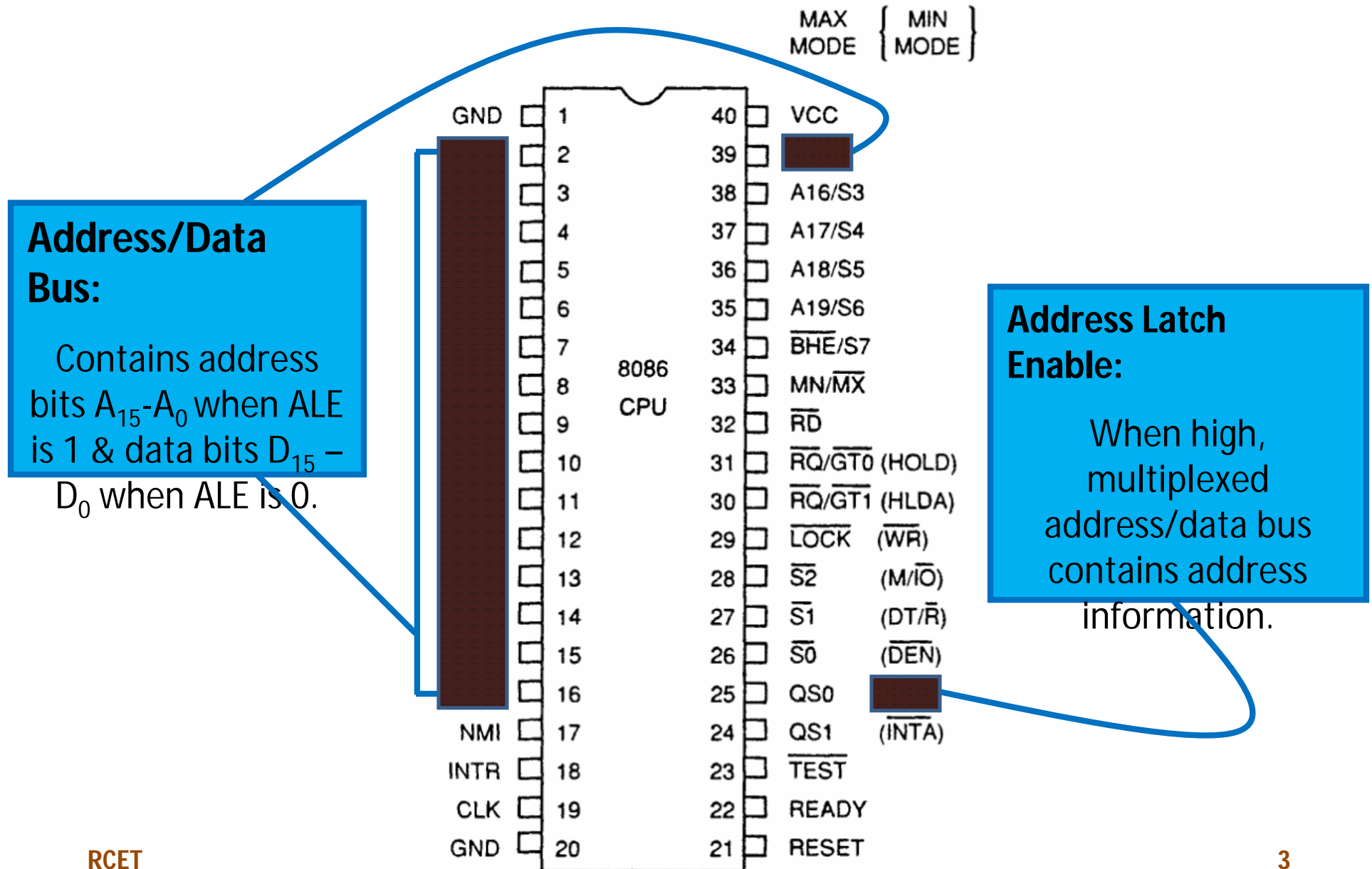
INTEL 8086 - Pin Diagram



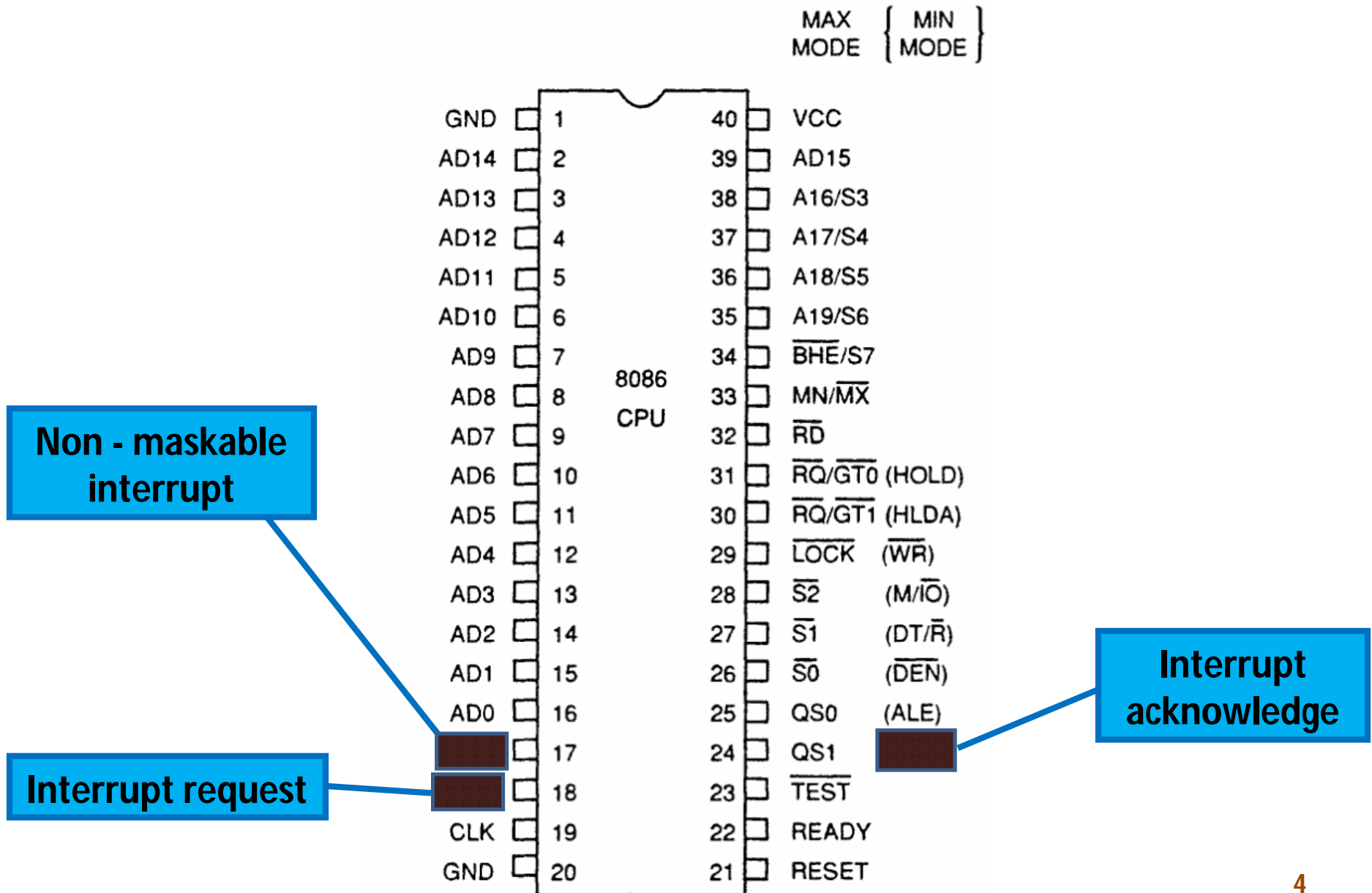
INTEL 8086 - Pin Details



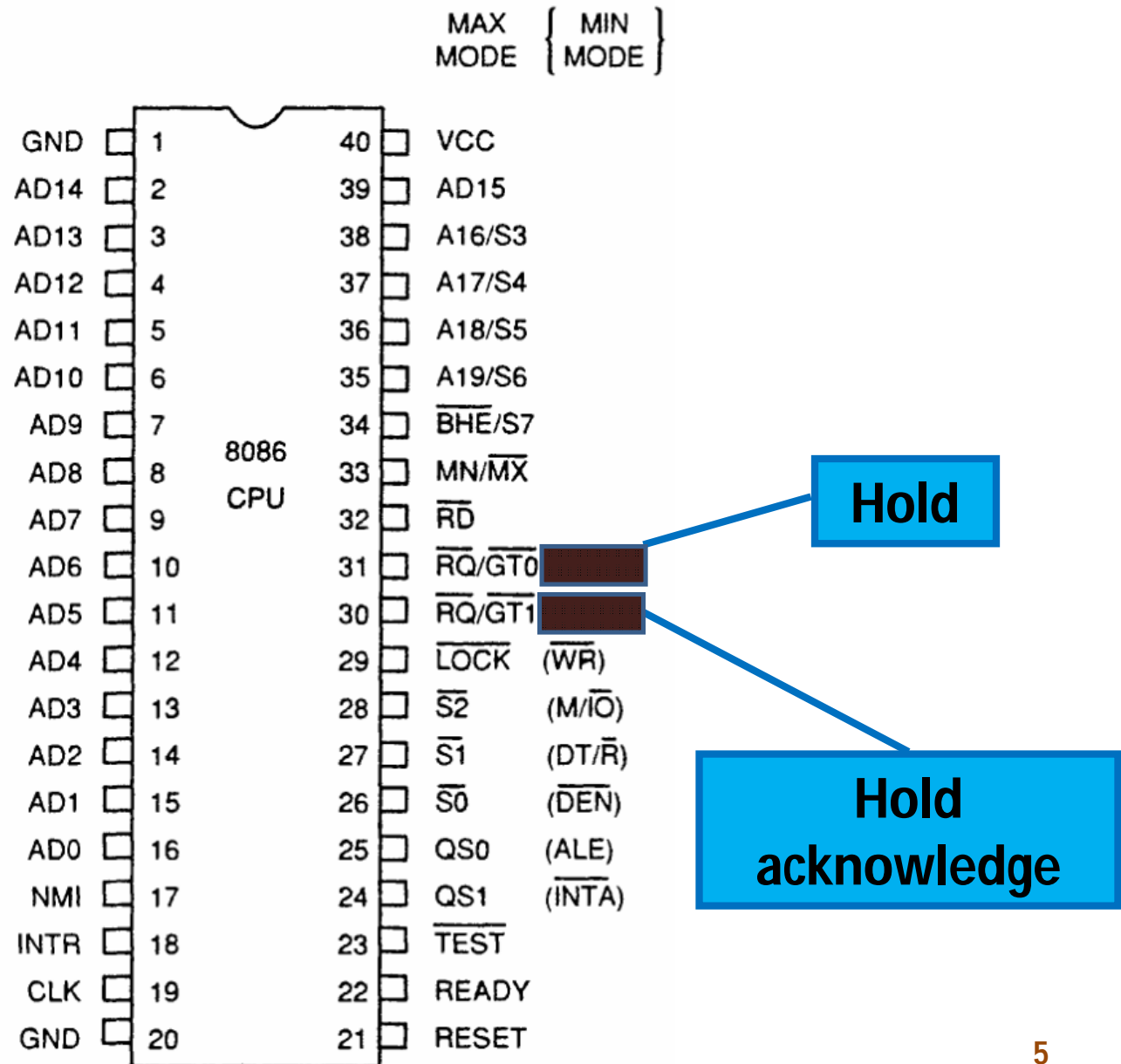
INTEL 8086 - Pin Details



INTEL 8086 - Pin Details



INTEL 8086 - Pin Details



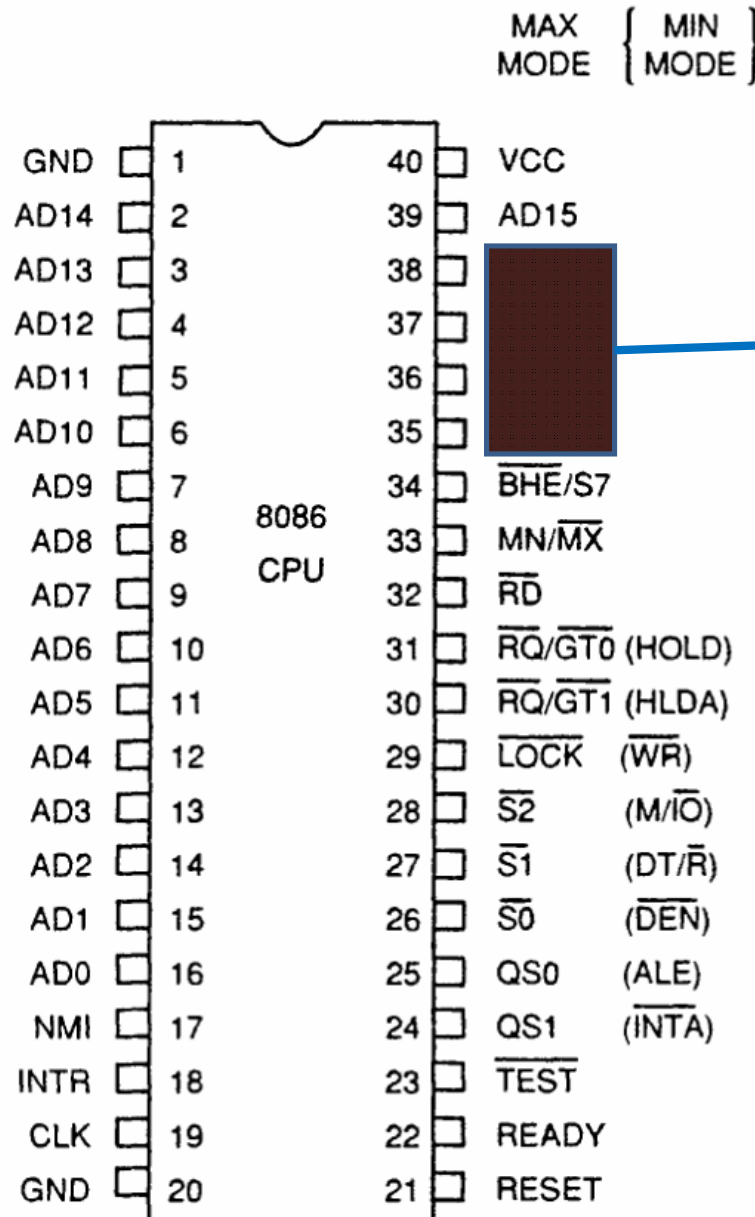
INTEL 8086 - Pin Details

S6: Logic 0.

S5: Indicates condition of IF flag bits.

S4-S3: Indicate which segment is accessed during current bus cycle:

S4	S3	Function
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment



Address/Status Bus

Address bits $A_{19} - A_{16}$ & Status bits $S_6 - S_3$

INTEL 8086 - Pin Details

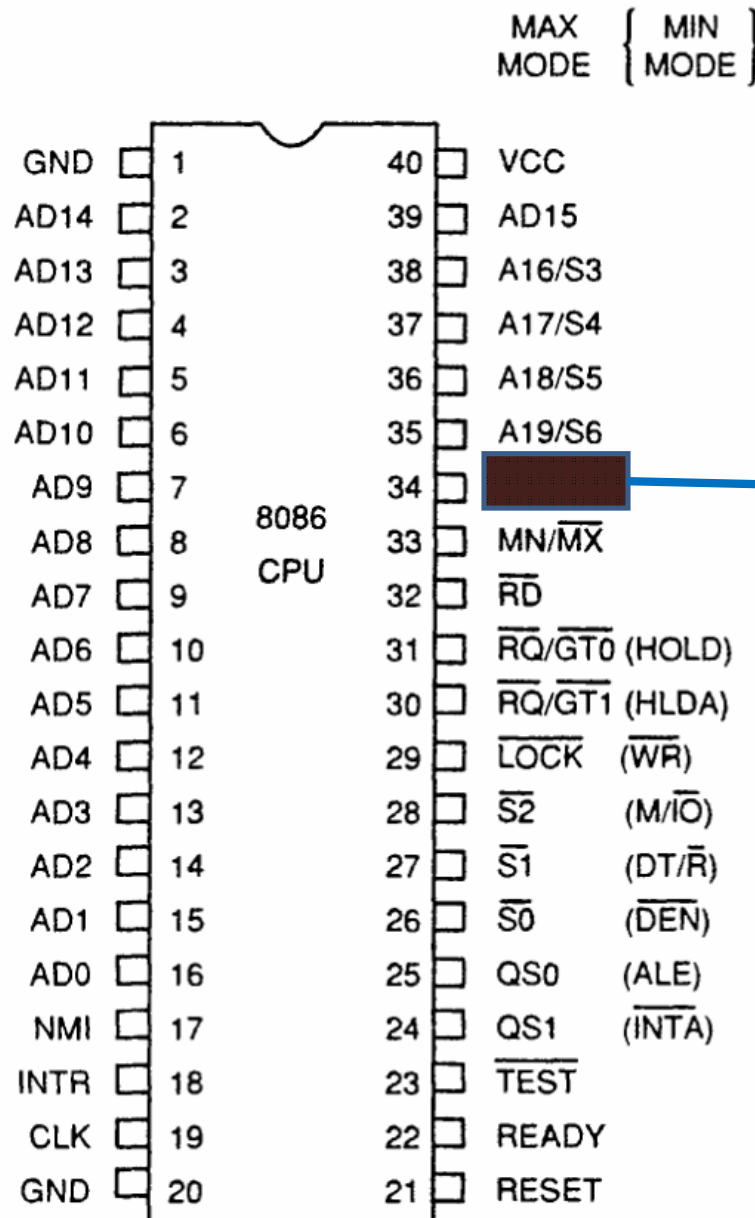
BHE#, A₀:

0,0: Whole word
(16-bits)

0,1: High byte
to/from odd address

1,0: Low byte
to/from even address

1,1: No selection

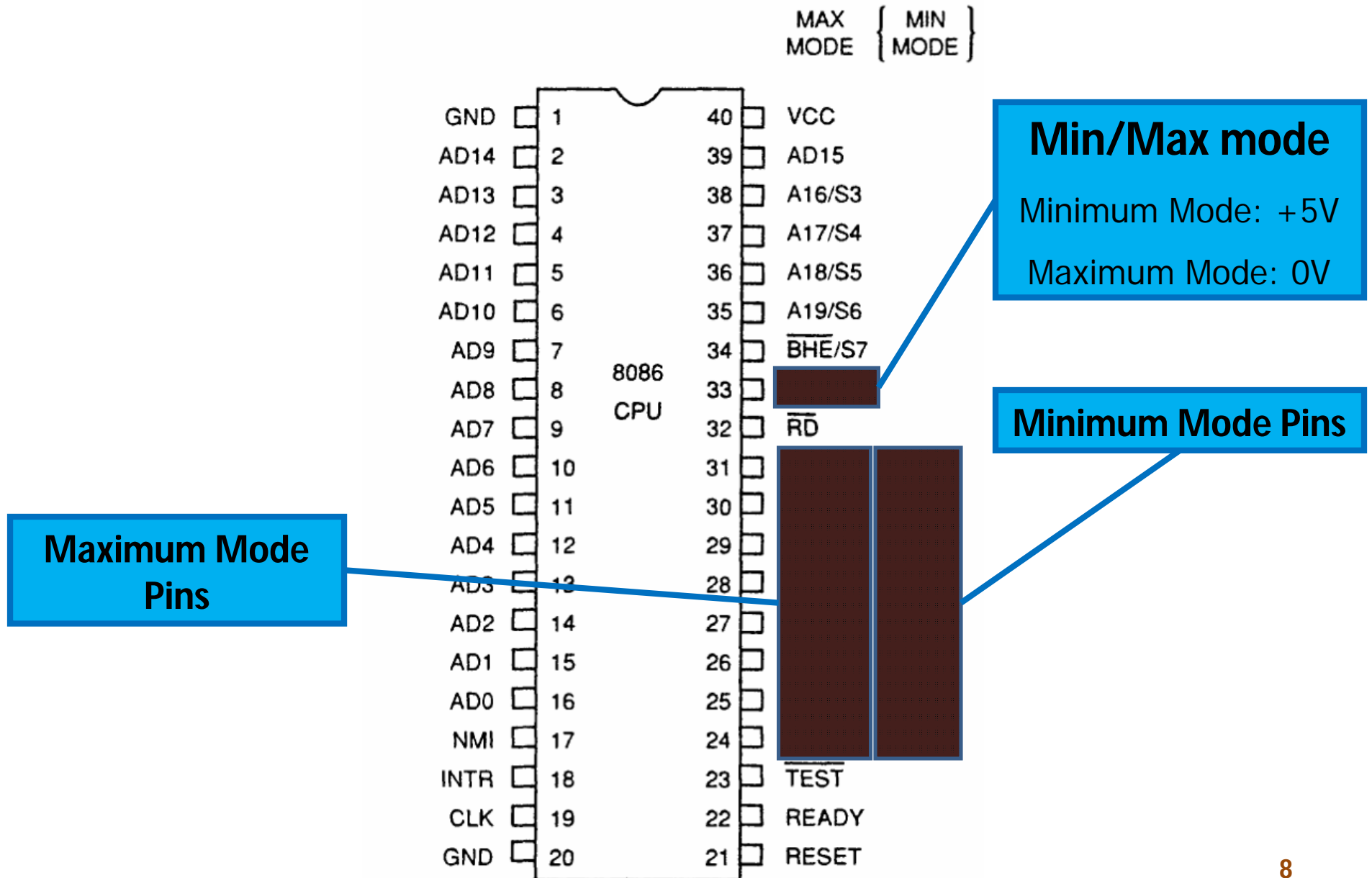


Bus High Enable/S7

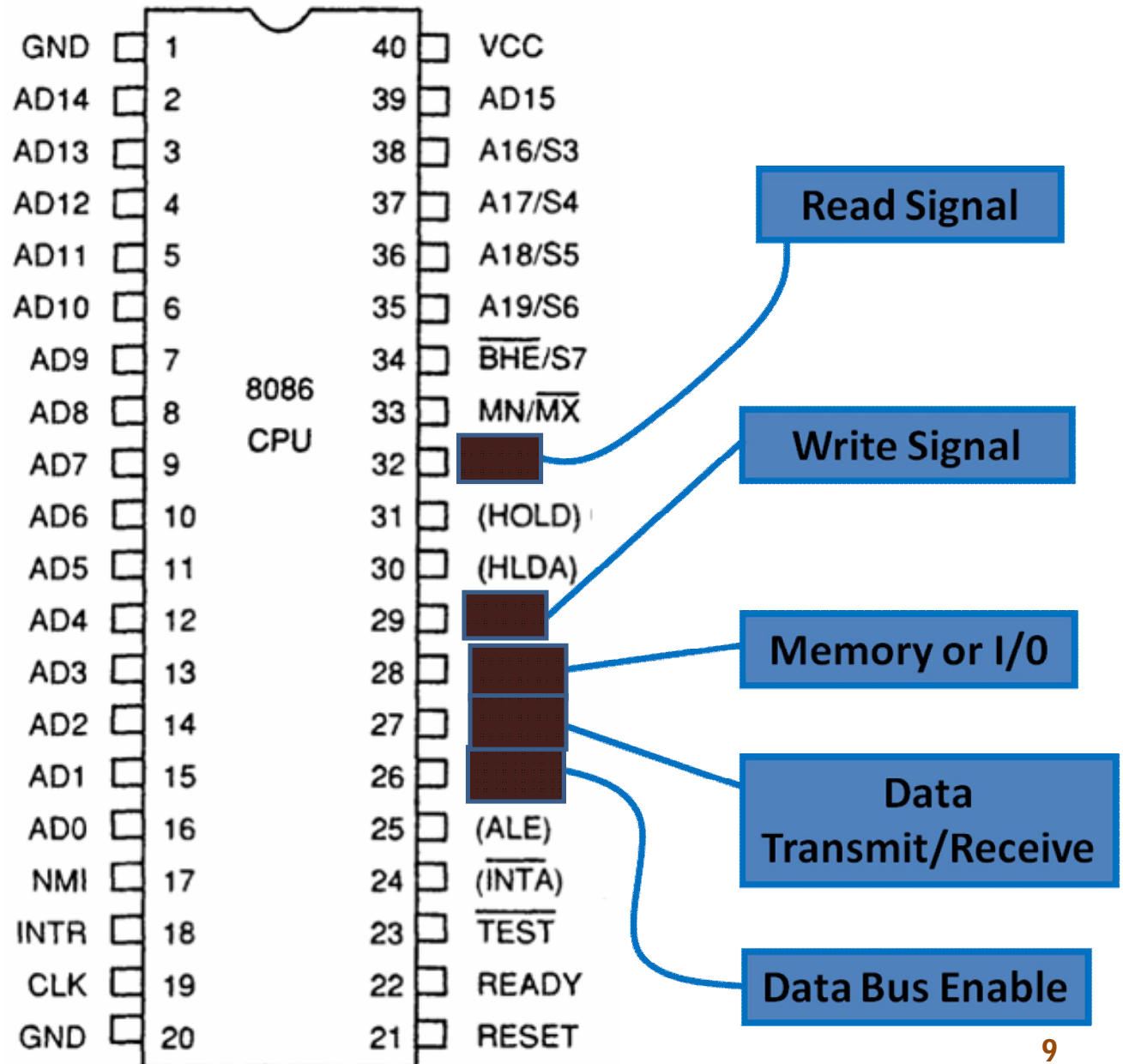
Enables most significant data bits D₁₅ – D₈ during read or write operation.

S₇: Always 1.

INTEL 8086 - Pin Details



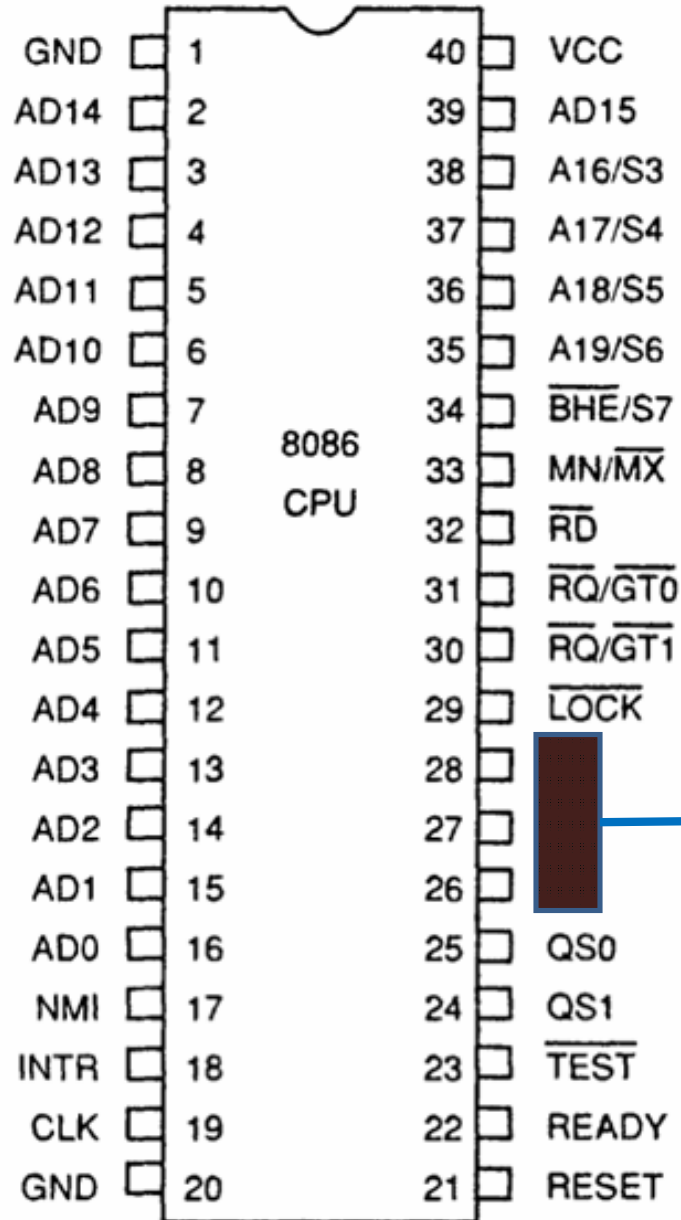
Minimum Mode- Pin Details



Maximum Mode - Pin Details

S2 S1 S0

000: INTA
001: read I/O port
0010: write I/O port
011: halt
100: code access
101: read memory
110: write memory
111: none -passive



Status Signal

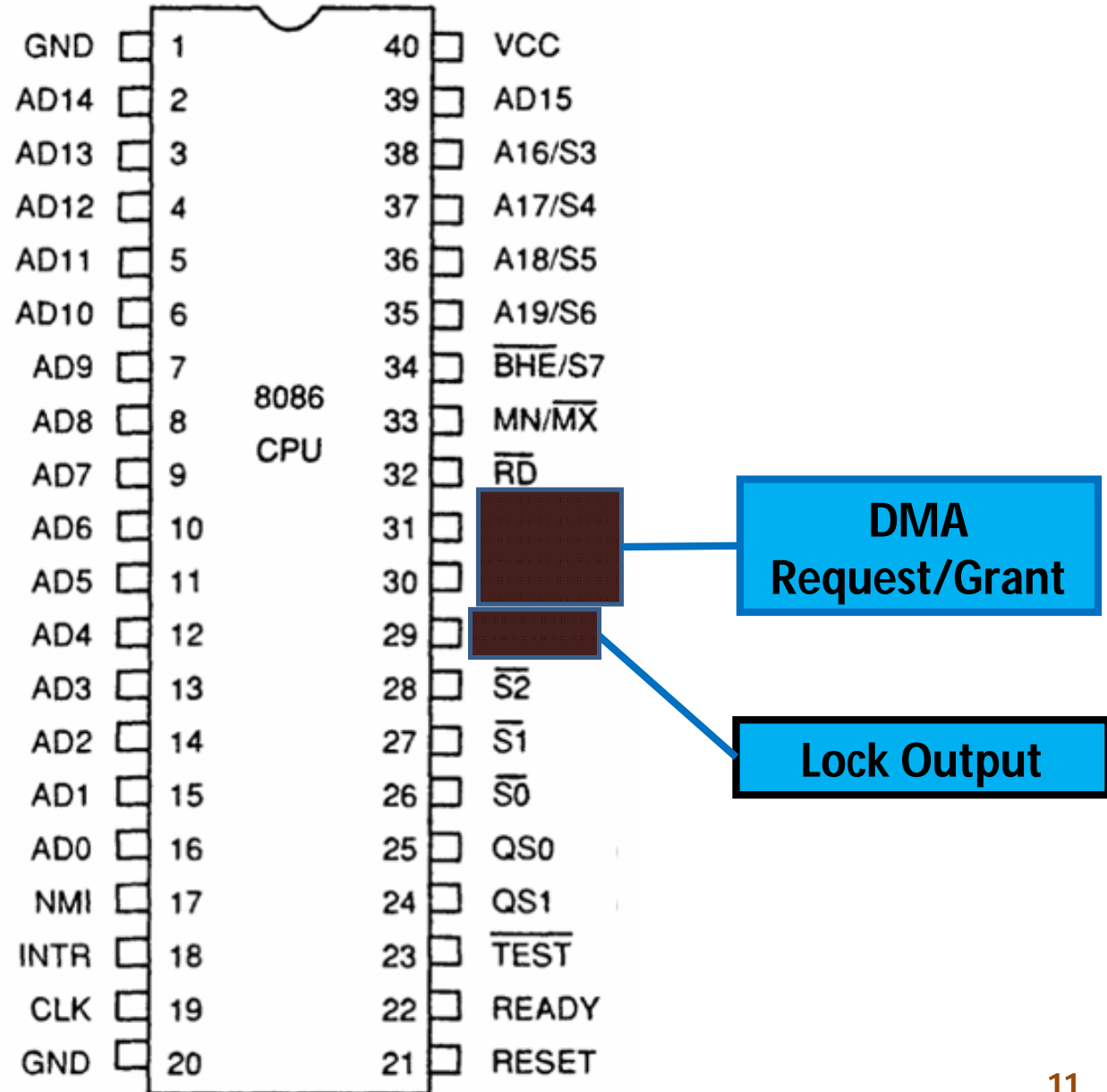
Inputs to 8288 to generate eliminated signals due to max mode.

Maximum Mode - Pin Details

Lock Output

Used to lock peripherals off the system

Activated by using the LOCK: prefix on any instruction



Maximum Mode - Pin Details

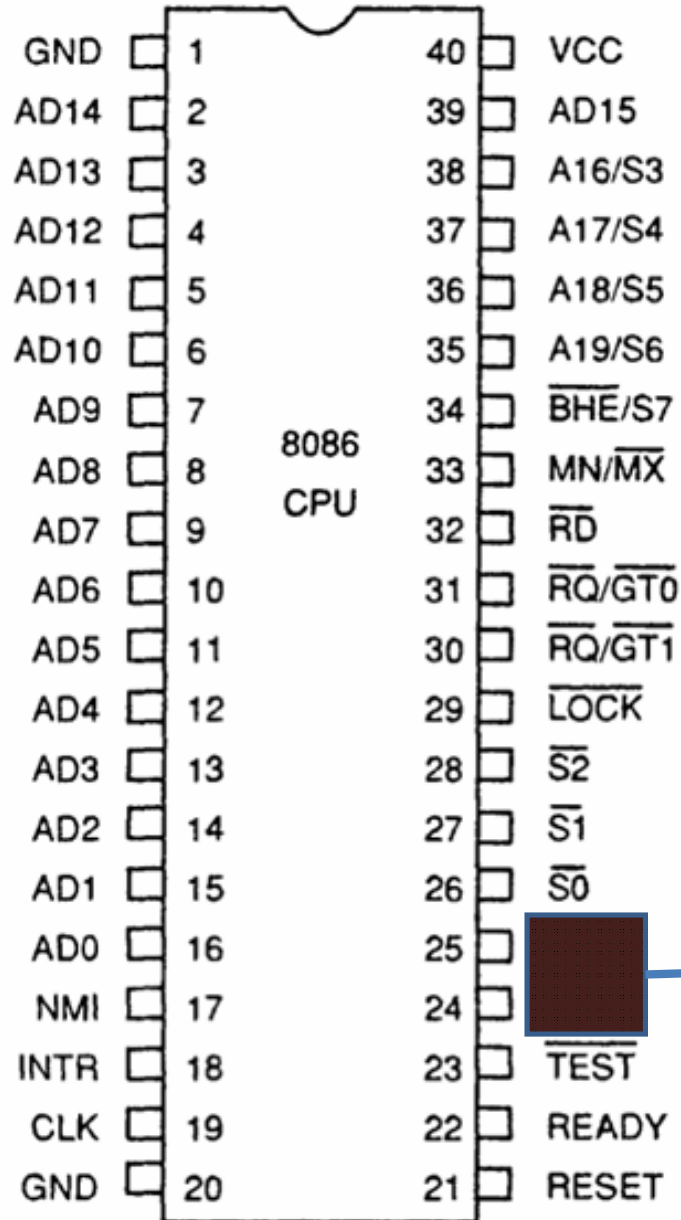
QS1 QS0

00: Queue is idle

01: First byte of opcode

10: Queue is empty

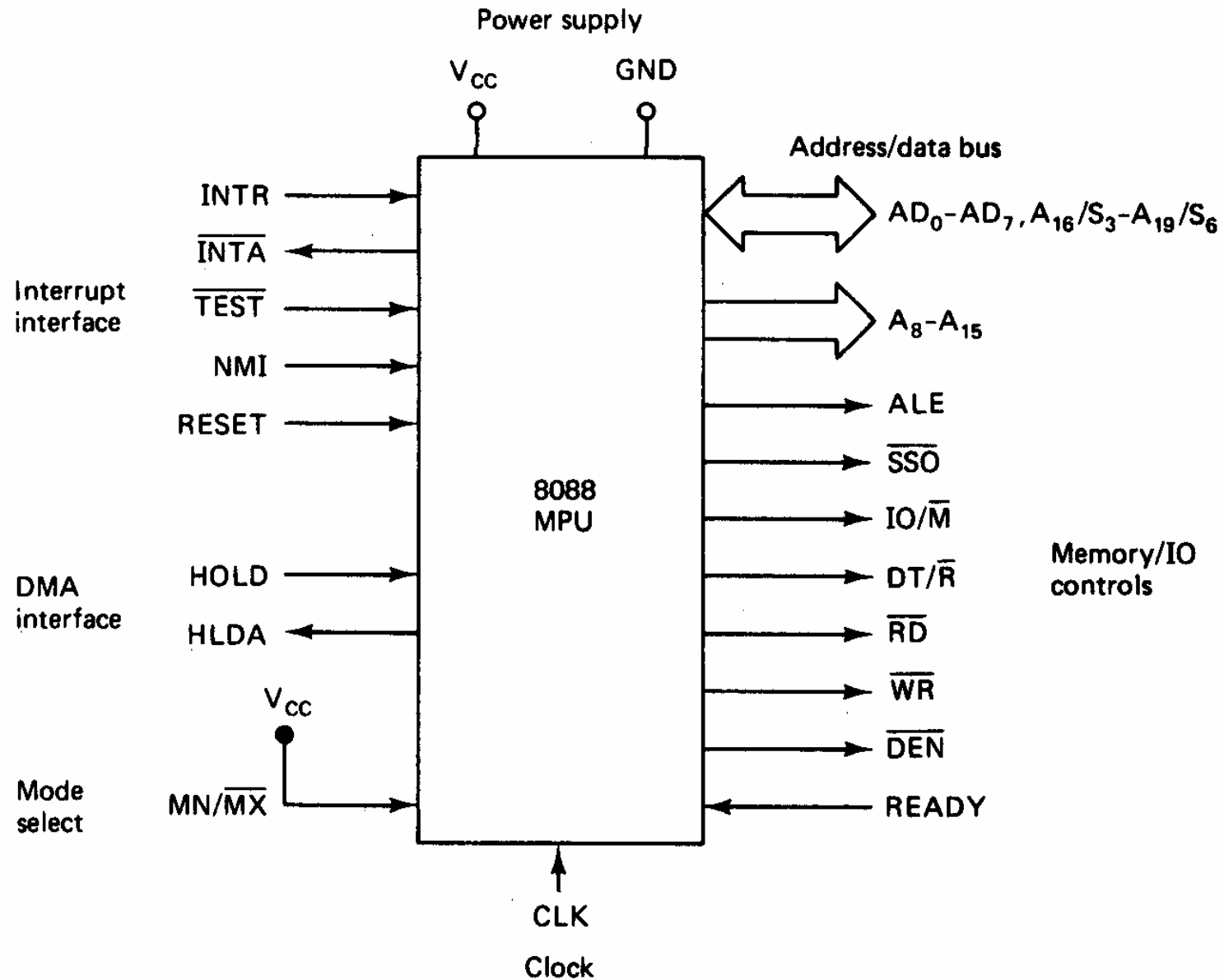
11: Subsequent byte of opcode



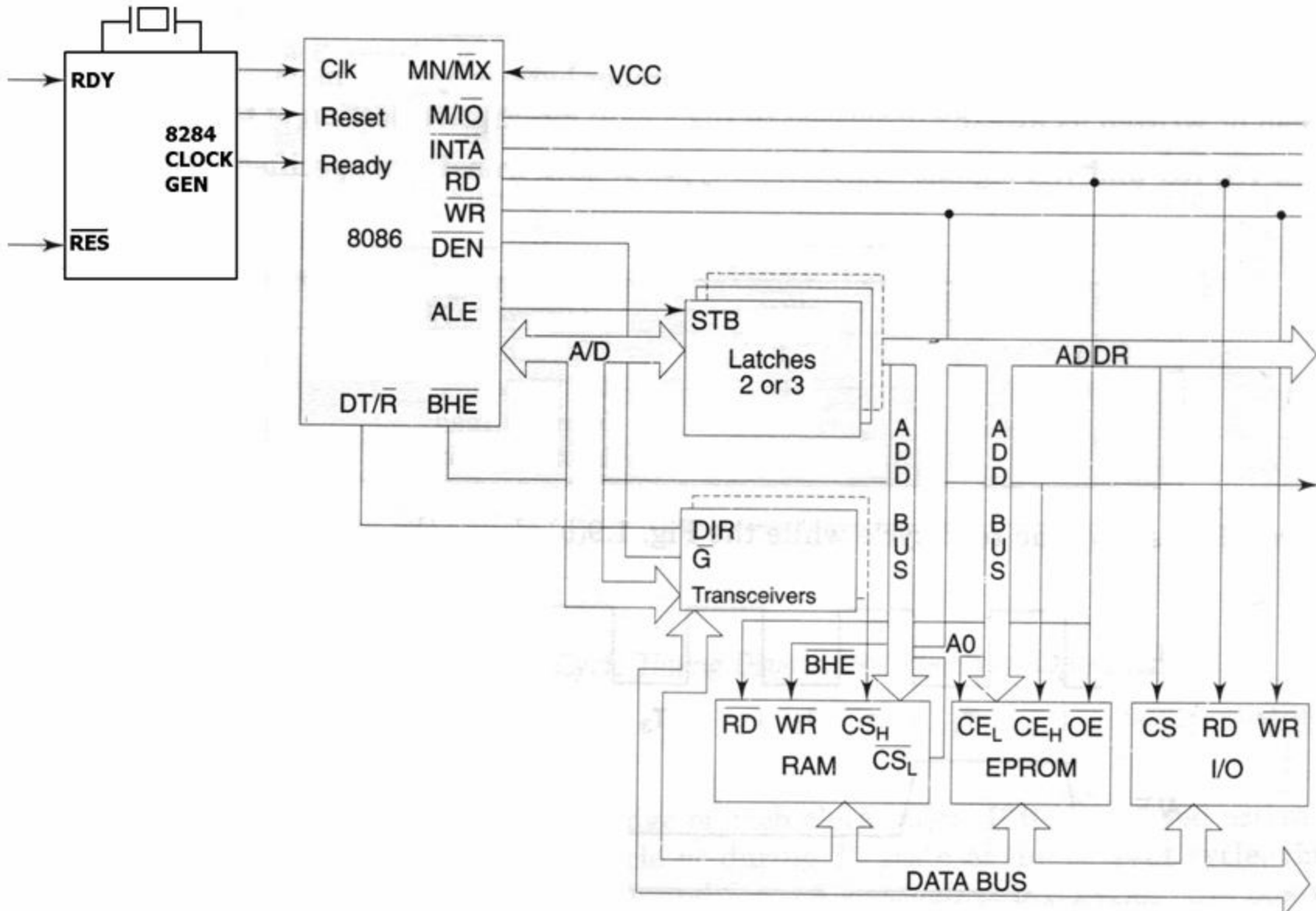
Queue Status

Used by numeric coprocessor (8087)

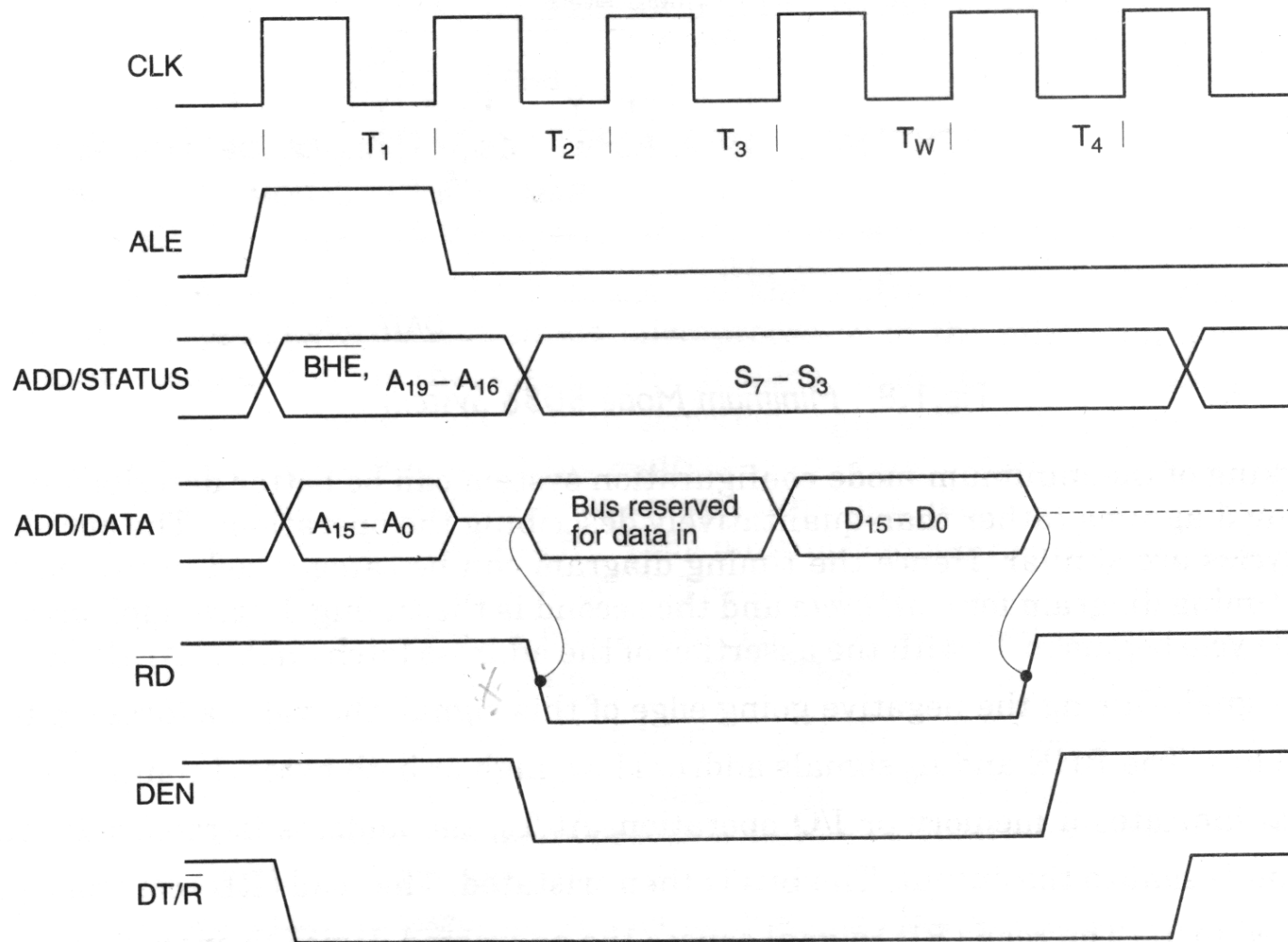
Minimum Mode 8086 System



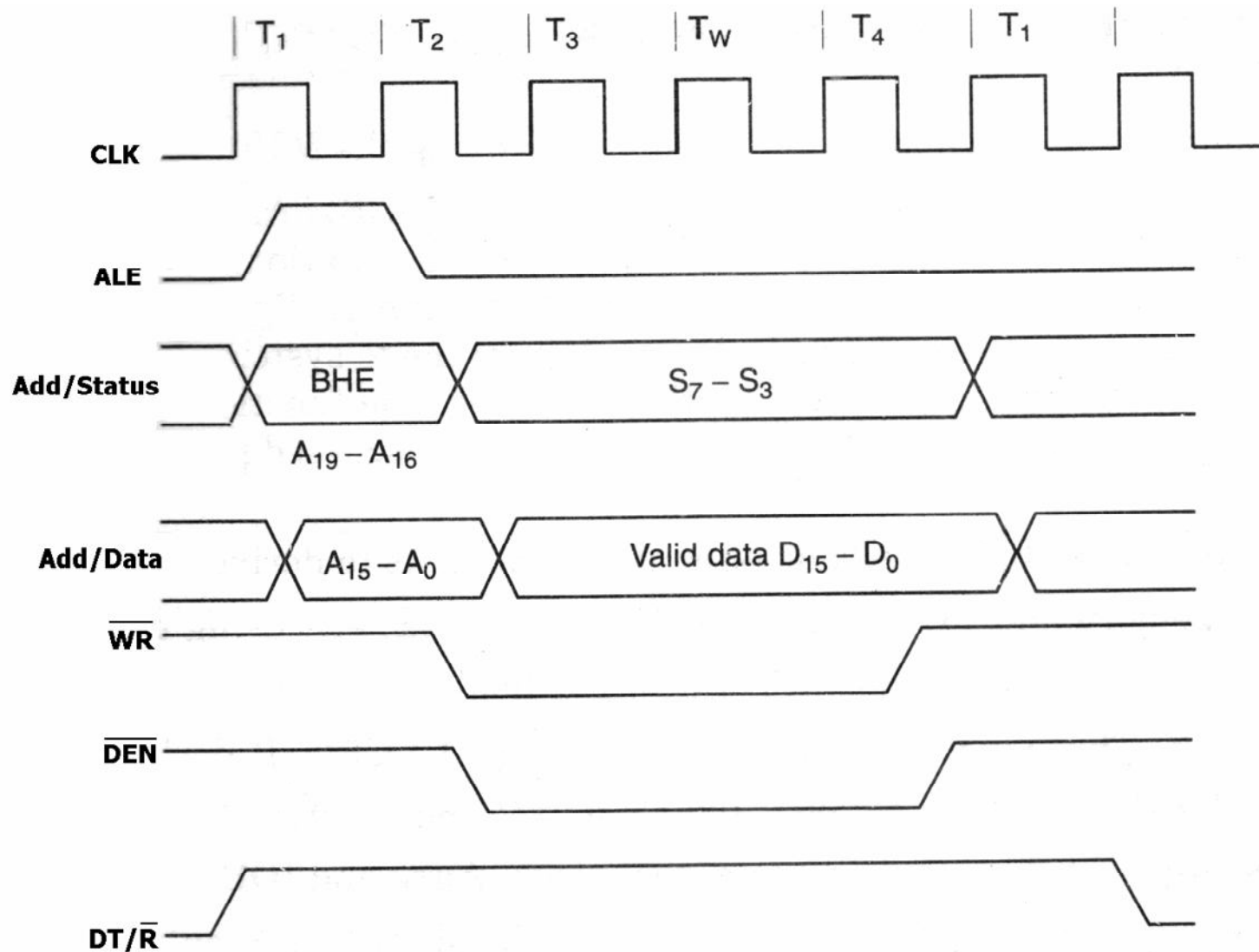
Minimum Mode 8086 System



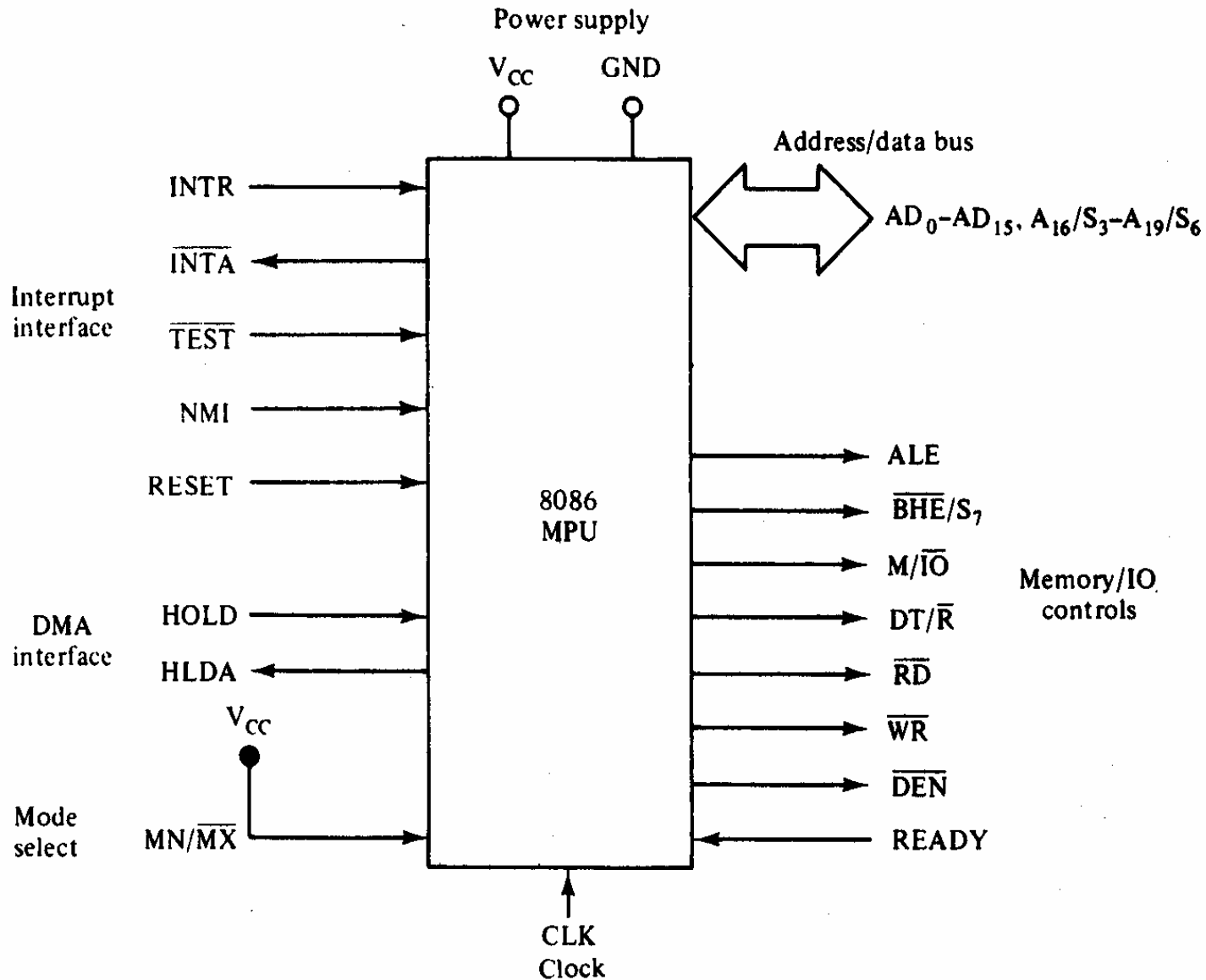
'Read' Cycle timing Diagram for Minimum Mode



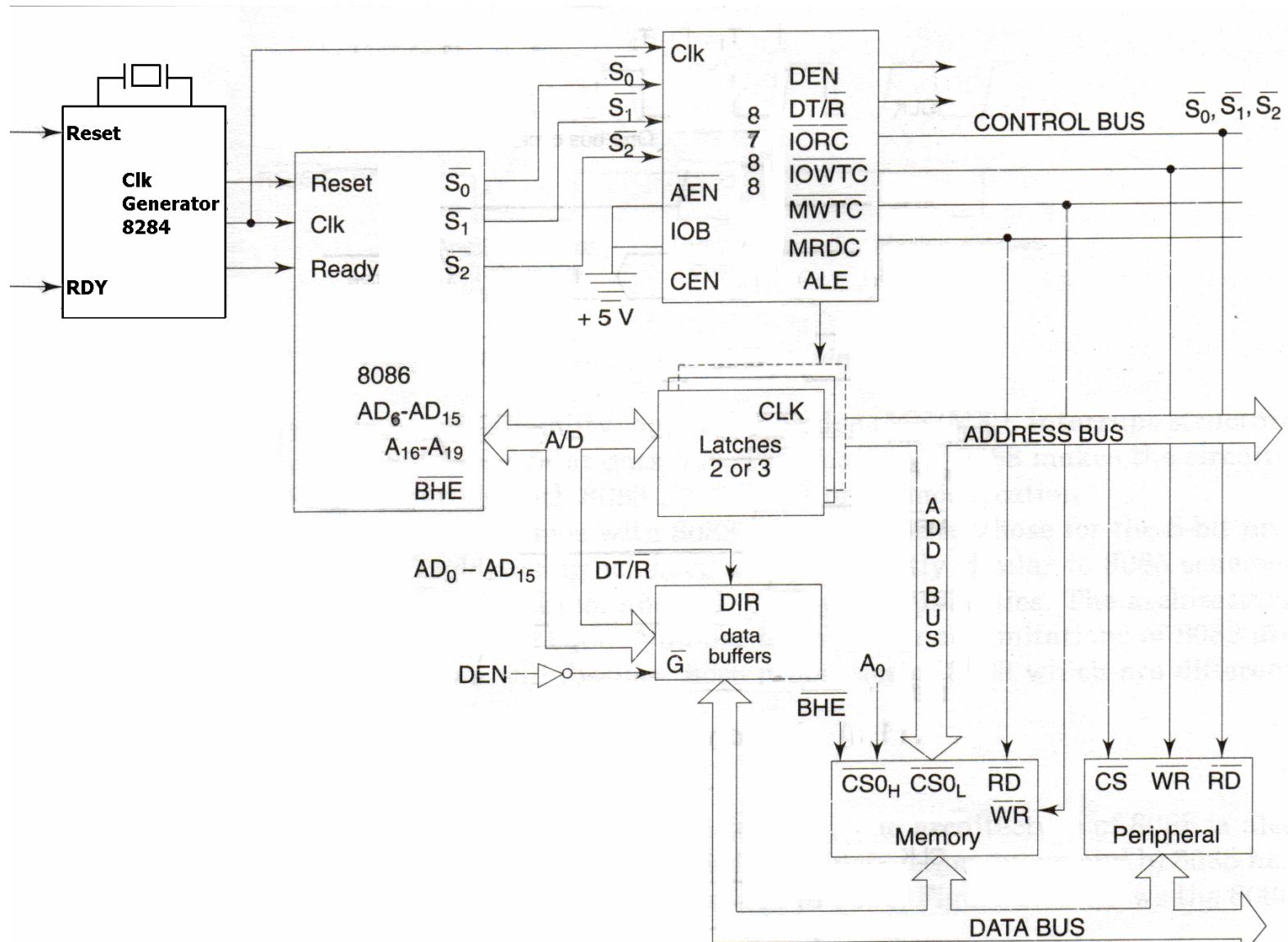
'Write' Cycle timing Diagram for Minimum Mode



Maximum Mode 8086 System



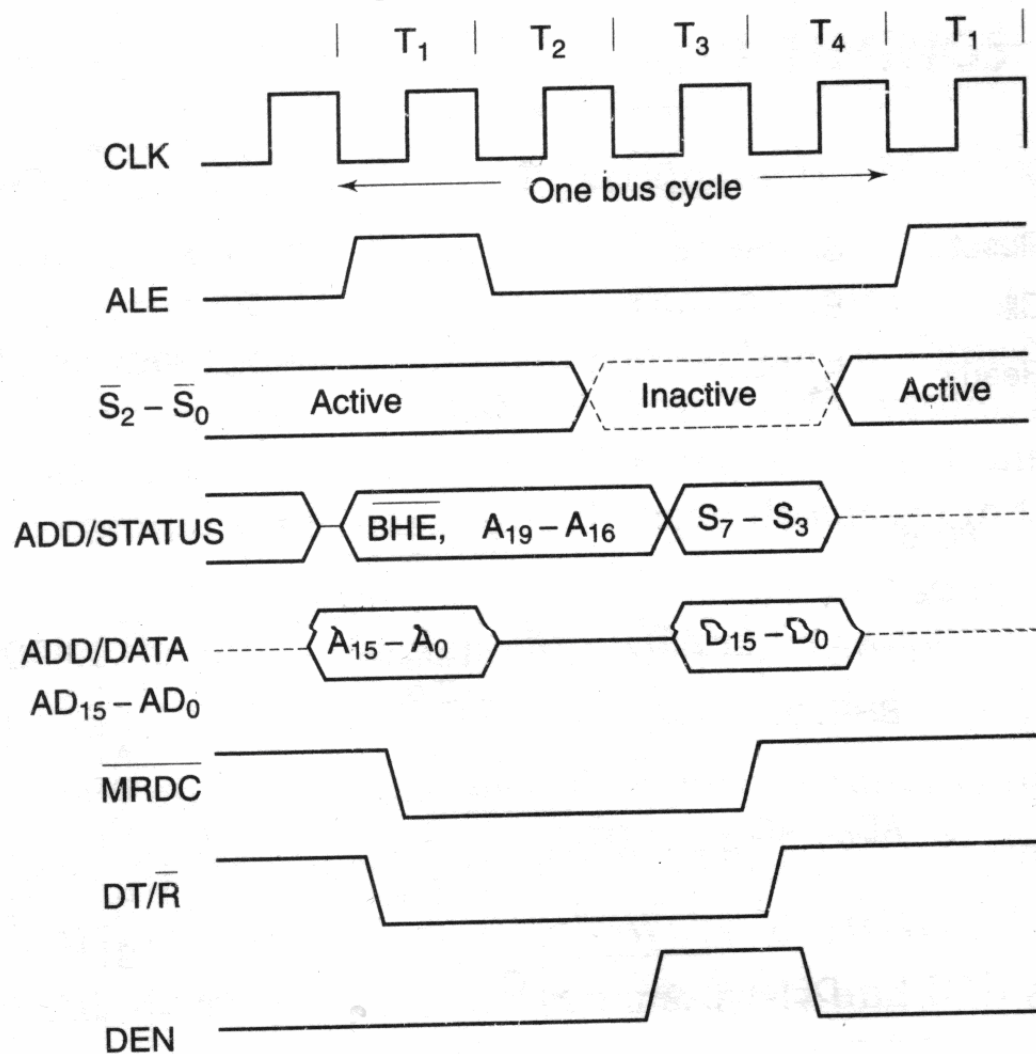
Maximum Mode 8086 System



Maximum Mode 8086 System

- Here, either a numeric coprocessor of the type 8087 or another processor is interfaced with 8086.
- The Memory, Address Bus, Data Buses are shared resources between the two processors.
- The control signals for Maximum mode of operation are generated by the Bus Controller chip 8788.
- The three status outputs $S0^*$, $S1^*$, $S2^*$ from the processor are input to 8788.
- The outputs of the bus controller are the Control Signals, namely DEN , DT/R^* , $IORC^*$, $IOWTC^*$, $MWTC^*$, $MRDC^*$, ALE etc.

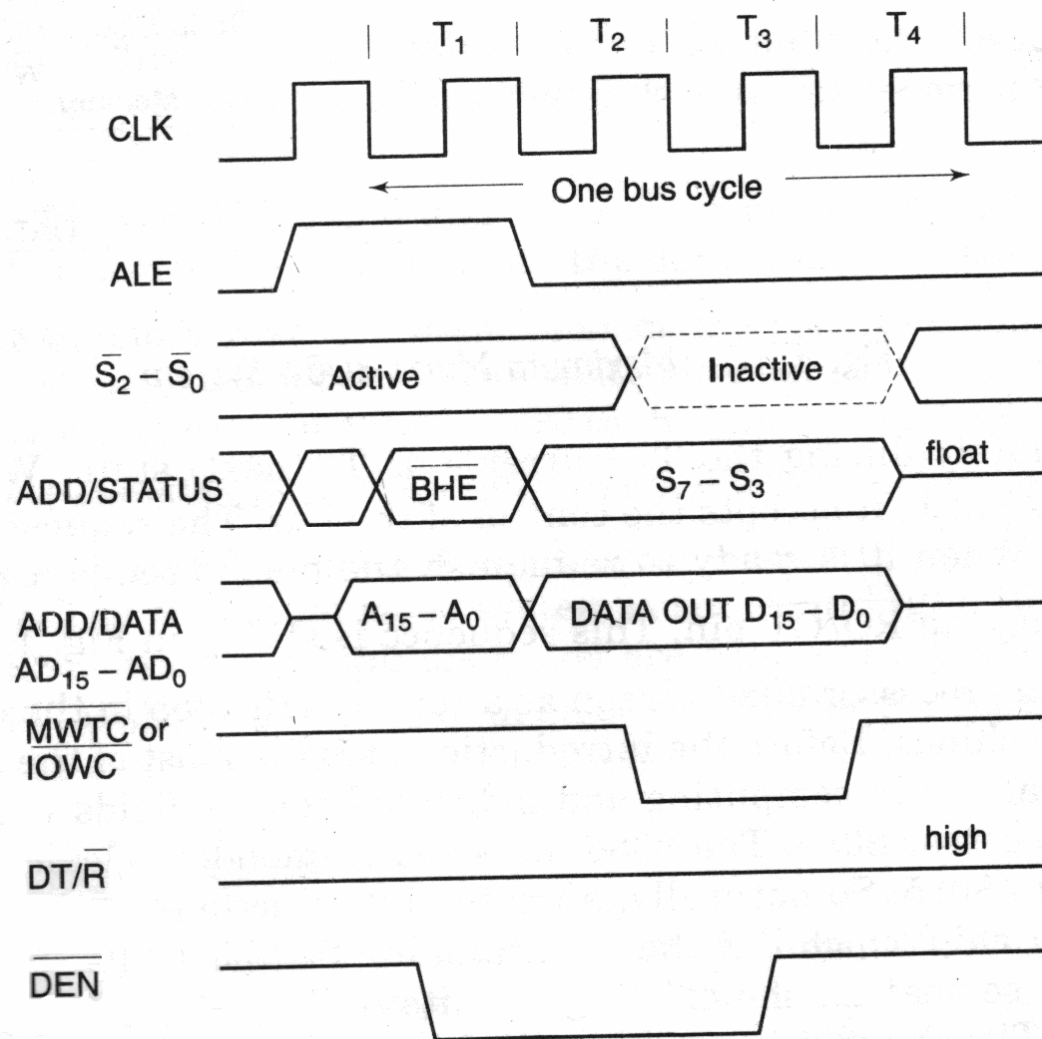
Memory Read timing in Maximum Mode



$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Function
0	0	0	Interrupt acknowledge
0	0	1	I/O read
0	1	0	I/O write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive

TABLE 8-6 Bus control functions generated by the bus controller (8288) using $\overline{S_2}$, $\overline{S_1}$, and $\overline{S_0}$

Memory Write timing in Maximum Mode

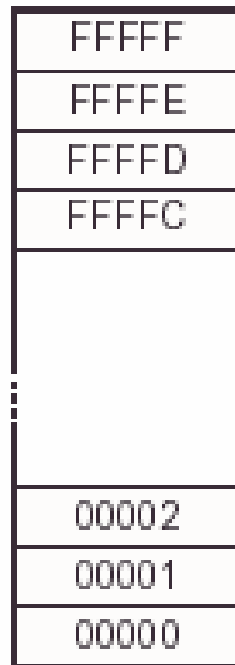


$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Function
0	0	0	Interrupt acknowledge
0	0	1	I/O read
0	1	0	I/O write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive

TABLE 8-6 Bus control functions generated by the bus controller (8288) using $\overline{S_2}$, $\overline{S_1}$, and $\overline{S_0}$

Memory Banking

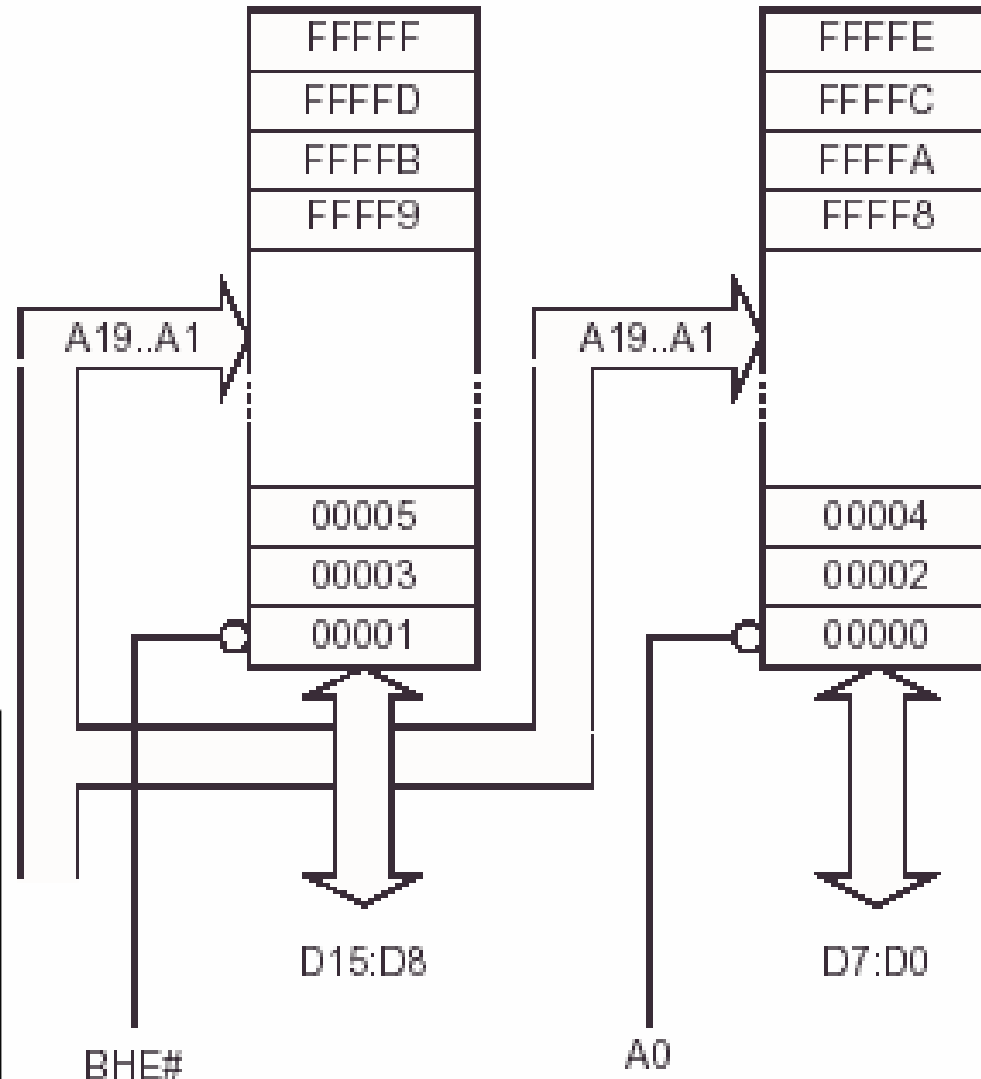
Byte-Wide addressing
(8088)



BHE	A0	CHARACTERISTICS
0	0	Whole word
0	1	Upper Byte From/To Odd Address
1	0	Lower Byte From/To Even Address
1	1	None

ODD Addresses (8086)

EVEN Addresses (8086)



8086 Control Signals

1. ALE
2. BHE
3. M/IO
4. DT/R
5. RD
6. WR
7. DEN