8251-USART

8251 USART

- The 8251 USART (Universal Synchronous Asynchronous Receiver Transmitter) is capable of implementing either an asynchronous or synchronous serial data communication.
- As a peripheral device of a microcomputer system, the 8251 receives parallel data from the CPU and transmits serial data after conversion. This device also receives serial data from the outside and transmits parallel data to the CPU after conversion

What is Serial Communications

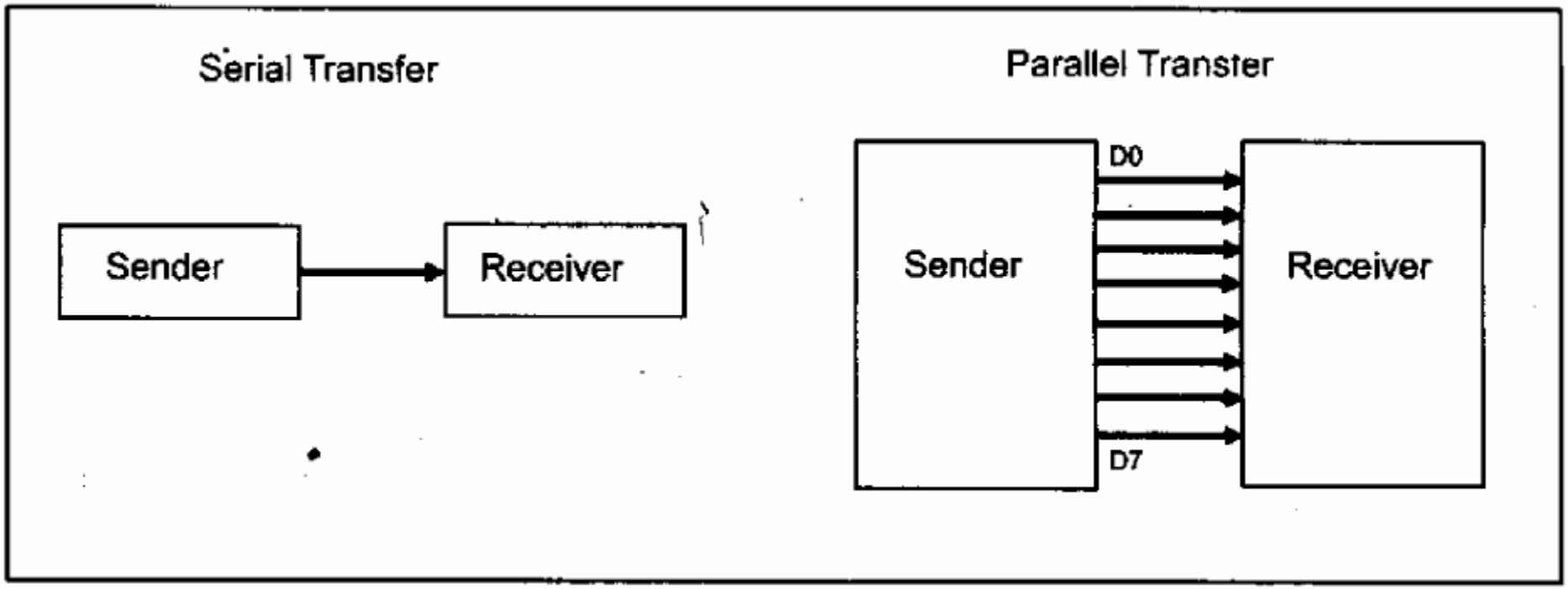


Figure 9-1. Serial vs. Parallel Data Transfer

Serial Communication Types

- Asynchronous
- Synchronous
- Transfer:
  - Simplex
  - Half duplex
  - Full duplex

Transfer Types

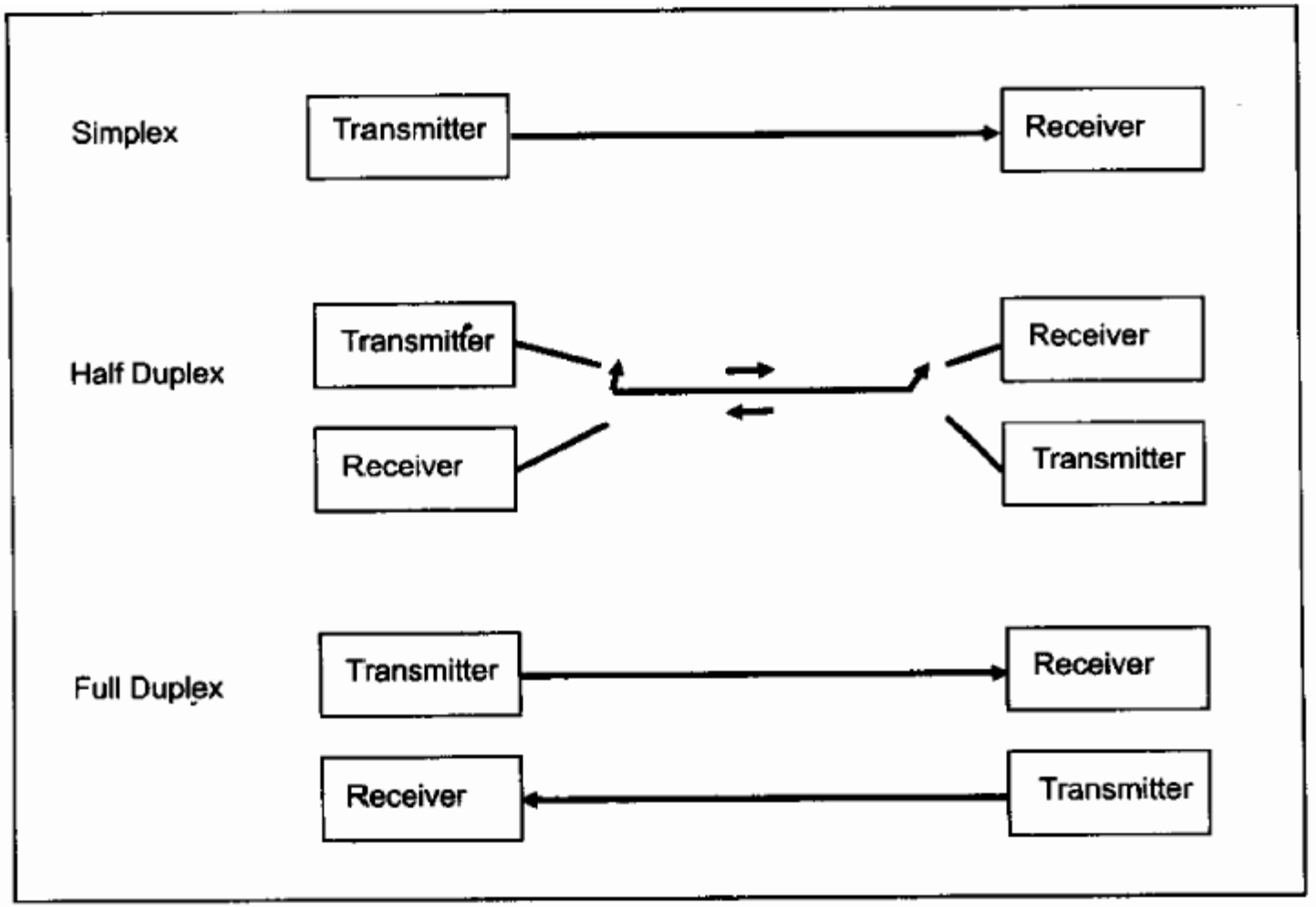
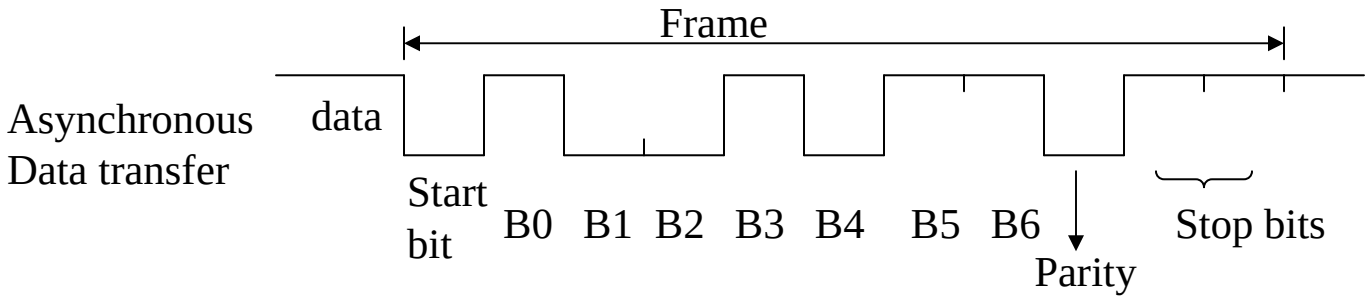
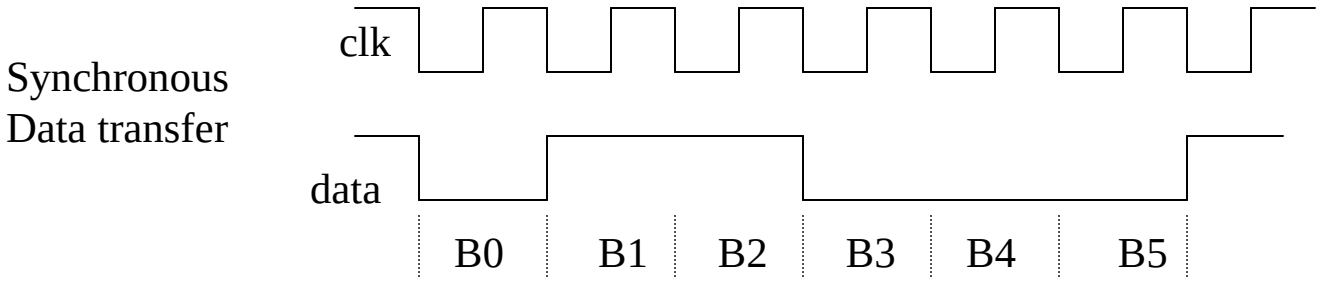


Figure 9-2. Simplex, Half- and Full-Duplex Transfers

Serial Data Transfer

- Asynchronous ***v.s.*** Synchronous
  - — Asynchronous transfer does not require clock signal. However, it transfers extra bits (start bits and stop bits) during data communication
  - — Synchronous transfer does not transfer extra bits. However, it requires clock signal





Asynchronous vs Synchronous

How can the receiver get each data bit when it is delivered by the transmitter?

- In synchronous transmission an explicit clock signal describes the instants of valid data. A single data bit is sent at each clock.
- Minimum three signal lines required for full duplex, Receive-DATA, Transmit-DATA, and CLOCK.

- In asynchronous transmission clock is derived using a-priory parameters and a start bit. Transfer rate known, internal clock starts to pulse with the start bit, at the known transfer rate. Ony two signal lines required for full duplexReceive-DATA and Transmit-DATA

Asynchronous Data Framing

- Start bit is required to synchronize the internal clock of receiver.
- Stop bit is required to test the clock frequency.
- Only DATA is transmitted, internal clock is generated locally.

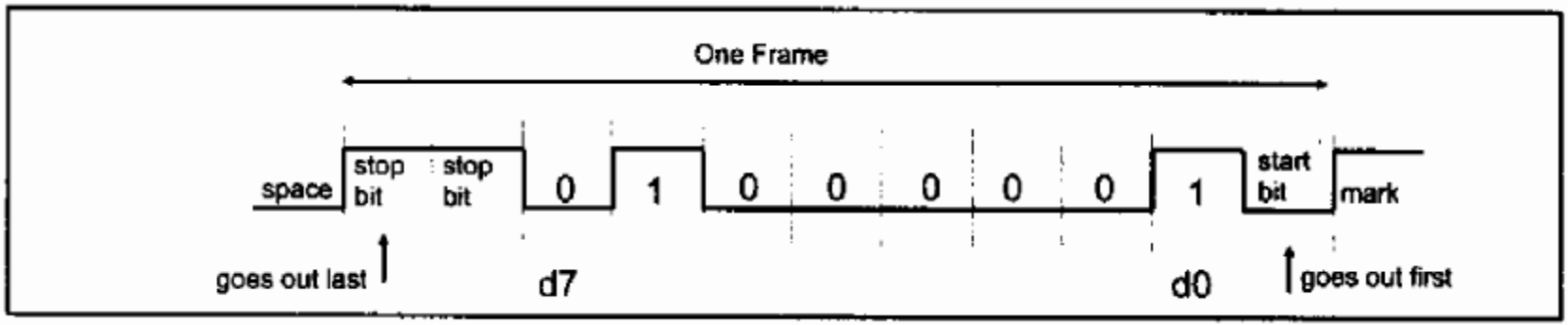
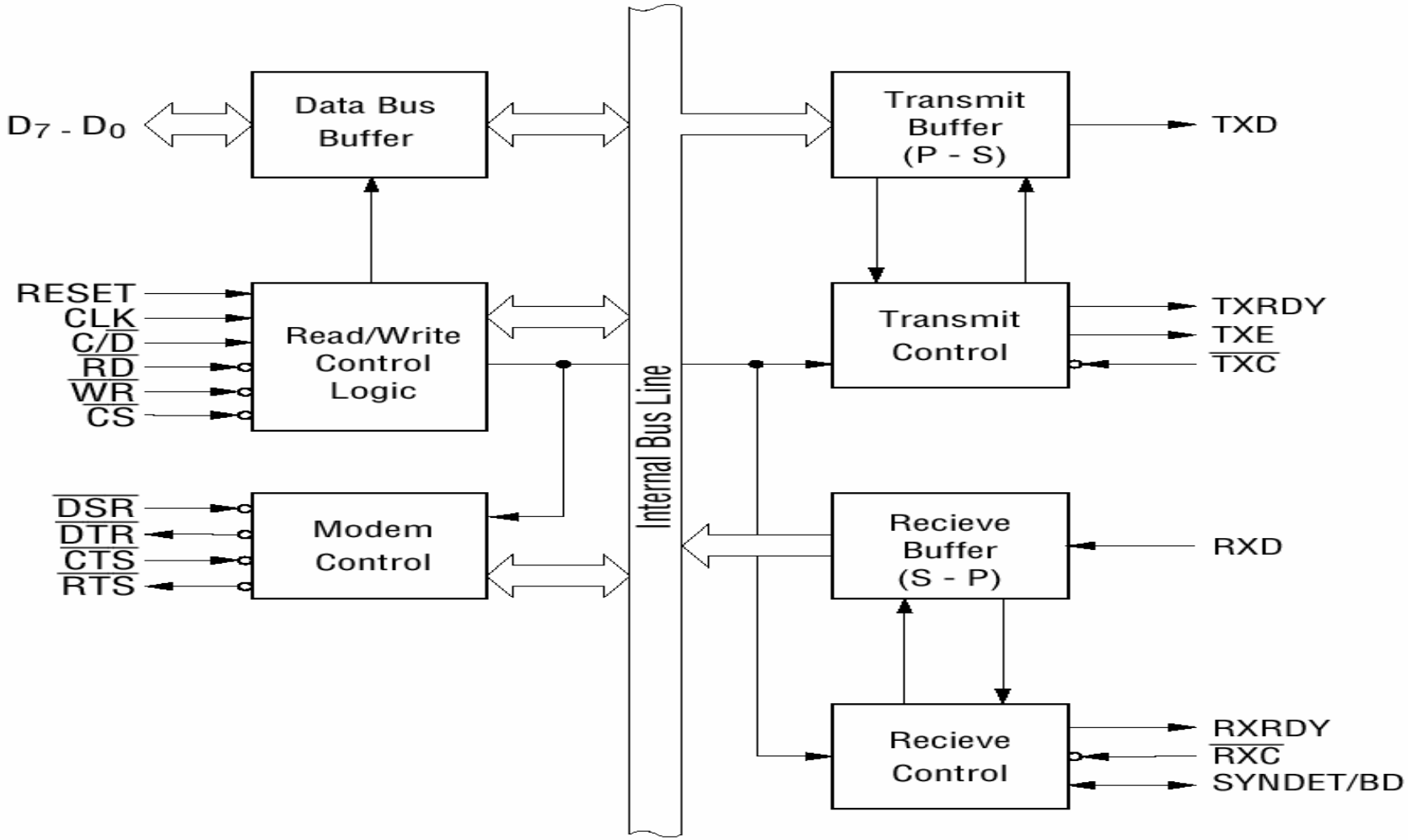


Figure 9-3. Framing ASCII "A" (41H)

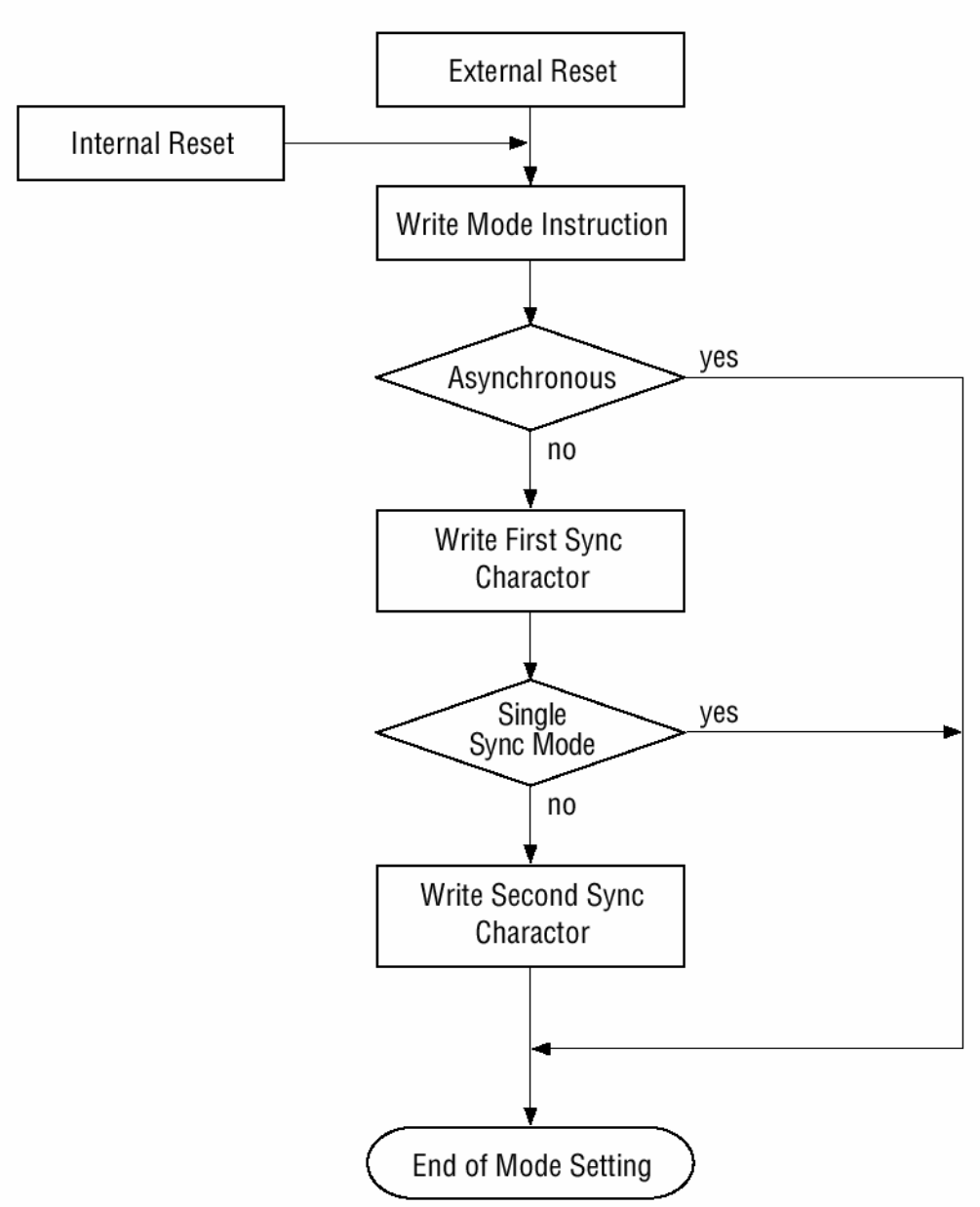
Block diagram of 8251



8251 Registers

$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	
1	×	×	×	Data Bus 3-State
0	×	1	1	Data Bus 3-State
0	1	0	1	Status → CPU
0	1	1	0	Control Word ← CPU
0	0	0	1	Data → CPU
0	0	1	0	Data ← CPU

Mode Register



- **DATA BUFFER** :- This data buffer interfaces the internal bus of 8251 with the system bus. This can transfer data and control word.
- **READ/WRITE Control Logic**:- This READ/WRITE control logic controls the operation of the peripheral depending on the operations initiated by the CPU. This unit also selects one of the two internal addresses i.e., control address or data address with the help of C/D signal.
- **Modem Control Unit**: - This modem control unit handles the modem handshake signals to coordinate the communication between modem and the USART. Modem is used as a modulating/demodulating device.
- **Transmit Control**: - This unit transmits the data byte received by the data buffer from the CPU, for further serial communication. The transmit rate is controlled by the T x C input frequency of this unit. This also contain two status signal named T x RDY and T x EMPTY. Which the CPU for handshaking can use?
- **Transmit Buffer**: - This transmit buffer is a parallel to serial converter that receives parallel byte of data from CPU for conversion into a serial signal. This unit transmits this serial signal onto the communication channel.
- **Receive Control** :- This receive control unit decides the receive frequency . Which does the R x C input frequency control? This unit **Receive Control** :- This receive control unit decides the receive frequency . Which does the R x C input frequency control? This unit generates a R x RDY receiver ready signal that can be used by the CPU for handshaking. This unit also detects the break in the data string while 8251 is in a synchronous mode and detects the synchronous characters in synchronous mode. Using the SYNDET/BD pin.
- **Receiver Buffer** :- This can be considered as a serial to parallel converter which can receive the serial stream of data and convert it in to parallel data format for transmitting it to the CPU.

Pin Description

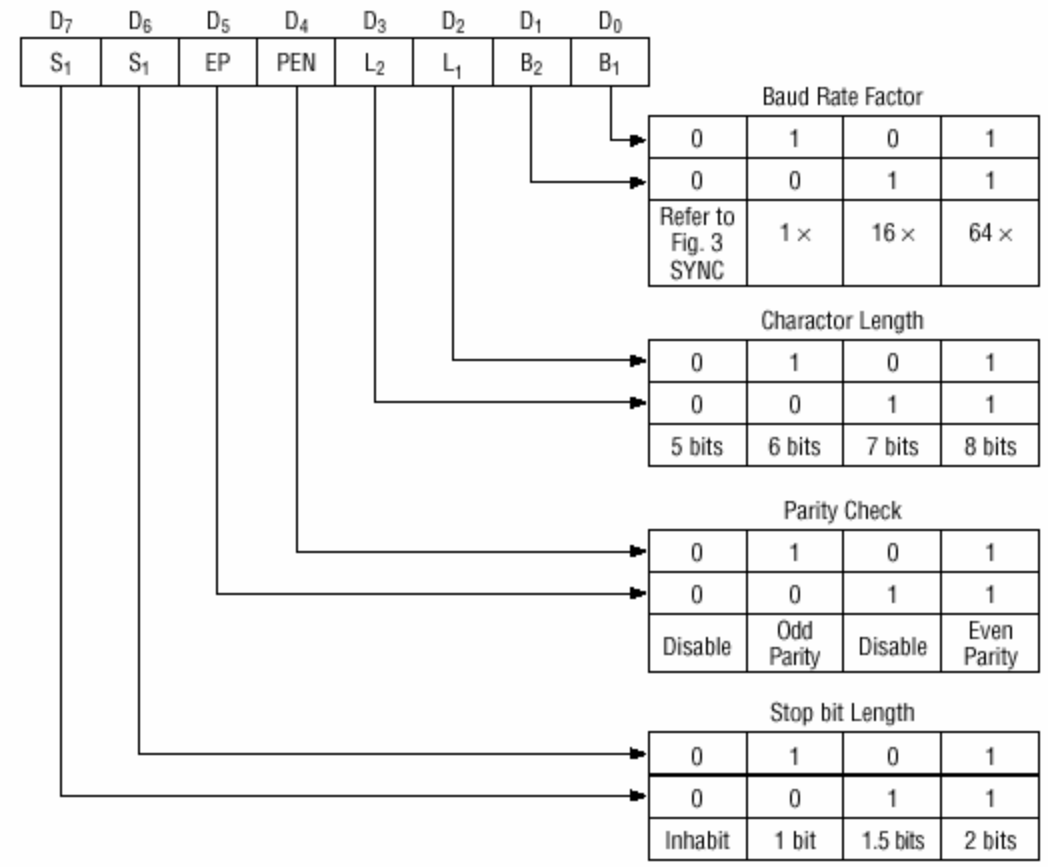
- **D 0 to D 7 (I/O terminal)**
- This is bidirectional data bus which receive control words and transmits data from the CPU and sends status words and received data to CPU.
- **RESET (Input terminal)**
- A "High" on this input forces the 8251 into "reset status." The device waits for the writing of "mode instruction." The min. reset width is six clock inputs during the operating status of CLK.
- **CLK (Input terminal)**
- CLK signal is used to generate internal device timing. CLK signal is independent of RXC or TXC. However, the frequency of CLK must be greater than 30 times the RXC and TXC at Synchronous mode and Asynchronous "x1" mode, and must be greater than 5 times at Asynchronous "x16" and "x64" mode.
- **WR (Input terminal)**
- This is the "active low" input terminal which receives a signal for writing transmit data and control words from the CPU into the 8251.
- **RD (Input terminal)**
- This is the "active low" input terminal which receives a signal for reading receive data and status words from the 8251.
- **C/D (Input terminal)**
- This is an input terminal which receives a signal for selecting data or command words and status words when the 8251 is accessed by the CPU. If C/D = low, data will be accessed. If C/D = high, command word or status word will be accessed.

- **CS (Input terminal)**
- This is the "active low" input terminal which selects the 8251 at low level when the CPU accesses. Note: The device won’t be in "standby status"; only setting CS = High.
- **TXD (output terminal)**
- This is an output terminal for transmitting data from which serial-converted data is sent out. The device is in "mark status" (high level) after resetting or during a status when transmit is disabled. It is also possible to set the device in "break status" (low level) by a command.
- **TXRDY (output terminal)**
- This is an output terminal which indicates that the 8251is ready to accept a transmitted data character. But the terminal is always at low level if CTS = high or the device was set in "TX disable status" by a command. Note: TXRDY status word indicates that transmit data character is receivable, regardless of CTS or command. If the CPU writes a data character, TXRDY will be reset by the leading edge or WR signal.
- **TXEMPTY (Output terminal)**
- This is an output terminal which indicates that the 8251 has transmitted all the characters and had no data character. In "synchronous mode," the terminal is at high level, if transmit data characters are no longer remaining and sync characters are automatically transmitted. If the CPU writes a data character, TXEMPTY will be reset by the leading edge of WR signal. Note : As the transmitter is disabled by setting CTS "High" or command, data written before disable will be sent out. Then TXD and TXEMPTY will be "High". Even if a data is written after disable, that data is not sent out and TXE will be "High".After the transmitter is enabled, it sent out. (Refer to Timing Chart of Transmitter Control and Flag Timing)

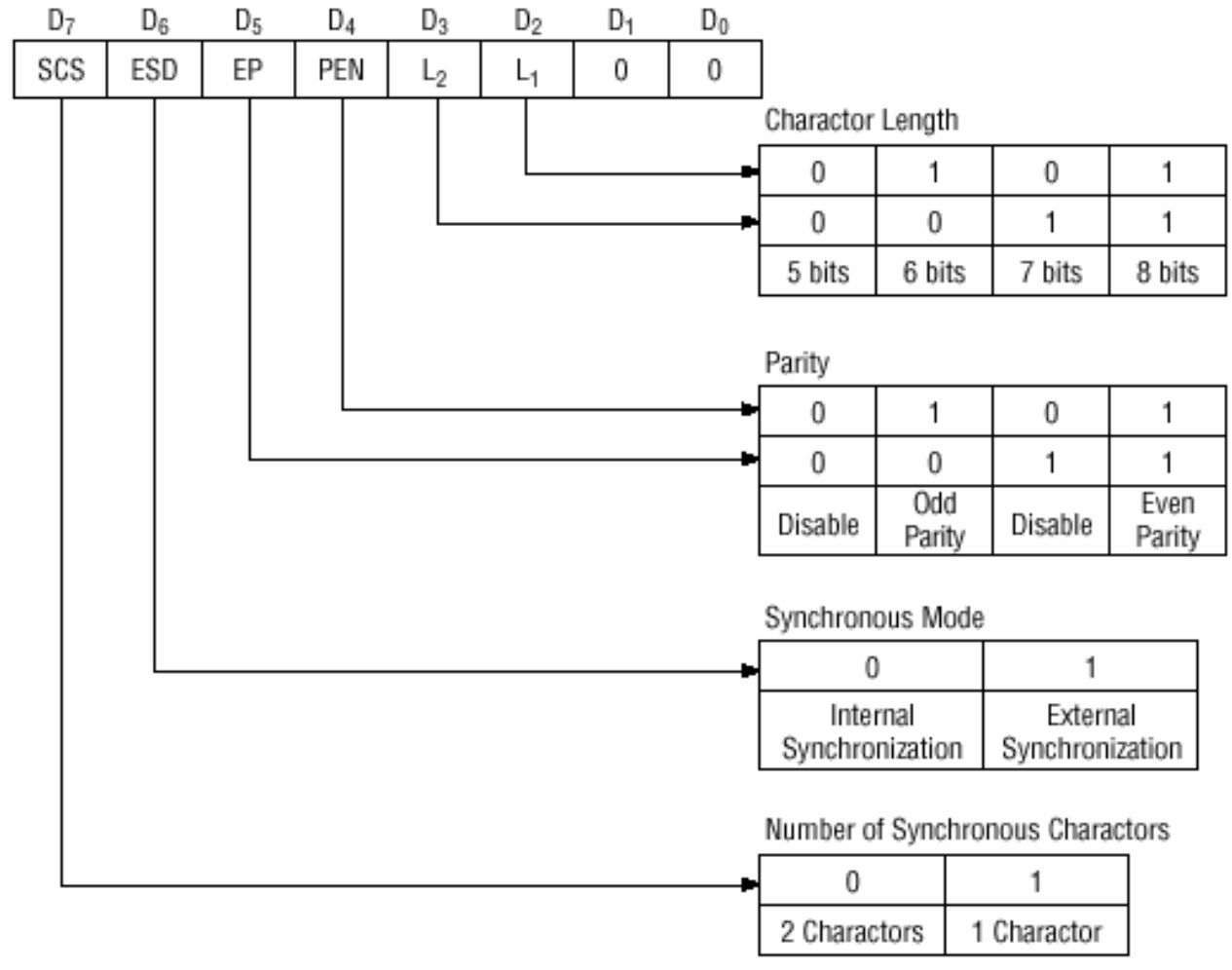
- **TXC (Input terminal)**
- This is a clock input signal which determines the transfer speed of transmitted data. In "synchronous mode," the baud rate will be the same as the frequency of TXC. In "asynchronous mode", it is possible to select the baud rate factor by mode instruction. It can be 1, 1/16 or 1/64 the TXC. The falling edge of TXC sifts the serial data out of the 8251.
- **RXD (input terminal)**
- This is a terminal which receives serial data.
- **RXRDY (Output terminal)**
- This is a terminal which indicates that the 8251 contains a character that is ready to READ. If the CPU reads a data character, RXRDY will be reset by the leading edge of RD signal. Unless the CPU reads a data character before the next one is received completely, the preceding data will be lost. In such a case, an overrun error flag status word will be set.
- **RXC (Input terminal)**
- This is a clock input signal which determines the transfer speed of received data. In "synchronous mode," the baud rate is the same as the frequency of RXC. In "asynchronous mode," it is possible to select the baud rate factor by mode instruction. It can be 1, 1/16, 1/64 the RXC.

- **SYNDET/BD (Input or output terminal)**
- This is a terminal whose function changes according to mode. In "internal synchronous mode." this terminal is at high level, if sync characters are received and synchronized. If a status word is read, the terminal will be reset. In "external synchronous mode, "this is an input terminal. A "High" on this input forces the 8251 to start receiving data characters.
- In "asynchronous mode," this is an output terminal which generates "high level"output upon the detection of a "break" character if receiver data contains a "low-level" space between the stop bits of two continuous characters. The terminal will be reset, if RXD is at high level. After Reset is active, the terminal will be output at low level.
- **DSR (Input terminal)**
- This is an input port for MODEM interface. The input status of the terminal can be recognized by the CPU reading status words.
- **DTR (Output terminal)**
- This is an output port for MODEM interface. It is possible to set the status of DTR by a command.
- **CTS (Input terminal)**
- This is an input terminal for MODEM interface which is used for controlling a transmit circuit. The terminal controls data transmission if the device is set in "TX Enable" status by a command. Data is transmitable if the terminal is at low level.
- **RTS (Output terminal)**
- This is an output port for MODEM interface. It is possible to set the status RTS by a command.

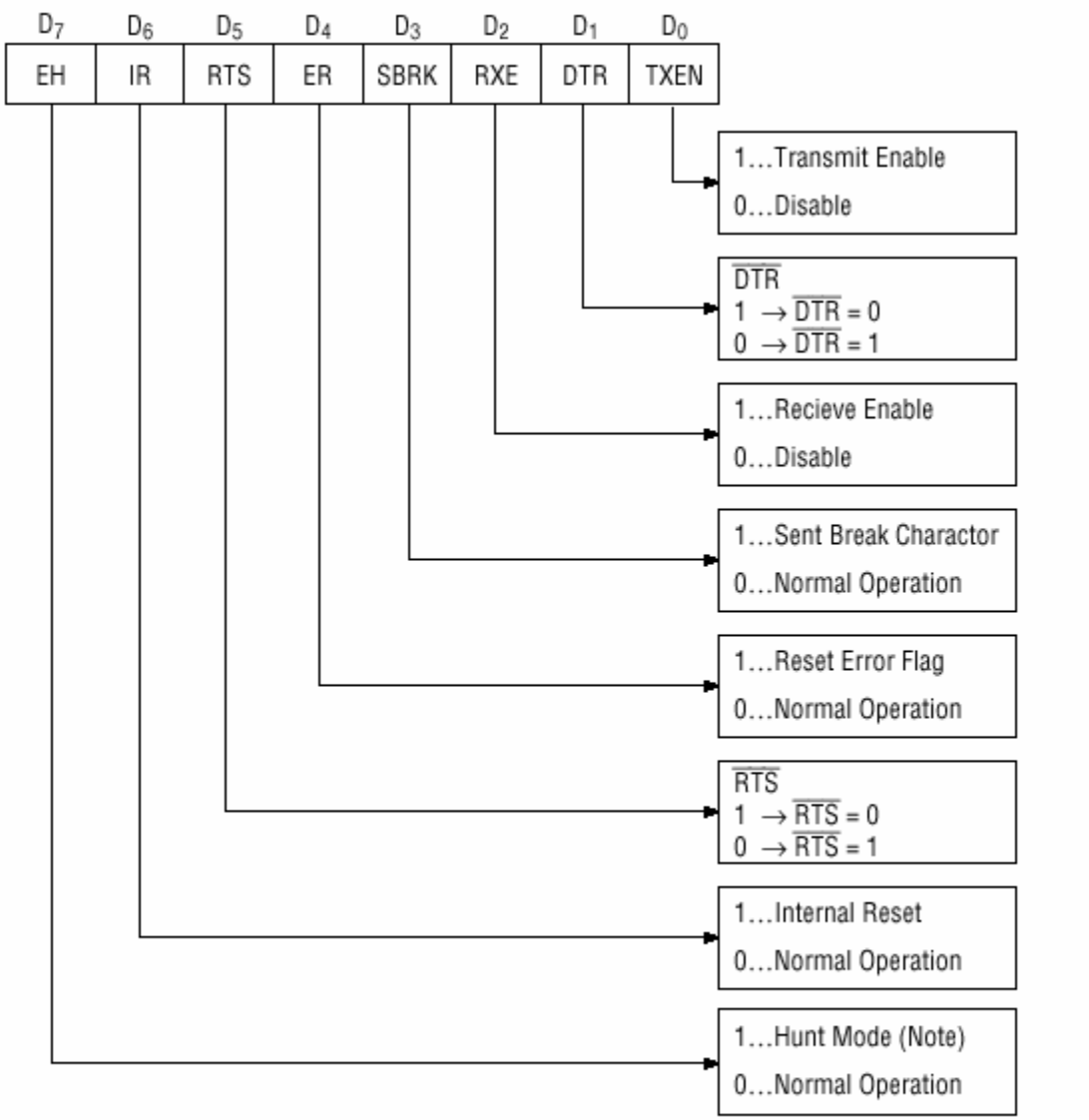
Mode Instruction (Asynchronous)



Mode Instruction (Synchronous)



Command Register



Note: Seach mode for synchronous charactors in synchronous mode.

Status Register