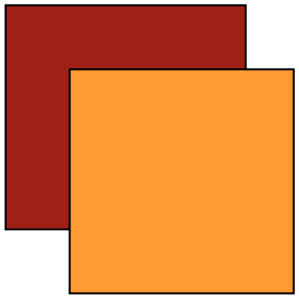
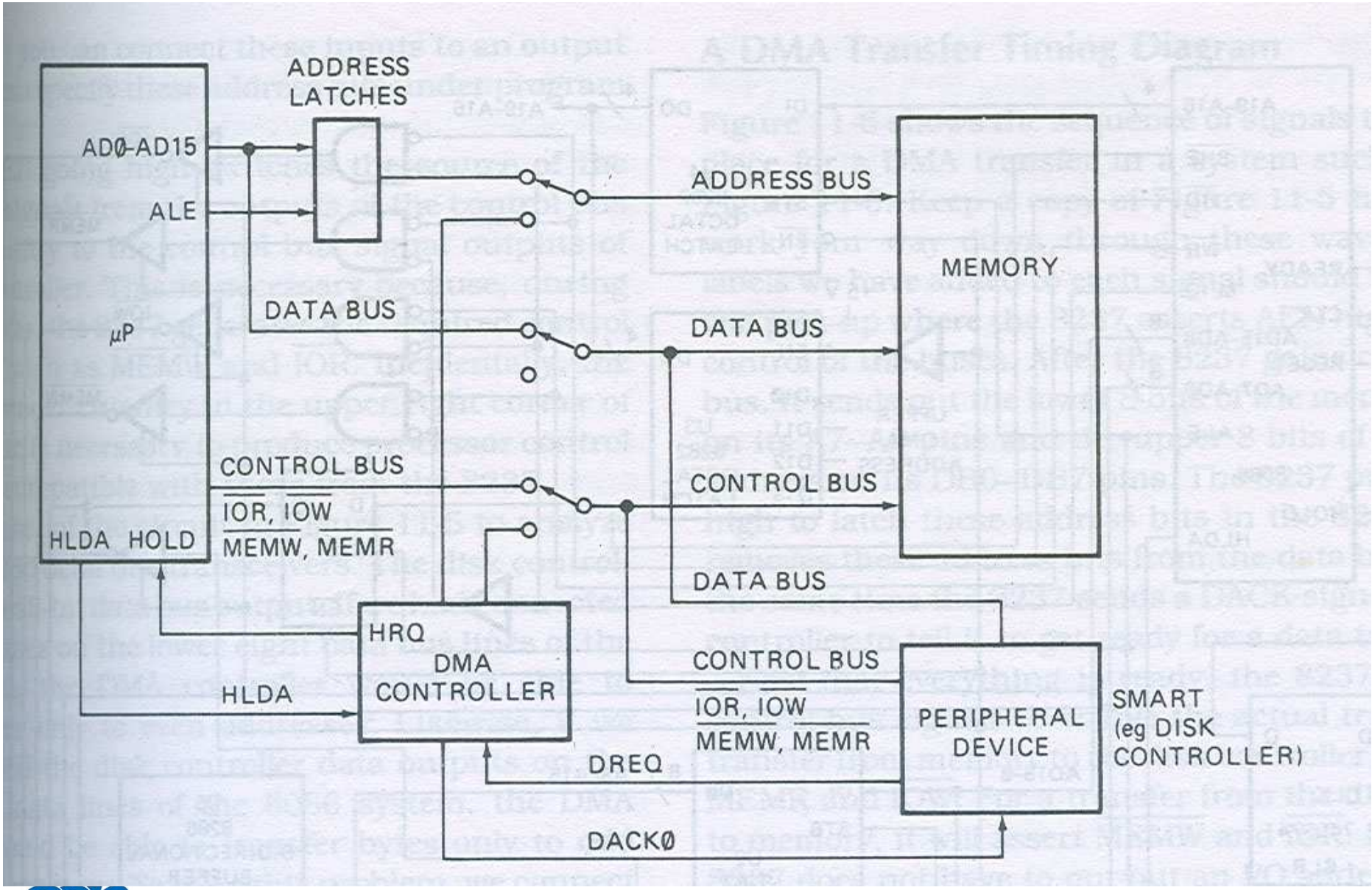


8237 – Programmable DMA Controller

8237 – Programmable DMA Controller- General DMA Structure



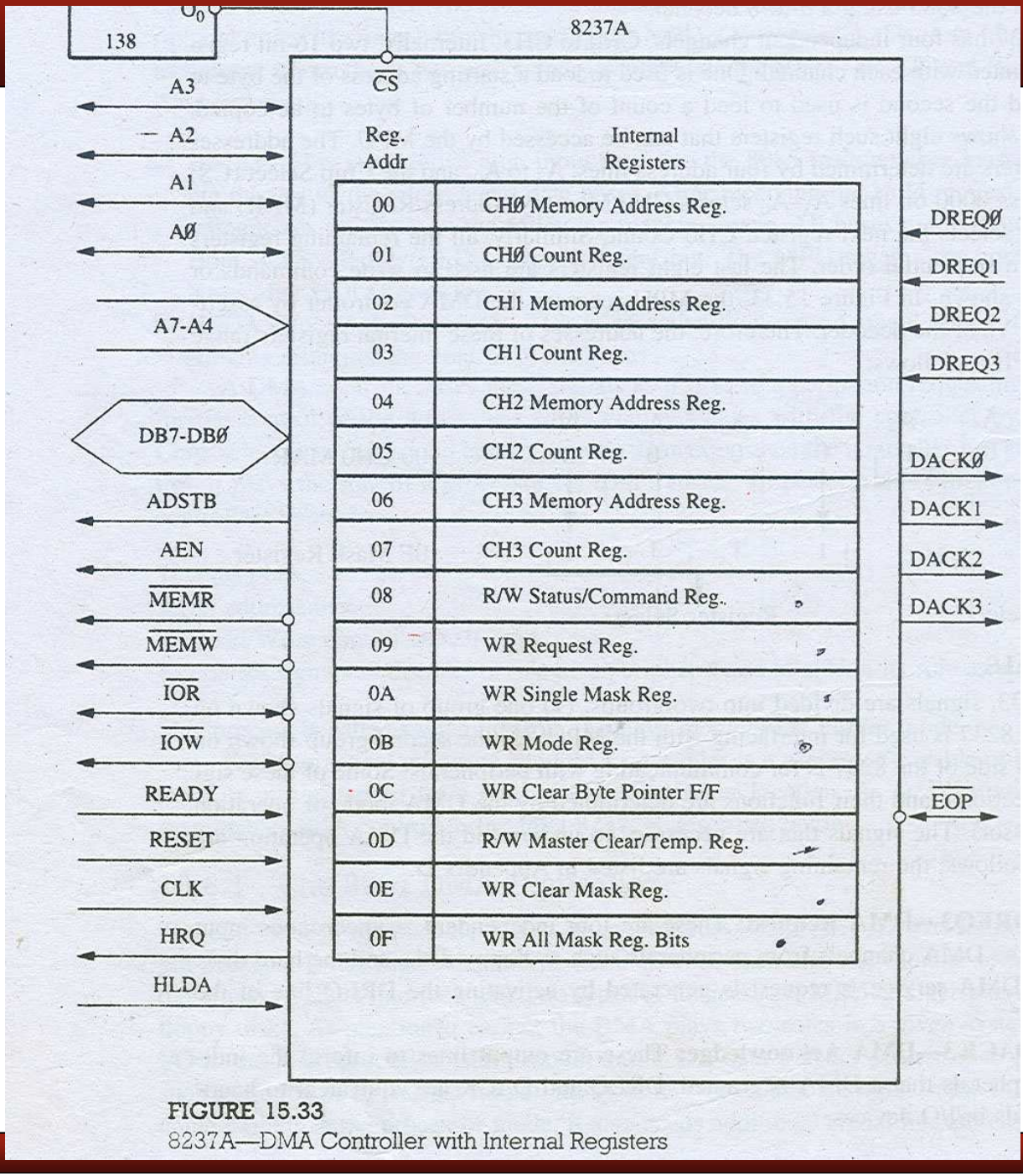
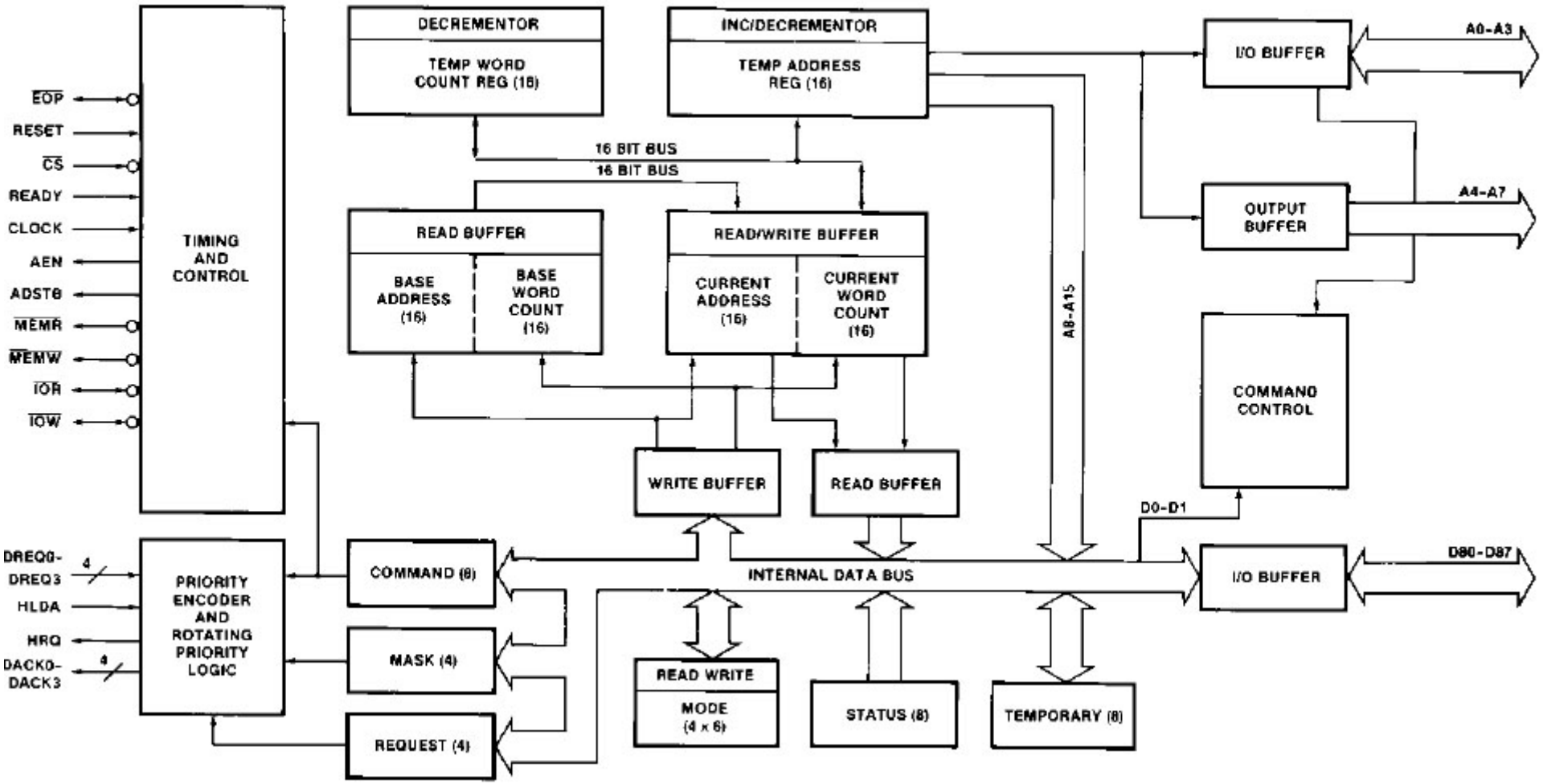
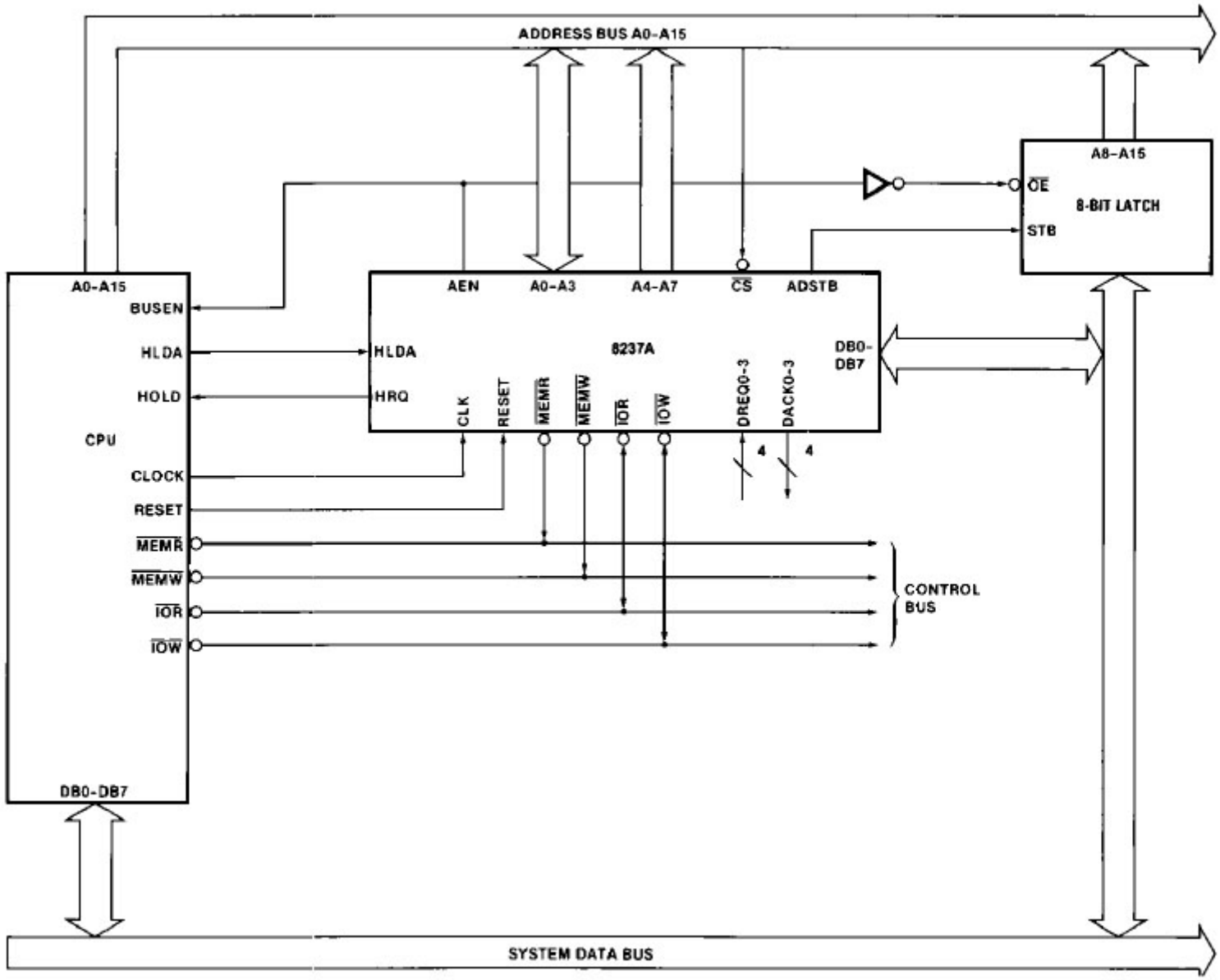


FIGURE 15.33
8237A—DMA Controller with Internal Registers

8237 – Programmable DMA Controller



8237 – Programmable DMA Controller – 16 bit address generation



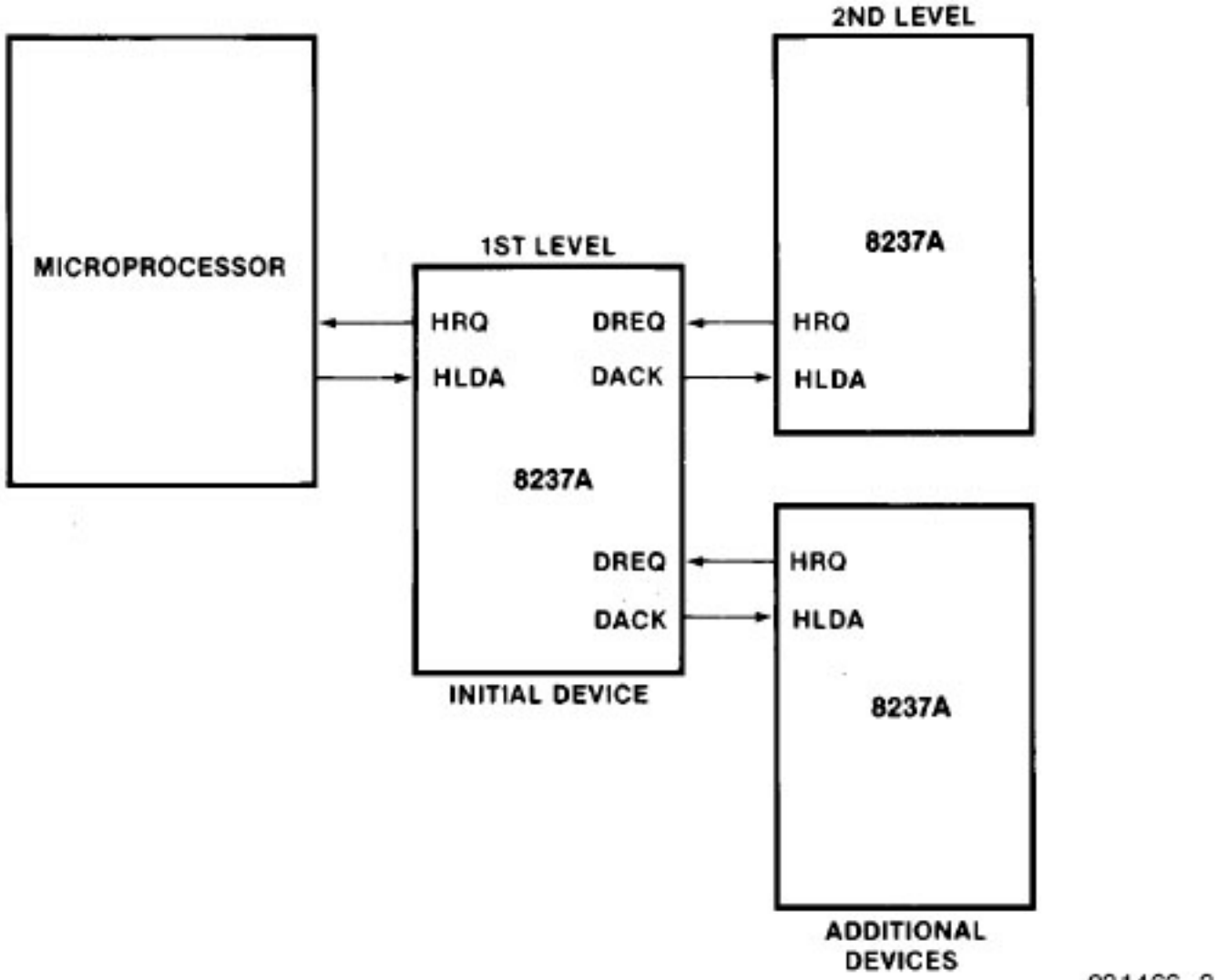
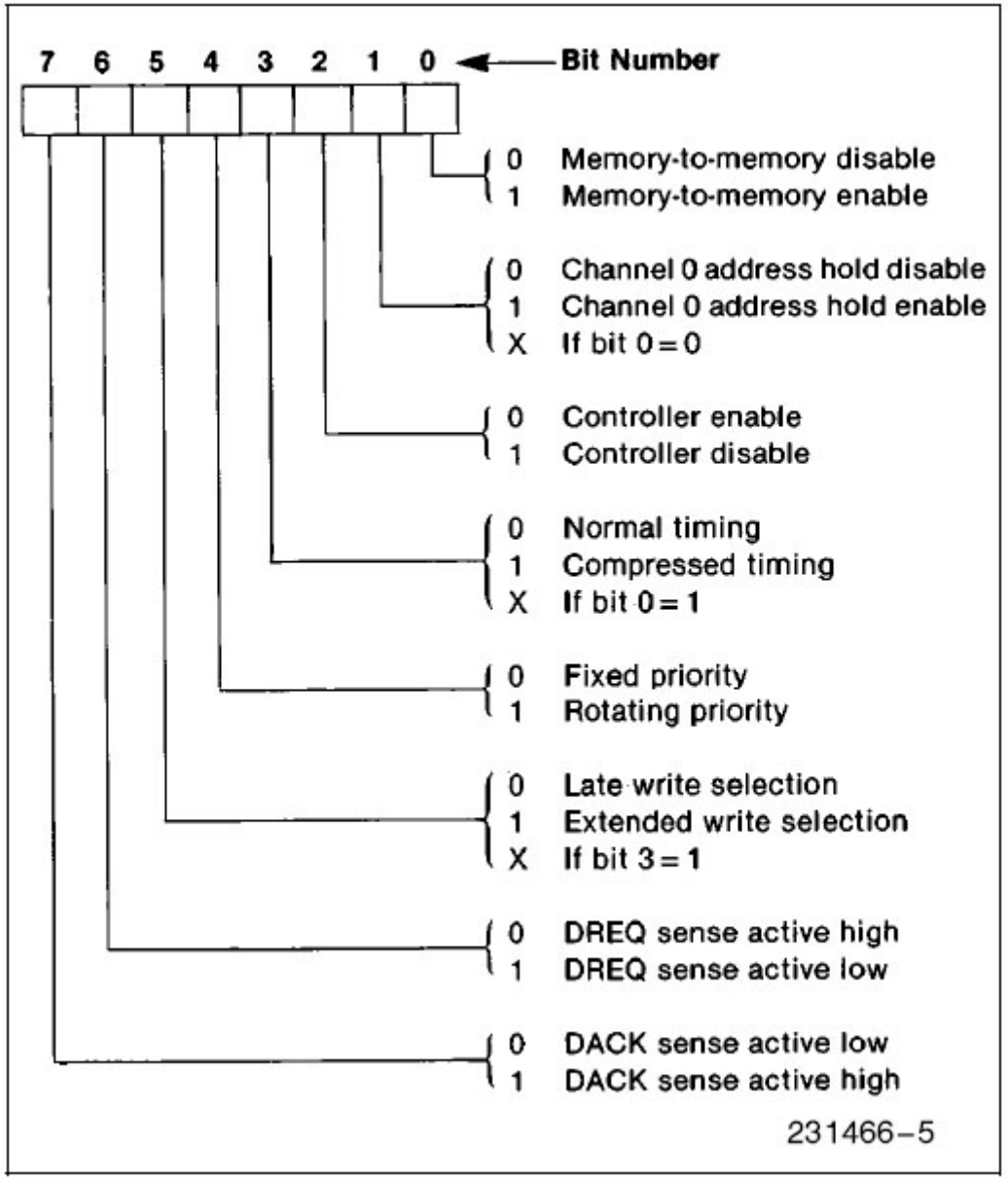
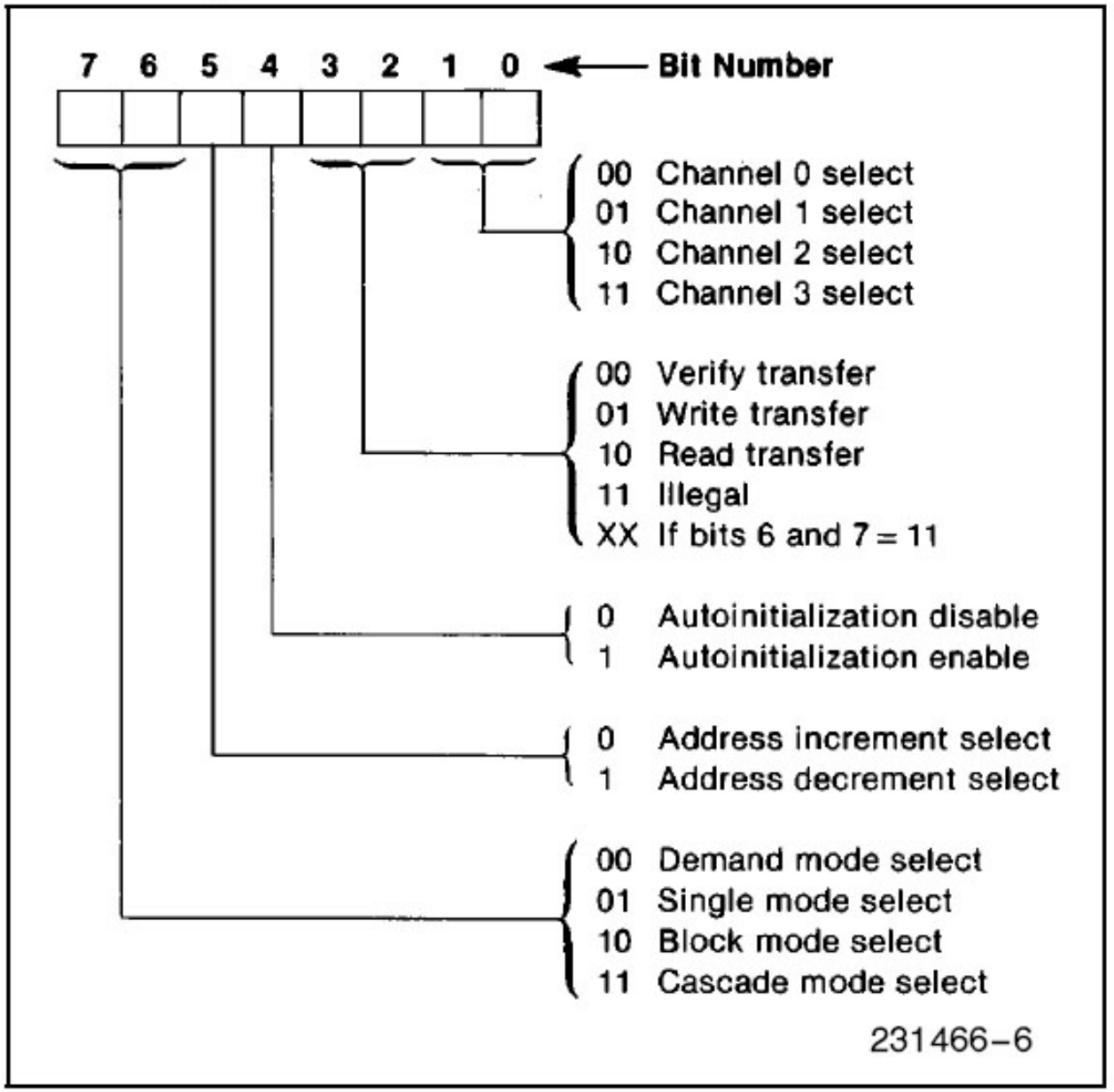


Figure 4. Cascaded 8237As

Command Register

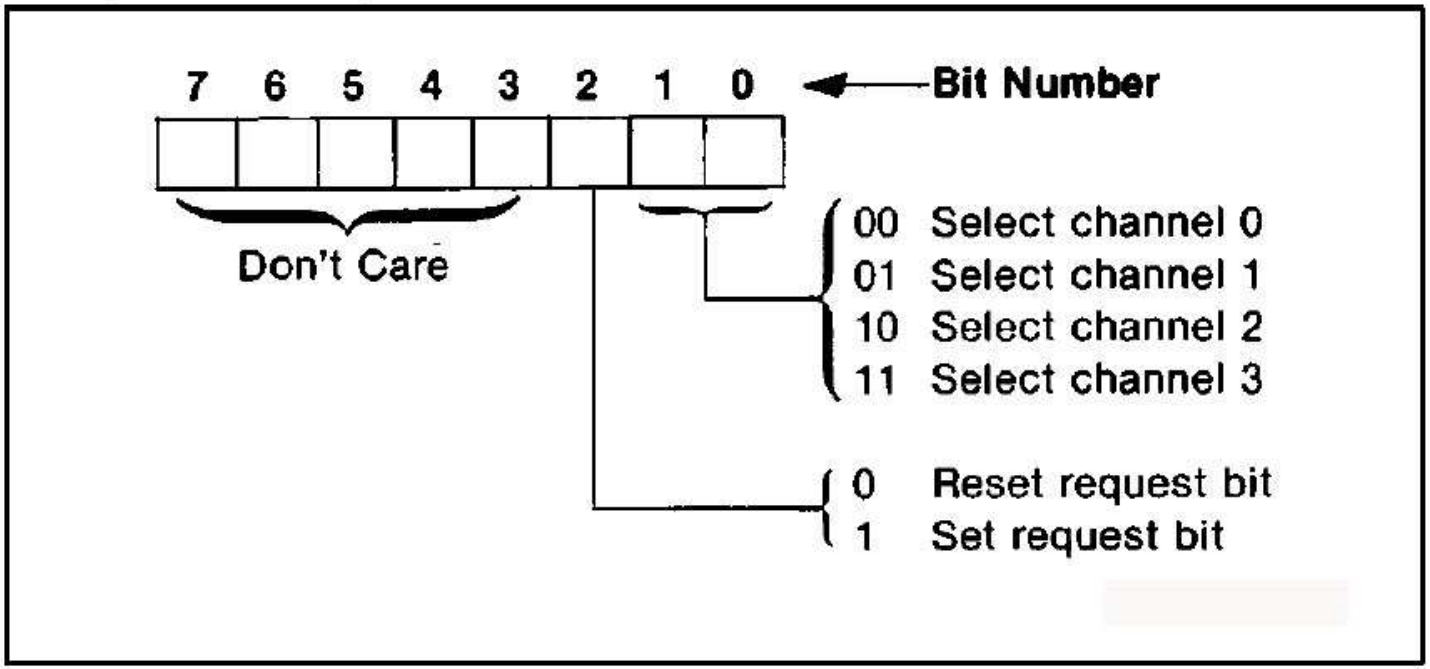


Mode Register

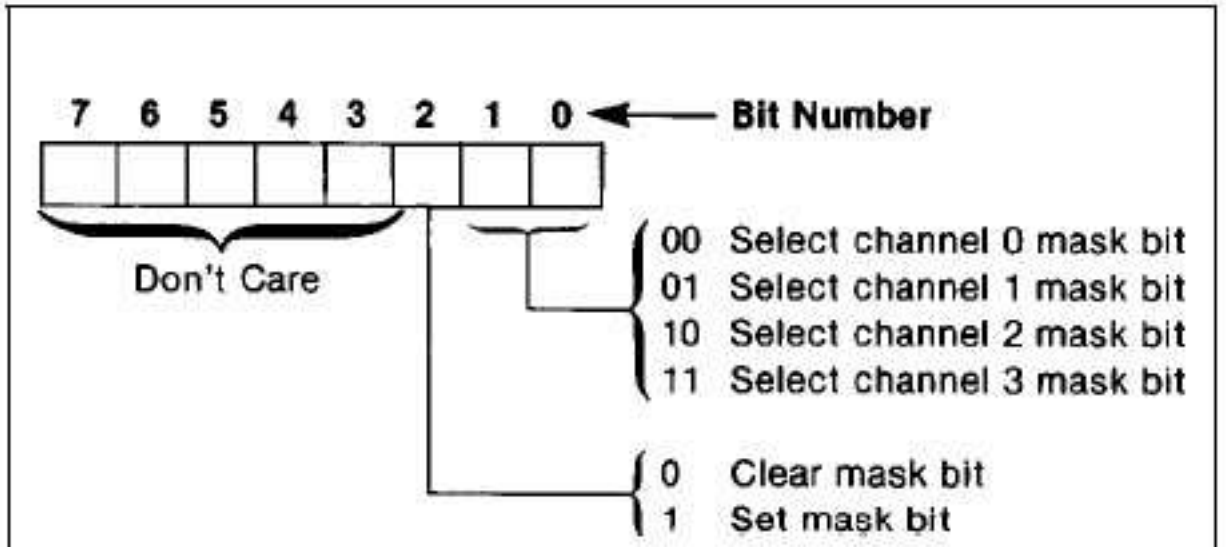


Request register It is used to request DMA data transfer which is initiated by software. It is very useful in memory to memory DMA data transfer where an external signal is not available to begin DMA data transfer.

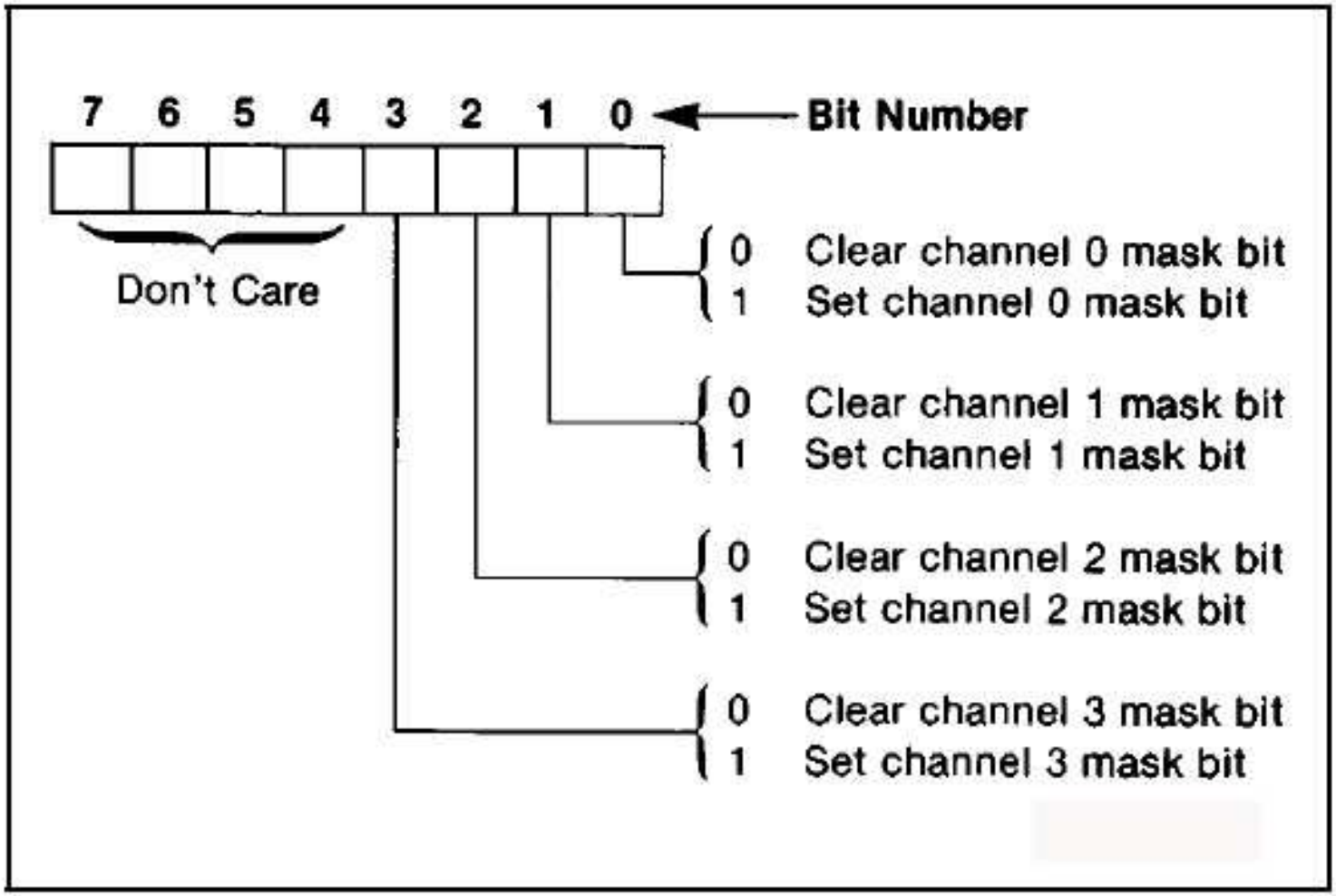
Request Register

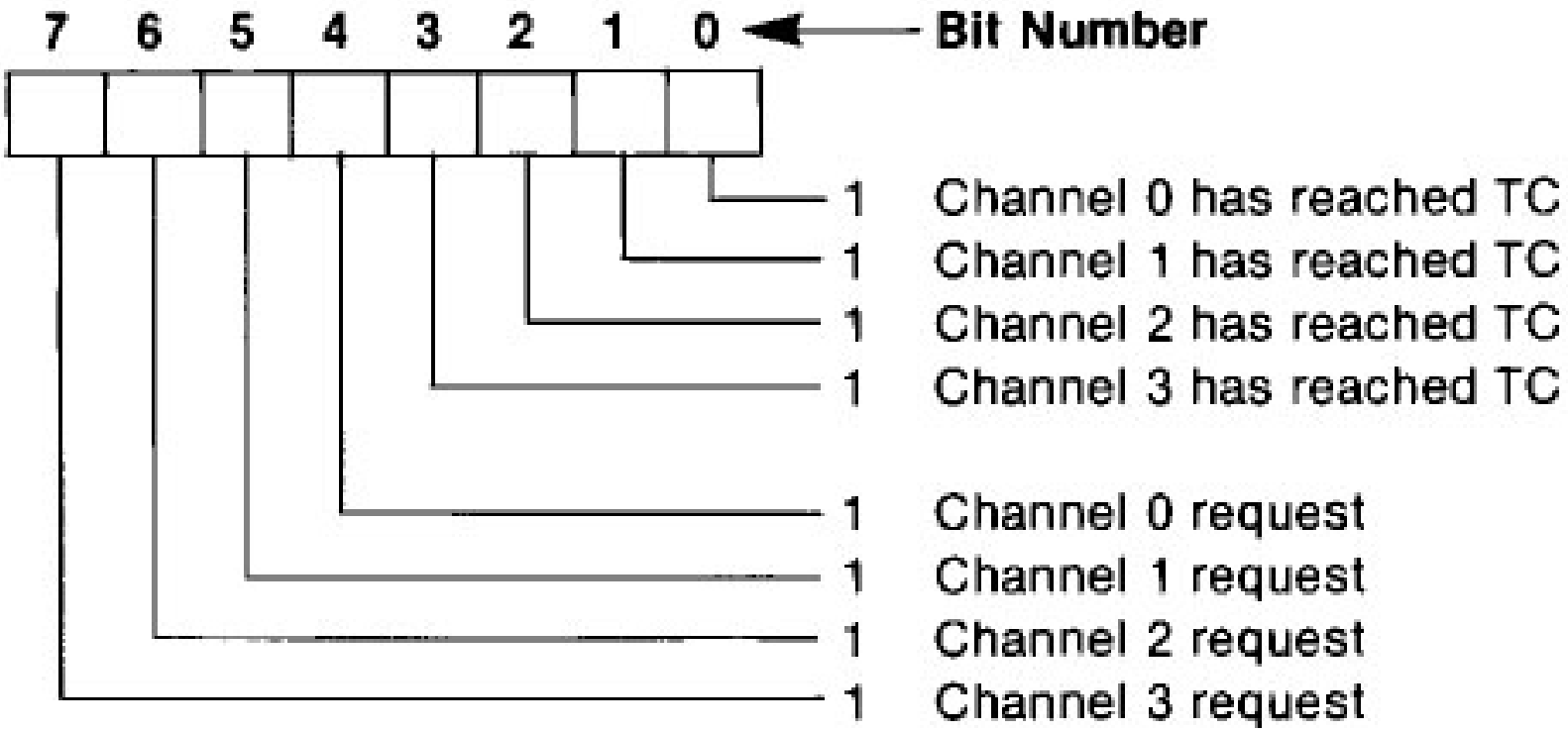


Mask Register—Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed for Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset. This disables all DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register.



All four bits of the Mask register may also be written with a single command.




7 6 5 4 3 2 1 0
Bit Number
1 Channel 0 has reached TC
1 Channel 1 has reached TC
1 Channel 2 has reached TC
1 Channel 3 has reached TC
1 Channel 0 request
1 Channel 1 request
1 Channel 2 request
1 Channel 3 request