8251 – Programmable Communication Interface

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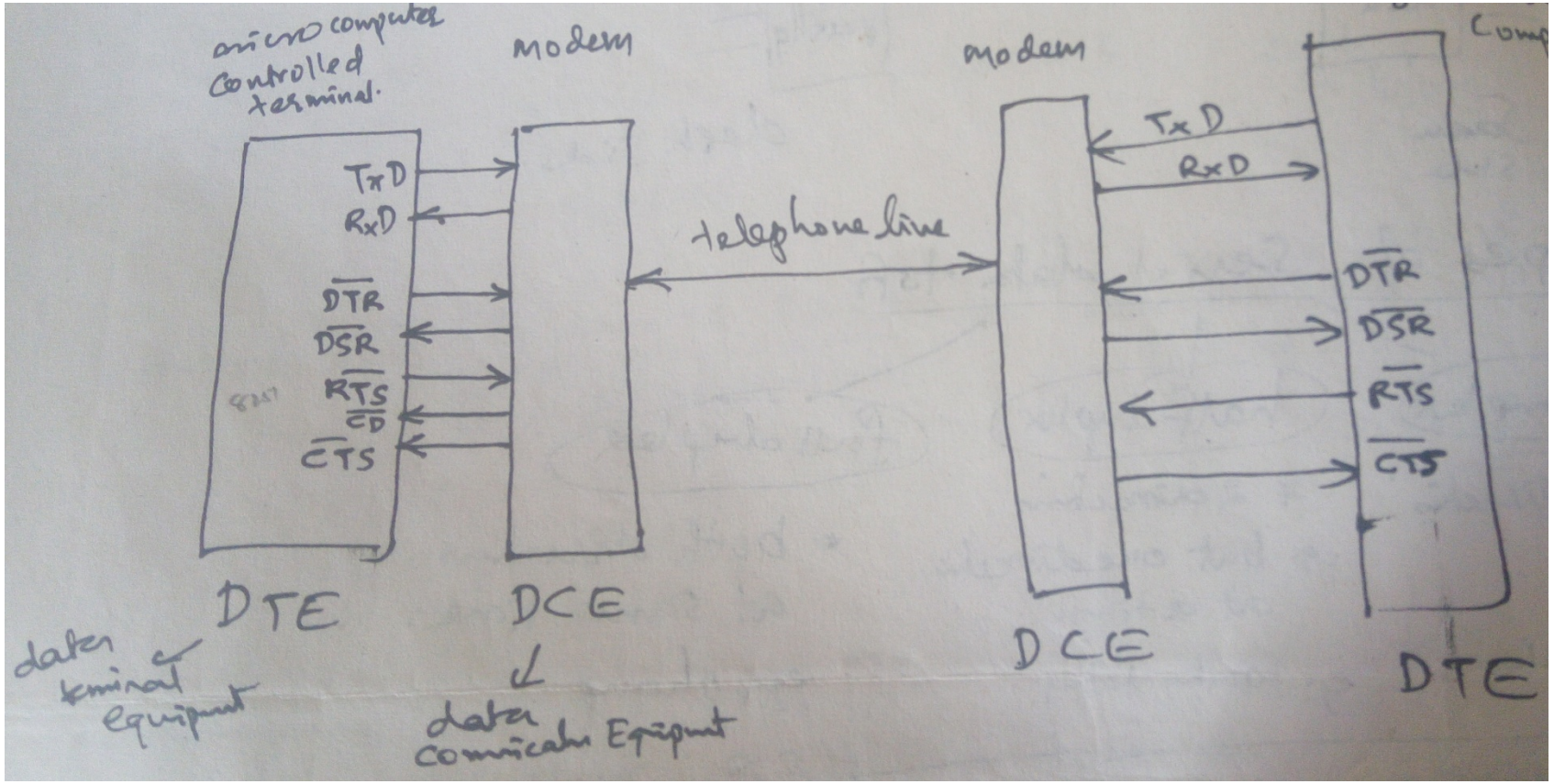
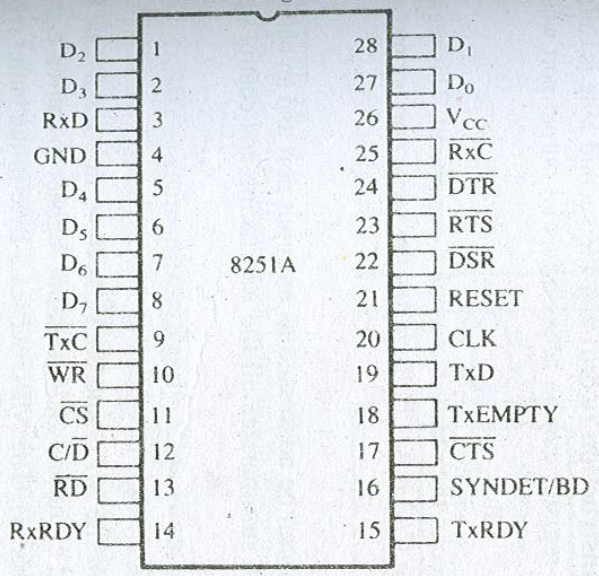
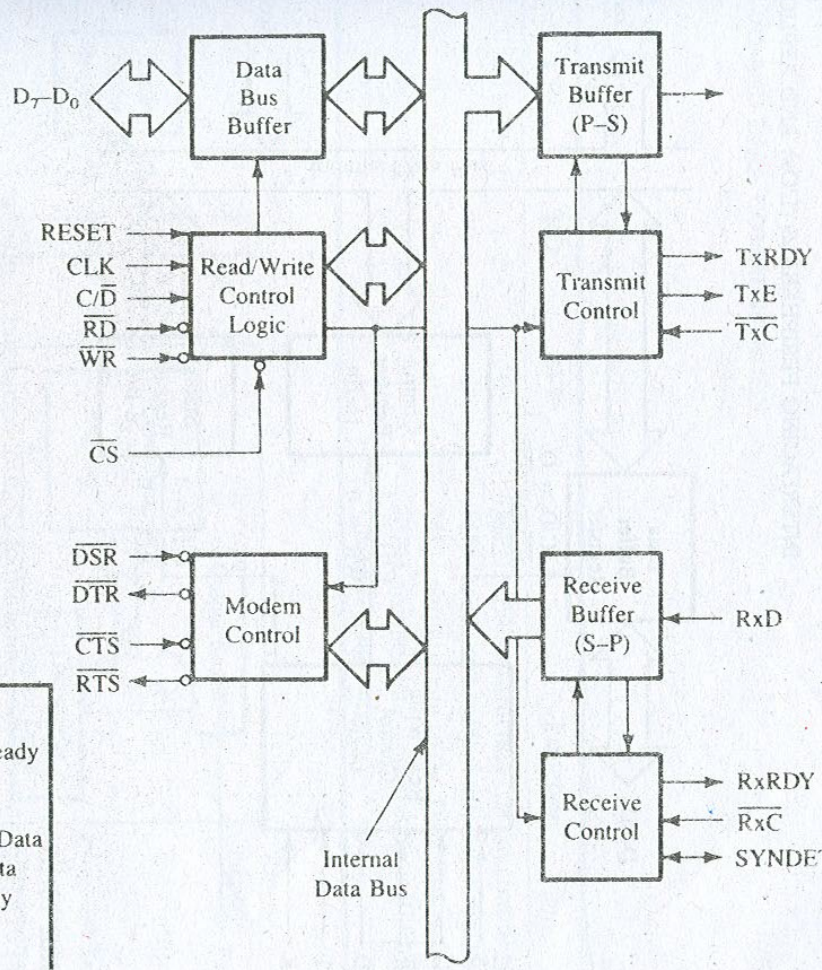


8251 – Programmable Communication Interface

Pin Configuration



Block Diagram



Pin Names

D_7–D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready
TxRDY	Transmitter Ready

DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET/BD	Sync Detect/ Break Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

8251 – Programmable Communication Interface

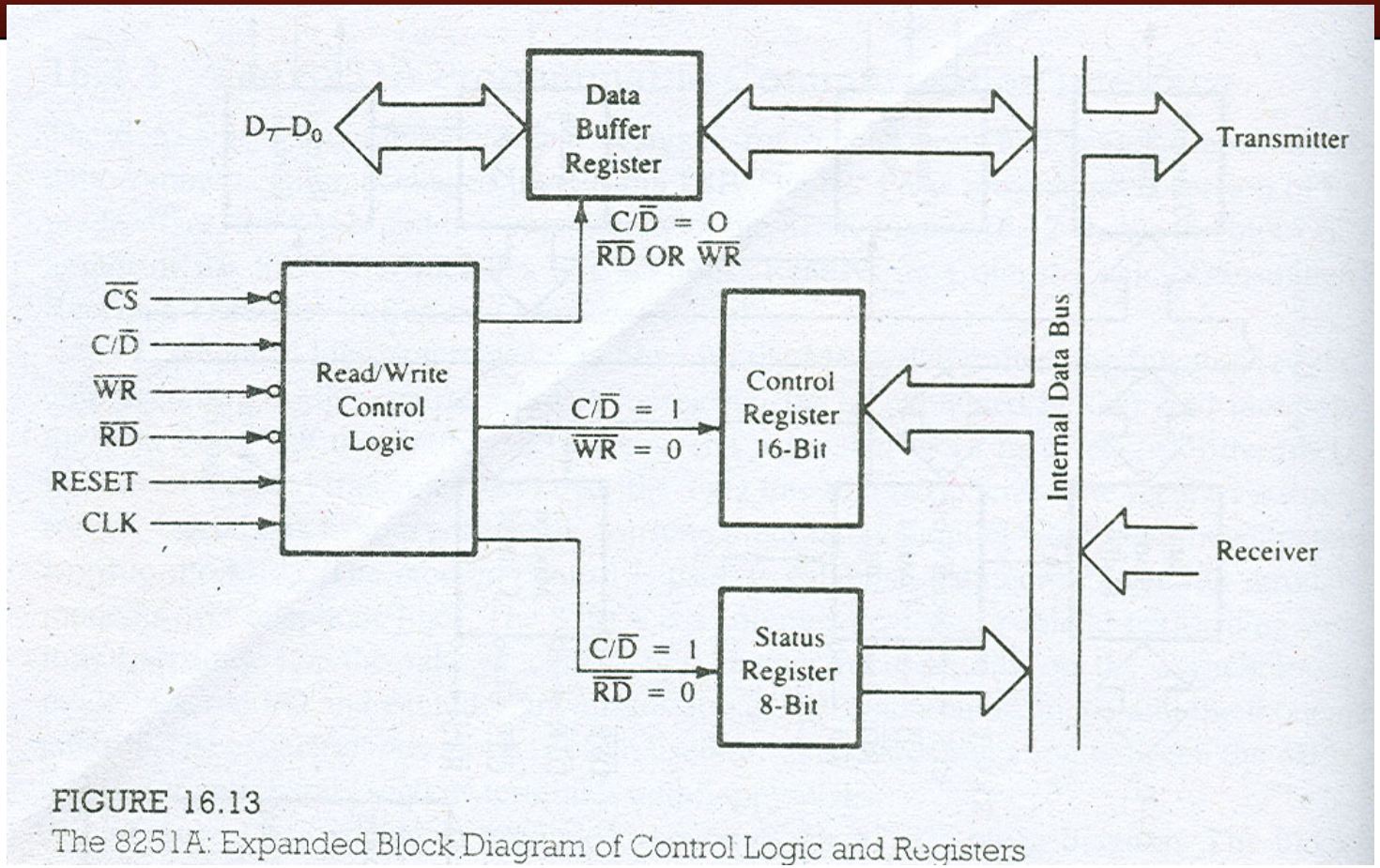


FIGURE 16.13
The 8251A: Expanded Block Diagram of Control Logic and Registers

TABLE 16.4
Summary of Control Signals for the 8251A

$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	Function
0	1	1	0	MPU writes instructions in the control register
0	1	0	1	MPU reads status from the status register
0	0	1	0	MPU outputs data to the Data Buffer
0	0	0	1	MPU accepts data from the Data Buffer
1	X	X	X	USART is not selected

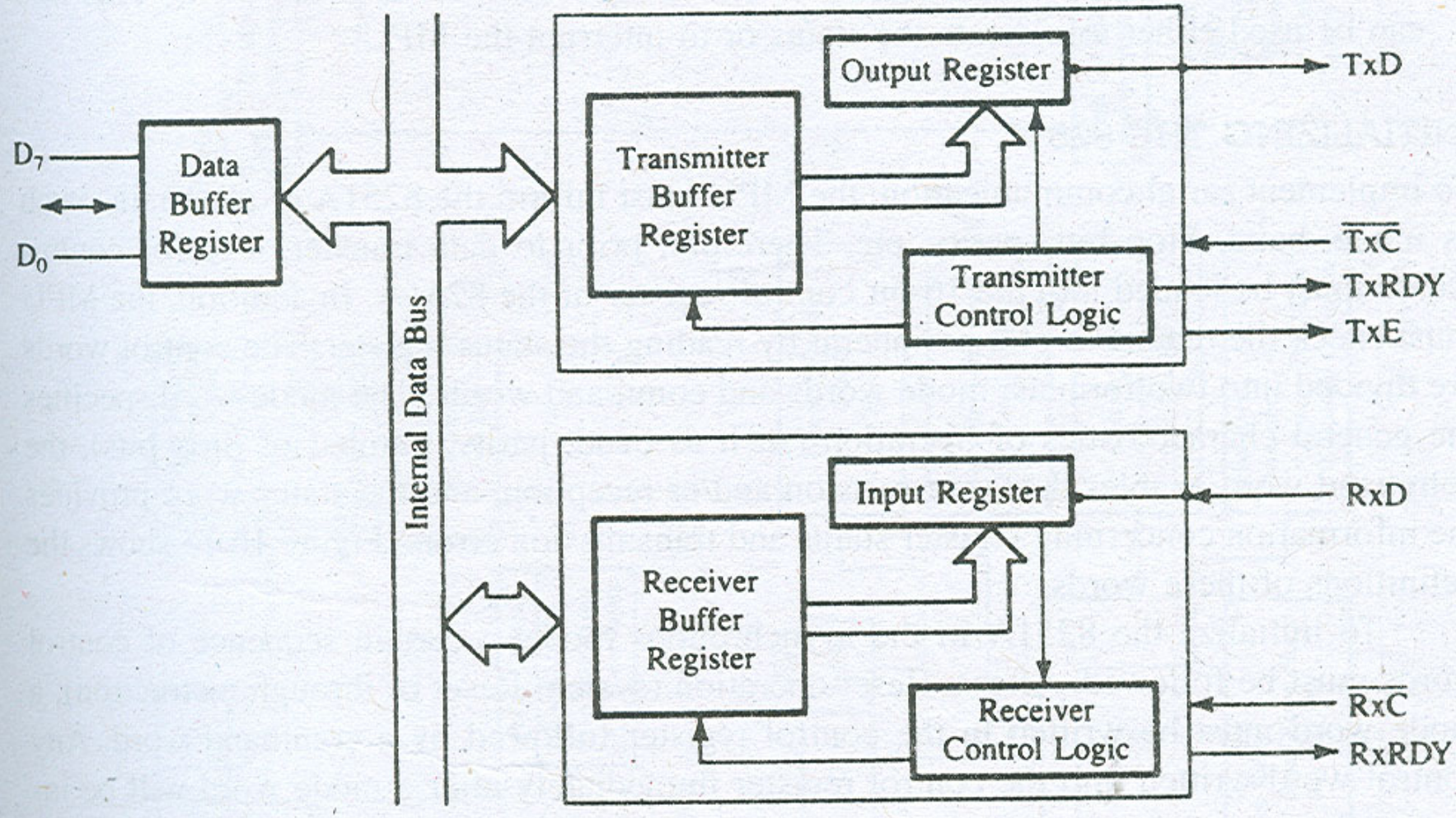
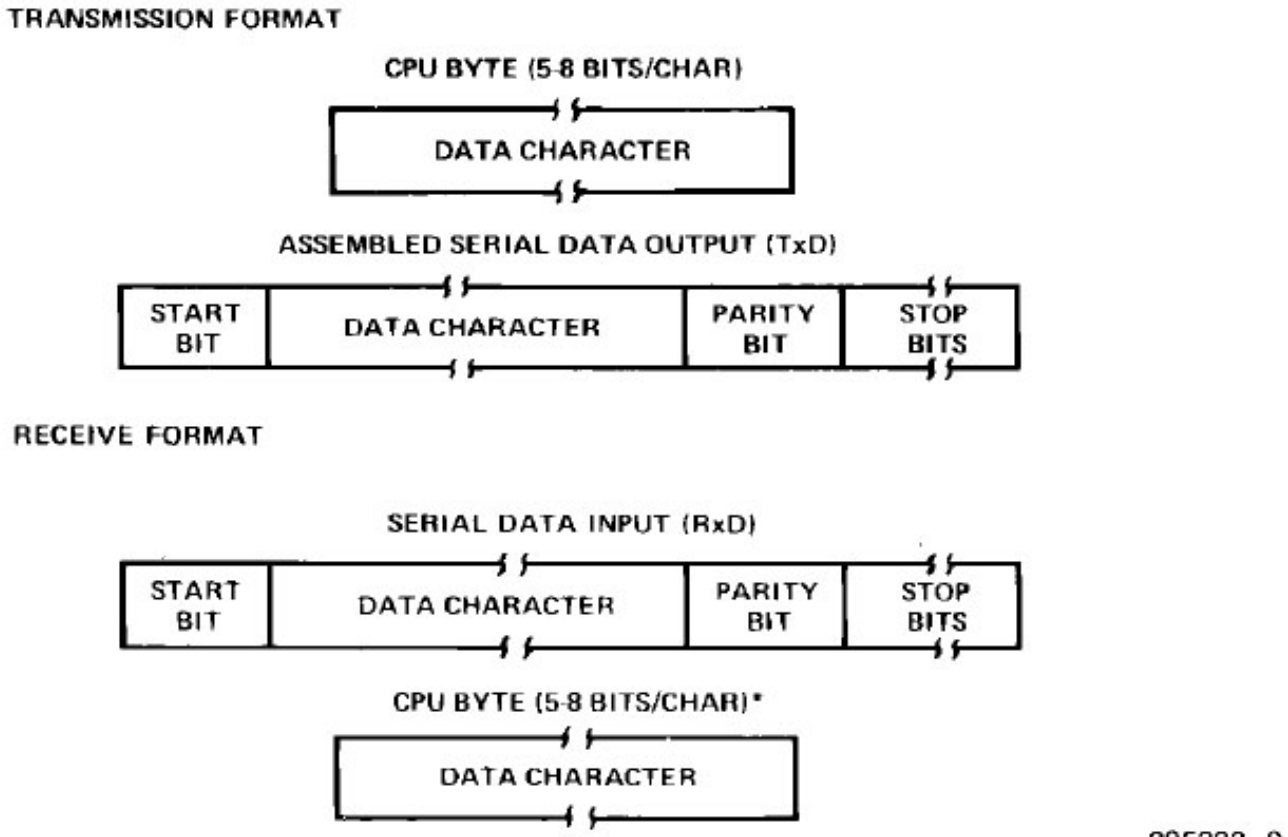


FIGURE 16.14
The 8251A: Expanded Block Diagram of Transmitter and Receiver Sections



*NOTE:
If character length is defined as 5, 6, or 7 bits the unused bits are set to "zero".

Figure 9. Asynchronous Mode

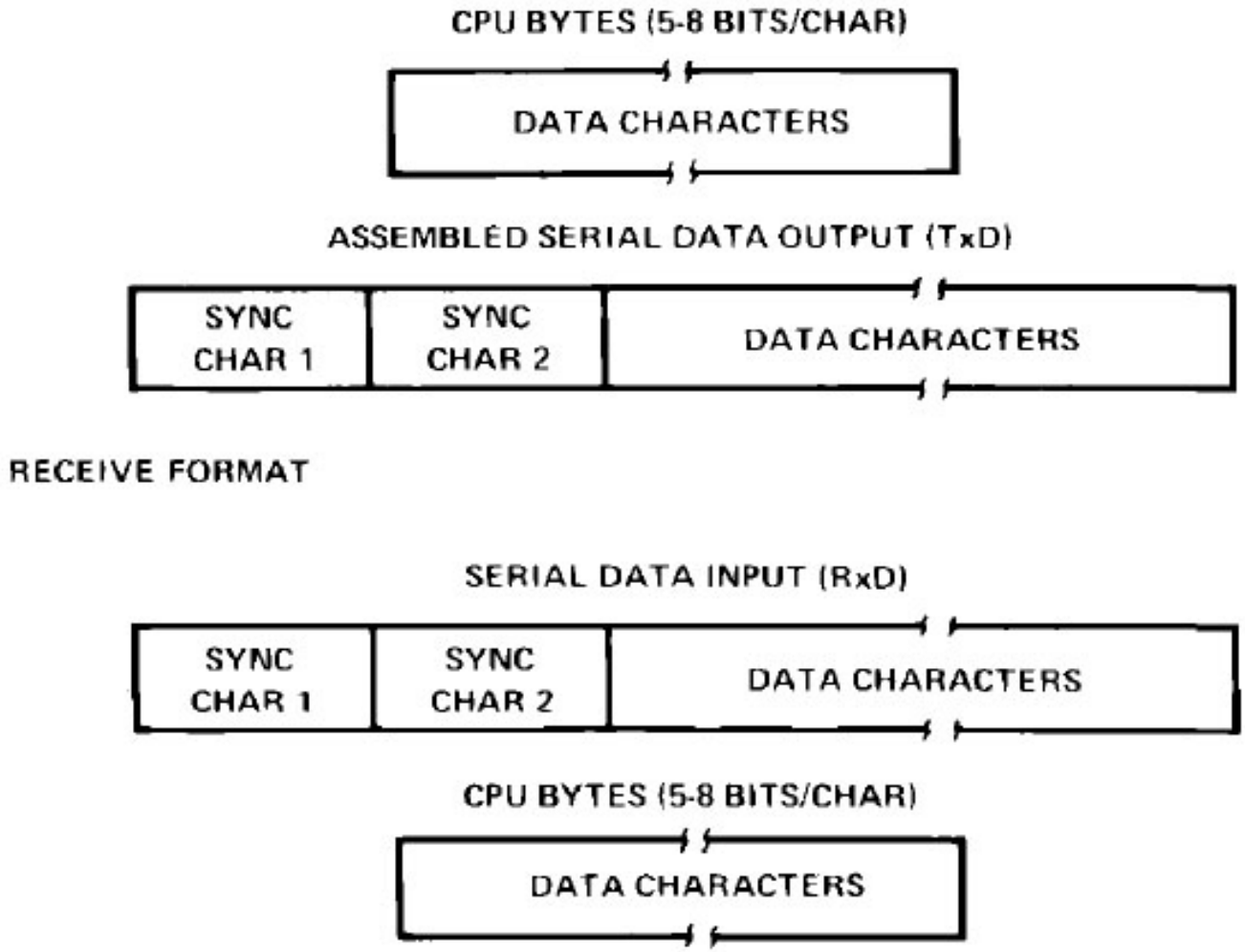


Figure 11. Data Format, Synchronous Mode

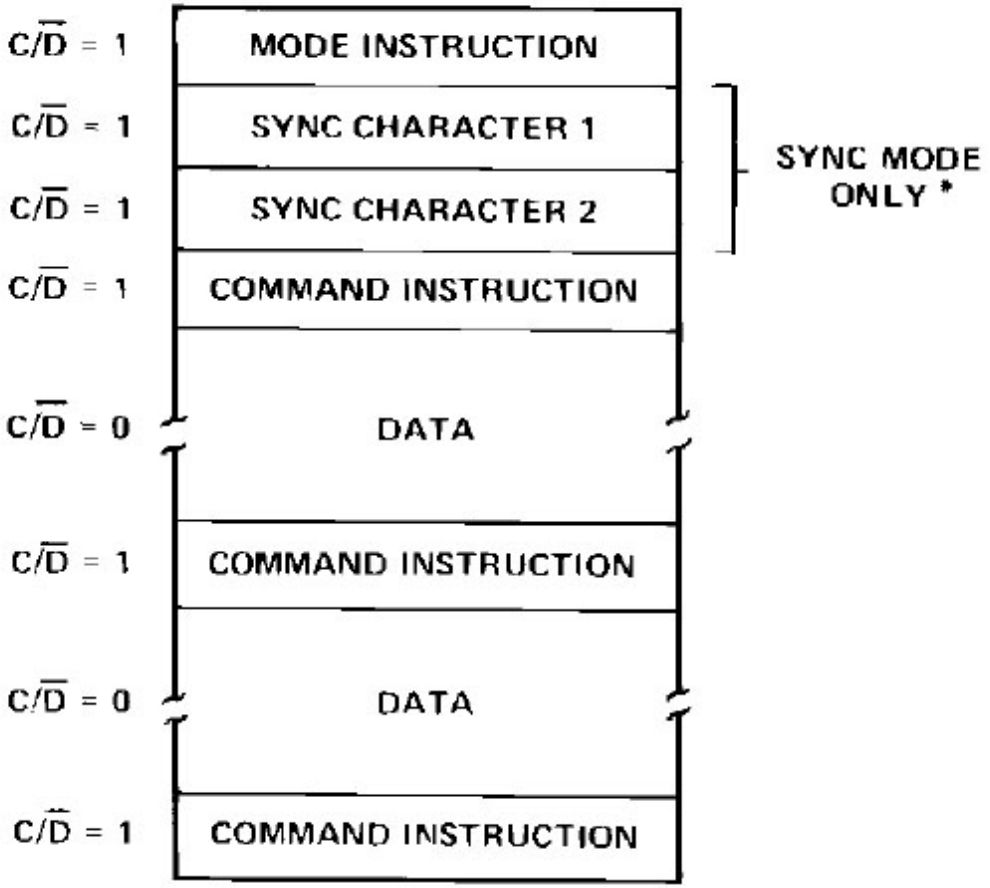
Programming the 8251A

Prior to starting data transmission or reception, the 8251A must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the 8251A and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:

1. Mode Instruction
2. Command Instruction

8251 – Programmable Communication Interface



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*The second sync character is skipped if mode instruction has programmed the 8251A to single character sync mode. Both sync characters are skipped if mode instruction has programmed the 8251A to async mode.

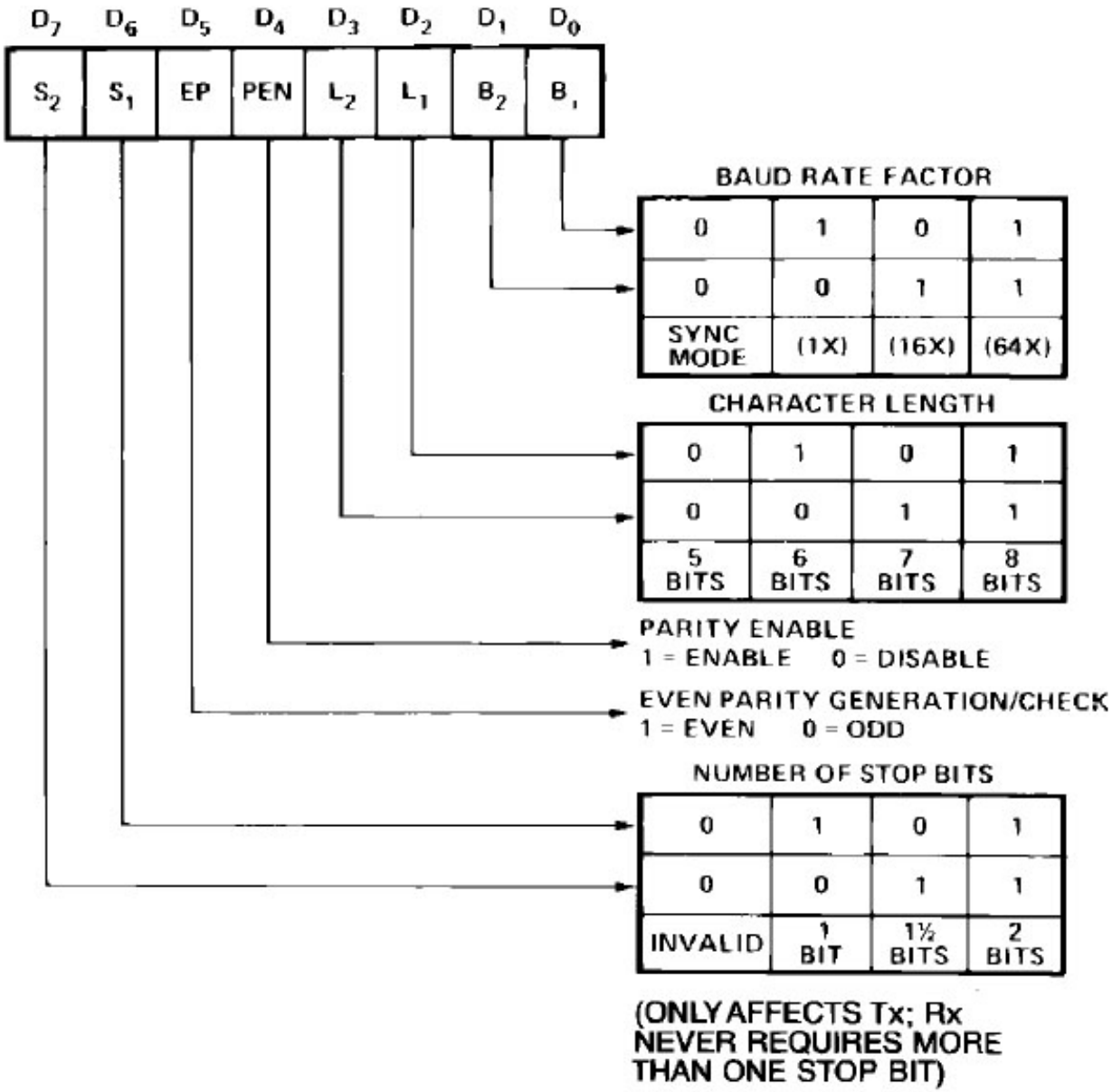


Figure 8. Mode Instruction Format, Asynchronous Mode

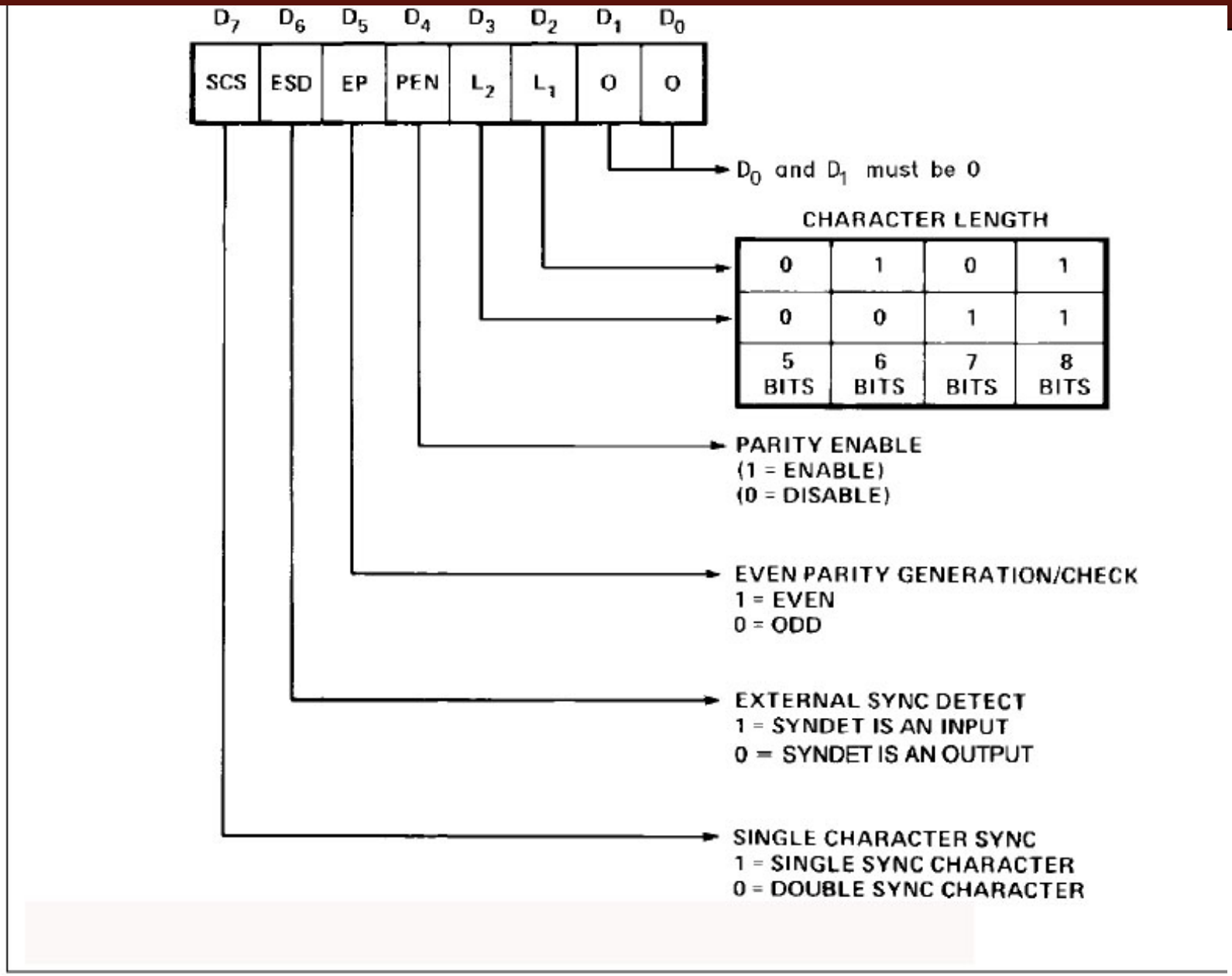
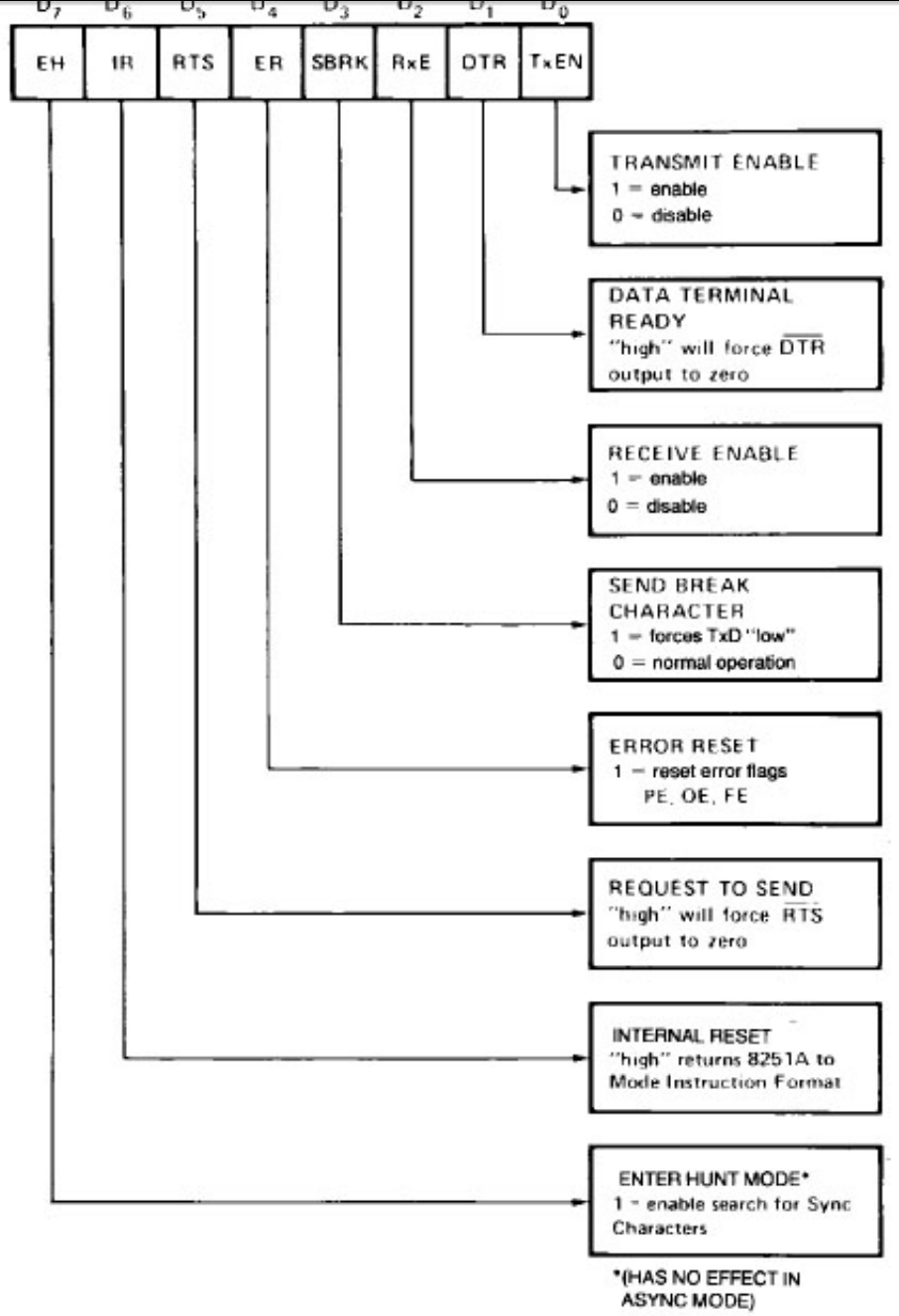
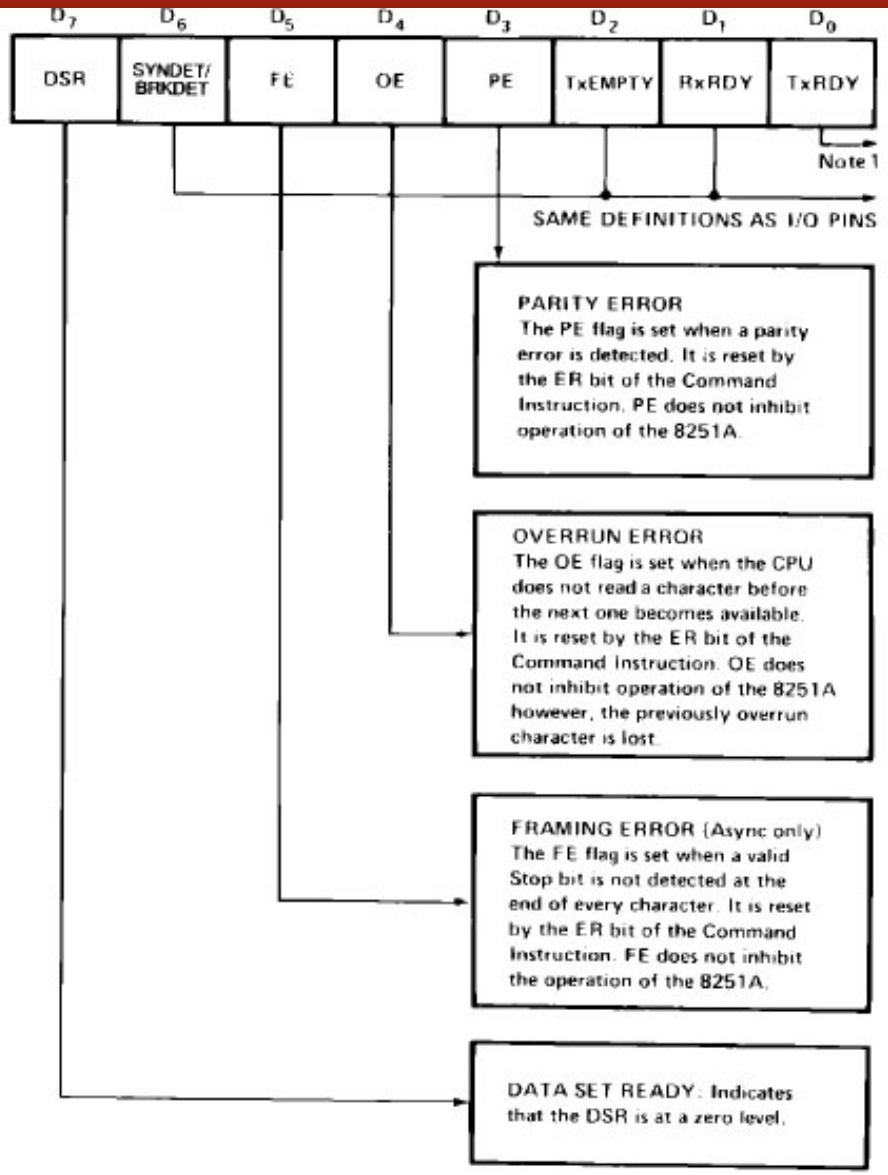


Figure 10. Mode Instruction Format, Synchronous Mode



NOTE:
Error Reset must be performed whenever RxEnable and Enter Hunt are programmed.

Figure 12. Command Instruction Format



NOTE:
1. TxRDY status bit has different meanings from the TxRDY output pin. The former is not conditioned by CTS and TxEN; the latter is conditioned by both CTS and TxEN.
i.e. TxRDY status bit = DB Buffer Empty
TxRDY pin out = DB Buffer Empty • (CTS = 0) • (TxEN = 1)

Figure 13. Status Read Format