I am deeply intrigued by the prevalence and impact that integrated circuits have on technology's evolution and unhesitatingly chose my major, microelectronics, where I have located my great passion. The enriching academic experiences in algorithm optimization and computer-aided design have instilled my keen interest to further my research in **CAD** to build reliable and efficient EDA tools and flows. To integrate high-level ideas, I, therefore, seek to pursue a Ph.D. to explore frontiers and contribute to promoting hardware systems from a broad view.

I have never restricted myself by our course syllabus; instead, my intellectual curiosity has facilitated a robust foundation in not only hardware but also software as well as the 1st rank in my department in both the sophomore and junior years.

I have never rested in my laurels but keep a keen eye out for research chances to explore and consolidate my knowledge. Noticing that limiting computing and energy resources available in real applications always stand at odds with the promised power of the given algorithm, it would be wise to design specific algorithms to satisfy metrics beyond original performance such as low power and latency. Motivated by this, I initiated research on efficient detection algorithm optimization in the massive MIMO system at the cost of low computational complexity. Indeed, after carefully delving the message passing detection (MPD) algorithm, I found that it suffers from high complexity caused by internal complex computations during iterative updating with the increasing number of antennas. Instead, I used a simplified probability updating scheme to calculate each symbol's variance/mean and update needed messages by sorting and using the maximum element in each symbol's LLR vector and corresponding constellation point. In doing so, we could omit divisions and largely reduce the number of multiplications and additions, which wouldn't add much computational burden due to extra comparison operations. My modification was verified as efficient and reliable by introducing much lower complexity with a slight degradation in the bit error rate performance, making it very suitable for efficient hardware and software implementation, i.e., "hardware-friendly". This experience strengthened my math and algorithm ability, which also propelled my further understanding of the aid and effeteness of algorithm-level optimization to meet a high computing efficiency.

The first time that I was marveled at the charm of electronic design automation was in the project to develop an HSPICE-like circuit simulator written in Python and based on the modified nodal analysis method in eight weeks. By a general stamp method, I established different device models for both linear and nonlinear circuits to support DC/AC/TRAN analysis. I introduced the Newton-Rapson method to address the nonlinearity and took some tricks to solve the divergence problem in circuit simulation like adding a small resistance between the source and the drain of the MOSFET. To further increase the accuracy of simulation, I added dynamic time step control in my simulator. The simulation results verified the correctness and practicability of the simulator. Following the effort I had invested, I am able to hone my math and coding skills, which largely ignites my passion for electronic design automation.

Next, with such a desire for design automation flow, my experiences using EDA tools inspired me to ponder a question: how to embed an abstract circuit description into silicon, creating a detailed geometric layout on a die? I seized an internship opportunity to join the UTDA lab at the UT-Austin to work with Prof. David. Z. Pan, focused on two projects. In my independent project, I addressed the graph partition problem with a heuristic partitioning solver, which was motivated by recognizing the improving space of partitioning quality in the widely-used tool, Metis. The difficulty here was when

adopting a K-means-like method to partition vertexes in the graph, we had to pre-define “distance” and “centroid”. After studying related literature, I introduced a modified load-balancing mechanism into the graph to obtain hill-like load distribution results as the evaluation of the “distance” between vertexes. Thus, I designed the whole framework to alternate between choosing centroids and determining a partitioning based on the clustering mechanism. In practice, I faced the issue that the bad initialization by randomly selecting centroids could interfere with results. I refined the initialization scheme to choose initial centroids more dispersedly by considering graph structure, which largely boosted the partitioning quality. Later, I worked on transforming the whole program to run in parallel as well as a CUDA version to boost the speed at scale. Finally, partitioning results on tested graphs had a ~5% improvement over Metis on edge-cut with an acceptable run-time. **Meanwhile**, to strengthen my skills, I joined another project to adapt optical neural networks (ONNs) to low-precision controls and non-ideal environments with phase shifter noises. I actively discussed the proposed method and implemented the baseline by iterative quantization. Our method can effectively tackle the non-ideal issues and hold better accuracy under various control precisions and device noises. In the end, I am beyond excited that this collaborative work was accepted by the Design, Automation and Test in Europe Conference (DATE) 2020. I am grateful for this opportunity this summer to reveal the fascination and powerfulness of computer-aided design to me, which further cultivates my independent problem-solving abilities by integrating multi-layer knowledge and ignites my great academic ambition.

Triggered by my previous experiences and interests, I currently start to work on the HLS-level quality estimation for a specific domain, FPGA-based electromagnetic transient emulation system, to provide a fast and accurate prediction with the aid of machine learning. We aim to provide aid for early-stage design optimization and extend to further work on design space exploration. I firmly believe that I could further strengthen my abilities and be better prepared for my graduate study through this chance.

During the past three years of attaining ample satisfaction from research experiences and building a solid knowledge in both VLSI and EDA, I am confident in my ultimate motivation to contribute my skills and knowledge to build smart and reliable EDA tools and flows with the aid of the Ph.D. program at **UC San Diego**, where owns excellent research groups in VLSI/CAD area. After carefully delving into exciting research projects conducted by your exceptional scholars, I strongly desire to research under their supervision to be a top researcher in the future. I want to use my background knowledge to further my research in IC physical design flow with Prof. **Andrew B. Kahng**; Also, I want to work with Prof. **Chung-Kuan Cheng** in circuit simulation as well as VLSI physical layout in placement and routing. It would be a great honor and privilege if your program could allow me to further my study at UCSD, and I believe that my experiences, knowledge and skills can develop my fullest research potential, add new insights, and bring us a step closer to the next milestone of intelligence and technology.

Thank you for your consideration of my application.