Monolithic Digital FM/MW/SW Receiver Radio-on-a-Chip™

KT0937-D8

■ Features

Worldwide full band FM/MW/SW support
- FM: 32MHz-110MHz
- MW: 500KHz-1750KHz
- SW: 1.75MHz-32MHz

Fully integrated frequency synthesizer with no external components

Simple control interfaces
- Integrated channel control

Versatile tuning interfaces
- Key-press mode, variable resistor mode.

Support LCD display
- Output channel frequency through 2-wire interface

High Fidelity
- SNR (FM/AM): 60dB/55dB(without weighting filter)
- THD: 0.3%

Low Supply Current
- 29mA (operating)
- <45uA (standby)

Advanced features
- Automatic antenna tuning
- Adjustable AM channel filters (1.2/2.4/3.6/4.8/6KHz)
- Enhanced FM Automatic Frequency Control (AFC) Capability (up to 200KHz)
- Flexible Automatic Gain Control (AGC)
- Integrated stereo headphone driver
- 2-wire control interface for MCU
- Advanced Softmute
- Flexible stereo Blend

Low supply voltage
- 2.1V to 3.6V, can be supplied by 2 AAA batteries

Integrated low power crystal oscillator
- Support both 32.768KHz and 38KHz crystal

True Continuous Reference Clock supported
- From 30KHz to 40MHz with 3V voltage tolerance

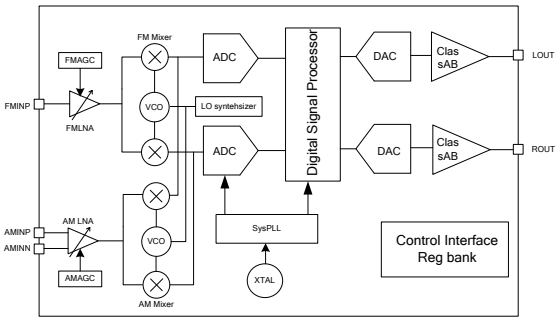
Compatible with EN55020

Small form factor SSOP16L package

RoHS Compliant

■ Applications

Desktop and portable radio, Boombox, Micro systems, Clock radio, Campus radio system.



KT0937-D8 System Diagram

■ Description

The KT0937-D8 is KT Micro's 3rd generation of proprietary fully integrated FM/MW/SW receiver chip with patented technologies that delivers superior audio and RF performance, supports direct and simple interface for tuning wheel and push button, and supports LCD displays through 2-wire interface .The new features include improved flatness of sensitivity on the whole band, independent status indicator, improved EMI/EMC and higher FM stereo separation.

Thanks to the patented tuning technology, the receiver maintains good signal reception even with short antennas. The chip consumes merely 29mA current and can be powered by 2 AAA batteries.

KT0937-D8 supports a wide range of reference clocks from 30 KHz to 40 MHz, hence can share system clocks with a varieties of MCUs further reducing the system BOM cost. The KT0937-D8 provides direct and simple interface to support multiple tuning schemes.

With high audio performance, fully integrated features and low BOM cost, KT0937-D8 is ideal for portable radios that require LCD displays.

Rev. 2.1

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1. Electrical Specification

Table 1: Operation Condition

Parameter	Symbol	Operating Condition	Min	Typ	Max	Units
Analog Power Supply	AVDD	Relative to AVSS	2.1	3.3	3.6	V
Digital Power Supply	DVDD	Relative to DVSS	2.1	3.3	3.6	V
Ambient Temperature	Ta		-30	25	70	℃

Table 2: Absolute Maximum Ratings[1]

Parameter	Symbol	Value	Units
Analog Supply Voltage	AVDD	–0.5 to 3.9	V
Digital and I/O Supply Voltage	DVDD	–0.5 to 3.9	V
Input Current[2]	I_{IN}	10	mA
Input Voltage[2]	V_{IN}	–0.3 to (V_{IO} + 0.3)	V
RF Input Level		0.7	V_{PK}

Notes:
1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. For input pins SDA, SCL.

Table 3: DC Characteristics

(Unless otherwise noted Ta = -30~70℃, AVDD = DVDD = 2.1V to 3.6V)

Parameter		Symbol	Test/Operating Condition	Min	Typ	Max	Units
Current Consumption	FM Mode	I_{FM}		-	-	30	mA
	MW Mode	I_{MW}		-	-	29	mA
	SW Mode	Isw				29	mA
Standby Current		I_{APD}		-	-	45	μA
High Level Input Voltage[1]		V_{IH}		0.7 x DVDD		DVDD + 0.3	V
Low Level Input Voltage[1]		V_{IL}		-0.3		0.3 x DVDD	V
High Level Input Current[1]		I_{IH}	VIN = AVDD = DVDD = 3.6V	-10		10	uA
Low Level Input Current[1]		I_{IL}	VIN = 0V, AVDD = DVDD = 3.6V	-10		10	uA
High Level Output Voltage[2]		V_{OH}	IOUT = 500uA	0.8 x DVDD			V
Low Level Output Voltage[2]		V_{OL}	IOUT = -500uA			0.2 x DVDD	V
ST pin Output Impedance		R_{OST}	VDD=3.6V			200	ohm
			VDD=3V			230	ohm
			VDD=2.1V			300	ohm

Notes:
1. For input pins SCL, SDA.
2. For output pins SDA.

Table 4: FM Receiver Characteristics

(Unless otherwise noted Ta = -30~70℃, AVDD = DVDD = 2.1V to 3.6V)

Parameter	Symbol	Test/Operating Condition	Min	Typ	Max	Units
FM Frequency Range	F_{RX}		32		110	MHz
Sensitivity[1,2,3,7,9,10]	Sen	(S+N)/N=26dB		1.6	2	uVEMF
Input referred 3rd Order Intermodulation Point[4,5]	IIP3			100		dBuVEMF
Adjacent Channel Selectivity		±200KHz	40		51	dB
Alternate Channel Selectivity		±400KHz	50		70	dB
Image Rejection Radio				43		dB
AM suppression				50		dB
RCLK frequency Range			30	32.768	40,000	KHz
RCLK frequency tolerance[8]			-100		100	ppm
Audio Output Voltage[1,2,4,7,10,11]		FM_GAIN=4 △F=75KHz	-	345	-	mV_{RMS}
Audio Band Limits[1,2,4,9,10]		±3dB	30		15k	Hz
Audio Stereo Separation[1,4,6,9,10]			40			dB
Audio Mono S/N[1,2,3,4,9,10]			55	58		dB
Audio Stereo S/N[1,4,6,7,9,10]		DBLEND=1		64		dB
Audio THD[1,2,4,6,7,8,9,10,11]				0.3		%
De-emphasis Time Constant		DE=0		75		μs
		DE=1		50		μs
Audio Common Mode Voltage range			0.85	1.05	1.6	V
Audio Output Load Resistance	R_L	Single-ended		32		Ω
Power-up Time			200		600	ms

Notes:
1. FMOD=1KHz, 75us de-emphasis
2. MONO=1
3. △F=22.5KHz
4. VEMF=1mV, F_{RX}=32MHz~110MHz
5. RFAGCD=1
6. △F=75KHz
7. VOLUME<4:0>=11111
8. The supported RCLK frequency is continuous. Please refer to application notes.
9. FM_GAIN=6
10. Without weighting filter
11. 32ohm load

Table 5: MW Receiver Characteristics

(Unless otherwise noted Ta = -30~70℃, AVDD = DVDD = 2.1V to 3.6V)

Parameter	Symbol	Test/Operating Condition	Min	Typ	Max	Units
MW Frequency Range	F_{rx}		500		1750	KHz
Sensitivity[1,2,4,5,6,7]	Sen	(S+N)/N=26dB		15		uVEMF
Audio Output Voltage[1,3,4,5,6,7,8]		32ohm load		360		mV_{RMS}
Audio Mono S/N[1,2,3,4,5,6,7]				55		dB
Audio THD[1,2,4,5,6,7]				0.3	0.6	%
Antenna inductance	L		360	-	620	uH

Notes:
1. FMOD=1KHz
2. Modulation index is 30%
3. VEMF=1mV, Frx=500KHz~1750KHz

4. VOLUME<4:0>=11111
5. MW_GAIN=4
6. MW_VOLUME=10
7. Without weighting filter
8. Modulation index is 80%

Table 6: SW Receiver Characteristics

(Unless otherwise noted Ta = -30~70℃, AVDD = DVDD = 2.1V to 3.6V)

Parameter	Symbol	Test/Operating Condition	Min	Typ	Max	Units
SW Frequency Range	F_{rx}		1.75		32	MHz
Sensitivity[1,2,3,5,6,7,8,]	Sen	(S+N)/N=20dB		13		uVemf
Audio Output Voltage[2,4,5,6,7,8,9]		32ohm load		360		mV_{RMS}
Audio Mono S/N[2,3,4,5,6,7,8]				55	62	dB
Audio THD[2,3,4,5,6,7,8]				0.3	0.6	%

Notes:
1. With External LNA
2. FMOD=1KHz
3. Modulation index is 30%
4. VEMF=1mV
5. VOLUME<4:0>=11111
6. SW_GAIN=4
7. SW_VOLUME=10
8. Without weighting filter
9. Modulation index is 80%

Table 7: Power-On Reset Timing Characteristics

(Unless otherwise noted Ta = -30~70℃, AVDD = DVDD = 2.1V to 3.6V)

Parameter	Symbol	Test/Operating Condition	Min	Typ	Max	Units
Pulse Width	t_{pw}		100			us
Rising Edge	t_{re}		10		50000	us

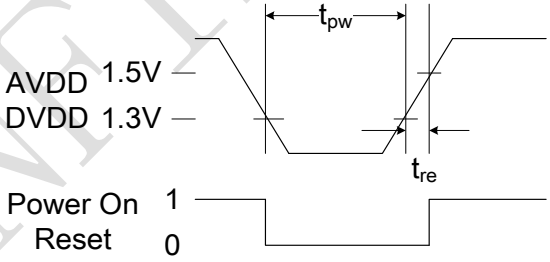


Figure 1: Power-On Reset Timing Parameters

Table 8: 2-wire Interface Characteristics[1]

(Unless otherwise noted Ta = -30~70℃, AVDD = DVDD = 2.1V to 3.6V)

Parameter	Symbol	Test/Operating Condition	Min	Typ	Max	Units
SCL Frequency	f_{SCL}		0	-	-	KHz
SCL Low Time	t_{LOW}		1.3	-	-	us
SCL High Time	t_{HIGH}		0.6	-	-	us
SCL Input to SDA Falling Edge Setup (START)	$t_{SU:STA}$		0.6	-	--	us
SCL Input to SDA Falling Edge Hold (START)	$t_{HD:STA}$		0.6	-	-	us
SDA Input to SCL Rising Edge Setup	$t_{SU:DAT}$		100	-	-	ns

SDA Input to SCL Falling Edge Hold[2]	$t_{HD:DAT}$		0	-	900	ns
SCL Input to SDA Rising Edge Setup (STOP)	$t_{SU:STO}$		0.6	-	-	us
STOP to START Time	t_{BUF}		1.3	-	-	us
SDA Output Fall Time	$t_{f:OUT}$			-	250	ns
SDA Input, SCL Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$			-	300	ns
SCL, SDA Capacitive Loading	C_b		-	-	50	pF
Input Filter Pulse Suppression	t_{SP}		-	-	50	ns

Notes:
1. When POWER DOWN, SCL and SDA are low impedance.
2. The maximum $t_{HD:DAT}$ has only to be met when f_{SCL} = 400 KHz.

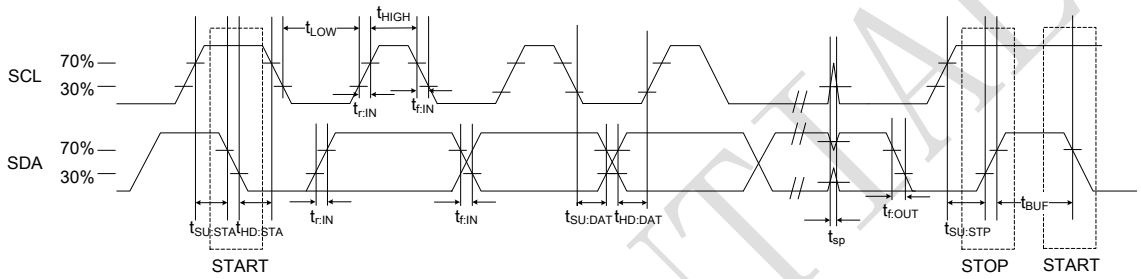
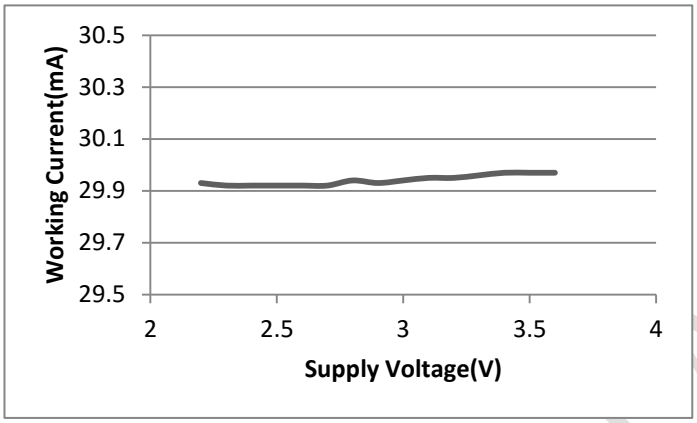


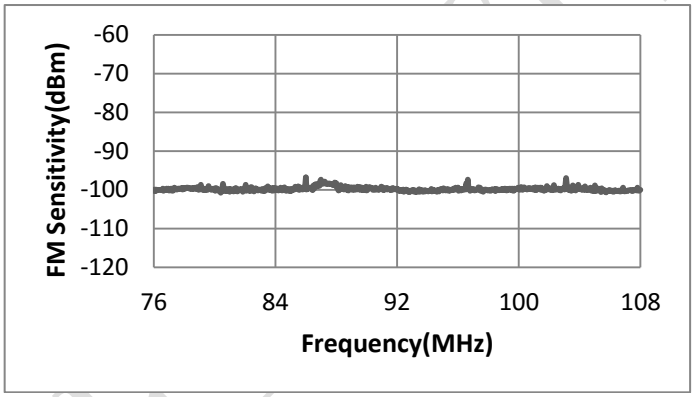
Figure 2: 2-wire Interface Read and Write Timing Parameters

2. Typical performance characteristics

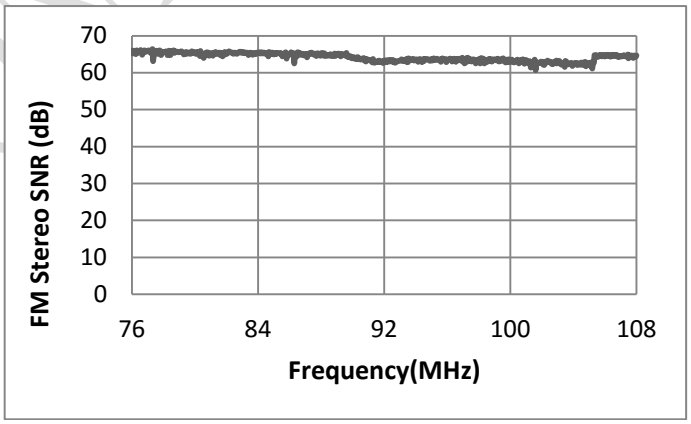
2.1. FM Characteristics



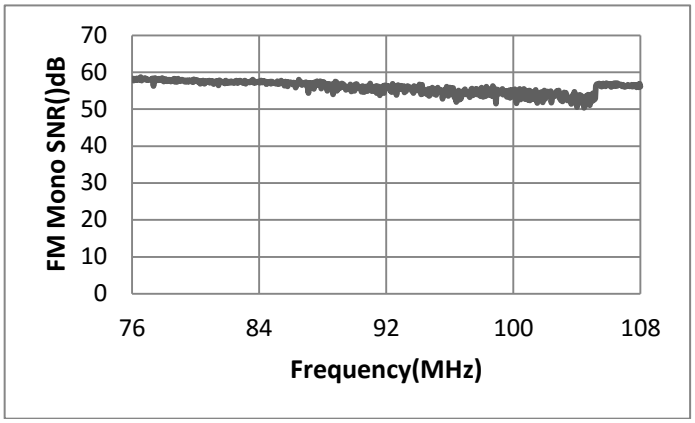
Test condition (Ta = 27℃, Crystal=32.768KHz, FMOD=1KHz, 75us de-emphasis, MONO=1, Carrier Frequency=98MHz, Carrier Power=60dBuVEMF, △F=22.5KHz,Without weighting filter, Load=100Kohm)



Test condition (Ta = 27℃, VDD= 3.0V, Crystal=32.768KHz, SNR=40dB, FMOD=1KHz, 75us de-emphasis, MONO=1, △F=22.5KHz,Without weighting filter)

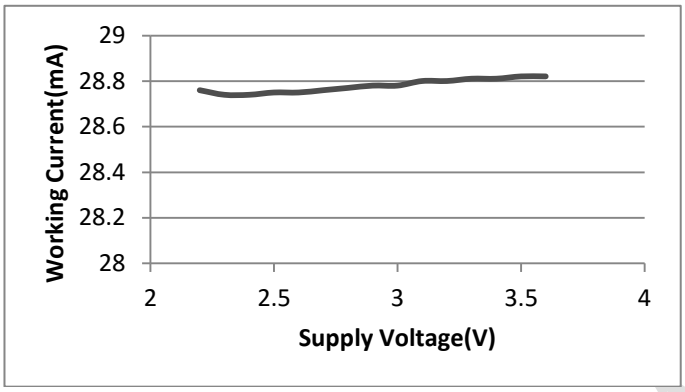


Test condition (Ta = 27℃, VDD= 3.0V, Crystal=32.768KHz, FMOD=1KHz, 75us de-emphasis, MONO=0, △F=75KHz,P_{in}=60dBuVEMF, Without weighting filter)

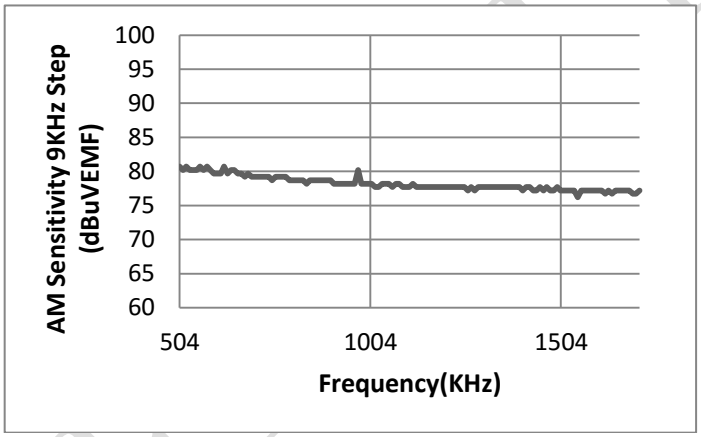


Test condition (Ta = 27℃, VDD= 3.0V, Crystal=32.768KHz, FMOD=1KHz, 75us de-emphasis, MONO=1, △F=22.5KHz,P_{in}=60dBuVEMF, Without weighting filter)

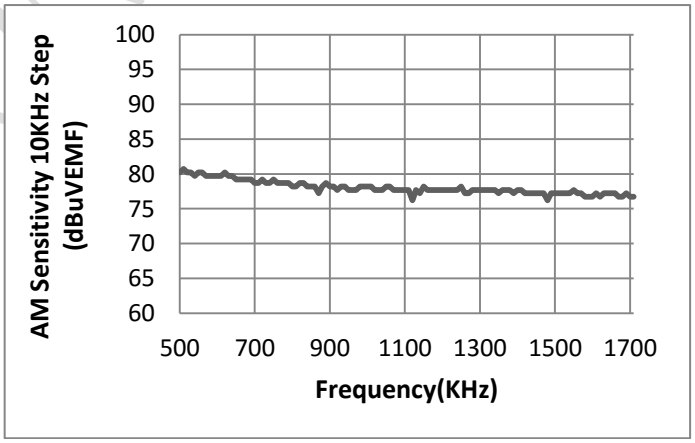
2.2. MW Characteristics



Test condition (Ta = 27℃, Crystal=32.768KHz, FMOD=1KHz, 75us de-emphasis, Carrier Frequency=999KHz, Carrier Power=99dBuVEMF, AM modulation index=30%, Without weighting filter, Load=100Kohm, ferrite antenna =420uH, distance between Tx & Rx antenna=60cm)



Test condition (Ta = 27℃, VDD= 3.0V, Crystal=32.768KHz, SNR=20dB, FMOD=1KHz,AM modulation index=30%,Without weighting filter, ferrite antenna =420uH,distance between Tx&Rx antenna=60cm)



Test condition (Ta = 27℃, VDD= 3.0V, Crystal=32.768KHz, SNR=20dB, FMOD=1KHz,AM modulation index=30%,Without weighting filter, ferrite antenna =420uH,distance between Tx&Rx antenna=60cm)

3. Pin List

Table 9: Pin list

Pin Index	Name	I/O Type	Description
1	AMINN	Analog Input	AM RF negative input.
2	AMINP	Analog Input	AM RF positive input.
3	RFINP	RF Input	FM RF input.
4	RFGND	RF Ground	RF ground.
5	DVSS	Digital Ground	Digital ground.
6	DVDD	Digital Power	Digital power supply.
7	INT	Digital Output	Interrupt output.
8	CH	Analog Input	Channel adjustment.
9	SDA	Digital I/O	SDA of 2-wire interface. Tied to an internal 47kohm pull-up resistor.
10	SCL	Digital I/O	SCL of 2-wire interface. Tied to an internal 47kohm pull-up resistor.
11	ROUT	Analog Output	Right channel audio output.
12	LOUT	Analog Output	Left channel audio output.
13	AVSS	Analog Ground	Analog ground.
14	XI/RCLK	Analog I/O	Crystal.
15	XO	Analog I/O	Crystal.
16	AVDD	Analog Power	Power supply.

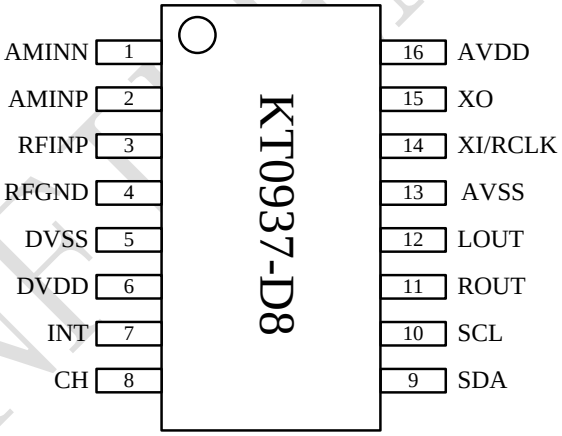


Figure 3: KT0937-D8 Pin assignment (Top view)

4. Function Description

4.1. Overview

KT0937-D8 offers a true single-chip, full-band FM/MW/SW and versatile radio solution by minimizing the external components and offering a variety of configurations. There are no external filters or frequency-tuning devices thanks to a proprietary digital low-IF architecture, a fully-integrated LNA, automatic gain control(AGC), high-performance ADCs, high-quality analog and digital filters, and an on-chi high-fidelity Class-AB driver further eliminates the need for any external audio amplifiers and can drive stereo headphones directly.

4.2. FM Receiver

KT0937-D8 enters FM mode by setting register AM_FM to 0. The FM receiver is based on the architecture of KT Micro's latest generation FM receiver chips in mass production. There are no external filters or frequency-tuning devices thanks to a proprietary digital low-IF architecture consisting of a fully-integrated LNA, an automatic gain control (AGC), a set of high-performance ADCs, high-quality analog and digital filters, and an on-chip low-noise self-tuning VCO. The on-chip high-fidelity Class-AB driver further eliminates the need for external audio amplifiers and can drive stereo headphones directly.

4.3. AM Receiver

KT0937-D8 enters AM mode by setting register AM_FM to 1. The AM Receiver employs a similar digital low IF architecture and share many circuits with the FM receiver. The minimum AM channel spacing can be set to 1KHz. For SW, the AM receiver supports arbitrary frequency range from 1.75MHz to 32MHz. The bandwidth of the channel filter can be set to 1.2KHz to 6KHz to suit various requirements by setting register FLT_SEL<2:0>.

The MW receiver in KT0937-D8 can provide accurate and automatic MW tuning without manual alignment. It supports ferrite loop antenna with value between 360uH and 620uH.

4.4. Operation Bands

KT0937-D8 supports worldwide FM bands, MW bands and SW band. The FM receiver covers frequencies from 32MHz to 110MHz. The MW band is from 500KHz to 1750KHz. The SW band is from 1.75MHz to 32MHz.

4.5. Standby

To enter standby mode, the STDBY register shall be set to 1 through 2-wire interface. To quit standby mode, STDBY should be set to 0.

4.6. Crystal and reference clock

KT0937-D8 integrates a low frequency crystal oscillator that supports 32.768KHz or 38KHz crystals. Alternatively a CMOS level external reference clock may be used by setting the RCLK_EN register to 1 and setting FPFD<19:0> according to the frequency of the reference clock. The FPFD<19:0> is the frequency value in the unit of 1/16Hz. In order to illuminate the usage of these bits clearly some examples are given in Table 10.

Table 10: Examples using different crystal or reference clock

	RCLK_EN	FPFD<19:16>	FPFD<15:0>	DIVIDERP<10:0>	DIVIDERN<10:0>
32.768KHz crystal	0	0x08	0x0000	0x0001	0x029C
38KHz crystal	0	0x09	0x4700	0x0001	0x0240
32.768KHz reference clock	1	0x08	0x0000	0x0001	0x029C
75KHz reference clock	1	0x09	0x27C0	0x0002	0x0247
4.2336 MHz reference clock	1	0x07	0x5499	0x008D	0x02D9
12MHz reference clock	1	0x07	0xD000	0x0177	0x02AC
24MHz reference clock	1	0x07	0xD000	0x02EE	0x02AC
40MHz reference clock	1	0x07	0xD000	0x04E2	0x02AC

4.7. User-Machine Interface

KT0937-D8 offers multiple user-machine interface options including Key Mode (push button) and Dial Mode (tuning wheel).

4.7.1. Key Mode

KT0937-D8 allows user to control the channel by using keys/buttons to send digital control signals to CH pin. Please refer to Figure 4 for a typical application circuit. The key mode is enabled by setting CH_PIN<1:0>=01.

The CH key mode is enabled by setting CH_PIN<1:0> to 01. Figure shows its connection.

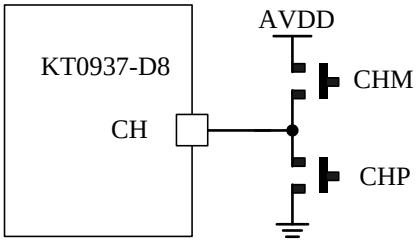


Figure 4: CH pin connection in key-mode

4.7.2. Dial Mode

KT0937-D8 supports a unique Dial Mode whose application circuit is shown in Figure 13.
The dial is implemented by a variable resistor with the center tap connected to the chip. KT0937-D8 measures the ratio of two parts of the variable resistor and maps the result to the real control parameters, such as channel frequency.

The channel controller enters dial mode by setting register CH_PIN<1:0> to 10. The illustration circuit is shown in Figure 5. If the center tap of the variable resistor is located in the white area, the tuned channel could be expressed as:

$$f_{tune} = \frac{X}{X+Y}(f_{top} - f_{bot} + 2 \times N_{guard} \times f_{step}) - N_{guard} \times f_{step} + f_{bot}$$

Where f_{step} is the channel step, set by register FM_SPACE<1:0> , MW_SPACE<1:0> and SW_SPACE<1:0>, f_{top} is the upper bound of the band, f_{bot} is the lower bound of the band and N_{guard} is the number of guard channel in channel step to prevent mechanical limit of the wheels. Each band's guard number can be configured by register CH_GUARD<7:0>. When the center tap goes in the shaded guard area, the tuned channel stays at the upper or lower bound of band.

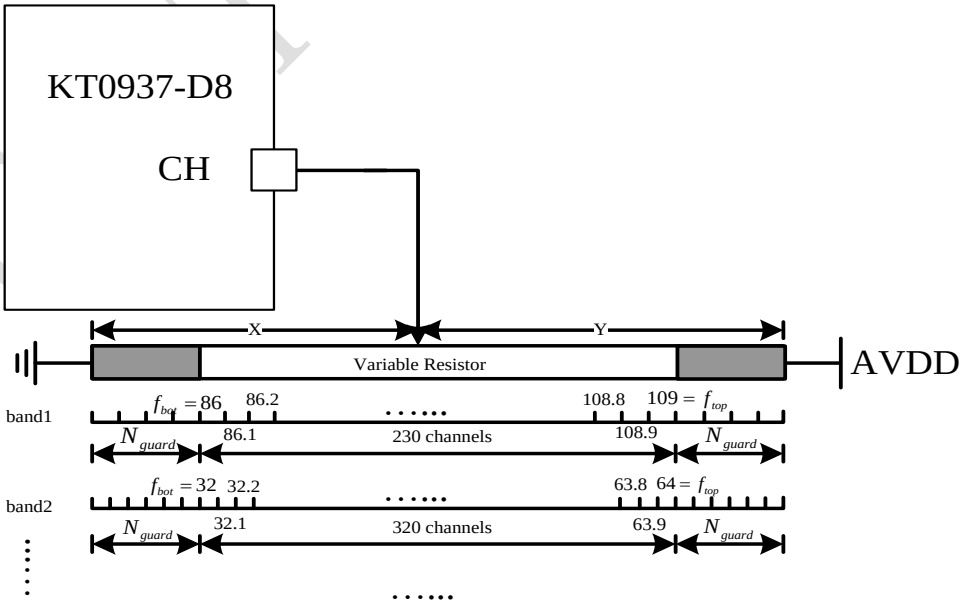


Figure 5: CH pin connection in dial-mode

4.8. Tune Interrupt

The INT external interrupt sources are configurable as active high or low, edge or level sensitive.
The TUNE_INT_PL (INT Polarity) bit in the 0x001F register select active high or active low. The TUNE_INT_MODE (INT Mode) bit in 0x0022 register select level or edge sensitive. The table below lists the possible configurations.
In the level active mode, the interrupt flag must be manually cleared by the INT_PIN bit in the 0x004F register.

Table 11 : Interrupt Selection

TUNE_INT_MODE	TUNE_INT_PL	INT Interrupt	Automatically Cleared by HW
1	0	Active low, edge sensitive	Yes
1	1	Active high, edge sensitive	Yes
0	0	Active low, level sensitive	No (INT_PIN= 2b'01)
0	1	Active high, level sensitive	No (INT_PIN= 2b'10)

4.9. Digital Signal Processing

4.9.1. FM Stereo Decoder

The digitized IF signal is fed to the FM demodulator which demodulates the signal and outputs a digital multiplexed (MPX) signal consisting of L+R audio, L-R audio, 19KHz pilot tone. The left channel signal and the right channel signal can be extracted from the MPX signal by simply adding and subtracting the L+R signal and L-R signal. The spectrum diagram is shown in Figure 6.

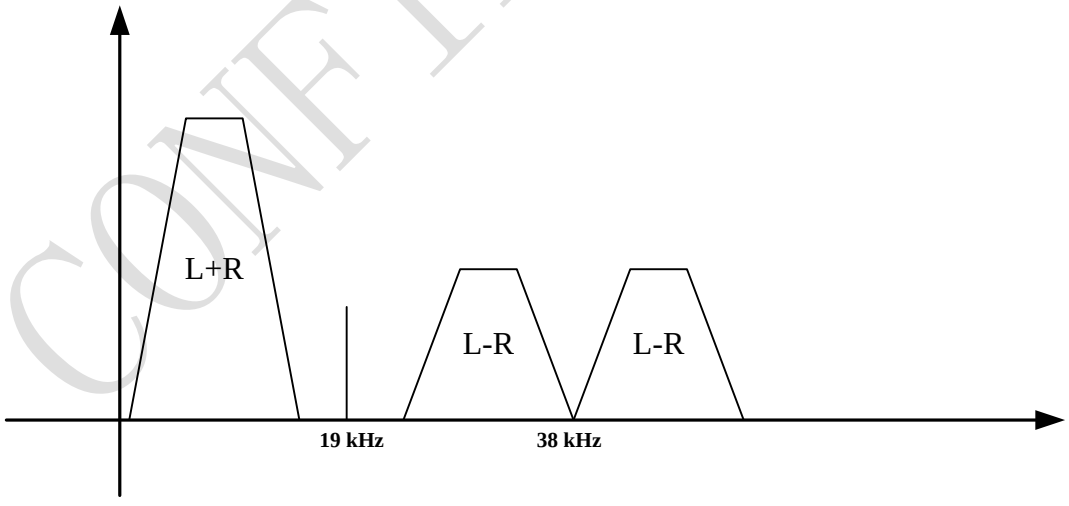


Figure 6: Spectrum diagram of the MPX signal

4.9.2. Mute / Softmute

KT0937-D8 can be hard muted by setting VOLUME<4:0> to 0 and the output of the audio signal is set to the common mode voltage.

FM:
There is also a Soft Mute feature that is enabled by setting FM_DSMUTE to 0. In this mode, the audio volume is gradually attenuated when the signal reception is weak. (i.e. when the RSSI or SNR is below a certain level defined by FM_SMUTE_START_RSSI<2:0> or FM_SMUTE_START_SNR<5:0>, respectively.) The attenuation slope can be configured through FM_SMUTE_SLOPE_RSSI<2:0> or FM_SMUTE_SLOPE_SNR<2:0>, respectively.

The maximum attenuation of volume is -21dB when RSSI is used as soft mute judgment threshold. The maximum attenuation of volume is -12dB when SNR is used as soft mute judgment threshold. The maximum total attenuation of volume can be configured through FM_SMUTE_MIN_GAIN<2:0>.

MW:
There is also a Soft Mute feature that is enabled by setting MW_DSMUTE to 0. In this mode, the audio volume is gradually attenuated when the signal reception is weak. (i.e. when the RSSI and SNR are below a certain level as defined by MW_SMUTE_START_RSSI<6:0> or MW_SMUTE_START_SNR<6:0>, respectively.) The attenuation slope can be configured through MW_SMUTE_SLOPE_RSSI<2:0> or MW_SMUTE_SLOPE_SNR<2:0>, respectively.

The maximum attenuation of volume is -21dB when RSSI is used as soft mute judgment threshold. The maximum attenuation of volume is -12dB when SNR is used as soft mute judgment threshold. The maximum total attenuation of volume can be configured through MW_SMUTE_MIN_GAIN<2:0>.

SW:
There is also a Soft Mute feature that is enabled by setting SW_DSMUTE to 0. In this mode, the audio volume is gradually attenuated when the signal reception is weak. (i.e. when the RSSI and SNR are below a certain level as defined by SW_SMUTE_START_RSSI<6:0> or SW_SMUTE_START_SNR<6:0>, respectively.) The attenuation slope can be configured through SW_SMUTE_SLOPE_RSSI<2:0> or SW_SMUTE_SLOPE_SNR<2:0>, respectively.

The maximum attenuation of volume is -21dB when RSSI is used as soft mute judgment threshold. The maximum attenuation of volume is -12dB when SNR is used as soft mute judgment threshold. The maximum total attenuation of volume can be configured through SW_SMUTE_MIN_GAIN<2:0>.

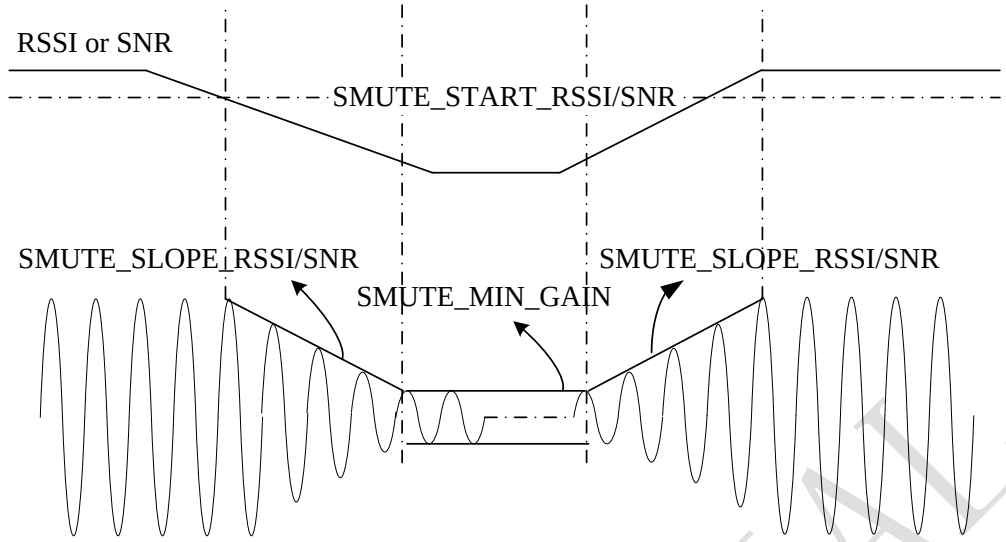


Figure7: Softmute

4.9.3. Stereo / Mono Blending

In order to provide a comfortable listening experience, KT0937-D8 blends the stereo signal with mono signal gradually when in weak reception in FM mode while the noise floor keep at the same level. The stereo separation starts increasing when the RSSI (SNR) of KT0937-D8 grows up to the level defined by BLEND_START_RSSI<3:0> (BLEND_START_SNR<5:0>) and stop increasing when meets the level defined by the BLEND_STOP_RSSI<3:0> (BLEND_STOP_SNR<5:0>). The blending is disabled when DBLEND is set to 1. BLEND_MOD is used to select judgment condition: RSSI or SNR.

MONO playback mode can be forced by setting the MONO to 1.

4.9.4. Bass

KT0937-D8 provides bass boost feature for audio enhancement. The gain of the bass boost can be programmed through BASS<1:0>. With BASS<1:0>=00, this feature is disabled.

4.9.5. Stereo DAC, Audio Filter and Driver

Two high-quality audio digital-to-analog converters (DAC) are integrated along with high-fidelity analog audio filters and Class-AB drivers. Headphones with impedance as low as 16ohms can be direct driven without adding external audio drivers. An integrated anti-pop circuit suppresses the click-and-pop sound during power up and power down.

In order to suit different applications, the gain of the audio driver can be adjusted through register bits FM_GAIN<2:0>, MW_GAIN<3:0>, SW_GAIN<3:0>, MW_VOLUME<3:0> and SW_VOLUME<3:0> to avoid the saturation in output stage, the common mode voltage can also be adjust according to different power supply voltage through register bits AUDV_DCLVL<2:0>.

4.9.6. AM Channel Filter Bandwidth

KT0937-D8 provides programmable AM channel bandwidth from 1.2KHz to 6KHz through FLT_SEL<2:0>.

4.10. 2-wire Control Interface

Write Operations:

BYTE WRITE:

The write operation is accomplished via a 3-byte sequence:

Serial address with write command
Register address
Register data

A write operation requires an 8-bit register address following the device address word and acknowledgment. Upon receipt of this address, the KT0937-D8 will again respond with a "0" and then clock in the 8-bit register data. Following receipt of the 8-bit register data, the KT0937-D8 will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition (see **Figure 8**).

Read Operations:

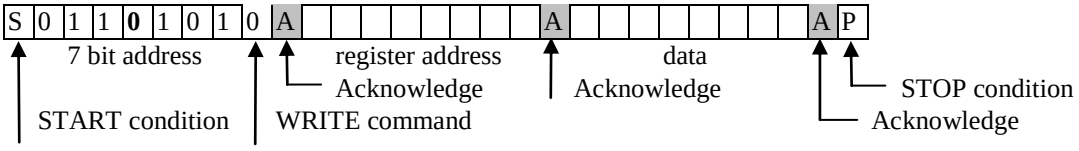
RANDOM READ:

The read operation is accomplished via a 4-byte sequence:

Serial address with write command
Register address
Serial address with read command
Register data

Once the device address and register address are clocked in and acknowledged by the KT0937-D8, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The KT0937-D8 acknowledges the device address and serially clocks out the register data. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 8).

RANDOM REGISTER WRITE PROCEDURE



RANDOM REGISTER READ PROCEDURE

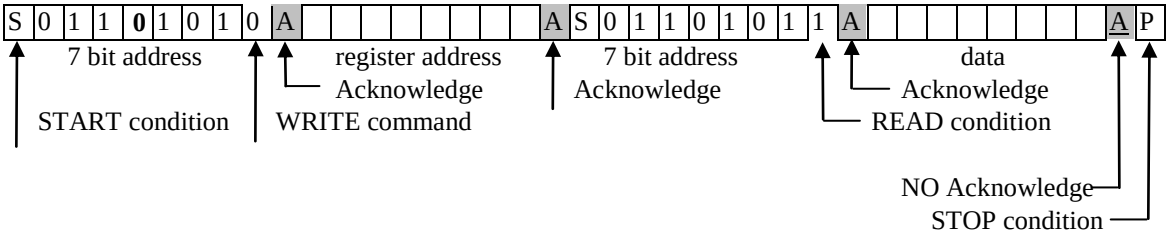


Figure 8: Serial Interface Protocol

CURRENT ADDRESS READ: The internal data register address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the KT0937-D8, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 9)

CURRENT REGISTER READ
PROCEDURE

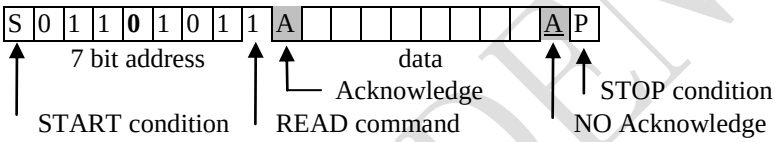


Figure 9: Serial Interface Protocol

Note: The serial controller supports slave mode only. Any register can be addressed randomly.

The address of the slave in the first 7 bits and the 8th bit tells whether the master is receiving data from the slave or transmitting data to the slave. The 2-wire write address is 0x6A and the read address is 0x6B.

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure10). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see **Figure** 11).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the KT0937-D8 in a standby power mode (see **Figure** 11).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the KT0937-D8 in 8-bit words. The KT0937-D8 sends a "0" to acknowledge

that it has received each word. This happens during the ninth clock cycle (see **Figure** 12).

Data Validity

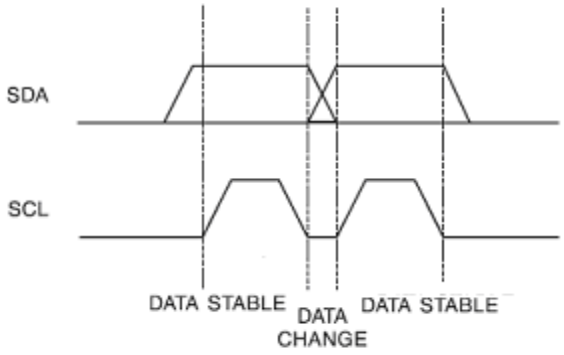


Figure10: Clock and Data Transitions

Start and Stop Definition

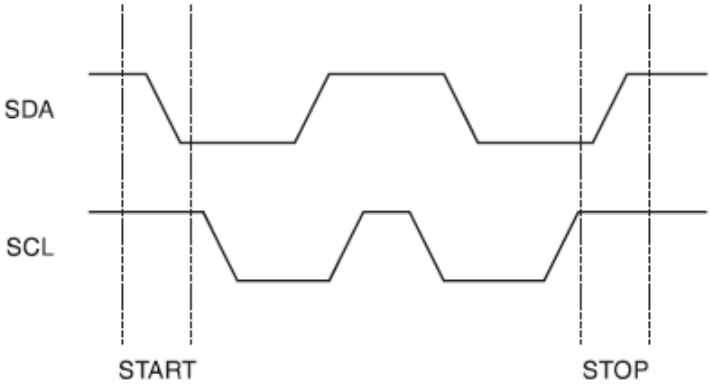


Figure 11: Start and Stop Definition

Output Acknowledge

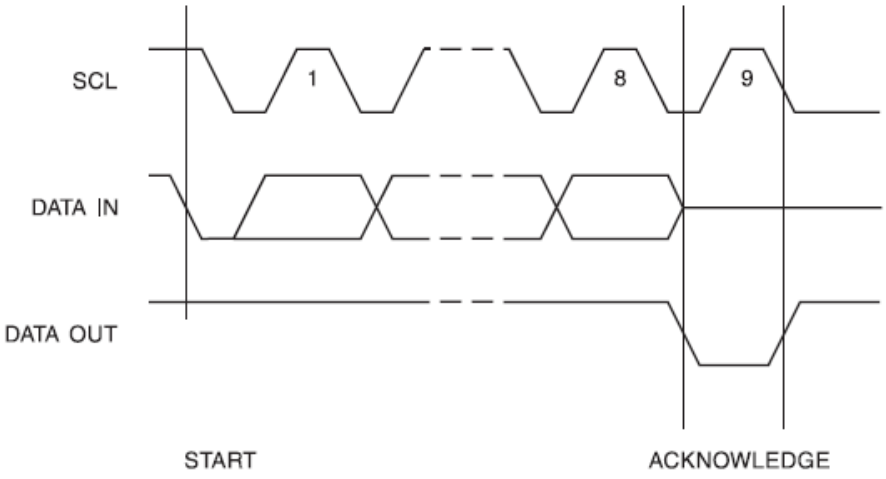


Figure 12: Acknowledge

4.11. Register Bank

4.11.1. DEVICEID0 (Address 0x0000)

Bit	Name	Access	Default Value	Functional Description
7:0	Device ID0	R	0x82	

4.11.2. DEVICEID1 (Address 0x0001)

Bit	Name	Access	Default Value	Functional Description
7:0	Device_ID1	R	0x06	

4.11.3. KTMARK0 (Address 0x0002)

Bit	Name	Access	Default Value	Functional Description
7:0	KT_Mark0	R	0x4B	**ASCII form of string "K".**

4.11.4. KTMARK1 (Address 0x0003)

Bit	Name	Access	Default Value	Functional Description
7:0	KT_Mark1	R	0x54	**ASCII form of string "T".**

4.11.5. PLLCFG0 (Address 0x0004)

Bit	Name	Access	Default Value	Functional Description
7	SYS_CFGOK	RW	0	**Clock initialization completed.**
6:3	Reserved	RW	000_0	**Reserved.**
2:0	DIVIDERP<10:8>	RW	000	**PLL divider P configuration.**

4.11.6. PLLCFG1 (Address 0x0005)

Bit	Name	Access	Default Value	Functional Description
7:0	DIVIDERP<7:0>	RW	0x01	**PLL divider P configuration.**

4.11.7. PLLCFG2 (Address 0x0006)

Bit	Name	Access	Default Value	Functional Description
7:3	Reserved	RW	0000_0	**Reserved.**
2:0	DIVIDERN<10:8>	RW	010	**PLL divider N configuration.**

4.11.8. PLLCFG3 (Address 0x0007)

Bit	Name	Access	Default Value	Functional Description
7:0	DIVIDERN<7:0>	RW	0x9C	**PLL divider N configuration.**

4.11.1. SYSCLK_CFG0 (Address 0x0008)

Bit	Name	Access	Default Value	Functional Description
7:4	Reserved	RW	0000	**Reserved.**
3:0	FPFD<19:16>	RW	1000	**Phase-detection Frequency. FPFD<19:0> = External Xtal clock or RCLK frequency / DIVIDERP.**

4.11.2. SYSCLK_CFG1 (Address 0x0009)

Bit	Name	Access	Default Value	Functional Description
7:0	FPFD<15:8>	RW	0x00	**Phase-detection Frequency. FPFD<19:0> = External Xtal clock or RCLK frequency / DIVIDERP.**

4.11.3. SYSCLK_CFG2 (Address 0x000A)

Bit	Name	Access	Default Value	Functional Description
7:0	FPFD<7:0>	RW	0x00	**Phase-detection Frequency. FPFD<19:0> = External Xtal clock or RCLK frequency / DIVIDERP.**

4.11.4. XTALCFG (Address 0x000D)

Bit	Name	Access	Default Value	Functional Description
7:5	Reserved	RW	110	**Reserved.**
4	RCLK_EN	RW	0	**Reference Clock Enable.** 0 = Crystal. 1 = External reference clock.
3:0	Reserved	RW	0011	**Reserved.**

4.11.5. RXCFG0 (Address 0x000E)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	RW	00	**Reserved.**
5	STDBY	RW	0	**Standby Mode Control.** 0 = Normal operation. 1 = Standby mode.
4	DSP_RST	RW	0	**DSP Reset**
3:0	Reserved	RW	0000	**Reserved.**

4.11.6. RXCFG1 (Address 0x000F)

Bit	Name	Access	Default Value	Functional Description
7:5	Reserved	R	000	**Reserved.**
4:0	VOLUME<4:0>	RW	1_1111	**Volume Control Bits:** 11111 = 0dB 11110 = -2dB 11101 = -4dB …… 00010 = -58dB 00001 = -60dB 00000 = Mute

4.11.7. PVTCALI0 (Address 0x0010)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	**Reserved.**
6	STBYLDO_CALI_EN	RW	0	**Standby LDO Calibration Enable.** 0 = Disable. 1 = Enable.

Bit	Name	Access	Default Value	Functional Description
5:0	Reserved	RW	00_000	**Reserved.**

短波模式必须设置

4.11.8. BANDCFG0 (Address 0x0016)

Bit	Name	Access	Default Value	Functional Description
7:5	Reserved	RW	100	**Reserved.**
4	SW_EN	RW	0	**Short Wave Enable Control:** 0 = Disable 1 = Enable
3:0	Reserved	RW	1010	**Reserved.**

4.11.9. BANDCFG2 (Address 0x0018)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	RW	01	**Reserved.**
5:4	FM_SPACE<1:0>	RW	01	**FM Band Space Selection.** 00 = 200 kHz (USA, Europe) 01 = 100KHz (Europe, Japan) 10 = 50KHz 11 = 50KHz
3:2	Reserved	RW	10	**Reserved.**
1:0	MW_SPACE<1:0>	RW	01	**MW Band Space Selection.** 00 = 1kHz 01 = 9kHz 10 = 10kHz 11 =10kHz

4.11.10. BANDCFG3 (Address 0x0019)

Bit	Name	Access	Default Value	Functional Description
7:5	MW_SMUTE_MIN_GAIN<2:0>	RW	001	**The Total Attenuation of Volume Can Be Configured:** 000 = -9dB 001 = -12dB 010 = -15dB 011 = -18dB 100 = -21dB 101 = -24dB 110 = -27dB 111 = -30dB
4:2	FM_SMUTE_MIN_GAIN<2:0>	RW	1_00	**The Total Attenuation of Volume Can Be Configured:** 000 = -9dB 001 = -12dB 010 = -15dB 011 = -18dB 100 = -21dB 101 = -24dB 110 = -27dB 111 = -30dB
1:0	SW_SPACE<1:0>	RW	01	**SW Band Space Selection.** B'00 = 1kHz B'01 = 5kHz B'10 = 9kHz B'11 =10kHz

4.11.11. MUTECFG0 (Address 0x001A)

Bit	Name	Access	Default Value	Functional Description
7	FM_DSMUTE	RW	0	**FM Softmute Disable.** 0 = FM softmute enable. 1 = FM softmute disable.
6	MW_DSMUTE	RW	0	**MW Softmute Disable.** 0 = MW softmute enable. 1 = MW softmute disable.
5:0	Reserved	R	00_1000	**Reserved.**

4.11.12. G38KCFG0 (Address 0x001B)

Bit	Name	Access	Default Value	Functional Description
7:3	Reserved	RW	1000_0	**Reserved.**
2	POWERON_FINISH	RW	0	**Power On Flow Finish Flag.** 0 = Initialization. 1 = Finish.
1:0	Reserved	RW	0	**Reserved.**

4.11.13. G38KCFG1 (Address 0x001C)

Bit	Name	Access	Default Value	Functional Description
7:0	ST_DEMOD<7:0>	RW	0x00	**Stereo Demodulation Indicator.** 0x00 = Mono. Others = Stereo.

4.11.14. SOFTMUTE0 (Address 0x001D)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	1	**Reserved.**
6:0	MW_SMUTE_START_RSSI<6:0>	RW	001_0111	**The Starting Level of Attenuation According to RSSI in MW Mode.**

4.11.15. SOFTMUTE1 (Address 0x001E)

Bit	Name	Access	Default Value	Functional Description
7:3	Reserved	RW	0010_0	**Reserved.**
2:0	MW_SMUTE_SLOPE_RSSI<2:0>	RW	100	**The Slope of Attenuation According to RSSI in AM Mode.** 000=4 001=3 010=2 011=1 100=1/2 101=1/3 110=1/4 111=0

4.11.16. SOFTMUTE2 (Address 0x001F)

Bit	Name	Access	Default Value	Functional Description

7	TUNE_INT_PL	RW	0	**Interrupt Polarity.** 0 = INT interrupt is active low. 1 = INT interrupt is active high.
6:4	FM_SMUTE_START_RSSI<2:0>	RW	101	**The Starting Level of Attenuation According to RSSI in FM Mode:** 000 = 22 dBuVEMF 001 = 20 dBuVEMF 010 = 18 dBuVEMF 011 = 16 dBuVEMF 100 = 14 dBuVEMF 101 = 12 dBuVEMF 110 = 10 dBuVEMF 111 = 8 dBuVEMF
3	Reserved	RW	0	**Reserved.**
2:0	FM_SMUTE_SLOPE_RSSI<2:0>	RW	011	The Slope of Attenuation According to RSSI in FM Mode**:** 000 = 4 001 = 3 010 = 2 011 = 1 100 = 1/2 101 = 1/3 110 = 1/4 111 = 0

4.11.17. SOFTMUTE3 (Address 0x0020)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	**Reserved.**
6:0	MW_SMUTE_START_SNR<6:0>	RW	011_0000	**The Starting Level of Attenuation According to SNR in MW Mode.** 000_0000 = 0 000_0001 = 1 …… 111_1110 = 126 111_1111 = 127

4.11.18. SOFTMUTE4 (Address 0x0021)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	**Reserved.**
6:4	MW_SMUTE_SLOPE_SNR<2:0>	RW	000	**The Slope of Attenuation According to SNR in MW Mode:** 000 = 4 001 = 3 010 = 2 011 = 1 100 = 1/2 101 = 1/3 110 = 1/4 111 = 0
3	Reserved	RW	0	**Reserved.**
2:0	FM_SMUTE_SLOPE_SNR<2:0>	RW	010	**The Slope of Attenuation According to SNR in FM**

Bit	Name	Access	Default Value	Functional Description
				Mode: 000 = 4 001 = 3 010 = 2 011 = 1 100 = 1/2 101 = 1/3 110 = 1/4 111 = 0

4.11.19. SOFTMUTE5 (Address 0x0022)

Bit	Name	Access	Default Value	Functional Description
7	TUNE_INT_EN	RW	0	**Tune Interrupt Output Enable Bit.** 0 = Disable. 1 = Enable.
6	TUNE_INT_MODE	RW	0	**Tune Interrupt Mode Selection.** This bit selects whether the configured INT interrupt will be edge or level sensitive. 0 = INT is level triggered. 1 = INT is edge triggered.
5:0	FM_SMUTE_START_SNR<5:0>	RW	01_0101	**The Starting Level of Attenuation According to SNR in FM Mode.** 00_0000 = 0 00_0001 = 1 …… 11_1110 = 62 11_1111 = 63

4.11.20. SOUNDCFG (Address 0x0028)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	R	00	**Reserved.**
5:4	BASS<1:0>	RW	00	**Bass Boost Effect Mode Selection:** 00 = Bypass 01 = 9.4 dB@70Hz 10 = 13.3dB@70Hz 11 = 18.2dB@70Hz
3:0	Reserved	RW	1101	**Reserved.**

4.11.21. FLT_CFG (Address 0x0029)

Bit	Name	Access	Default Value	Functional Description
7:5	Reserved	RW	000	**Reserved.**
4	BLEND_MOD	RW	0	**Blend Mode Selection:** 0 = RSSI mode 1 = SNR mode
3:0	Reserved	R	0_0000	**Reserved.**

4.11.22. DSPCFG0 (Address 0x002A)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	1	**Reserved.**
6:4	FM_GAIN<2:0>	RW	100	**Audio Gain for FM Audio Processor:** 000 = 0dB 001 = 3.5dB 010 = 6dB 011 = 9.5dB 100 = -2.5dB 101 = -3.66dB 110 = -6dB 111 = -8.5dB
3:0	Reserved	RW	0000	**Reserved.**

4.11.23. DSPCFG1 (Address 0x002B)

Bit	Name	Access	Default Value	Functional Description
7	MONO	RW	0	**Mono Selection:** 0 = Stereo 1 = Force mono
6:4	Reserved	RW	010	**Reserved.**
3	DE	RW	1	**De-emphasis Time Constant Selection:** 0 = 75us. Used in USA. 1 = 50us. Used in Europe, Australia, Japan.
2:1	Reserved	RW	00	**Reserved.**
0	DBLEND	RW	0	**Blend Disable:** 0 = Blend enable 1 = Blend disable

4.11.24. DSPCFG2 (Address 0x002C)

Bit	Name	Access	Default Value	Functional Description
7:4	BLEND_START_RSSI<3:0>	RW	0101	**The Starting Value of Blend According to RSSI in FM Mode:** 0000 = 8dbuVEMF 0001 = 10dbuVEMF 0010 = 12dbuVEMF 0011 = 14dbuVEMF 0100 = 16dbuVEMF 0101 = 18dbuVEMF 0110 = 20dbuVEMF 0111 = 22dbuVEMF 1000 = 24dbuVEMF 1001 = 26dbuVEMF 1010 = 28dbuVEMF 1011 = 30dbuVEMF 1100 = 32dbuVEMF 1101 = 34dbuVEMF 1110 = 36dbuVEMF 1111 = 38dbuVEMF
3:0	BLEND_STOP_RSSI<3:0>	RW	1111	**The Ending Value of Blend According to RSSI in FM**

				Mode: 0000 = 8dbuVEMF 0001 = 10dbuVEMF 0010 = 12dbuVEMF 0011 = 14dbuVEMF 0100 = 16dbuVEMF 0101 = 18dbuVEMF 0110 = 20dbuVEMF 0111 = 22dbuVEMF 1000 = 24dbuVEMF 1001 = 26dbuVEMF 1010 = 28dbuVEMF 1011 = 30dbuVEMF 1100 = 32dbuVEMF 1101 = 34dbuVEMF 1110 = 36dbuVEMF 1111 = 38dbuVEMF

4.11.25. DSPCFG5 (Address 0x002F)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	RW	00	**Reserved.**
5	ANT_CALI_SWITCH_BAND	RW	0	**Antenna Calibrate When Switching Band.** 0 = Disable. 1 = Enable.
4	BLEND_COMBO_MODE	RW	0	**Blend Combo Mode Enable Bit.** 0 = Disable combo Mode. 1 = Enable combo Mode.
3	Reserved	RW	0	**Reserved.**
2	AM_SUP_ENHANCE	RW	0	**AM suppression Enhance.** 0 = Disable. 1 = Enable.
1	SMUTE_FILTER_EN	RW	0	**Softmute Filter Enable.** 0 = Disable. 1 = Enable.
0	AM_SEL_ENHANCE	RW	0	**AM Channel Selectivity Enhance.** 0 = Disable. 1 = Enable.

4.11.26. DSPCFG6 (Address 0x0030)

Bit	Name	Access	Default Value	Functional Description
7:5	Reserved	RW	101	**Reserved.**
4:0	FM_RSSI_BIAS<4:0>	RW	0_0000	**FM RSSI Bias:** 10000 = -16dB 10001 = -15dB …… 11110 = -2dB 11111 = -1dB 00000 = 0dB 00001 = 1dB …… 01111 = 15dB

4.11.27. DSPCFG7 (Address 0x0034)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	R	00	**Reserved.**
5:0	BLEND_START_SNR<5:0>	RW	00_0000	**The Stop Level of Blend According to SNR in FM Mode.** When the starting value meets the ending value, it is separated immediately.

4.11.28. DSPCFG8 (Address 0x0035)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	R	00	**Reserved.**
5:0	BLEND_STOP_SNR<5:0>	RW	00_0000	**The Stop Level of Blend According to SNR in FM Mode.** When the starting value meets the ending value, it is separated immediately.

4.11.29. SW_CFG0 (Address 0x0038)

Bit	Name	Access	Default Value	Functional Description
7	SW_AFCD	RW	0	**AFC Disable Control Bit in SW Mode:** 0 = AFC enable 1 = AFC disable
6:4	SW_BBAGC_RATIO<2:0>	RW	101	**SW Baseband AGC Ratio:** 000 = 1/inf. 001 = 1/16 010 = 1/8 011 = 1/4 100 = 1/3 101 = 1/2 110 = Reserved 111 = Reserved
3:0	SW_GAIN<3:0>	RW	0100	**Audio Gain for SW Audio Processor:** 0000 = 6dB 0001 = 3dB 0010 = 0dB 0011 = -3dB 0100 = -6dB 0101 = -9dB 0110 = -12dB 0111 = -15dB 1000 = -18dB

4.11.30. SW_CFG1 (Address 0x0039)

Bit	Name	Access	Default Value	Functional Description
7:4	Reserved	RW	0000	**Reserved.**
3:0	SW_VOLUME<3:0>	RW	1010	**SW Volume Control Bits:** 1111 = 0dB 1110 = -0.5dB

Bit	Name	Access	Default Value	Functional Description
				1101 =-1.0dB 1100 = -1.5dB 1011 = -2.0dB 1010 = -2.5dB 1001 = -3.0dB 1000 = -3.5dB 0111 = -4.0dB 0110 = -4.5dB 0101 = -5.0dB 0100 = -5.5dB 0011 = -6.0dB 0010 = -6.5dB 0001 = -7.0dB 0000 = -7.5dB

4.11.31. SW_CFG2 (Address 0x003A)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	RW	00	**Reserved.**
5:0	SW_BBAGC_HI_TH<3:0>	RW	01_1011	**SW Baseband AGC High Threshold:** 0 = 0dBm 1= -3dBm 2=--6dBm …… 32= -96dBm 33= -99dBm

4.11.32. AFC2 (Address 0x003E)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	**Reserved.**
6	FM_AFCD	RW	0	**AFC Disable Control Bit in FM Mode:** 0 = AFC enable. 1 = AFC disable.
5:3	Reserved	RW	00_0	**Reserved.**
2:0	FM_TH_AFC<2:0>	RW	011	**Programmable threshold for FM AFC ᐞF digital IF offset that can be adjusted in FM mode:** 000 = 5k 001 = 15k 010 = 25k 011 = 35k 100 = 50k 101 = 100k 110 = 150k 111 = 200k

4.11.33. AFC3 (Address 0x003F)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	**Reserved.**
6	MW_AFCD	RW	0	**AFC Disable Control Bit in MW Mode:**

Bit	Name	Access	Default Value	Functional Description
				0 = AFC enable. 1 = AFC disable.
5:3	Reserved	RW	00_0	**Reserved.**
2:0	MW_TH_AFC<2:0>	RW	000	**MW AFC Threshold:** 000 = 2944Hz 001 = 4992Hz 010 = 6016Hz 011 = 8064Hz 100 = 9984Hz 101 = 12032 Hz 110 = 14976 Hz 111 = 16256 Hz

4.11.34. ANACFG (Address 0x004E)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	RW	00	**Reserved.**
5:4	DEPOP_TC<1:0>	RW	11	**De-pop Time Constant:** 00 = 250ms 01 = 500ms 10 = 750ms 11 = 1s
3	Reserved	RW	0	**Reserved.**
2:0	AUDV_DCLVL<2:0>	RW	010	**Audio Output Common Voltage:** 000= 0.85v 001=0.91v 010= 1.05v 011= 1.15v 100= 1.20v 101= 1.35v 110= 1.50v 111=1.60v

4.11.35. ANACFG (Address 0x004F)

Bit	Name	Access	Default Value	Functional Description
7:2	Reserved	RW	1000_00	**Reserved.**
1:0	INT_PIN<1:0>	RW	10	**INT pin function control:** 00 = Reserved. 01 = Output high. 10 = Output low. 11 = Reserved.

4.11.36. GPIOCFG2 (Address 0x0051)

Bit	Name	Access	Default Value	Functional Description
7:2	Reserved	RW	0000_00	**Reserved.**
1:0	CH_PIN<1:0>	RW	00	**CH pin function control.** 00 = high Z. 01 = Key controlled channel increase / decrease input. 10 = Dial controlled channel increase / decrease input. 11 = Reserved.

4.11.37. SW_CFG3 (Address 0x0052)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	RW	00	**Reserved.**
5:0	SW_BBAGC_LOW_TH<2:0>	RW	01_0110	**SW Baseband AGC Low Threshold:** 0 = 0dBm 1= -3dBm 2=--6dBm …… 32= -96dBm 33= -99dBm

4.11.38. AMCALI0 (Address 0x0055)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	RW	00	**Reserved.**
5:3	SW_TH_AFC<2:0>		00_0	**SW AFC Threshold:** 000 = 2944Hz 001 = 4992Hz 010 = 6016Hz 011 = 8064Hz 100 = 9984Hz 101 = 12032 Hz 110 = 14976 Hz 111 = 16256 Hz
2:0	MW_Q<2:0>	RW	100	**MW Antenna Q Factor Control.** 000 = Minimum Q factor. …… 111 = Maximum Q factor.

4.11.39. AMCALI1 (Address 0x0056)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	R	00	**Reserved.**
5:0	CAP<13:8>	RW	11_1111	**High 6 Bits of Capacitor for LC Tank:** 0x0000 = Minimum Capacitor. …… 0x3FFF = Maximum Capacitor.

4.11.40. AMCALI2 (Address 0x0057)

Bit	Name	Access	Default Value	Functional Description
7:0	CAP<7:0>	RW	1110_1111	**Low 8 Bits of Capacitor for LC Tank:** 0x0000 = Minimum Capacitor. …… 0x3FFF = Maximum Capacitor.

4.11.41. AMDSP0 (Address 0x0062)

Bit	Name	Access	Default Value	Functional Description
7:4	MW_GAIN<3:0>	RW	0100	**Audio Gain for MW Audio Processor:**

Bit	Name	Access	Default Value	Functional Description
				0000 = 6dB 0001 = 3dB 0010 = 0dB 0011 = -3dB 0100 = -6dB 0101 = -9dB 0110 = -12dB 0111 = -15dB 1000 = -18dB
3	Reserved	R	0	**Reserved.**
2:0	FLT_SEL<2:0>	RW	001	**AM Channel Filter Bandwidth Selection:** 000=1.2KHz 001=2.4KHz 010=3.6KHz 011=4.8KHz 100=6.0KHz

4.11.42. AMDSP1 (Address 0x0063)

Bit	Name	Access	Default Value	Functional Description
7:5	Reserved	RW	000	**Reserved.**
4:0	AM_RSSI_BIAS<4:0>	RW	0_0000	**AM RSSI Bias.** 10000 = -16dB 10001 = -15dB …… 11110 = -2dB 11111 = -1dB 00000 = 0dB 00001 = 1dB …… 01111 = 15dB

4.11.43. AMDSP3 (Address 0x0065)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	1	**Reserved.**
6:4	MW_BBAGC_RATIO<2:0>	RW	101	**MW Baseband AGC Ratio:** 000 = 1/inf. 001 = 1/16 010 = 1/8 011 = 1/4 100 = 1/3 101 = 1/2 110 = Reserved 111 = Reserved
3	Reserved	R	0	**Reserved.**
2:0	AM_BBAGC_BW<2:0>	RW	000	**AM Baseband AGC Bandwidth Selection:** 000 = Minimum Bandwidth …… 111 = Maximum Bandwidth

4.11.44. AMDSP4 (Address 0x0066)

Bit	Name	Access	Default Value	Functional Description
7:3	Reserved	R	0001_1	**Reserved.**

2:0	AM_SNR_MODE_SEL<2:0>	RW	000	**AM SNR Mode Selection:** 000 = AM_SNR_MODE1 001 = AM_SNR_MODE2 010 = AM_SNR_MODE2 011 = AM_SNR_MODE2 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved

4.11.45. AMDSP5 (Address 0x0067)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	R	00	**Reserved.**
5:0	MW_BBAGC_HI_TH<3:0>	RW	01_1011	**MW Baseband AGC High Threshold:** 0 = 0dBm 1 = -3dBm 2 = -6dBm …… 32 = -96dBm 33 = -99dBm

4.11.46. AMDSP6 (Address 0x0068)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	R	00	**Reserved.**
5:0	MW_BBAGC_LOW_TH<3:0>	RW	01_0110	**MW Baseband AGC Low Threshold:** 0 = 0dBm 1 = -3dBm 2 = -6dBm …… 32 = -96dBm 33 = -99dBm

4.11.47. AMDSP7 (Address 0x0069)

Bit	Name	Access	Default Value	Functional Description
7:4	Reserved	RW	1000	**Reserved.**
3:0	MW_VOLUME<3:0>	RW	1010	**MW Volume Control Bits:** 1111 = 0dB 1110 = -0.5dB 1101 = -1.0dB 1100 = -1.5dB 1011 = -2.0dB 1010 = -2.5dB 1001 = -3.0dB 1000 = -3.5dB 0111 = -4.0dB 0110 = -4.5dB 0101 = -5.0dB 0100 = -5.5dB 0011 = -6.0dB 0010 = -6.5dB 0001 = -7.0dB 0000 = -7.5dB

4.11.48. ADC0 (Address 0x0071)

Bit	Name	Access	Default Value	Functional Description
7	CH_ADC_DIS	RW	0	**Channel ADC Enable:** **0 = Enable ADC.** **1 = Disable ADC.**
6:3	Reserved	RW	000_0	**Reserved.**
2	CH_ADC_START	RW	0	**Channel ADC Start:** **0 = None.** **1 = Start.** **Note:** CH_ADC_START register will be automatically cleared, after one clock cycle when it be set to 1.
1:0	Reserved	RW	00	**Reserved.**

4.11.49. ADC3 (Address 0x0074)

Bit	Name	Access	Default Value	Functional Description
7:5	Reserved	RW	111	**Reserved.**
4:0	CH_ADC_WIN<12:8>	RW	0_0001	**Channel ADC Window Length.**

4.11.50. ADC4 (Address 0x0075)

Bit	Name	Access	Default Value	Functional Description
7:0	CH_ADC_WIN<7:0>	RW	0001_0100	**Channel ADC Window Length.**

4.11.51. ADC5 (Address 0x0076)

Bit	Name	Access	Default Value	Functional Description
7:2	Reserved	RW	1010_01	**Reserved.**
1	STBYLDO_PD	RW	1	**Standby LDO Power Down Control:** 0 = Power on. 1 = Power down.
0	Reserved	RW	0	**Reserved.**

4.11.52. STATUS10 (Address 0x0079)

Bit	Name	Access	Default Value	Functional Description
7:0	AFC_AAF<7:0>	R	0x00	**AFC Accumulative Adjust Frequency:** **FM mode:** 0x80 = -128*2048Hz 0x81 = -127*2048Hz …… 0xFF = -1*2048Hz 0x00 = 0Hz 0x01 = 1*2048Hz …… 0x7E=126*2048Hz 0x7F = 127 *2048Hz **AM mode:** 0x80 = -128*128Hz

Bit	Name	Access	Default Value	Functional Description
				0x81 = -127*128Hz …… 0xFF = -1*128Hz 0x00 = 0Hz 0x01 = 1*128Hz …… 0x7E = 126*128Hz 0x7F = 127 *128Hz

4.11.53. FMST_CFG (Address 0x007E)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	**Reserved.**
6:4	BLEND_START_COMBO<2:0>	RW	010	**The Starting Value of Blend According to RSSI** and SNR **in FM Mode.** 000 = 17dBuVEMF 001 = 19dBuVEMF 010 = 21dBuVEMF 011 = 23dBuVEMF 100 = 25dBuVEMF 101 = 27dBuVEMF 110 = 29dBuVEMF 111 = 31dBuVEMF
3:0	Reserved	RW	1100	**Reserved.**

4.11.54. FMTUNE_VALID0 (Address 0x007F)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	**Reserved.**
6:4	FM_TUN_SNR_HITH<2:0>	RW	101	**Set FM SNR High Threshold for Valid Channel Indicator.** 000 = 8 001 = 10 010 = 12 011 = 15 100 = 18 101 = 21 110 = 24 111 = 27
3	Reserved	RW	0	**Reserved.**
2:0	FM_TUN_SNR_LOWTH<2:0>	RW	101	**Set FM SNR Low Threshold for Valid Channel Indicator.** 000 = 6 001 = 8 010 = 10 011 = 12 100 = 15 101 = 18 110 = 21 111 = 24

4.11.55. FMTUNE_VALID1 (Address 0x0080)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	**Reserved.**
6:4	FM_TUN_RSSI_HITH<2:0>	RW	101	**Set FM RSSI High Threshold**

Bit	Name	Access	Default Value	Functional Description
				for Valid Channel Indicator. 001 = -108dBm 010 = -106dBm 011 = -104dBm 100 = -102dBm 101 = -100dBm 110 = -98dBm 111 = -96dBm 111 = -94dBm
3	Reserved	RW	0	**Reserved.**
2:0	FM_TUN_RSSI_LOWTH<2:0>	RW	011	**Set FM RSSI Low Threshold for Valid Channel Indicator.** 000 = -110dBm 001 = -108dBm 010 = -106dBm 011 = -104dBm 100 = -102dBm 101 = -100dBm 110 = -98dBm 111 = -96dBm

4.11.56. MWTUNE_VALID0 (Address 0x0081)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	**Reserved.**
6:0	MW_TUN_SNR_HITH<6:0>	RW	011_1010	**Set MW SNR High Threshold for Valid Channel Indicator.** 000_0000 = 0 000_0001 = 1 …… 111_1110 = 126 111_1111 = 127

4.11.57. MWTUNE_VALID1 (Address 0x0082)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	**Reserved.**
6:0	MW_TUN_SNR_LOWTH<6:0>	RW	011_0101	**Set MW SNR Low Threshold for Valid Channel Indicator.** 000_0000 = -110dBm 000_0001 = -107dBm …… 111_0111 = 9dBm 111_1000 = 10dBm

4.11.58. MWTUNE_VALID2 (Address 0x0083)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	**Reserved.**
6:0	MW_TUN_RSSI_HITH<6:0>	RW	010_0100	**Set MW RSSI High Threshold for Valid Channel Indicator.** 000_0000 = -110dBm 000_0001 = -107dBm …… 111_0111 = 9dBm 111_1000 = 10dBm

4.11.59. MWTUNE_VALID3 (Address 0x0084)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	**Reserved.**
6:0	MW_TUN_RSSI_LOWTH<6:0>	RW	001_1111	**Set MW RSSI Low Threshold for Valid Channel Indicator.** 000_0000 = -110dBm 000_0001 = -107dBm …… 111_0111 = 9dBm 111_1000 = 10dBm

4.11.60. SPARE2 (Address 0x0087)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	RW	00	**Reserved.**
5	SMUTE_GAIN_CTRL_EN	RW	0	**Softmute Gain Control by SMUTE_GAIN<7:0>:** 0 = Disable 1 = Enable
4:0	Reserved	RW	0_0000	**Reserved.**

4.11.61. FMCHAN0 (Address 0x0088)

Bit	Name	Access	Default Value	Functional Description
7	CHANGE_BAND	RW	0	**Change Band:** 0 = Keep current band. 1 = Change band. This bit will automatically clear 0 after band switching process.
6	AM_FM	RW	1	**AM/FM Mode Switching:** 0 = FM mode. 1 = AM mode.
5:4	Reserved	RW	00	**Reserved.**
3:0	FM_HIGH_CHAN<11:8>	RW	0110	**High edge frequency of FM band with 50KHz per LSB.** Frequency(KHz)=FM_HIGH_CHAN<11:0>*50KHz

4.11.62. FMCHAN1 (Address 0x0089)

Bit	Name	Access	Default Value	Functional Description
7:0	FM_HIGH_CHAN<7:0>	RW	1011_1000	**High edge frequency of FM band with 50KHz per LSB.** Frequency(KHz)=FM_HIGH_CHAN<11:0>*50KHz

4.11.63. AMCHAN0 (Address 0x008C)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	R	0	**Reserved.**
6:0	AM_HIGH_CHAN<14:8>	RW	000_0001	**High edge frequency of AM band with 50KHz per LSB.** Frequency(KHz) = AM_CHAN<14:0>*1KHz

4.11.64. AMCHAN1 (Address 0x008D)

Bit	Name	Access	Default Value	Functional Description
7:0	AM_HIGH_CHAN<7:0>	RW	1111_1000	**High edge frequency of AM band with 50KHz per LSB.** Frequency(KHz) = AM_CHAN<14:0>*1KHz

4.11.65. LOW_CHAN0 (Address 0x0098)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	R	0	Reserved.
6:0	LOW_CHAN<14:8>	RW	000_0001	Low edge frequency of MW band with 1KHz per LSB and default is 513KHz(0x0201). Low edge frequency of FM band with 50KHz per LSB. Low edge frequency of SW band with 1KHz per LSB.

4.11.66. LOW_CHAN1 (Address 0x0099)

Bit	Name	Access	Default Value	Functional Description
7:0	LOW_CHAN<7:0>	RW	0xF8	Low edge frequency of band with 1KHz per LSB and default is 513KHz(0x0201). Low edge frequency of FM band with 50KHz per LSB. Low edge frequency of SW band with 1KHz per LSB.

4.11.67. CHAN_NUM0 (Address 0x009A)

Bit	Name	Access	Default Value	Functional Description
7:4	Reserved	R	0000	**Reserved.**
3:0	CHAN_NUM<11:8>	RW	0000	Channel number of band and the channel number is CHAN_NUM<11:0> + 1. If CHAN_NUM<11:0> is set to 0, only one channel is defined.

4.11.68. CHAN_NUM1 (Address 0x009B)

Bit	Name	Access	Default Value	Functional Description
7:0	CHAN_NUM<7:0>	RW	0x86	Channel number of band and the channel number is CHAN_NUM<11:0> + 1. If CHAN_NUM<11:0> is set to 0, only one channel is defined.

4.11.69. GUARD2 (Address 0x00A0)

Bit	Name	Access	Default Value	Functional Description
7:0	CH_GUARD<7:0>	RW	0x17	Channel guard range in dial mode.

4.11.70. STATUS0 (Address 0x00DE)

Bit	Name	Access	Default Value	Functional Description
7:3	Reserved	RW	1101_0	**Reserved.**
2	VALID_TUNE	RW	0	**Valid Channel Indicator:** 0 = Invalid channel. 1 = Valid channel.
1	Reserved	R	1	**Reserved.**
0	ST_TURE	RW	0	**Stereo Signal Indicator:** 0 = Mono state 1 = Stereo state

4.11.71. STATUS4 (Address 0x00E2)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	R	0	**Reserved.**
5:0	FM_SNR<5:0>	R	000_0000	**Channel SNR Value in FM Mode:** 000000 = Minimum SNR …… 111111 = Maximum SNR

4.11.72. STATUS5 (Address 0x00E3)

Bit	Name	Access	Default Value	Functional Description
7:0	SMUTE_GAIN<7:0>	RW	0x00	**Softmute Gain.** 0x00 = Mute. 0x01~0x80 = $20\log\frac{\text{SMUTE\_GAIN<7:0>}}{128}$. 0x81~0xFF = Reserved.

4.11.73. STATUS6 (Address 0x00E4)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	R	0	**Reserved.**
6:0	RDCHAN<14:8>	RW	000_0110	**Current Channel Indicator:** **FM mode:** Frequency(KHz) = RDCHAN<14:0>*50KHz **AM mode:** Frequency(KHz) = RDCHAN<14:0>*1KHz

4.11.74. STATUS7 (Address 0x00E5)

Bit	Name	Access	Default Value	Functional Description
7:0	RDCHAN<7:0>	RW	0xB8	**Current Channel Indicator:** **FM mode:** Frequency(KHz) = RDCHAN<14:0>*50KHz **AM mode:** Frequency(KHz) = RDCHAN<14:0>*1KHz

4.11.75. STATUS8 (Address 0x00E6)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	R	0	**Reserved.**
6:0	FM_RSSI<6:0>	R	000_0000	**FM RSSI Value Indicator.** FM RSSI(dBm) = -110 + FM_RSSI<6:0> * 1dB

4.11.76. AFC_STATUS0 (Address 0x00E8)

Bit	Name	Access	Default Value	Functional Description
7:0	AM_CARRIER_OFST<7:0>	R	0x00	**AM Carrier Frequency Offset:** 0x80 = -128*128Hz 0x81 = -127*128Hz …… 0xFF = -1*128Hz 0x00 = 0 0x01 = 1*128Hz …… 0x7E=126*128Hz 0x7F = 127 *128Hz

4.11.77. AFC_STATUS1 (Address 0x00E9)

Bit	Name	Access	Default Value	Functional Description
7:0	FM_CARRIER_OFST<7:0>	R	0x00	**FM Carrier Frequency Offset:** 0x80 = -128*1024Hz 0x81 = -127*1024Hz …… 0xFF = -1*1024Hz 0x00 = 0Hz 0x01 = 1*1024Hz …… 0x7E=126*1024Hz 0x7F = 127 *1024Hz

4.11.78. AMSTATUS0 (Address 0x00EA)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	R	0	**Reserved.**
6:0	AM_RSSI<6:0>	R	000_0000	**AM RSSI Value Indicator.** AM RSSI(dBm) = -110 + AM_RSSI<6:0> * 1dB

4.11.79. AMSTATUS2 (Address 0x00EC)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	R	0	**Reserved.**
6:0	AM_SNR_MODE1<6:0>	R	000_0000	**AM Channel SNR Value (Mode 1):** 000000 = Minimum SNR …… 111111 = Maximum SNR

4.11.80. AMSTATUS3 (Address 0x00ED)

Bit	Name	Access	Default Value	Functional Description

Bit	Name	Access	Default Value	Functional Description
7	AM_CARRY_LOCK	R	0	**AM Carry Frequency Lock Flag:** 0 = Lock loses. 1 = Lock.
6:0	AM_SNR_MODE2<6:0>	R	000_0000	**AM Channel SNR value (Mode 2):** 000000 = Minimum SNR …… 111111 = Maximum SNR When AM_SNR_MODE_SEL=1/2/3, AM_SNR_MODE2 is valid.

4.11.81. SWTUNE_VALID0 (Address 0x00F0)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	**Reserved.**
6:0	SW_TUN_SNR_HITH<6:0>	RW	011_1010	**Set SW SNR High Threshold for Valid Channel Indicator.** 000_0000 = 0 000_0001 = 1 …… 111_1110 = 126 111_1111 = 127

4.11.82. SWTUNE_VALID1 (Address 0x00F1)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	**Reserved.**
6:0	SW_TUN_SNR_LOWTH<6:0>	RW	011_0101	**Set SW SNR Low Threshold for Valid Channel Indicator.** 000_0000 = 0 000_0001 = 1 …… 111_1110 = 126 111_1111 = 127

4.11.83. SWTUNE_VALID2 (Address 0x00F2)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	**Reserved.**
6:0	SW_TUN_RSSI_HITH<6:0>	RW	010_0100	**Set SW RSSI High Threshold for Valid Channel Indicator.** 000_0000 = -110dBm 000_0001 = -107dBm …… 111_0111 = 9dBm 111_1000 = 10dBm

4.11.84. SWTUNE_VALID3 (Address 0x00F3)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	**Reserved.**
6:0	SW_TUN_RSSI_LOWTH<6:0>	RW	001_1111	**Set SW RSSI Low Threshold for Valid Channel Indicator.** 000_0000 = -110dBm

Bit	Name	Access	Default Value	Functional Description
				000_0001 = -107dBm …… 111_0111 = 9dBm 111_1000 = 10dBm

4.11.85. SW_SOFTMUTE0 (Address 0X00F4)

Bit	Name	Access	Default Value	Functional Description
7	SW_DSMUTE	RW	0	**SW Softmute Disable:** 0 = SW softmute enable 1 = SW softmute disable
6:0	SW_SMUTE_START_SNR<6:0>	RW	011_0000	**The Starting Level of Attenuation According to SNR in SW Mode.** 000_0000 = 0 000_0001 = 1 …… 111_1110 = 126 111_1111 = 127

4.11.86. SW_SOFTMUTE1 (Address 0X00F5)

Bit	Name	Access	Default Value	Functional Description
7	Reserved	RW	0	**Reserved.**
6:0	SW_SMUTE_START_RSSI<6:0>	RW	001_0111	**The Starting Level of Attenuation According to RSSI in SW Mode.** 000_0000 = -110dBm 000_0001 = -107dBm …… 111_0111 = 9dBm 111_1000 = 10dBm

4.11.87. SW_SOFTMUTE2 (Address 0X00F6)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	RW	01	**Reserved.**
5:3	SW_SMUTE_SLOPE_SNR<2:0>	RW	00_0	**The Slope of Attenuation According to SNR in SW Mode:** 000 = 4 001 = 3 010 = 2 011 = 1 100 = 1/2 101 = 1/3 110 = 1/4 111 = 0
2:0	SW_SMUTE_SLOPE_RSSI<2:0>	RW	100	**The Slope of Attenuation According to RSSI in SW Mode:** 000 = 4 001 = 3 010 = 2 011 = 1 100 = 1/2 101 = 1/3

Bit	Name	Access	Default Value	Functional Description
				110 = 1/4 111 = 0

4.11.88. SW_SOFTMUTE3 (Address 0x00F7)

Bit	Name	Access	Default Value	Functional Description
7:6	Reserved	RW	00	**Reserved.**
5:3	SW_SMUTE_MIN_GAIN<2:0>	RW	00_1	**The Total Attenuation of Volume Can Be Configured:** 000 = -9dB 001 = -12dB 010 = -15dB 011 = -18dB 100 = -21dB 101 = -24dB 110 = -27dB 111 = -30dB
2:0	Reserved	RW	011	**Reserved.**

5. Typical application circuits

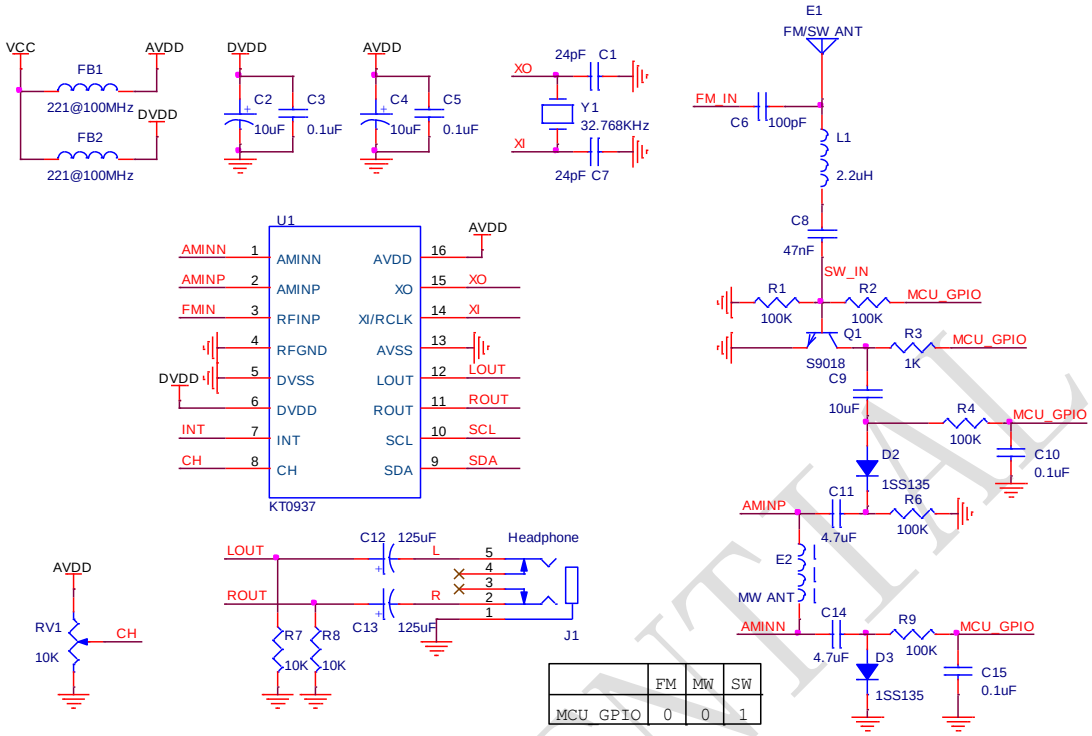
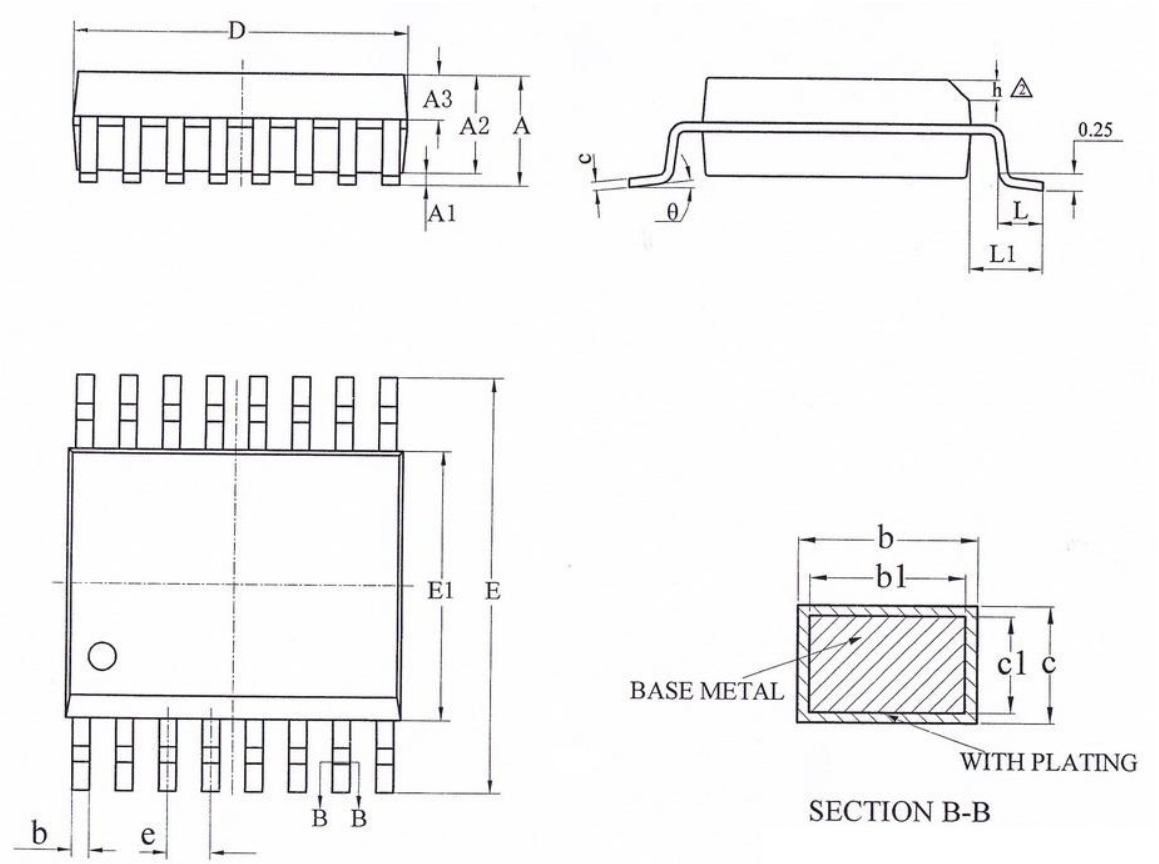


Figure 13: Typical application circuits

Components	Description	Value/Suppliers
C1,C7	Crystal load capacitor	24pF
C2,C4	Supply decoupling capacitor	10uF
C3,C5,C10,C15	Supply decoupling capacitor	0.1uF
C6	AC coupling capacitor	100pF
C8	Capacitor	47nF
C9	AC coupling capacitor	10uF
C11,C14	AC coupling capacitor	4.7uF
C12,C13	AC coupling capacitor	125uF
D1	ST indicator	LED
D2,D3	Diode	1SS135
E1	FM/SW antenna	
E2	MW ferrite antenna	420uH
FB1,FB2	Ferrite bead	221@100MHz
J1	Headphone Jack	
L1	Inductor	2.2uH
R1,R2,R4,R6,R9	Resistor	100Kohm
R3,R5	Resistor	1Kohm
R7,R8	Resistor	10Kohm
U1	FM/MW/SW Receiver	KT0937-D8
Y1	Crystal	32.768KHz

6. Package Outline



Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.50	0.60	0.70
b	0.24	-	0.30
b1	0.23	0.254	0.28
c	0.20	-	0.25
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	-	4.00
e	0.635BSC		
h	0.25	-	0.50
L	0.50	0.65	0.80
L1	1.05BSC		
θ	0 °	-	8 °

7. Package Markings

Figure14: Top Markings

Mark Method	YAG Laser	
Line 1 Marking	Device ID	KT0937-D8
Line 2 Marking	LOT Number	GMS411.1.F8
Line 3 Marking	Year Work week Manufacturing code	16 11 B

8. Order Information

Part number	Description	Package	MOQ
KT0937-D8	3rd generation monolithic digital FM/MW/SW receiver	SSOP16L(0.635-D1.4), Pb free	2500 pcs

9. Revision History

V1.0 Firstly Released
V1.1 Modified section 4.8, section 4.9.6, **Table 11** and register bank.
V1.2 Modified register bank.
V2.0 Modified Audio Output Voltage and Audio Common Mode Voltage Range in **Table 4**.
Modified Audio Output Voltage in **Table 5**.
Modified Audio Output Voltage in **Table 6**.
Modified Figure 2, Figure 3, Figure4 and Figure 5.
Modified section 7 Package Markings.
Modified default value of registers 0x18, 0x2A, 0x2B, 0x38, 0x39, 0x4E, 0x51, 0x62, 0x69, 0x7E, 0x98, 0x99, 0x9B and 0xA0.
V2.1 Modified register bank.

District,

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