

# Ting's FPGA, HPC and Embedded Blog

Personal Projects

## Run Linux on Avnet Spartan-6 LX9 MicroBoard

AV-LX9 MicroBoard (<http://www.em.avnet.com/s6microboard>) is a new low cost Spartan-6 LX9 device based development kit from Avnet. XC6SLX9 ([http://www.wikifpga.com/index.php?title=Spartan-6\\_LX](http://www.wikifpga.com/index.php?title=Spartan-6_LX))

has 1,430 slices, or 5,720 LUTs, and 32 Block RAM. Rich features, such as 64MB DDR, 128Mb SPI Flash, 10/100 Ethernet PHY, USB-UART port, JTAG, LEDs, DIP switches and expansion ports, make the board an affordable and very useful experimental prototyping tool.

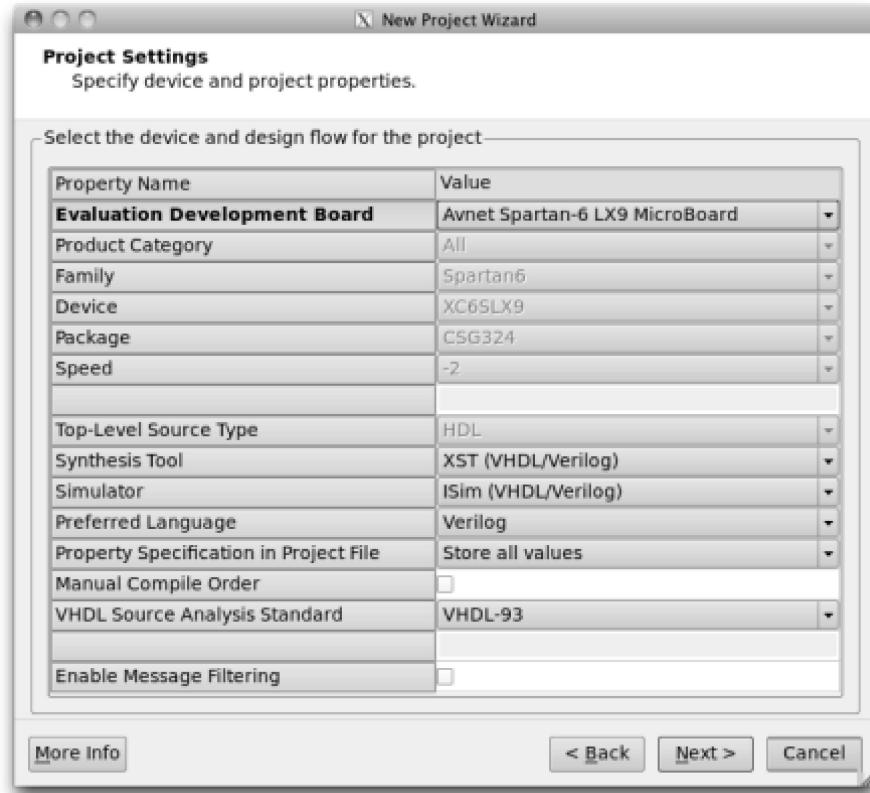
Thanks for Avnet's Frank for the LX9 MicroBoard, I was lucky to be able to try out the board early. My main goal was to get Petalinux running on this this USB-stick form factor board, with httpd server serving web pages and certain peripherals to demonstrate user defined functionalities. After many weekends' efforts, I was always couple hundreds of LUTs in short to fit designs of MicroBlaze with MMU into LX9 device, even after removing most peripherals, and enabling Legalizer placement algorithm.

Then Petalogix's John offered me a Linux BSP, used for hobby purpose. This convinced me the goal was possible, and kept me trying my own SOPC designs.

Finally I got it working before the recent Avnet LX9 MicroBoard SpeedWay Design Workshops. The keys were to remove non-essential MicroBlaze features and not use MDM's JTAG-based UART thus saves a AXI4-Lite connection. I am sure it can go further to use less resources and/or add more peripherals, but still has a stable Linux running on the board.

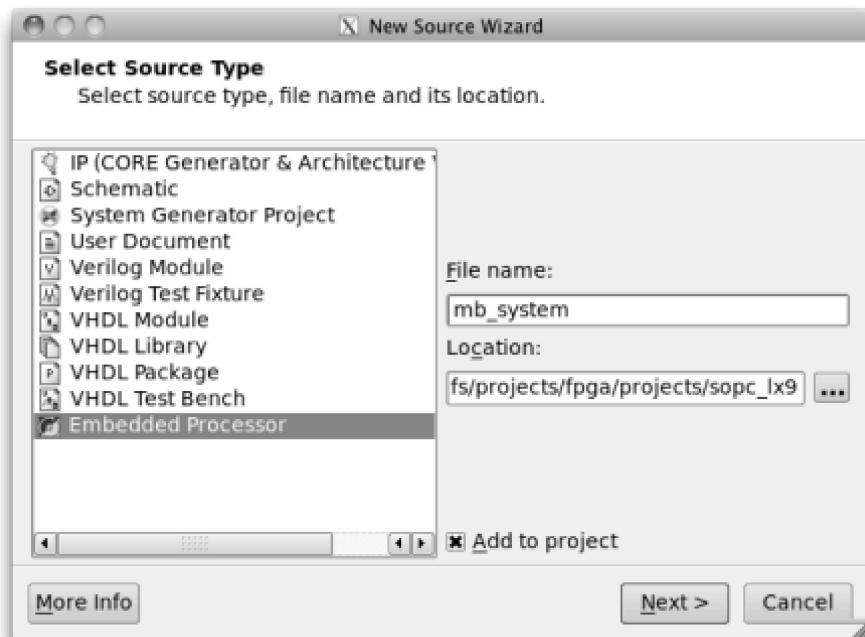
Here's how the working design was done in details. I am using PetaLinux SDK 2.1 and ISE 13.2 for 32 bit Linux, starting design flow from Project Navigator.

Create a new project based on Avnet LX9 MicroBoard XBD.



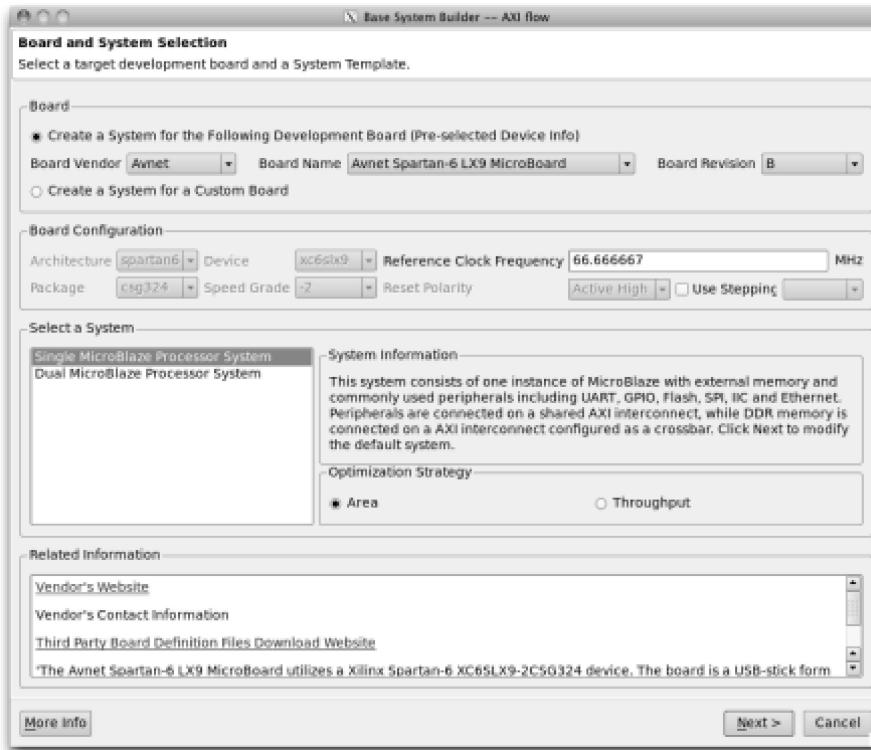
(<https://tingcao.files.wordpress.com/2011/09/ise.png>).  
Create New ISE Project

Select Embedded Processor for Source Type with New Source Wizard.



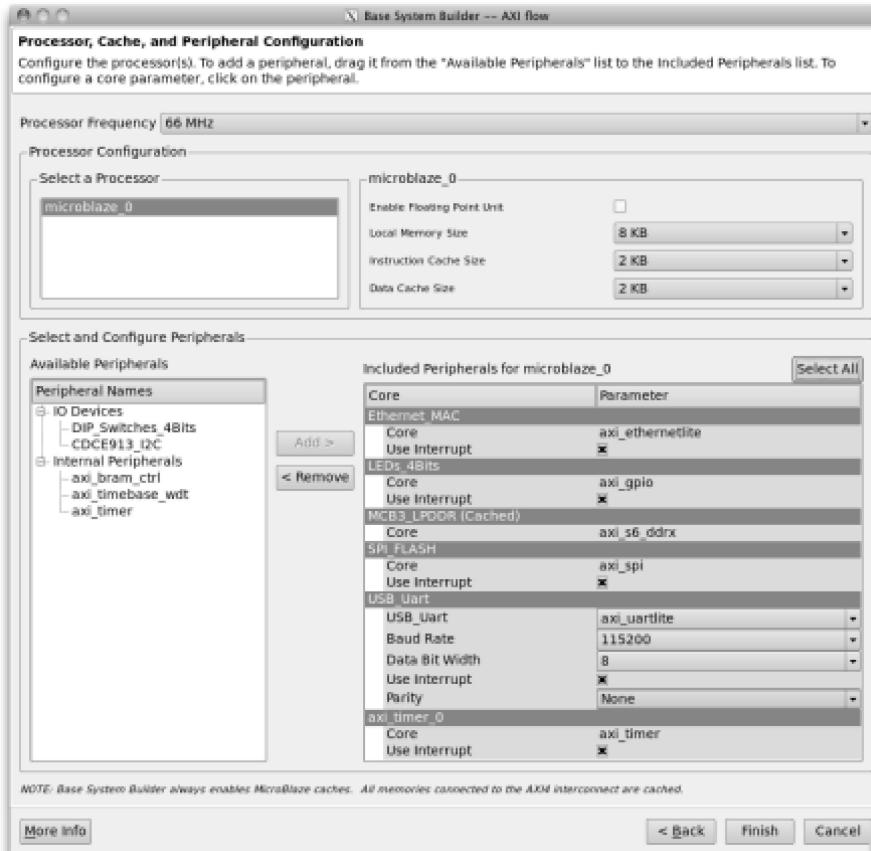
([https://tingcao.files.wordpress.com/2011/09/ise\\_newsource.png](https://tingcao.files.wordpress.com/2011/09/ise_newsource.png)).  
Select Source Type

When BSB starts, choose AXI flow.



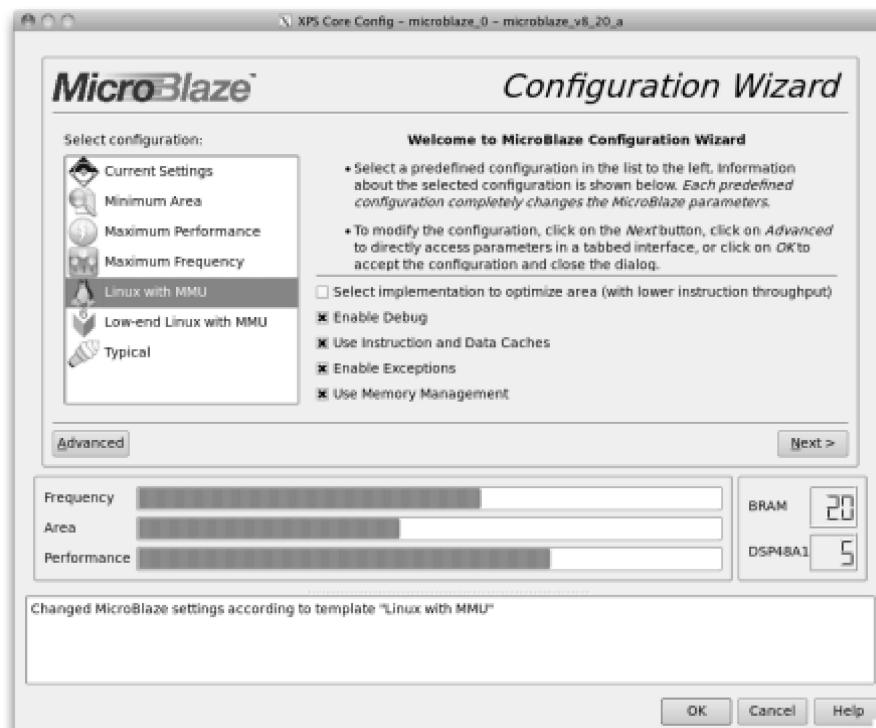
([https://tingcao.files.wordpress.com/2011/09/bsb\\_axi\\_flow.png](https://tingcao.files.wordpress.com/2011/09/bsb_axi_flow.png)).  
AXI Flow

And configure below processor, cache and peripherals.



([https://tingcao.files.wordpress.com/2011/09/bsb\\_axi\\_flow\\_processor\\_cache\\_peripheral\\_config.png](https://tingcao.files.wordpress.com/2011/09/bsb_axi_flow_processor_cache_peripheral_config.png)).  
Processor, Cache and Peripheral Configuration

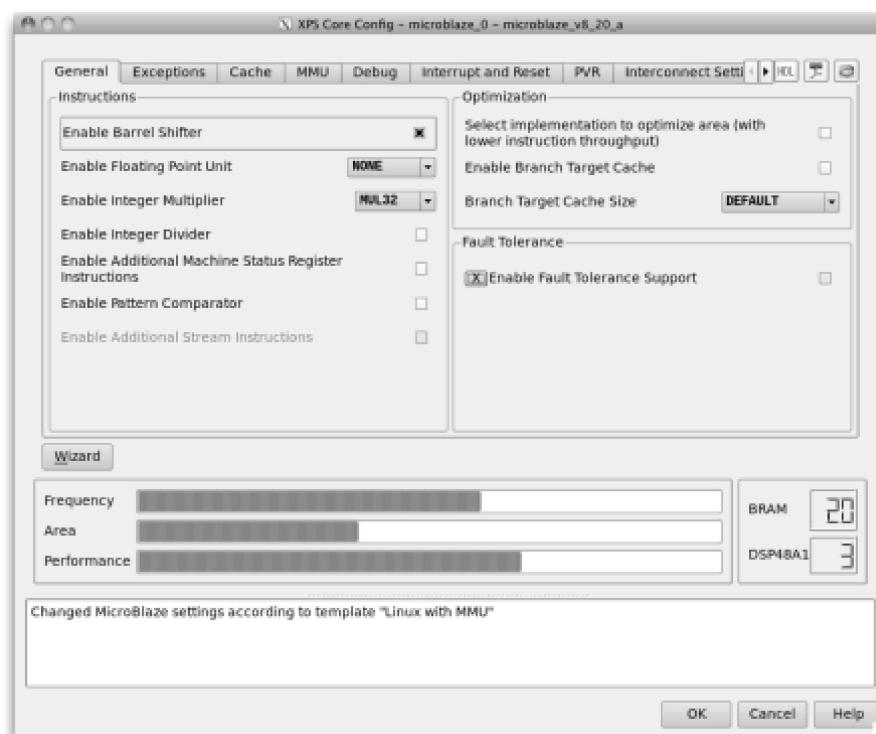
Once XPS project is created, configure MicroBlaze by double clicking the IP from System Assembly View.



([https://tingcao.files.wordpress.com/2011/09/mb\\_config.png](https://tingcao.files.wordpress.com/2011/09/mb_config.png)).

### MicroBlaze with MMU Configuration

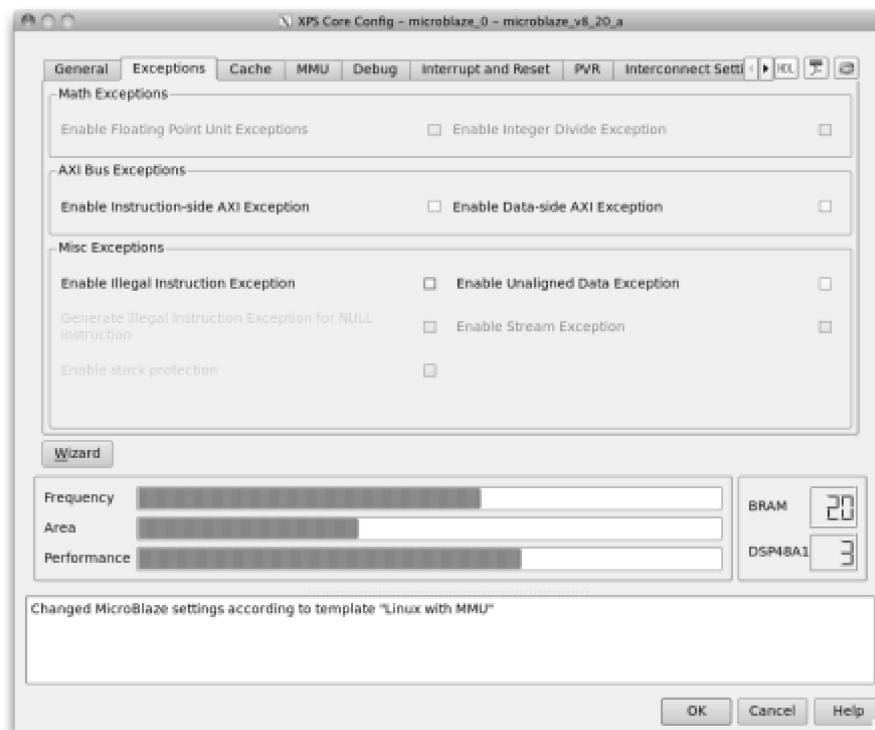
After select MMU configuration, click Advanced button to fine tune. The following setups can be done by going back and forth to enable then disable certain features. Here's General configuration.



([https://tingcao.files.wordpress.com/2011/09/mb\\_config\\_general2.png](https://tingcao.files.wordpress.com/2011/09/mb_config_general2.png)).

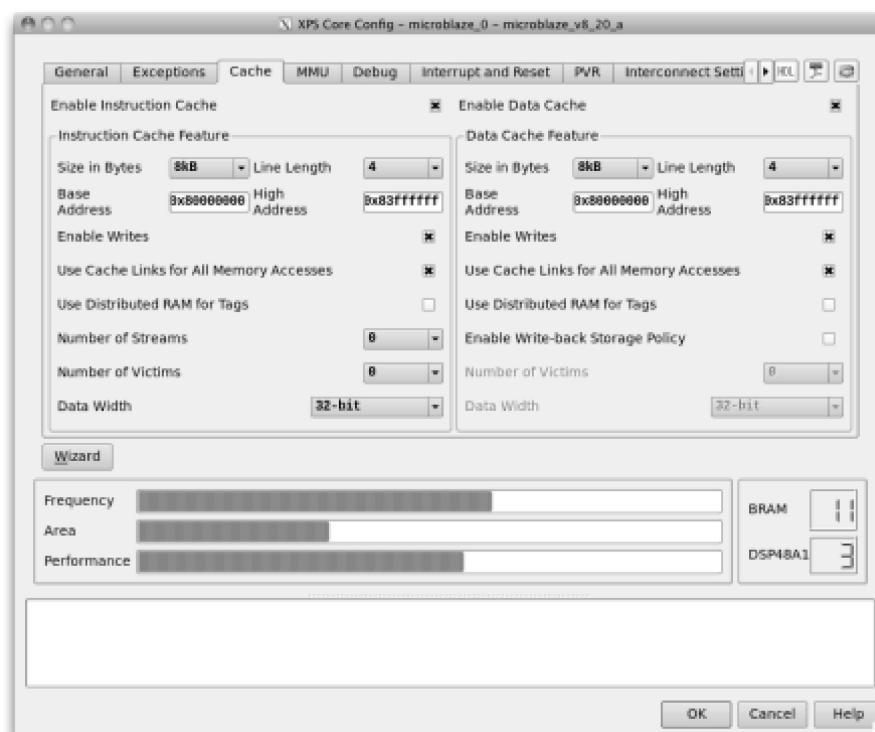
### MicroBlaze General Configuration

Disable all exceptions.



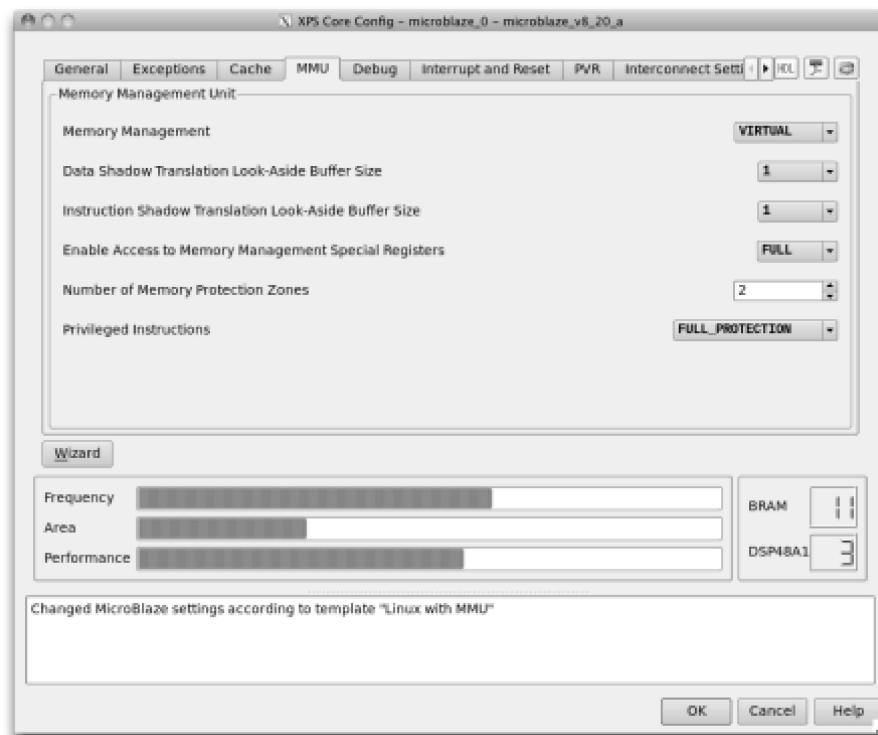
([https://tingcao.files.wordpress.com/2011/09/mb\\_config\\_exceptions2.png](https://tingcao.files.wordpress.com/2011/09/mb_config_exceptions2.png)).  
MicroBlaze Exception Configuration

Make sure instruction cache base address is setup properly. This is the location where Linux kernel starts.



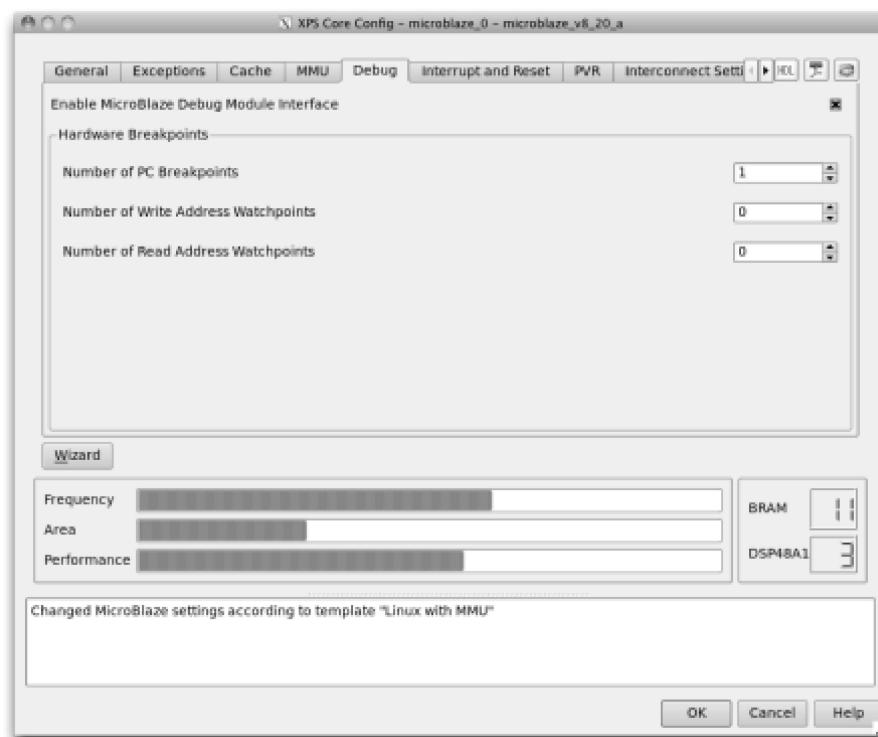
([https://tingcao.files.wordpress.com/2011/09/mb\\_config\\_cache.png](https://tingcao.files.wordpress.com/2011/09/mb_config_cache.png)).  
MicroBlaze Cache Configuration

Here's MMU setup.



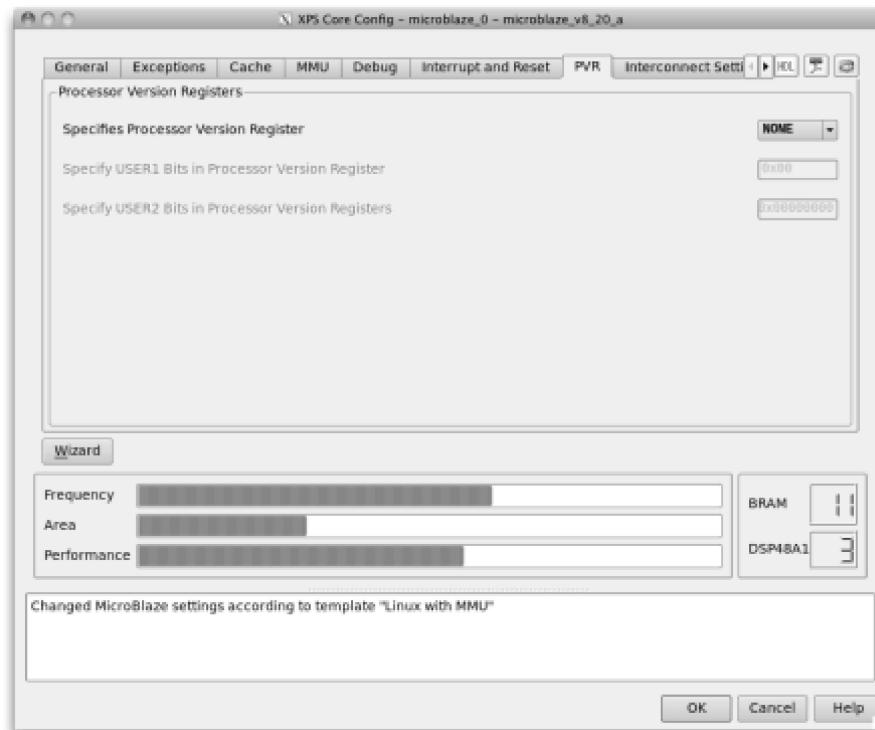
([https://tingcao.files.wordpress.com/2011/09/mb\\_config\\_mmu.png](https://tingcao.files.wordpress.com/2011/09/mb_config_mmu.png)).  
MicroBlaze MMU Configuration

Enable MDM so XMD can be used to debug.



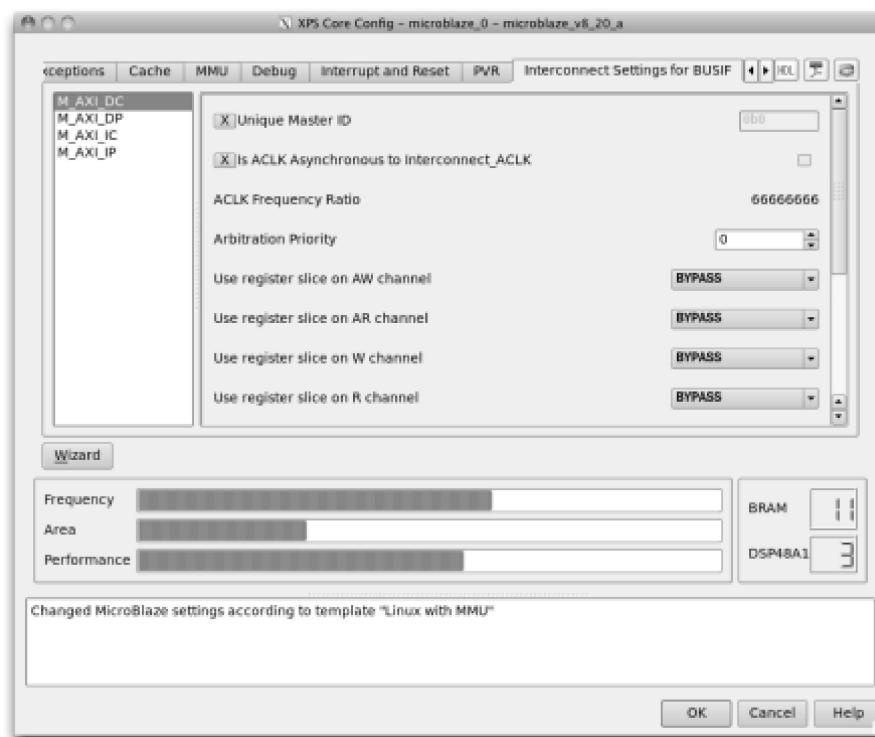
([https://tingcao.files.wordpress.com/2011/09/mb\\_config\\_debug.png](https://tingcao.files.wordpress.com/2011/09/mb_config_debug.png)).  
MicroBlaze Debug Configuration

No need for Processor Version Registers.



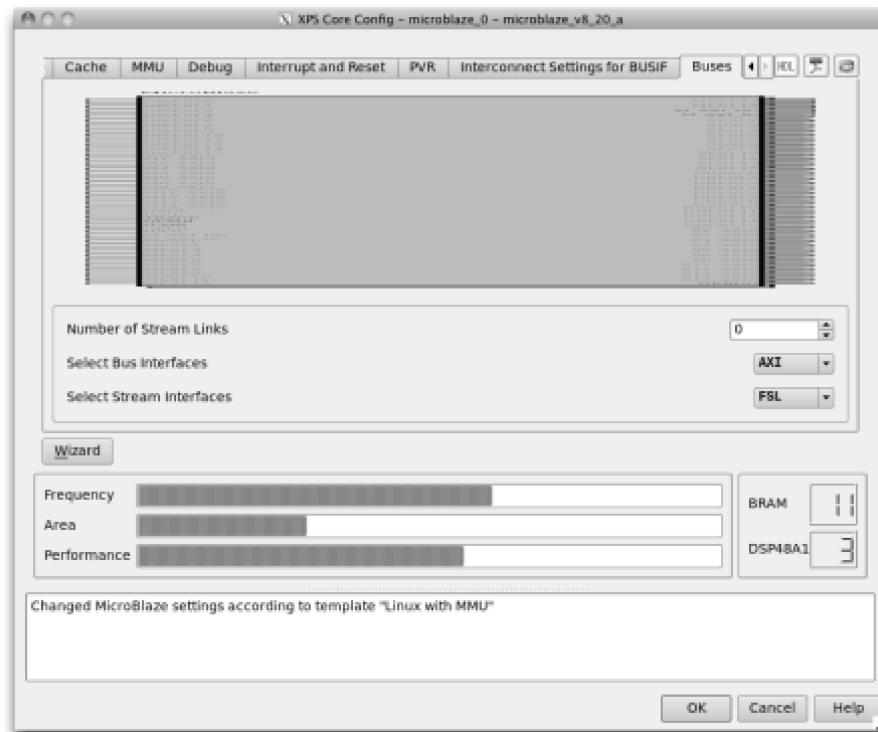
([https://tingcao.files.wordpress.com/2011/09/mb\\_config\\_pvr.png](https://tingcao.files.wordpress.com/2011/09/mb_config_pvr.png)).  
MicroBlaze PVR Configuration

Here's the Interconnection I used.



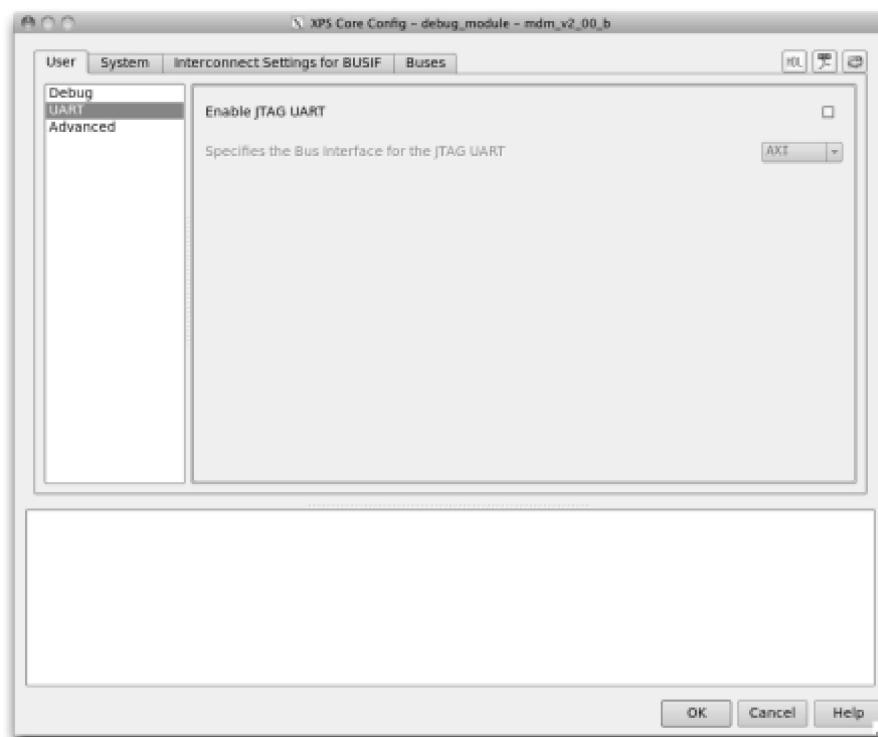
([https://tingcao.files.wordpress.com/2011/09/mb\\_config\\_interconnect.png](https://tingcao.files.wordpress.com/2011/09/mb_config_interconnect.png)).  
MicroBlaze Interconnect Configuration

Buses setup is the last MicroBlaze configuration.



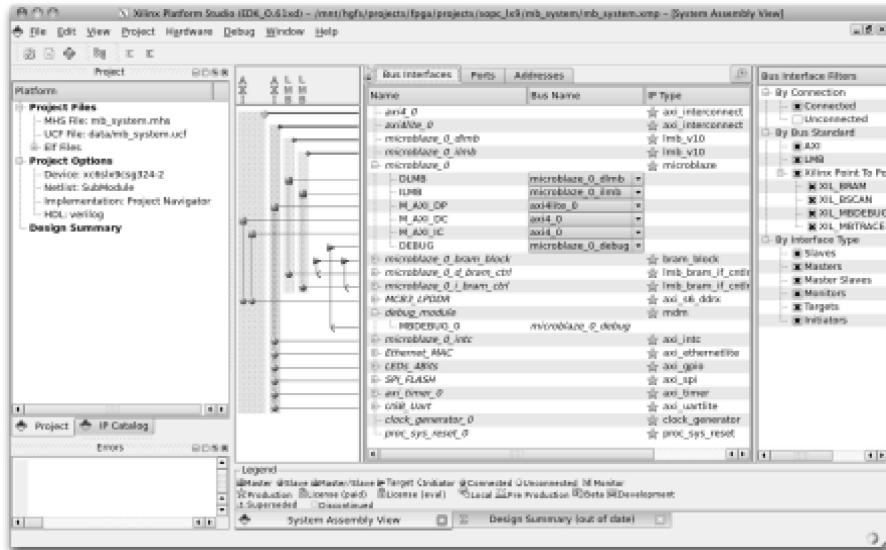
([https://tingcao.files.wordpress.com/2011/09/mb\\_config\\_buses.png](https://tingcao.files.wordpress.com/2011/09/mb_config_buses.png)).  
MicroBlaze Buses Configuration

Now configure MDM by disabling JTAG UART.



(<https://tingcao.files.wordpress.com/2011/09/mdm.png>).  
MDM Configuration

Here's XPS System Assembly View when design is done.



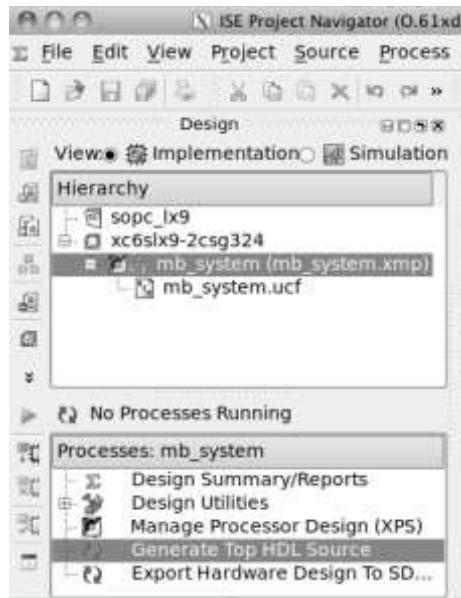
([https://tingcao.files.wordpress.com/2011/09/xps\\_system\\_assembly\\_view.png](https://tingcao.files.wordpress.com/2011/09/xps_system_assembly_view.png)).  
XPS System Assembly View

Return to Project Navigator when XPS is closed. Add constraints by Project > Add Copy of Source.



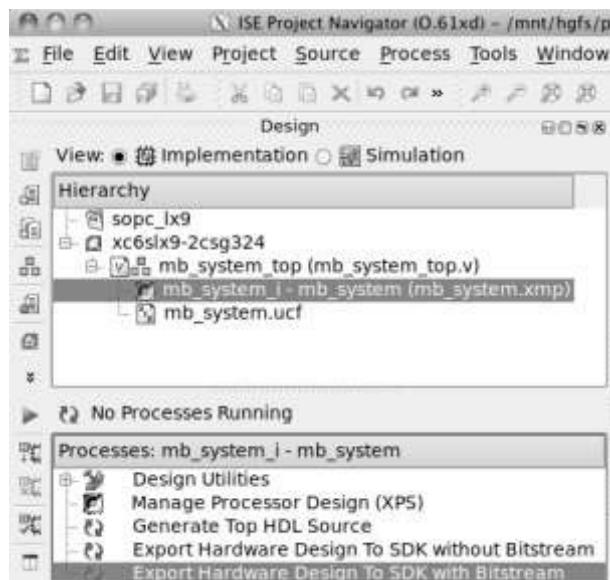
([https://tingcao.files.wordpress.com/2011/09/ise\\_add\\_copy\\_source.png](https://tingcao.files.wordpress.com/2011/09/ise_add_copy_source.png)).  
ISE Add Constraints

Double click Generate Top HDL Source to create HDL instantiation template for the MicroBlaze design.



([https://tingcao.files.wordpress.com/2011/09/ise\\_generate\\_top\\_hdl.png](https://tingcao.files.wordpress.com/2011/09/ise_generate_top_hdl.png)).  
ISE Generate Top HDL Source

Export hardware design to SDK.



([https://tingcao.files.wordpress.com/2011/09/ise\\_export\\_hardware.png](https://tingcao.files.wordpress.com/2011/09/ise_export_hardware.png)).  
ISE Export Hardware To SDK with Bitstream

If there are errors for placement and routing, try to set environment variable XIL\_PAR\_ENABLE\_LEGALIZER to 1, and rerun PAR.

Here's my XPS Synthesis Summary (estimated).

XPS Synthesis Summary (estimated values)					
Report	Generated	Flip Flops Used	LUTs Used	BRAMs Used	Errors
mb_system	Fri Sep 2 14:13:56 2011	5000	5753	17	0
clock generator 0 wrapper	Fri Sep 2 14:13:10 2011				0
ethernet mac wrapper	Fri Sep 2 02:48:08 2011	603	725	2	0
leds 4bits wrapper	Fri Sep 2 02:43:55 2011	72	85		0
mcb3 lpddr wrapper	Fri Sep 2 02:43:28 2011	322	544		0
spi flash wrapper	Fri Sep 2 02:42:55 2011	198	320		0
usb uart wrapper	Fri Sep 2 02:42:24 2011	86	106		0
axi4_0 wrapper	Fri Sep 2 02:41:59 2011	281	273		0
axi4lite_0 wrapper	Fri Sep 2 02:41:30 2011	123	234		0
axi timer 0 wrapper	Fri Sep 2 02:41:00 2011	219	274		0
debug module wrapper	Fri Sep 2 02:40:09 2011	89	62		0
microblaze_0 wrapper	Fri Sep 2 02:39:44 2011	2854	2957	11	0
microblaze_0 bram block wrapper	Fri Sep 2 02:36:23 2011			4	0
microblaze_0 d bram ctrl wrapper	Fri Sep 2 02:36:07 2011	2	6		0
microblaze_0 dlimb wrapper	Fri Sep 2 02:35:49 2011	1			0
microblaze_0 i bram ctrl wrapper	Fri Sep 2 02:35:33 2011	2	6		0
microblaze_0 ilimb wrapper	Fri Sep 2 02:35:14 2011	1			0
microblaze_0 intc wrapper	Fri Sep 2 02:34:57 2011	76	105		0
proc sys reset 0 wrapper	Fri Sep 2 02:34:30 2011	69	54		0

(<https://tingcao.files.wordpress.com/2011/09/synthesissummary.png>).  
XPS Synthesis Summary

Here's partial ISE Device Utilization Summary.

Device Utilization Summary				[+]
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	3,985	11,440	34%	
Number used as Flip Flops	3,976			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	9			
Number of Slice LUTs	4,781	5,720	83%	
Number used as logic	4,375	5,720	76%	
Number using O6 output only	3,380			
Number using O5 output only	92			
Number using O5 and O6	903			
Number used as ROM	0			
Number used as Memory	228	1,440	15%	
Number used as Dual Port RAM	96			
Number using O6 output only	4			
Number using O5 output only	1			
Number using O5 and O6	91			
Number used as Single Port RAM	4			
Number using O6 output only	4			
Number using O5 output only	0			
Number using O5 and O6	0			
Number used as Shift Register	128			
Number using O6 output only	43			
Number using O5 output only	1			
Number using O5 and O6	84			
Number used exclusively as route-thrus	178			
Number with same-slice register load	168			
Number with same-slice carry load	10			
Number with other load	0			
Number of occupied Slices	1,429	1,430	99%	
Number of LUT Flip Flop pairs used	5,091			
Number with an unused Flip Flop	1,555	5,091	30%	
Number with an unused LUT	310	5,091	6%	
Number of fully used LUT-FF pairs	3,226	5,091	63%	
Number of unique control sets	302			

(<https://tingcao.files.wordpress.com/2011/09/deviceutilizationsummary.png>).

### ISE Device Utilization Summary

Follow [PetaLinux](#) [SDK](#) [Board](#) [Bringup](#) [Guide](#) ([http://www.petalogix.com/resources/documentation/petalinux\\_sdk/PetaLinux-BoardBringup.pdf/view](http://www.petalogix.com/resources/documentation/petalinux_sdk/PetaLinux-BoardBringup.pdf/view)) to configure software settings of the hardware project and fs-boot.

I am using the following XMD commands to configure FPGA and download Linux image.

```
xmd.log.1:1 #  
1 XMD% fpga -f mb_system_top.bit  
2 Fpga Programming Progress ...1020.Done  
3 Successfully downloaded bit file.  
4  
5 JTAG chain configuration  
-----  
6 Device ID Code IR Length Part Name  
7 1 04001093 6 XC6SLX9  
8  
9 XMD% connect mb mdm -cable type xilinx_plugin modulename digilent_plugin  
10 MicroBlaze Processor Configuration :  
11 -----  
12 Version.....8.20.a  
13 Optimization.....Performance  
14 Interconnect.....AXI-LE  
15 MMU Type.....Full_MMU  
16 No of PC Breakpoints.....1  
17 No of Read Addr/Data Watchpoints...0  
18 No of Write Addr/Data Watchpoints..0  
19 Instruction Cache Support.....on  
20 Instruction Cache Base Address.....0x80000000  
21 Instruction Cache High Address.....0x83fffff  
22 Data Cache Support.....on  
23 Data Cache Base Address.....0x80000000  
24 Data Cache High Address.....0x83fffff  
25 Exceptions Support.....on  
26 FPU Support.....off  
27 Hard Divider Support.....off  
28 Hard Multiplier Support.....on - (Mul32)  
29 Barrel Shifter Support.....on  
30 MSR clr/set Instruction Support....off  
31 Compare Instruction Support.....off  
32 Data Cache Write-back Support.....off  
33 Fault Tolerance Support.....off  
34 Stack Protection Support.....off  
35  
36 Connected to "mb" target, id = 0  
37 Starting GDB server for "mb" target (id = 0) at TCP port no 1234  
38  
39 XMD% target 0  
40  
41 XMD% dow "image.elf"  
42 XMD% run  
43 Processor started. Type "stop" to stop processor  
44  
45  
46 RUNNING> 0  
47  
48
```

(<https://tingcao.files.wordpress.com/2011/09/xmd.png>)This is the PetaLinux login screen.

```

Welcome to
[Logo]
on socp_lx9

sopc_lx9 login: root
Password:
~ # uname -a
Linux socp_lx9 2.6.37.4-00531-g2db5587 #7 Fri Sep 2 17:41:55 MDT 2011 microblaze GNU/Linux
~ # dmesg |grep axi
XGpio: /axis@/gpio@00000000: registered
~ # ls -al /sys/devices/axi.0/
drwxr-xr-x  8 root    0          0 Jan  1 00:00 .
drwxr-xr-x  6 root    0          0 Jan  1 00:00 ..
drwxr-xr-x  2 root    0          0 Jan  1 00:01 40000000.gpio
drwxr-xr-x  3 root    0          0 Jan  1 00:01 40600000.serial
drwxr-xr-x  4 root    0          0 Jan  1 00:01 40a00000.spi
drwxr-xr-x  3 root    0          0 Jan  1 00:01 40e00000.ethernet
drwxr-xr-x  2 root    0          0 Jan  1 00:01 41200000.interrupt-controller
drwxr-xr-x  2 root    0          0 Jan  1 00:01 41c00000.system-timer
-r--r--r--  1 root    0        4096 Jan  1 00:01 modalias
lrwxrwxrwx  1 root    0          0 Jan  1 00:01 subsystem -> ../../bus/platform
-rw-r--r--  1 root    0        4096 Jan  1 00:01 uevent
~ # cat /proc/cpuinfo
CPU-Family: MicroBlaze
FPGA-Arch: spartan6
CPU-Ver: Unknown, little endian
CPU-MHz: 66.666666
BogoMips: 31.88
HW:
Shift: yes
MSR: no
PCMP: no
DIV: no
MMU: 3
MUL: vli
FPU: no
Exc:
Icache: 8kB    line length: 16B
Dcache: 8kB    line length: 16B
           write-through
HW-Debug: yes
PVR-USR1: 00
PVR-USR2: 00000000
Page size: 4096
~ #

```

(<https://tingcao.files.wordpress.com/2011/09/booted.png>).  
PetaLinux Login Screen

And PetaLinux Process Status.

```

~ # ps -ef
PID  USER      TIME  COMMAND
 1 root      0:02  init
 2 root      0:00  [kthreadd]
 3 root      0:00  [ksoftirqd/0]
 4 root      0:00  [kworker/0:0]
 5 root      0:00  [kworker/u0]
 6 root      0:00  [khelper]
 7 root      0:00  [sync_supers]
 8 root      0:00  [bdi-default]
 9 root      0:00  [kblockd]
10 root      0:00  [rpciod]
11 root      0:01  [kworker/0:1]
12 root      0:00  [kswapd0]
13 root      0:00  [fsnotify_mark]
14 root      0:00  [aio]
15 root      0:00  [infsiod]
16 root      0:00  [40a00000.spi]
17 root      0:00  [kworker/u1]
54 1         0:00  /bin/portmap
56 root      0:00  /home/httpd/cgi-bin/petalinux server 80
60 root      0:00  /bin/inetd /etc/inetd.conf
61 root      0:01  -sh
62 root      0:00  /bin/syslogd -n
63 root      0:00  /bin/flatifsd
110 root     0:00  ps -ef
~ # ls -al
drwxr-xr-x 12 root    0          0 Jan  1 00:01 .
drwxr-xr-x 12 root    0          0 Jan  1 00:01 ..
-rw-r--r--  1 root    0 747 Jan  1 00:37 .ash_history
drwxr-xr-x  2 root    0          0 Sep  2 2011 bin
drwxr-xr-x  7 root    0          0 Jan  1 00:01 dev
drwxr-xr-x  7 root    0          0 Sep  2 2011 etc
drwxr-xr-x  3 root    0          0 Sep  2 2011 home
lrwxrwxrwx  1 root    0          0 Sep  2 2011 init -> bin/init
drwxr-xr-x  4 root    0          0 Sep  2 2011 lib
lrwxrwxrwx  1 root    0 11 Sep  2 2011 linuxrc -> bin/busybox
drwxr-xr-x  2 root    0          0 Sep  2 2011 mnt
dr-xr-xr-x  33 root   0          0 Jan  1 00:00 proc
drwxr-xr-x 11 root   0          0 Jan  1 00:00 sys
lrwxrwxrwx  1 root    0          0 Sep  2 2011 tmp -> /var/tmp
drwxr-xr-x  4 root    0          0 Sep  2 2011 usr
drwxr-xr-x  6 root    0          0 Jan  1 00:00 var
~ #
CTRL-A Z for help |115200 B9N | NOR | Minicom 2.5 | VT102 | Offline

```

(<https://tingcao.files.wordpress.com/2011/09/booted1.png>).

Another fun experiment is to write code to turn on and off LEDs in certain patterns. 4 bit LED IP's address is 0x40000000, to turn on all LEDs, you can use:

*poke 0x40000000 0x0f*

Let me know if you're interested running my design, I have it [here](#) ([http://tingcao.s3.amazonaws.com/avnet\\_lx9\\_petalinux/avnet\\_lx9\\_microboard\\_petalinux.rar](http://tingcao.s3.amazonaws.com/avnet_lx9_petalinux/avnet_lx9_microboard_petalinux.rar)). If you like to try the commercial PetaLinux, please contact [Petalogix](#) (<http://www.petalogix.com/>).

This entry was posted on September 6, 2011 at 8:56 am and is filed under [Embedded](#), [FPGA](#), [LX9 MicroBoard](#), [MicroBlaze](#), [Petalinux](#), [SoPC](#), [Spartan-6](#), [Xilinx](#). You can follow any responses to this entry through the [RSS 2.0](#) feed. You can [leave a response](#), or [trackback](#) from your own site.

## 47 Responses to “Run Linux on Avnet Spartan-6 LX9 MicroBoard”

**servet ayok Says:**

[September 18, 2011 at 9:28 am](#) | [Reply](#)

Hello Mr CAO,

I would like to use microblaze and linux to interface a system using TCP/IP. Specifically, my system needs to give dynamic IP to the device connected to it, I mean it should act as a DHCP server.

Is your design suitable for this, can I directly use your bit file for my lx9 microboard?

You said "If you like to try the commercial PetaLinux, please contact Petalogix." is the commercial version free? what is the difference between commercial version and the one you used?

I would appreciate if you can help me.

Thanks for your help.

**tingcao Says:**

[September 18, 2011 at 4:07 pm](#) | [Reply](#)

When I did the design (just for LX9 MicroBoard), I used static IP address.

I'm sure you can enable DHCP server, either during kernel config, or add that functionality as a custom app.

I will check that out when I have time.

You're welcome to use my bit file.

If you want to build your own custom Linux kernel for Spartan-6 device MicroBlaze, you have two options:

1) Use free distribution:

Michal Simek

<http://www.monstr.eu/wiki/doku.php?id=start>

Xilinx

<http://xilinx.wikidot.com/microblaze-linux>

2) Use the commercial Petalinux, which is not cheap, but will get you to the market sooner.

This is what I'm using, but will try 1) later.

**servet ayok Says:**

[September 19, 2011 at 1:34 pm](#) | [Reply](#)

Hello Mr CAO,

Firstly I wanna thank you for your help. I used your .bit and .elf files and started linux on my microboard. But when I restart my board, I think I need to reload the image. I can convert bit file to mcs file and load it to flash so, FPGA can boot with microblaze. Is there a way that when FPGA boots, microblaze starts with Linux and I dont have to download linux again?

Waiting to hear from you,

Thanks.

**tingcao Says:**

September 19, 2011 at 1:45 pm | Reply

Actually that's what I'm going to do:

- 1) program SPI flash, so the board is configured when powered on.
- 2) add more peripherals, like DIP? Hope there is still resource left.
- 3) add more apps, to drive LEDs? Hope I can time to do it.

So expecting another post or two in coming weeks.

**servet ayok Says:**

September 19, 2011 at 1:59 pm | Reply

When we program SPI flash, board will be configured with just microblaze not linux, we will have to download linux again. Am I true?

Is not there a way to boot with microblaze and linux together so it is a stand alone module?

**tingcao Says:**

September 19, 2011 at 3:07 pm | Reply

No, the board can be configured to boot linux, w/o downloading anything.

**servet ayok Says:**

September 19, 2011 at 4:19 pm

Can you please direct me about how to do that?

**tingcao Says:**

September 20, 2011 at 3:18 pm

Following Xilinx Application Notes are useful:

xapp978 – FPGA Configuration from Flash PROMs on the Spartan-3E 1600E Board

xapp1146 – Embedded Platform Software and Hardware In-the-Field Upgrade Using Linux  
There are some more.

Also if you are a registered user for Avnet's website (Support Files & Downloads from <http://www.em.avnet.com/s6microboard>), you can get some LX9 MicroBoard tutorials, one is for SPI flash:

EDK – Creating a MicroBlaze SPI Flash Bootloader (Zip)

Solution: SPI Flash Bootloader (Zip)

**servet ayok Says:**

September 21, 2011 at 6:38 am

I read many papers including the ones you offered. As I understand I should load the mcs file to flash starting from 0x000000 address and load the image to flash starting from an address you defined while creating the boot loader. Because your bootloader says "No existing image in the flash".

If I am true, can you send me the address where image should start?

In some documents it says .elf can not be directly loaded, it should be converted to another format(some say .srec, some say .bin, some say .b).

Can you tell me which format your design requires?

**tingcao Says:**

September 28, 2011 at 6:27 am

I didn't design the bit/elf for splash programming, but now I'm still trying to do that.

Also there is a useful discussion about SPI programming. I tried, but didn't get to the end because I didn't setup tftp.

<http://community.em.avnet.com/t5/Spartan-6-LX9-MicroBoard/Remarks-on-AvtS6LX9MicroBoard-SW302-PetaLinux/td-p/3417>

**tingcao Says:**

October 13, 2011 at 1:27 am

I had another posting about FPGA/SPI Flash configuration. You can find the download at the end.

Here's the post link:

<https://tingcao.wordpress.com/2011/10/13/configure-fpgaspiflash-to-run-linux-on-lx9-microboard-part-2-quick-way/>

[Configure FPGA/SPI Flash to Run Linux on LX9 MicroBoard, Part 1 – Preparation](#) « Ting Cao's Blog Says:

October 17, 2011 at 3:13 am | [Reply](#)

[...] The FPGA design is done with ISE 13.2 based on AXI/Little Endian MicroBlaze 8.20a. The details were presented here at Run Linux on Avnet Spartan-6 LX9 MicroBoard. [...]

**Sven Andersson Says:**

October 18, 2011 at 4:40 pm | [Reply](#)

I have followed your instructions and generated the hardware design. My axi.4\_0\_wrapper is almost twice as big as yours (562f/f 375 LUTs). Did you change the configuration of the AXI4 wrapper?

Sven

**tingcao Says:**

October 18, 2011 at 9:18 pm | [Reply](#)

Hi Sven, I didn't change AXI configuration, and not sure why your AXI4 wrapper takes more resources.

I believe AXI4 is only used by external memory LPDDR.

I did change how to use AXI4 Lite for peripherals. In my design, I removed MDM's AXI4 Lite connection (JTAG/UART). That's one of the two keys to fit the design into LX9 device.

Here's my [MHS](#) if you're interested.

By the way, I read all (almost, 😊) of your blogs, way back several years ago. I'm still enjoying to read them. Great work indeed.

Ting

**Sven Andersson Says:**

October 20, 2011 at 9:54 am | [Reply](#)

Thanks for sending me the mhs file. I was using two different clocks (66MHz and 100MHz) in my system which added a lot of logic.

Sven

**fpga Says:**

October 18, 2011 at 6:22 pm | [Reply](#)

Any change to not use petalinux but the following : [http://xilinx.wikidot.com/ ???](http://xilinx.wikidot.com/)

**tingcao** Says:

October 18, 2011 at 6:44 pm | [Reply](#)

It is for sure possible. I will try it by using Xilinx' distribution, probably starting sometime next month

**fpga** Says:

November 4, 2011 at 4:59 pm

I can't wait for your guide for thisone!

**tingcao** Says:

November 4, 2011 at 5:54 pm

I didn't forget, but I'm sorry I will not have time this month. It will be my first thing (of fpga blog) to do to run Xilinx distribution Linux.

**Magali** Says:

October 20, 2011 at 2:20 pm | [Reply](#)

Good article. Its realy nice. More information help me.

**Mostofa Noor** Says:

October 24, 2011 at 11:24 pm | [Reply](#)

nice!

**cianuro** Says:

February 26, 2012 at 6:46 pm | [Reply](#)

Hi!

I'm trying to make this work without Petalinux and I'm facing a few problems. I think that I'm having some kind of trouble configuring the Linux kernel. Could you post your .config file along the sources of the XPS project? That'd be great!

Thank you!

**tingcao** Says:

February 27, 2012 at 12:53 am | [Reply](#)

I will get back to you, hopefully soon, once I get the files ready.

Thanks for your interest.

Here's the .config, I changed it to mb\_kernel.config

[http://tingcao.s3.amazonaws.com/avnet\\_lx9\\_petalinux\(mb\\_kernel.config](http://tingcao.s3.amazonaws.com/avnet_lx9_petalinux(mb_kernel.config)

Here's the complete EDK project (note I used ISE to create/manage EDK):

[http://tingcao.s3.amazonaws.com/avnet\\_lx9\\_petalinux\(mb\\_system.rar](http://tingcao.s3.amazonaws.com/avnet_lx9_petalinux(mb_system.rar)

Hope it helps. Please let me know when you get Linux built for MicroBlaze.  
I will start working on this soon.

**cianuro** Says:

February 28, 2012 at 4:39 pm

Thanks a lot. I will try to use buildroot to create the filesystem and will reach back when I got it. Maybe I'll even write a short tutorial.

Regards

**Kursad Gol Says:**

February 28, 2012 at 1:23 pm | Reply

Hi Mr. CAO,

Clearly i wanna ask you a pretty question? Please can you provide me your custom petalinux vhdl and c codes for educational using? Thanks in advance.

Best regards.

**tingcao Says:**

February 28, 2012 at 2:38 pm | Reply

Please check my other comment submitted on 02/27/2012.

The link to the complete EDK project was listed, plus Linux kernel config data.

**Kursad Gol Says:**

February 29, 2012 at 10:07 am

Hi Mr. CAO,

Isn't there any C code about the project application on your link as you mentioned [http://tingcao.s3.amazonaws.com/avnet\\_lx9\\_petalinux\(mb\\_system.rar](http://tingcao.s3.amazonaws.com/avnet_lx9_petalinux(mb_system.rar)? Am I right? Is there any necessity to C codes for upgrade from your petalinux project to my custom project?

I thank you many for your kindly regards.

**tingcao Says:**

March 1, 2012 at 2:03 am

You may need some C code in EDK project for driver support of custom IPs, and for bootloader.

But I'm not sure about the copy right issue of FS-Boot used in PetaLinux/MicroBlaze.

**Kursad Gol Says:**

March 1, 2012 at 6:57 am | Reply

Hi Mr. CAO,

I started to develop my project and i will feed you about my experiences back. But from now on there is a different problem from C codes issue. Daily problem is; i set environment variable XIL\_PAR\_ENABLE\_LEGALIZER to 1 but anything changes about 3 ERRORS:

ERROR:Place:543 – This design does not fit into the number of slices available in this device due to the complexity of  
the design and/or constraints.

ERROR:Place:120 – There were not enough sites to place all selected components.

Total REAL time to Placer completion: 3 hrs 42 mins 59 secs

Total CPU time to Placer completion: 3 hrs 42 mins 48 secs

ERROR:Pack:1654 – The timing-driven placement phase encountered an error.

Is there any knowledge regarding this issue?

Thank you again very much.

**Kursad Gol Says:**

March 1, 2012 at 7:07 am | Reply

And i forgot and also my PC uses Windows XP Pro service pack 3. My design suite is ISE 13.2. I try to configure and program my board using iMPACT with the on-board USB-JTAG circuitry.

**tingcao Says:**

March 1, 2012 at 4:08 pm | [Reply](#)

I would suggest review your design, to drop any IPs not actually needed. Use only one clock source, check Sven Andersson's comment on 2011/10/20.

Make sure XIL\_PAR\_ENABLE\_LEGALIZER kicks in. If you set it up from a console, start EDK from that same console.

**Kursad Gol Says:**

March 4, 2012 at 12:07 pm

Hi Mr. CAO,

I solve the mapping anp placement prolem. But still i have a problem too. When I do "Export hardware design to SDK with bitstream" and after this i did "Program FPGA" on SDK v13.2 I have my\_project.bit files 333 KB and microblaze\_0.elf 1KB. I am sure i couldn't create the right download.bit file. Because these files are dummy files. What will be the problem?

Thank you very much indeed.

**Kursad Gol Says:**

March 4, 2012 at 12:12 pm | [Reply](#)

And also i have too many warnings on my generation bit file. ISE v13.2 Design Summary says that "No errors and 284 warnings" Is this can be the problem? My computer's Operating System is Windows XP Pro 2002 with Service Pack 3.

**tingcao Says:**

March 5, 2012 at 4:06 pm | [Reply](#)

I had tons of warnings too, but it turned to be fine.

**Kursad Gol Says:**

March 5, 2012 at 8:41 pm | [Reply](#)

With your experience, what am i doing wrong?

**Kursad Gol Says:**

March 5, 2012 at 8:45 pm | [Reply](#)

Could you please explain with snapshots the musts of creating bit file? Because your sopc\_lx9.mcs file is running and its capacity is 30 MByte? But mine is 333 KByte?

**tingcao Says:**

March 5, 2012 at 11:24 pm

The actual size is about 1/3 of that of mcs (in ascii encoding).

I have bootloader, Linux kernel and Linux apps built in, that's why it is about 11M.

**Kursad Gol Says:**

March 6, 2012 at 9:53 pm

Hi Mr. CAO,

Can the problem ocuured because of my computer's operating system Windows XP? At your petalinux project given as .mcs file write "Linux version 2.6.37.4-00532-gb3a5c37 (tcao@ubuntu) (gcc version 4.1.2) #8 Tue Oct 11 00:46:35 MDT 2011".

Thank you.

**tingcao Says:**

March 6, 2012 at 10:08 pm

On which OS (XP, Linux, etc) you run the design tool (ISE/EDK) does no matter. Make sure you include the bit stream, and your app (such as Linux), etc.

**Tom Rae Says:**

March 25, 2013 at 9:13 pm | [Reply](#)

Mr. Cao,

Are the pmod connectors wired up on your LX9 Petalinux build?

If so, how?

Thank You,

Tom

**tingcao Says:**

March 25, 2013 at 9:40 pm | [Reply](#)

Hi Tom, I didn't use pmod peripherals in my Petalinux build.

I have a camera board which takes 2 pmod connectors, will try it once I get a chance. Since the space is tight on LX9, I probably will do a camera pmod design, and with Xilinx kernel but not with Linux support.

**vysakhpillai Says:**

November 18, 2013 at 7:06 am | [Reply](#)

Reblogged this on [EmbeddedInn](#).

**MagicPhoton Says:**

December 27, 2013 at 1:44 pm | [Reply](#)

Hi Cao,

I know that you posted this blog a long time ago but I will be very grateful if you could try to help me.

I'm using ISE 13.2 on windows XP and BXD 13.2 for Avnet LX9 microboard. I followed all your steps until the Synthesis. I removed MDM's AXI4 Lite connection (JTAG/UART). I am using only 66 MHz clock but I don't know why my number of Slice LUTs is at 102% when in your design is amazingly at 84%.

I check your MHS file and I find a little difference I tried too to do the synthesis with your file and I had the same result. Any suggestion?

I couldn't find XIL\_PAR\_ENABLE\_LEGALIZER variable, in what file is placed? What does it mean with rerun PAR?

Congratulations for this blog and thank you very much for sharing your knowledge. Thanks in advance and best regards.

MagicPhoton

**Sven Andersson Says:**

January 8, 2014 at 11:44 am | [Reply](#)

Hi MagicPhoton,

I noticed the same thing when I moved from ISE 13.1 to ISE 13.2.

I think the reason is that Xilinx has updated some of its IP blocks which made them larger. I never manage to fit the design into the FPGA anymore.

Sven

**Salman Sheikh Says:**

February 12, 2014 at 1:52 am | [Reply](#)

Hello,

I am getting errors when setting the cache addresses like yours...these addresses seem to cover more than 8KB from 0x80000000 to 0x83fffff?

ERROR:EDK:3900 – issued from TCL procedure “check\_cache” line 44

microblaze\_0 (microblaze) – Cacheable segment size defined by C\_DCACHE\_BASEADDR = 0x08000000 and C\_DCACHE\_HIGHADDR = 0x83FFFFFF must be a power-of-two.

ERROR:EDK:3900 – issued from TCL procedure “check\_cache” line 44

microblaze\_0 (microblaze) – Cacheable segment size defined by C\_DCACHE\_BASEADDR = 0x08000000 and C\_DCACHE\_HIGHADDR = 0x83FFFFFF must be a power-of-two.

ERROR:EDK:3900 – issued from TCL procedure “check\_cache” line 44

microblaze\_0 (microblaze) – Cacheable segment size defined by C\_DCACHE\_BASEADDR = 0x08000000 and C\_DCACHE\_HIGHADDR = 0x83FFFFFF must be a power-of-two.

**Nilesh Says:**

January 2, 2016 at 4:50 am | [Reply](#)

I have deployed petalinux on microboard , now want to test did my user application work on Linux full flesh , which tool-chain i can use to compile my application c code to run on this petalinux ?

I have tried crosstool-ng.org

microblaze-xilinx-linux-gnu-  
microblazeel-xilinx-linux-gnu-  
microblaze-xilinx-elf

if any other tool-chain plz give me link.

**tingcao Says:**

January 2, 2016 at 5:35 am | [Reply](#)

The only option is microblaze-xilinx-linux-gnu (big endian and linux).

[Blog at WordPress.com.](#)  
[Entries \(RSS\)](#) and [Comments \(RSS\)](#).