

Design for Flying Probe Testing



DFT Seminar Series 2000

Experts In Limited Access Testing



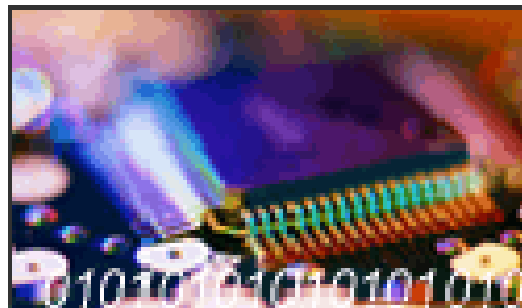
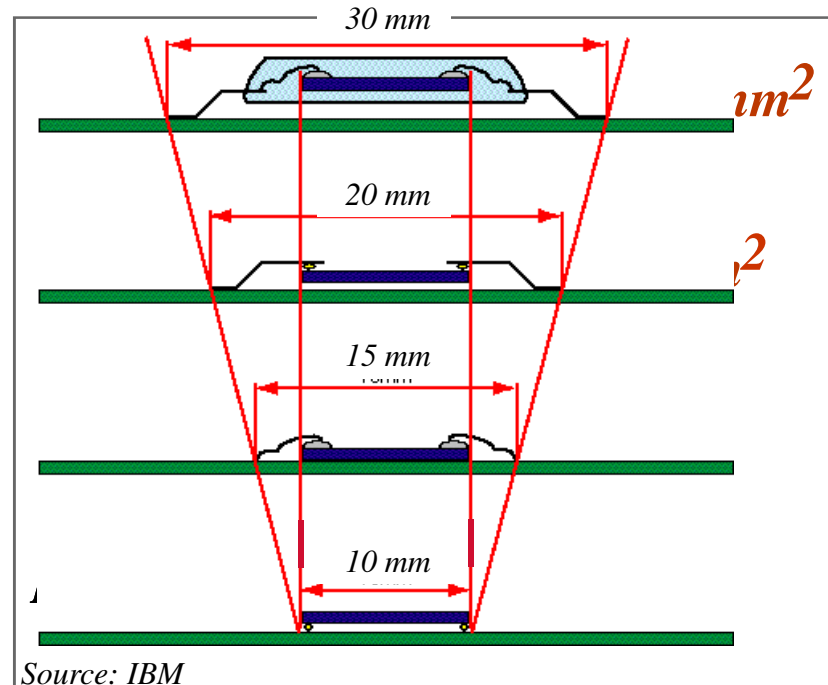
- *Introduction*
- *The DFT Concepts*
- *Mechanical DFT Issues*
- *Circuit DFT Issues*
- *Flying Probe Test Systems*
- *Discussions*

Glossary of Terms

- *DFT – Design for Testability*
- *DFM – Design for Manufacture*
- *DFx – Design for Excellence = DFT+DFM*
- *SMT – Surface Mount Technology*
- *SMD – Surface Mount Device*
- *JTAG – Joint Test Action Group*
- *TAP – Test Access Port*
- *ICT – In Circuit Test*
- *FPT – Flying Probe Test*
- *MDA – Manufacturing Defect Analyzer*
- *PCA – Loaded Printed Circuit Assembly*
- *PCB – Bare Printed Circuit Board*
- *UUT – Unit Under Test*

Why is DFT required in today's designs?

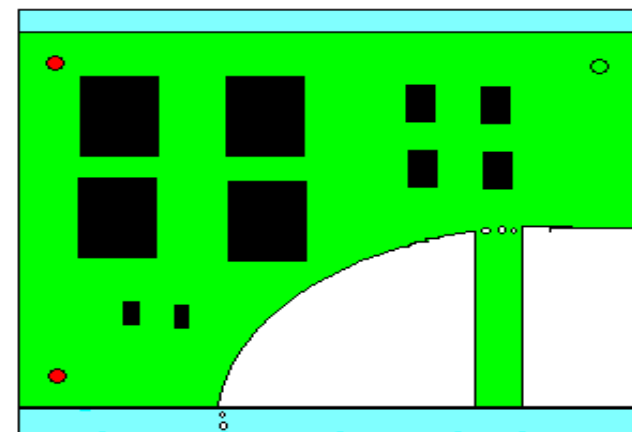
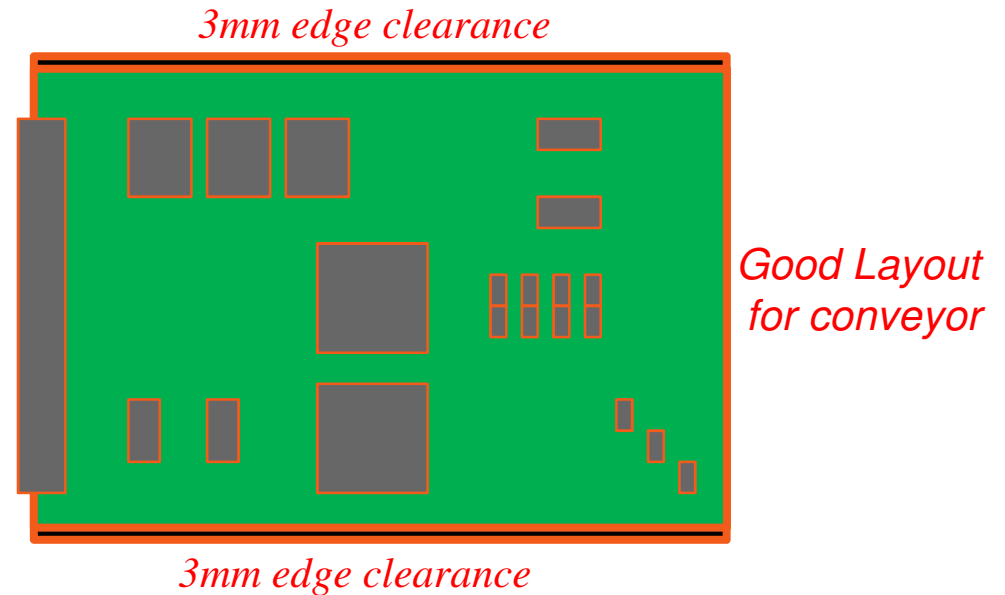
- Design Complexity Increasing
- Part Sizes Decreasing
- Part Pin Out Increasing
 - System On Chip
 - 1100+ Pin BGA
 - uBGA
 - Fan out issues
- Part Placement Density Increasing
- Complex Fault Isolation without DFT



- *PCA Handler Issues*
- *PCA Alignment System*
- *Tall Part Test Limitations*
- *No Fly Zones*
- *Test Accessibility Near Card Edges*
- *Types of Test Access Point*
- *Test Point Dimension Recommendations*

PCA Handler Issues – 3 mm rule

- *Edge Clearance on two Parallel sides of the UUT are required – 3 mm*
 - *Best along the longest edges of the UUT to prevent sag*
- *Predictable leading edge dimension required for board stopping position on systems with automatic conveyors*
- *In the case with odd shaped boards two solutions exist*
 - *Use break away rails that comply with the above*
 - *Use a custom or universal carrier to move the UUT into the machine.*

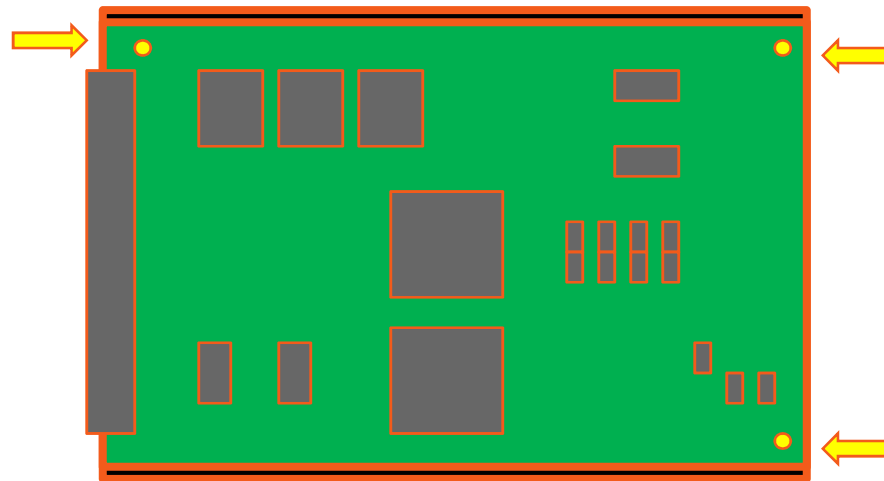


suitable for conveyor

PCA Alignment and Fiducials – 3 FID rule

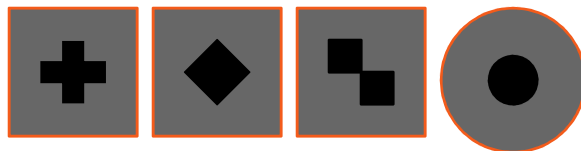
3 Board FID points are required on both top and bottom of the UUT

- *Placed near the perimeter of the UUT*
- *Must be free from solder after production*
- *Must not be identical from top to bottom*
- *Must not be near similar graphics, etches, silk screens.*
- *Must be clear from the 3 mm edge clearance*
- *Should be in the CAD as a part or easily identifiable entity.*

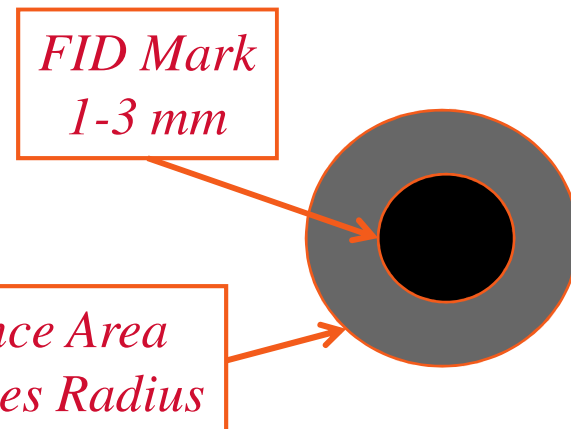


3 Fiducial points place properly

- According to the IPC-SMEMA Council Fiducial Locating marks should have the following characteristics:
 - Size: 1 mm to 3 mm in diameter (40 – 118 mils)
 - Clearance Area around the FID: - 1-2 times the radius of the size
- Some samples are below, most commonly used is the circle in circular clearance area.



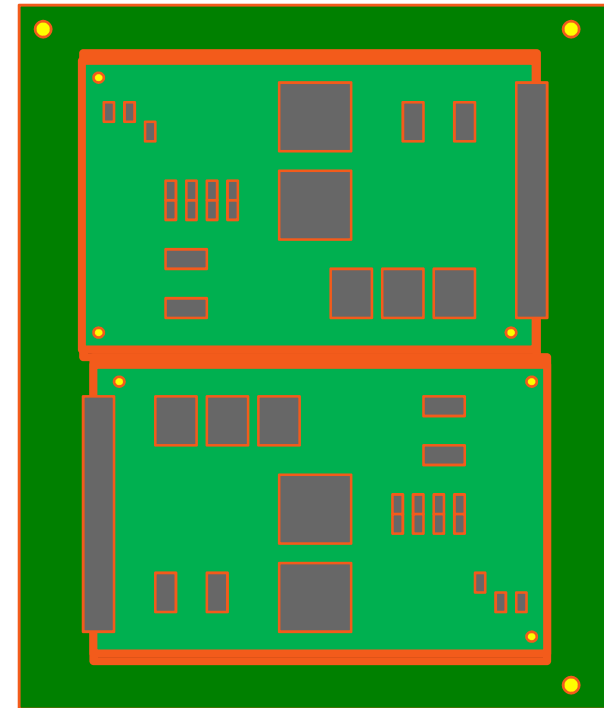
Sample FID Patterns



PCA Alignment of Panelized UUTs

*Panels should have panel FID
Points that follow single
board requirements*

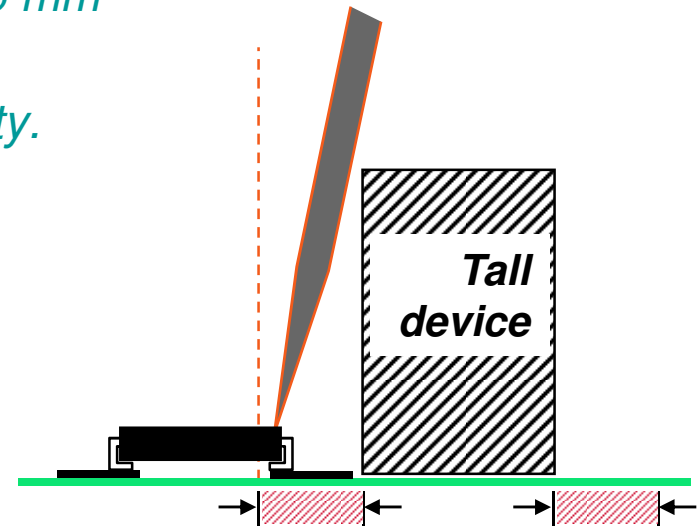
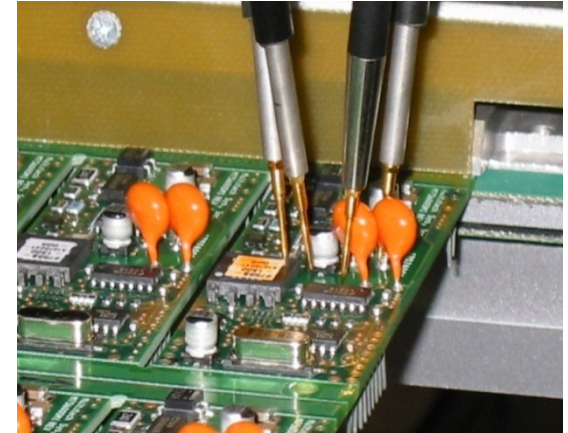
- *Clear from the edge, 3 top, three bottom, 1-3 mm is size and 1-3 mm clearance*
- *Must be in CAD or Mechanical Drawing and accurately referenced to individual UUT.*
- *This does not remove the requirement for Single Board FIDs, these are still required*



In the case when real FID points are not available most systems can capture another image and use it as a locating, but probing and placement accuracy goes down

No Fly Limits and Part Selection

- *As robotic systems, flying probe machines need to move over parts to go from place to place. Given that they are to contact the board under test and they are not infinitely high from the surface of the UUT some UUT mechanical limits will exist depending on the system you have, or plan to use.*
 - *Fly over heights range from 30 mm to 45 mm*
 - *Fly around heights range from 30 mm to 85mm in systems that have this capability.*
- *Fly Over or Fly Around issues can be minimized*
 - *Select low profile parts*
 - *Place tall parts after test*
 - *Place heat syncs after test*



Test Point Types:

- *Dedicated Test Points*
- *Via Holes as Test Points*
- *Through Hole Pins as Test Points*
- *Surface Mount Pads as Test Points*
- *Virtual Test Points*

Ideal DFT from an access point of view

- *Full access to every net on the board is ideal*
- *One or more access point per connected net*
- *One access point per unconnected net*

As named are entities in the design that are specifically meant for test access. Two main types exist:

- *Copper areas that are free from solder resistive mask and other impediments.*
 - *Should be as close as possible to the source end of the track as possible.*
- *Physical Parts that can be mounted/placed on the PCA*
 - *Ground/VCC Stake*
 - *Ground/VCC Clip*

Vias as Test Points

Four types of vias are common in PCB Layout:

■ *Testable Vias*



- *Standard Via – accessible to both top and bottom and may be connected to a mid plane layer*
 - *Annular ring aperture may differ from top to bottom indicating the preferred side to probe*
- *Blind Via – accessible to top OR bottom side and connects to a mid plane layer*

■ *Non-Accessible Vias*



- *Buried Via – not accessible to the top or bottom and only connects mid plane layers to one another.*
- *Tented or Masked Via – can belong to all of the above categories and has a solder resist mask or other coating that prevents it from allowing electrical contact.*

Soldered Through Holes

- *Connector, socket, resistor, etc device leads that are soldered through holes in PCB can be ideal test access locations.*
 - *Flying probe will typically require that the actual contact point be offset from the center of the leg as its position is not absolutely fixed in x, y or z planes.*
 - *Standard practice is to have the probe point offset to the ring where the leg is soldered*
 - *ICT/MDA will use the leg centers and a crown probe type*

Press Fit Through Hole

- *Usually connectors*
 - *Flying Probe must be targeting to the annular ring of these access points*
 - *care must be taken not to stick the probe into the connector hole and jam if from retraction for systems that do not have z-axis feedback.*

SMD/SMT Pads as Test Points

- *The accuracy and repeatability of certain FP machines will allow you to use these leads at viable test access locations.*
 - *0603 – easy for most machines*
 - *0402- easy for some machine*
 - *0201 – getting harder*
 - *01005 - difficult*
 - *IC Leads – depends on pitch*

- *PAD exposures need to be meeting the minimum targeting requirements of the system used.*
 - *RF and other special circuits are burying pads under the parts*
 - *cannot probe what cannot be seen*

Some SMD Packages – from Wikipedia

1x1 mm ■

0402 -

0603 -

1005 -

1608 -

2012 ■

3216 ■

3225 ■

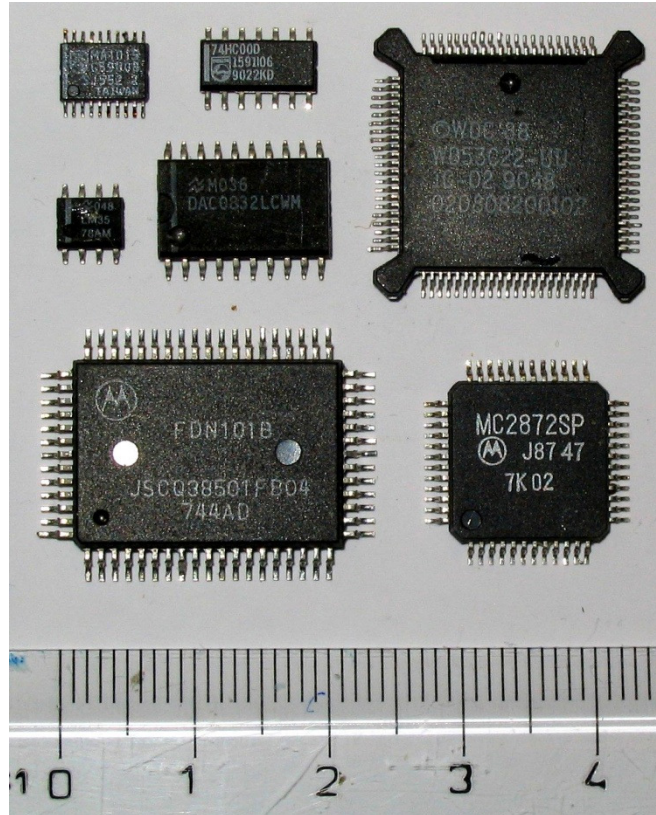
4516 ■

4532 ■

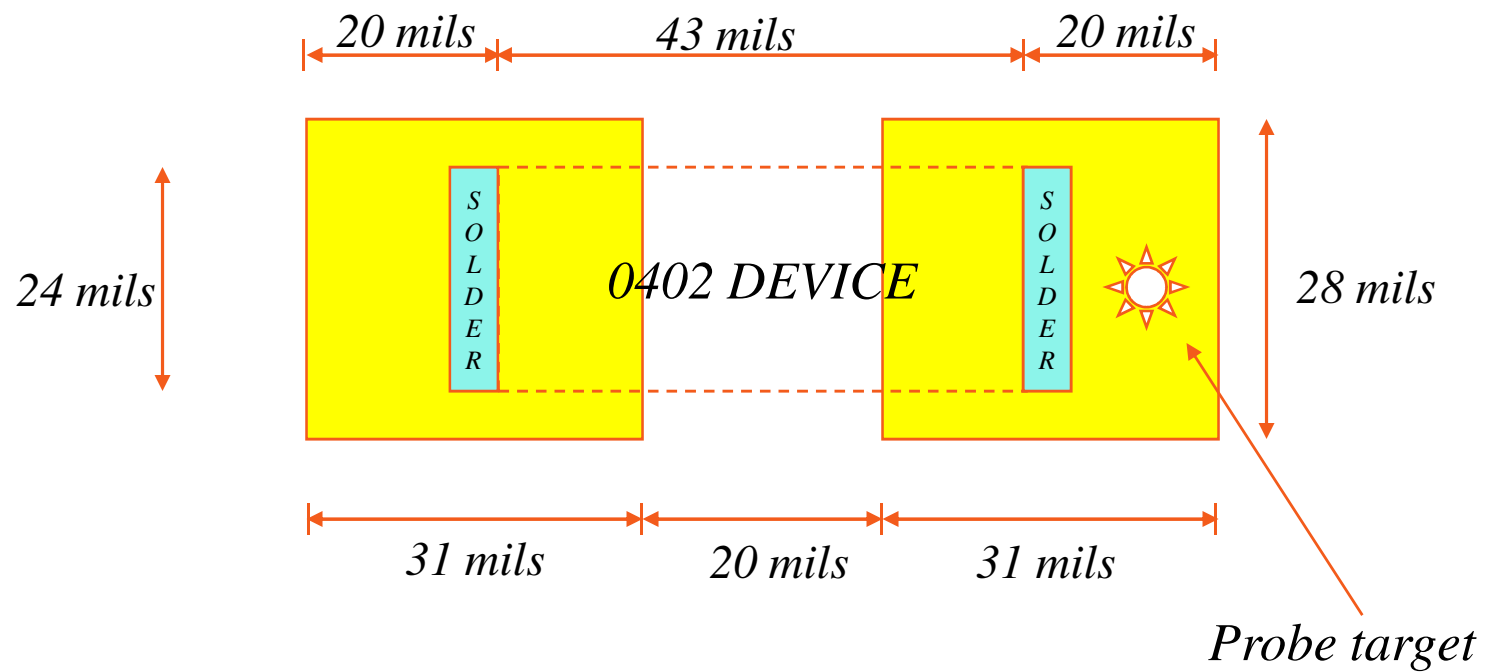
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1x1 cm

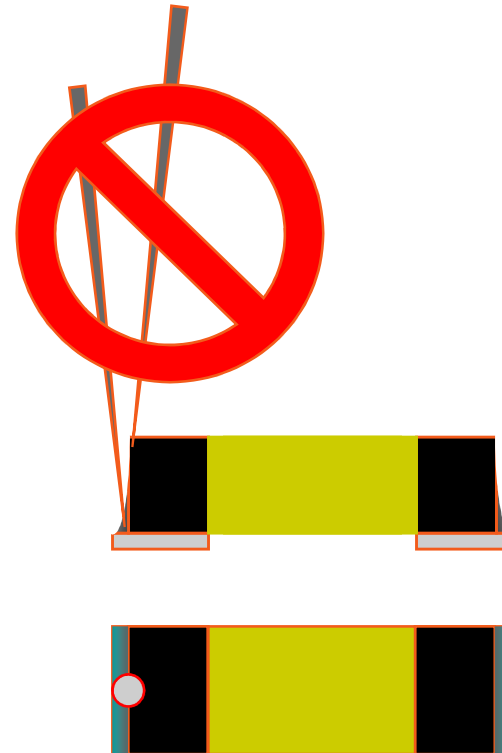
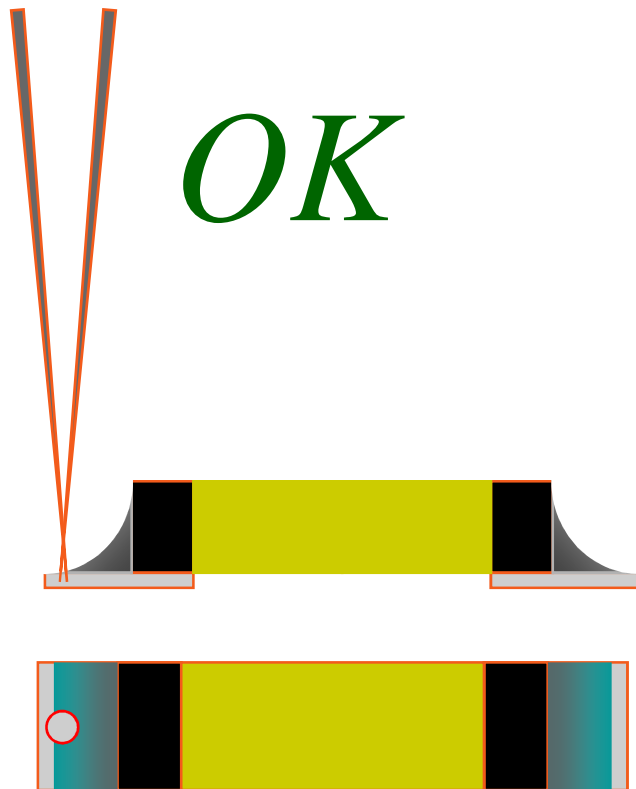


TYPICAL 0402 LAND PATTERN



drawing not to scale

- *Provided there is enough space*



Manufacturing Issues that Impact Test

- *Clean or No Clean Process*
 - *If the UUT has flux residue or other non-conductive substance this can cause:*
 - *False failures – of all test types*
 - *False passes – of shorts tests*
- *Lead Free or Leaded Solder*
 - *Lead free is harder and can provide worse contact over time with probe tip aging*
- *Through Hole Part Placement*
 - *Drift in hand placement can prevent use as viable test points location*
 - *Can damage the machine and parts if not consistently placed*
- *SMD Device Flow Variance*

DFT Recommendations

- *Ensure that output enable pins are not tied to ground or VCC directly.*
 - *Use pull-up/pull-down resistors that can be driven such that the device when powered will be tri-stated.*
- *Ensure that each device that has a disable pin is independently controllable*
 - *As an example, if you have a bank of buffers that are used in conjunction with a memory data bus, the buffers and memories will need to be controlled from two nets so that we can effectively and discretely test each of the individual parts.*
- *Ensure that all clock/oscillator/crystal circuits can be isolated or stopped from oscillating*
- *Ensure that watch-dog timers can be disabled so that they are not continually resetting the UUT during test vector execution*

Double-Sided Flying Prober Scorpion 8xx/9xx series

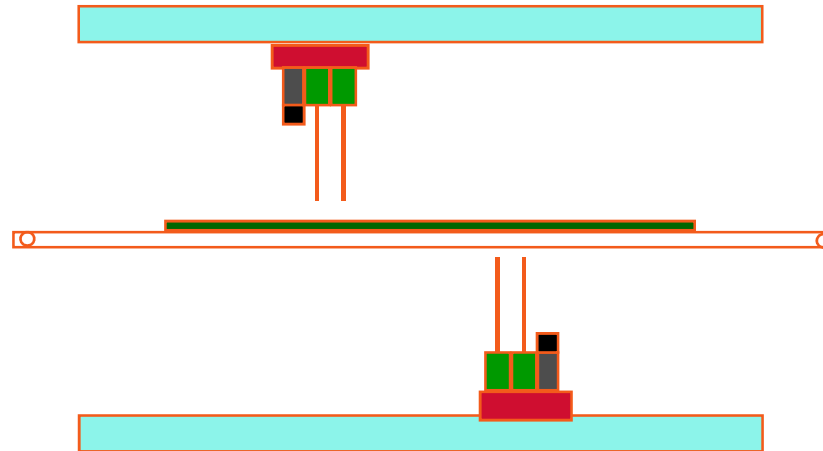


Single-Sided Flying Prober Sprint 4510

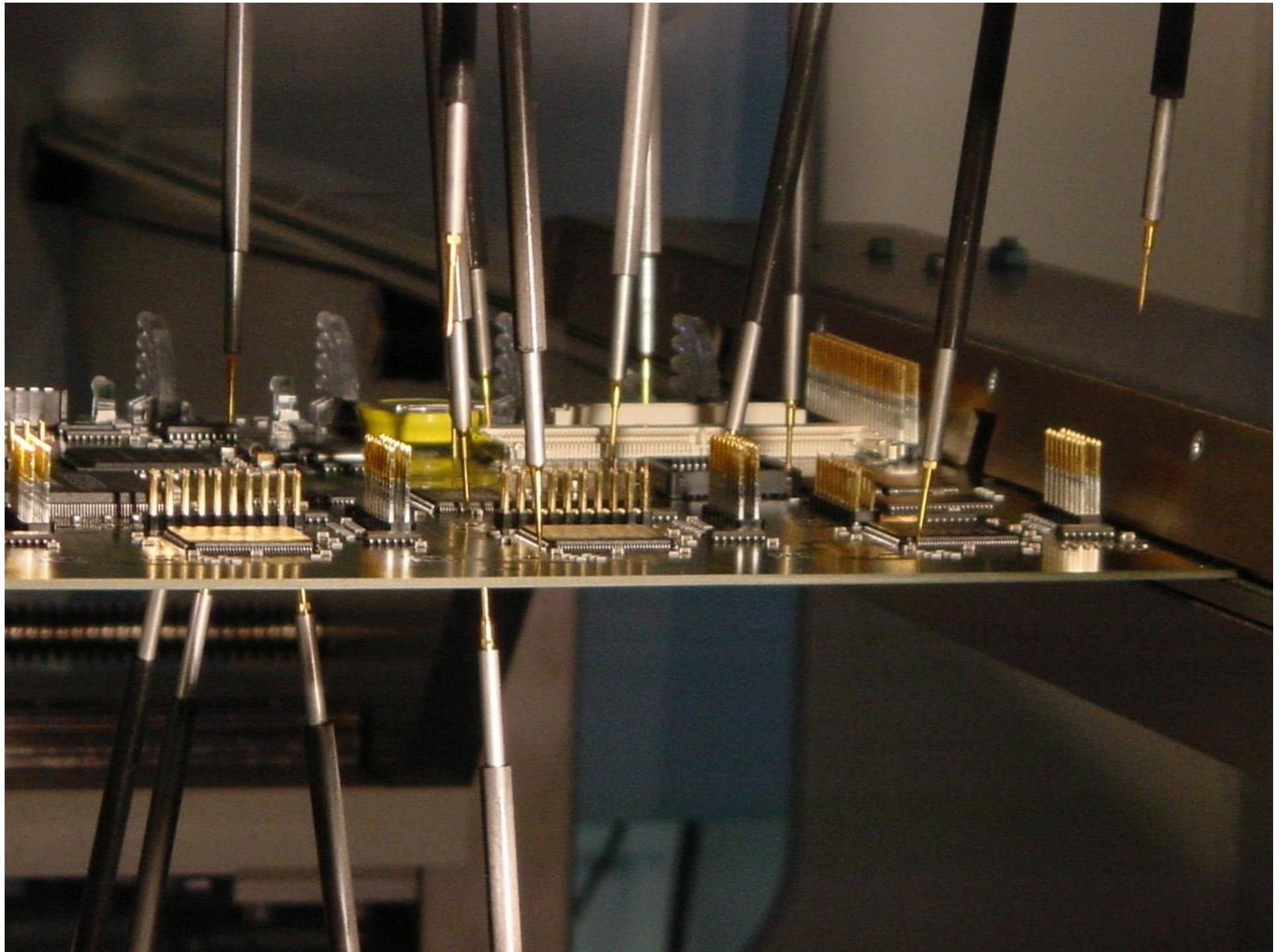
Benefits of using a Flying Probers

- Enables Prototype , NPI & low volume PCBs to be tested
- Test PCBs with minimal NRE
- Greater Test Access with targets down to 4 mil (0.1 mm)
- Enables testing of PCBs without traditional ICT test pads
- Provide for greater test coverage with AOI capability
- Implement same day testing
- BOM verification

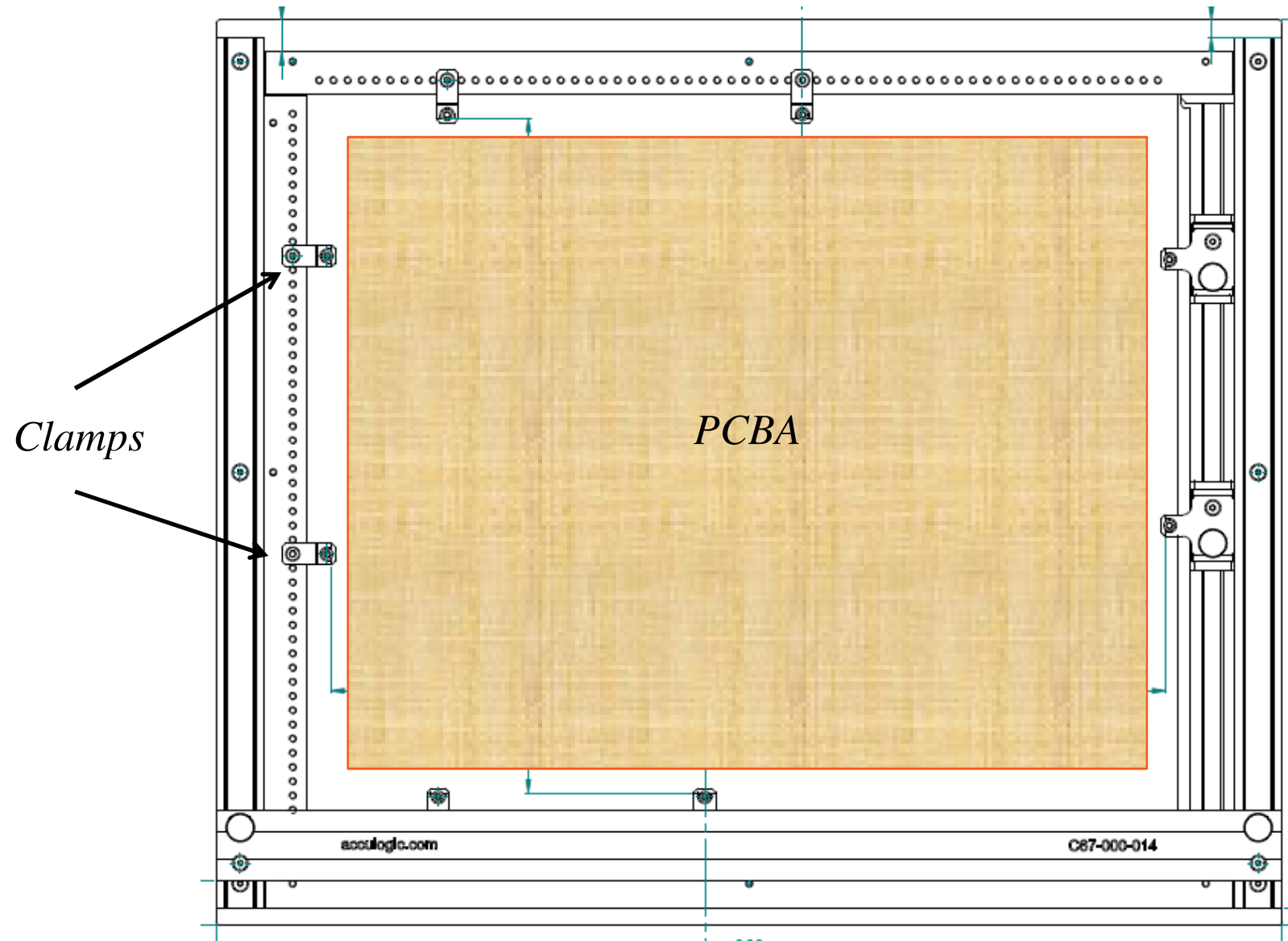
FLS Configuration flexibility



- **2 Stators - Topside and Bottom-side**
- **Up to 4 Shuttles per Stator**
- **3 Probe Slots per Shuttle**
- **Max Probes 11 Topside / 11 Bottom-side**
- **Total Maximum Probes 16**



PCBA Carrier



FLS Test Techniques

➤ **Passive Components:**

- Resistors (R)
- Capacitors (C)
- Inductors (L)

➤ **Discrete Semiconductor:**

- Diode
- Zener diode (to 100V)
- Transistors
- FET
- Thyristor
- Triac

➤ **Other Devices:**

- Bridges
- Switches
- Relay
- Optocoupler

➤ **Active analog and hybrid Components:**

- Comparator and Regulator
- Operational Amplifier

➤ **Other Tests:**

- Contact
- Shorts
- Power Up and Functional Test
- Flash and ISP
- Boundary Scan
- AOI on all shuttles

➤ **Vectorless Opens Test:**

- ChipScan
- C-Scan

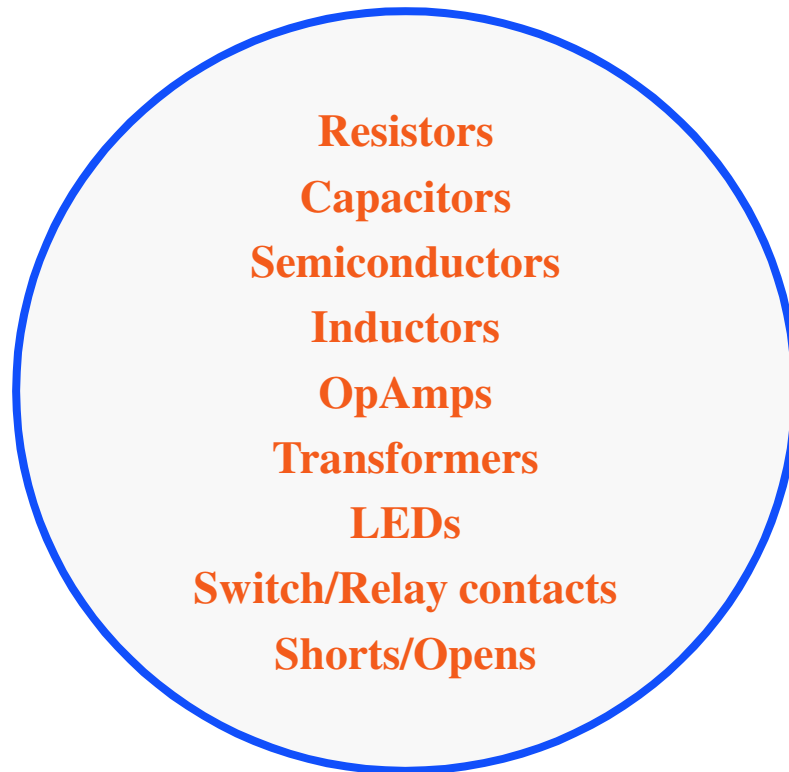
➤ **Network Analysis:**

- BodeScan

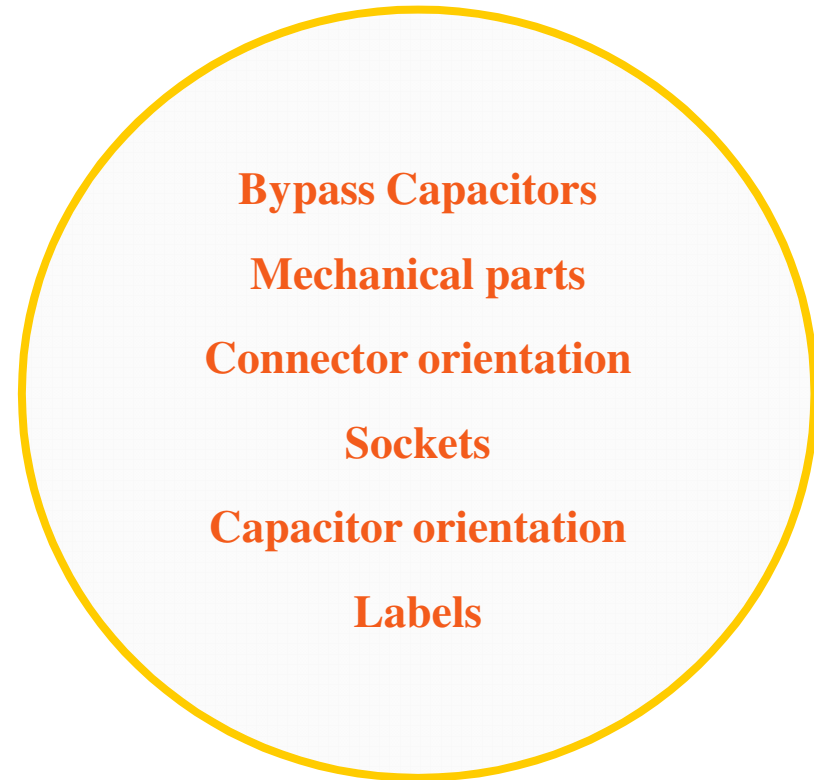
Complementary Vision Inspection



Electrical Test



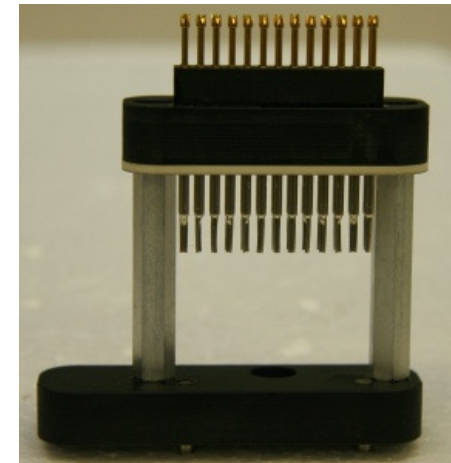
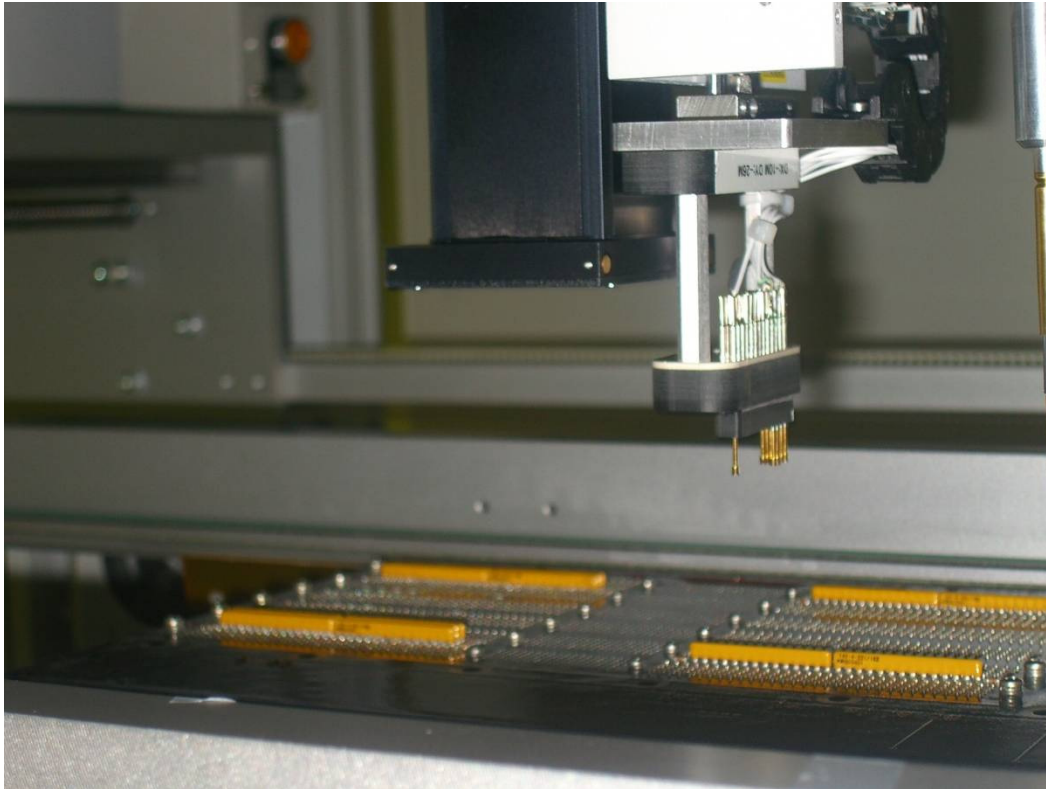
Vision Inspection



FLYING PROBER COMPARISON

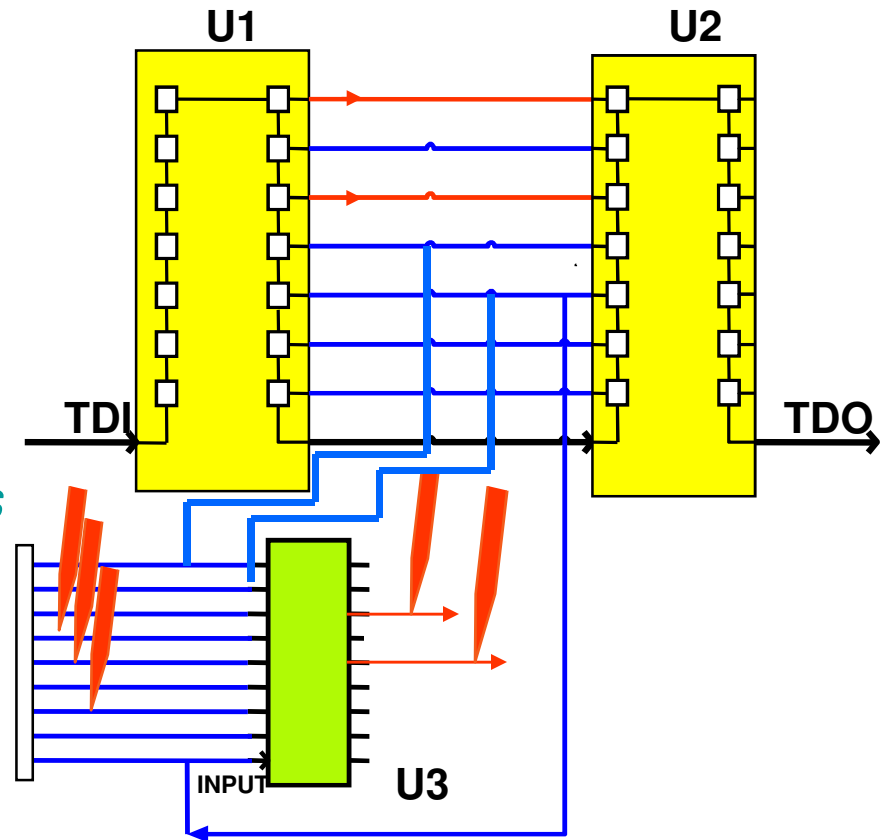
TEST TECHNIQUE	MDA FP-SS	PON FP-SS	MDA FP-DS	PON FP-DS	NOTES
Shorts					Nets on one side only not detectable
Opens					
Passives					
Bypass caps					Vision option on FP
Low value RLC					Dedicated hardware at DUT; kelvin tests
Actives					
Markings/Barcode					Vision inspection; barcode on one side only
Switches					Mechanical contact
Connectors					Probe connector pin tip
LED colors					
IC Opens					Vectorless testing (TestJet, FrameScan...)
Frequency Test					
Voltage Test					
IC Internal Logic					
IC Programming					Using B/S
Boundary Scan					FP needs B/S chain
Test Target					Largest target on either side for -2
Datalog					1 log for both sides
Test time					Two pass testing on 1 sided FP

Flying Fixture probing ...



Stages of Boundary Scan Test

- **TAPIT** – Test Access Port Integrity Test – Class 6
- **VIT**: Class 1, 2, 3, 4, Test
- **VIT+**: Boundary Scan and Non-Boundary Scan Device Test
 - Digital I/Os behind Flying Probes
 - Digital I/Os at Carrier I/O Interface
- **VCCT**: Cluster, Memory Test & Programming
- Each stage is generated in SVF Format and comes with Diagnostics
- Usually, test Coverage on UUT increases with each additional stage
- SVF is an Industry standard for generating serial and parallel patterns in ASCII format file



VIT+ makes testing U3 possible