LABORATORY FORMAT / MPROCESSOR THEORY (INTEL 8085)

1. Folder (name, TITLE, course, SECTION, dates)
2. INDEX. (label all pages)
3. OBJECTIVES
4. THEORY NEEDED
5. CALCULATED VALUES / SINGLE STEPPING
6. PROGRAM, FLOWCHART, MNEMONICS, O.C.
7. QUESTIONS / ANSWERS.
8. CONCLUSION / DISCUSSION
9. APPLICATIONS (OPTIONAL).
10. ATTACH LAB. MANUAL INSTRUCTIONS.

LATE PENALTIES:

1 week = -5pts
2 weeks = -10pts
3 weeks = -20pts
4 or more weeks = NOT ACCEPTED

COURSE TEXT

MOHAMED RAFIQUIZZMAN,
"Microcomputer Theory and Applications with the (INTEL 8085) SDK-85", WILEY

M.K.

Course No._____ Name_____

Section No._____

REPORT FOLDER

New York City College of Technology

OF THE CITY UNIVERSITY OF NEW YORK

Department of_____

Experiment No._____

Title_____

_____

FACULTY ONLY

Returned for corrections_____

Corrections due_____

Corrections handed in_____

Comments

Grade_____ Approved by_____

STUDENTS ONLY

Date experiment completed_____

Date due_____

Date handed in_____

Squad No._____

List Members

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Objective

- Get a handle for manipulating data using the SDK-85 (Student Development Kit)
- Use Appendix F (8085 Instruction Set), specifically the Arithmetic Group, to perform operations on the registers and memory locations of the SDK-85.

Theory

- The SDK-85 (Student Development Kit) is a single board microcomputer system kit using the 8085 processor. It is made by Intel and is now used to teach students about the concepts of microprocessors. Contains the following
    - **Microprocessor**
    - **Memory Element** – This describes both ROM (Read Only Memory) and RAM (Random Access Memory)
        - ROM (Read Only Memory) – Contains system boot up instructions
        - RAM (Random Access Memory) – Has Read/Write capabilities
    - **I/O Unit** – Handles input from user and provides output
- Microprocessors are computer processors that incorporate the functions of a central processing unit on a single integrated circuit (IC) or at most a few integrated circuits. They contain the following:
    - **Combinational logic Unit** – are logic circuits implemented by Boolean (logic gates) circuits, where the output is a pure function of the present input only. Think Half-Adders, Full-Adders, Encoders, and Decoders.
    - **Sequential logic Unit** – this is a type of logic circuit whose output depends on previous inputs as well as on the present inputs.
        - Contains Memory
        - Contains a clock

This lab focuses on **Appendix F (the 8085 Instruction Set)**, specifically the **Subroutines**. This is the set of assembly instructions that performs preset programs that's stored in ROM

Part A

Draw flow chart of the program that will display the course code EE 2262 on the address fields, using the following subroutines.

UPDAD (0363)
UPDAT (036E)
RDKBD (02E7)
DELAY (05F1)

[SP] ←20C2
A ← 62
DISPLAY'A'
|DE|←EE22
DE DISPLAY
Call RD KBRD

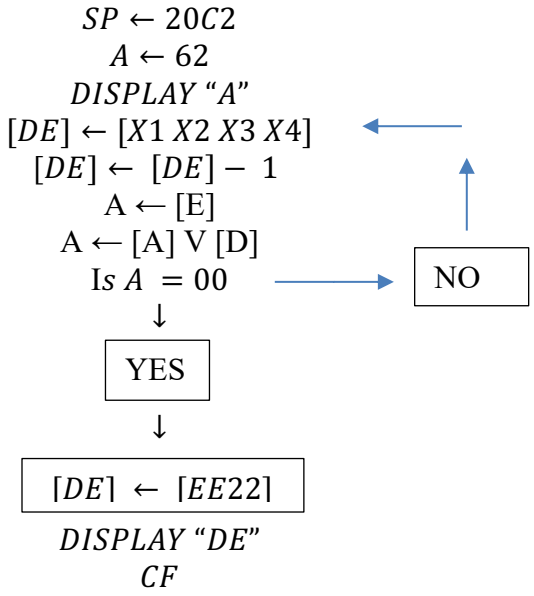
Part B

Mnemonics	OP	Address
	31 C2 2D	2000 1 2
MVI A,62	3E 62	3 4
CD O36E	CD 6E 03	5 6 7
LXID, EE22	11 22 EE	8 9 A
CD O363	CD 63 03	B C D
CD 62E7	CD E7 D2 CF	E F 10

Part C

ADDRESS	OP CODE	MNEMONICS
2000 1 2 3 4 5 6 7 8 9 10	31 C2 20 31 C2 20 3E 62 CD 6E 03	LXI,SP
11 12 13	11 99 F6	LXI DF699
14	1B	DCX D
15	7B	MOV E
16	B2	ORX D
17 18 19	CA 0F 20	JMP 200F
20 21 22	11 22 EE	LXI,D E622
21 22 23	CD 63 03	CD O363

FLOWCHART



Part D

ADDRESS	OP CODES	MNEMONICS
2000 1 2 3	31 C2 20	LXI 20C2
4 5	3E EF	MVI A, EF
6 7 8	CD 6E 03	CD 036E
9 200A 200B	11 CD AB	LXID ABCD
200C 200D 200E	CD 63 03	CD 0363
200F	11	LXID, F699
2010	99	
2011	F6	
2012	1B	DCX D
2013	7B	MOV E
2014	B2	ORX D
2015	CA	JZ 2012

2016 2017	12 20	
2018	11	LXID, F699
2019	99	
201A	F6	
201B	1B	DCX D
201C	7B	MOV E
201D	B2	ORX D
201E 201F 2020	CA 1B 20	JZ 201 B
2021 2022	3E 56	MVI 56
2023 2024 2025	CD 6E 03	CD 036E
2026 2027 2028	11 34 12	LXID, 1234
2029 202A 202B	CD 6E 03	CD 036E
202C	11	LXID, F699
202D	99	
202E	F6	
202F	1B	DCX D
2031	7B	MOV E
2032	B2	ORX D
2033 2034 2035	CA 2F 20	JZ 202F
2036	11	LXID, F699
2037	99	
2038	F6	
2039	1B	DCX D
203A	7B	MOV E
203B	B2	ORX D
203C 203D 203E	CA 28 20	JZ 2028
203F	CF	RESTART

FLOWCHART

SP ← 20C2

A ← EF
DISPLAY “A”
DE ← ABCD
DISPLAY “DE”
DE ← [F699]
DE ← [DE] -1
A ← E
A ←A V D
Is A=00
DE ← [F699]
DE ← [DE] – 1
A ←E
A ← A V D
Is A=00
A ←56
DISPLAY “A”
DE ← 1234
DISPLAY DE
DE ← [F699]
DE ← [DE] – 1
A ←E
A ← A V D
Is A=00
DE ← [F699]
DE ← [DE] – 1
A← E
A ←A V D
Is A= 00
STOP

Conclusion

In conclusion based on the value for the delay time we determined that the values for Part C and D were close enough with just slight variations of the proceeding decimal places as such we put F699 into DE. Using the formula for delay, in part C having an inside of 48 cycles and outside of 45. In the same instance for part D 48 cycles inside the first loop and 70 for outside.