Course No._____ Name_____

Section No._____

REPORT FOLDER

New York City College of Technology

OF THE CITY UNIVERSITY OF NEW YORK

Department of_____

Experiment No._____

Title_____

_____

FACULTY ONLY

Returned for corrections_____

Corrections due_____

Corrections handed in_____

Comments

Grade_____ Approved by_____

STUDENTS ONLY

Date experiment completed_____

Date due_____

Date handed in_____

Squad No._____

List Members

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Table of Contents

Objective

- Get a handle for manipulating data using the SDK-85 (Student Development Kit)
- Use Appendix F (8085 Instruction Set), specifically the Arithmetic Group, to perform operations on the registers and memory locations of the SDK-85.

Theory

- The SDK-85 (Student Development Kit) is a single board microcomputer system kit using the 8085 processor. It is made by Intel and is now used to teach students about the concepts of microprocessors. Contains the following
    - **Microprocessor**
    - **Memory Element** – This describes both ROM (Read Only Memory) and RAM (Random Access Memory)
        - ROM (Read Only Memory) – Contains system boot up instructions
        - RAM (Random Access Memory) – Has Read/Write capabilities
    - **I/O Unit** – Handles input from user and provides output
- Microprocessors are computer processors that incorporate the functions of a central processing unit on a single integrated circuit (IC) or at most a few integrated circuits. They contain the following:
    - **Combinational logic Unit** – are logic circuits implemented by Boolean (logic gates) circuits, where the output is a pure function of the present input only. Think Half-Adders, Full-Adders, Encoders, and Decoders.
    - **Sequential logic Unit** – this is a type of logic circuit whose output depends on previous inputs as well as on the present inputs.
        - Contains Memory
        - Contains a clock

This lab focuses on **Appendix F (the 8085 Instruction Set)**, specifically the **Arithmetic Group**. This is the set of assembly instructions that perform the adds, subtracts, increments, or decrements of data in registers or memory.

PART A

OP Codes

2000	3E
1	03
2	32
3	50
4	20
5	3E
6	05
7	32
8	51
9	20
10	3E
11	FB
12	32
13	52
14	20
15	3E
16	FD
17	32
18	53
19	20
20	3E
21	12
22	32
23	54
24	20
25	3E
26	17
27	32
28	55
29	20
30	3E
31	18
32	32
33	56
34	20
35	3E
36	EE

37	32
38	57
39	20
40	3E
41	EF
42	32
43	58
44	20

FLOWCHART

A ←03
[2050] ←A
A ←05
[2051] ←A
FB ← -05
[2052] ←FB
FD ← -03
[2053] ←FD
A ←12
[2054] ←A
A ←17
[2055] ←A
A ←18
[2056] ←A
EE ← -18
[2057] ←EE
EF ← -17
[2058] ← EF

Part B

2000	3E
2001	03
2002	06
2003	05
2004	80
2005	32
2006	59
2007	20
2008	3E
2009	03
200A	06
200B	FB
200C	80
200D	32
200E	5A
200F	20
2010	3E
2011	FD
2012	06
2013	05
2014	80
2015	32
2016	5B
2017	20
2018	3E
2019	FD
201A	06
201B	FB
201C	80
201D	32
201E	5C
201F	20
2020	3E
2021	12
2022	06
2023	17
2024	80
2025	32
2026	5D
2027	20
2028	3E

2029	12
202A	06
202B	EF
202C	80
202D	32
202E	5E
202F	20
2030	3E
2031	F8
2032	06
2033	EF
2034	80
2035	32
2036	5F
2037	20
2038	3E
2039	F8
203A	06
203B	17
203C	80
203D	32
203E	60
203F	20
2040	CF

Part C

DATA	OP	A	B	2059	205A	205B	205C	205D	205E	205F	2060
2000	3E										
2002	06	03									
2004	80	03	05								
2005	32	08	05								
2008	3E	08	05	08							
200A	06	03	05	08							
200C	80	03	FB	08							
200D	32	FE	FB	08							
2010	3E	FE	FB	08	FE						
2012	06	FD	FB	08	FE						
2014	80	FD	05	08	FE						
2015	32	02	05	08	FE						
2018		02	05	08	FE	02					
201A		FD	05	08	FE	02					
201C		FD	FB	08	FE	02					
201D		F8	FB	08	FE	02					
2020		F8	FB	08	FE	02	F8				
2022		12	FB	08	FE	02	F8				
2024		12	17	08	FE	02	F8				
2025		29	17	08	FE	02	F8				
2028		29	17	08	FE	02	F8	29			
202A		12	17	08	FE	02	F8	29			
202C		12	EF	08	FE	02	F8	29			
202D		FB	EF	08	FE	02	F8	29			
2030		FB	EF	08	FE	02	F8	29	FB		
2032		F8	EF	08	FE	02	F8	29	FB		
2034		F8	EF	08	FE	02	F8	29	FB		
2035		E3	EF	08	FE	02	F8	29	FB		
2038		E3	EF	08	FE	02	F8	29	FB	E3	
203A		F8	EF	08	FE	02	F8	29	FB	E3	
203C		F8	17	08	FE	02	F8	29	FB	E3	
203D		05	17	08	FE	02	F8	29	FB	E3	
2040	CF	05	17	08	FE	02	F8	29	FB	E3	05

Part D

$$[-03] + [03] = [00]$$
$$[03] - [+03] = [00]$$

$$-03 \rightarrow 1111\ 1101$$
$$\underline{+03 \rightarrow 0000\ 0011}$$
$$00 \rightarrow 1\ 0000\ 0000$$

- There's an overflow

Part E

Flow Chart	Mnemonics	Memory	OP Code
$[A] \leftarrow [2051]$	LDA 2051	2000	3A
		2001	51
		2002	20
$\left[[HL]\right] \leftarrow [A]$	MOV M, A	2003	77
$[A] \leftarrow [2050]$	LDA 2050	2004	3A
		2005	50
		2006	20
$[A] \leftarrow [A] - [[HL]]$	SUB M	2007	96

Flow Chart	Mnemonics	Memory	OP Code
$[A] \leftarrow [2051]$	LDA 2051	2000	3A
		2001	51
		2002	20
$\left[[HL]\right] \leftarrow [A]$	MOV M, A	2003	77
$[A] \leftarrow [2053]$	LDA 2053	2004	3A
		2005	53
		2006	20
$[A] \leftarrow [A] + [[HL]]$	ADD M	2007	86

Part F

Flow Chart	Mnemonics	Memory	OP Code
$[A] \leftarrow [2056]$	LDA 2056	2000	3A
		2001	56
		2002	20
$[C] \leftarrow [A]$	MOV C, A	2003	4F
$[A] \leftarrow [2055]$	LDA 2055	2004	3A
		2005	55
		2006	20
$[B] \leftarrow [A]$	MOV B, A	2007	47
$[A] \leftarrow [2054]$	LDA 2054	2008	3A
		2009	54
		200A	20
$[A] \leftarrow [A] + [B]$	ADD B	200B	80
	DAA	200C	27
$[2061] \leftarrow [A]$	STA 2061	200D	32
		200E	61
		200F	20
$[A] \leftarrow [2054]$	LDA 2054	2010	3A
		2011	54
		2012	20
$[A] \leftarrow [A] + [C]$	ADD C	2013	81
	DAA	2014	27
$[2062] \leftarrow [A]$	STA 2062	2015	32
		2016	62
		2017	20

Part G

Flow Chart	Mnemonics	Memory	OP Code
$[A] \leftarrow [2054]$	LDA 2054	2000	3A
		2001	54
		2002	20
$[C] \leftarrow [A]$	MOV C, A	2003	4F
$[A] \leftarrow [2055]$	LDA 2055	2004	3A
		2005	55
		2006	20
$[A] \leftarrow [A] - [C]$	SUB C	2007	91
	DAA	2008	27
$[2063] \leftarrow [A]$	STA 2063	2009	32
		200A	63
		200B	20
$[A] \leftarrow [2055]$	LDA 2055	200C	3A
		200D	55
		200E	20
$[C] \leftarrow [A]$	MOV C, A	200F	4F
$[A] \leftarrow [2054]$	LDA 2054	2010	3A
		2011	54
		2012	20
$[A] \leftarrow [A] - [C]$	SUB C	2013	91
	DAA	2014	27
$[2064] \leftarrow [A]$	STA 2064	2015	32
		2016	64
		2017	20
$[A] \leftarrow [2050]$	LDA 2050	2018	3A

		2019	50
		201A	20
$[C] \leftarrow [A]$	MOV C, A	201B	4F
$[A] \leftarrow [2054]$	LDA 2054	201C	3A
		201D	54
		201E	20
$[A] \leftarrow [A] - [C]$	SUB C	201F	91
	DAA	2020	27
$[2065] \leftarrow [A]$	STA 2065	2021	32
		2022	65
		2023	20

Part H

Flow Chart	Mnemonics	Memory	OP Code
$[[HL]] \leftarrow [0793]$	LXI H, 0793	2000	21
		2001	93
		2002	07
$[[DE]] \leftarrow [0805]$	LXI D, 0805	2003	11
		2004	05
		2005	08
$[HL] \leftarrow [HL] + [DE]$	DAD D	2006	19
	DAA	2007	27
$[A] \leftarrow [H]$	MOV A, H	2008	7C
$[2065] \leftarrow [A]$	STA 2065	2009	32
		200A	65
		200B	20
$[A] \leftarrow [L]$	MOV A, L	200C	7D
$[2066] \leftarrow [A]$	STA 2066	200D	32
		200E	66
		200F	20
$[[HL]] \leftarrow [0793]$	LXI H, 0793	2010	21
		2011	93
		2012	07
$[[BC]] \leftarrow [0585]$	LXI B, 0585	2013	01
		2014	85
		2015	05
$[HL] \leftarrow [HL] + [BC]$	DAD B	2016	09
	DAA	2017	27
$[A] \leftarrow [H]$	MOV A, H	2018	7C

$[2067] \leftarrow [A]$	STA 2067	2019	32
		201A	67
		201B	20
$[A] \leftarrow [L]$	MOV A, L	201C	7D
$[2068] \leftarrow [A]$	STA 2068	201D	32
		201E	68
		201F	20

Part I

Flow Chart	Mnemonics	Memory	OP Code
$[[HL]] \leftarrow [1793]$	LXI H, 1793	2000	21
		2001	93
		2002	17
$[[DE]] \leftarrow [3805]$	LXI D, 3805	2003	11
		2004	05
		2005	38
$[HL] \leftarrow [HL] + [DE]$	DAD D	2006	19
	DAA	2007	27
$[A] \leftarrow [H]$	MOV A, H	2008	7C
$[2069] \leftarrow [A]$	STA 2069	2009	32
		200A	69
		200B	20
$[A] \leftarrow [L]$	MOV A, L	200C	7D
$[206A] \leftarrow [A]$	STA 206A	200D	32
		200E	6A
		200F	20
$[[HL]] \leftarrow [7793]$	LXI H, 0793	2010	21
		2011	93

		2012	77
$[[BC]] \leftarrow [6585]$	LXI B, 6585	2013	01
		2014	85
		2015	65
$[HL] \leftarrow [HL] + [BC]$	DAD B	2016	09
	DAA	2017	27
$[A] \leftarrow [H]$	MOV A, H	2018	7C
$[206C] \leftarrow [A]$	STA 2065	2019	32
		201A	6C
		201B	20
$[A] \leftarrow [L]$	MOV A, L	201C	7D
$[206D] \leftarrow [A]$	STA 206D	201D	32
		201E	6D
		201F	20

Conclusion

- We didn't have enough time to test the code. This can be considered if errors were to pop up. However, we do feel as though we have a firm grasp of what was going on within this lab. Therefore, we assume that we did pretty well in solving the problems presented within this lab.

LABORATORY FORMAT / MPROCESSOR THEORY (INTEL 8085)

1. Folder (name, TITLE, course, SECTION, dates)
2. INDEX. (label all pages)
3. OBJECTIVES
4. THEORY NEEDED
5. CALCULATED VALUES / SINGLE STEPPING
6. PROGRAM, FLOWCHART, MNEMONICS, O.C.
7. QUESTIONS / ANSWERS.
8. CONCLUSION / DISCUSSION
9. APPLICATIONS (OPTIONAL).
10. ATTACH LAB. MANUAL INSTRUCTIONS.

LATE PENALTIES:

1 week = -5pts
2 weeks = -10pts
3 weeks = -20pts
4 or more weeks = NOT ACCEPTED

COURSE TEXT

MOHAMED RAFIQUIZZMAN,
"Microcomputer Theory and Applications with the (INTEL 8085) SDK-85", WILEY

M.K.