
**INSTITUTO TECNOLÓGICO DE COSTA RICA**
**ESCUELA DE INGENIERÍA EN ELECTRÓNICA**
**EL3310: DISEÑO DE SISTEMAS DIGITALES**

**TIPO DE ASIGNACIÓN: TRABAJO INDIVIDUAL**

**TÍTULO:**
**“Trabajo Individual #2 -**
**Bancos de Memoria”**

**AUTOR:**
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**RESPONSABLE TÉCNICO:**
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**Cartago, Costa Rica**
**2022**

## Introducción

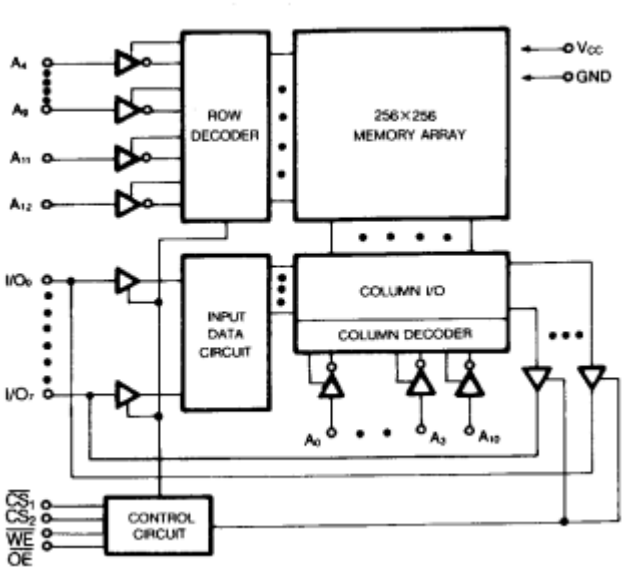
El presente documento corresponde a la Asignación de tipo Trabajo Individual, por parte del curso Diseño de Sistemas Digitales (EL3310) del Instituto Tecnológico de Costa Rica, el mismo pretende dotar al estudiante de capacidades para diseñar bancos de memoria para un microprocesador en particular.

## Desarrollo

Utilizando la memoria RAM HY 6264 construya un banco de memoria de 16KX8 bits.

**PIN NAMES**

| | |
|---|---|
| $A_0$-$A_{12}$ | ADDRESS INPUT |
| $I/O_0$-$I/O_7$ | DATA INPUT/OUTPUT |
| $\overline{CS_1}$ | CHIP SELECT ONE |
| $CS_2$ | CHIP SELECT TWO |
| $\overline{WE}$ | WRITE ENABLE |
| $\overline{OE}$ | OUTPUT ENABLE |
| $V_{CC}$ | POWER |
| GND | GROUND |




**DC CHARACTERISTICS**

($V_{CC}$=5V± 10%, $T_A$=0°C to 70°C)

| SYMBOL | PARAMETER | TEST CONDITIONS | | HY6264 MIN. | HY6264 TYP.(1) | HY6264 MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $\|I_{LI}\|$ | Input Leakage Current | $V_{IN}$=GND to $V_{CC}$ | | – | – | 2 | μA |
| $\|I_{LO}\|$ | Output Leakage Current | $\overline{CS_1}$=$V_{IH}$, $CS_2$=$V_{IL}$ or $\overline{OE}$=$V_{IH}$, $V_{I/O}$=GND to $V_{CC}$ | | – | – | 2 | μA |
| $I_{CC}$ | Operating Power Supply Current | $\overline{CS_1}$=$V_{IL}$, $CS_2$=$V_{IH}$, $I_{I/O}$=0mA | | – | 30 | 50 | mA |
| $I_{CC1}$ | Average Operating Current | Min. Duty Cycle=100%, $\overline{CS_1}$=$V_{IL}$, $CS_2$=$V_{IH}$ | | – | 40 | 70 | mA |
| $I_{SB}$ | Standby Power Supply Current | $\overline{CS_1}$=$V_{IH}$ or $CS_2$=$V_{IL}$ | | – | 1 | 3 | mA |
| $I_{SB1}$(2) | | $\overline{CS_1}$≥$V_{CC}$−0.2V, $CS_2$≤ 0.2V or ≥ $V_{CC}$−0.2V | L | – | 20 | 2000 | μA |
| | | | | – | 2 | 300 | |
| $I_{SB2}$(2) | | $\overline{CS_1}$≥2.2V or ≥$V_{CC}$−0.2V, $CS_2$≥2.2V | L | – | 20 | 2000 | μA |
| | | | | – | 2 | 100 | |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$=2.1mA | | – | – | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$=−1.0mA | | 2.4 | – | – | V |

NOTES:
1. Typical limits are at $V_{CC}$=5.0V, $T_A$=25°C and specified loading.
2. $V_{IL}$ min=−0.5V

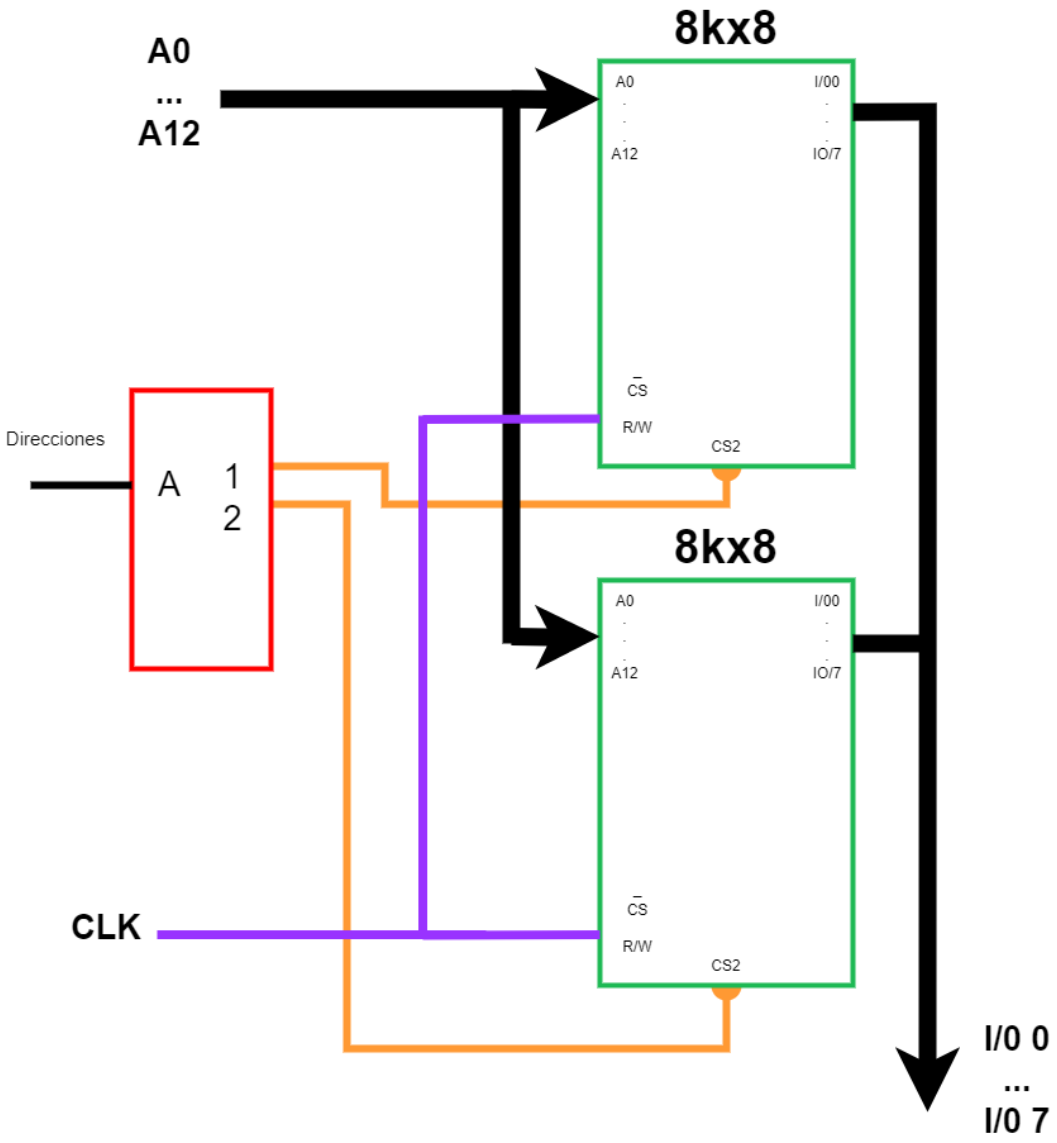
**AC CHARACTERISTICS**

($V_{CC}$=5V± 10%, $T_A$= 0°C to 70°C)

READ CYCLE

| SYMBOL | PARAMETER | | HY6264-70 MIN. | HY6264-70 MAX. | HY6264-85 MIN. | HY6264-85 MAX. | HY6264-10 MIN. | HY6264-10 MAX. | HY6264-12 MIN. | HY6264-12 MAX. | HY6264-15 MIN. | HY6264-15 MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{RC}$ | Read Cycle Time | | 70 | – | 85 | – | 100 | – | 120 | – | 150 | – | ns |
| $t_{AA}$ | Address Access Time | | – | 70 | – | 85 | – | 100 | – | 120 | – | 150 | ns |
| $t_{ACS1}$ | Chip Select Access Time | $\overline{CS_1}$ | – | 70 | – | 85 | – | 100 | – | 120 | – | 150 | ns |
| $t_{ACS2}$ | | $CS_2$ | – | 70 | – | 85 | – | 100 | – | 120 | – | 150 | ns |
| $t_{OE}$ | Output Enable to Output Valid | | – | 45 | – | 50 | – | 55 | – | 60 | – | 70 | ns |
| $t_{CLZ1}$ | Chip Select to Output in Low-Z | $\overline{CS_1}$ | 10 | – | 10 | – | 10 | – | 10 | – | 15 | – | ns |
| $t_{CLZ2}$ | | $CS_2$ | 10 | – | 10 | – | 10 | – | 10 | – | 15 | – | ns |
| $t_{OLZ}$ | Output Enable to Output in Low-Z | | 5 | – | 5 | – | 5 | – | 5 | – | 5 | – | ns |
| $t_{CHZ1}$ | Chip Deselect to Output in High-Z | $\overline{CS_1}$ | 0 | 30 | 0 | 35 | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| $t_{CHZ2}$ | | $CS_2$ | 0 | 30 | 0 | 35 | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| $t_{OHZ}$ | Output Disable to Output in High-Z | | 0 | 30 | 0 | 35 | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| $t_{OH}$ | Output Hold from Address Change | | 10 | – | 10 | – | 10 | – | 10 | – | 15 | – | ns |

Datasheet: https://datasheetspdf.com/pdf-file/237462/HynixSemiconductor/HY6264-85/1

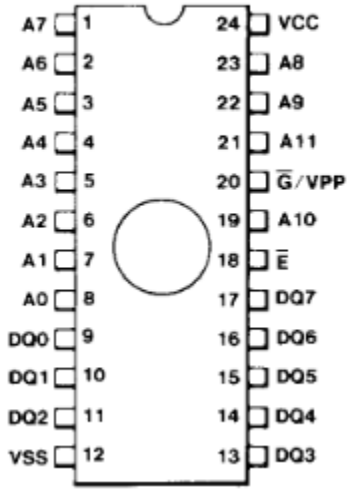

A0
...
A12
8kx8
A0
A12
I/00
IO/7
CS
R/W
CS2
Direcciones
A
1
2
8kx8
A0
A12
I/00
IO/7
CS
R/W
CS2
CLK
I/0 0
...
I/0 7

Utilizando la memoria EPROM 2732 construya un banco de memoria de 16KX8 bits.

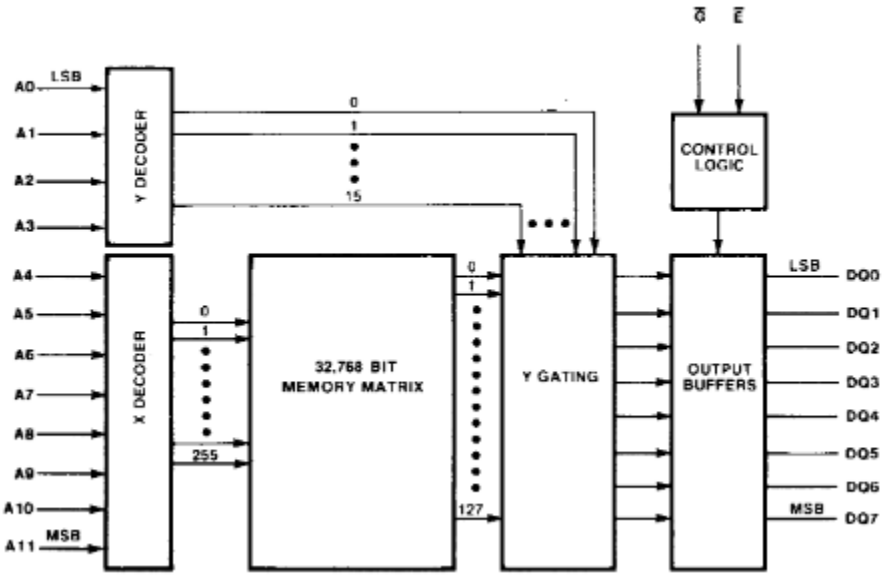
**Pin Names**

| | |
|---|---|
| A0–A11 | Address Inputs |
| $\overline{E}$ | Chip Enable (Power Down) Input |
| $\overline{G}$/VPP | Output Enable/+25 V Program Input |
| DQ0–DQ7 | Data Output/Programming Inputs |
| VCC | +5 V Supply |
| VSS | Ground |

**Connection Diagram**
**24-Pin DIP**




**Block Diagram**




Datasheet: https://pdf1.alldatasheet.com/datasheet-pdf/view/129050/FAIRCHILD/2732.html

$2^n = 16(1024) \Rightarrow n = 14 líneas$