#### SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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- Choice of Eight Latches or Eight D-Type Flip-Flops in a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Clock-Enable Input Has Hysteresis to Improve Noise Rejection ('S373 and 'S374)
- P-N-P Inputs Reduce DC Loading on Data Lines ('S373 and 'S374)

#### description

These 8-bit registers feature 3-state outputs designed specifically for driving highly capacitive relatively low-impedance loads. high-impedance 3-state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pullup components. These devices are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches, meaning that while the enable (C or CLK) input is high, the Q outputs follow the data (D) inputs. When C or CLK is taken low, the output is latched at the level of the data that was set up.

The eight flip-flops of the 'LS374 and 'S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic states that were set up at the D inputs.

SN54LS373, SN54LS374, SN54S373, SN54S374...J OR W PACKAGE SN74LS373, SN74S374...DW, N, OR NS PACKAGE SN74LS374...DB, DW, N, OR NS PACKAGE SN74S373...DW OR N PACKAGE (TOP VIEW)

The state of the s		$\overline{}$		1
OC [	1	O	20	] ∨ <sub>cc</sub>
1Q [	2		19	[] 8Q
1D [	3		18	] 8D
2D [	4		17	] 7D
2Q [	5		16	] 7Q
3Q [	6		15	] 6Q
3D [	7		14	] 6D
4D [	8		13	] 5D
4Q [	9		12	] 5Q
GND [	10		11	] C†

† C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.

SN54LS373, SN54LS374, SN54S373, SN54S374 . . . FK PACKAGE (TOP VIEW)



† C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.

Schmitt-trigger buffered inputs at the enable/clock lines of the 'S373 and 'S374 devices simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output-control  $(\overline{OC})$  input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

OC does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered, even while the outputs are off.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



#### **ORDERING INFORMATION**

TA	PACI	KAGE <sup>†</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
		Tube	SN74LS373N	SN74LS373N
	PDIP – N	Tube	SN74LS374N	SN74LS374N
	PDIP = N	Tube	SN74S373N	SN74S373N
		Tube	SN74S374N	SN74S374N
		Tube	SN74LS373DW	LS373
		Tape and reel	SN74LS373DWR	L33/3
		Tube	SN74LS374DW	1.0074
000 to 7000	SOIC - DW	Tape and reel	SN74LS374DWR	LS374
0°C to 70°C	SOIC - DW	Tube	SN74S373DW	0070
		Tape and reel	SN74S373DWR	S373
		Tube	SN74S374DW	0074
		Tape and reel	SN74S374DWR	S374
		Tape and reel	SN74LS373NSR	74LS373
	SOP - NS	Tape and reel	SN74LS374NSR	74LS374
		Tape and reel	SN74S374NSR	74S374
	SSOP - DB	Tape and reel	SN74LS374DBR	LS374A
		Tube	SN54LS373J	SN54LS373J
		Tube	SNJ54LS373J	SNJ54LS373J
		Tube	SN54LS374J	SN54LS374J
	CDIP – J	Tube	SNJ54LS374J	SNJ54LS374J
	CDIP - J	Tube	SN54S373J	SN54S373J
		Tube	SNJ54S373J	SNJ54S373J
		Tube	SN54S374J	SN54S374J
–55°C to 125°C		Tube	SNJ54S374J	SNJ54S374J
		Tube	SNJ54LS373W	SNJ54LS373W
	CFP – W	Tube	SNJ54LS374W	SNJ54LS374W
		Tube	SNJ54S374W	SNJ54S374W
		Tube	SNJ54LS373FK	SNJ54LS373FK
	LCCC – FK	Tube	SNJ54LS374FK	SNJ54LS374FK
	LCCC - FK	Tube	SNJ54S373FK	SNJ54S373FK
		Tube	SNJ54S374FK	SNJ54S374FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



#### **Function Tables**

'LS373, 'S373 (each latch)

	INPUTS		OUTPUT
<u>oc</u>	С	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	$Q_0$
Н	Χ	Χ	z

'LS374, 'S374 (each latch)

	INPUTS		OUTPUT
oc	CLK	D	Q
L	$\uparrow$	Н	Н
L	$\uparrow$	L	L
L	L	Χ	$Q_0$
Н	X	X	Z

#### logic diagrams (positive logic)

'LS373, 'S373 **Transparent Latches**  $\overline{\mathsf{oc}}$ C1 - 1Q 1D -1D C1 1D 2D C1 3Q 1D C1 1D 4D C1 13 1D 5D C1 14 1D 6D C1 17 1D 7D

C1

1D

18

8D





8Q

#### schematic of inputs and outputs

#### 'LS373



'LS374



#### SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)† ('LS devices)

Supply voltage, V <sub>CC</sub> (see Note 1)		7 V
Input voltage, V <sub>I</sub>		7 V
Off-state output voltage		5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 2):	DB package	70°C/W
***	DW package	58°C/W
	N package	69°C/W
	NS package	60°C/W
Storage temperature range, T <sub>sto</sub>		-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

			SN54LS'			SN74LS'			UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX	UNII	
Vcc	Supply voltage		4.5	5	5	4.75	5	5.25	V	
Vон	High-level output voltage				5.5			5.5	V	
Іон	High-level output current				-1			-2.6	mA	
loL	Low-level output current				12			24	mA	
	Pulse duration	CLK high	15			15			no	
t <sub>W</sub>		CLK low	15			15			ns	
	Data setup time	'LS373	5↓			5↓			no	
t <sub>su</sub>	Data setu <b>p</b> time	'LS374	20↑			20↑			ns	
4.	Data hold time	'LS373	20↓			20↓			ns	
th	Data hold time	'LS374 <sup>‡</sup>	5↑			01				
TA	Operating free-air temperature				125	0		70	°C	

<sup>‡</sup> The th specification applies only for data frequency below 10 MHz. Designs above 10 MHz should use a minimum of 5 ns (commercial only).



NOTES: 1. Voltage values are with respect to network ground terminal.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETED			+	,	SN54LS	,	,	SN74LS	'	
	PARAMETER	TEST	CONDITION	ISI	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage				2			2			V
V <sub>IL</sub>	Low-level input voltage						0.7			0.8	V
٧ıĸ	Input clamp voltage	V <sub>CC</sub> = MIN,	l <sub>l</sub> = −18 mA				-1.5			-1.5	V
VOH	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = V <sub>IL</sub> max,	V <sub>IH</sub> = 2 V, I <sub>OH</sub> = MAX		2.4	3.4		2.4	3.1		٧
V	/	V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V,	I <sub>OL</sub> = 12 mA		0.25	0.4		0.25	0.4	V
VOL	Low-level output voltage	V <sub>IL</sub> = V <sub>IL</sub> max		I <sub>OL</sub> = 24 mA					0.35	0.5	V
lozh	Off-state output current, high-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7 V	V <sub>IH</sub> = 2 V,				20			20	μΑ
lozL	Off-state output current, low-level voltage applied	$V_{CC} = MAX,$ $V_{O} = 0.4 V$	V <sub>IH</sub> = 2 V,				-20			-20	μΑ
ΙΙ	Input current at maximum input voltage	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 7 V				0.1			0.1	mA
lн	High-level input current	$V_{CC} = MAX$ ,	V <sub>I</sub> = 2.7 V				20			20	μΑ
Ι <sub>Ι</sub> L	Low-level input current	$V_{CC} = MAX$ ,	V <sub>I</sub> = 0.4 V				-0.4			-0.4	mA
los	Short-circuit output current§	$V_{CC} = MAX$			-30		-130	-30		-130	mA
la a	Cumply ourront	V <sub>CC</sub> = MAX,		'LS373		24	40		24	40	mA
Icc	Supply current	Output control a	t 4.5 V	'LS374		27	40		27	40	IIIA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

#### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$ (see Figure 1)

PARAMETER	FROM	то	TEST CONDITIONS	'LS373			'LS374			UNIT
PARAMETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f <sub>max</sub>			$R_L = 667 \Omega$ , $C_L = 45 pF$ , See Note 3				35	50		MHz
t <sub>PLH</sub>	Data	Any Q	$R_L = 667 \Omega, C_L = 45 pF,$		12	18				no
tPHL	Dala	Arry Q	See Note 3		12	18				ns
tPLH	C or CLK	Any Q	$R_L = 667 \Omega$ , $C_L = 45 pF$ , See Note 3		20	30		15	28	no
t <sub>PHL</sub>	C OI CLK	Ally Q			18	30		19	28	ns
<sup>t</sup> PZH	<del>oc</del>	Any Q	$R_L = 667 \Omega, C_L = 45 pF,$		15	28		20	26	ns
t <sub>PZL</sub>	00	Arry Q	See Note 3		25	36		21	28	110
<sup>t</sup> PHZ	<del>oc</del>	Any Q	$R_1 = 667 \Omega, C_1 = 5 pF$		15	25		15	28	ns
t <sub>PLZ</sub>	5	Ally Q	KL = 007 32, CL = 5 pr		12	20		12	20	115

NOTE 3: Maximum clock frequency is tested with all outputs loaded.

fmax = maximum clock frequency

tplH = propagation delay time, low-to-high-level output

tpHL = propagation delay time, high-to-low-level output

tpzH = output enable time to high level

tpzL = output enable time to low level

tPHZ = output disable time from high level

t<sub>PLZ</sub> = output disable time from low level



<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>§</sup> Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

### OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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#### schematic of inputs and outputs

'S373 and 'S374

#### 'S373 and 'S374



# SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS373, SN74LS374, SN74S373, SN74S374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)† ('S devices)

Supply voltage, V <sub>CC</sub> (see Note 1)		7 V
Input voltage, V <sub>I</sub>		5.5 V
Off-state output voltage		5.5 V
Package thermal impedance, θ <sub>JA</sub> (see Note 2)	: DW package	58°C/W
	N package	69°C/W
	NS package	60°C/W
Storage temperature range, T <sub>sto</sub>		-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.

#### recommended operating conditions

				SN54S'			SN74S'		UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX	UNII	
V <sub>CC</sub> Supply voltage			4.5	5	5.5	4.75	5	5.25	V	
Vон	High-level output voltage				5.5			5.5	V	
loh	High-level output current				-2			-6.5	mA	
	Pulse duration, clock/enable	High	6			6			ns	
t <sub>W</sub>	ruise duration, clock/enable	Low	7.3			7.3			115	
	Data actus timo	'S373	0↓			0↓			20	
t <sub>su</sub>	Data setup time	'S374	5↑			5↑			ns	
4.	Data hold time	'S373	10↓			10↓			no	
<sup>t</sup> h	Data Holu time	'S374	2↑			2↑			ns	
TA	Operating free-air temperature		-55		125	0		70	°C	



<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (SN54S373, SN54S374, SN74S373, SN74S374)

PARA	METER		TES	ST CONDITIONS†		MIN	TYP‡	MAX	UNIT
٧ıH						2			V
V <sub>IL</sub>								0.8	V
٧ıK		$V_{CC} = MIN,$	$I_{I} = -18 \text{ mA}$					-1.2	V
Va	SN54S'	Voo – MIN	\/ 2 \/	V: 0.8 V	lou - MAY	2.4	3.4		V
VOH	SN74S'	$V_{CC} = MIN,$	$V_{IH} = 2 V$	$V_{IL} = 0.8 V$	I <sub>OH</sub> = MAX	2.4	3.1		V
$V_{OL}$		$V_{CC} = MIN,$	V <sub>IH</sub> = 2 V,	$V_{IL} = 0.8 V$ ,	$I_{OL} = 20 \text{ mA}$			0.5	V
lozh		$V_{CC} = MAX$ ,	V <sub>IH</sub> = 2 V,	V <sub>O</sub> = 2.4 V				50	μΑ
lozL		$V_{CC} = MAX$ ,	V <sub>IH</sub> = 2 V,	$V_0 = 0.5 V$				-50	μΑ
II		$V_{CC} = MAX$ ,	V <sub>I</sub> = 5.5 V					1	mA
lιΗ		$V_{CC} = MAX$ ,	V <sub>I</sub> = 2.7 V					50	μΑ
IIL		$V_{CC} = MAX$ ,	V <sub>I</sub> = 0.5 V					-250	μΑ
los§		$V_{CC} = MAX$				-40		-100	mA
				Outputs high				160	
			'S373	Outputs low				160	
				Outputs disable	d			190	
ICC		$V_{CC} = MAX$		Outputs high				110	mA
		,	'S374	Outputs low				140	
			33/4	Outputs disable	d			160	
				CLK and OC at	4 V, D inputs at 0 V			180	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

#### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$ (see Figure 2)

PARAMETER	FROM	то	TEST CONDITIONS		'S373		'S374			UNIT
PARAMETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f <sub>max</sub>			$R_L = 280 \Omega$ , $C_L = 15 pF$ , See Note 3				75	100		MHz
t <sub>PLH</sub>	Data	Any Q	$R_L = 280 \Omega, C_L = 15 pF,$		7	12				ns
<sup>t</sup> PHL	Dala	Ally Q	See Note 3		7	12				115
t <sub>PLH</sub>	C or CLK	Any O	Any Q $R_L = 280 \Omega$ , $C_L = 15 pF$ , See Note 3		7	14		8	15	ns
t <sub>PHL</sub>	COICLK	Ally Q			12	18		11	17	115
<sup>t</sup> PZH	<del>oc</del>	Any Q	$R_L = 280 \Omega, C_L = 15 pF,$		8	15		8	15	ns
t <sub>PZL</sub>	00	Ally Q	See Note 3		11	18		11	18	115
<sup>t</sup> PHZ	<del>oc</del>	Any Q	P 200 O C 5 pE		6	9		5	9	ns
<sup>t</sup> PLZ	UC	Ally Q	$R_L = 280 \Omega, C_L = 5 pF$		8	12		7	12	115

NOTE 3. Maximum clock frequency is tested with all outputs loaded.

f<sub>max</sub> = maximum clock frequency

tpLH = propagation delay time, low-to-high-level output

tpHL = propagation delay time, high-to-low-level output

tpzH = output enable time to high level

tpzL = output enable time to low level

tpHZ = output disable time from high level

tpl 7 = output disable time from low level



<sup>&</sup>lt;sup>‡</sup> All typical values are at  $V_{CC}$ = 5 V,  $T_A$  = 25°C.

<sup>§</sup> Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

### PARAMETER MEASUREMENT INFORMATION SERIES 54LS/74LS DEVICES



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All diodes are 1N3064 or equivalent.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. S1 and S2 are closed for tpLH, tpHZ, and tpLZ; S1 is open and S2 is closed for tpZH; S1 is closed and S2 is open for tpZL.
  - E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
  - F. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_{O} \approx 50 \Omega$ ,  $t_{f} \leq 1.5$  ns,  $t_{f} \leq 2.6$  ns.
  - G. The outputs are measured one at a time with one input transition per measurement.
  - H. All parameters and waveforms are not applicable to all devices .

Figure 1. Load Circuits and Voltage Waveforms



#### OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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#### PARAMETER MEASUREMENT INFORMATION **SERIES 54S/74S DEVICES**



- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. All diodes are 1N3064 or equivalent.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. S1 and S2 are closed for tpLH, tpHL, tpHZ, and tpLZ; S1 is open and S2 is closed for tpZH; S1 is closed and S2 is open for tpZL.
  - E. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O \approx 50 \Omega$ ;  $t_r$  and  $t_f \leq$  7 ns for Series 54/74 devices and  $t_r$  and  $t_f \le 2.5$  ns for Series 54S/74S devices.
  - F. The outputs are measured one at a time with one input transition per measurement.
  - G. All parameters and waveforms are not applicable to all devices .

Figure 2. Load Circuits and Voltage Waveforms



#### **TYPICAL APPLICATION DATA**



Expandable 4-Word by 8-Bit General Register File









10-Jun-2014

#### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Sample
5962-7801102VRA	ACTIVE	CDIP	J	20	20	TBD	A42	N / A for Pkg Type	-55 to 125	5962-7801102VR A SNV54LS374J	Sampl
5962-7801102VSA	ACTIVE	CFP	W	20	25	TBD	A42	N / A for Pkg Type	-55 to 125	5962-7801102VS A SNV54LS374W	Sampl
78011022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	78011022A SNJ54LS 374FK	Sampl
7801102RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7801102RA SNJ54LS374J	Sampl
7801102SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7801102SA SNJ54LS374W	Samp
JM38510/32502B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32502B2A	Samp
JM38510/32502BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32502BRA	Samp
JM38510/32502BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32502BSA	Samp
JM38510/32502SRA	ACTIVE	CDIP	J	20	20	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32502SRA	Samp
JM38510/32502SSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32502SSA	Samp
JM38510/32503B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32503B2A	Samp
JM38510/32503BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32503BRA	Samp
JM38510/32503BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32503BSA	Samp
M38510/32502B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32502B2A	Samp
M38510/32502BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32502BRA	Samp
M38510/32502BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32502BSA	Samp





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Orderable Device	Status	Package Type		Pins		Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
M38510/32502SRA	ACTIVE	CDIP	J	20	20	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32502SRA	Samples
M38510/32502SSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32502SSA	Samples
M38510/32503B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32503B2A	Samples
M38510/32503BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32503BRA	Samples
M38510/32503BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32503BSA	Samples
SN54LS373J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS373J	Samples
SN54LS374J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS374J	Samples
SN54S373J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S373J	Samples
SN54S374J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S374J	Samples
SN74LS373DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS373	Samples
SN74LS373DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS373	Samples
SN74LS373DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS373	Samples
SN74LS373DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS373	Samples
SN74LS373N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS373N	Samples
SN74LS373N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74LS373NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS373N	Samples
SN74LS373NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS373	Samples
SN74LS374DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS374A	Samples
SN74LS374DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS374	Samples





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Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
SN74LS374DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS374	Sample
SN74LS374DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS374	Sample
SN74LS374DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS374	Sample
SN74LS374J	OBSOLETI	CDIP	J	20		TBD	Call TI	Call TI	0 to 70		
SN74LS374N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS374N	Sample
SN74LS374N3	OBSOLETI	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74LS374NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS374N	Sample
SN74LS374NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS374	Sample
SN74LS374NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS374	Sample
SN74S373DW	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S373	
SN74S373J	OBSOLETI	CDIP	J	20		TBD	Call TI	Call TI	0 to 70		
SN74S373N	NRND	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S373N	
SN74S373N3	OBSOLETI	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74S374J	OBSOLETI	CDIP	J	20		TBD	Call TI	Call TI	0 to 70		
SN74S374N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S374N	Sample
SN74S374N3	OBSOLETI	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SNJ54LS373FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 373FK	Sample
SNJ54LS373J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type -55 to 125 SNJ54LS3		SNJ54LS373J	Sample
SNJ54LS373W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS373W	Sample
SNJ54LS374FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	78011022A SNJ54LS 374FK	Sample



#### PACKAGE OPTION ADDENDUM

10-Jun-2014

Orderable Device	Status	Package Type	_	Pins	_	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	<b>Device Marking</b>	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
SNJ54LS374J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7801102RA SNJ54LS374J	Samples
SNJ54LS374W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7801102SA SNJ54LS374W	Samples
SNJ54S373FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 373FK	Samples
SNJ54S373J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S373J	Samples
SNJ54S374FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 374FK	Samples
SNJ54S374J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S374J	Samples
SNJ54S374W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S374W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** Tl's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



#### PACKAGE OPTION ADDENDUM

10-Jun-2014

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS373, SN54LS373-SP, SN54LS374, SN54LS374-SP, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74LS373, SN74LS374, S

Catalog: SN74LS373, SN54LS373, SN74LS374, SN54LS374, SN74S373, SN74S374

Military: SN54LS373, SN54LS374, SN54S373, SN54S374

Space: SN54LS373-SP, SN54LS374-SP

NOTE: Qualified Version Definitions:

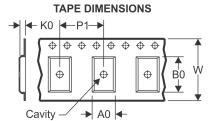
- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application

#### PACKAGE MATERIALS INFORMATION

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#### TAPE AND REEL INFORMATION





Α0	
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS373DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS373NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LS374DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LS374DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS374NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.5	4.0	24.0	Q1

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\*All dimensions are nominal

7 til diffictioloffo die floriffiat							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS373DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS373NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LS374DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LS374DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS374NSR	SO	NS	20	2000	367.0	367.0	45.0

#### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

### W (R-GDFP-F20)

#### CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

  D. Index point is provided on cap for terminal identification only.

  E. Falls within Mil—Std 1835 GDFP2—F20



#### FK (S-CQCC-N\*\*)

#### LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



#### N (R-PDIP-T\*\*)

#### PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

#### PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



### DW (R-PDSO-G20)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



#### DB (R-PDSO-G\*\*)

#### PLASTIC SMALL-OUTLINE

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

#### **MECHANICAL DATA**

#### NS (R-PDSO-G\*\*)

### 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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<u>SN74LS373DWE4 SN74LS373DWR SN74LS373DWRE4 SN74LS373NE4 SN74LS373NSR SN74LS373NSRE4</u>

<u>SN74S373DW SN74S373DWE4 SN74S373N SN74S373NE4 SN74LS373NSRG4 SN74LS374NSRG4</u>

<u>SN74LS373DWG4 SN74LS373DWRG4 SN74LS374DBRG4 SN74LS373DWG4 SN74S374N SN74S374NE4</u>