TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS038C – Revised October 2003

# CD4035B Types

## CMOS 4-Stage Parallel In/Parallel Out Shift Register

with J-$\overline{K}$ Serial Inputs and True/Complement Outputs

High-Voltage Types (20-Volt Rating)

■ CD4035B is a four-stage clocked signal serial register with provision for synchronous PARALLEL inputs to each stage and SERIAL inputs to the first stage via J$\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low).

Parallel entry into each register stage is permitted when the PARALLEL/SERIAL control is high.

In the parallel or serial mode information is transferred on positive clock transitions.

When the TRUE/COMPLEMENT control is high, the true contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with respect to the CLOCK signal.

J$\overline{K}$ input logic is provided on the first stage SERIAL input to minimize logic requirements particularly in counting and sequence-generation applications. With J$\overline{K}$ inputs connected together, the first stage becomes a D flip-flop. An asynchronous common RESET is also provided.

The CD4035B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

*Features:*

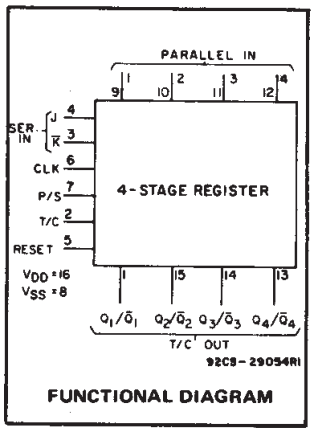
- 4-Stage clocked shift operation
- Synchronous parallel entry on all 4 stages
- J$\overline{K}$ inputs on first stage
- Asynchronous True/Complement control on all outputs
- Static flip-flop operation; Master-slave configuration
- Buffered inputs and outputs
- High speed – 12 MHz (typ.) at $V_{DD}$ = 10 V
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"

*Applications:*

- Counters, Registers
  Arithmetic-unit registers
  Shift-left – shift right registers
  Serial-to-parallel/parallel-to-serial conversions
- Sequence generation
- Control circuits
- Code conversion

FIRST STAGE TRUTH TABLE

| CL | $t_{n-1}$ (INPUTS) J | K | R | $Q_{n-1}$ | $t_n$ (OUTPUTS) $Q_n$ |
|---|---|---|---|---|---|
| ⎍ | 0 | X | 0 | 0 | 0 |
| ⎍ | 1 | X | 0 | 0 | 1 |
| ⎍ | X | 0 | 0 | 1 | 0 |
| ⎍ | 1 | 0 | 0 | $Q_{n-1}$ | $\overline{Q_{n-1}}$ TOGGLE MODE |
| ⎍ | X | 1 | 0 | 1 | 1 |
| ⎎ | X | X | 0 | $Q_{n-1}$ | $Q_{n-1}$ |
| X | X | X | 1 | X | 0 |




FUNCTIONAL DIAGRAM

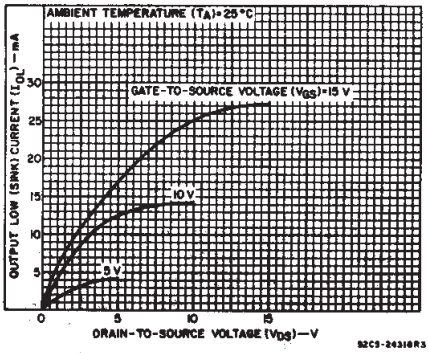



*Fig. 1 – Typical output low (sink) current characteristics.*

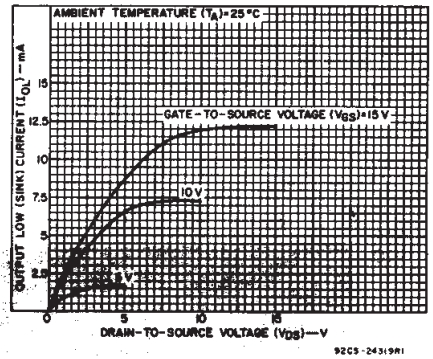



*Fig. 2 – Minimum output low (sink) current characteristics.*

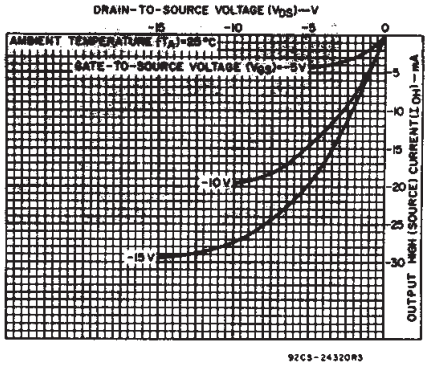



*Fig. 3 – Typical output high (source) current characteristics.*

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
(Voltages referenced to $V_{SS}$ Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -55°C to +100°C ..... 500mW
For $T_A$ = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW
OPERATING-TEMPERATURE RANGE ($T_A$) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

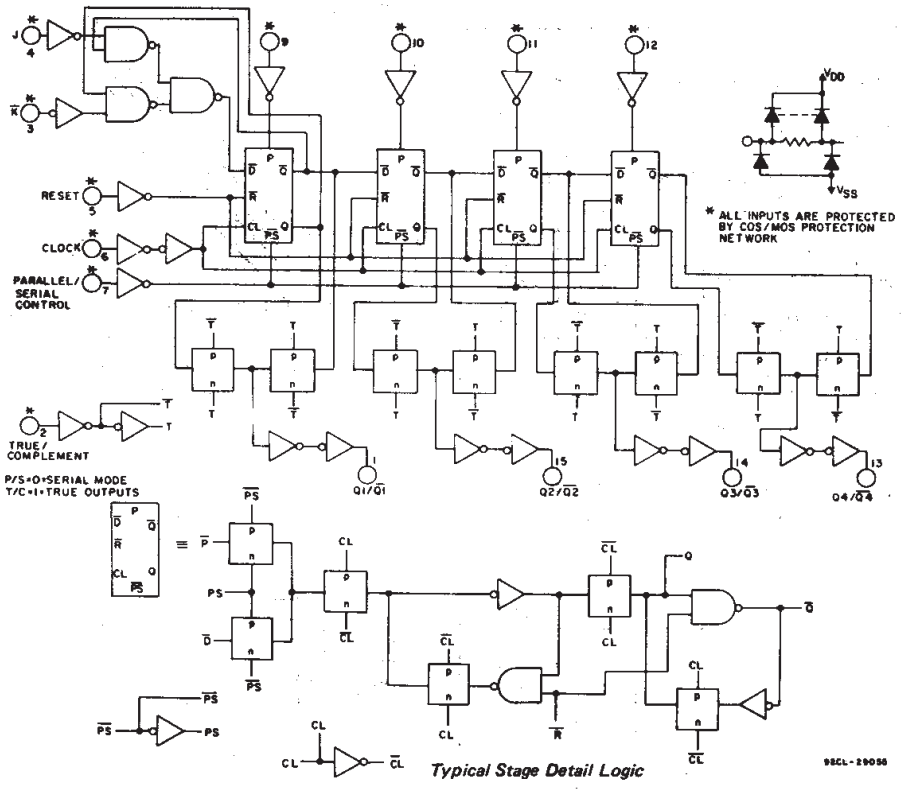



*Fig. 4 – Logic diagram.*

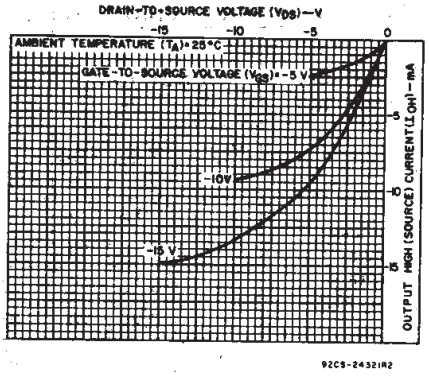



*Fig. 5 – Minimum output high (source) current characteristics.*

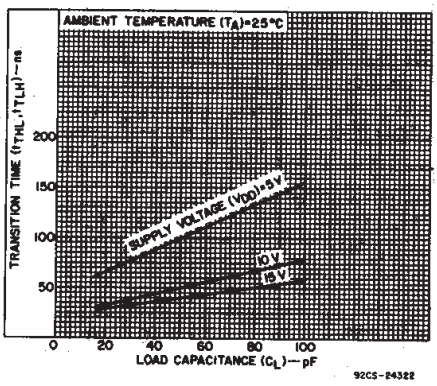



*Fig. 6 – Typical transition time as a function of load capacitance.*

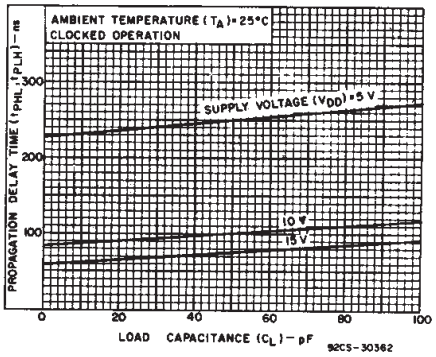



*Fig. 7 – Typical propagation delay times as a function of load capacitance (Q output).*

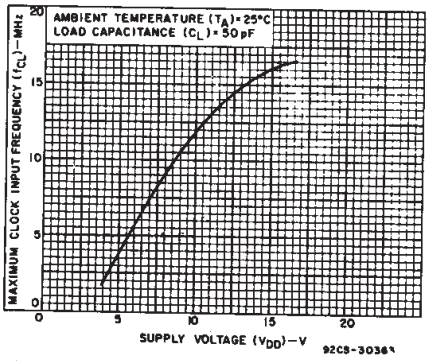



*Fig. 8 – Typical maximum clock input frequency as a function of supply voltage.*

**RECOMMENDED OPERATING CONDITIONS at $T_A$ = 25°C, Except as Noted.**
**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | $V_{DD}$ (V) | LIMITS | | UNITS |
|---|---|---|---|---|
| | | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A$ = Full Package-Temperature Range) | | 3 | 18 | V |
| Data Setup Time, $t_S$: J/$\overline{K}$ Lines | 5 | 220 | – | ns |
| | 10 | 80 | – | |
| | 15 | 60 | – | |
| Parallel-In Lines | 5 | 140 | – | ns |
| | 10 | 50 | – | |
| | 15 | 40 | – | |
| Clock Pulse Width, $t_W$ | 5 | 200 | – | ns |
| | 10 | 90 | – | |
| | 15 | 60 | – | |
| Clock Input Frequency, $f_{CL}$ | 5 | dc | 2 | MHz |
| | 10 | | 6 | |
| | 15 | | 8 | |
| Clock Rise or Fall Time, $t_rCL$, $t_fCL$: | 5 | – | 15 | μs |
| | 10 | – | 15 | |
| | 15 | – | 15 | |
| Reset Pulse Width, $t_W$ | 5 | 250 | – | ns |
| | 10 | 110 | – | |
| | 15 | 80 | – | |

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | +25 | | | |
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | −55 | −40 | +85 | +125 | Min. | Typ. | Max. | |
| Quiescent Device Current, $I_{DD}$ Max. | – | 0,5 | 5 | 5 | 5 | 150 | 150 | – | 0.04 | 5 | μA |
| | – | 0,10 | 10 | 10 | 10 | 300 | 300 | – | 0.04 | 10 | |
| | – | 0,15 | 15 | 20 | 20 | 600 | 600 | – | 0.04 | 20 | |
| | – | 0,20 | 20 | 100 | 100 | 3000 | 3000 | – | 0.08 | 100 | |
| Output Low (Sink) Current $I_{OL}$ Min. | 0.4 | 0,5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | – | mA |
| | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | – | |
| | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | – | |
| Output High (Source) Current, $I_{OH}$ Min. | 4.6 | 0,5 | 5 | −0.64 | −0.61 | −0.42 | −0.36 | −0.51 | −1 | – | |
| | 2.5 | 0,5 | 5 | −2 | −1.8 | −1.3 | −1.15 | −1.6 | −3.2 | – | |
| | 9.5 | 0,10 | 10 | −1.6 | −1.5 | −1.1 | −0.9 | −1.3 | −2.6 | – | |
| | 13.5 | 0,15 | 15 | −4.2 | −4 | −2.8 | −2.4 | −3.4 | −6.8 | – | |
| Output Voltage: Low-Level, $V_{OL}$ Max. | – | 0,5 | 5 | 0.05 | | | | – | 0 | 0.05 | V |
| | – | 0,10 | 10 | 0.05 | | | | – | 0 | 0.05 | |
| | – | 0,15 | 15 | 0.05 | | | | – | 0 | 0.05 | |
| Output Voltage: High-Level, $V_{OH}$ Min. | – | 0,5 | 5 | 4.95 | | | | 4.95 | 5 | – | |
| | | 0,10 | 10 | 9.95 | | | | 9.95 | 10 | – | |
| | | 0,15 | 15 | 14.95 | | | | 14.95 | 15 | – | |
| Input Low Voltage $V_{IL}$ Max. | 0.5,4.5 | | 5 | 1.5 | | | | – | – | 1.5 | V |
| | 1,9 | | 10 | 3 | | | | – | – | 3 | |
| | 1.5,13.5 | | 15 | 4 | | | | – | – | 4 | |
| Input High Voltage, $V_{IH}$ Min. | 0.5,4.5 | | 5 | 3.5 | | | | 3.5 | – | – | |
| | 1,9 | – | 10 | 7 | | | | 7 | – | – | |
| | 1.5,13.5 | | 15 | 11 | | | | 11 | – | – | |
| Input Current $I_{IN}$ Max. | | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | – | $±10^{-5}$ | ±0.1 | μA |

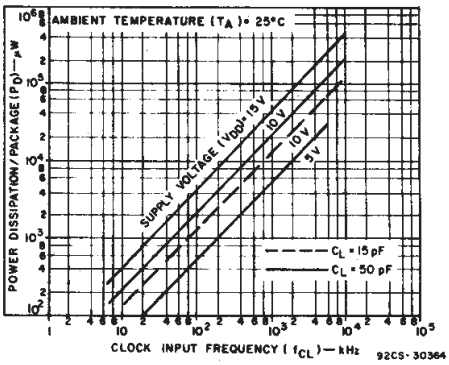



*Fig. 9 – Typical dynamic power dissipation as a function of clock input frequency.*

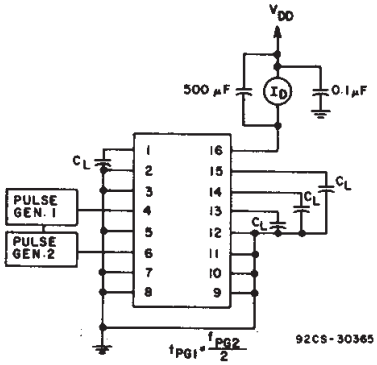



*Fig. 10 – Dynamic power dissipation test circuit.*

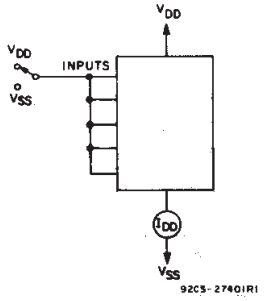



*Fig. 11 – Quiescent-device current test circuit.*

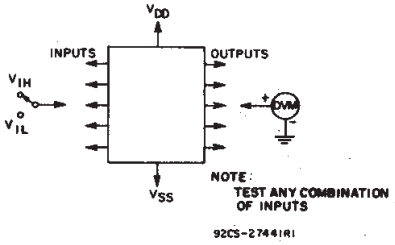



*Fig. 12 – Input-voltage test circuit.*

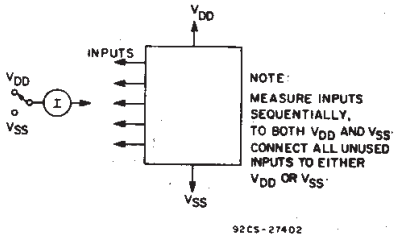



*Fig. 13 – Input-current test circuit.*

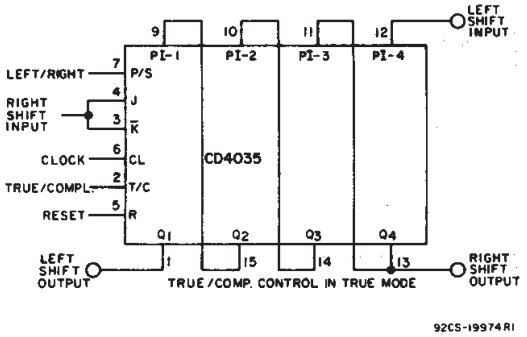
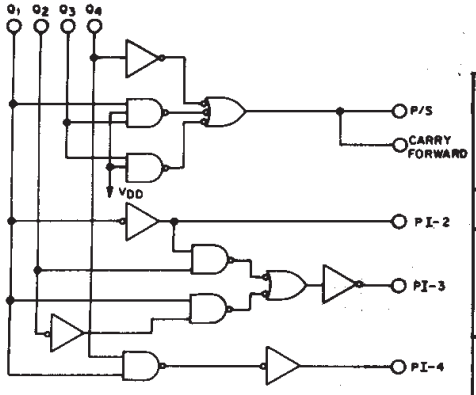



*Fig. 14 – Shift left/shift right register.*




Using Couleur's Technique (BIDEC)▲, a binary number (most significant bit, MSB) first is shifted and processed, such that the BCD equivalent is obtained when the last binary bit is clocked into the register. The CD4035B, with the correct conversion logic, can also be used as a BCD-to-binary converter.

▲The basic rule is: If a 4 or less is in a decade, shift with the next clock pulse; if a 5 or greater is in a decade, add 3 and then shift at the next clock pulse. For more information refer to "IRE TRANSACTIONS ON ELECTRONIC COMPUTERS", Dec. 1958, Pages 313–316.

*Fig. 15 – BIDEC logic.*

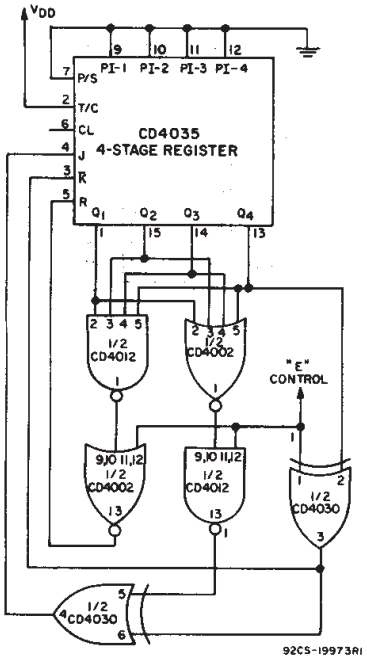



*Fig. 16(a) – Double sequence generator.*

**DYNAMIC ELECTRICAL CHARACTERISTICS**

*At $T_A$ = 25°C, Input $t_r$, $t_f$ = 20 ns, $C_L$ = 50 pF, $R_L$ = 200 kΩ*

| CHARACTERISTICS | TEST CONDITIONS $V_{DD}$ (V) | LIMITS Min. | Typ. | Max. | UNITS |
|---|---|---|---|---|---|
| **CLOCKED OPERATION** | | | | | |
| Propagation Delay Time: $t_{PHL}$, $t_{PLH}$ | 5 | – | 250 | 500 | ns |
| | 10 | – | 100 | 200 | |
| | 15 | – | 75 | 150 | |
| Transition Time: $t_{THL}$, $t_{TLH}$ | 5 | – | 100 | 200 | ns |
| | 10 | – | 50 | 100 | |
| | 15 | – | 40 | 80 | |
| Minimum Clock Pulse Width, $t_W$ | 5 | – | 100 | 200 | ns |
| | 10 | – | 45 | 90 | |
| | 15 | – | 30 | 60 | |
| Clock Rise or Fall Time, $t_rCL$, $t_fCL$* | 5,10, 15 | – | – | 15 | μs |
| Minimum Setup Time: J/$\overline{K}$ Lines | 5 | – | 110 | 220 | ns |
| | 10 | – | 40 | 80 | |
| | 15 | – | 30 | 60 | |
| Parallel-In-Lines | 5 | – | 70 | 140 | ns |
| | 10 | – | 25 | 50 | |
| | 15 | – | 20 | 40 | |
| Maximum Clock Frequency, $f_{CL}$ | 5 | 2 | 4 | – | MHz |
| | 10 | 6 | 12 | – | |
| | 15 | 8 | 16 | – | |
| Input Capacitance, $C_{IN}$ | Any Input | – | 5 | 7.5 | pF |
| **RESET OPERATION** | | | | | |
| Propagation Delay Time: $t_{PHL}$, $t_{PLH}$ | 5 | – | 230 | 460 | ns |
| | 10 | – | 100 | 200 | |
| | 15 | – | 80 | 160 | |
| Minimum Reset Pulse Width, $t_W$ | 5 | – | 125 | 250 | ns |
| | 10 | – | 55 | 110 | |
| | 15 | – | 40 | 40 | |

*If more than one unit is cascaded $t_rCL$ should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

| Control = E = | 0 | | | | 1 | | | |
|---|---|---|---|---|---|---|---|---|
| | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ |
| | A | B | C | D | A | B | C | D |
| 0 | 0 | 0 | 0 | 0 | 15 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 14 | 0 | 1 | 1 |
| 2 | 0 | 1 | 0 | 0 | 13 | 1 | 0 | 1 |
| 5 | 1 | 0 | 1 | 0 | 10 | 0 | 1 | 0 |
| 10 | 0 | 1 | 0 | 1 | 5 | 1 | 0 | 1 |
| 4 | 0 | 0 | 1 | 0 | 11 | 1 | 1 | 0 |
| 9 | 1 | 0 | 0 | 1 | 6 | 0 | 1 | 1 |
| 3 | 1 | 1 | 0 | 0 | 12 | 0 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 | 9 | 1 | 0 | 0 |
| 13 | 1 | 0 | 1 | 1 | 2 | 0 | 1 | 0 |
| 11 | 1 | 1 | 0 | 1 | 4 | 0 | 0 | 1 |
| 7 | 1 | 1 | 1 | 0 | 8 | 0 | 0 | 0 |
| 14 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 12 | 0 | 0 | 1 | 1 | 3 | 1 | 1 | 0 |
| 8 | 0 | 0 | 0 | 1 | 7 | 1 | 1 | 1 |

Using a control line (E) two different state sequences can be generated. For example, suppose the following two sequences are desired on command (control line E)

*Fig. 16(b) – State sequences.*

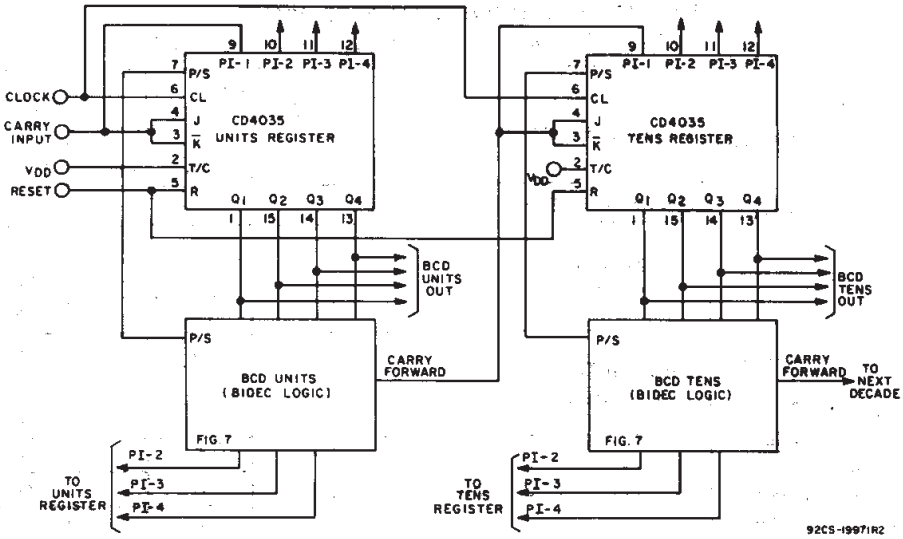
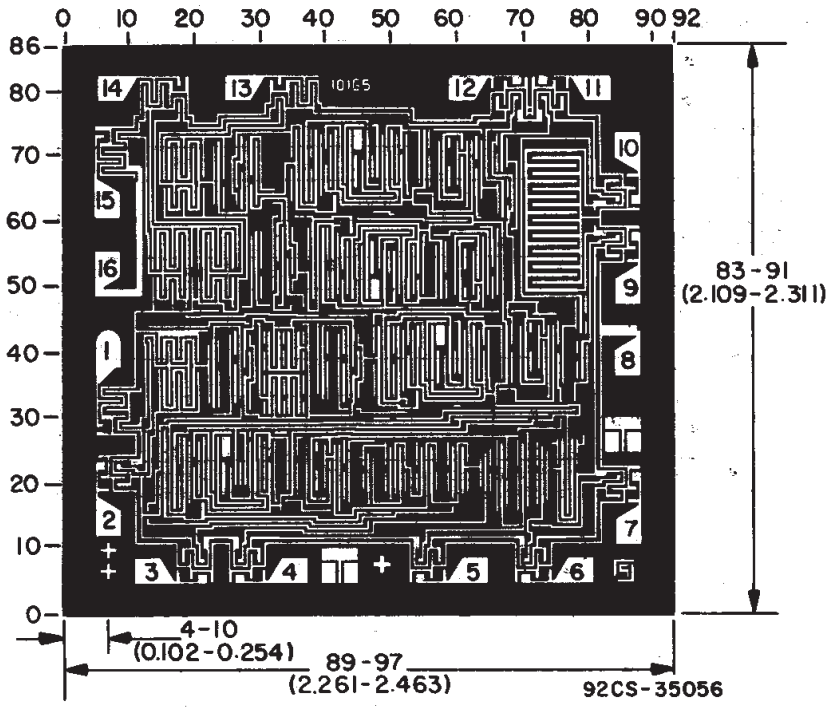
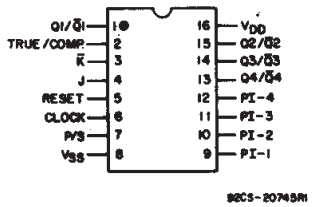



*Fig. 17 — Binary-to-BCD converter.*




**TERMINAL DIAGRAM**
**Top View**




*Dimensions and pad layout for CD4035BH.*

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).*

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| 8101701EA | ACTIVE | CDIP | J | 16 | 1 | None | Call TI | Level-NC-NC-NC |
| CD4035BE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| CD4035BF | ACTIVE | CDIP | J | 16 | 1 | None | Call TI | Level-NC-NC-NC |
| CD4035BF3A | ACTIVE | CDIP | J | 16 | 1 | None | Call TI | Level-NC-NC-NC |
| CD4035BM | ACTIVE | SOIC | D | 16 | 40 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4035BM96 | ACTIVE | SOIC | D | 16 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4035BMT | ACTIVE | SOIC | D | 16 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4035BNSR | ACTIVE | SO | NS | 16 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4035BPW | ACTIVE | TSSOP | PW | 16 | 90 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| CD4035BPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

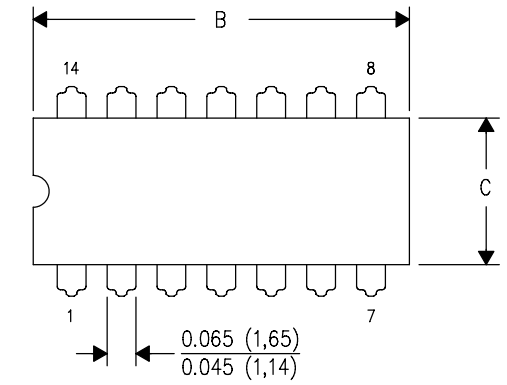
[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**None:** Not yet available Lead (Pb-Free).
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

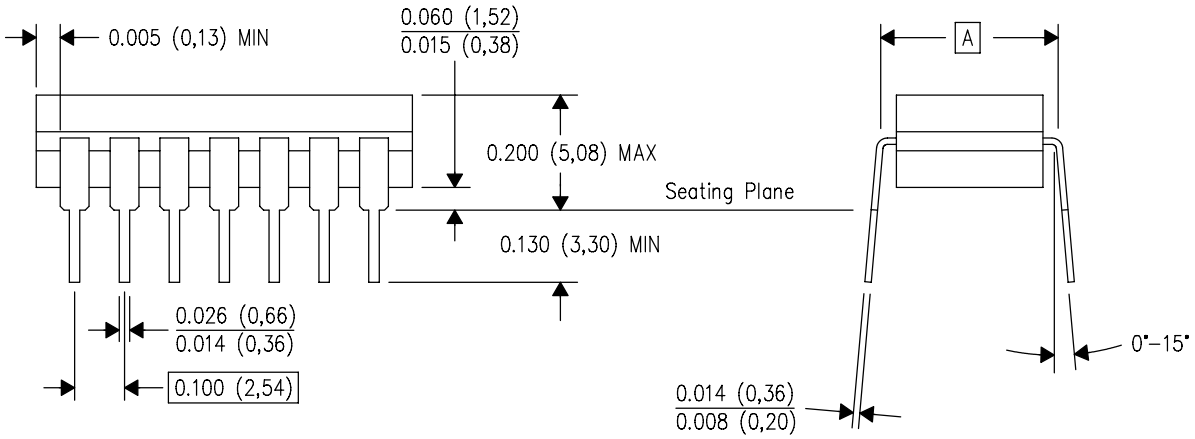
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



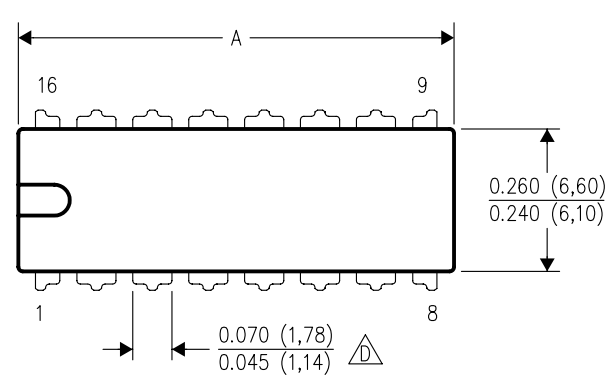

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

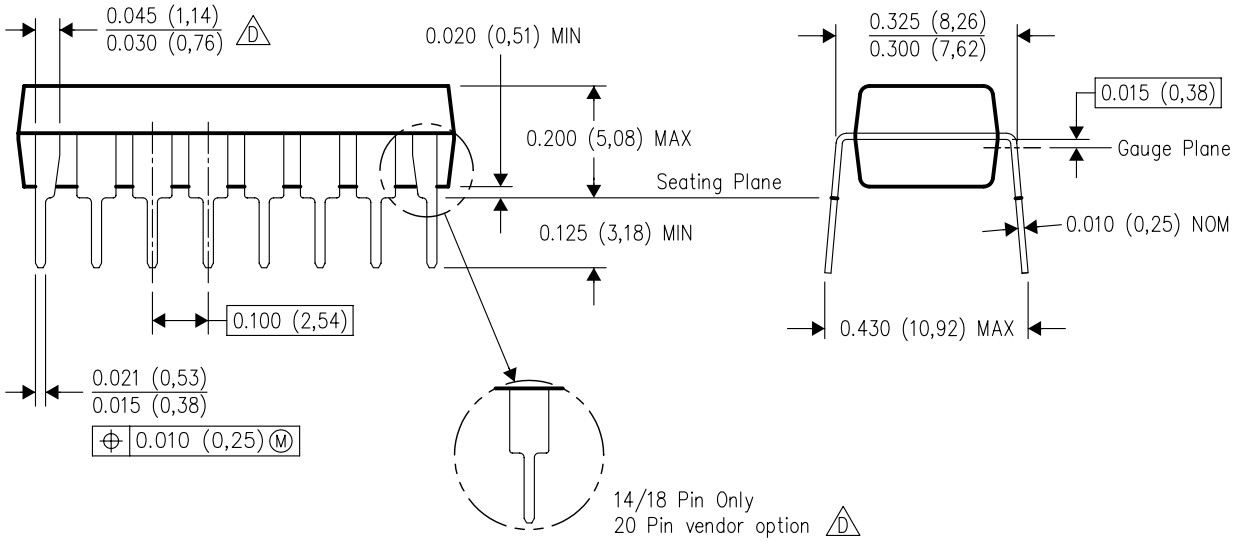
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



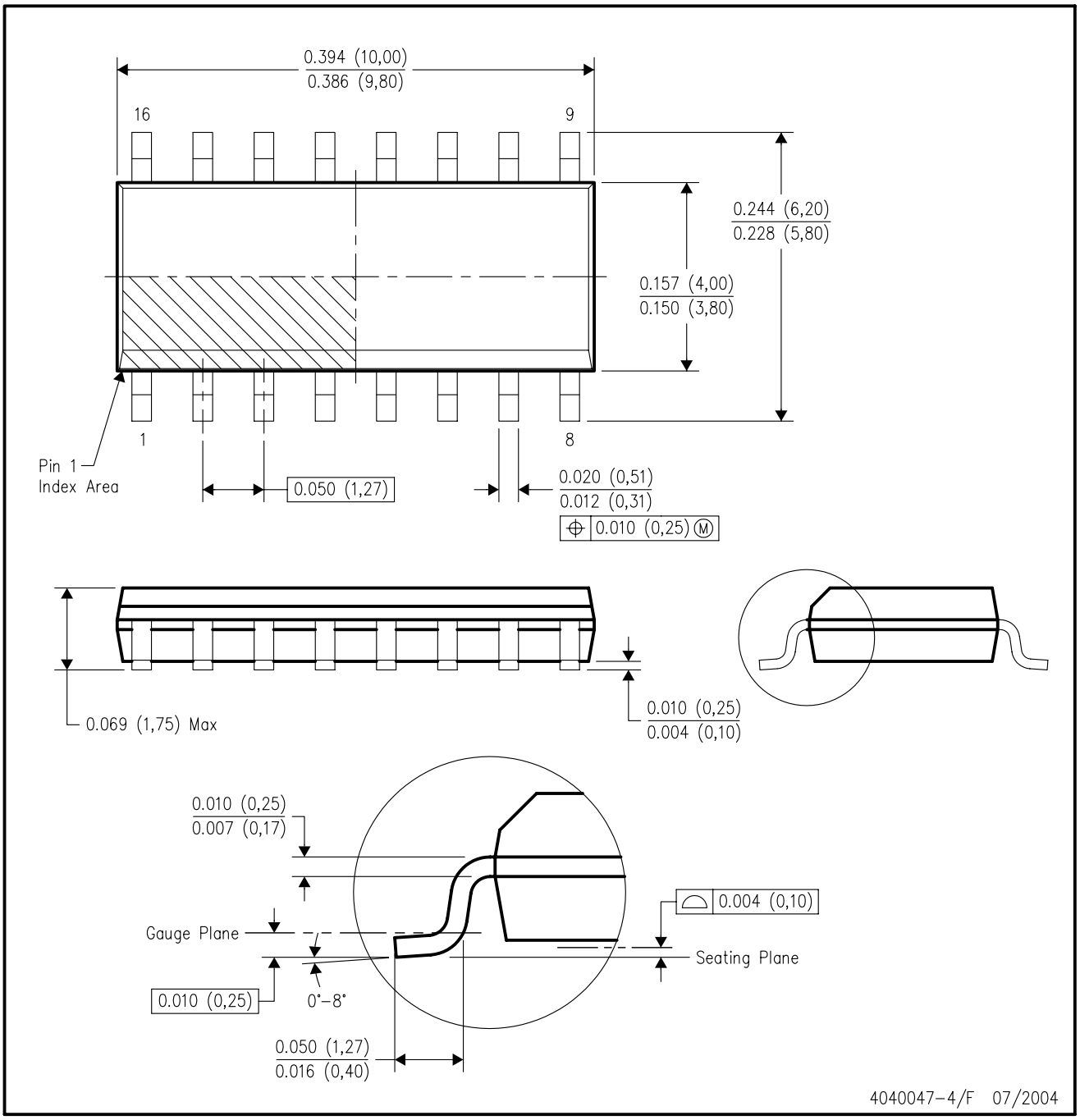

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE

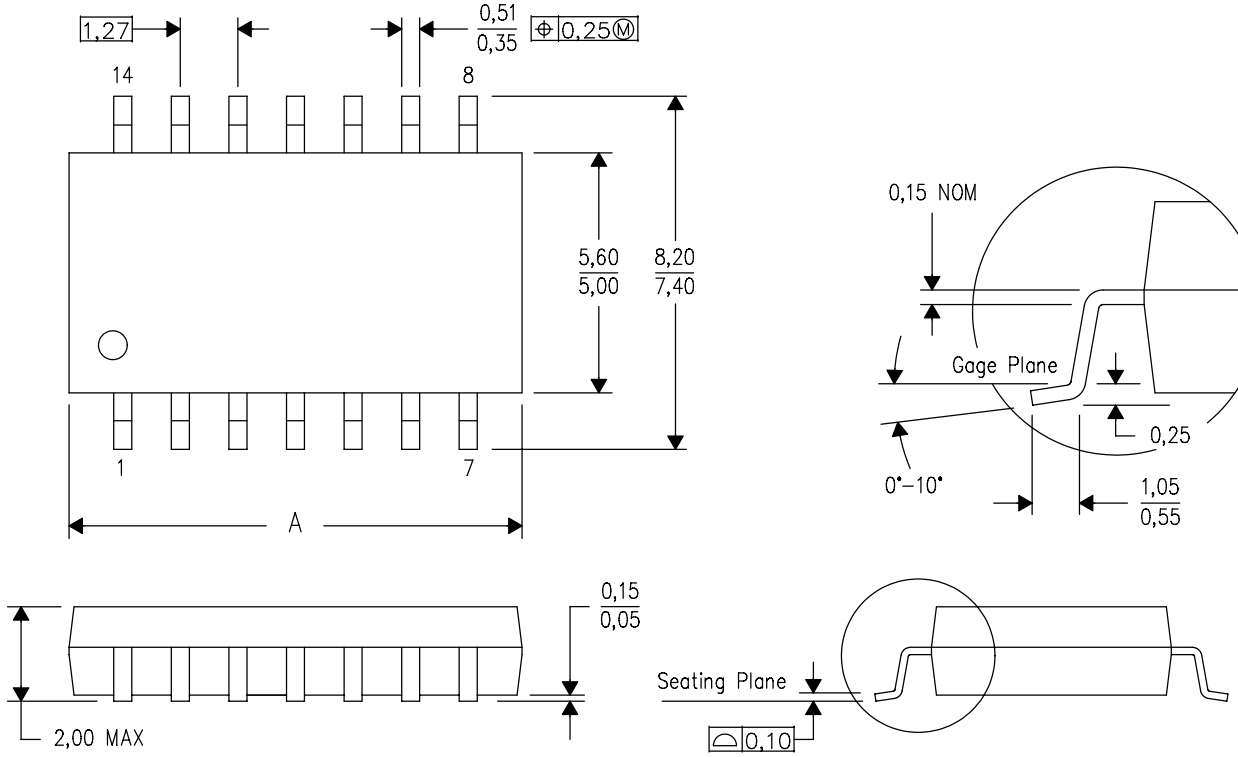



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AC.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



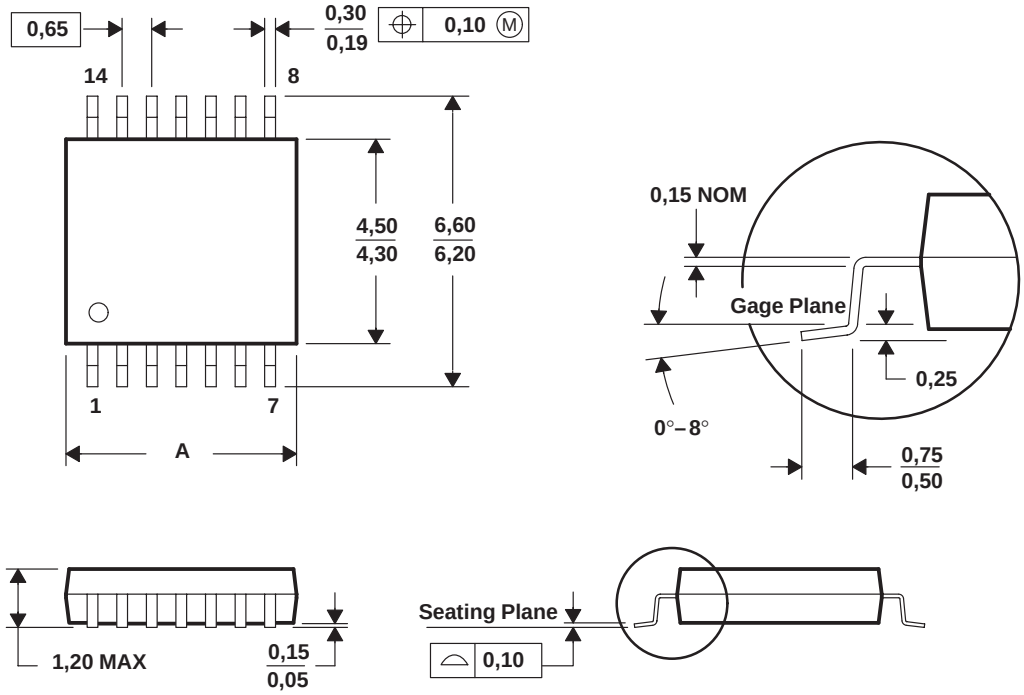

| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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CD4035BF3A - http://www.ti.com/product/cd4035bf3a?HQS=TI-null-null-dscatalog-df-pf-null-wwe

CD4035BNSR - http://www.ti.com/product/cd4035bnsr?HQS=TI-null-null-dscatalog-df-pf-null-wwe

CD4035BPW - http://www.ti.com/product/cd4035bpw?HQS=TI-null-null-dscatalog-df-pf-null-wwe

CD4035BPWR - http://www.ti.com/product/cd4035bpwr?HQS=TI-null-null-dscatalog-df-pf-null-wwe

CD4035B - http://www.ti.com/product/cd4035b?HQS=TI-null-null-dscatalog-df-pf-null-wwe

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CD4035BF - http://www.ti.com/product/cd4035bf?HQS=TI-null-null-dscatalog-df-pf-null-wwe

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