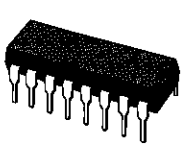
SGS-THOMSON MICROELECTRONICS

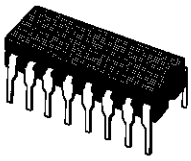
HCC/HCF4031B

64-STAGE STATIC SHIFT REGISTER

- FULLY STATIC OPERATION : DC to 16MHz (TYP.) @ $V_{DD} - V_{SS} = 15V$
- STANDARD TTL DRIVE CAPABILITY ON Q OUTPUT
- RECIRCULATION CAPABILITY
- THREE CASCADING MODES :
  DIRECT CLOCKING FOR HIGH-SPEED OPERATION
  DELAYED CLOCKING FOR REDUCED CLOCK DRIVE REQUIREMENTS
  ADDITIONAL 1/2 STAGE FOR SLOW CLOCKS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA at 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



EY
(Plastic Package)



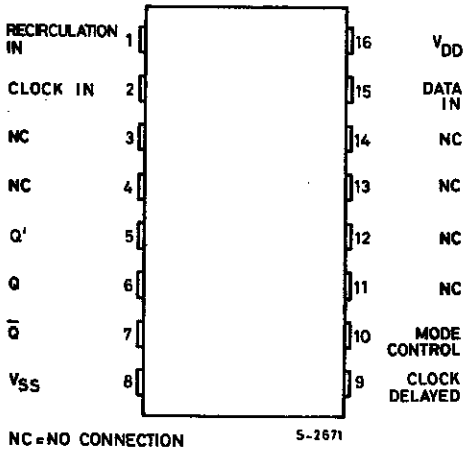
F
(Ceramic Package)

C1
(Chip Carrier)

ORDER CODES :

HCC4031BF HCF4031BEY
HCF4031BC1

PIN CONNECTIONS



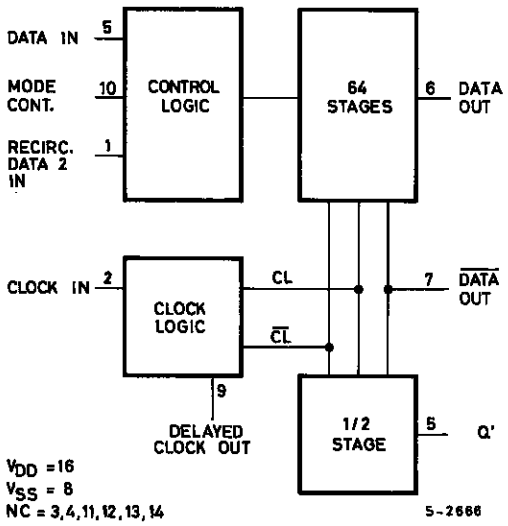
DESCRIPTION

The **HCC4031B** (extended temperature range) and **HCF4031B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package.

The **HCC/HCF4031B** is a static shift register that contains 64 D-type, master-slave flip-flop stages and one stage which is a D-type master flip-flop only (referred to as a 1/2 stage). The logic level present at the DATA input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 16 Megahertz (typical) can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the low or high state. The **HCC/HCF4031B** has a MODE CONTROL input that, when in the high state, allows operation in the recirculating mode. The MODE CONTROL input can also be used to select between two separate data sources. Register packages can be cascaded and the clock lines driven directly for high-speed operation. Alternatively, a delayed clock output (CL_D) is provided that enables cascading reg-

ister packages while allowing reduced clock drive fan-out and transition-time requirements. A third cascading option makes use of the Q' output from the 1/2 stage, which is available on the next negative-going transition of the clock after the Q output occurs. This delayed output, like the delayed clock CL_D, is used with clocks having slow rise and fall times.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}*	Supply Voltage : **HCC** Types **HCF** Types	– 0.5 to + 20 – 0.5 to + 18	V V
V_I	Input Voltage	– 0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for T_{op} = Full Package-temperature Range	200 100	mW mW
T_{op}	Operating Temperature : **HCC** Types **HCF** Types	– 55 to + 125 – 40 to + 85	°C °C
T_{stg}	Storage Temperature	– 65 to + 150	°C

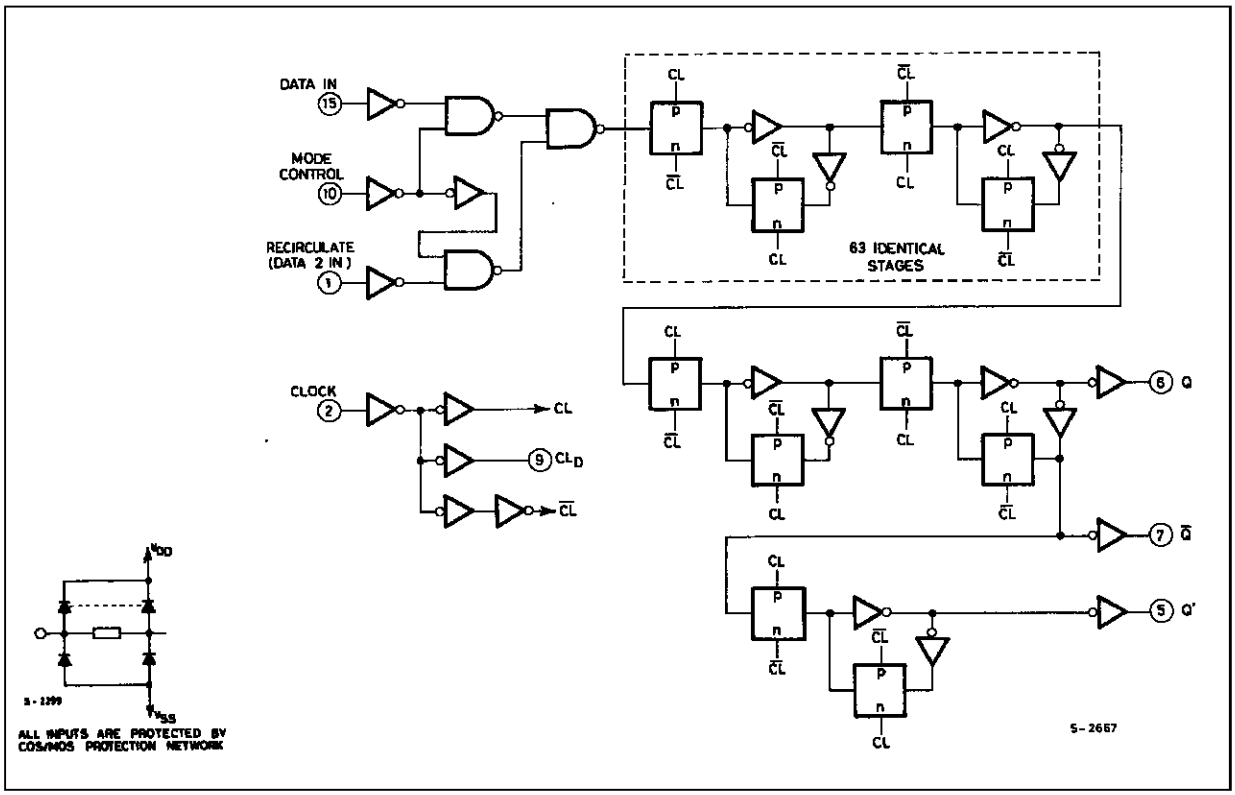
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage : **HCC** Types **HCF** Types	3 to + 18 3 to + 15	V V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature : **HCC** Types **HCF** Types	– 55 to + 125 – 40 to + 85	°C °C

LOGIC DIAGRAM AND TRUTH TABLES



INPUT CONTROL CIRCUIT

Data	Recirc.	Mode	Bit Into Stage 1
1	X	0	1
0	X	0	0
X	1	1	1
X	0	1	0

TYPICAL STAGE

Data	CL	Data + 1
0	_/‾	0
1	_/‾	1
X	‾_	NC

1 = HIGH LEVEL 0 = LOW LEVEL
X = DON'T CARE

OUTPUT FROM Q' (pin 5)

Data + 64	CL	Data + 64.5
0	‾_	0
1	‾_	1
X	_/‾	NC

NC = NO CHANGE

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter		Test Conditions V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	Value T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	Unit
I_L	Quiescent Current	HCC Types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF Types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output High Voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output Low Voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input High Voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input Low Voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output Source Current (Source) Q, $\overline{Q}$, Q CL_D	HCC Types	0/ 5	2.5		5	– 2		– 1.6	– 3.2		– 1.15		mA
			0/ 5	4.6		5	– 0.64		– 0.51	– 1		– 0.36		
			0/10	9.5		10	– 1.6		– 1.3	– 2.6		– 0.9		
			0/15	13.5		15	– 4.2		– 3.4	– 6.8		– 2.4		
		HCF Types	0/ 5	2.5		5	– 1.53		– 1.36	– 3.2		– 1.1		
			0/ 5	4.6		5	– 0.52		– 0.44	– 1		– 0.36		
			0/10	9.5		10	– 1.3		– 1.1	– 2.6		– 0.9		
			0/15	13.5		15	– 3.6		– 3.0	– 6.8		– 2.4		
I_{OL}	Output Sink Current Q	HCC Types	0/ 5	0.4		5	2.56		2.04	4		1.44		mA
			0/10	0.5		10	6.4		5.2	10.4		3.6		
			0/15	1.5		15	16.8		13.6	27.2		9.6		
		HCF Types	0/ 5	0.4		5	2.08		1.74	4		1.43		
			0/10	0.5		10	5.01		4.42	10.4		3.74		
			0/15	1.5		15	13.6		11.56	27.2		9.52		
I_{OL}	Output Sink Current $\overline{Q}$, Q' CL_D	HCC Types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF Types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input Leakage Current	HCC Types	0/18	Any Input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μA
		HCF Types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	
C_I	Input Capacitance			Any Input						5	7.5			pF

* T_{Low} = – 55°C for **HCC** device : – 40°C for **HCF** device.
* T_{High} = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with V_{DD} = 5V, 2V min. with V_{DD} = 10V, 2.5 V min. with V_{DD} = 15V.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20ns)

Symbol	Parameter	Test Conditions		Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH}, t_{PLH}	Propagation Delay Time : Clock to $\overline{Q}$, Clock to Q		5		250	500	ns
			10		110	220	
			15		90	180	
t_{PHL}, t_{PLH}, t_{PHL}	Propagation Delay Time : Clock to Q' Clock to Q		5		190	380	ns
			10		80	160	
			15		65	130	
	Clock to CL_D		5		100	200	ns
			10		50	100	
			15		40	80	
$t_{THL'}$, t_{TLH}	Transition Time : (any output, except Qt_{THL})		5		100	200	ns
			10		50	100	
			15		40	80	
t_{THL}	Q,		5		50	100	ns
			10		25	50	
			15		20	40	
t_{setup}	Data Setup Time		5		30	60	ns
			10		15	30	
			15		10	20	
t_{hold}	Data Hold Time		5		30	60	ns
			10		15	30	
			15		10	20	
t_W	Clock Pulse Width		5		120	240	ns
			10		50	100	
			15		40	80	
f_{max}	Maximum Clock Input Frequency**		5	2	4		MHz
			10	5	10		
			15	6	12		
t_r, t_f	Clock Input Rise or Fall Time*		5			1000	µs
			10			1000	
			15			200	

* If more than one unit is cascaded in the parallel clocked application, trCL should be made less than or equal to the sum of the propagation delay at 50pF and the transmition time of the output driving stage.

* * Maximum Clock Frequency for Cascaded Units;

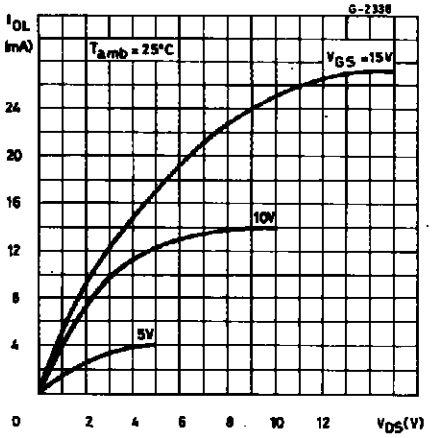
a) Using Delayed Clock Feature in Recirculation Mode :

$$fmax = \frac{1}{(n-1)\ \text{CLD prop. delay} + \text{Q prop. delay} + \text{set-up time}}$$ where n = nimber of packages

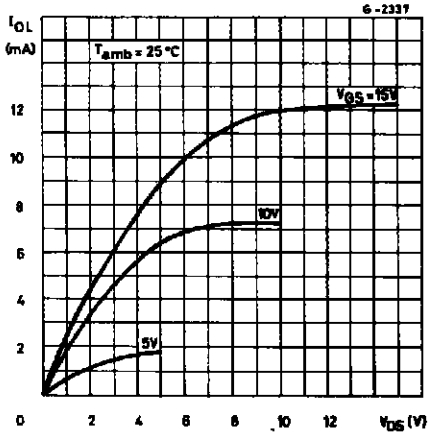
b) Not Usng Delaye Clock :

$$fmax = \frac{1}{\text{propagation delay} + \text{set-up time}}$$

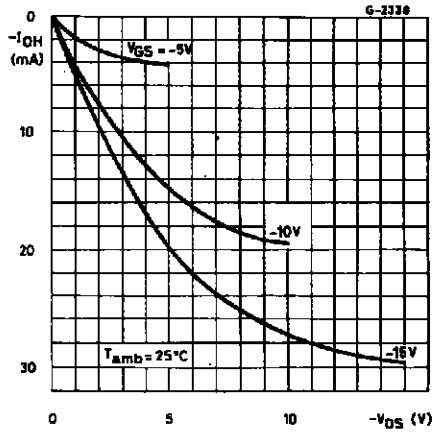
Typical Output Low (sink) Current Characteristics.



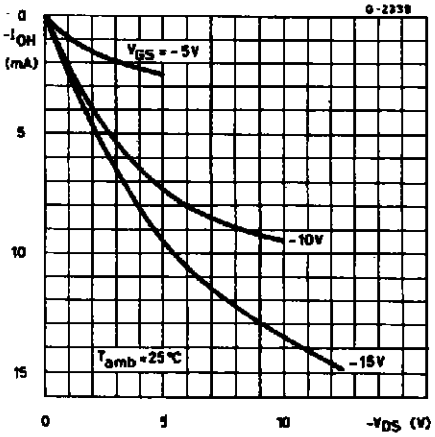
Minimum Output Low (sink) Current Characteristics.



Typical Output High (source) Current Characteristics.

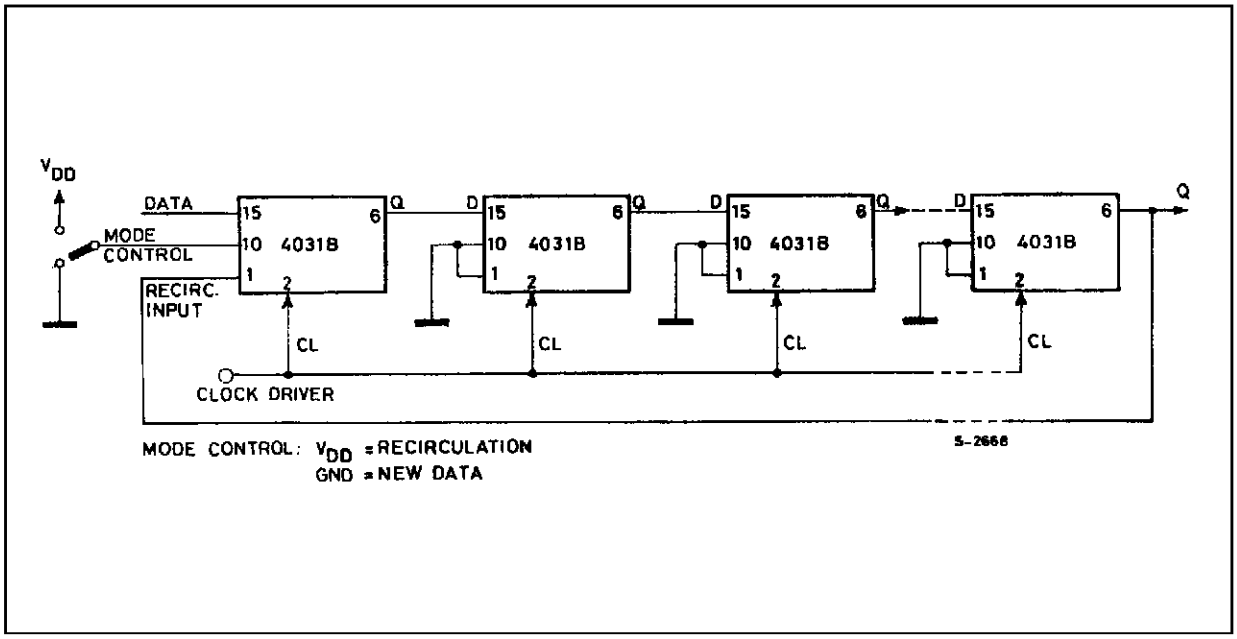


Minimum Output High (source) Current Characteristics.

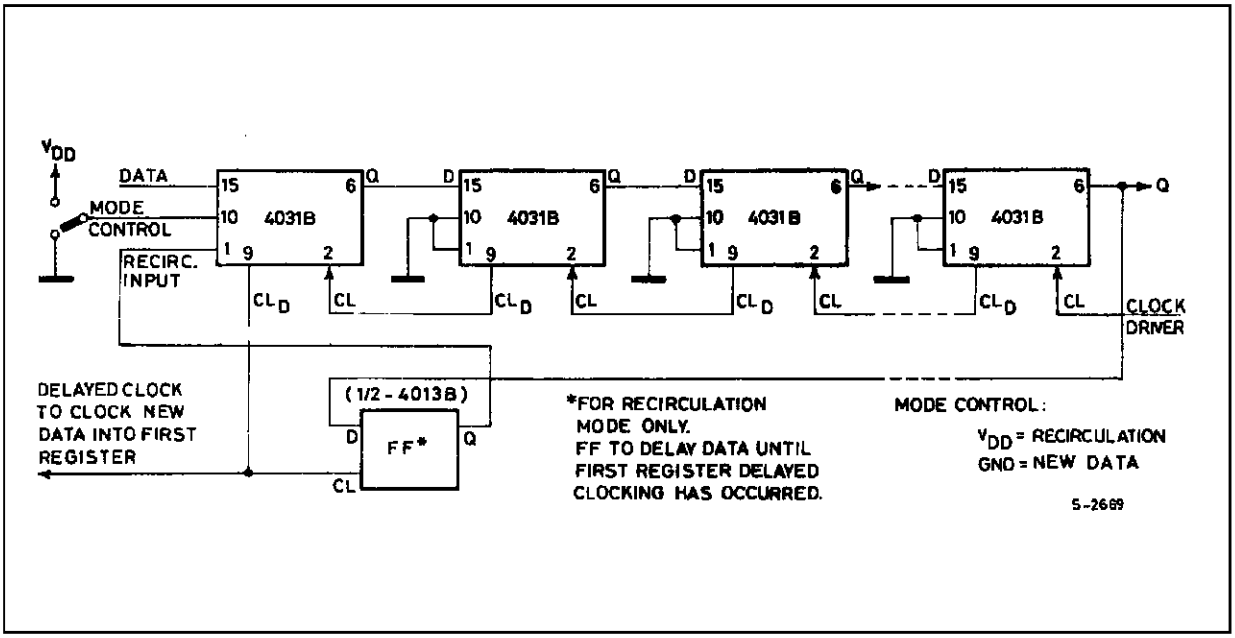


TYPICAL APPLICATIONS

CASCADING USING DIRECT CLOCKING FOR HIGH SPEED OPERATION (SEE CLOCK RISE AND FALL TIME REQUIREMENT).

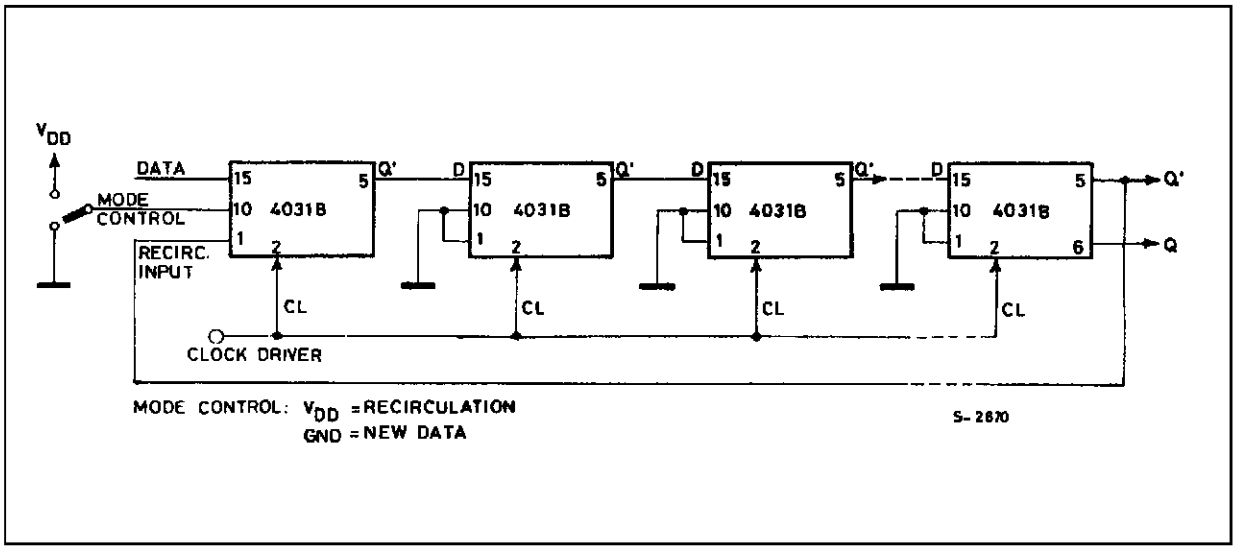


CASCADING USING DELAYED CLOCKING FOR REDUCED CLOCK DRIVE REQUIREMENTS.



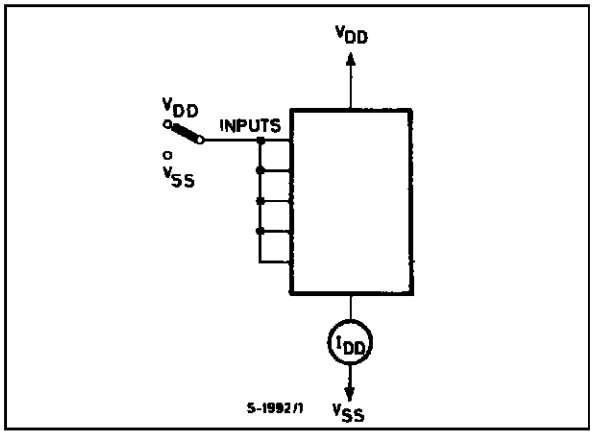
TYPICAL APPLICATIONS (continued)

CASCADING USING HALF- CLOCK-PULSE DELAYED DATA OUTPUT (Q') TO PERMIT USE OF SLOW RISE AND FALL TIME CLOCK INPUTS.

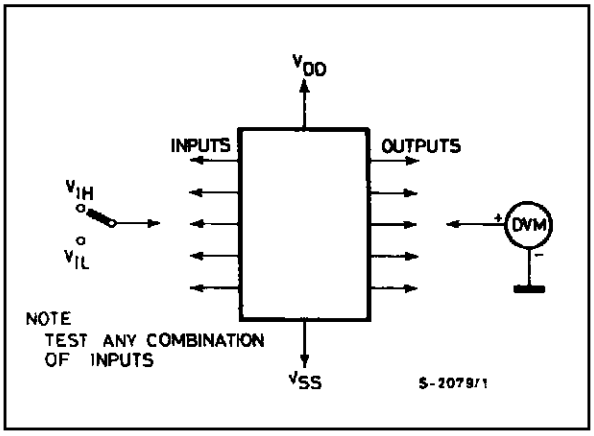


TEST CIRCUITS

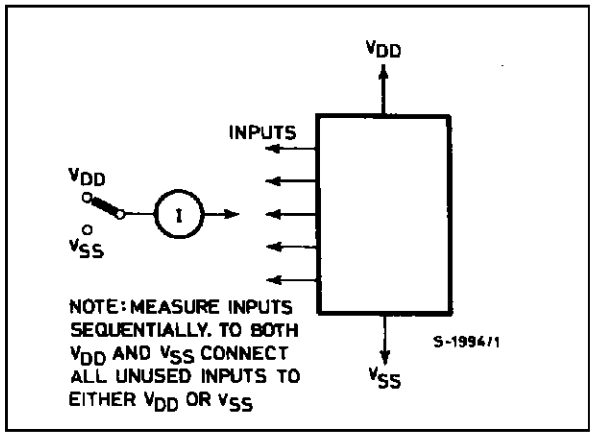
Quiescent Device Current.



Noise Immunity.

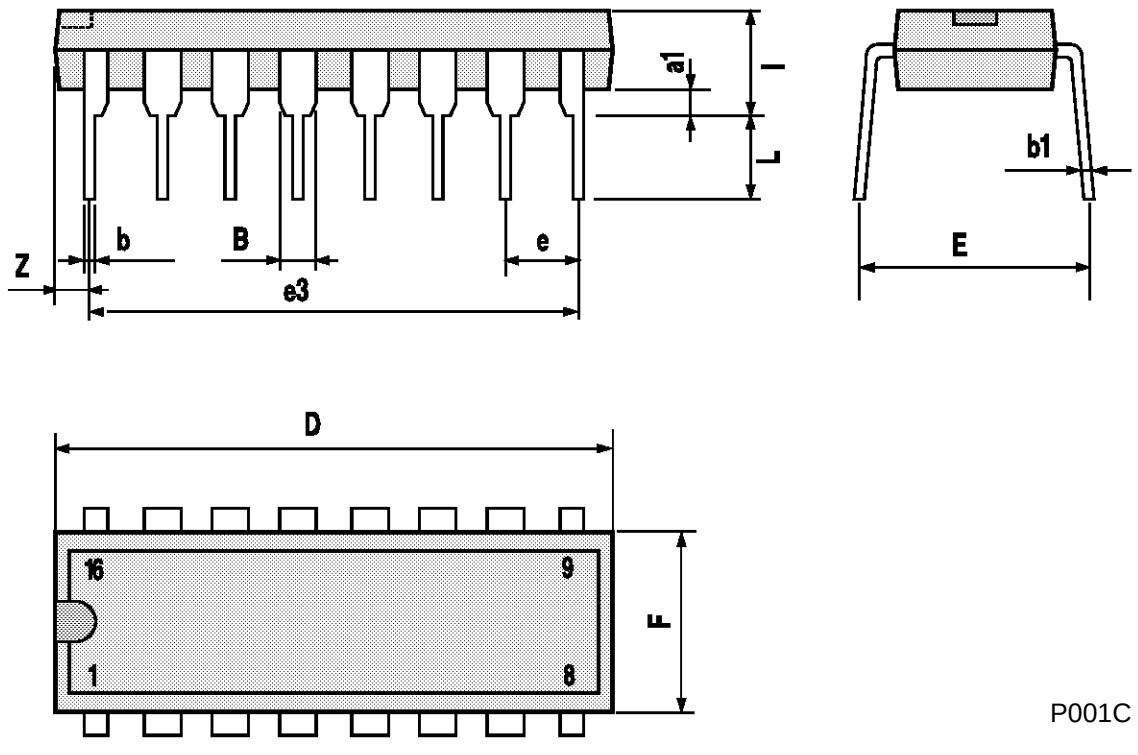


Input Leakage Current.



Plastic DIP16 (0.25) MECHANICAL DATA

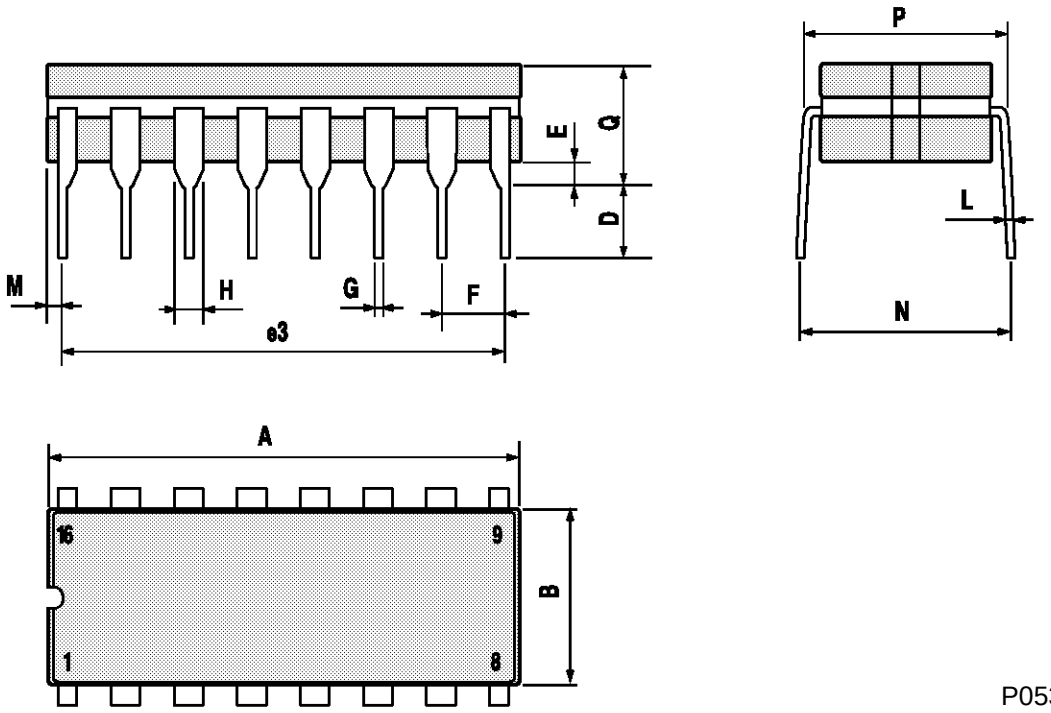
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

Ceramic DIP16/1 MECHANICAL DATA

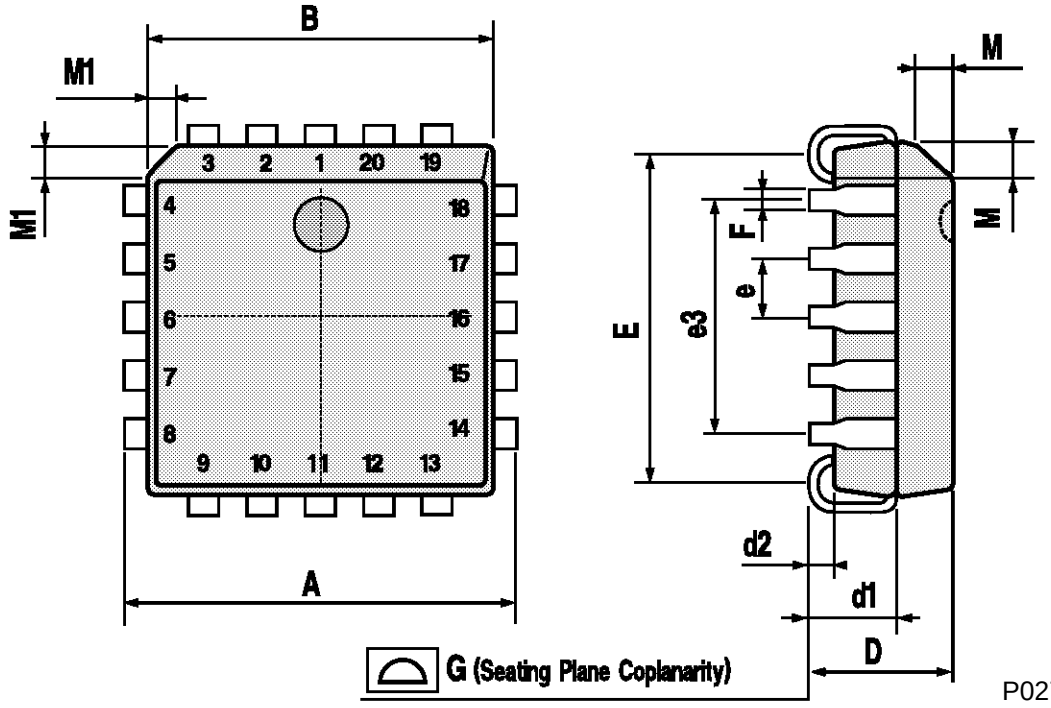
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



P053D

PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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