CD4067BMS
CD4097BMS

CMOS Analog Multiplexers/Demultiplexers

December 1992

Features

- **High Voltage Types (20V Rating)**
- **CD4067BMS Single 16 Channel Multiplexer/Demultiplexer**
- **CD4097BMS Differential 8 Channel Multiplexer/Demultiplexer**
- **Low ON Resistance: 125Ω (typ) Over 15Vp-p Signal Input Range for VDD - VSS = 15V**
- **High OFF Resistance: Channel Leakage of ±10pA (typ) at VDD - VSS = 18V**
- **Matched Switch Characteristics: RON = 5Ω (typ) for VDD - VSS = 15V**
- **Very Low Quiescent Power Dissipation Under All Digital Control Input and Supply Conditions: 0.2μW (typ) at VDD - VSS = 10V**
- **Binary Address Decoding on Chip**
- **5V, 10V and 15V Parametric Ratings**
- **100% Tested for Quiescent Current at 20V**
- **Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C**
- **Standardized Symmetrical Output Characteristics**

Applications

- **Analog and Digital Multiplexing and Demultiplexing**
- **A/D and D/A Conversion**
- **Signal Gating**

* When these devices are used as demultiplexers the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminals are the inputs.

Description

CD4067BMS and CD4097BMS CMOS analog multiplexers/demultiplexers* are digitally controlled analog switches having low ON Impedance, low OFF leakage current, and internal address decoding. In addition, the ON resistance is relatively constant over the full input-signal range.

The CD4067BMS is a 16 channel multiplexer with four binary control inputs, A, B, C, D and an inhibit input, arranged so that any combination of the inputs selects one switch.

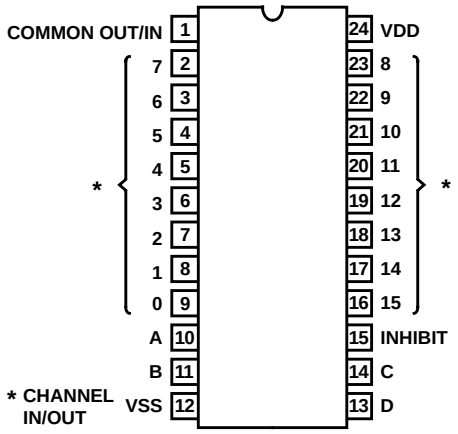
The CD4097BMS is a differential 8 channel multiplexer having three binary control inputs A, B, C and an inhibit input. The inputs permit selection of one of eight pairs of switches. A logic "1" present at the inhibit input turns all channels off.

The CD4067BMS and CD4097BMS are supplied in these 24 lead outline packages:

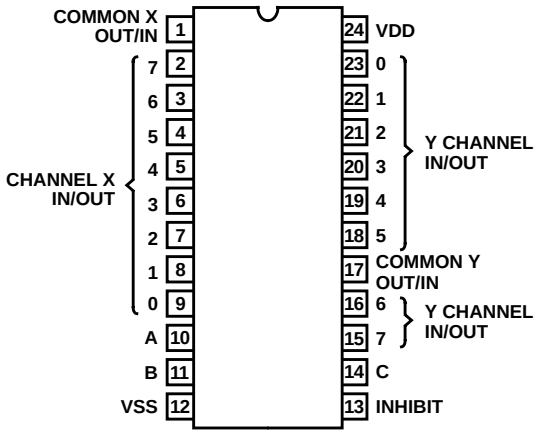
Braze Seal DIP	*H4V	†H6M
Frit Seal DIP	*H1Z	†HFN
Ceramic Flatpack	*H4P	†H4P
*CD4067B Only	†CD4097B	

Pinout

CD4067BMS
TOP VIEW



CD4097BMS
TOP VIEW



File Number **3190**

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Operating Temperature Range . . . . . -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . . +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) . . . . . Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
ON-State Resistance RL = 10K Returned to VDD - VSS/2	RON	VDD = 5V VIS = VSS to VDD		1	+25°C	-	1050	Ω
				2	+125°C	-	1300	Ω
				3	-55°C	-	800	Ω
		VDD = 10V VIS = VSS to VDD		1	+25°C	-	400	Ω
				2	+125°C	-	500	Ω
				3	-55°C	-	310	Ω
		VDD = 15V VIS = VSS to VDD		1	+25°C	-	240	Ω
				2	+125°C	-	320	Ω
				3	-55°C	-	220	Ω
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional (Note 4)	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V = VIS Thru 1K VEE = VSS RL = 1K to VSS |ISS| < 2µA on all OFF Channels		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH			1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V = VIS Thru 1K VEE = VSS RL = 1K to VSS |ISS| < 2µA on all OFF Channels		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH			1, 2, 3	+25°C, +125°C, -55°C	11	-	V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
OFF Channel Leakage Any Channel OFF or All Channels OFF (Common OUT/IN)	IOZL	VOUT = 0V	VDD = 20V	1	+25°C	-0.1	-	µA
				2	+125°C	-1.0	-	µA
			VDD = 18V	3	-55°C	-0.1	-	µA
	IOZH	VOUT = VDD	VDD = 20V	1	+25°C	-	0.1	µA
				2	+125°C	-	1.0	µA
			VDD = 18V	3	-55°C	-	0.1	µA

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.
4. VDD = 2.8/3.0V, RL = 200K
   VDD = 20V/18V, RL = 10K - 25K

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay (Signal In to Output)	TPHL TPLH	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	60	ns
			10, 11	+125°C, -55°C	-	81	ns
Propagation Delay Address or Inhibit to Signal Out. (Channel Turning On)	TPZH TPZL	VDD = 5V, VIN = VDD or GND (Notes 2, 3)	9	+25°C	-	650	ns
			10, 11	+125°C, -55°C	-	878	ns

NOTES:
1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
3. CL = 50pF, RL = 10K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS		NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND		1, 2	-55°C, +25°C	-	5	µA
					+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND		1, 2	-55°C, +25°C	-	10	µA
					+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND		1, 2	-55°C, +25°C	-	10	µA
					+125°C	-	600	µA
Input Voltage Low	VIL	VDD = VIS = 10V VEE = VSS RL = 1K to VSS IIS < 2µA ON OFF Channel		1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH			1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Address or Inhibit to Signal Out. (Channel Turning On)	TPZH TPZL	VDD = 10V		1, 2, 4	+25°C	-	270	ns
		VDD = 15V		1, 2, 4	+25°C	-	190	ns
Propagation Delay Signal In to Output	TPHL TPLH	VDD = 10V	VIS = VDD or GND	1, 2, 3	+25°C	-	30	ns
		VDD = 15V		1, 2, 3	+25°C	-	20	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Address or Inhibit to Signal Out (Channel Turning Off)	TPHZ TPLZ	VDD = 5V	1, 2, 5	+25°C	-	440	ns
		VDD = 10V	1, 2, 5	+25°C	-	180	ns
		VDD = 15V	1, 2, 5	+25°C	-	130	ns
Input Capacitance	CIN	Any Address or Inhibit	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 10K, Input TR, TF < 20ns.
5. CL = 50pF, RL = 300Ω, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
ON Resistance	RONDEL10	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

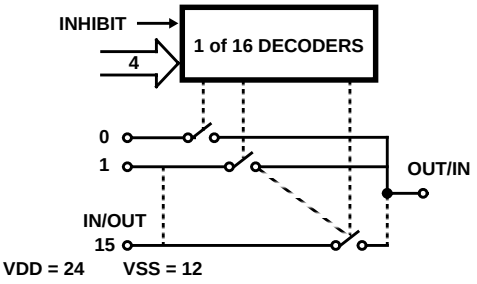
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER CD4067BMS						
Static Burn-In 1 Note 1	1	2 - 23	24			
Static Burn-In 2 Note 1	1	12	2 - 11, 13 - 24			
Dynamic Burn-In Note 1	-	12, 15	24	1	2 - 9, 16 - 23	10, 11, 13, 14 (Note 3)
Irradiation Note 2	1	12	2 - 11, 13 - 24			
PART NUMBER CD4097BMS						
Static Burn-In 1 Note 1	1, 17	2 - 16, 18 - 23	24			
Static Burn-In 2 Note 1	1, 17	12	2 - 11, 13 - 16, 18 - 24			
Dynamic Burn-In Note 1	-	12, 13	24	1, 17	2 - 9, 15, 16, 18 - 23	10, 11, 14 (Note 4)
Irradiation Note 2	1, 17	12	2 - 11, 13 - 16, 18 - 24			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V
3. Pin 10 is at 14kHz, Pin 11 is at 7kHz, Pin 13 is at 1.7kHz, Pin 14 is at 3.5kHz
4. Pin 10 is at 14kHz, Pin 11 is at 7kHz, Pin 14 is at 3.5kHZ

Functional Diagram



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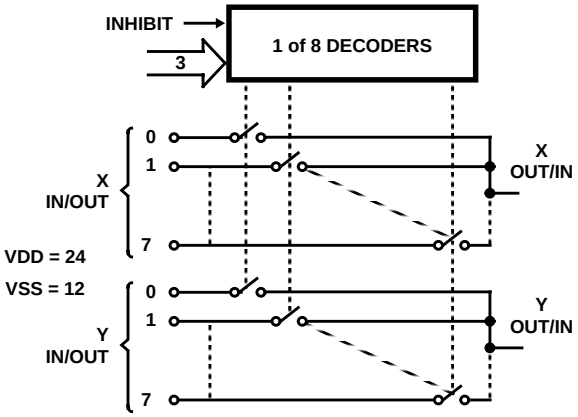

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CD4067 TRUTH TABLE

A	B	C	D	Inh	SELECTED CHANNEL
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

CD4097 TRUTH TABLE

A	B	C	Inh	SELECTED CHANNEL
X	X	X	1	None
0	0	0	0	0X, 0Y
1	0	0	0	1X, 1Y
0	1	0	0	2X, 2Y
1	1	0	0	3X, 3Y
0	0	1	0	4X, 4Y
1	0	1	0	5X, 5Y
0	1	1	0	6X, 6Y
1	1	1	0	7X, 7Y

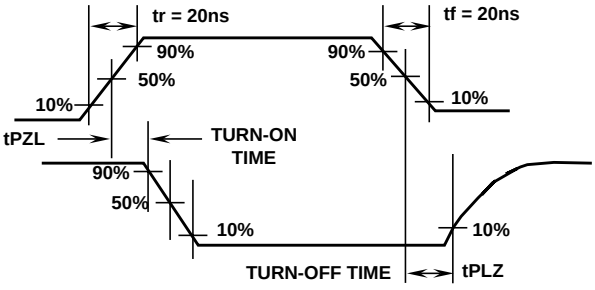


FIGURE 1. WAVEFORM CHANNEL BEING TURNED ON, OFF

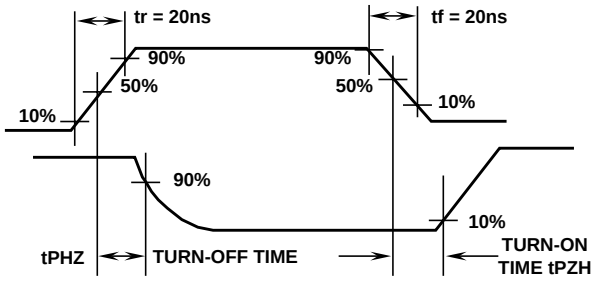


FIGURE 2. PROPAGATION DELAY WAVEFORM, CHANNEL BEING TURNED OFF, ON

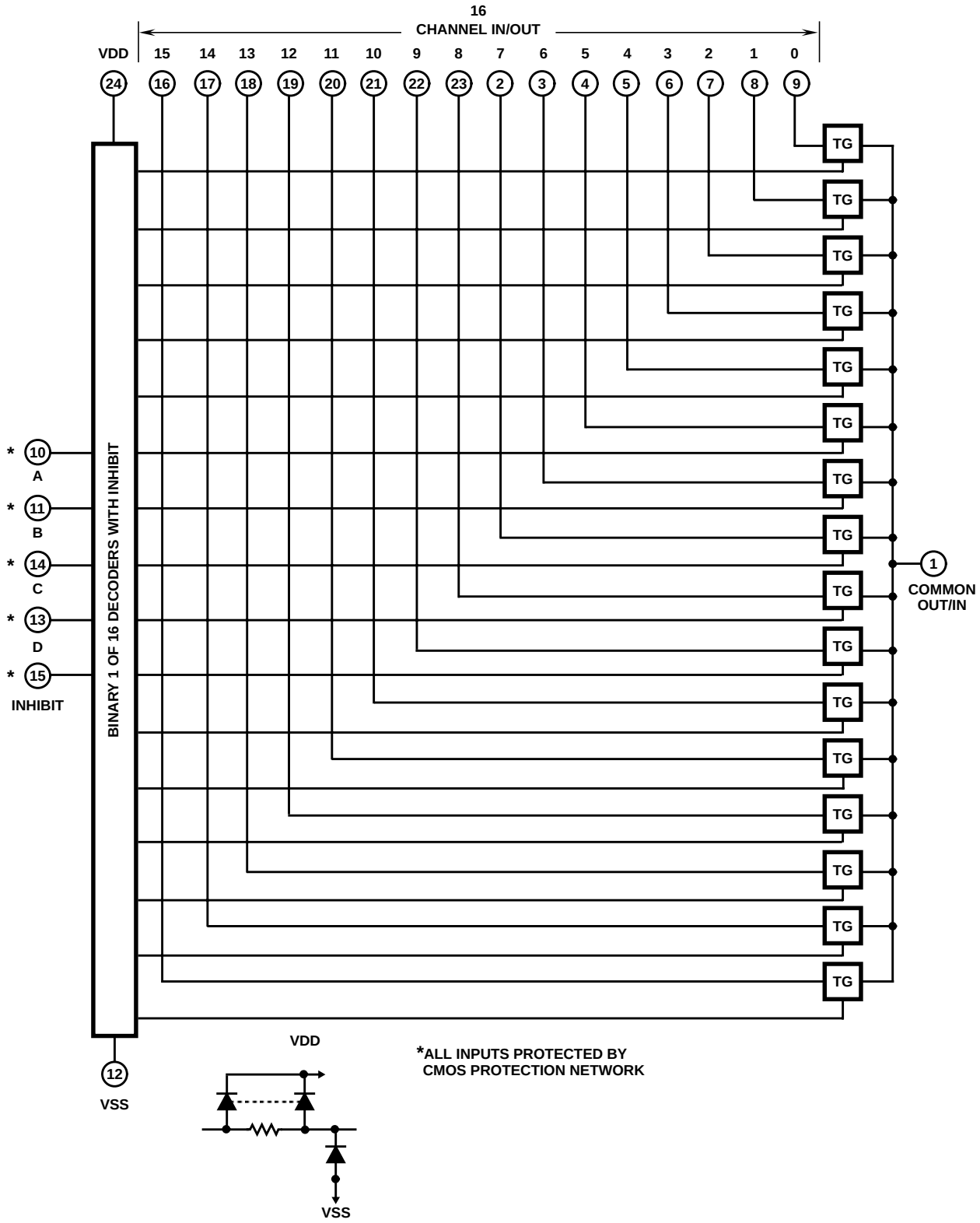


FIGURE 3. CD4067BMS LOGIC DIAGRAM

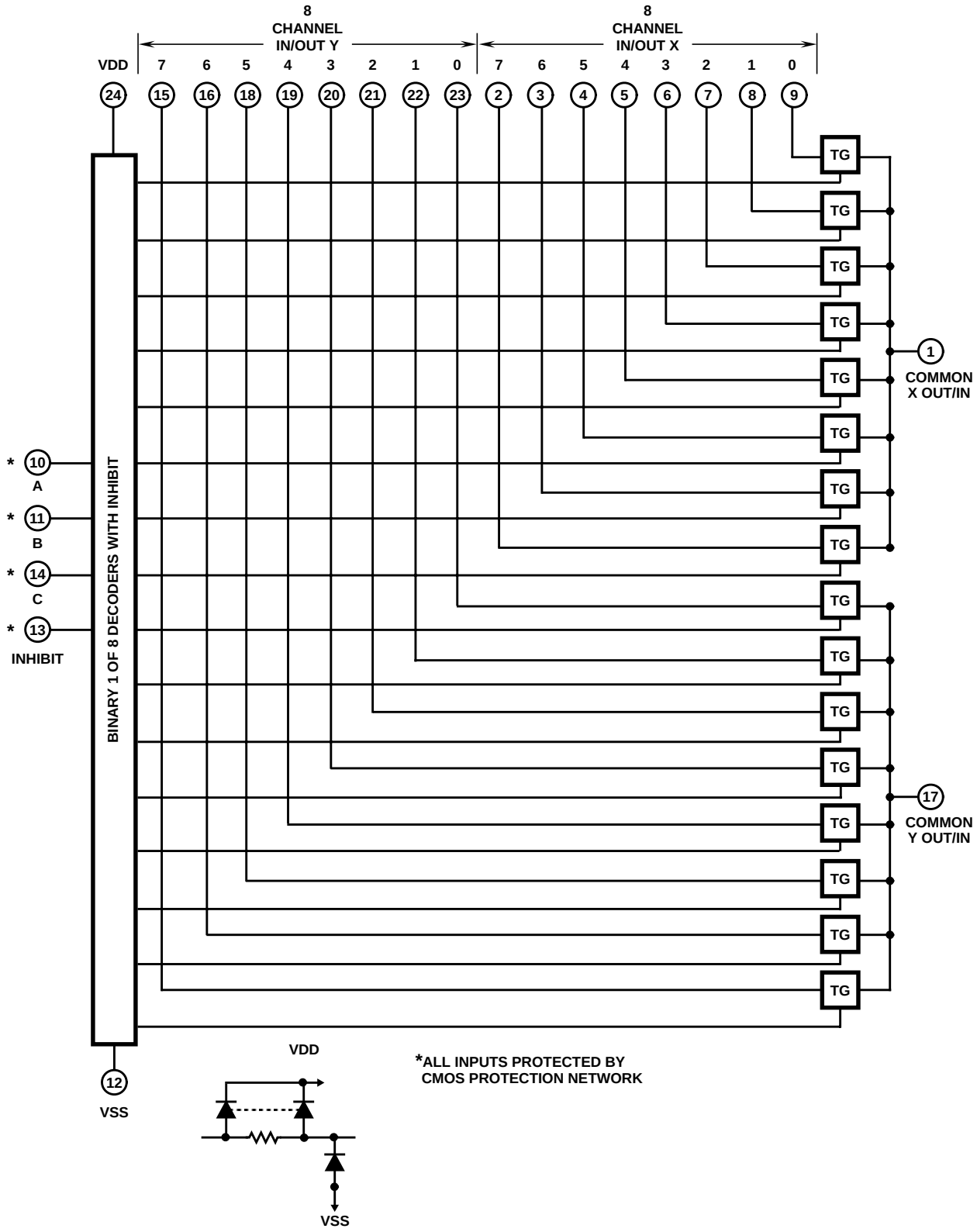


FIGURE 4. CD4097BMS LOGIC DIAGRAM

Typical Performance Characteristics

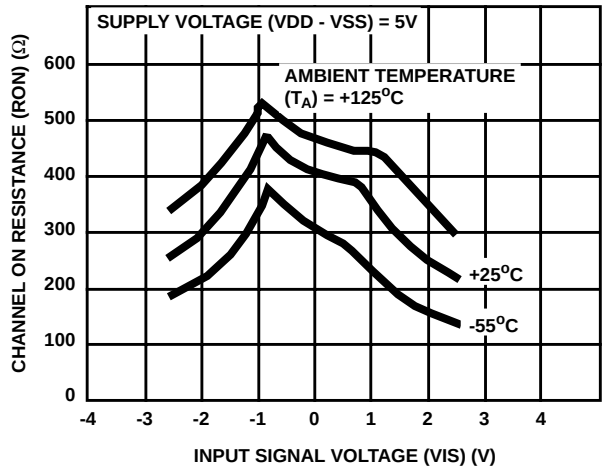


FIGURE 5. TYPICAL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

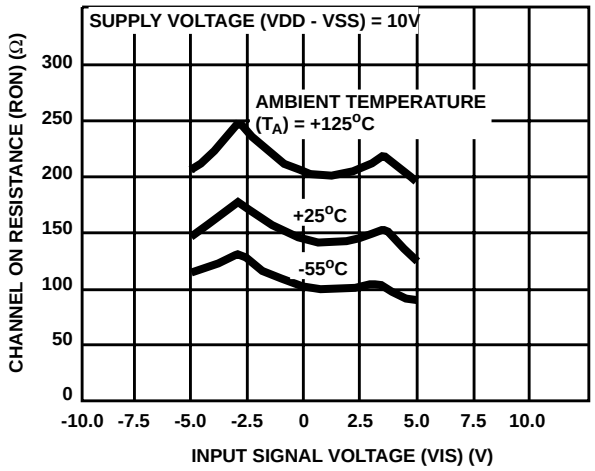


FIGURE 6. TYPICAL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

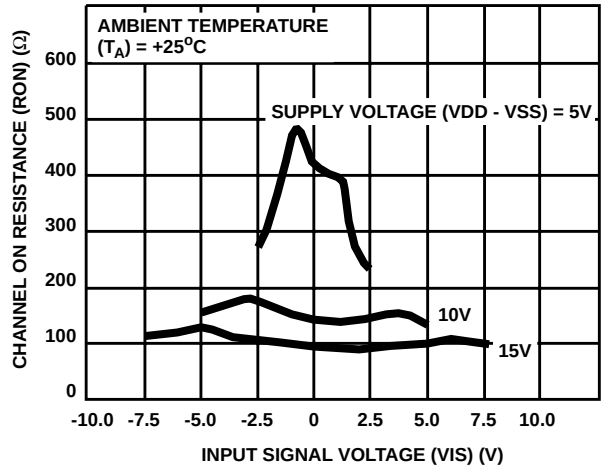


FIGURE 7. TYPICAL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

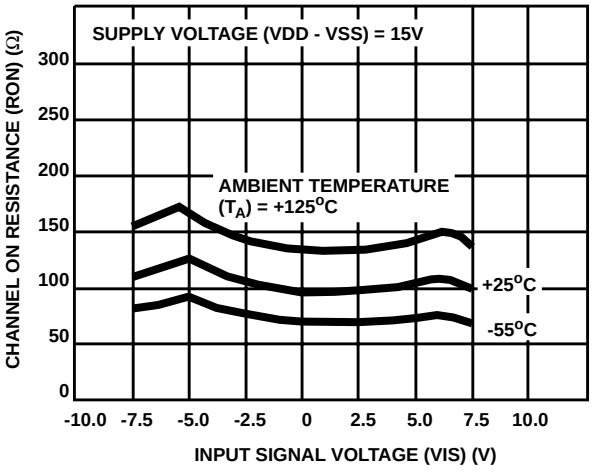
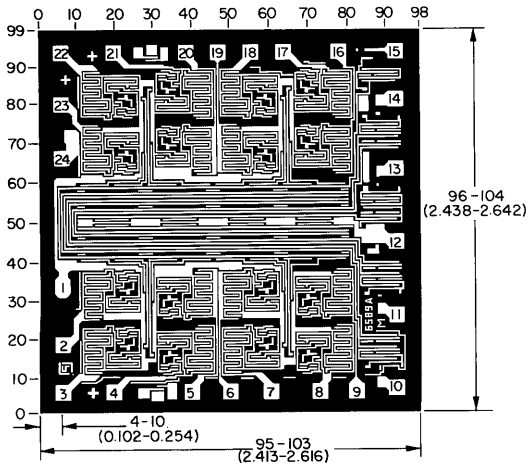
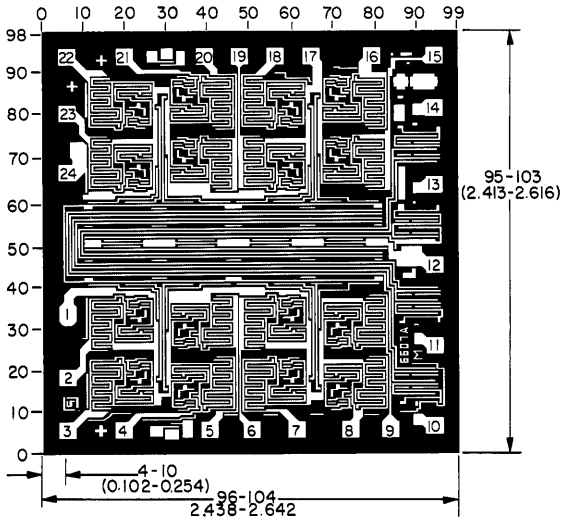


FIGURE 8. TYPICAL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

Chip Dimensions and Pad Layouts



CD4067BMSH



CD4097BMSH

Dimensions in parentheses are in millimeters
and are derived from the basic inch dimensions
as indicated. Grid graduations are in mils (10^{-3} inch)

Special Considerations

In applications where separate power sources are used to drive VDD and the signal inputs, the VDD current capability should exceed VDD/RL (RL = effective external load). This provision avoids permanent current flow or clamp action on the VDD supply when power is applied or removed from the CD4067BMS or CD4097BMS.

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned on or off by an address input, there is a momentary conductive path from the channel to VSS, which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning on a channel will similarly dump some charge to VSS.

The amount of charge dumped is mostly a function of the signal level above VSS. Typically, at VDD - VSS = 10V, a 100pF capacitor connected to the input or output of the channel will lose 3 to 4% of its voltage at the moment the channel turns on or off. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1 - 2µs. When the inhibit signal turns a channel off, there is no charge dumping to VSS. Rather, there is a slight rise in the channel voltage level (65mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

In certain applications, the external load resistor current may include both VDD and signal-line components. To avoid drawing VDD current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from RON values shown in ELECTRICAL CHARACTERISTICS CHART - Table 1). no VDD current will flow through RL if the switch current flows into terminal 1 on the CD4067BMS, terminals 1 and 17 on the CD4097BMS.

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches