



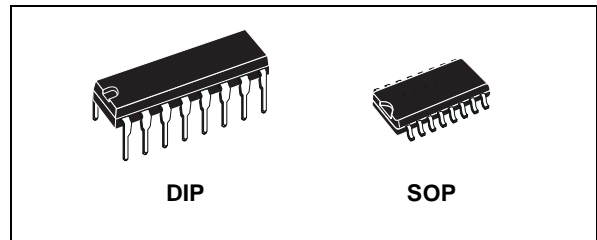
## HCF4015B

### DUAL 4-STAGE STATIC SHIFT REGISTER WITH SERIAL INPUT/PARALLEL OUTPUT

- MEDIUM SPEED OPERATION 12 MHz (Typ.)  
CLOCK RATE AT  $V_{DD} - V_{SS} = 10V$
- FULLY STATIC OPERATION
- 8 MASTER-SLAVE FLIP-FLOPS PLUS  
INPUT AND OUTPUT BUFFERING
- HIGH NOISE IMMUNITY
- QUIESCENT CURRENT SPECIFIED UP TO  
20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT  
 $I_l = 100nA$  (MAX) AT  $V_{DD} = 18V$   $T_A = 25^\circ C$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC  
JESD13B "STANDARD SPECIFICATIONS  
FOR DESCRIPTION OF B SERIES CMOS  
DEVICES"

#### DESCRIPTION

HCF4015B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. HCF4015B consists of two identical, independent, 4 stage serial-input/parallel-output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the

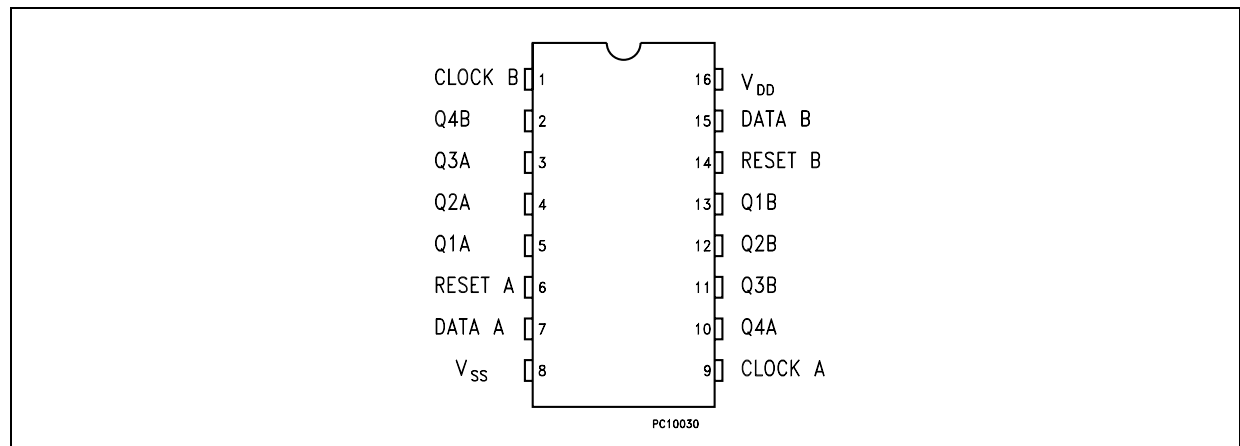


#### ORDER CODES

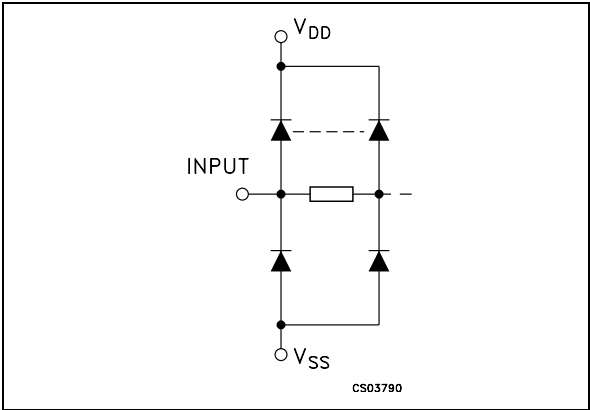
PACKAGE	TUBE	T & R
DIP	HCF4015BEY	
SOP	HCF4015BM1	HCF4015M013TR

four stages on both registers. All register stages are D-TYPE, MASTER-SLAVE flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive going clock transition. The resetting of all stages is accomplished by a high level on the reset line. It is possible to expand the register to 8 stages using one HCF4015B package and to expand to more than 8 stages by using addition HCF4015Bs.

#### PIN CONNECTION



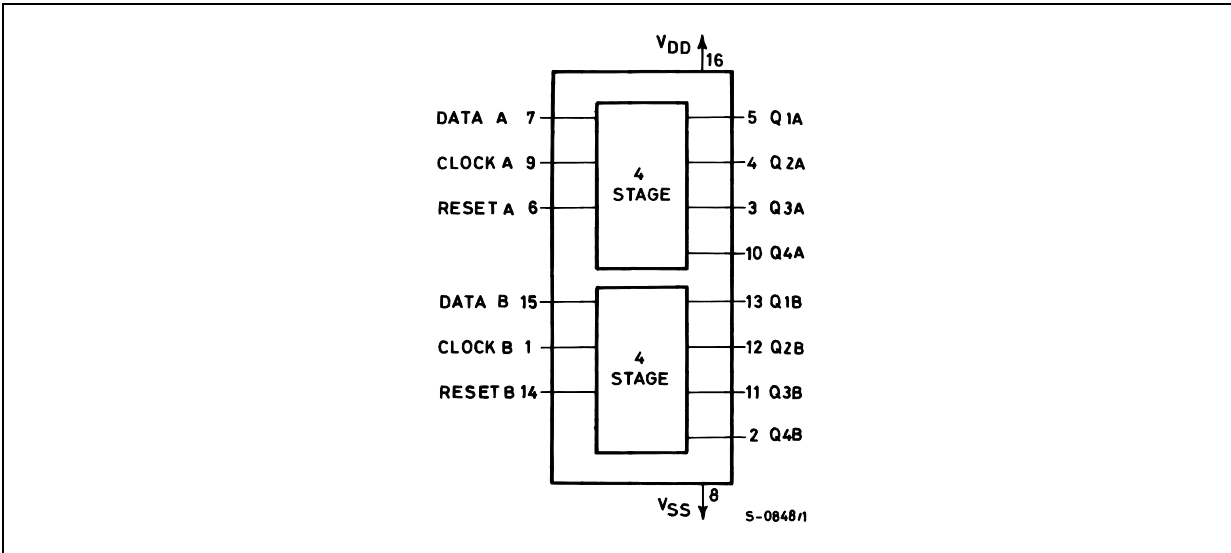
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 9	CLOCK A CLOCK B	Clock Input
6, 14	RESET A RESET B	Reset Input
7, 15	DATA A DATA B	Data Inputs
5, 4, 3, 10	QnA	Outputs A-Stage
13, 12, 11, 2	QnB	Outpus B-Stage
8	VSS	Negative Supply Voltage
16	VDD	Positive Supply Voltage

FUNCTIONAL DIAGRAM

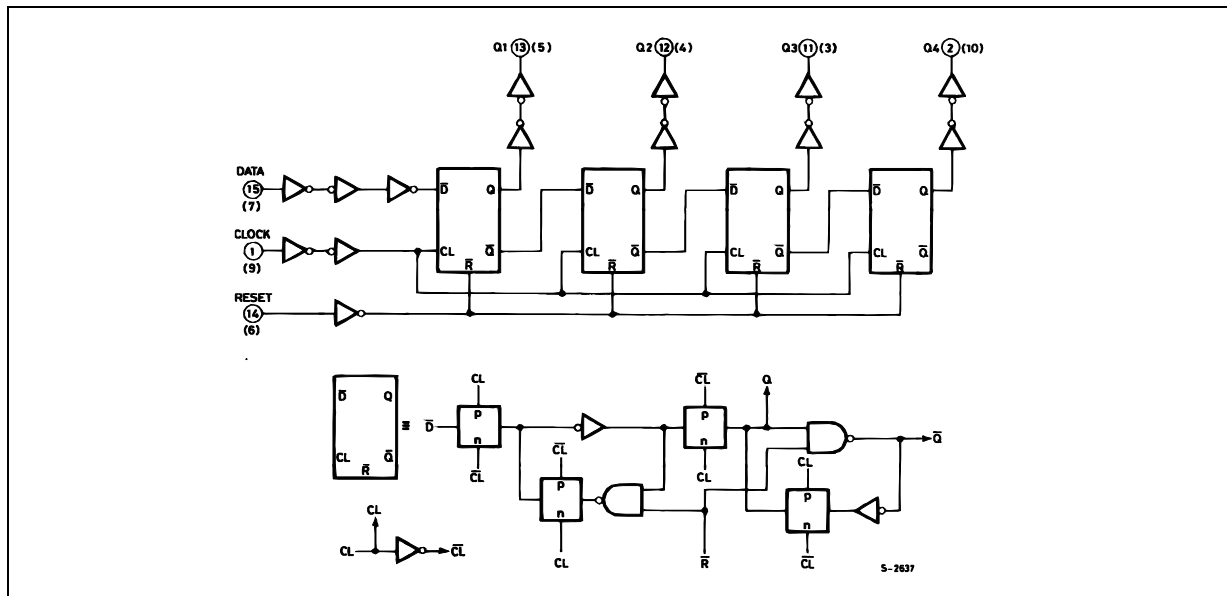


TRUTH TABLE

CLOCK	D	R	Q <sub>1</sub>	Q <sub>n</sub>
	L	L	L	Q <sub>n</sub> - 1
	H	L	H	Q <sub>n</sub> - 1
	X	L	Q <sub>1</sub>	Q <sub>n</sub> - (NO CHANGE)
X	X	H	L	0

X : Don't Care

## LOGIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	-0.5 to +22	V
$V_I$	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
$I_I$	DC Input Current	$\pm 10$	mA
$P_D$	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
$T_{op}$	Operating Temperature	-55 to +125	°C
$T_{stg}$	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to  $V_{SS}$  pin voltage.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	3 to 20	V
$V_I$	Input Voltage	0 to $V_{DD}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value								Unit
		V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>O</sub>   (μA)	V <sub>DD</sub> (V)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C			
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
I <sub>L</sub>	Quiescent Current	0/5			5		0.04	5		150		150	μA	
		0/10			10		0.04	10		300		300		
		0/15			15		0.04	20		600		600		
		0/20			20		0.08	100		3000		3000		
V <sub>OH</sub>	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V	
		0/10		<1	10	9.95			9.95		9.95			
		0/15		<1	15	14.95			14.95		14.95			
V <sub>OL</sub>	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V	
		10/0		<1	10		0.05			0.05		0.05		
		15/0		<1	15		0.05			0.05		0.05		
V <sub>IH</sub>	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V	
			1/9	<1	10	7			7		7			
			1.5/13.5	<1	15	11			11		11			
V <sub>IL</sub>	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V	
			9/1	<1	10			3		3		3		
			13.5/1.5	<1	15			4		4		4		
I <sub>OH</sub>	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA	
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36			
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9			
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4			
I <sub>OL</sub>	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA	
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9			
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4			
I <sub>I</sub>	Input Leakage Current	0/18	Any Input		18		±10 <sup>-5</sup>	±0.1		±1		±1	μA	
C <sub>I</sub>	Input Capacitance		Any Input				5	7.5					pF	

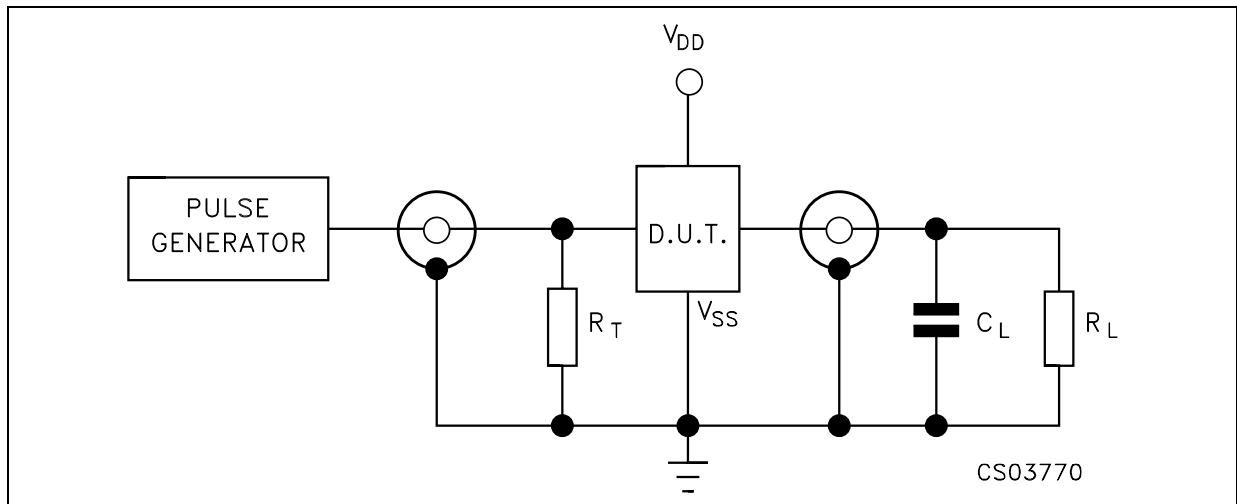
The Noise Margin for both "1" and "0" level is: 1V min. with V<sub>DD</sub>=5V, 2V min. with V<sub>DD</sub>=10V, 2.5V min. with V<sub>DD</sub>=15V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ}\text{C}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 200\text{K}\Omega$ ,  $t_r = t_f = 20\text{ ns}$ )

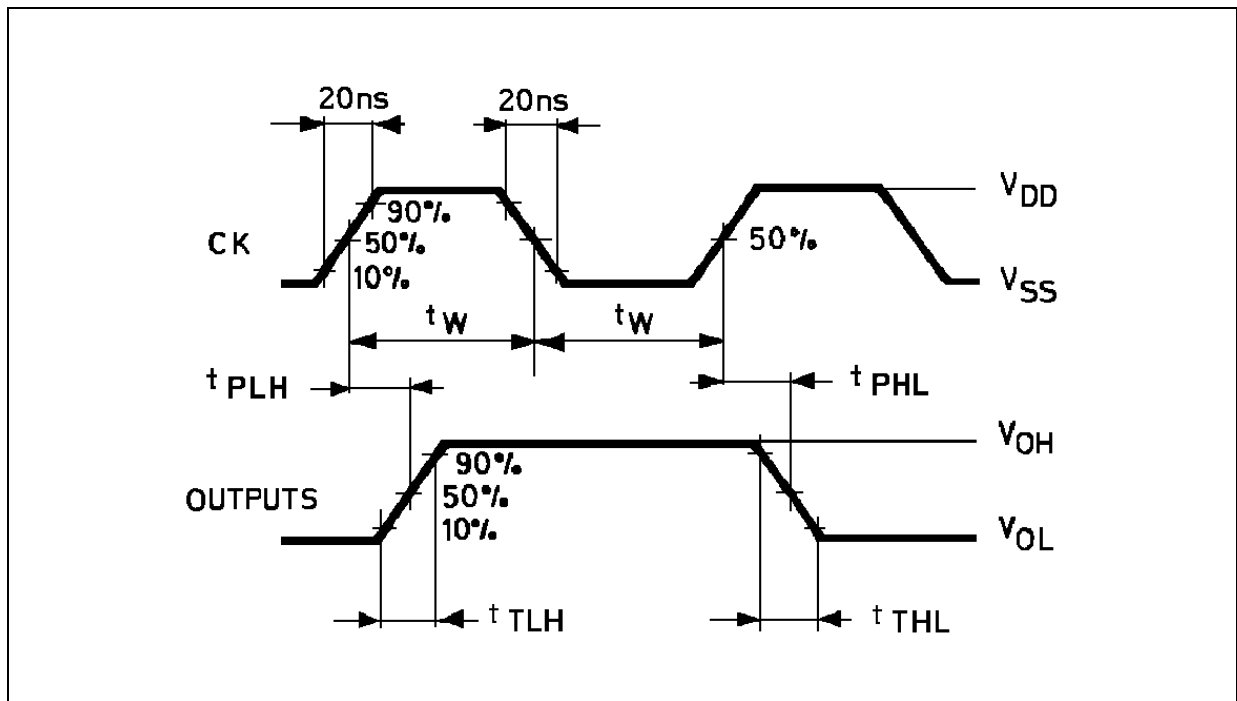
Symbol	Parameter	Test Condition		Value (*)			Unit
		V <sub>DD</sub> (V)		Min.	Typ.	Max.	
CLOCKED OPERATION							
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (carry out or decoded out lines)	5			160	320	ns
		10			80	160	
		15			60	120	
t <sub>THL</sub> t <sub>TLH</sub>	Transition Time (carry out or decoded out lines)	5			100	200	ns
		10			50	100	
		15			40	80	
f <sub>CL</sub>	Maximum Clock Input Frequency	5		3	6		MHz
		10		6	12		
		15		8.5	17		
t <sub>W</sub>	Clock Pulse Width	5		180	90		ns
		10		80	40		
		15		50	25		
t <sub>r</sub> , t <sub>f</sub> <sup>(1)</sup>	Clock Input Rise or Fall Time	5				15	μs
		10				15	
		15				15	
t <sub>setup</sub>	Data Setup Time	5		70	35		ns
		10		40	20		
		15		30	15		
RESET OPERATION							
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time	5			200	400	ns
		10			100	200	
		15			80	160	
t <sub>W</sub>	Reset Pulse Width	5		200	100		ns
		10		80	40		
		15		60	30		

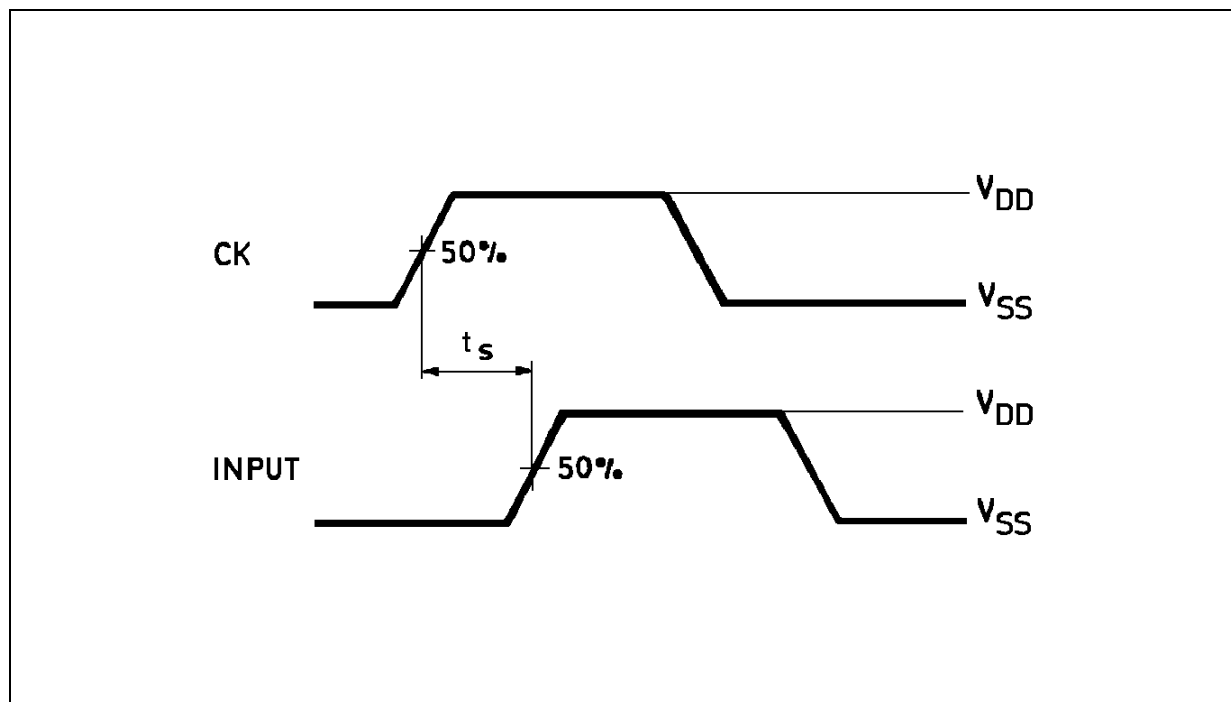
(\*) Typical temperature coefficient for all  $V_{DD}$  value is 0.3 %/°C.(1) If more than one unit is cascaded in the parallel clocked application,  $t_{CL}$  should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transmission time of the carry output driving stage of the estimated capacitive load.

## TEST CIRCUIT



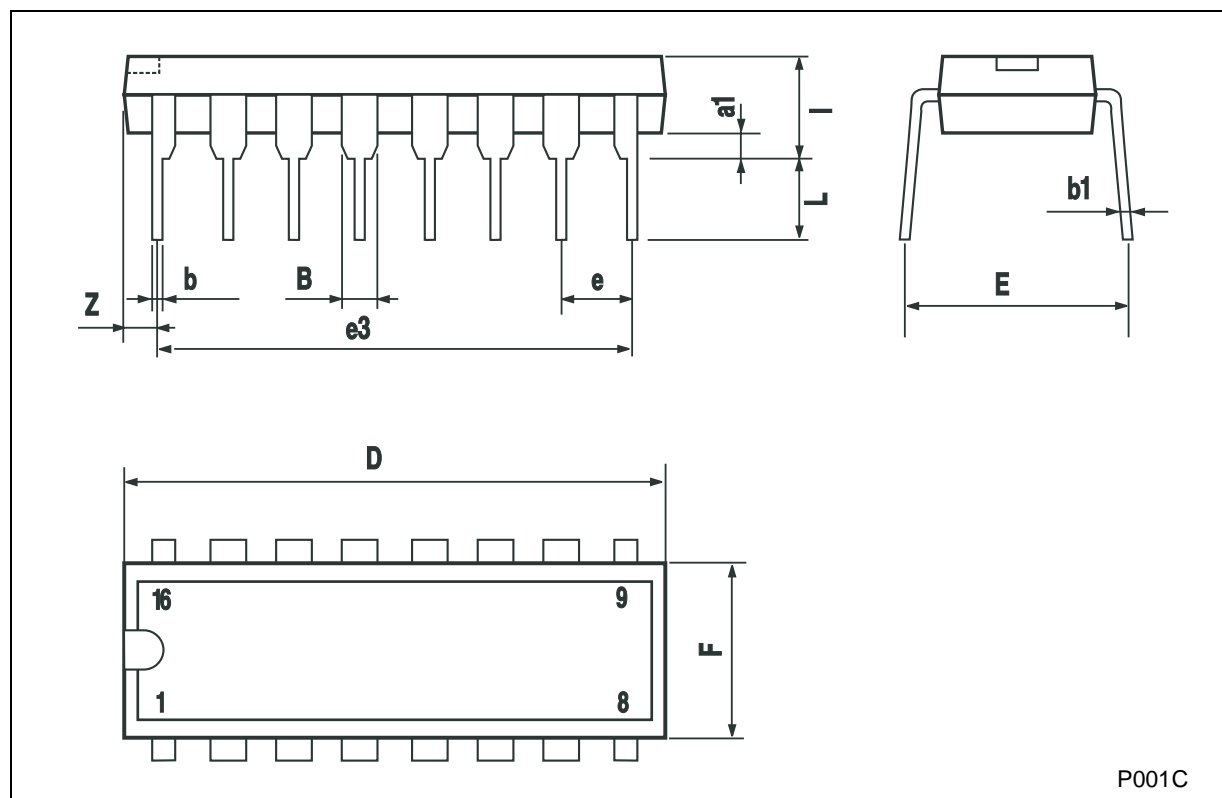
$C_L = 50\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_L = 200\text{K}\Omega$   
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

WAVEFORM 1 : MINIMUM PULSE WIDTH, PROPAGATION DELAY TIME ( $f=1\text{MHz}$ ; 50% duty cycle)

**WAVEFORM 2 : MINIMUM SETUP TIME** ( $f=1\text{MHz}$ ; 50% duty cycle)

### Plastic DIP-16 (0.25) MECHANICAL DATA

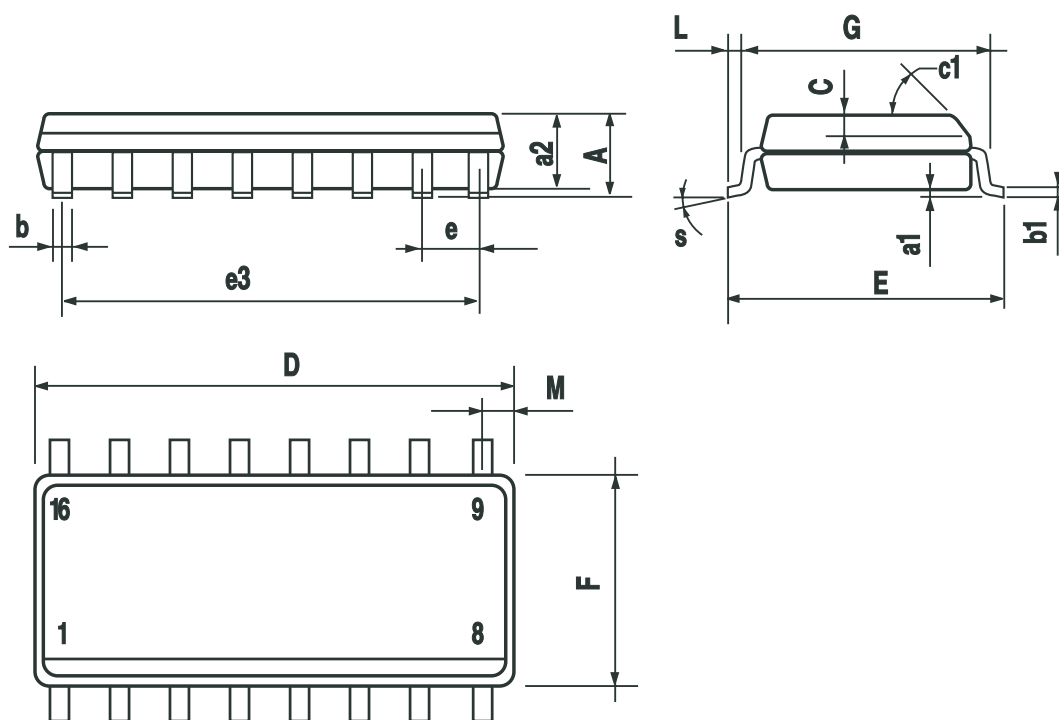
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050





## SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

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