74HC05

Hex inverter with open-drain outputs Rev. 02 — 18 June 2009

Product data sheet

General description 1.

The 74HC05 is a high-speed Si-gate CMOS device that complies with JEDEC standard no. 7A.

The 74HC05 contains six inverters. The outputs of the 74HC05 are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions. The open-drain outputs require pull-up resistors to perform correctly.

2. **Features**

- Wide operating voltage 2.0 V to 6.0 V
- Input levels:
 - ◆ For 74HC05: CMOS level
- Latch-up performance exceeds 100 mA per JESD 78 Class II level A
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

Ordering information 3.

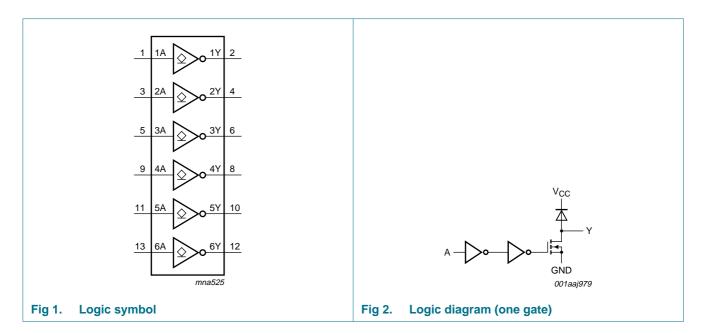
Table 1. **Ordering information**

Type number	Package										
	Temperature range	Name	Description	Version							
74HC05D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1							
74HC05PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1							
74HC05BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5\times3\times0.85$ mm	SOT762-1							



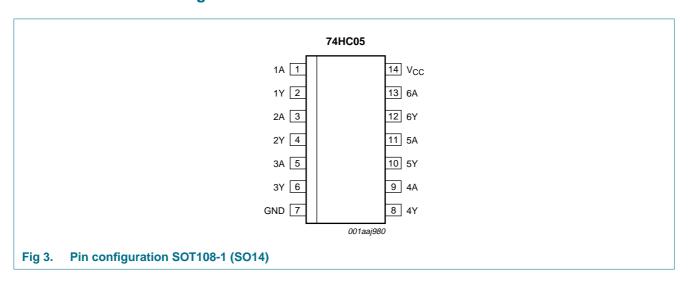
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4. Functional diagram

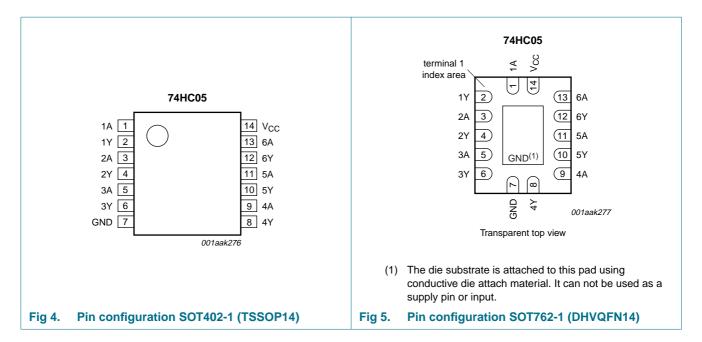


5. Pinning information

5.1 Pinning



Hex inverter with open-drain outputs



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 6A	1, 3, 5, 9, 11, 13	data input
1Y to 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table [1]

Input	Output
nA	nY
L	Z
H	L

^[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$	<u>[1]</u> _	20	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$	<u>[1]</u> _	20	mA
Vo	output voltage		<u>[1]</u> –0.5	V_{CC} + 0.5 V	V

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Table 4. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
Io	output current	$V_{O} < V_{CC} + 0.5 V$	-	25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation		[2] _	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_{I}	input voltage		0	-	V_{CC}	V
V_{O}	output voltage		0	-	V_{CC}	V
T _{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0 V$	-	-	625	ns/V
		V _{CC} = 4.5 V	-	1.67	139	ns/V
		$V_{CC} = 6.0 \text{ V}$	-	-	83	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		–40 °C 1	to +85 °C	-40 °C to	-40 °C to +125 °C		
			Min	Тур	Max	Min	Max	Min	Max		
V_{IH}	HIGH-level	$V_{CC} = 2.0 \text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V	
	input voltage	$V_{CC} = 4.5 \text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V	
		$V_{CC} = 6.0 \text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V	
V _{IL} LOW-level	$V_{CC} = 2.0 \text{ V}$	-	8.0	0.5	-	0.5	-	0.5	V		
	input voltage	$V_{CC} = 4.5 \text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V	
		$V_{CC} = 6.0 \text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V	
V_{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}									
	output voltage	$I_O = 20 \mu A; V_{CC} = 2.0 V$	-	0	0.1	-	0.1	-	0.1	V	
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V	
		$I_O = 20 \mu A; V_{CC} = 6.0 V$	-	0	0.1	-	0.1	-	0.1	V	
		$I_O = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V	
		$I_{O} = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V	

^[2] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For TSSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

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Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C t	o +85 °C	–40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
II	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	0.1	-	1	-	1	μΑ
l _{OZ}	OFF-state output current	per input pin; $V_I = V_{IL}$; $V_O = V_{CC}$ or GND; other inputs at V_{CC} or GND; $V_{CC} = 6.0 \text{ V}$; $I_O = 0 \text{ A}$	-	-	0.5	-	5.0	-	10	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	2.0	-	20	-	40	μΑ
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; for test circuit see Figure 7.

Symbol	Parameter	Conditions			25 °C		–40 °C to	Unit	
				Min	Тур	Max	Max (85 °C)	Max (125 °C)	
t _{PLZ} LOW to OFF-state		nA to nY; see Figure 6							
	propagation delay	V _{CC} = 2.0 V		-	20	90	115	135	ns
		V _{CC} = 4.5 V		-	11	18	23	27	ns
		V _{CC} = 6.0 V		-	10	15	20	23	ns
	OFF-state to LOW	nA to nY; see Figure 6							
	propagation delay	V _{CC} = 2.0 V		-	22	90	115	135	ns
		V _{CC} = 4.5 V		-	9	18	23	27	ns
		V _{CC} = 6.0 V		-	8	15	20	23	ns
t _{THL}	HIGH to LOW	see Figure 6							
	output transition time	V _{CC} = 2.0 V		-	18	75	95	110	ns
	ume	V _{CC} = 4.5 V		-	6	15	19	22	ns
		V _{CC} = 6.0 V		-	5	13	16	19	ns
C_{PD}	power dissipation capacitance	per inverter; $V_I = GND$ to V_{CC} ; $V_{CC} = 5.0 \text{ V}$	<u>[1]</u>	-	4	-	-	-	pF

^[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(0.5 \times C_L \times V_O^2 \times f_o) \text{ where:}$

 f_i = input frequency in MHz;

 f_o = output frequency in MHz;

 V_O = output voltage in V (output HIGH);

 V_{CC} = supply voltage in V;

N = number of inputs switching;

 R_L = load resistance in $M\Omega$;

C_L = load capacitance in pF;

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Hex inverter with open-drain outputs

11. Waveforms

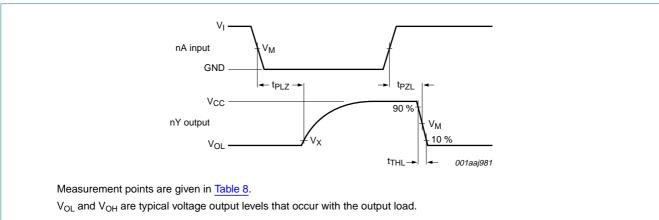
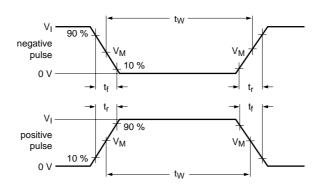


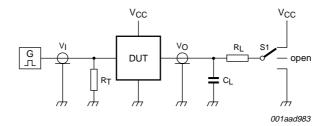
Fig 6. The input nA to output nY propagation delays and output transition times

Table 8. Measurement points

Input	Dutput						
V_{M}	V _M	V _X					
0.5V _{CC}	0.5V _{CC}	0.1V _{CC}					

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Test data is given in Table 9.

Definitions test circuit:

 R_{T} = termination resistance should be equal to output impedance Z_{o} of the pulse generator.

 C_L = load capacitance including jig and probe capacitance.

R_L = Load resistance.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

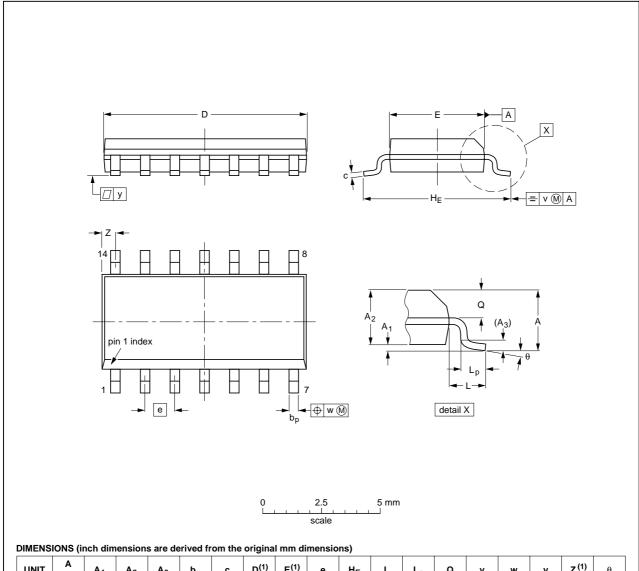
Input		Load		S1 position
VI	t _r , t _f	CL	R _L	t _{PZL} , t _{PLZ}
V_{CC}	6 ns	50 pF	1 kΩ	V _{CC}

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12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01	1	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

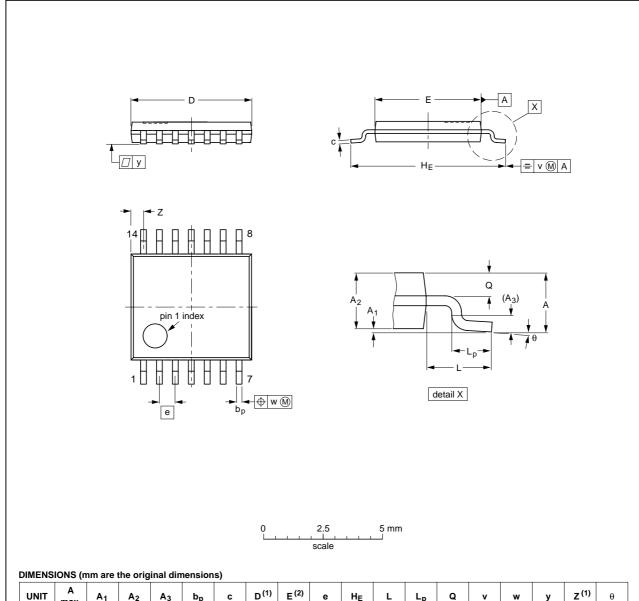
	OUTLINE VERSION		REFER	EUROPEAN	ISSUE DATE		
		IEC	JEDEC	JEITA		PROJECTION	1330E DATE
	SOT108-1	076E06	MS-012				99-12-27 03-02-19

Fig 8. Package outline SOT108-1 (SO14)

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



UNIT	max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

	OUTLINE		REFER	EUROPEAN	ISSUE DATE		
	VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
	SOT402-1		MO-153				99-12-27 03-02-18
l						— •	03-02-10

Fig 9. Package outline SOT402-1 (TSSOP14)

 74HC05_2
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DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1

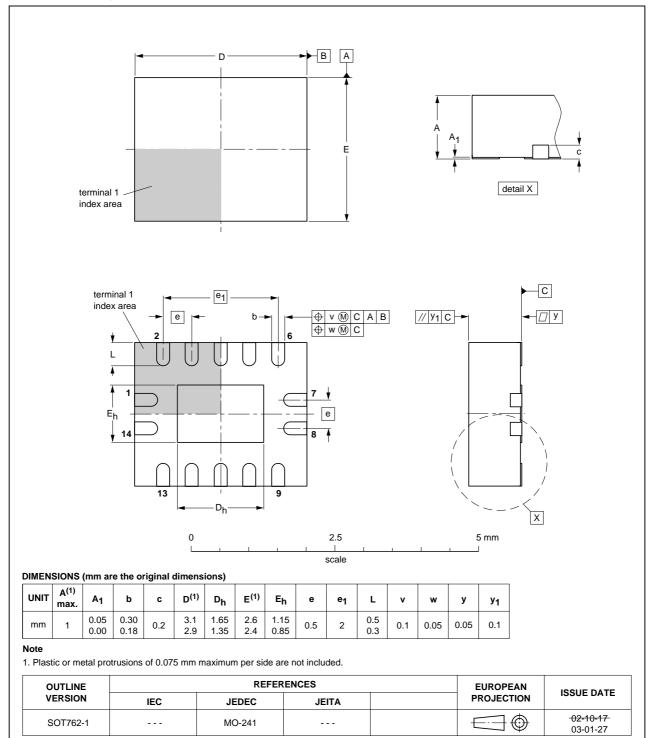


Fig 10. Package outline SOT762-1 (DHVQFN14)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description			
CDM	Charged Device Model			
CMOS	Complementary Metal-Oxide Semiconductor			
DUT	Device Under Test			
ESD	ElectroStatic Discharge			
HBM	Human Body Model			

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74HC05_2	20090618	Product data sheet	-	74HC05_1	
Modifications: • Added type numbers 74HC05PW (TSSOP14 package) and 74HC05BQ (DHVQFN package)					
74HC05_1	20090427	Product data sheet	-	-	

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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