# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

# HEF4018B
# MSI
## Presettable divide-by-N counter

Product specification
File under Integrated Circuits, IC04

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Philips Semiconductors

PHILIPS

# PRESETTABLE DIVIDE-BY-N COUNTER

The HEF4018B is a 5-stage Johnson counter with a clock input (CP), a data input (D), an asynchronous parallel load input (PL), five parallel inputs ($P_0$ to $P_4$), five active LOW buffered outputs ($\overline{O}_0$ to $\overline{O}_4$), and an overriding asynchronous master reset input (MR).
Information on $P_0$ to $P_4$ is asynchronously loaded into the counter while PL is HIGH, independent of CP and D inputs. When $P_L$ is LOW, the counter advances on the LOW to HIGH transition of CP. By connecting $\overline{O}_0$ to $\overline{O}_4$ to D, the counter operates as a divide-by-n counter (n = 2 to 10; see also function selection below). Each register stage is a D-type master-slave flip-flop with a set-direct/clear-direct input. An internal code correction circuit provides automatic code correction of the counter. From any illegal code the counter is in a proper counting mode within 11 clock pulses.

A HIGH on MR resets the counter ($\overline{O}_0$ to $\overline{O}_4$ = HIGH) independent of all other inputs.

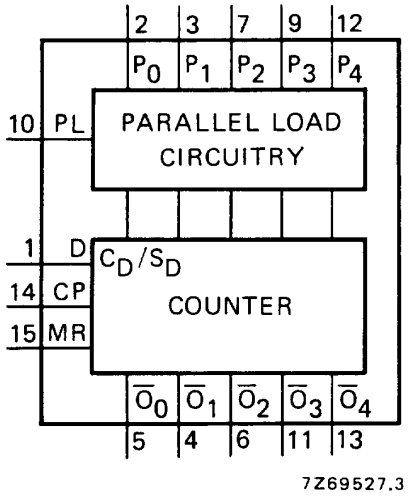


Fig. 1 Functional diagram.

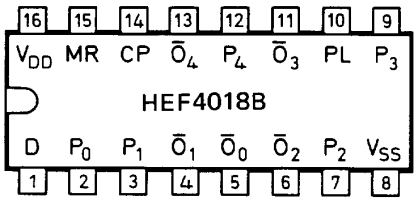


Fig. 2 Pinning diagram.

HEF4018BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4018BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4018BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

## FUNCTION SELECTION

| counter mode; divide by | connect D input to | remarks |
|---|---|---|
| 10 | $\overline{O}_4$ | no external components needed |
| 8 | $\overline{O}_3$ | |
| 6 | $\overline{O}_2$ | |
| 4 | $\overline{O}_1$ | |
| 2 | $\overline{O}_0$ | |
| 9 | $\overline{O}_3 \cdot \overline{O}_4$ | AND gate needed; counter skips all HIGH states |
| 7 | $\overline{O}_2 \cdot \overline{O}_3$ | |
| 5 | $\overline{O}_1 \cdot \overline{O}_2$ | |
| 3 | $\overline{O}_0 \cdot \overline{O}_1$ | |

## PINNING

| | |
|---|---|
| PL | parallel load input |
| $P_0$ to $P_4$ | parallel inputs |
| D | data input |
| CP | clock input (LOW to HIGH edge triggered) |
| MR | master reset input |
| $\overline{O}_0$ to $\overline{O}_4$ | buffered output (active LOW) |

## APPLICATION INFORMATION

Some examples of applications for the HEF4018B are:

- Programmable divide-by-n counter
- Programmable frequency division
- Timers

## FAMILY DATA

$I_{DD}$ LIMITS category MSI } see Family Specifications

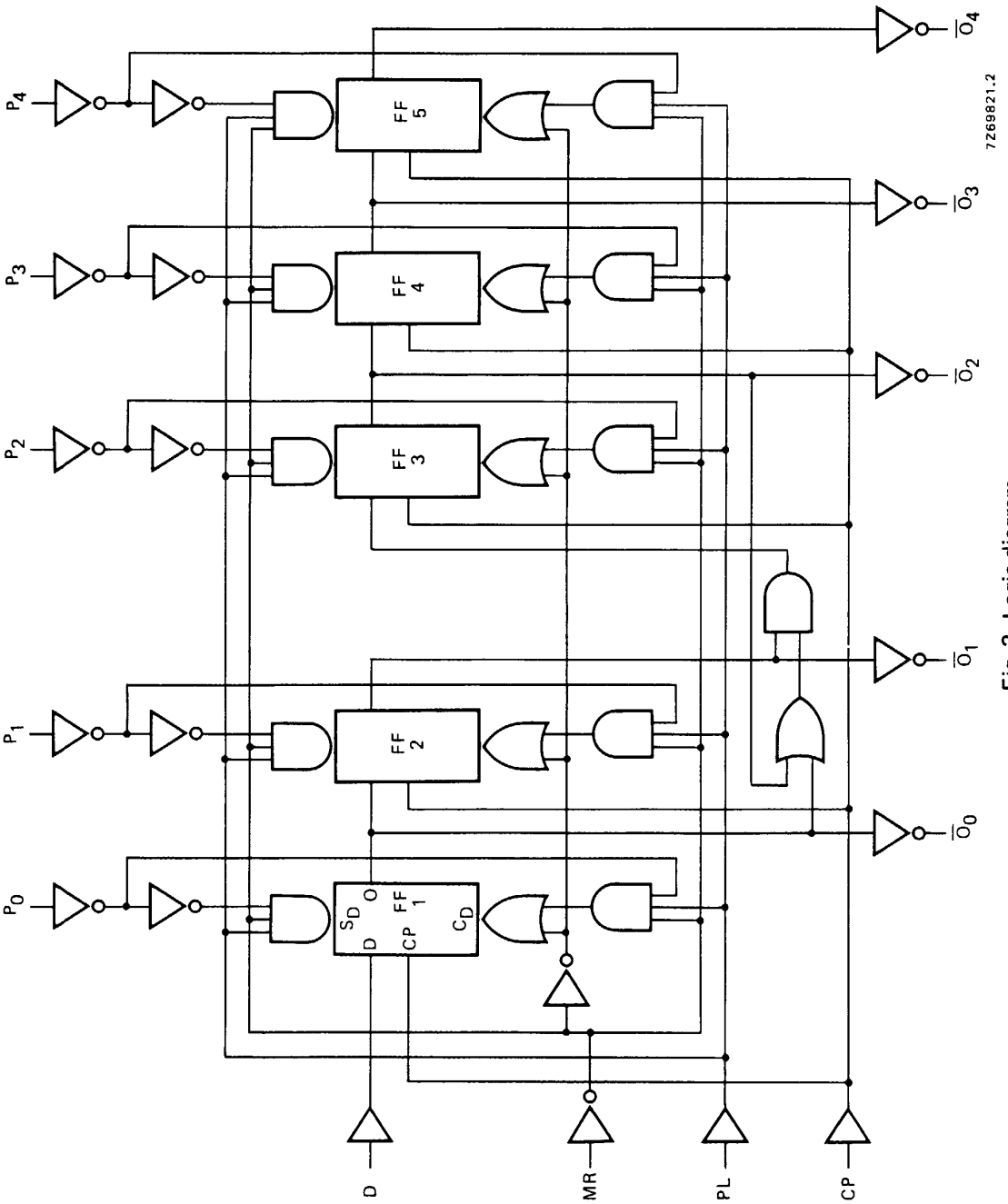


Fig. 3 Logic diagram.

## A.C. CHARACTERISTICS

$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; input transition times ⩽ 20 ns

| | $V_{DD}$ V | typical formula for P (μW) | where |
|---|---|---|---|
| Dynamic power dissipation per package (P) | 5 | 700 $f_i$ + Σ($f_o C_L$) x $V_{DD}^2$ | $f_i$ = input freq. (MHz)<br>$f_o$ = output freq. (MHz)<br>$C_L$ = load capacitance (pF)<br>Σ($f_o C_L$) = sum of outputs<br>$V_{DD}$ = supply voltage (V) |
| | 10 | 3450 $f_i$ + Σ($f_o C_L$) x $V_{DD}^2$ | |
| | 15 | 10 300 $f_i$ + Σ($f_o C_L$) x $V_{DD}^2$ | |

## A.C. CHARACTERISTICS

$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; $C_L$ = 50 pF; input transition times ⩽ 20 ns

| | $V_{DD}$ V | symbol | min. | typ. | max. | | typical extrapolation formula |
|---|---|---|---|---|---|---|---|
| Propagation delays | | | | | | | |
| CP → $\overline{O}$ | 5 | | | 185 | 370 | ns | 158 ns + (0,55 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{PHL}$ | | 65 | 135 | ns | 54 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 50 | 95 | ns | 42 ns + (0,16 ns/pF) $C_L$ |
| | 5 | | | 145 | 295 | ns | 118 ns + (0,55 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{PLH}$ | | 55 | 110 | ns | 44 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 40 | 85 | ns | 32 ns + (0,16 ns/pF) $C_L$ |
| PL → $\overline{O}$ | 5 | | | 205 | 415 | ns | 178 ns + (0,55 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{PHL}$ | | 70 | 140 | ns | 59 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 50 | 105 | ns | 42 ns + (0,16 ns/pF) $C_L$ |
| | 5 | | | 175 | 350 | ns | 148 ns + (0,55 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{PLH}$ | | 65 | 125 | ns | 54 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 50 | 95 | ns | 42 ns + (0,16 ns/pF) $C_L$ |
| MR → $\overline{O}$ | 5 | | | 140 | 280 | ns | 113 ns + (0,55 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{PLH}$ | | 55 | 105 | ns | 44 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) $C_L$ |
| Output transition times | 5 | | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{THL}$ | | 30 | 60 | ns | 9 ns + (0,42 ns/pF) $C_L$ |
| | 15 | | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) $C_L$ |
| | 5 | | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{TLH}$ | | 30 | 60 | ns | 9 ns + (0,42 ns/pF) $C_L$ |
| | 15 | | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) $C_L$ |

## A.C. CHARACTERISTICS

$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; $C_L$ = 50 pF; input transition times ⩽ 20 ns

| | $V_{DD}$ V | symbol | min. | typ. | max. | | typical extrapolation formula |
|---|---|---|---|---|---|---|---|
| Set-up time D → CP | 5 | $t_{su}$ | 130 | 65 | | ns | see also waveforms Figs 4, 5 and 6 |
| | 10 | | 40 | 20 | | ns | |
| | 15 | | 30 | 15 | | ns | |
| Hold time D → CP | 5 | $t_{hold}$ | 20 | −45 | | ns | |
| | 10 | | 5 | −15 | | ns | |
| | 15 | | 5 | −10 | | ns | |
| Minimum clock pulse width; LOW | 5 | $t_{WCPL}$ | 140 | 70 | | ns | |
| | 10 | | 50 | 25 | | ns | |
| | 15 | | 40 | 20 | | ns | |
| Minimum MR pulse width; HIGH | 5 | $t_{WMRH}$ | 100 | 50 | | ns | |
| | 10 | | 35 | 20 | | ns | |
| | 15 | | 25 | 15 | | ns | |
| Minimum PL pulse width; HIGH | 5 | $t_{WPLH}$ | 145 | 75 | | ns | |
| | 10 | | 50 | 25 | | ns | |
| | 15 | | 35 | 20 | | ns | |
| Recovery time for MR | 5 | $t_{RMR}$ | 135 | 70 | | ns | |
| | 10 | | 40 | 20 | | ns | |
| | 15 | | 25 | 15 | | ns | |
| Recovery time for PL | 5 | $t_{RPL}$ | 170 | 85 | | ns | |
| | 10 | | 55 | 30 | | ns | |
| | 15 | | 40 | 20 | | ns | |
| Maximum clock pulse frequency | 5 | $f_{max}$ | 2 | 4 | | MHz | |
| | 10 | | 6 | 11 | | MHz | |
| | 15 | | 8 | 16 | | MHz | |

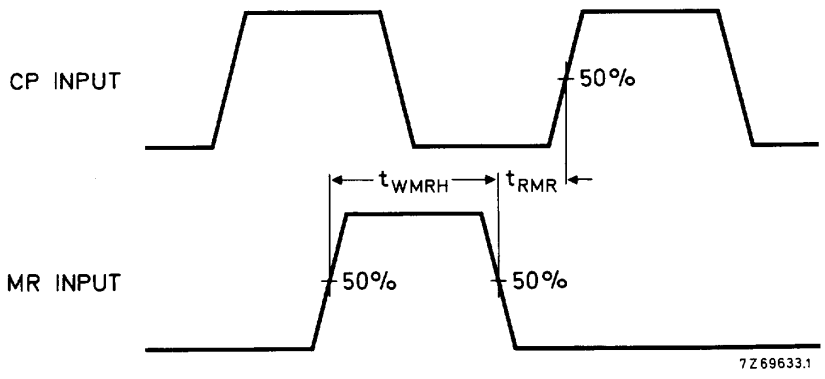


Fig. 4 Waveforms showing minimum MR pulse width and MR recovery time.

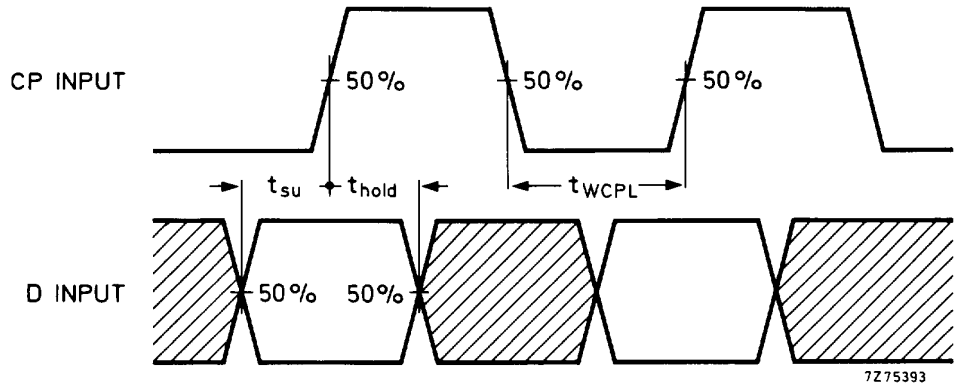


Fig. 5 Waveforms showing minimum clock pulse width, set-up time and hold time for CP and D.

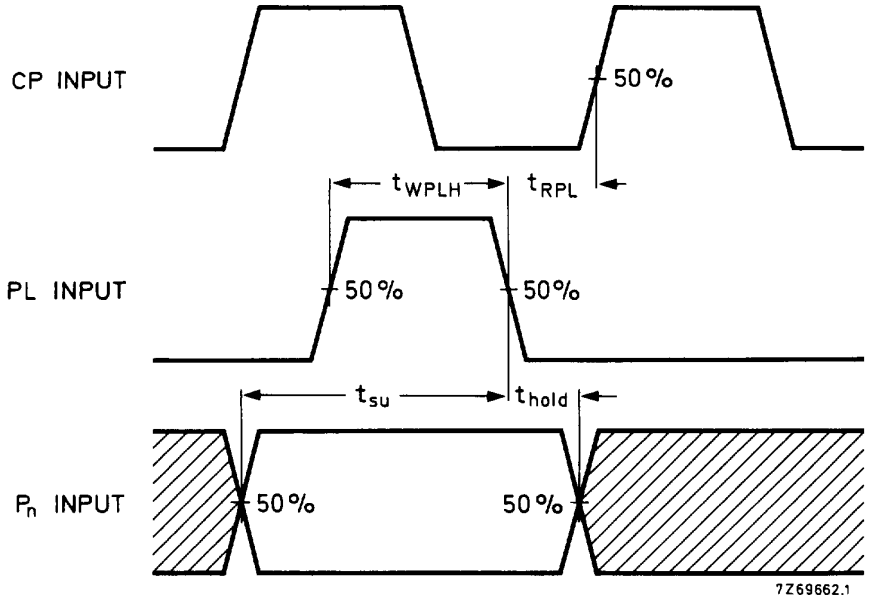


Fig. 6 Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for $P_n$ to PL. Set-up and hold times are shown as positive values but may be specified as negative values.

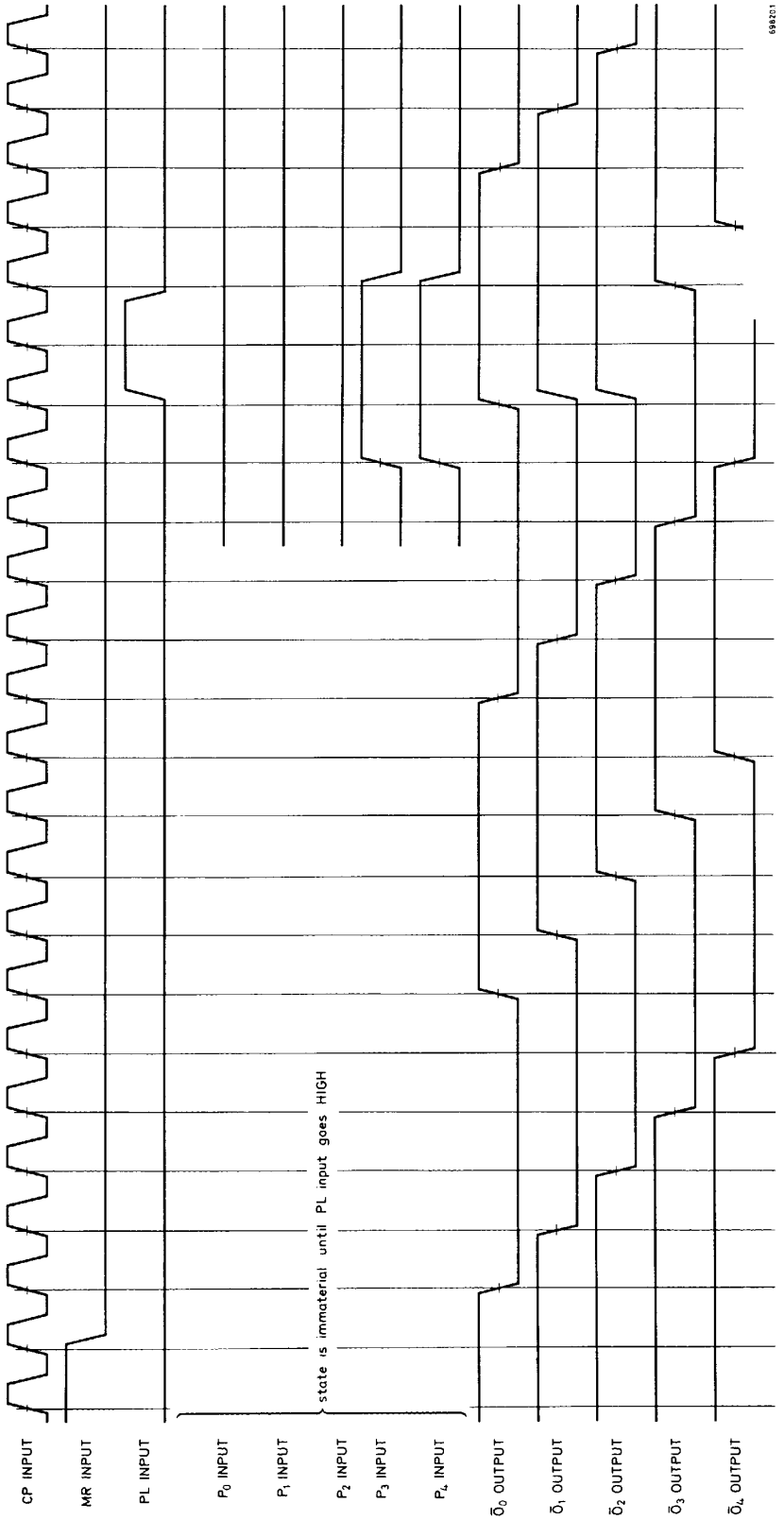


Fig. 7 Timing diagram.

**Note**

D input connected to $\overline{Q}_4$ for decade counter configuration.