

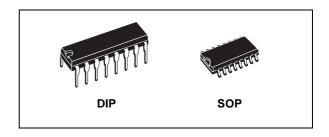


4 BIT D TYPE REGISTERS

- THREE STATE OUTPUTS
- INPUT DISABLE WITHOUT GATING THE CLOCK
- GATED OUTPUT CONTROL LINES FOR ENABLING OR DISABLING THE OUTPUTS
- BUFFERED INPUTS AND OUTPUTS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



HCF4076B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. HCF4076B is a four bit register consisting of D-TYPE flip-flops that feature three state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data

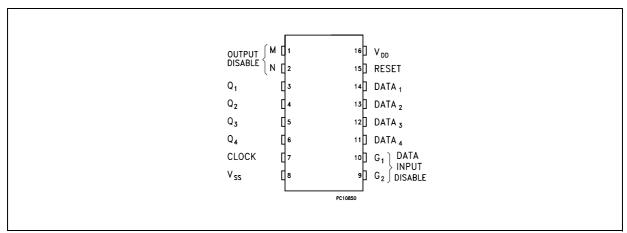


ORDER CODES

PACKAGE	TUBE	T&R
DIP	HCF4076BEY	
SOP	HCF4076BM1	HCF4076M013TR

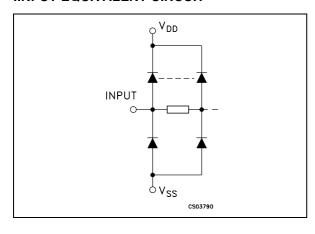
Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disable inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at either Output Disable input, and present a high impedance.

PIN CONNECTION



September 2002 1/9

IINPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

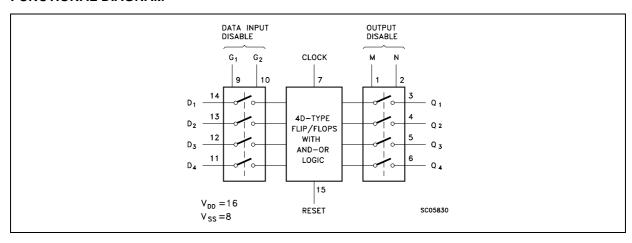
PIN No	SYMBOL	NAME AND FUNCTION
14, 13, 12, 11	DATA1 to DATA 4	D Inputs
10, 9	G1, G2	Data Input Disable Control
1, 2	M, N	Output Disable Control
7	CLOCK	Clock Input
15	RESET	Reset Input
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

TRUTH TABLE

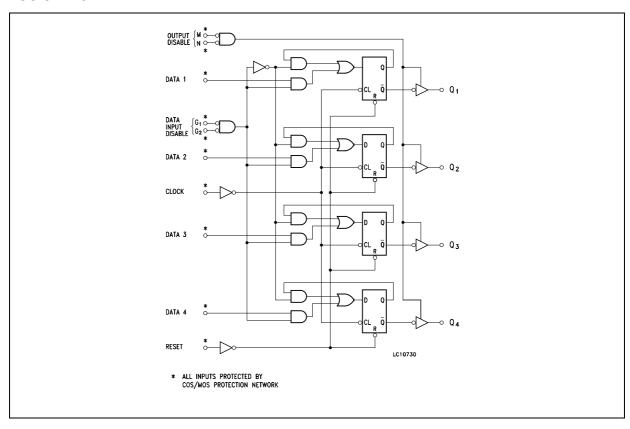
RESET	CLOCK	DATA INPU	DATA INPUT DISABLE		NEXT STATE	
KESEI	CLOCK	G1	G2	DATA D	OUTPUT	
Н	Х	X	Х	X	L	
L	L	X	X	X	Q	NO CHANGE
L	」	Н	X	X	Q	NO CHANGE
L		Х	Н	Х	Q	NO CHANGE
L		L	L	Н	Н	
L		L	L	L	L	
L	Н	Х	X	X	Q	NO CHANGE
L	7	X	X	X	Q	NO CHANGE

X : Don't Care
When either Output Disable M or N is high, the outputs are disabled (high impedance state) : however sequential operation of the flip-flop is not affected.

FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V _I	DC Input Voltage	-0.5 to V _{DD} + 0.5	V
I _I	DC Input Current	± 10	mA
P _D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T _{op}	Operating Temperature	-55 to +125	°C
T _{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V _I	Input Voltage	0 to V _{DD}	V
T _{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

			Test Con	dition		Value							
Symbol	Parameter	Vı	V _O	l _o	V_{DD}	Т	_A = 25°	С	-40 to	85°C	-55 to 125°C		Unit
		(V)	(V)	(μ A)	(V)	Min.	Тур.	Max.	Min.	Max.	Min.	Max.	
ΙL	Quiescent Current	0/5			5		0.04	5		150		150	
		0/10			10		0.04	10		300		300	^
		0/15			15		0.04	20		600		600	μΑ
		0/20			20		0.08	100		3000		3000	
V _{OH}	High Level Output	0/5		<1	5	4.95			4.95		4.95		
	Voltage	0/10		<1	10	9.95			9.95		9.95		V
		0/15		<1	15	14.95			14.95		14.95		
V _{OL}	Low Level Output	5/0		<1	5		0.05			0.05		0.05	
	Voltage	10/0		<1	10		0.05			0.05		0.05	V
		15/0		<1	15		0.05			0.05		0.05	
V _{IH}	High Level Input		0.5/4.5	<1	5	3.5			3.5		3.5		
	Voltage		1/9	<1	10	7			7		7		V
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input		4.5/0.5	<1	5			1.5		1.5		1.5	
	Voltage		9/1	<1	10			3		3		3	V
			13.5/1.5	<1	15			4		4		4	
I _{OH}	Output Drive	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		
	Current	0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		mA
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		ША
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I _{OL}	Output Sink	0/5	0.4	<1	5	0.44	1		0.36		0.36		
	Current	0/10	0.5	<1	10	1.1	2.6		0.9		0.9		mΑ
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
Ι _Ι	Input Leakage Current	0/18	Any In	put	18		±10 ⁻⁵	±0.1		±1		±1	μΑ
I _{OZ}	3-State Output Current	0/18			18		±10 ⁻⁴	±0.4		±12		±12	μΑ
C _I	Input Capacitance		Any In	put			5	7.5					рF

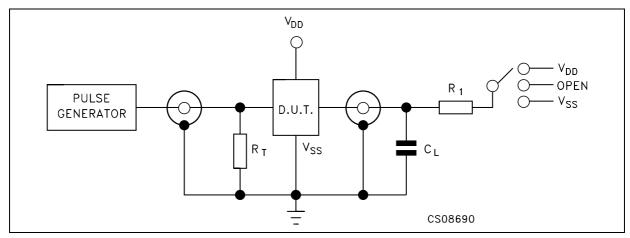
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} =5V, 2V min. with V_{DD} =10V, 2.5V min. with V_{DD} =15V

$\textbf{DYNAMIC ELECTRICAL CHARACTERISTICS} \; (\textbf{T}_{amb} = 25^{\circ} \textbf{C}, \;\; \textbf{C}_{L} = 50 \text{pF}, \; \textbf{R}_{L} = 200 \text{K}\Omega, \;\; \textbf{t}_{r} = \textbf{t}_{f} = 20 \; \text{ns})$

	_		Test Condition	,	Value (*)			
Symbol	Parameter	V _{DD} (V)		Min.	Тур.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Time	5			300	600		
	(Clock to Q Output)	10	1		125	250	ns	
		15	1		90	180		
t _{PHL(R)}	Propagation Delay Time	5			230	460		
()	(Reset)	10]		100	200	ns	
		15	1		75	150		
t _{P(1-H)}	3-State Out H or L to High	5			150	300		
. (,	Impedance	10	$R_L = 1K\Omega$		75	150	ns	
		15	1		60	120		
t _{P(L-1)}	3-State High Impedance to	5			150	300		
. (= .)	H or L Output	10	$R_L = 1K\Omega$		75	150	ns	
		15	1 -		60	120		
t _W	Clock Pulse Width	5		200	100			
		10	1	100	50		ns	
		15	1	80	40			
t _W	Reset Pulse Width	5		120	60			
		10	1	50	25		ns	
		15]	40	20			
t _{setup}	Data Setup Time	5		200	100			
		10	1	80	40		ns	
		15]	60	30			
t _{setup}	Data Input Disable Setup Time	5		180	90			
		10	1	100	50		ns	
		15]	70	35			
f _{max}	Maximum Clock Frequency	5		3	6			
		10	1	6	12		MHz	
		15	1	8	16			
t _{r,} t _f	Clock input Rise or Fall Time	5		15				
,		10	1	5			μs	
		15	1	5				

^(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

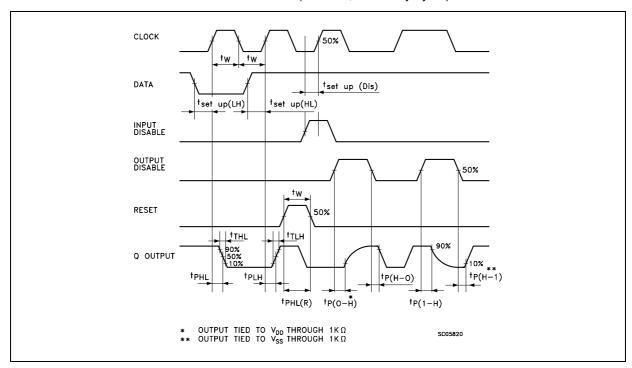
TEST CIRCUIT



TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ}	V_{DD}
t _{PZH} , t _{PHZ}	V_{SS}

C_L = 50pF or equivalent (includes jig and probe capacitance)

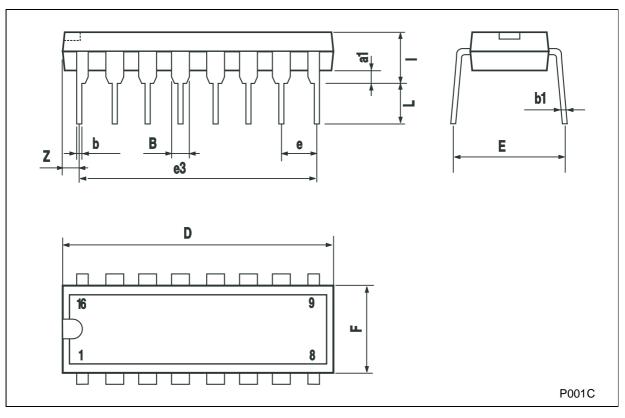
WAVEFORM: PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)



 $R_L = 200 K\Omega$ $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

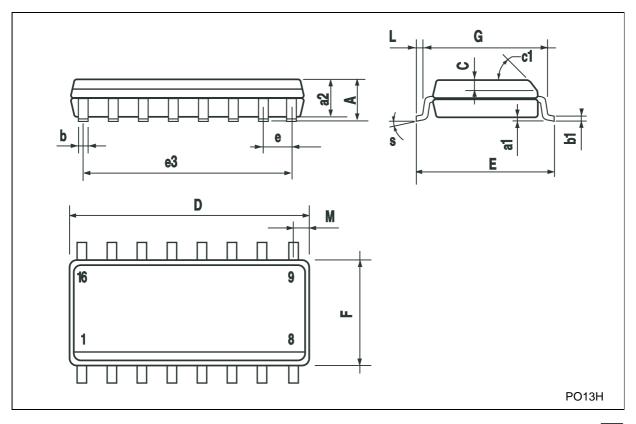
Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.		mm.				
DIWI.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
В	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
е		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



SO-16 MECHANICAL DATA

DIM		mm.		inch				
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.		
Α			1.75			0.068		
a1	0.1		0.2	0.003		0.007		
a2			1.65			0.064		
b	0.35		0.46	0.013		0.018		
b1	0.19		0.25	0.007		0.010		
С		0.5			0.019			
c1			45°	(typ.)				
D	9.8		10	0.385		0.393		
E	5.8		6.2	0.228		0.244		
е		1.27			0.050			
e3		8.89			0.350			
F	3.8		4.0	0.149		0.157		
G	4.6		5.3	0.181		0.208		
L	0.5		1.27	0.019		0.050		
М			0.62			0.024		
S			8° (max.)		•		



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