

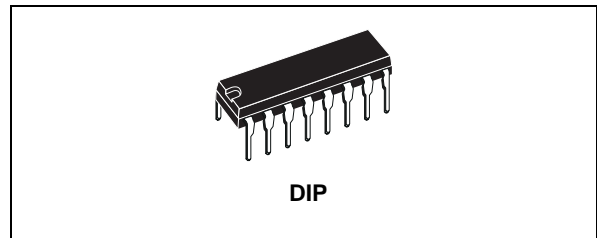
DUAL 64 STAGE STATIC SHIFT REGISTER

- CLOCK FREQUENCY 12MHz (Typ.)
at $V_{DD} = 10V$
- SCHMITT TRIGGER CLOCK INPUTS
ALLOWS OPERATION WITH VERY SLOW
CLOCK RISE AND FALL TIMES
- THREE STATE OUTPUTS
- QUIESCENT CURRENT SPECIFIED UP TO
20V
- STANDARDIZED, SYMMETRICAL OUTPUT
CHARACTERISTICS
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT
 $I_l = 100nA$ (MAX) AT $V_{DD} = 18V$ $T_A = 25^\circ C$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC
JESD13B "STANDARD SPECIFICATIONS
FOR DESCRIPTION OF B SERIES CMOS
DEVICES"

DESCRIPTION

HCF4517B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP package.

This device is a dual 64-stage static shift register consisting of two independent registers each having a clock, data, and write enable input and outputs accessible by stages following the 16th,

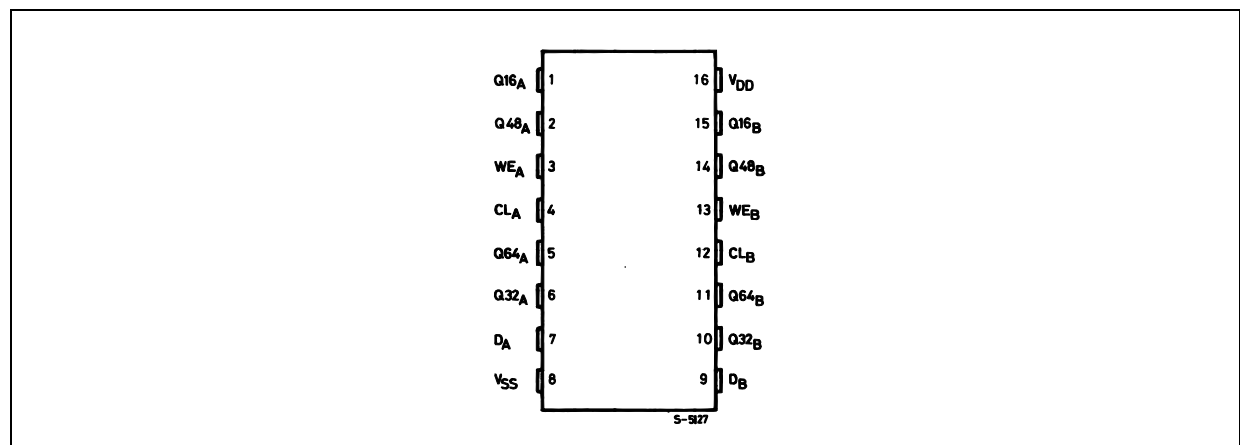


ORDER CODES

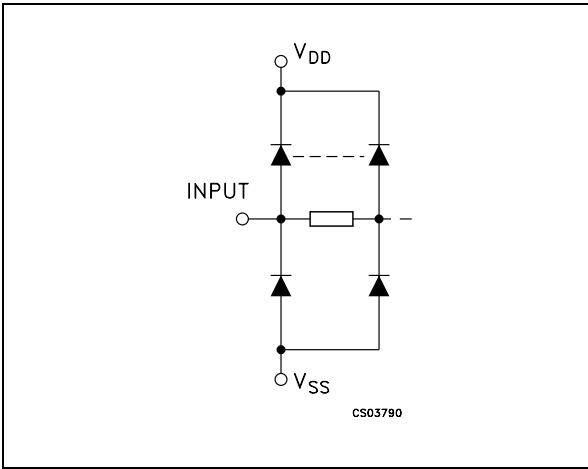
PACKAGE	TUBE	T & R
DIP	HCF4517BEY	
SOP	HCF4517BM1	HCF4517M013TR

32nd, 48th, and 64th stages. These stages also serve as input points allowing data to be put in at the 17th, 33rd, and 49th stages when the write enable input is a logic 1 and the clock goes through a low to high transition. The truth table indicates how the clock and write enable inputs control the operation of HCF4517B. Inputs at the intermediate stages allow entry of 64-bits into the register with 16 clock pulses. The 3-state outputs permit connection of this device to an external bus.

PIN CONNECTION



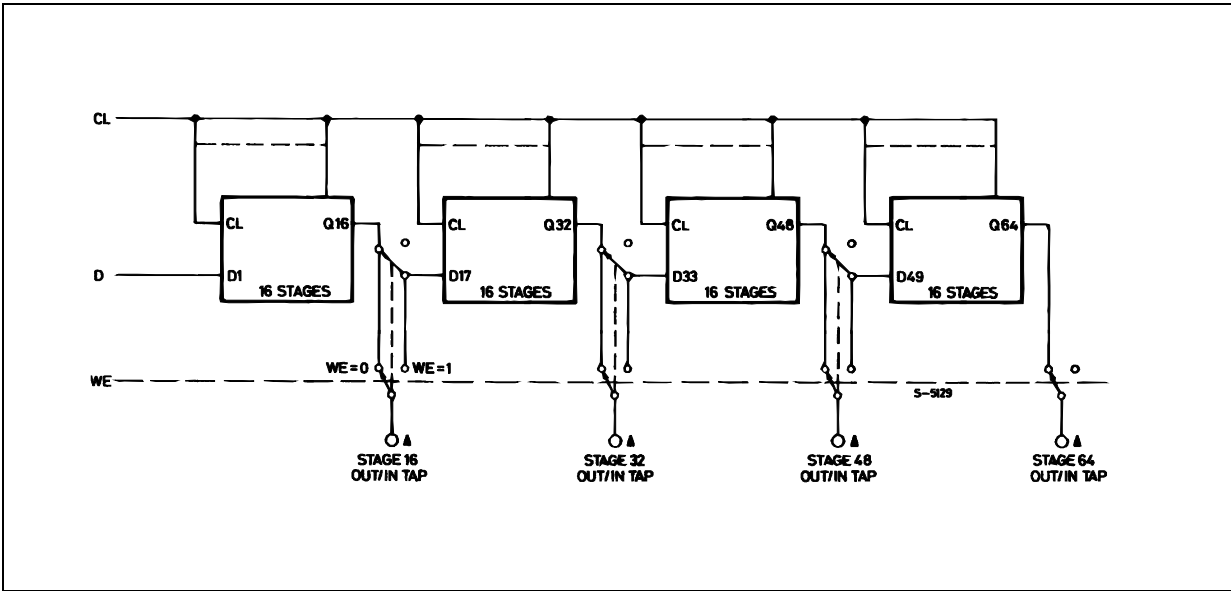
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 5, 6	QnA	IN/OUT Stage
10, 11,14, 15	QnB	IN/OUT Stage
3, 13	WEA, WEB	Write Enable
7, 9	DA, DB	Data Input
4, 12	CLA, CLB	Clock
8	V _{SS}	Negative Supply Voltage
16	V _{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM (One Half)



TRUTH TABLES

CLOCK	WRITE ENABLE	DATA	STAGE 16 TAP	STAGE 32 TAP	STAGE 48 TAP	STAGE 64 TAP
L	L	X	Q16	Q32	Q48	Q64
L	H	X	Z	Z	Z	Z
H	L	X	Q16	Q32	Q48	Q64
H	H	X	Z	Z	Z	Z
	L	DI In	Q16	Q32	Q48	Q64
	H	DI In	D17 In	D33 In	D49 In	Z
	L	X	Q16	Q32	Q48	Q64
	H	X	Z	Z	Z	Z

X : Don't Care

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I _L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V _{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V _{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V _{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V _{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I _{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I _{OL}	Output Sink Current Q	0/5	0.4	<1	5	1.74	4		1.43		1.43		mA
		0/10	0.5	<1	10	4.42	10.4		3.74		3.74		
		0/15	1.5	<1	15	11.56	27.2		9.52		9.52		
I _{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I _I	Input Leakage Current	0/18	Any Input		18		±10 ⁻⁵	±0.1		±1		±1	μA
I _{OZ}	3-State Output Leakage Current	0/18	Any Input		18		±10 ⁻⁴	±0.4		±12		±12	μA
C _I	Input Capacitance		Any Input				5	7.5					pF

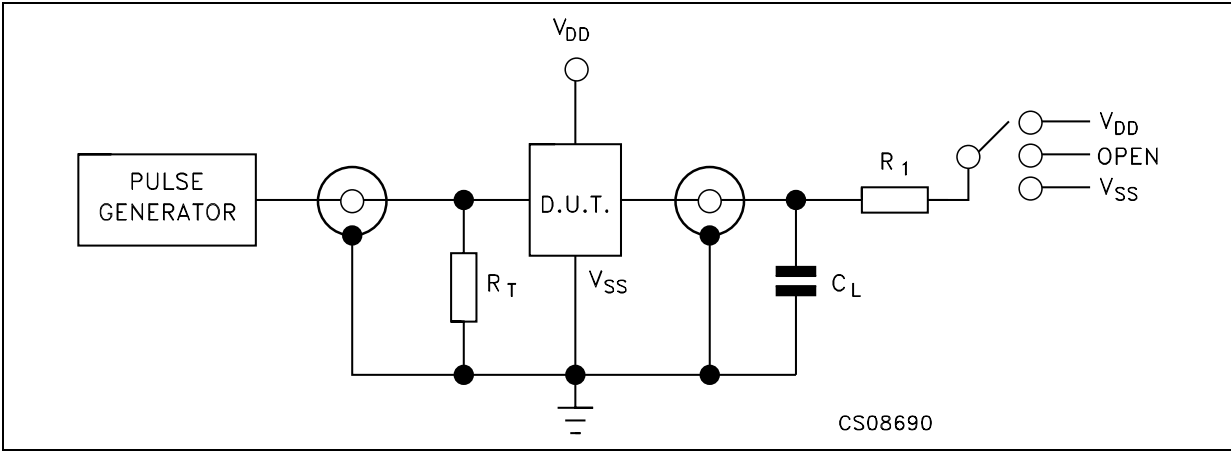
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50\text{pF}$, $R_L = 200\text{K}\Omega$, $t_r = t_f = 20\text{ ns}$)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PHL} t_{PLH}	Propagation Delay Time : CL to Bit 16 Tap	5			200	400	ns
		10			110	220	
		15			90	180	
t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	3-State Output WE to Bit 16 Tap (see note)	5			75	150	ns
		10			40	80	
		15			30	60	
t_{THL} t_{TLH}	Output Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_{setup}	Setup Time (WRITE ENABLE to CLOCK)	5		-100	-50		ns
		10		-50	-25		
		15		-30	-15		
t_{setup}	Setup Time (DATA to CLOCK)	5		-100	-50		ns
		10		-60	-30		
		15		-30	-15		
	Release Time (WRITE ENABLE to CLOCK)	5			50	100	ns
		10			25	50	
		15			20	40	
t_{hold}	Hold Time (DATA to CLOCK)	5			100	200	ns
		10			50	100	
		15			25	50	
t_W	Minimum Clock Pulse Width	5			90	180	ns
		10			40	80	
		15			25	50	
f_{CL}	Maximum Clock Input Frequency	5		3	6		MHz
		10		6	12		
		15		8	15		
t_r t_f	Maximum Clock Input Rise or Fall Time	5		Unlimited			μs
		10					
		15					

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.NOTE : Measured at the point of 10% change in output load of 50pF, $R_L = 1\text{K}\Omega$ to V_{DD} for t_{PZL} , t_{PLZ} and $R_L = 1\text{K}\Omega$ to V_{SS} for t_{PHZ}

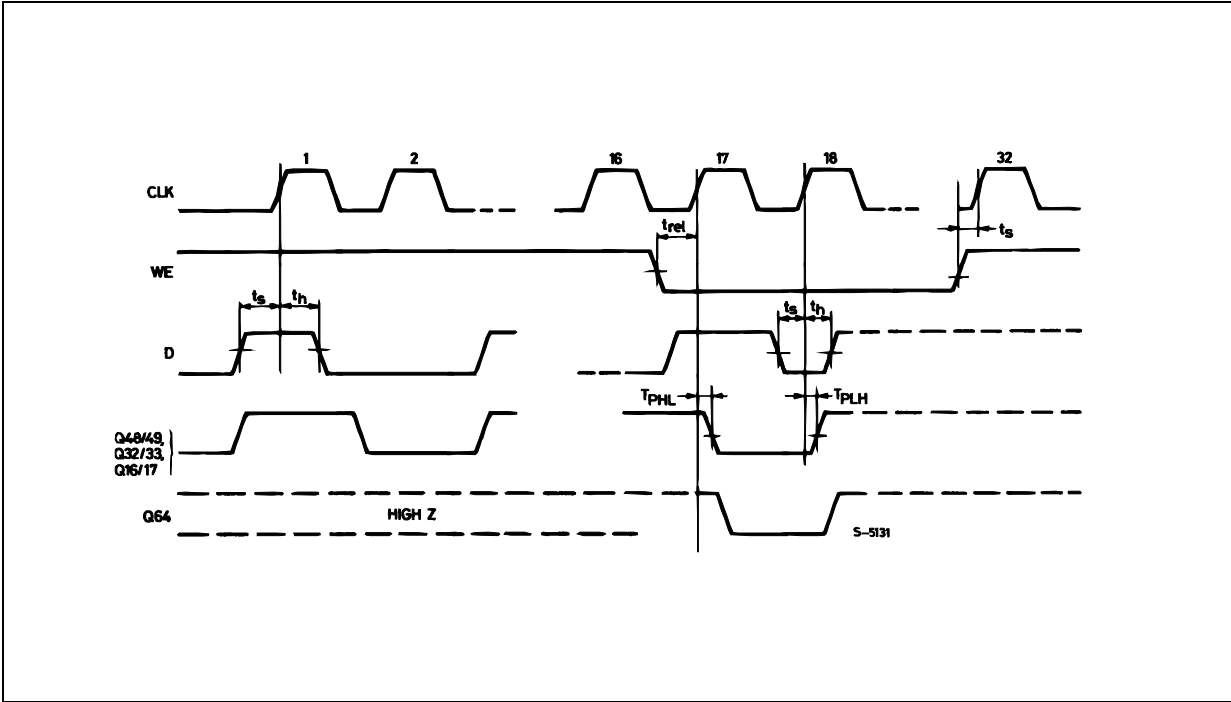
TEST CIRCUIT



TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	V_{DD}
t_{PZH} , t_{PHZ}	V_{SS}

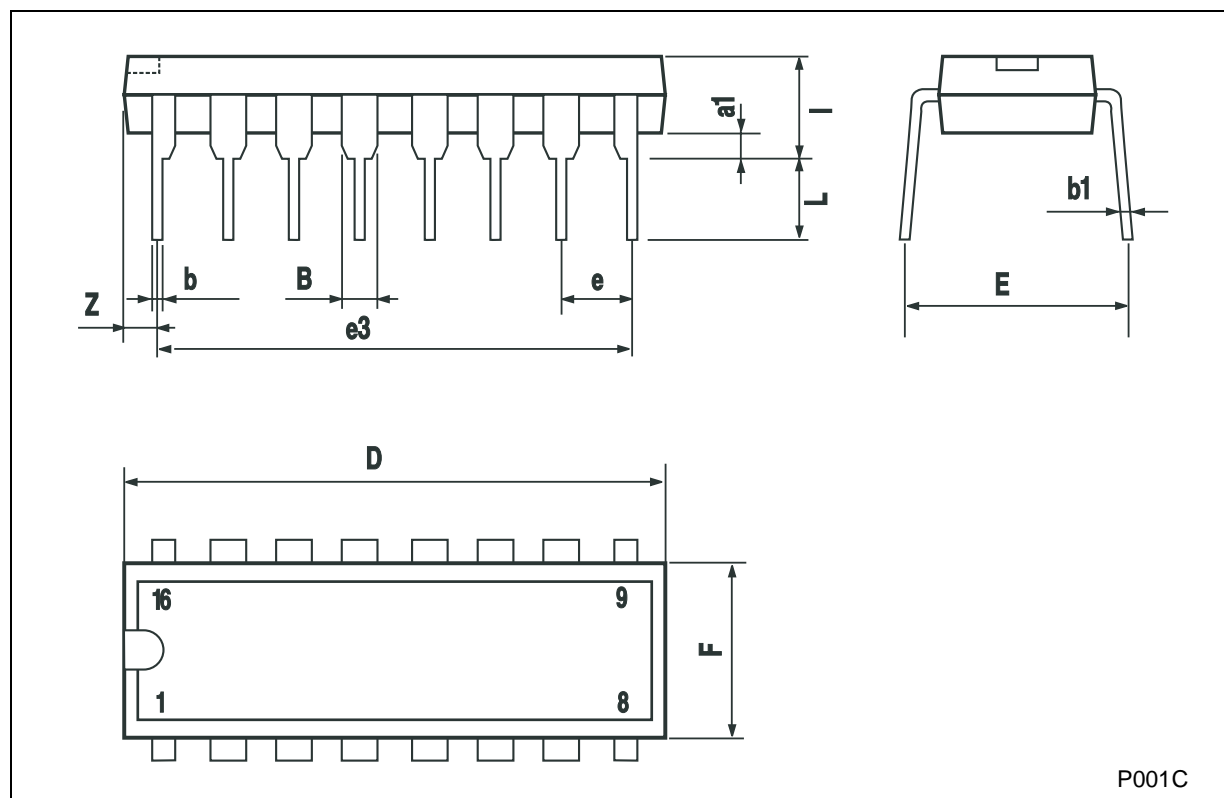
C_L = 50pF or equivalent (includes jig and probe capacitance)
 R_L = 200K Ω
 R_T = Z_{OUT} of pulse generator (typically 50 Ω)

WAVEFORM : PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)



Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



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