DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4104B
MSI
Quadruple low to high voltage translator with 3-state outputs

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

Quadruple low to high voltage translator with 3-state outputs

HEF4104B MSI

DESCRIPTION

The HEF4104B quadruple low voltage to high voltage translator with 3-state outputs provides the capability of interfacing low voltage circuits to high voltage circuits, such as low voltage LOCMOS and TTL to high voltage LOCMOS. It has four data inputs (I_0 to I_3), an active HIGH output enable input (EO), four data outputs (O_0 to O_3) and their complements ($\overline{O}_0$ to $\overline{O}_3$).

With EO HIGH, O_0 to O_3 and $\overline{O}_0$ to $\overline{O}_3$ are in the low impedance ON-state, either HIGH or LOW as determined by I_0 to I_3; with EO LOW, O_0 to O_3 and $\overline{O}_0$ to $\overline{O}_3$ are in the high impedance OFF-state.

The device uses a common negative supply (V_{SS}) and separate positive supplies for inputs (V_{DDI}) and outputs (V_{DDO}). V_{DDI} must always be less than or equal to V_{DDO}, even during power turn-on and turn-off. For the permissible operating range of V_{DDI} and V_{DDO} see graph Fig.4.

Each input protection circuit is terminated between V_{DDO} and V_{SS}. This allows the input signals to be driven from any potential between V_{DDO} and V_{SS}, without regard to current limiting. When driving from potentials greater than V_{DDO} or less than V_{SS}, the current at each input must be limited to 10 mA.

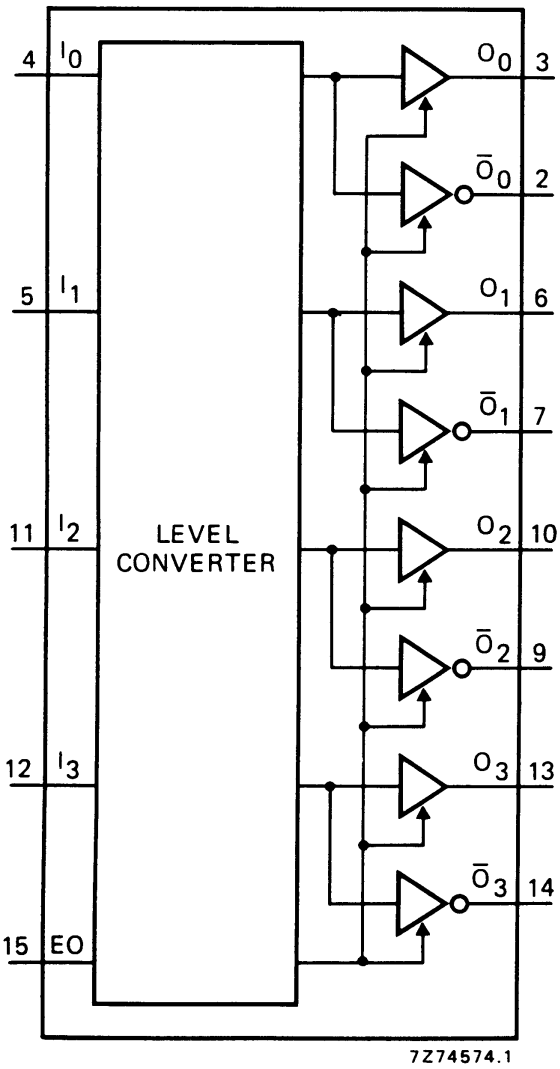

Fig.1 Functional diagram.

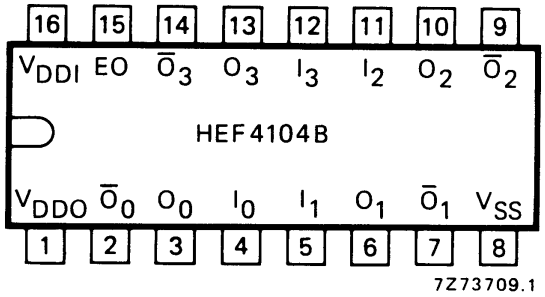

Fig.2 Pinning diagram.

HEF4104BP(N):	16-lead DIL; plastic (SOT38-1)
HEF4104BD(F):	16-lead DIL; ceramic (cerdip) (SOT74)
HEF4104BT(D):	16-lead SO; plastic (SOT109-1)

( ): Package Designator North America

PINNING

I_0 to I_3	data inputs
EO	output enable input
O_0 to O_3	data outputs
$\overline{O}_0$ to $\overline{O}_3$	complementary data outputs

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

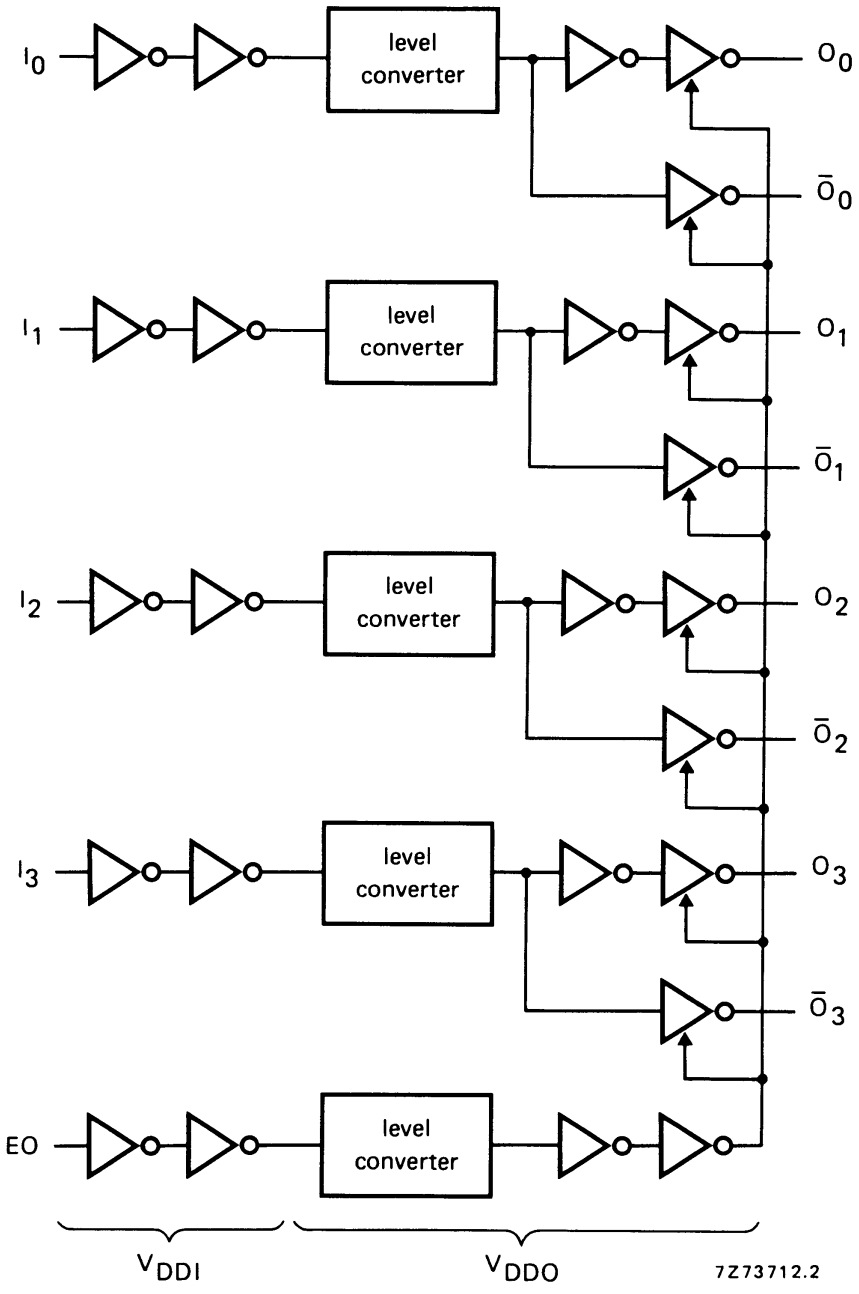

Fig.3 Logic diagram.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
$I_n \rightarrow O_n, \overline{O}_n$	5		170	340	ns	143 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	80	160	ns	69 ns + (0,23 ns/pF) C_L
	15		65	135	ns	57 ns + (0,16 ns/pF) C_L
	5		170	340	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	80	160	ns	69 ns + (0,23 ns/pF) C_L
	15		70	140	ns	62 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
3-state propagation delays						
Output disable times						
$EO \rightarrow O_n, \overline{O}_n$	5		70	135	ns	
HIGH	10	t_{PHZ}	55	110	ns	
	15		60	120	ns	
	5		70	135	ns	
LOW	10	t_{PLZ}	55	105	ns	
	15		55	110	ns	
Output enable times						
$EO \rightarrow O_n, \overline{O}_n$	5		195	395	ns	
HIGH	10	t_{PZH}	95	195	ns	
	15		80	165	ns	
	5		195	395	ns	
LOW	10	t_{PZL}	95	190	ns	
	15		80	160	ns	

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$3\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where
	10	$12\,200\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	15	$31\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\sum (f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

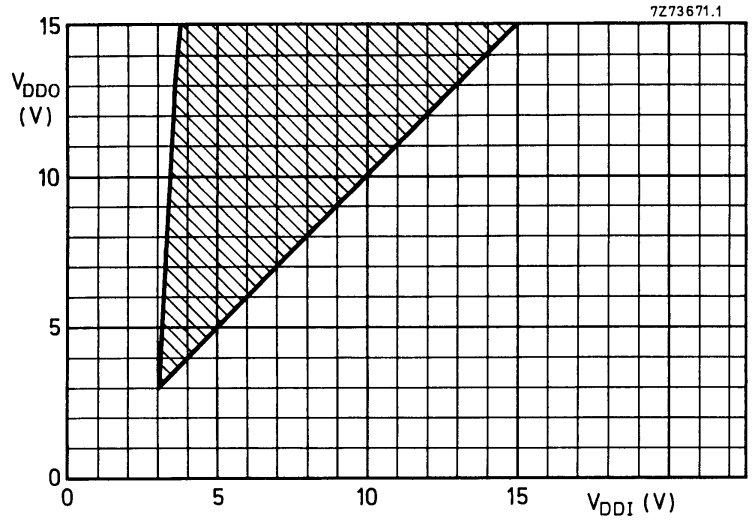

Fig.4 V_{DDO} as a function of V_{DDI}; the shaded area shows the permissible operating range.