CD4031BMS

December 1992

CMOS 64-Stage Static Shift Register

Features

- **High Voltage Type (20V Rating)**
- **Fully Static Operation: DC to 12MHz (typ.) at VDD - VSS = 15V**
- **Standard TTL Drive Capability on Q Output**
- **Recirculation Capability**
- **Three Cascading Modes:**
  - **Direct Clocking for High-Speed Operation**
  - **Delayed Clocking for Reduced Clock Drive Requirements**
  - **Additional 1/2 Stage for Slow Clocks**
- **100% Tested For Quiescent Current at 20V**
- **Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range;**
  - **100nA at 18V and +25°C**
- **Noise Margin (Over Full Package Temperature Range):**
  - **1V at VDD = 5V**
  - **2V at VDD = 10V**
  - **2.5V at VDD = 15V**
- **5V, 10V and 15V Parametric Ratings**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications

- **Serial Shift Registers**
- **Time Delay Circuits**

Description

The CD4031BMS is a static shift register that contains 64 D-type, master-slave flip-flop stages and one stage which is a D-type master flip-flop only (referred to as a 1/2 stage).

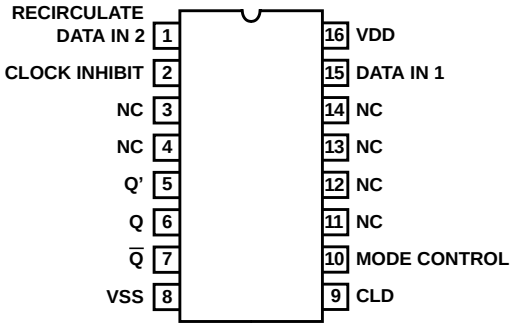
The logic level present at the DATA input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 12MHz (typical) can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the low or high state. The CD4031BMS has a MODE CONTROL input that, when in the high state, allows operation in the recirculating mode. The MODE CONTROL input can also be used to select between two separate data sources. Register packages can be cascaded and the clock lines driven directly for high-speed operation. Alternatively, a delayed clock output (CLD) is provided that enables cascading register packages while allowing reduced clock drive fan-out and transition-time requirements. A third cascading option makes use of the Q' output from the 1/2 stage, which is available on the next negative-going transition of the clock after the Q output occurs. This delayed output, like the delayed clock CLD, is used with clocks having slow rise and fall times.

The CD4031BMS is supplied in these 16 lead outline packages:

Braze Seal DIP	H4X
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

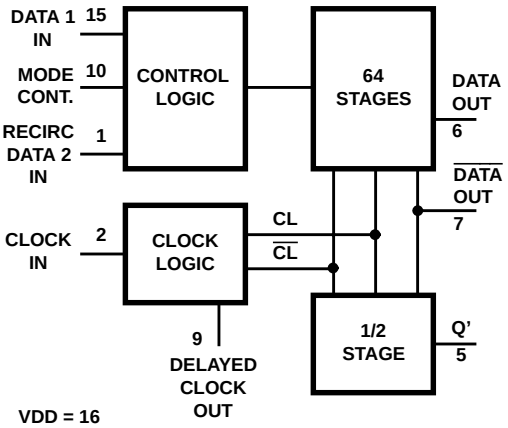
Pinout

CD4031BMS
TOP VIEW



NC = NO CONNECTION

Functional Diagram



VDD = 16
VSS = 8
NC = 3, 4, 11, 12, 13, 14

File Number **3306**

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Operating Temperature Range . . . . . -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . . +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) . . . . . Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current $\overline{Q}$, Q', CLD	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.51	-	mA
	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.3	-	mA
	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.4	-	mA
Output Current Q	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	2.04	-	mA
Output Current Q	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	5.2	-	mA
Output Current Q	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	13.6	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.51	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.6	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.3	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.4	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to $\overline{Q}$	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Propagation Delay Clock to Q	TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Propagation Delay Clock to Q	TPHL2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	380	ns
			10, 11	+125°C, -55°C	-	513	ns
Propagation Delay Clock to Q'	TPLH3 TPHL3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	380	ns
			10, 11	+125°C, -55°C	-	513	ns
Propagation Delay $\overline{\text{Clock}}$ to CLD	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency (See Note 5; Table 3)	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	2	-	MHz
			10, 11	+125°C, -55°C	1.48	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink) $\overline{Q}$, Q', CLD Outputs	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink) $\overline{Q}$, Q', CLD Outputs	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink) $\overline{Q}$, Q', CLD Outputs	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Sink) Q Outputs	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	1.44	-	mA
				-55°C	2.56	-	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Current (Sink) Q Outputs	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	3.6	-	mA
				-55°C	6.4	-	mA
Output Current (Sink) Q Outputs	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	9.6	-	mA
				-55°C	16.8	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Clock to $\overline{Q}$	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	220	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay Clock to Q	TPLH2	VDD = 10V	1, 2, 3	+25°C	-	220	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay Clock to Q	TPHL2	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Propagation Delay Clock to CLD	TPLH3 TPHL3	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Propagation Delay $\overline{\text{Clock}}$ to Q'	TPLH4 TPHL4	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency (Note 5)	FCL	VDD = 10V	1, 2, 3	+25°C	-	5	MHz
		VDD = 15V	1, 2, 3	+25°C	-	6	MHz
Clock Input Rise or Fall Time (Note 4)	TRCL TFCL	VDD = 5V	1, 2, 3	+25°C	-	1000	µs
		VDD = 10V	1, 2, 3	+25°C	-	1000	µs
		VDD = 15V	1, 2, 3	+25°C	-	200	µs
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	60	ns
		VDD = 10V	1, 2, 3	+25°C	-	30	ns
		VDD = 15V	1, 2, 3	+25°C	-	20	ns
Minimum Data Hold Time	TH	VDD = 5V	1, 2, 3	+25°C	-	60	ns
		VDD = 10V	1, 2, 3	+25°C	-	30	ns
		VDD = 15V	1, 2, 3	+25°C	-	20	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	240	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. If more than one unit is cascaded in the parallel clocked application, TRCL should be made ≤ the sum of the propagation delay at 50pF and the transition time of the output driving stage.
5. Maximum clock frequency for cascaded units;

   a) Using Delayed Clock feature in recirculation mode:

   $$FMAX = \frac{1}{(n-1)\,CL,\ \text{prop delay and Q prop delay and set} - \text{up time}}$$ where n = number of packages

   b) Not using Delayed Clock:

   $$FMAX = \frac{1}{\text{propagation delay and set} - \text{up time}}$$

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V (Worst Case)	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES:

1. All voltages referenced to device GND.
2. VDD = 5V, CL = 50pF, RL = 200K
3. See Table 2 for +25°C limit.

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25^{O}C

PARAMETER	SYMBOL	DELTA LIMIT
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

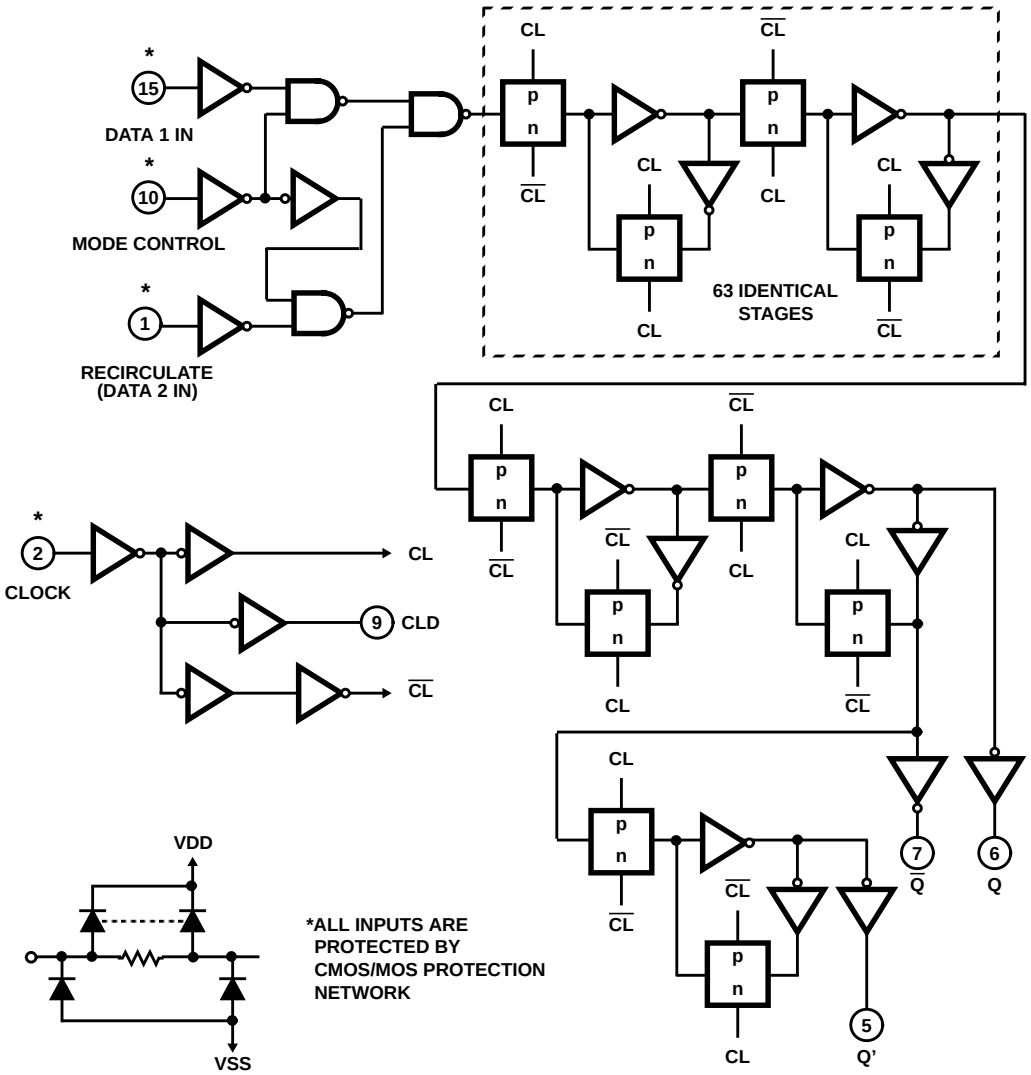
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	3 - 7, 9, 11 - 14	1, 2, 8, 10, 15	16			
Static Burn-In 2 Note 1	3 - 7, 9, 11 - 14	8	1, 2, 10, 15, 16			
Dynamic Burn-In Note 1	3 - 5, 11 - 14	8, 15	1, 16	6, 7, 9	2	10
Irradiation Note 2	3 - 7, 9, 11 - 14	8	1, 2, 10, 15, 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram



INPUT CONTROL CIRCUIT TRUTH TABLE

DATA	RECIR	MODE	BIT INTO STAGE 1
1	X	0	1
0	X	0	0
X	1	1	1
X	0	1	0

1 = High Level 0 = Low Level
X = Don't Care NC = No Change

TYPICAL STAGE TRUTH TABLE

DATA	CL	DATA + 1
0	⌐	0
1	⌐	1
X	⌐	NC

1 = High Level 0 = Low Level
X = Don't Care NC = No Change

TRUTH TABLE FOR OUTPUT FROM Q' (TERMINAL 5)

DATA + 64	CL	DATA + 64 1/2
0	⌐	0
1	⌐	1
X	⌐	NC

1 = High Level 0 = Low Level
X = Don't Care NC = No Change

Typical Performance Characteristics

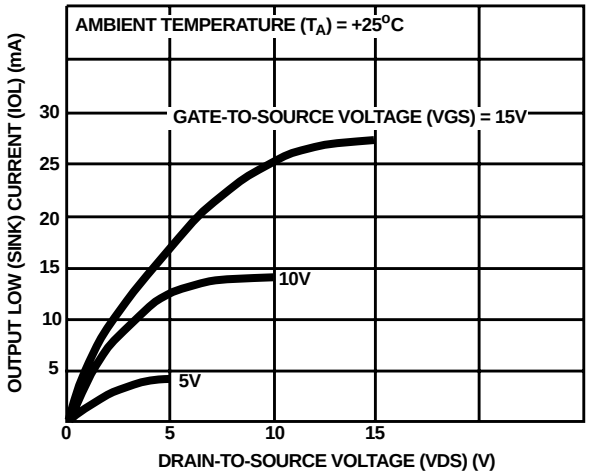


FIGURE 1 . TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS (Q SINK CURRENT = 4X ORDINATE)

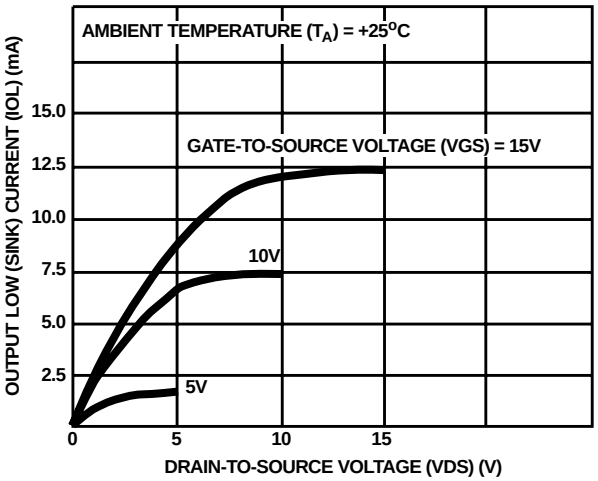


FIGURE 2. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS (Q SINK CURRENT = 4X ORDINATE)

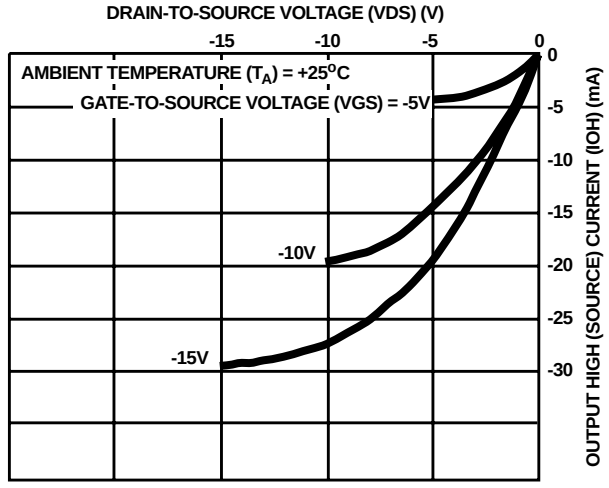


FIGURE 3. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

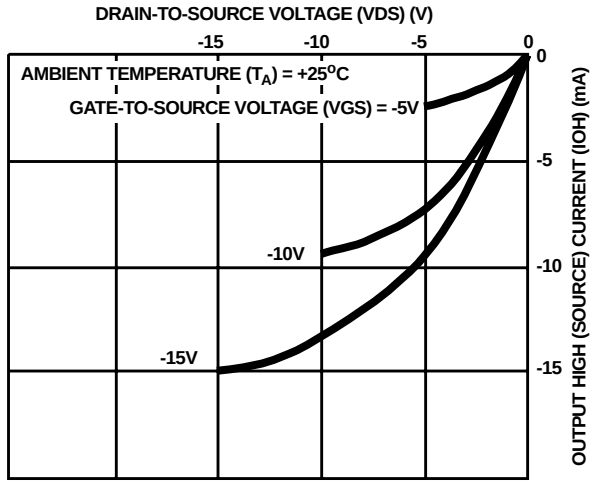


FIGURE 4. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

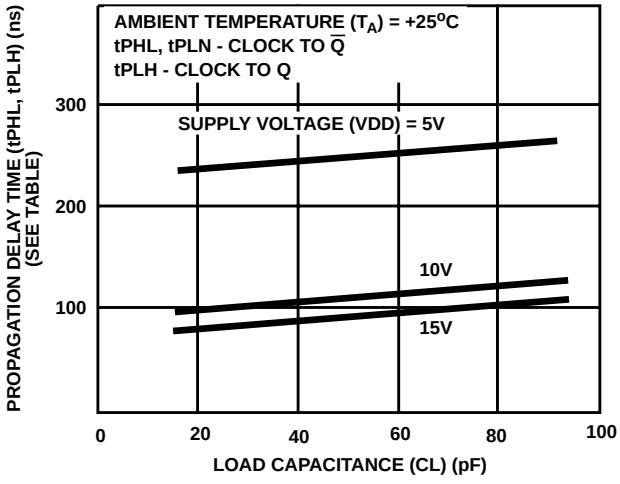


FIGURE 5. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (SEE TABLE)

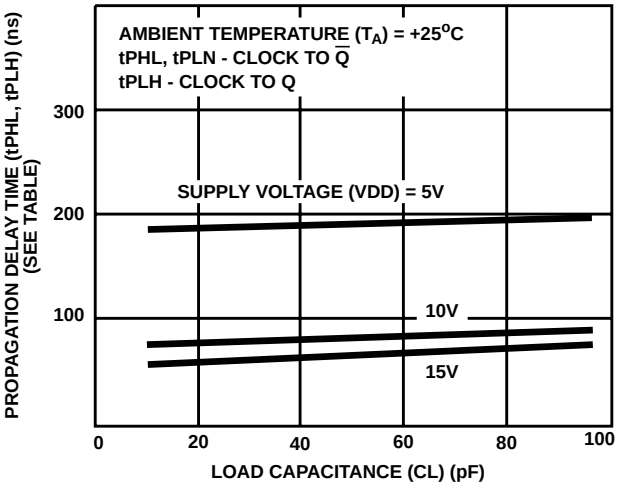


FIGURE 6. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (SEE TABLE)

Typical Performance Characteristics (Continued)

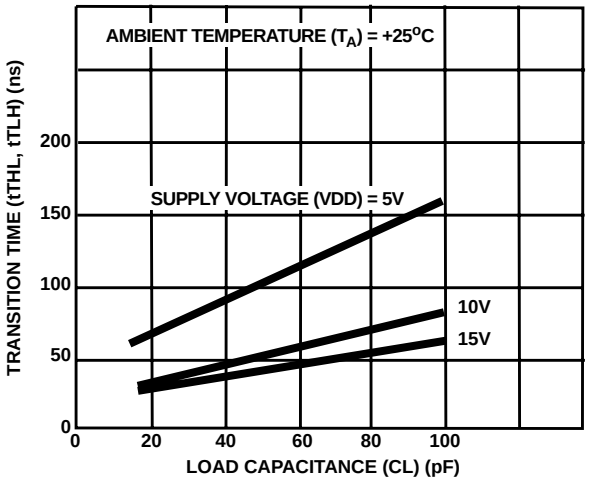


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE (EXCEPT Q, tTHL)

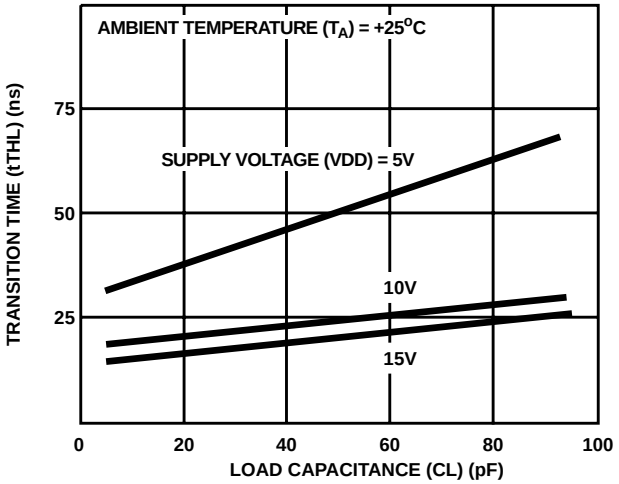


FIGURE 8. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE (Q, tTHL)

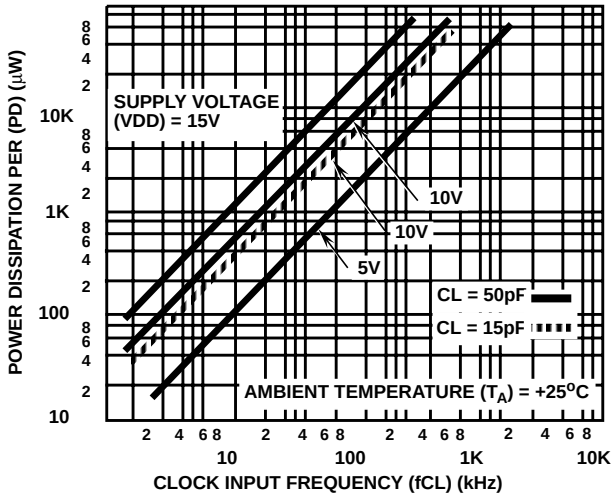


FIGURE 9. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF CLOCK INPUT FREQUENCY

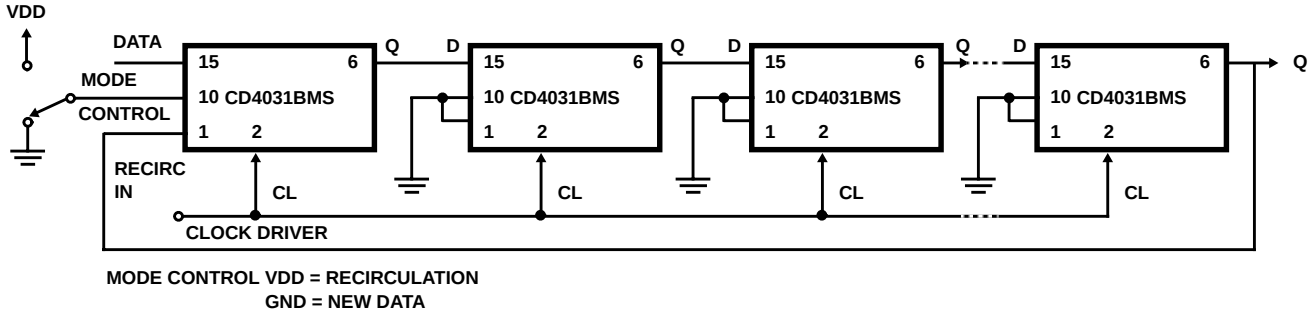


FIGURE 10. CASCADING USING DIRECT CLOCKING FOR HIGH-SPEED OPERATION (SEE CLOCK RISE AND FALL TIME REQUIREMENT)

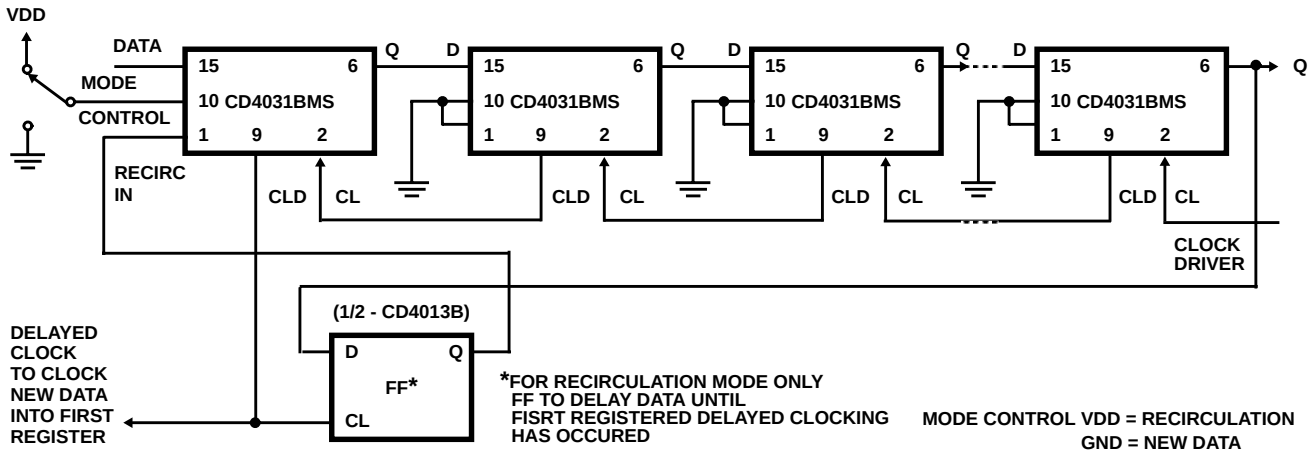


FIGURE 11. CASCADING USING DELAYED CLOCKING FOR REDUCED CLOCK DRIVE REQUIREMENTS

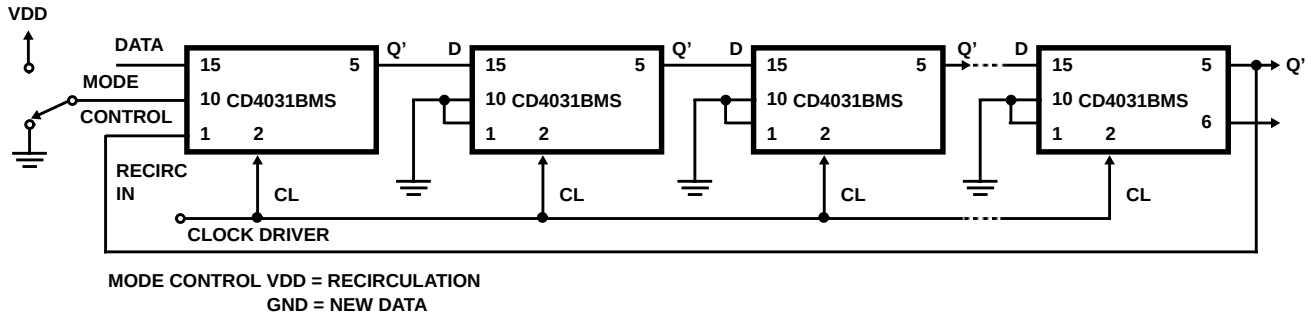
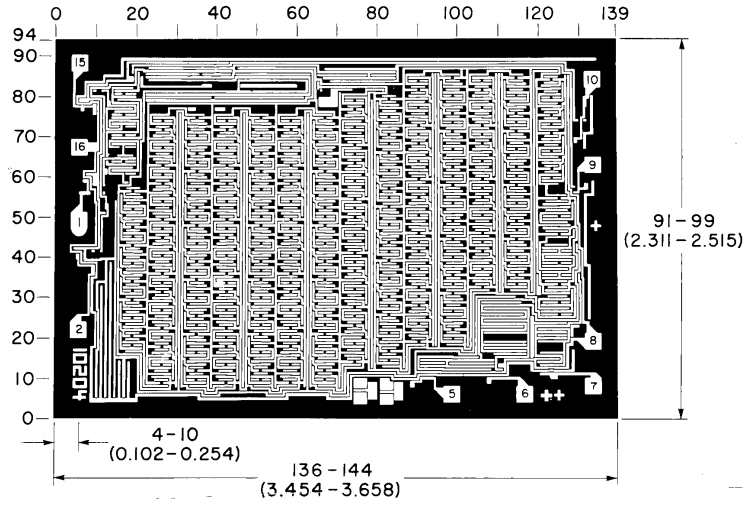


FIGURE 12. CASCADING USING HALF-CLOCK-PULSE DELAYED OUTPUT (Q') TO PERMIT USE OF SLOW RISE AND FALL CLOCK INPUTS

Chip Dimensions and Pad Layout



METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)