MC14035B

4-Bit Parallel-In/Parallel-Out Shift Register

The MC14035B 4–bit shift register is constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. It consists of a 4–stage clocked serial–shift register with synchronous parallel inputs and buffered parallel outputs. The Parallel/Serial (P/S) input allows serial–right shifting of data or synchronous parallel loading via inputs D_{P0} thru D_{P3}. The True/Complement (T/C) input determines whether the outputs display the Q or $\overline{Q}$ outputs of the flip–flop stages. J–K logic forms the serial input to the first stage. With the J and K inputs connected together they operate as a serial "D" input.

This device may be effectively used for shift–right/shift–left registers, parallel–to–serial/serial–to–parallel conversion, sequence generation, up/down Johnson or ring counters, pseudo–random code generation, frequency and phase comparators, sample and hold registers, etc . . .

- 4–Stage Clocked Serial–Shift Operation
- Synchronous Parallel Loading of all Four Stages
- J–K Serial Inputs on First Stage
- Asynchronous True/Complement Control of all Outputs
- Fully Static Operation
- Asynchronous Master Reset
- Data Transfer Occurs on the Positive–Going Clock Transition
- No Limit on Clock Rise and Fall Times
- All Inputs are Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

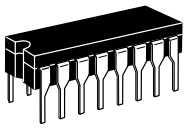
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

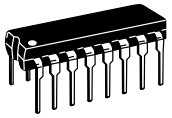
TRUTH TABLE

Inputs				t_n Output
C	J	$\overline{K}$	R	Q_0
↗	0	0	0	0
↗	0	1	0	Q0 (n – 1)
↗	1	0	0	$\overline{Q0}$ (n – 1)
↗	1	1	0	1
↘	X	X	0	Q0 (n – 1)
X	X	X	1	0

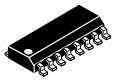
X = Don't Care
P/S = 0 = Serial Mode
T/C = 1 = True Outputs



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



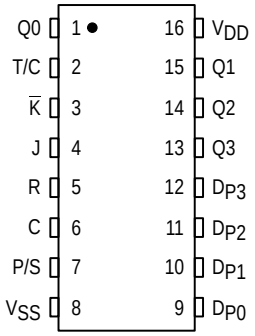
D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

T_A = – 55° to 125°C for all packages.

PIN ASSIGNMENT



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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs all buffers switching)	I_T	5.0 10 15	I_T = (1.0 µA/kHz) f + I_{DD} I_T = (2.0 µA/kHz) f + I_{DD} I_T = (3.0 µA/kHz) f + I_{DD}							µAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C, See Figure 1)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
T_{TLH}, T_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	—	100	200	
T_{TLH}, T_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
T_{TLH}, T_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	—	40	80	
Propagation Delay Time, Clock or Reset to Q	t_{PLH},					ns
T_{PLH}, T_{PHL} = (1.75 ns/pF) C_L + 223 ns	t_{PHL}	5.0	—	300	600	
T_{PLH}, T_{PHL} = (0.70 ns/pF) C_L + 89 ns		10	—	130	260	
T_{PLH}, T_{PHL} = (0.53 ns/pF) C_L + 67 ns		15	—	95	190	
Clock Pulse Width	t_{WH}	5.0	335	135	—	ns
		10	165	45	—	
		15	125	40	—	
Reset Pulse Width	t_{WH}	5.0	400	80	—	ns
		10	175	40	—	
		15	130	35	—	
Reset Removal Time	t_{rem}	5.0	80	40	—	ns
		10	30	15	—	
		15	25	10	—	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			—
		10				
		15				
Clock Pulse Frequency	f_{cl}	5.0	—	2.5	1.2	MHz
		10	—	6.0	2.0	
		15	—	10	3.0	
J–$\overline{K}$ to Clock Setup Time	t_{su}	5.0	500	120	—	ns
		10	200	50	—	
		15	150	30	—	
Clock to J–$\overline{K}$ Hold Time	t_h	5.0	40	– 40	—	ns
		10	30	– 5	—	
		15	25	0	—	
P/S to Clock Setup Time	t_{su}	5.0	500	25	—	ns
		10	200	10	—	
		15	150	7.5	—	
Clock to P/S Hold Time	t_h	5.0	30	– 70	—	ns
		10	20	– 20	—	
		15	20	– 10	—	
D_P to Clock Setup Time	t_{su}	5.0	500	90	—	ns
		10	200	20	—	
		15	150	15	—	
Clock to D_P Hold Time	t_h	5.0	90	– 25	—	ns
		10	40	0	—	
		15	40	5	—	

* The formulas given are for the typical characteristics only at 25°C.
#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

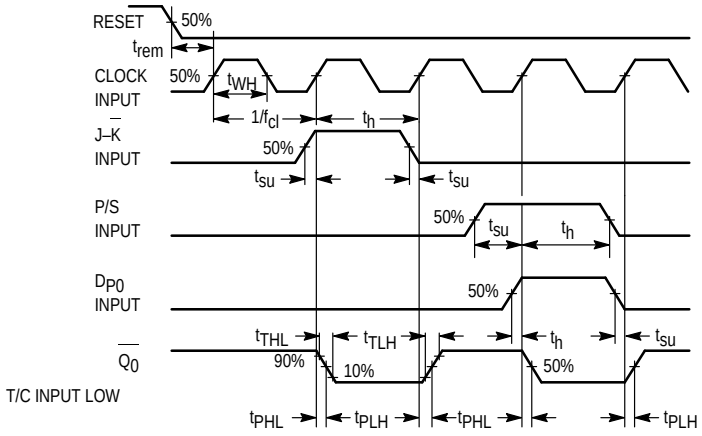
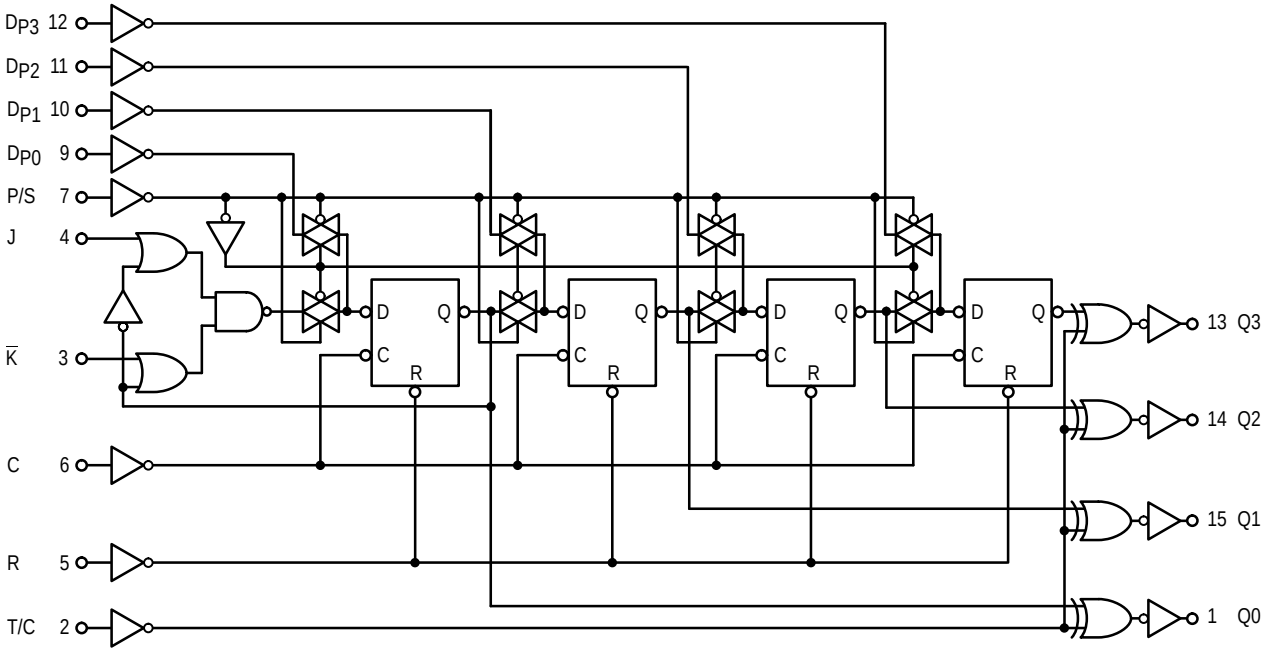
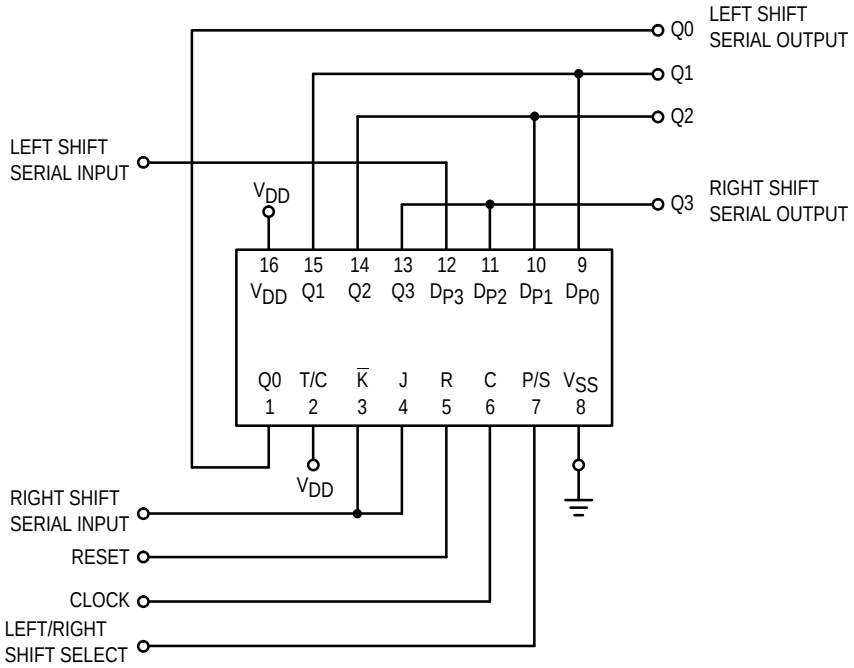


Figure 1. Timing Diagram

LOGIC DIAGRAM

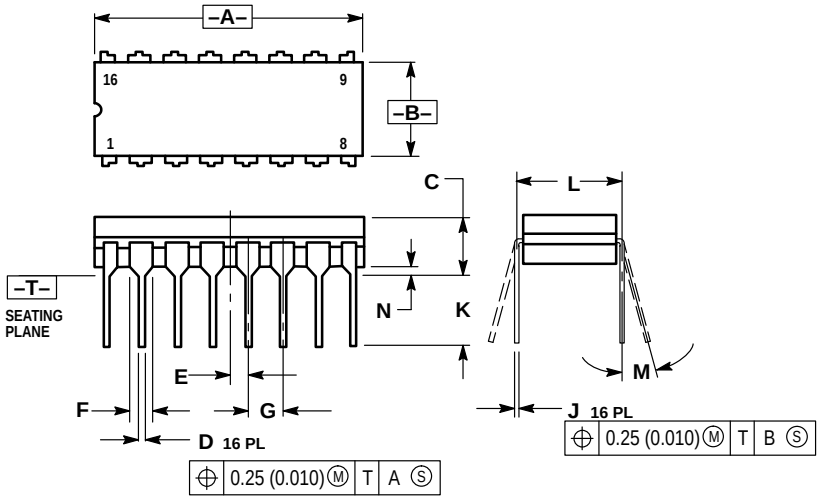


APPLICATION DIAGRAM
Shift Left/Shift Right Register



OUTLINE DIMENSIONS

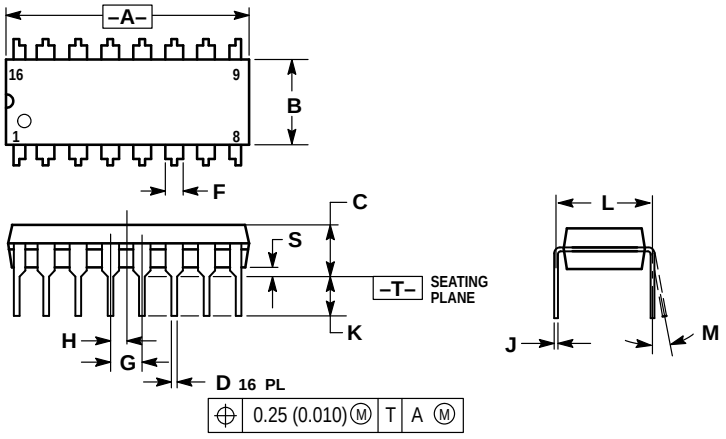
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

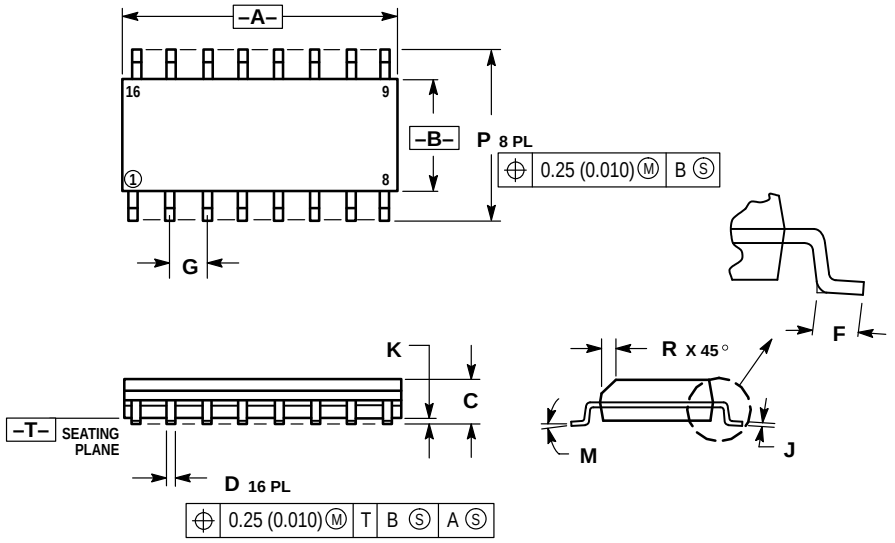


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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