Triple buffer
Rev. 12 — 15 December 2016

Product data sheet

1. **General description**

The 74LVC3G34 provides three buffers.

The inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of the 74LVC3G34 as a translator in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

Features and benefits 2.

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ♦ MM JESD22-A115-A exceeds 200 V
- \pm 24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



3. Ordering information

Table 1. Ordering information

Type number	Package						
	Temperature range	Name	Description	Version			
74LVC3G34DP	–40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2			
74LVC3G34DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1			
74LVC3G34GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 \times 1.95 \times 0.5 mm	SOT833-1			
74LVC3G34GF	–40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 \times 1 \times 0.5 mm	SOT1089			
74LVC3G34GD	–40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body $3 \times 2 \times 0.5$ mm	SOT996-2			
74LVC3G34GM	–40 °C to +125 °C	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 \times 1.6 \times 0.5 mm	SOT902-2			
74LVC3G34GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 \times 1.0 \times 0.35 mm	SOT1116			
74LVC3G34GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 \times 1.0 \times 0.35 mm	SOT1203			

4. Marking

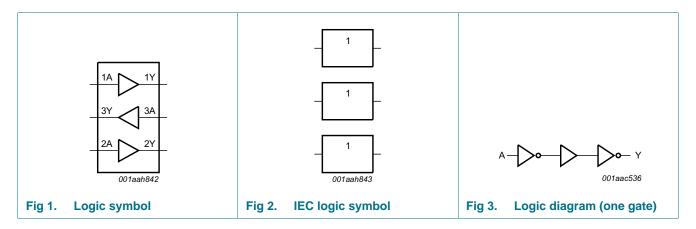
Table 2. Marking codes

Type number	Marking code ^[1]
74LVC3G34DP	V34
74LVC3G34DC	Y34
74LVC3G34GT	Y34
74LVC3G34GF	YA
74LVC3G34GD	Y34
74LVC3G34GM	Y34
74LVC3G34GN	YA
74LVC3G34GS	YA

^[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

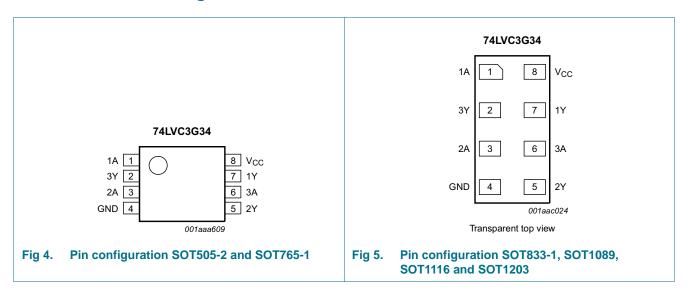
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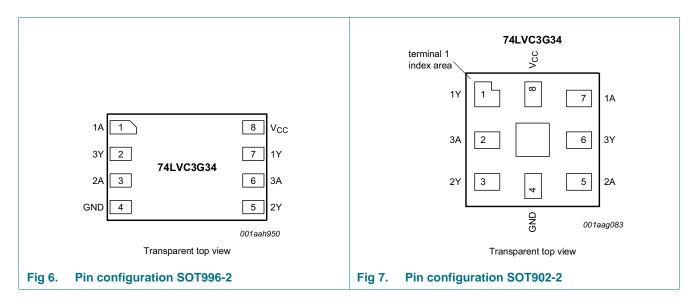
5. Functional diagram



6. Pinning information

6.1 Pinning





6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description	
	SOT505-2, SOT765-1, SOT833-1, SOT1089, SOT996-2, SOT1116 and SOT1203	SOT902-2	
1A, 2A, 3A	1, 3, 6	7, 5, 2	data input
1Y, 2Y, 3Y	7, 5, 2	1, 3, 6	data output
GND	4	4	ground (0 V)
V _{CC}	8	8	supply voltage

7. Functional description

Table 4. Function table[1]

Input nA	Output nY
L	L
Н	Н

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
VI	input voltage	[1]	-0.5	+6.5	V
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0 \text{ V}$	-	±50	mA
Vo	output voltage	Active mode [1]	-0.5	V _{CC} + 0.5	V
		Power-down mode [1][2]	-0.5	+6.5	V
Io	output current	$V_O = 0 V \text{ to } V_{CC}$	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	-	250	mW
T _{stg}	storage temperature		-65	+150	°C

^[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		1.65	5.5	V
VI	input voltage		0	5.5	V
Vo	output voltage	Active mode	0	V _{CC}	V
		Power-down mode; V _{CC} = 0 V	0	5.5	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	-	10	ns/V

^[2] When $V_{CC} = 0 \text{ V}$ (Power-down mode), the output voltage can be 5.5 V in normal operation.

^[3] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K. For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K. For XSON8, XQFN8 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

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10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T _{amb} = -	40 °C to +85 °C					
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V _{CC} = 4.5 V to 5.5 V	$0.7 \times V_{CC}$	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	$0.3 \times V_{CC}$	V
V _{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100 \mu A$; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	V _{CC} - 0.1	-	-	V
		$I_{O} = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$		-	-	V
		$I_{O} = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.9	-	-	V
		$I_{O} = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2	-	-	V
		$I_{O} = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.3	-	-	V
		$I_{O} = -32 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.8	-	-	V
V _{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100 \mu A$; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.3	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	V
		$I_O = 32 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.55	V
lį	input leakage current	$V_{I} = 5.5 \text{ V or GND}; V_{CC} = 0 \text{ V to } 5.5 \text{ V}$	-	±0.1	±1	μΑ
I _{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} = 5.5 \text{ V}$	-	±0.1	±2	μΑ
I _{CC}	supply current	$V_I = 5.5 \text{ V or GND};$ $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}; I_O = 0 \text{ A}$	-	0.1	4	μΑ
Δl _{CC}	additional supply current	per pin; $V_{CC} = 2.3 \text{ V to } 5.5 \text{ V};$ $V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}$	-	5	500	μΑ
Cı	input capacitance	$V_{CC} = 3.3 \text{ V}$; $V_I = \text{GND to } V_{CC}$	-	2.5	-	pF

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 Table 7.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T _{amb} = -	40 °C to +125 °C					
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V _{CC} = 4.5 V to 5.5 V	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	$0.3 \times V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100 \mu A$; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	V _{CC} – 0.1	-	-	V
		$I_O = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	0.95	-	-	V
		$I_{O} = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.7	-	-	V
		$I_{O} = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	1.9	-	-	V
		$I_O = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.0	-	-	V
		$I_{O} = -32 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.4	-	-	V
V _{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100 \mu A; V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.7	V
		$I_O = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.45	V
		$I_O = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	-	0.6	V
		$I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.8	V
		$I_O = 32 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.8	V
I _I	input leakage current	$V_{I} = 5.5 \text{ V or GND}; V_{CC} = 0 \text{ V to } 5.5 \text{ V}$	-	-	±1	μΑ
I _{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} = 5.5 \text{ V}$	-	-	±2	μΑ
I _{CC}	supply current	$V_I = 5.5 \text{ V or GND};$ $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}; I_O = 0 \text{ A}$	-	-	4	μΑ
Δl _{CC}	additional supply current	per pin; $V_{CC} = 2.3 \text{ V to } 5.5 \text{ V};$ $V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}$	-	-	500	μΑ

^[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 $^{\circ}C.$

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11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9.

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to	+125 °C	Unit	
			Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	nA to nY; see Figure 8						
		V _{CC} = 1.65 V to 1.95 V	1.0	3.8	8.6	1.0	10.8	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.4	4.4	0.5	5.5	ns
		V _{CC} = 2.7 V	0.5	2.5	5.0	0.5	6.3	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	2.2	4.1	0.5	5.1	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	1.9	3.2	0.5	4.0	ns
C _{PD}	power dissipation capacitance	$V_I = GND \text{ to } V_{CC}; V_{CC} = 3.3 \text{ V}$	-	14	-	-	-	pF

- [1] Typical values are measured at $T_{amb} = 25$ °C and $V_{CC} = 1.8$ V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}{}^2 \times f_o) \text{ where:}$$

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

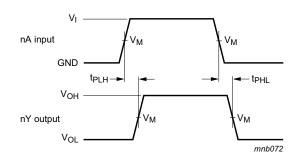
C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V;

N = number of inputs switching;

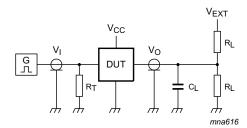
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. AC waveforms



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.



Test data is given in Table 10.

Definitions for test circuit:

 R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to the output impedance Z_0 of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Fig 8. The data input (nA) to output (nY) propagation delays

Fig 9. Test circuit for measuring switching times

Table 9. Measurement points

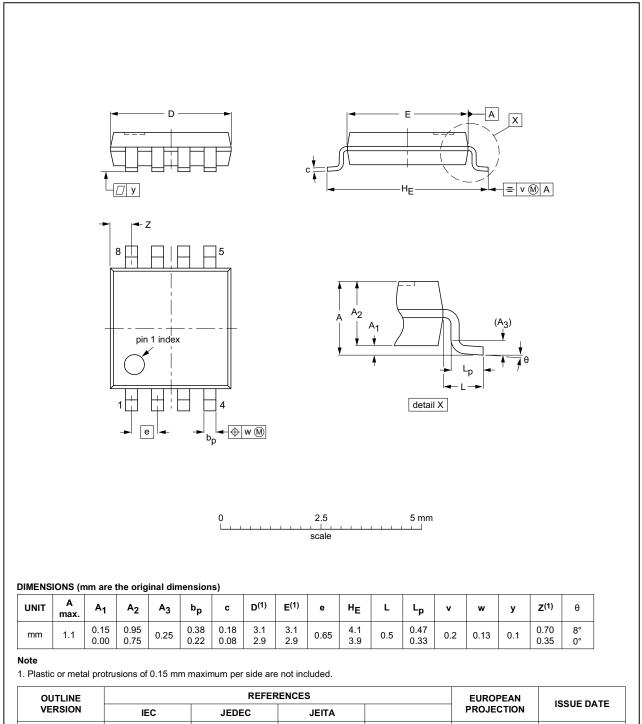
Supply voltage	Input	Output
V _{CC}	V _M	V _M
1.65 V to 1.95 V	0.5 × V _{CC}	0.5 × V _{CC}
2.3 V to 2.7 V	0.5 × V _{CC}	0.5 × V _{CC}
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	0.5 × V _{CC}	0.5 × V _{CC}

Table 10. Test data

Supply voltage	Input		Load	V _{EXT}	
V _{CC}	V _I	$t_r = t_f$	CL	R _L	t _{PLH} , t _{PHL}
1.65 V to 1.95 V	V _{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	open

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	1330E DATE
SOT505-2						02-01-16

Fig 10. Package outline SOT505-2 (TSSOP8)

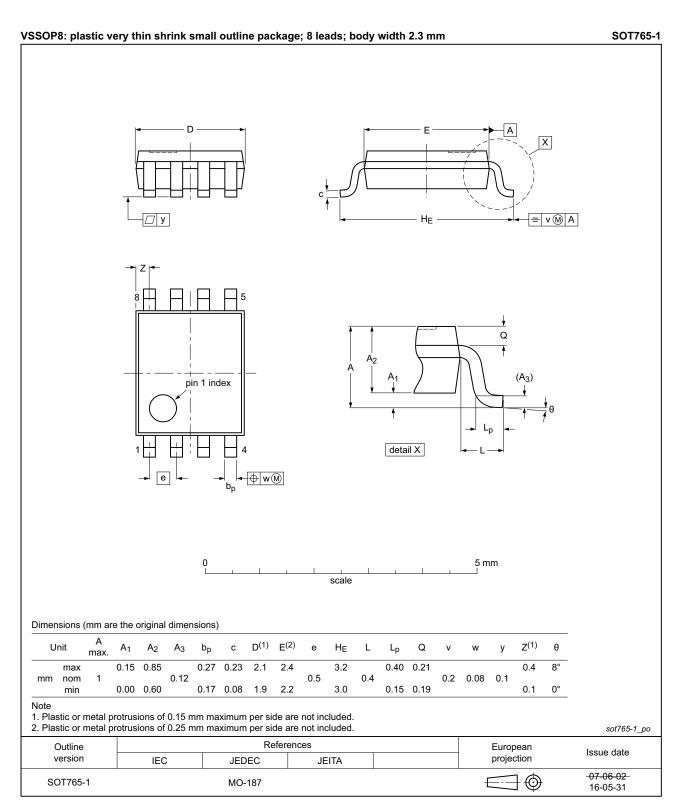


Fig 11. Package outline SOT765-1 (VSSOP8)

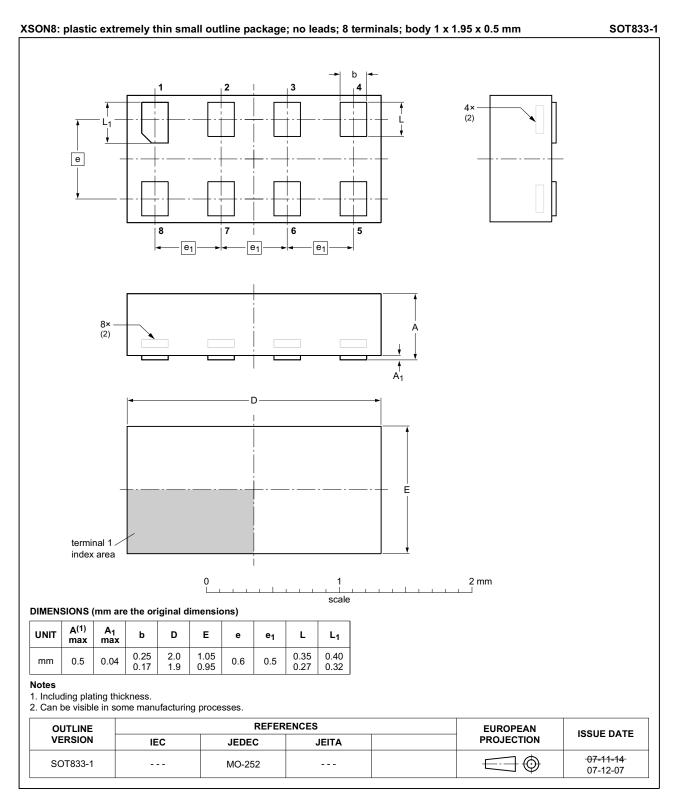


Fig 12. Package outline SOT833-1 (XSON8)

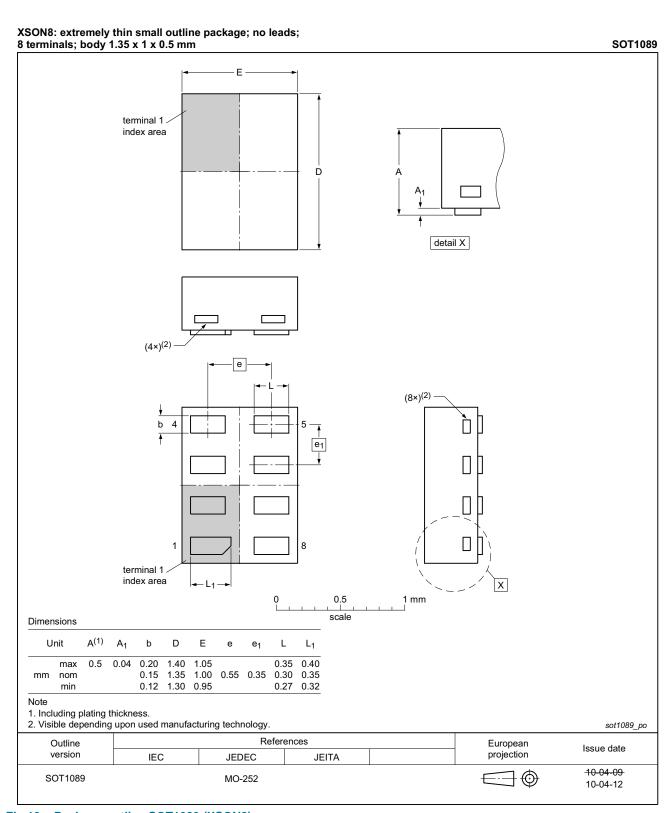


Fig 13. Package outline SOT1089 (XSON8)

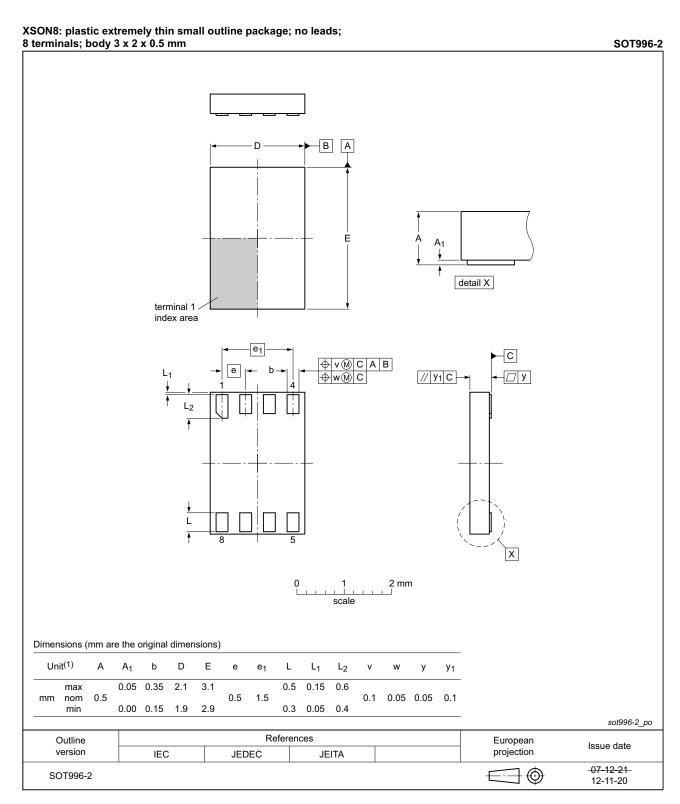


Fig 14. Package outline SOT996-2 (XSON8)

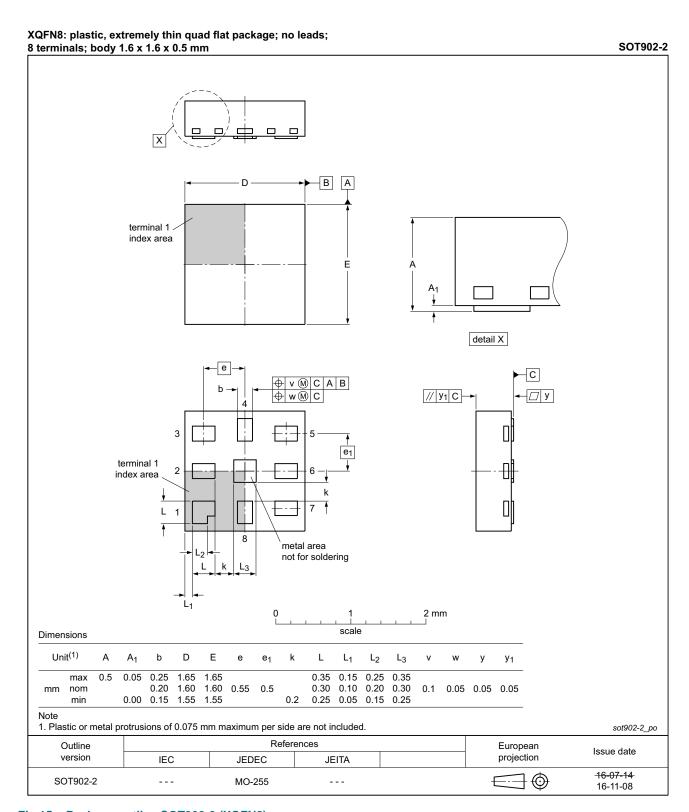


Fig 15. Package outline SOT902-2 (XQFN8)

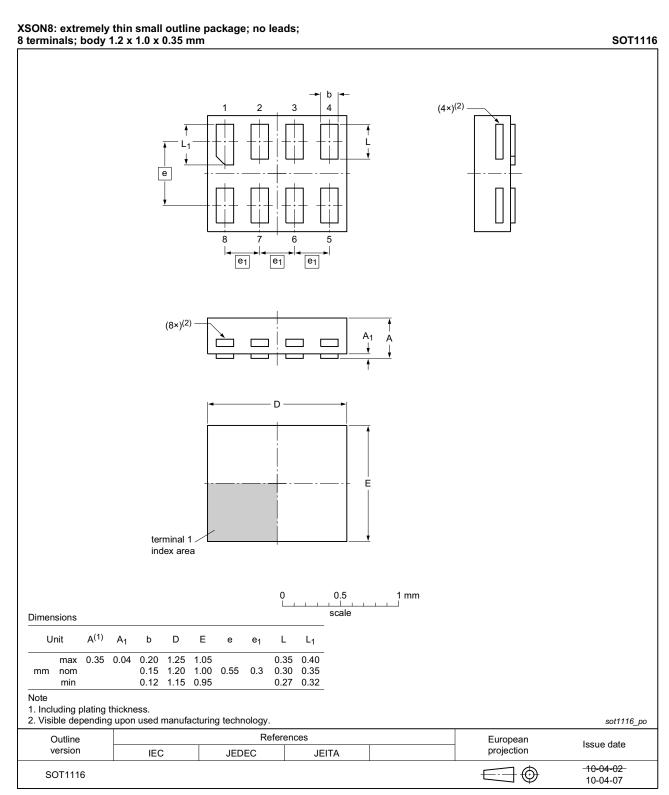


Fig 16. Package outline SOT1116 (XSON8)

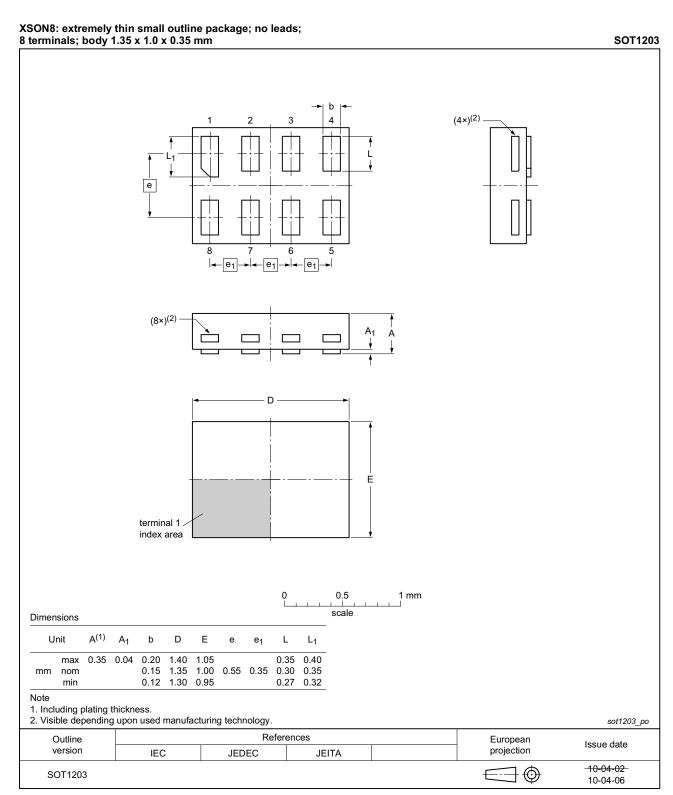


Fig 17. Package outline SOT1203 (XSON8)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74LVC3G34 v.12	20161215	Product data sheet	-	74LVC3G34 v.11	
Modifications:	• <u>Table 7</u> : The	maximum limits for leakage	current and supply cu	irrent have changed.	
74LVC3G34 v.11	20130402	Product data sheet	-	74LVC3G34 v.10	
Modifications:	For type nur	mber 74LVC3G34GD XSON8	U has changed to XS	ON8.	
74LVC3G34 v.10	20120808	Product data sheet	-	74LVC3G34 v.9	
Modifications:	For type number 74LVC3G34GM the SOT code has changed to SOT902-2.				
74LVC3G34 v.9	20111123	Product data sheet	-	74LVC3G34 v.8	
Modifications:	Legal pages	updated.			
74LVC3G34 v.8	20100902	Product data sheet	-	74LVC3G34 v.7	
74LVC3G34 v.7	20080509	Product data sheet	-	74LVC3G34 v.6	
74LVC3G34 v.6	20080312	Product data sheet	-	74LVC3G34 v.5	
74LVC3G34 v.5	20071005	Product data sheet	-	74LVC3G34 v.4	
74LVC3G34 v.4	20070302	Product data sheet	-	74LVC3G34 v.3	
74LVC3G34 v.3	20050131	Product data sheet	-	74LVC3G34 v.2	
74LVC3G34 v.2	20041027	Product data sheet	-	74LVC3G34 v.1	
74LVC3G34 v.1	20040429	Product data sheet	-	-	

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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