MC14034B

8-Bit Universal Bus Register

The MC14034B is a bidirectional 8–bit static parallel/serial, input/output bus register. The device contains two sets of input/output lines which allows the bidirectional transfer of data between two buses; the conversion of serial data to parallel form, or the conversion of parallel data to serial form. Additionally the serial data input allows data to be entered shift/right, while shift/left can be accomplished by hard–wiring each parallel output to the previous parallel bit input.

Other useful applications for this device include pseudo–random code generation, sample and hold register, frequency and phase–comparator, address or buffer register, and serial/parallel input/output conversions.

- Bidirectional Parallel Data Input
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range.
- Pin–for–Pin Replacement for CD4034B.

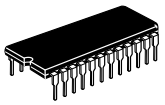
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

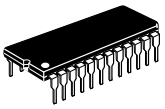
* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic “L” Packages: – 12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



L SUFFIX
CERAMIC
CASE 623



P SUFFIX
PLASTIC
CASE 709

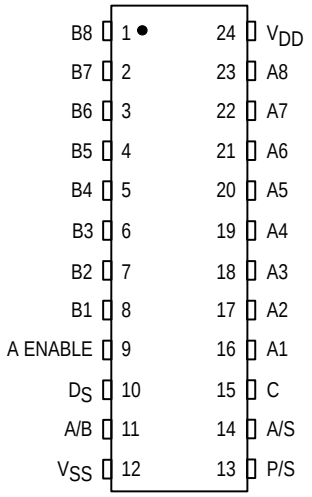
DW SUFFIX
SOIC
CASE 751E

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBDW	SOIC

T_A = – 55° to 125°C for all packages.

PIN ASSIGNMENT



REV 3
1/94

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
“1” Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage “0” Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
“1” Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	– 1.2 – 0.25 – 0.62 – 1.8	— — — —	– 1.0 – 0.2 – 0.5 – 1.5	– 1.7 – 0.36 – 0.9 – 3.5	— — — —	– 0.7 – 0.14 – 0.35 – 1.1	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.010 0.020 0.030	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (2.2 µA/kHz) f + I_{DD} I_T = (4.4 µA/kHz) f + I_{DD} I_T = (6.6 µA/kHz) f + I_{DD}							µAdc
3–State Output Leakage Current	I_{TL}	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	µAdc

#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time A or B	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	—	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	—	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	—	65	130	
Output Fall Time A or B	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time A (B) Synchronous Parallel Data Input, B (A) Parallel Data Output	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 440 ns		5.0	—	525	1050	
t_{PHL}, t_{PHL} = (0.66 ns/pF) C_L + 172 ns		10	—	205	410	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 120 ns		15	—	145	290	
Propagation Delay Time A (B) Asynchronous Parallel Data Input B (A) Parallel Data Output	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 420 ns		5.0	—	505	1010	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	—	180	360	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 105 ns		15	—	130	260	
Clock Pulse Width	t_{WH}	5.0	340	170	—	ns
		10	140	70	—	
		15	110	55	—	
Clock Pulse Frequency	f_{cl}	5.0	—	2.5	1.2	MHz
		10	—	6.0	3.0	
		15	—	8.0	4.0	
Clock Pulse Rise	t_{TLH}, t_{THL}	5.0	—	—	15	µs
		10	—	—	5	
		15	—	—	4	
A, B Input Setup Time	t_{su}	5.0	100	35	—	ns
		10	45	15	—	
		15	35	12	—	
High Level SE, P/S, A/S Pulse Width	t_{WH}	5.0	600	200	—	ns
		10	270	90	—	
		15	200	80	—	

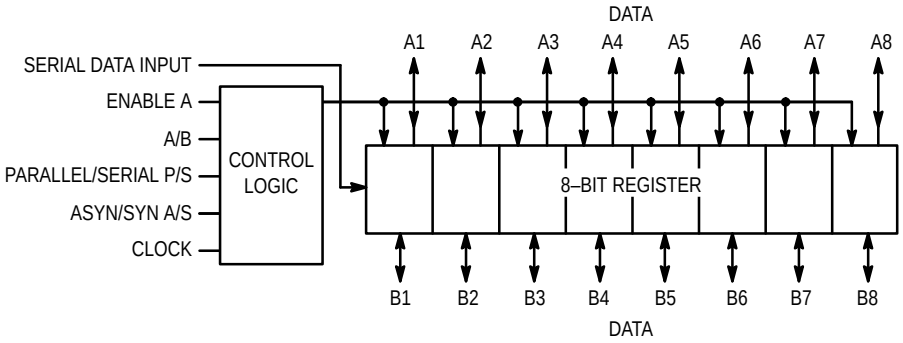
* The formulas given are for the typical characteristics only at 25°C.
#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

TRUTH TABLE

“A” Enable	P/S	A/B	A/S	Mode	Operation†
0	0	0	X	Serial	Synchronous Serial data input, A and B Parallel data outputs disabled.
0	0	1	X	Serial	Synchronous Serial data input, B–Parallel data output.
0	1	0	0	Parallel	B Synchronous Parallel data inputs, A–Parallel data outputs disabled.
0	1	0	1	Parallel	B Asynchronous Parallel data inputs, A–Parallel data outputs disabled.
0	1	1	0	Parallel	A–Parallel data inputs disabled, B–Parallel data outputs.
0	1	1	1	Parallel	A–Parallel data inputs disabled, B–Parallel data outputs.
1	0	0	X	Serial	Synchronous serial data input, A–Parallel data output.
1	0	1	X	Serial	Synchronous serial data input, B–Parallel data output.
1	1	0	0	Parallel	B–Synchronous Parallel data input, A–Parallel data output.
1	1	0	1	Parallel	B–Asynchronous Parallel data input, A–Parallel data output.
1	1	1	0	Parallel	A–Synchronous Parallel data input, B–Parallel data output.
1	1	1	1	Parallel	A–Asynchronous Parallel data input, B–Parallel data output.

X = Don’t Care
†Outputs change at positive transition of clock in the serial mode and when the A/S input is low in the parallel mode. During transfer from parallel to serial operation, A/S should remain low in order to prevent D_S transfer into flip–flops.

EXPANDED BLOCK DIAGRAM



OPERATING CHARACTERISTICS

The MC14034B is composed of eight register cells connected in cascade with additional control logic. Each register cell is composed of one “D” master–slave flip–flop with separate internal clocks, and two data transfer gates allowing the data to be transferred bi–directionally from bus A to bus B and from bus B to bus A, and to be memorized. Besides the single phase clock and the serial data inputs, the control logic provides four other features:

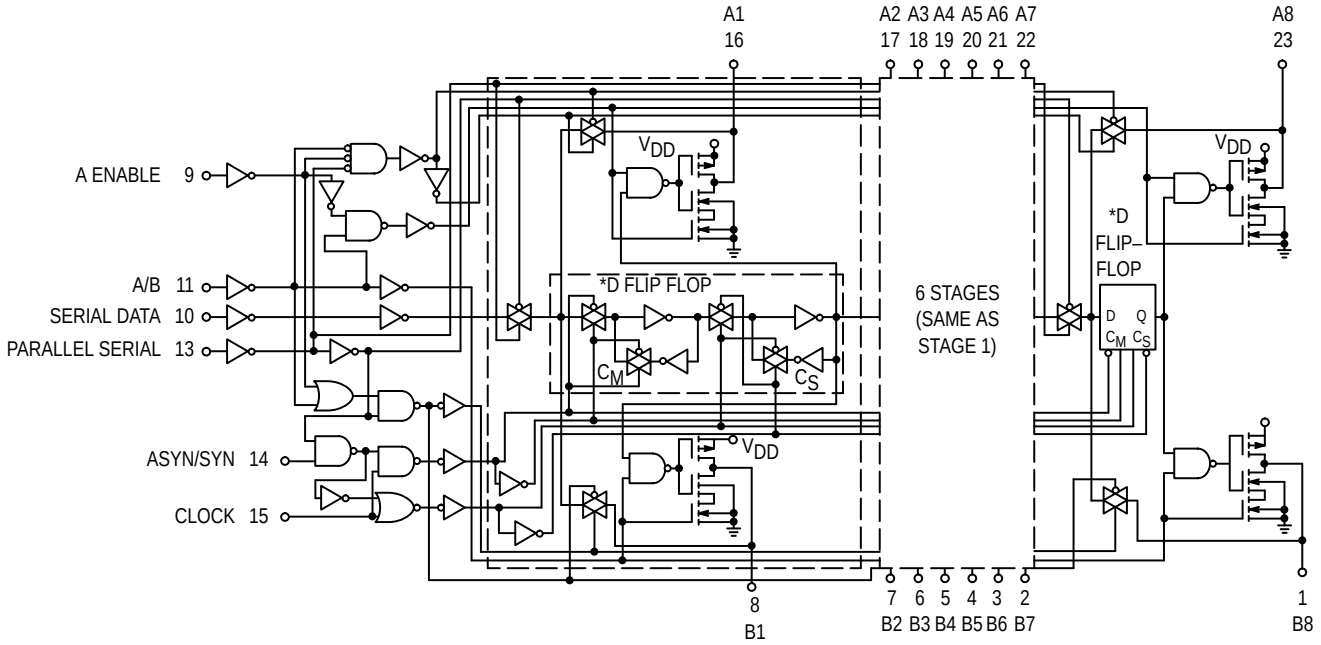
A Enable Input — When high, this input enables the bus A data lines.

A/B Input (Data A or B) — This input controls the direction of data flow: when high, the data flows from bus A to bus B; when low, the data flows from bus B to bus A.

P/S Input (Parallel/Serial) — This input controls the data input mode (parallel or serial). When high, the data is transferred to the register in a parallel asynchronous mode or a parallel synchronous mode (positive clock transition). When low, the data is entered into the register in a serial synchronous mode (positive clock transition).

A/S Input (Asynchronous/Synchronous to the Clock) — When this input is high, the data is transferred independently from the clock rate; when low, the clock is enabled and the data is transferred synchronously.

LOGIC DIAGRAM



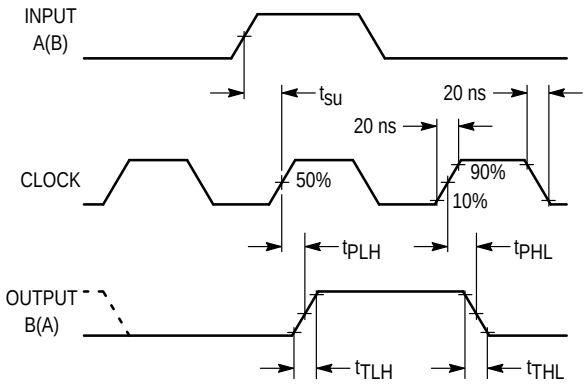


Figure 1. Propagation Delay and Transition Times Waveforms

PROPAGATION AND TRANSITION TIME TEST CIRCUITS

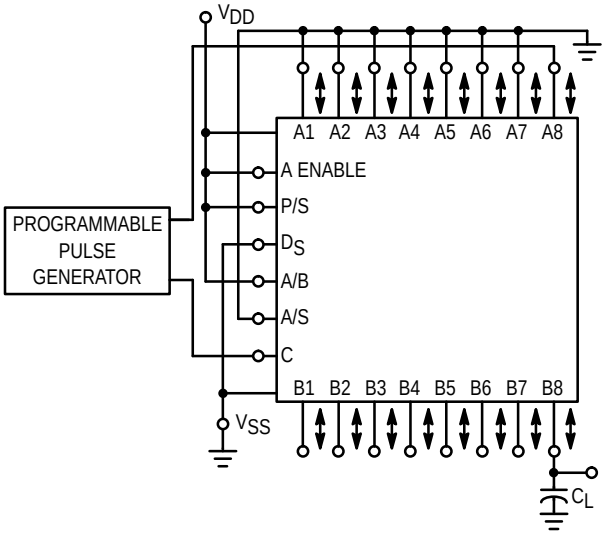


Figure 2. A Synchronous Data Input, B Parallel Data Output and Setup Time

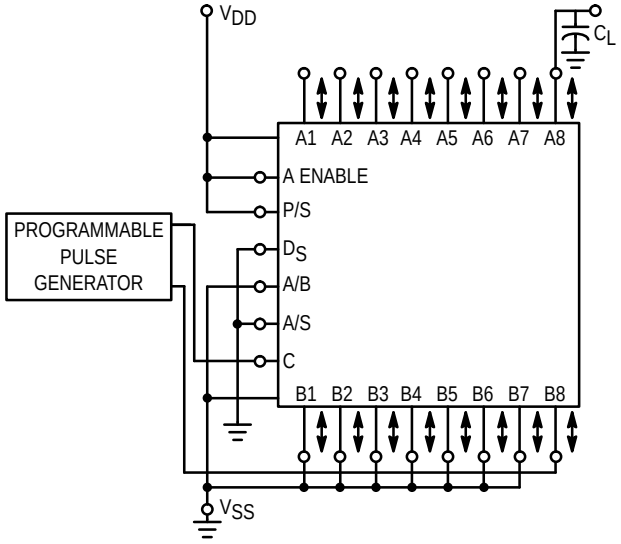


Figure 3. B Synchronous Data Input, A Parallel Data Output and Setup Time

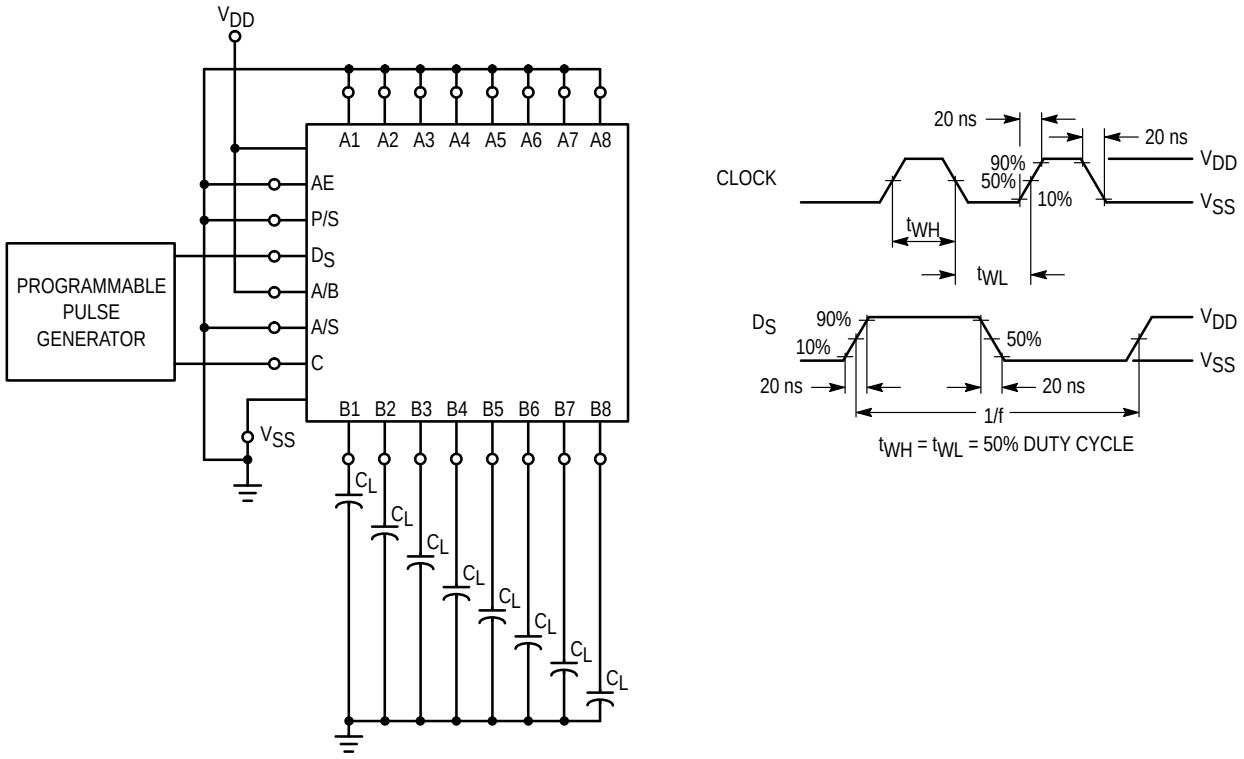


Figure 4. Power Dissipation Test Circuit and Waveforms

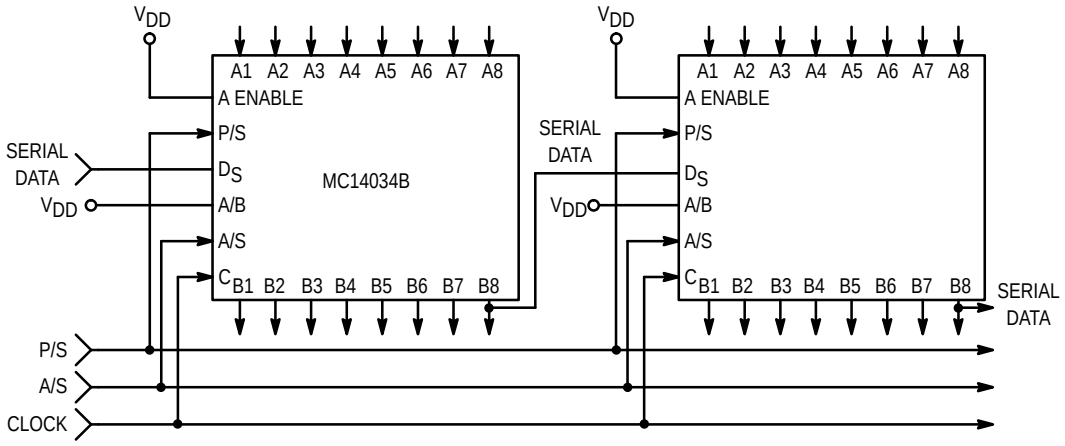
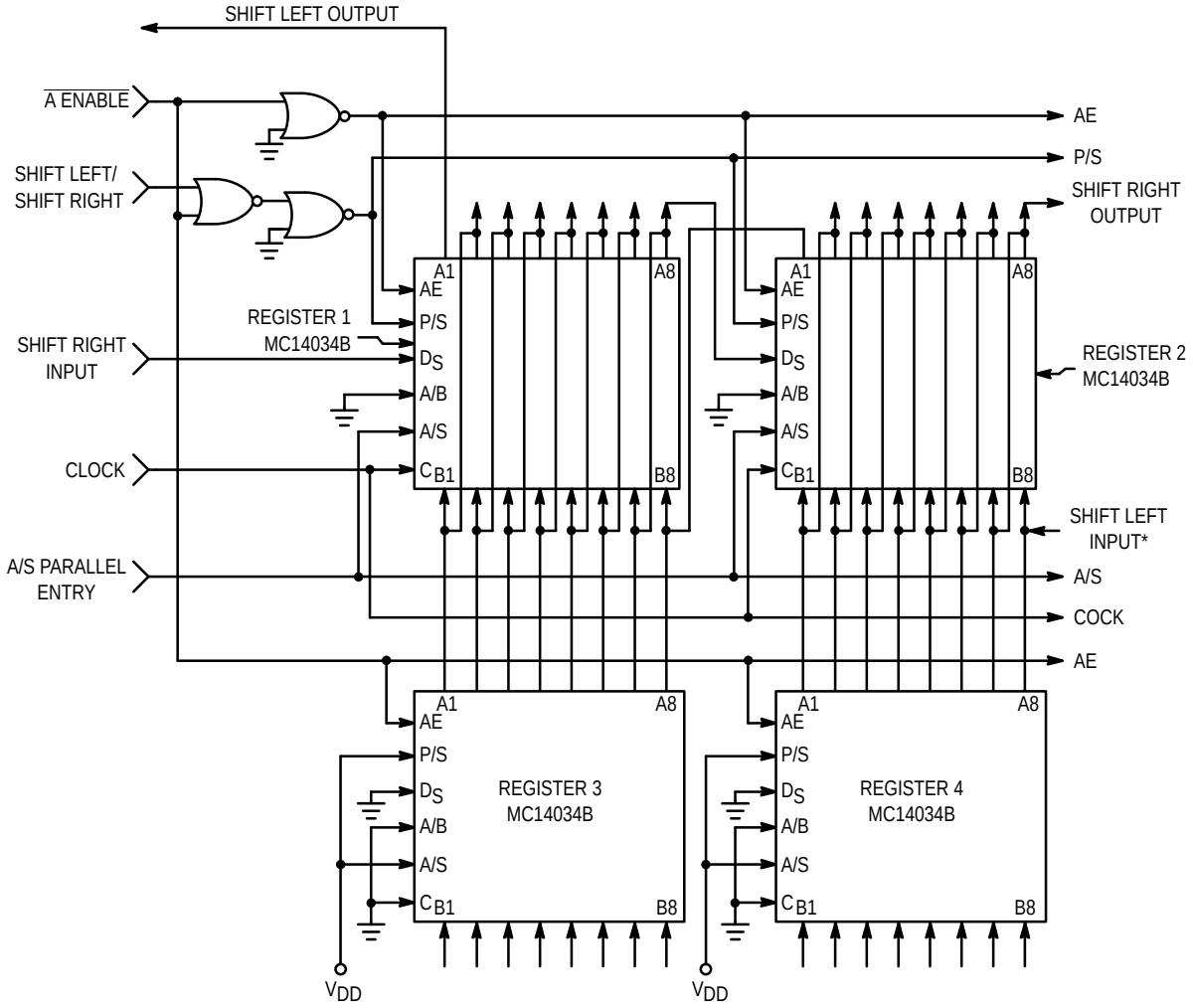


Figure 5. 16–Bit Parallel In/Parallel Out, Parallel In/Serial Out, Serial In/Parallel Out, Serial In/Serial Out Register



A “High” (“Low”) on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the lock signal. A “high” on the “A” Enable Input disables the “A” parallel data lines on Reg. 1 and 2 and enables the “A” data lines on registers 3 and 4 and allows parallel data into registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

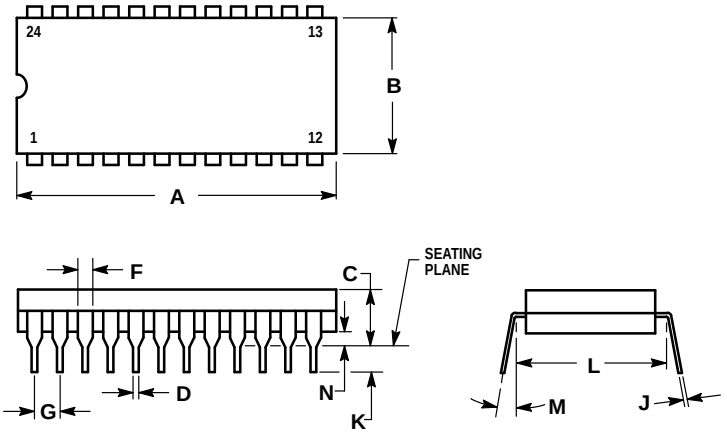
When parallel inputs are not used, Reg. 3 and 4 and associated logic are not required.

*Shift left input must be disabled during parallel entry.

Figure 6. Shift Right/Shift Left with Parallel Inputs

OUTLINE DIMENSIONS

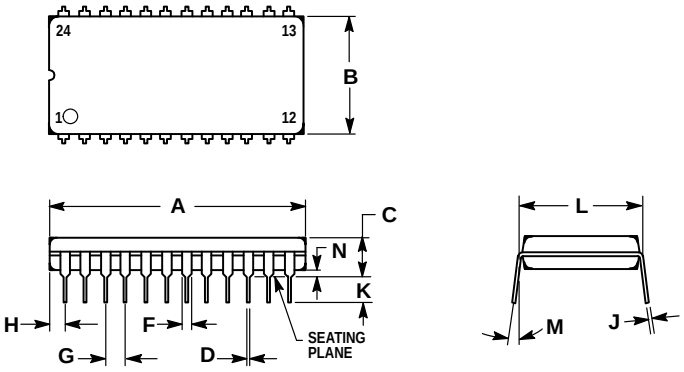
L SUFFIX
CERAMIC DIP PACKAGE
CASE 623–05
ISSUE M



NOTES:
1. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (WHEN FORMED PARALLEL).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0 °	15 °	0 °	15 °
N	0.51	1.27	0.020	0.050

P SUFFIX
PLASTIC DIP PACKAGE
CASE 709–02
ISSUE C

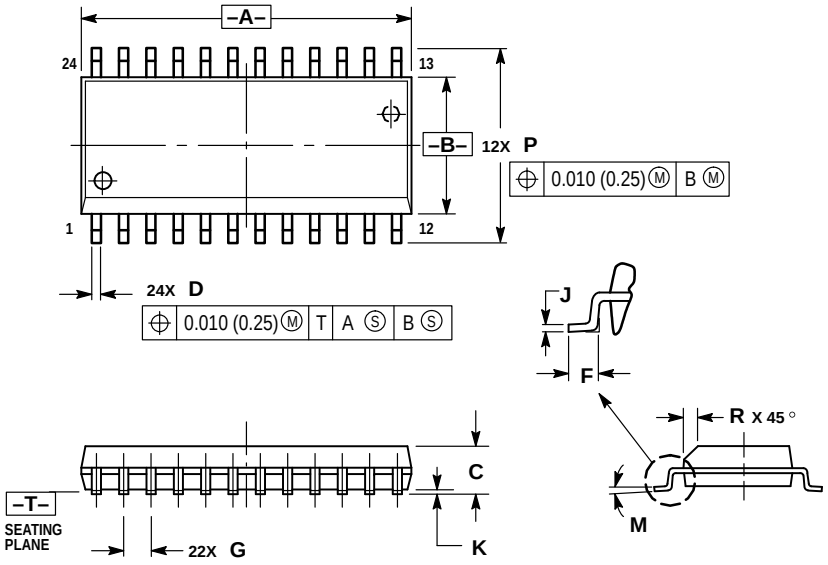


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0 °	15 °	0 °	15 °
N	0.51	1.02	0.020	0.040

OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751E–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0 °	8 °	0 °	8 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

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