CD4034BMS

CMOS 8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register

December 1992

Features

- **High Voltage Types (20V Rating)**
- **Bidirectional Parallel Data Input**
- **Parallel or Serial Inputs/Parallel Outputs**
- **Asynchronous or Synchronous Parallel Data Loading**
- **Parallel Data-Input Enable on "A" Data Lines (3-State Output)**
- **Data Recirculation for Register Expansion**
- **Multipackage Register Expansion**
- **Fully Static Operation DC-to-10MHz (typ.) at VDD = 10V**
- **Standardized Symmetrical Output Characteristics**
- **100% Tested for Quiescent Current at 20V**
- **5V, 10V and 15V Parametric Ratings**
- **Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range;**
  - **100nA at 18V and +25°C**
- **Noise Margin (Over Full Package Temperature Range):**
  - **1V at VDD = 5V**
  - **2V at VDD = 10V**
  - **2.5V at VDD = 15V**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications

- **Parallel Input/Parallel Output, Serial Input/Parallel Output, Serial Input/Serial Output Register**
- **Shift Right/Shift Left Register**
- **Shift Right/Shift Left With Parallel Loading**
- **Address Register**
- **Buffer Register**
- **Bus System Register with Enable Parallel Lines at Bus Side**
- **Double Bus Register System**
- **Up-Down Johnson or Ring Counter**
- **Pseudo-Random Code Generators**
- **Sample and Hold Register (Storage, Counting, Display)**
- **Frequency and Phase Comparator**

Description

CD4034BMS is a static eight-stage parallel-or serial-input parallel-output register. It can be used to:

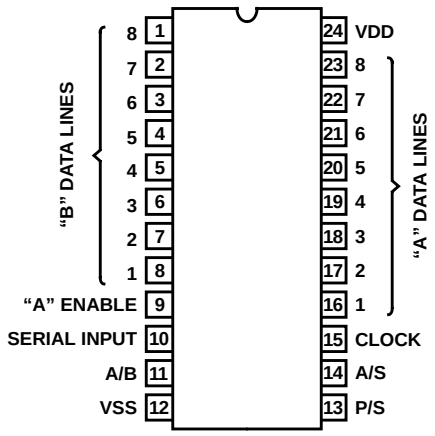
1) bidirectionally transfer parallel information between two buses, 2) convert serial data to parallel form and direct the parallel data to either of two buses, 3) store (recirculate) parallel data, or 4) accept parallel data from either of two buses and convert that data to serial form. Inputs that control the operations include a single-phase CLOCK (CL), A DATA ENABLE (AE), ASYNCHRONOUS/SYNCHRONOUS (A/S), A-BUS-TO-B-BUS/B-BUS-TO-A-BUS (A/B), and PARALLEL/SERIAL (P/S).

Data inputs include 16 bidirectional parallel data lines of which the eight A data lines are inputs (3-state outputs) and the B data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for SERIAL DATA is also provided.

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

Pinout

CD4034BMS
TOP VIEW



Parallel Operation

A high P/S input signal allows data transfer into the register via the parallel data lines synchronously with the positive transition of the clock provided the A/S input is low. If the A/S input is high the transfer is independent of the clock. The direction of data flow is controlled by the A/B input. When this signal is high the A data lines are inputs (and B data lines are outputs); a low A/B signal reverses the direction of data flow.

The AE input is an additional feature which allows many registers to feed data to a common bus. The A DATA lines are enabled only when this signal is high.

Data storage through recirculation of data in each register stage is accomplished by making the A/B signal high and the AE signal low.

Serial Operation

A low P/S signal allows serial data to transfer into the register synchronously with the positive transition of the clock. The A/S input is internally disabled when the register is in the serial mode (asynchronous serial operation is not allowed).

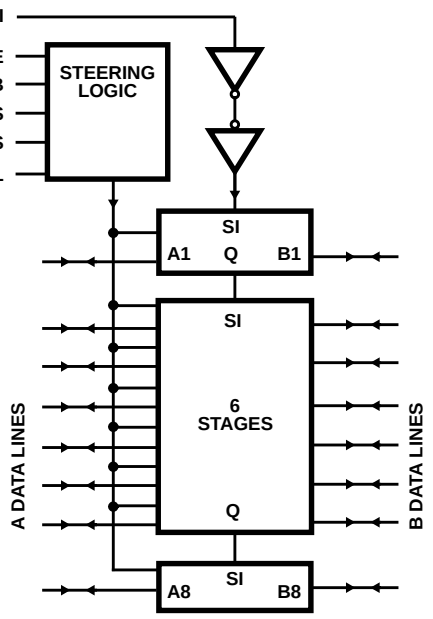
The serial data appears as output data on either the B lines (when A/B is high) or the A lines (when A/B is low and the AE signal is high).

Register expansion can be accomplished by simply cascading CD4034BMS packages.

The CD4034BMS is supplied in these 24 lead outline packages:

Braze Seal DIP	H4V
Ceramic Flatpack	H4P

Functional Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Operating Temperature Range . . . . . -55^oC to $+125^oC$
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . . -65^oC to $+150^oC$
Lead Temperature (During Soldering) . . . . . $+265^oC$
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	$80^oC/W$	$20^oC/W$
Flatpack Package	$70^oC/W$	$20^oC/W$

Maximum Package Power Dissipation (PD) at $+125^oC$
For TA = -55^oC to $+100^oC$ (Package Type D, F, K) 500mW
For TA = $+100^oC$ to $+125^oC$ (Package Type D, F, K) . . . . . Derate Linearity at $12mW/^oC$ to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . $+175^oC$

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	$+25^oC$	-	10	µA
				2	$+125^oC$	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55^oC	-	10	µA
Input Leakage Current Except A and B Lines	IIL	VIN = VDD or GND	VDD = 20	1	$+25^oC$	-100	-	nA
				2	$+125^oC$	-1000	-	nA
			VDD = 18V	3	-55^oC	-100	-	nA
Input Leakage Current Except A and B Lines	IIH	VIN = VDD or GND	VDD = 20	1	$+25^oC$	-	100	nA
				2	$+125^oC$	-	1000	nA
			VDD = 18V	3	-55^oC	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	$+25^oC$	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	$+25^oC$	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	$+25^oC$	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	$+25^oC$	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	$+25^oC$	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	$+25^oC$	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	$+25^oC$	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	$+25^oC$	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	$+25^oC$	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	$+25^oC$	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	$+25^oC$			
		VDD = 18V, VIN = VDD or GND		8A	$+125^oC$			
		VDD = 3V, VIN = VDD or GND		8B	-55^oC			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	$+25^oC$	-0.4	-	µA
				2	$+125^oC$	-12	-	µA
			VDD = 18V	3	-55^oC	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	$+25^oC$	-	0.4	µA
				2	$+125^oC$	-	12	µA
			VDD = 18V	3	-55^oC	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Parallel In to Parallel Out	TPHL TPLH	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	700	ns
			10, 11	+125°C, -55°C	-	945	ns
Propagation Delay 3 State AE to Out 'A'	TPLZ TPHZ	VDD = 5V, VIN = VDD or GND (Notes 2, 3)	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay 3-State AE to Out 'A'	TPZL TPZH	VDD = 5V, VIN = VDD or GND (Notes 2, 3)	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND (Note 2)	9	+25°C	2	-	MHz
			10, 11	+125°C, -55°C	1.48	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
3. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Parallel In to Parallel Out	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V	1, 2, 3	+25°C	-	170	ns
Propagation Delay Serial to Parallel Out	TPHL TPLH	VDD = 5V	1, 2, 3	+25°C	700	-	ns
		VDD = 10V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V	1, 2, 3	+25°C	-	170	ns
Propagation Delay 3-State AE to Out ‘A’	TPLZ TPHZ	VDD = 10V	1, 2, 3, 4	+25°C	-	160	ns
		VDD = 15V	1, 2, 3, 4	+25°C	-	120	ns
Propagation Delay 3-State AE to Out ‘A’	TPZL TPZH	VDD = 10V	1, 2, 3, 4	+25°C	-	160	ns
		VDD = 15V	1, 2, 3, 4	+25°C	-	120	ns
Transition Time	TTLH TTHL	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	5	-	MHz
		VDD = 15V	1, 2, 3	+25°C	7	-	MHz
Minimum Data Setup Time Serial Data to Clock	TS	VDD = 5V	1, 2, 3	+25°C	-	160	ns
		VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Minimum Data Setup Time Parallel Data to Clock	TS	VDD = 5V	1, 2, 3	+25°C	-	50	ns
		VDD = 10V	1, 2, 3	+25°C	-	30	ns
		VDD = 15V	1, 2, 3	+25°C	-	20	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	250	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
Maximum Clock Rise and Fall Time (Note 5)	TRCL TFCL	VDD = 5V	1, 2, 3	+25°C	-	15	µs
		VDD = 10V	1, 2, 3	+25°C	-	15	µs
		VDD = 15V	1, 2, 3	+25°C	-	15	µs
Minimum High Level Pulse Width AE, P/S, A/S	TW	VDD = 5V	1, 2, 3	+25°C	-	350	ns
		VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.
5. If more than one unit is cascaded, tRCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2, 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

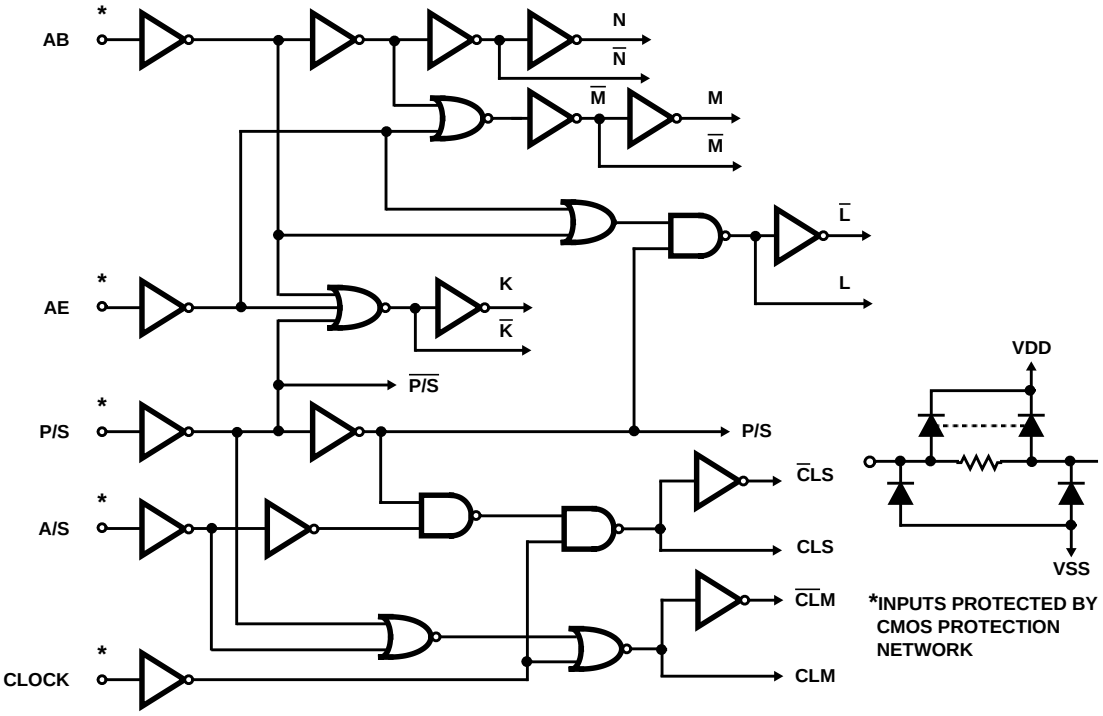
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1 - 8	12, 15 - 23	9 - 11, 13, 14, 24			
Static Burn-In 2 Note 1	1 - 8	12	9 - 11, 13 - 24			
Dynamic Burn-In Note 1	-	1 - 8, 11 - 14	9, 24	16 - 23	15	10
Irradiation Note 2	1 - 8	12	9 - 11, 13 - 24			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram



FLIP-FLOP TRUTH TABLE

INPUTS			OUTPUT
$\overline{CLM}$	$\overline{CLS}$	D	Q
↓	↓	0	0
↑	↓	0	0
↓	↑	0	Invalid Condition
↑	↑	X	0
↓	↓	1	1
↑	↓	1	1
↓	↑	1	Invalid Condition

1 = High Level 0 = Low Level X = Don't Care

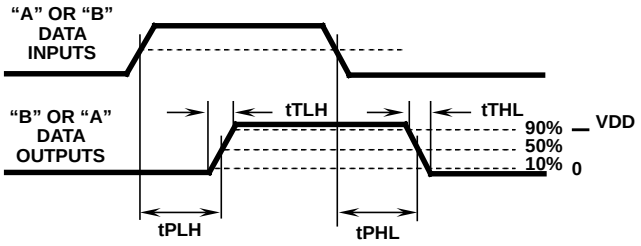
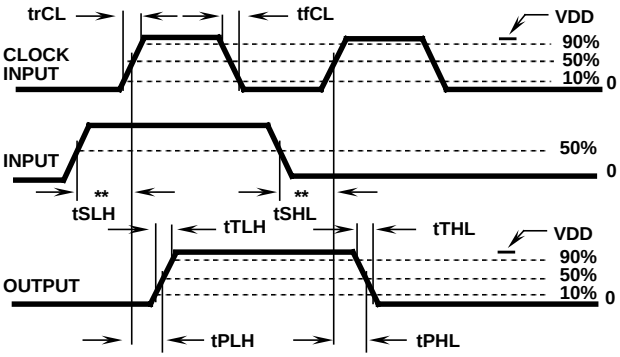


FIGURE 1. ASYNCHRONOUS OPERATION PROPAGATION DELAY TIME AND TRANSITION TIME



*Input refers to any of the "A" or "B" data inputs, "A" ENABLE, SERIAL INPUT, A/B, P/S, or A/S inputs

**tSLH and tSHL are Set-Up times

FIGURE 2. SYNCHRONOUS OPERATION PROPAGATION DELAY TIMES, TRANSITION TIMES, AND SET-UP TIMES

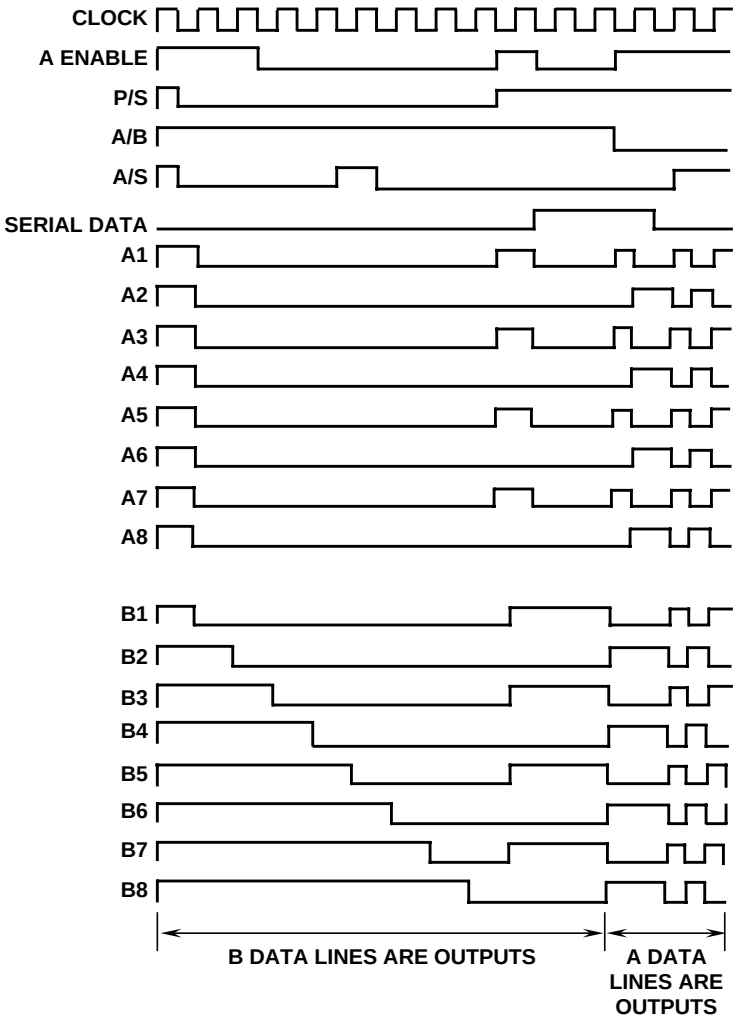


FIGURE 3. TIMING DIAGRAM

Typical Performance Characteristics

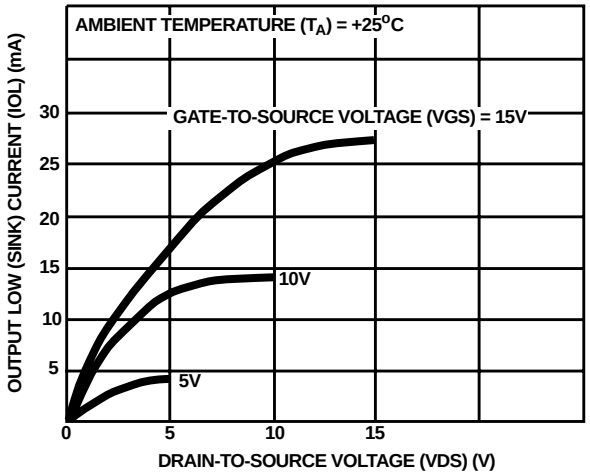


FIGURE 4. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

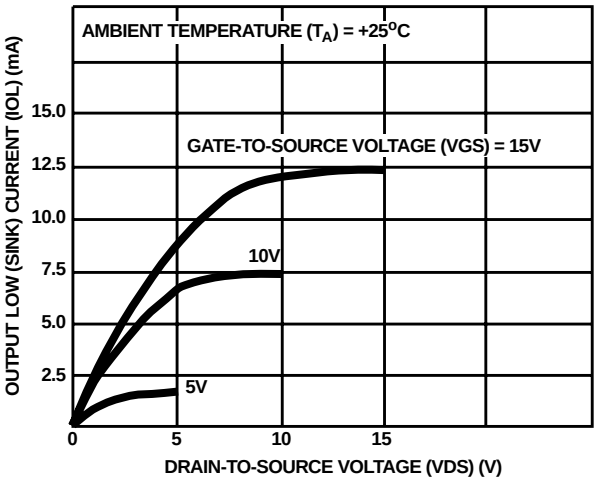


FIGURE 5. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

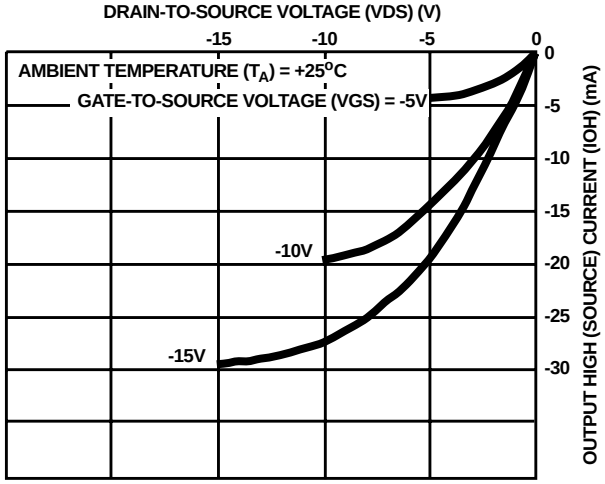


FIGURE 6. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

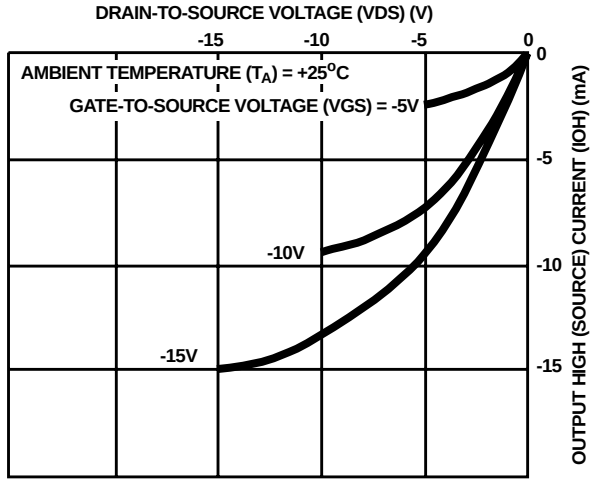


FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

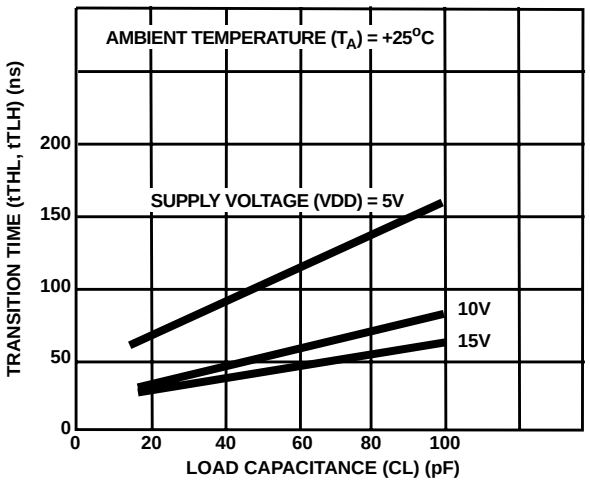


FIGURE 8. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

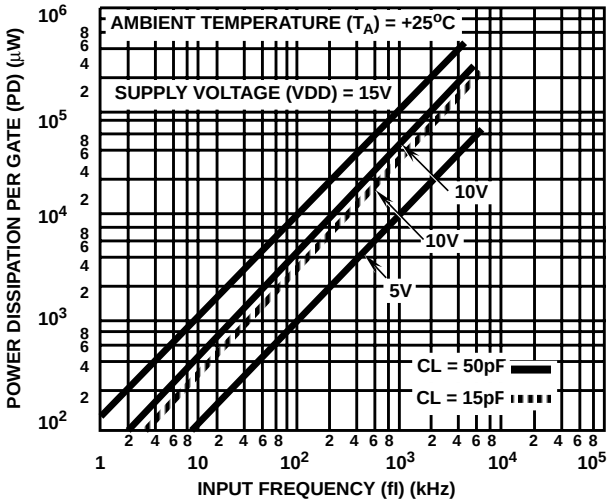


FIGURE 9. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF CLOCK FREQUENCY

Typical Performance Characteristics (Continued)

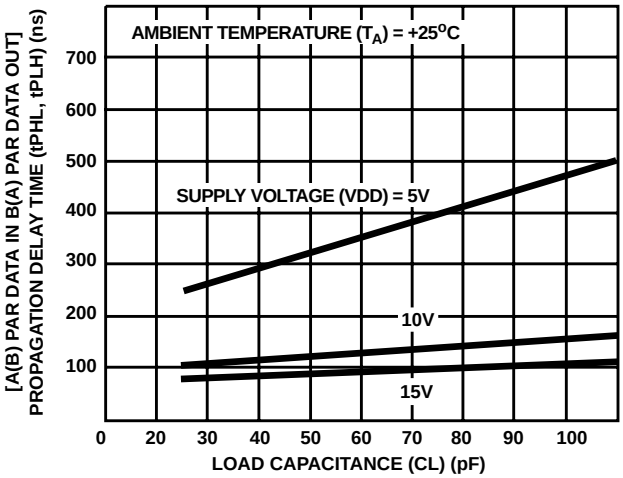


FIGURE 10. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE [A(B) PARALLEL DATA INPUT TO B(A) PARALLEL DATA OUTPUT, SYNCHRONOUS OR ASYNCHRONOUS])

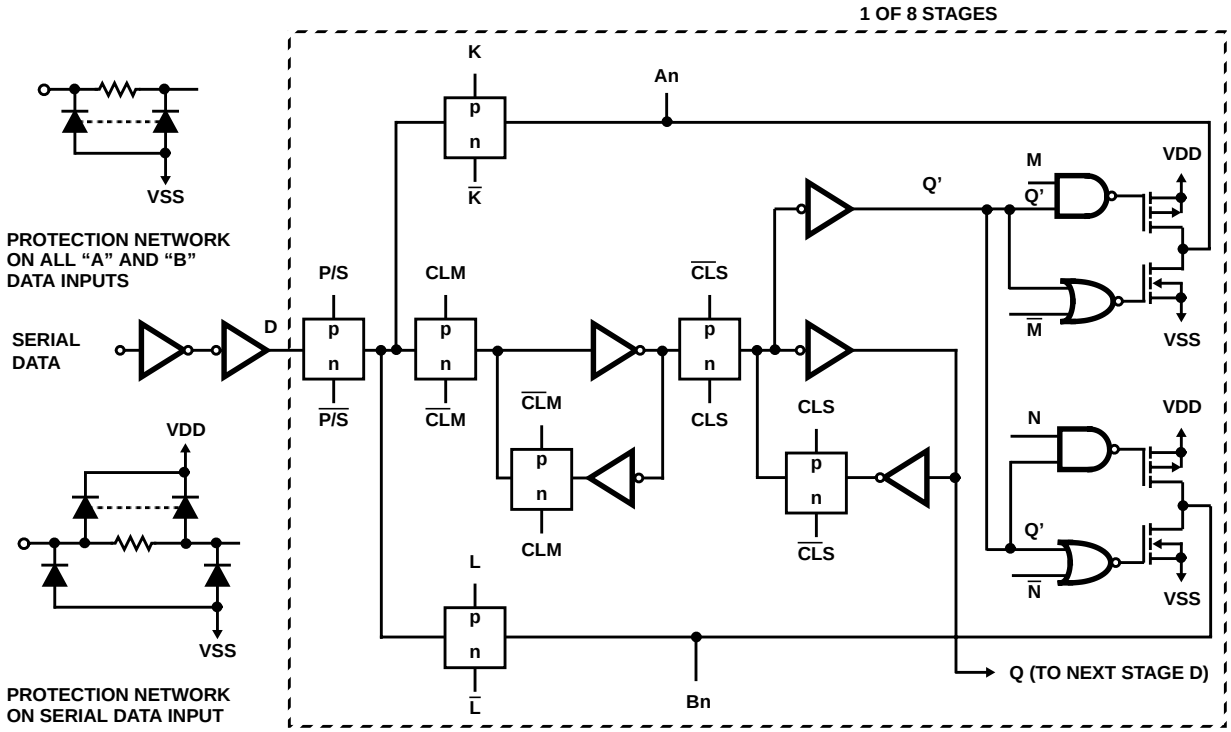


FIGURE 11. REGISTER STAGE LOGIC DIAGRAM (1 OF 8 STAGES)

TRUTH TABLE REGISTER INPUT-LEVELS AND RESULTING REGISTER OPERATION

"A" ENABLE	P/S	A/B	A/S	OPERATION*
0	0	0	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Outputs Disabled
0	0	1	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
0	1	0	0	Parallel Mode; "B" Synch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
0	1	0	1	Parallel Mode; "B" Asynch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
0	1	1	0	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Synch. Data Recirculation
0	1	1	1	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Asynch. Data Recirculation
1	0	0	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Output
1	0	1	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
1	1	0	0	Parallel Mode; "B" Synch. Parallel Data Input, "A" Parallel Data Output
1	1	0	1	Parallel Mode; "B" Asynch. Parallel Data Input, "A" Parallel Data Output
1	1	1	0	Parallel Mode; "A" Synch, Parallel Data Input, "B" Parallel Data Output
1	1	1	1	Parallel Mode; "A" Asynch. Parallel Data Input, "B" Parallel Data Output

*Outputs change at positive transition of clock in the serial mode and when the A/S control input is "low" in the parallel mode. During transfer from parallel to serial operation A/S should remain low in order to prevent DS transfer into Flip Flops.

1 = High Level 0 = Low Level X = Don't Care

Applications

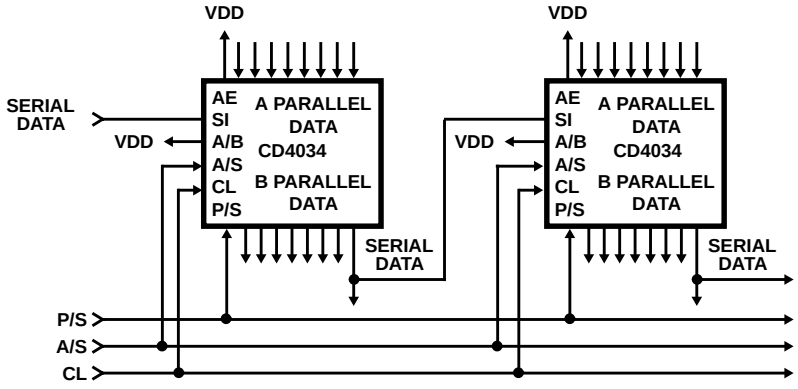


FIGURE 12. 16-BIT PARALLEL IN/PARALLEL OUT, PARALLEL IN/SERIAL OUT, SERIAL IN/PARALLEL OUT SERIAL IN/SERIAL OUT REGISTER

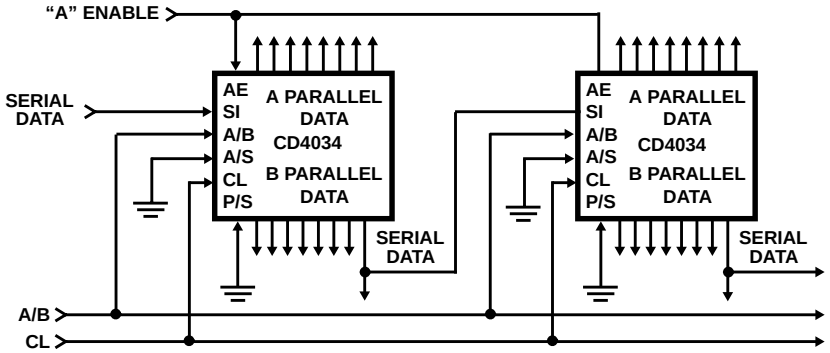
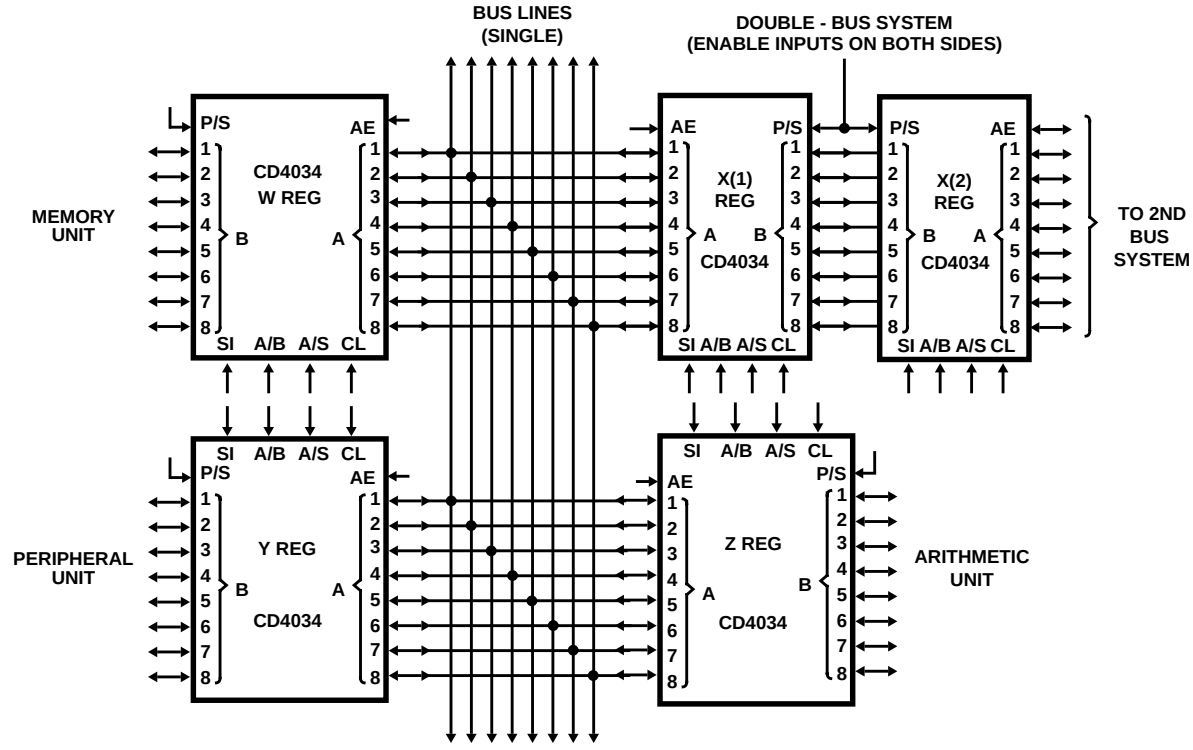


FIGURE 13. 16-BIT SERIAL IN/GATED PARALLEL OUT REGISTER



THE "A" ENABLE (AE) AND A/B SIGNALS CONTROL ALL COMBINATIONS OF TRANSFER BETWEEN THE REGISTERS AND BUS SYSTEMS

FIGURE 14. SINGLE AND DOUBLE-BUS SYSTEMS

Applications (Continued)

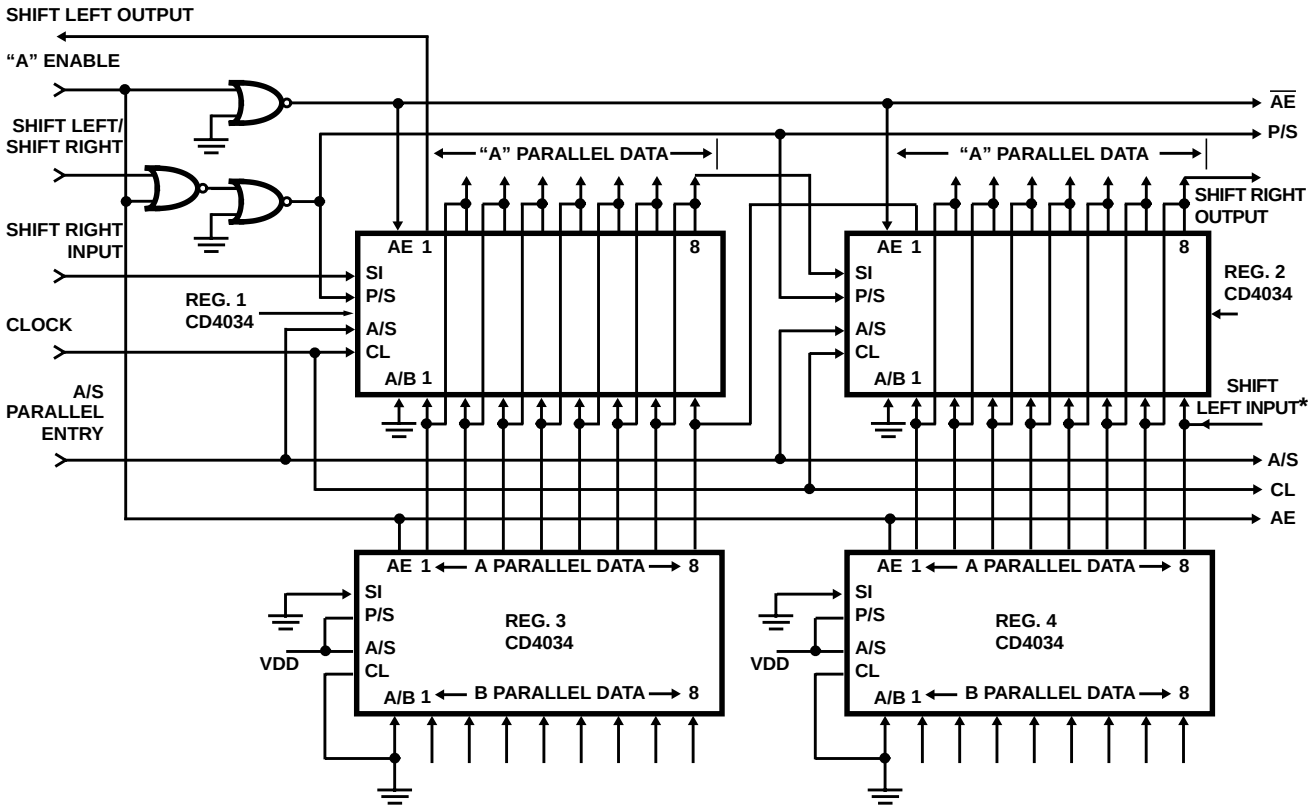


FIGURE 15. SHIFT RIGHT/SHIFT LEFT WITH PARALLEL INPUTS

A "High" ("Low") on the shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines Reg. 1 and 2 and enables the "A" data lines on registers 3 and 4 and allows parallel data into registers 1 and 2.

Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Reg. 3 and 4 and associated logic are not required.

* Shift left input must be disabled during parallel entry.

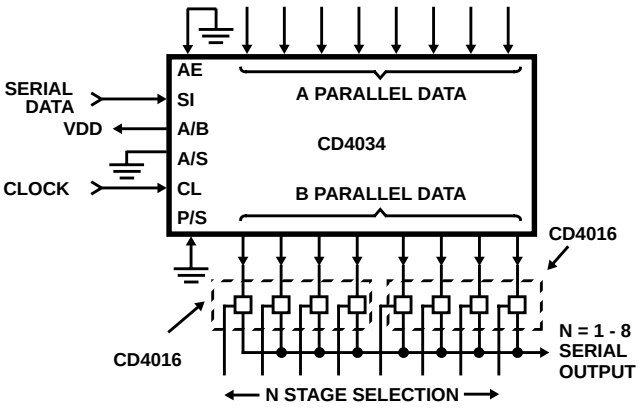


FIGURE 16. N-STAGE SHIFT REGISTER WITH FIXED SERIAL OUTPUT LINE

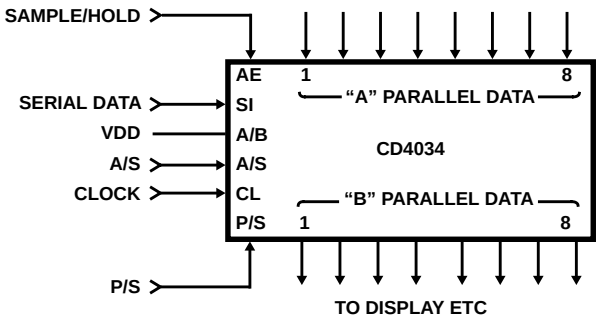
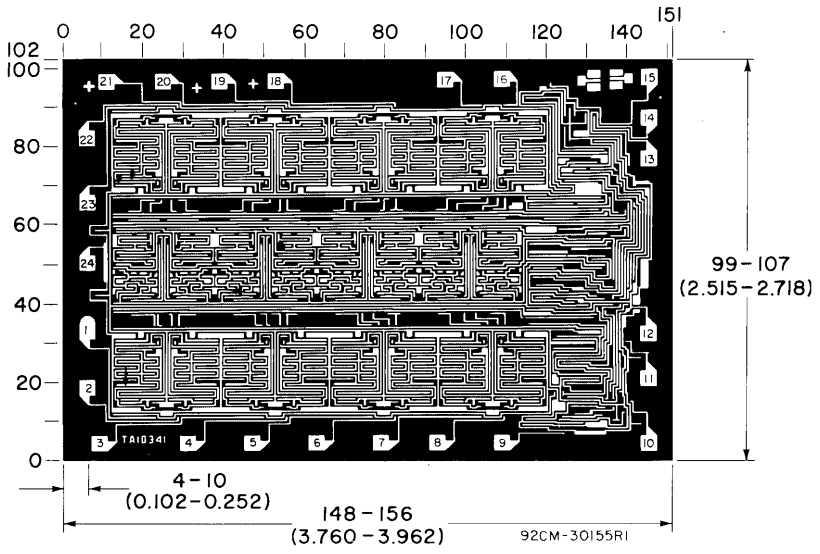


FIGURE 17. SAMPLE AND HOLD REGISTER - SERIAL/PARALLEL IN - PARALLEL OUT

Chip Dimensions and Pad Layout



Dimension in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

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