TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS049C − Revised October 2003

CD4060B Types

CMOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator

High-Voltage Types (20-Volt Rating)

■CD4060B consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all-O's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of ϕ_I (and ϕ_O). All inputs and outputs are fully buffered. Schmitt trigger action on the input-pulse line permits unlimited input-pulse rise and fall times.

The CD4060B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

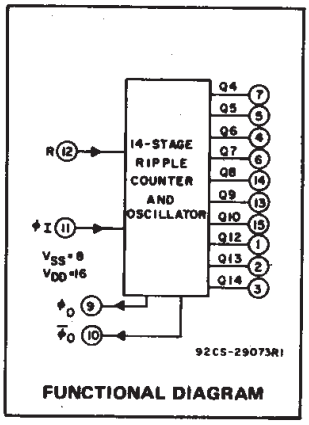
- 12 MHz clock rate at 15 V
- Common reset
- Fully static operation
- Buffered inputs and outputs
- Schmitt trigger input-pulse line
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for description of "B" Series CMOS Devices"

Oscillator Features:

- All active components on chip
- RC or crystal oscillator configuration
- RC oscillator frequency of 690 kHz min. at 15 V

Applications

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits



FUNCTIONAL DIAGRAM

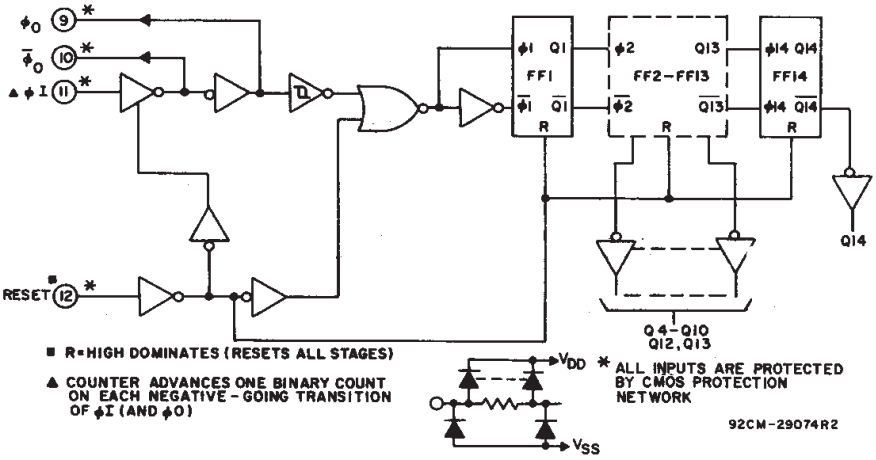


Fig. 1 – Logic diagram.

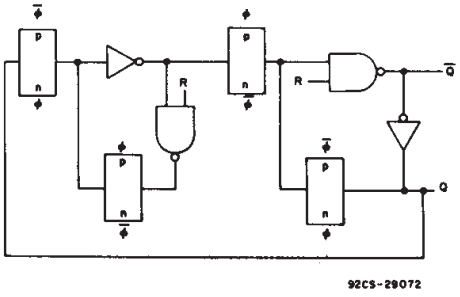


Fig. 2 – Detail of typical flip-flop stage.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) ..... −0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... −55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... −65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

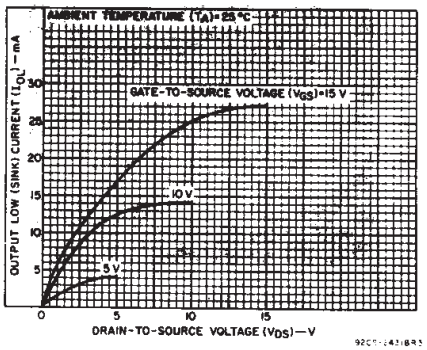


Fig. 3 – Typical n-channel output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current*, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current*, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

*Data not applicable to terminal 9 or 10.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

CHARACTERISTIC	V_{DD}	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V
Input-Pulse Width, t_W (f = 100 kHz)	5	100	–	ns
	10	40	–	
	15	30	–	
Input-Pulse Rise Time and Fall Time, $t_{r\phi}$, $t_{f\phi}$	5	Unlimited		
	10			
	15			
Input-Pulse Frequency, $f_{\phi I}$ (External pulse source)	5	–	3.5	MHz
	10	–	8	
	15	–	12	
Reset Pulse Width, t_W	5	120	–	ns
	10	60	–	
	15	40	–	

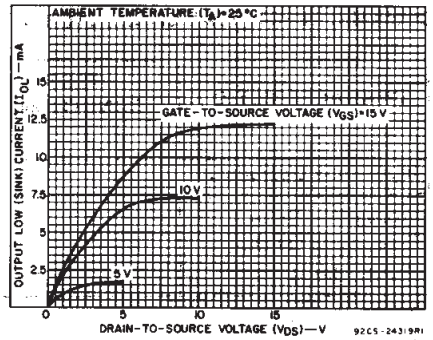


Fig. 4 – Minimum n-channel output low (sink) current characteristics.

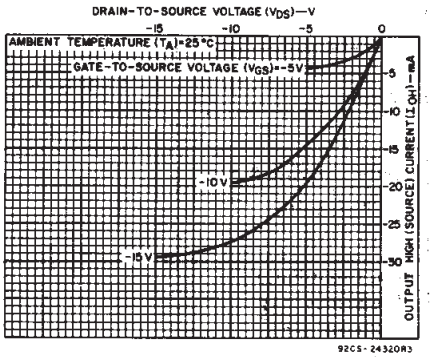


Fig. 5 – Typical p-channel output high (source) current characteristics.

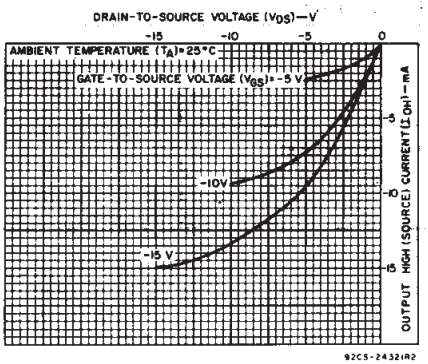


Fig. 6 – Minimum p-channel output high (source) current characteristics.

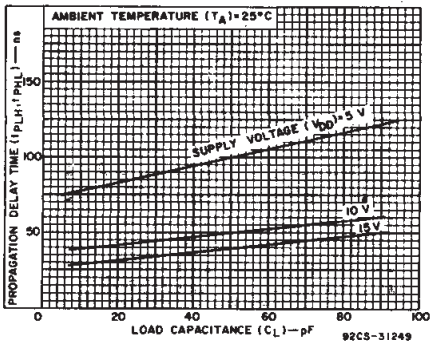


Fig. 7 – Typical propagation delay time (Q_n to Q_n+1) as a function of load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Input-Pulse Operation						
Propagation Delay Time, ϕ_I to Q4 Out; t_{PHL}, t_{PLH}		5	–	370	740	ns
		10	–	150	300	
		15	–	100	200	
Propagation Delay Time, Q_n to Q_{n+1}; t_{PHL}, t_{PLH}		5	–	100	200	
		10	–	50	100	
		15	–	40	80	
Transition Time, t_{THL}, t_{TLH}		5	–	100	200	
		10	–	50	100	
		15	–	40	80	
Min. Input-Pulse Width, t_W	f = 100 kHz	5	–	50	100	
		10	–	20	40	
		15	–	15	30	
Input-Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$		5	Unlimited			
		10				
		15				
Max. Input-Pulse Frequency, $f_{\phi I}$ (External pulse source)		5	3.5	7	–	MHz
		10	8	16	–	
		15	12	24	–	
Input Capacitance, C_I	Any Input		–	5	7.5	pF
Reset Operation						
Propagation Delay Time, t_{PHL}		5	–	180	360	ns
		10	–	80	160	
		15	–	50	100	
Minimum Reset Pulse Width, t_W		5	–	60	120	
		10	–	30	60	
		15	–	20	40	

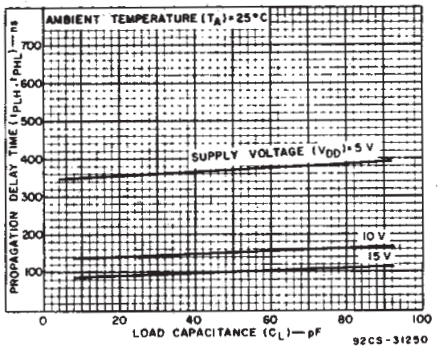


Fig. 8 – Typical propagation delay time (ϕ_I to Q_4 Output) as a function of load capacitance.

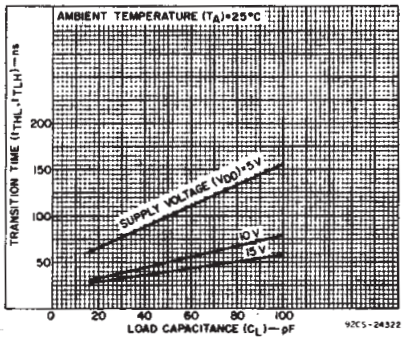


Fig. 9 – Typical transition time as a function of load capacitance.

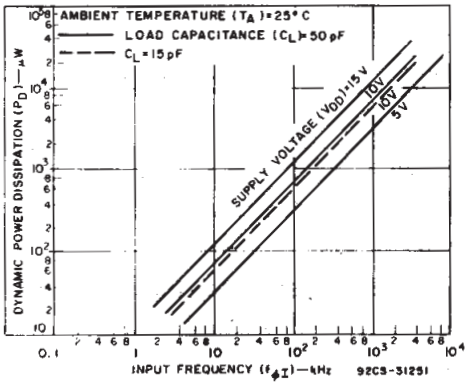


Fig. 10 – Typical dynamic power dissipation as a function of input frequency.

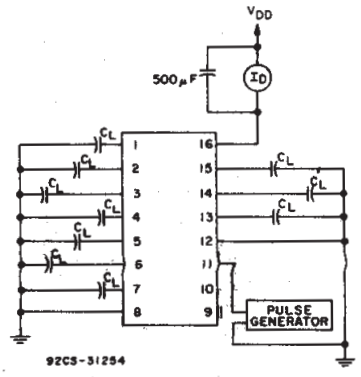


Fig. 11 – Dynamic power dissipation test circuit.

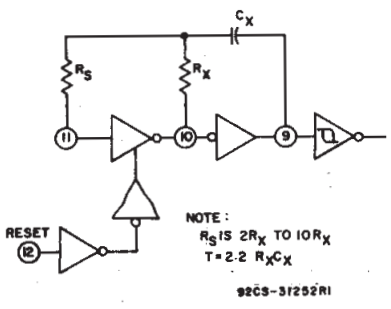


Fig. 12 – Typical RC circuit.

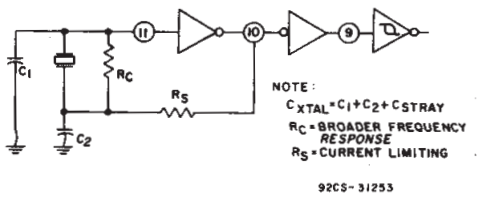


Fig. 13 – Typical crystal circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ [cont'd]

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
RC Operation						
Variation of Frequency (Unit-to-Unit)	C_X = 200 pF, R_S = 560 kΩ, R_X = 50 kΩ	5	—	23±10%	—	kHz
		10	—	24±10%	—	
		15	—	25±10%	—	
Variation of Frequency with voltage change (Same Unit)	C_X = 200 pF, R_S = 560 kΩ, R_X = 50 kΩ	5V to 10 V	—	1.5	—	
		10V to 15V	—	0.5	—	
R_X max.	C_X = 10 μF	5	—	—	20	MΩ
	= 50 μF	10	—	—	20	
	= 10 μF	15	—	—	10	
C_X max.	R_X = 500 kΩ	5	—	—	1000	μF
	= 300 kΩ	10	—	—	50	
	= 300 kΩ	15	—	—	50	
Maximum Oscillator Frequency*	R_X = 5 kΩ, R_S = 30 kΩ, C_X = 15 pF	10	530	650	810	kHz
		15	690	800	940	
Drive Current at Pin 9 (For Oscillator Design)						mA
I_{OL}	V_O = 0.4 V	5	0.16	0.35	—	
	= 0.5 V	10	0.42	0.8	—	
	= 1.5 V	15	1	2	—	
I_{OH}	V_O = 4.6 V	5	-0.16	-0.35	—	
	= 9.5 V	10	-0.42	-0.8	—	
	= 13.5 V	15	-1	-2	—	

*RC oscillator applications are not recommended at supply voltages below 7 V for R_X < 50 kΩ.

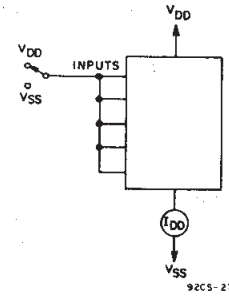


Fig. 14 – Quiescent device current.

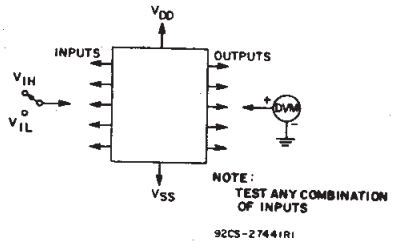


Fig. 15 – Input voltage.

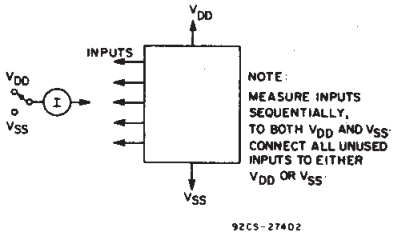
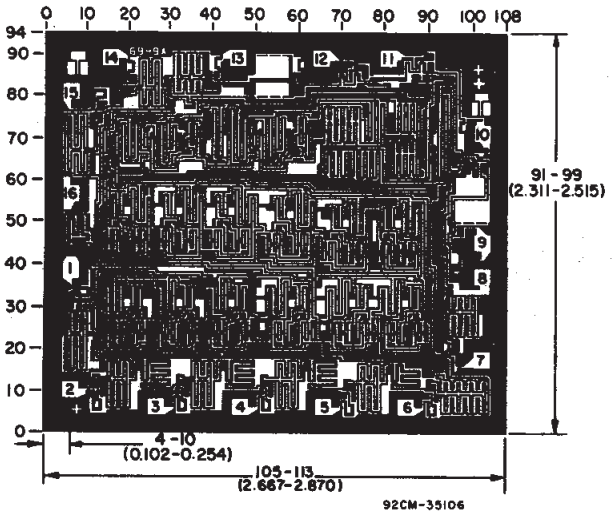


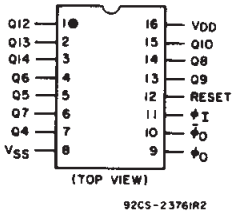
Fig. 16 – Input current.



Chip dimensions and pad layout for CD4060B

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

TERMINAL DIAGRAM



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD4060BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4060BF	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4060BF3A	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4060BM	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4060BM96	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4060BMT	ACTIVE	SOIC	D	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4060BNSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4060BPW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4060BPWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

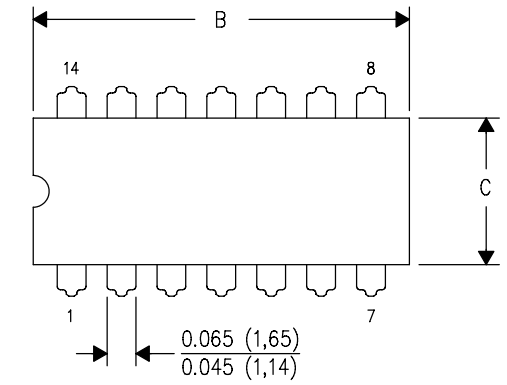
(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

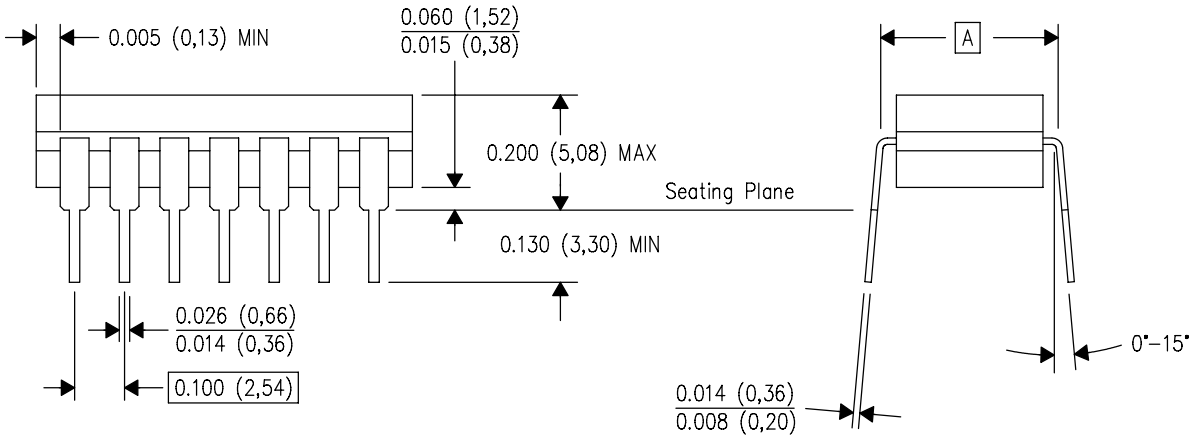
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



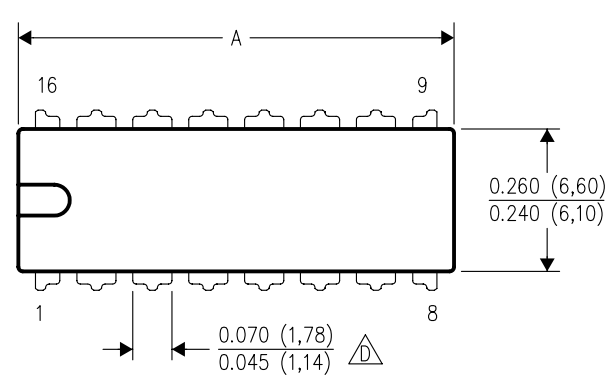
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

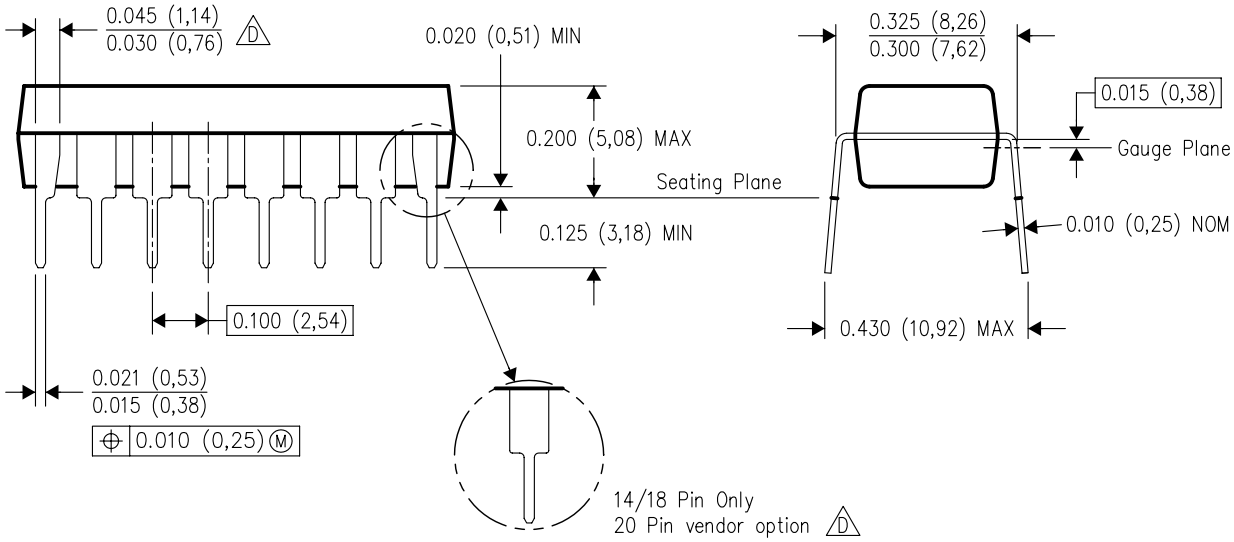
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



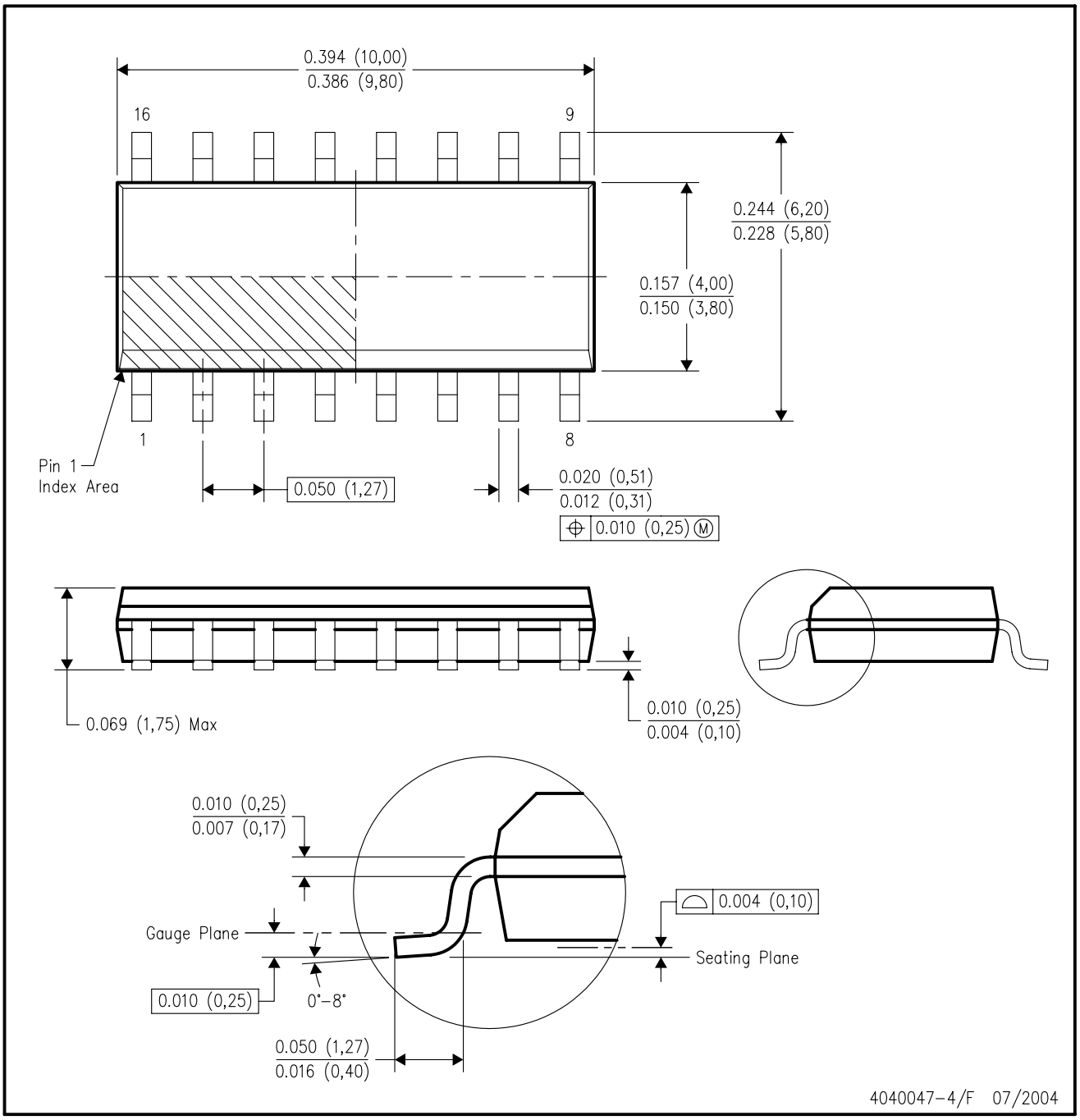
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE

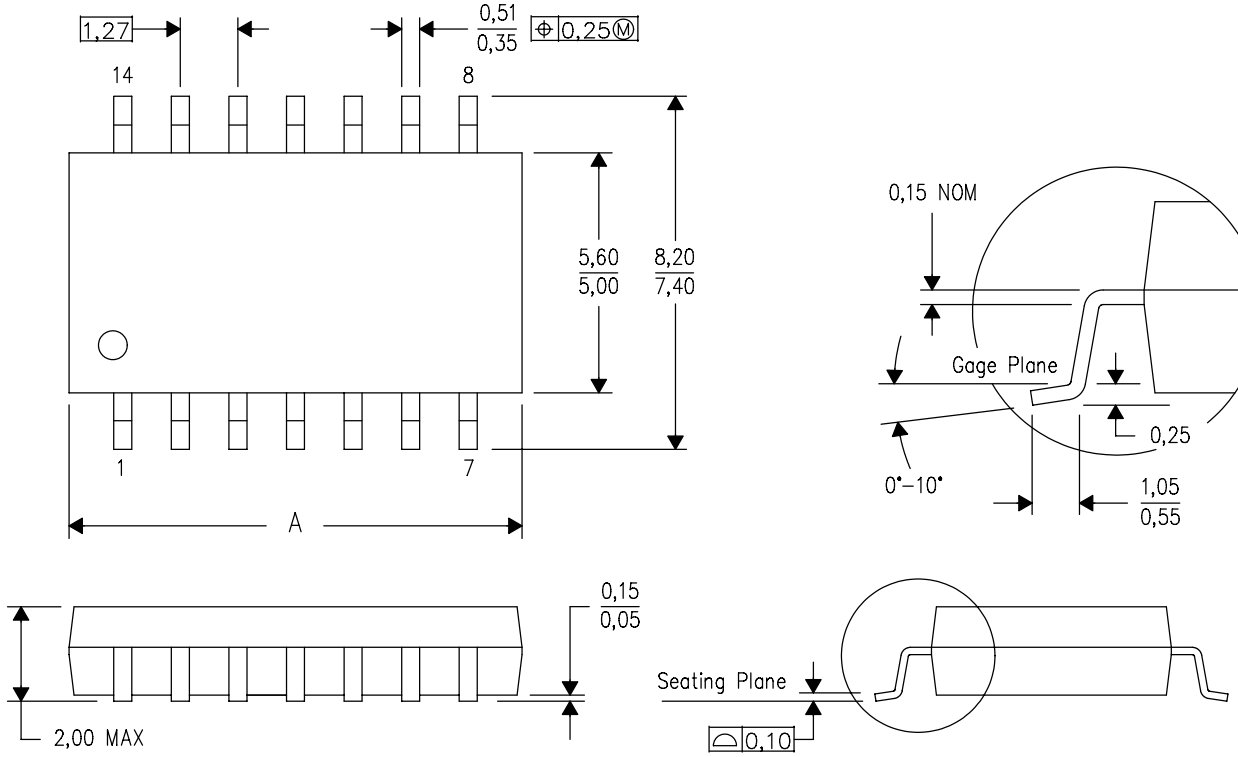


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



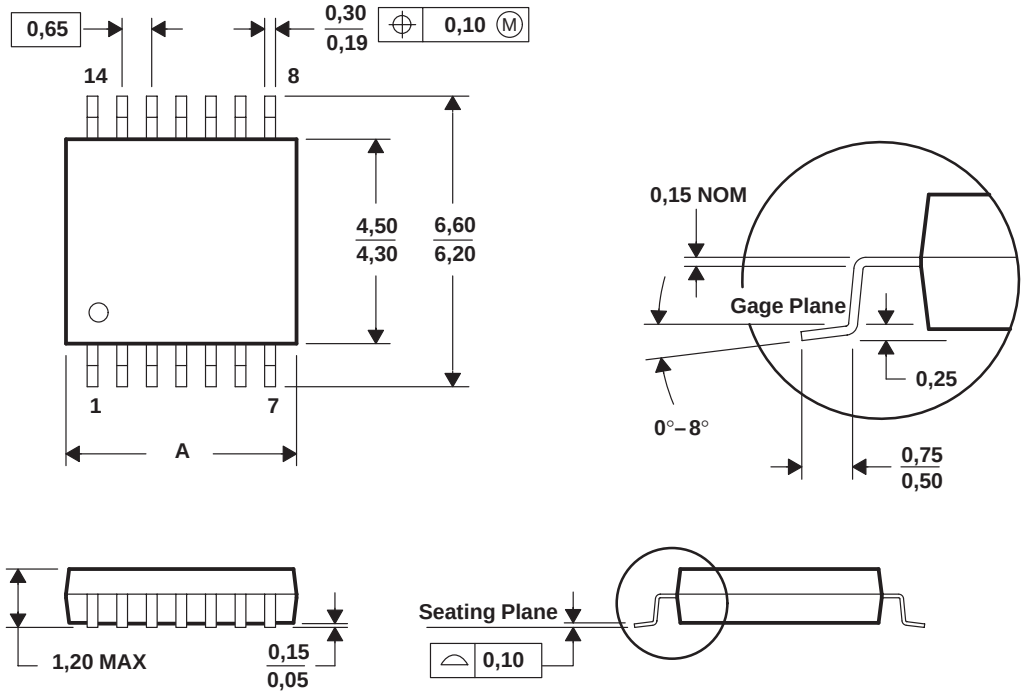
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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This file is the datasheet for the following electronic components:

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CD4060BM96 - http://www.ti.com/product/cd4060bm96?HQS=TI-null-null-dscatalog-df-pf-null-wwe

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