

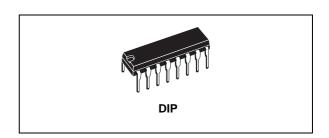
# **DUAL 64 STAGE STATIC SHIFT REGISTER**

- CLOCK FREQUENCY 12MHz (Typ.) at V<sub>DD</sub> = 10V
- SCHMITT TRIGGER CLOCK INPUTS ALLOWS OPERATION WITH VERY SLOW CLOCK RISE AND FALL TIMES
- THREE STATE OUTPUTS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTCS
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I<sub>I</sub> = 100nA (MAX) AT V<sub>DD</sub> = 18V T<sub>A</sub> = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



HCF4517B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP package.

This device is a dual 64-stage static shift register consisting of two independent registers each having a clock, data, and write enable input and outputs accessible by stages following the 16th,

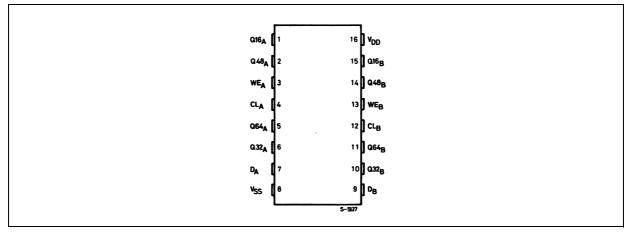


#### **ORDER CODES**

PACKAGE	TUBE	T&R
DIP	HCF4517BEY	
SOP	HCF4517BM1	HCF4517M013TR

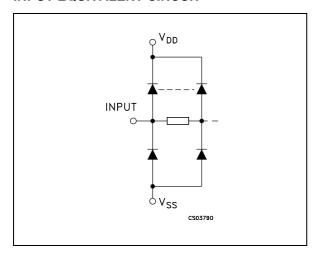
32nd, 48th, and 64th stages. These stages also serve as input points allowing data to be put in at the 17th, 33rd, and 49th stages when the write enable input is a logic 1 and the clock goes through a low to high transition. The truth table indicates how the clock and write enable inputs control the operation of HCF4517B. Inputs at the intermediate stages allow entry of 64-bits into the register with 16 clock pulses. The 3-state outputs permit connection of this device to an external bus.

#### **PIN CONNECTION**



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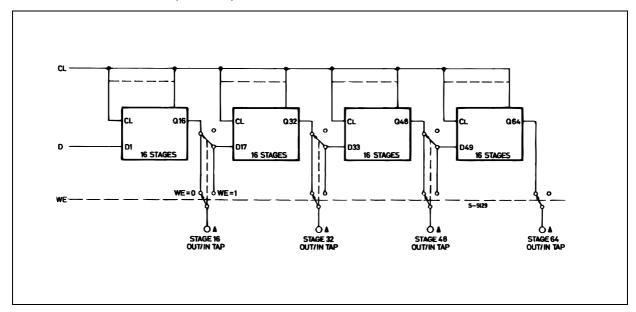
### INPUT EQUIVALENT CIRCUIT



### **PIN DESCRIPTION**

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 5, 6	QnA	IN/OUT Stage
10, 11,14, 15	QnB	IN/OUT Stage
3, 13	WEA, WEB	Write Enable
7, 9	DA, DB	Data Input
4, 12	CLA, CLB	Clock
8	$V_{SS}$	Negative Supply Voltage
16	V <sub>DD</sub>	Positive Supply Voltage

# FUNCTIONAL DIAGRAM (One Half)



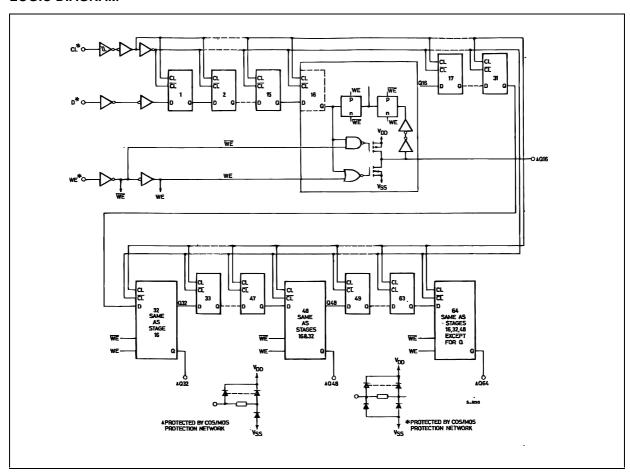
### **TRUTH TABLES**

CLOCK	WRITE ENABLE	DATA	STAGE 16 TAP	STAGE 32 TAP	STAGE 48 TAP	STAGE 64 TAP
L	L	Х	Q16	Q32	Q48	Q64
L	Н	Х	Z	Z	Z	Z
Н	L	Х	Q16	Q32	Q48	Q64
Н	Н	Х	Z	Z	Z	Z
	L	DI In	Q16	Q32	Q48	Q64
	Н	DI In	D17 In	D33 In	D49 In	Z
L	L	Х	Q16	Q32	Q48	Q64
	Н	X	Z	Z	Z	Z

X : Don't Care

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### **LOGIC DIAGRAM**



### **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	Supply Voltage	-0.5 to +22	V
V <sub>I</sub>	DC Input Voltage	-0.5 to V <sub>DD</sub> + 0.5	V
I <sub>I</sub>	DC Input Current	± 10	mA
$P_{D}$	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T <sub>op</sub>	Operating Temperature	-55 to +125	°C
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V<sub>SS</sub> pin voltage.

### **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	3 to 20	V
V <sub>I</sub>	Input Voltage	0 to V <sub>DD</sub>	V
T <sub>op</sub>	Operating Temperature	-55 to 125	°C



## **DC SPECIFICATIONS**

		Test Condition			Value								
Symbol	Parameter	VI	v <sub>o</sub>	I <sub>O</sub>	II <sub>O</sub> I V <sub>DD</sub>	T <sub>A</sub> = 25°C		-40 to 85°C		-55 to 125°C		Unit	
		(V)		(V)	Min.	Тур.	Max.	Min.	Max.	Min.	Max.		
ΙL	Quiescent Current	0/5			5		0.04	5		150		150	
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	μΑ
		0/20			20		0.08	100		3000		3000	
V <sub>OH</sub>	High Level Output	0/5		<1	5	4.95			4.95		4.95		
	Voltage	0/10		<1	10	9.95			9.95		9.95		V
		0/15		<1	15	14.95			14.95		14.95		
$V_{OL}$	Low Level Output	5/0		<1	5		0.05			0.05		0.05	
	Voltage	10/0		<1	10		0.05			0.05		0.05	V
		15/0		<1	15		0.05			0.05		0.05	
V <sub>IH</sub>	High Level Input		0.5/4.5	<1	5	3.5			3.5		3.5		
Voltage	Voltage		1/9	<1	10	7			7		7		V
			1.5/13.5	<1	15	11			11		11		
V <sub>IL</sub>	Low Level Input		4.5/0.5	<1	5			1.5		1.5		1.5	
	Voltage		9/1	<1	10			3		3		3	V
			13.5/1.5	<1	15			4		4		4	
I <sub>OH</sub>	Output Drive	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		
	Current	0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		mA
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		IIIA
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I <sub>OL</sub>	Output Sink	0/5	0.4	<1	5	1.74	4		1.43		1.43		
	Current Q	0/10	0.5	<1	10	4.42	10.4		3.74		3.74		mA
		0/15	1.5	<1	15	11.56	27.2		9.52		9.52		
l <sub>OL</sub>	Output Sink	0/5	0.4	<1	5	0.44	1		0.36		0.36		
	Current	0/10	0.5	<1	10	1.1	2.6		0.9		0.9		mA
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I <sub>I</sub>	Input Leakage Current	0/18	Any In	put	18		±10 <sup>-5</sup>	±0.1		±1		±1	μΑ
l <sub>OZ</sub>	3-State Output Leakage Current	0/18	Any In	put	18		±10 <sup>-4</sup>	±0.4		±12		±12	μΑ
C <sub>I</sub>	Input Capacitance		Any In	put			5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with  $V_{DD}$ =5V, 2V min. with  $V_{DD}$ =10V, 2.5V min. with  $V_{DD}$ =15V

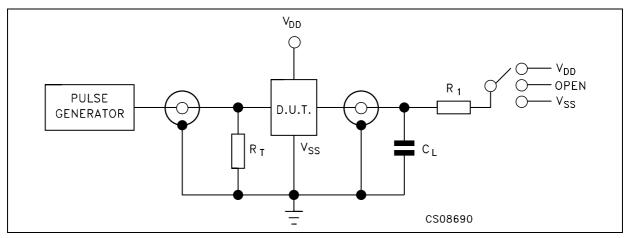
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**DYNAMIC ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ}C$ ,  $C_L = 50 pF$ ,  $R_L = 200 K\Omega$ ,  $t_f = t_f = 20 ns$ )

Symbol Parame			Test Condition	١	Value (*)		
	Parameter	V <sub>DD</sub> (V)		Min.	Тур.	Max.	
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay Time :	5			200	400	
	CL to Bit 16 Tap	10	1		110	220	ns
		15	]		90	180	
t <sub>PLZ</sub> t <sub>PHZ</sub>	3-State Output WE to Bit	5			75	150	
t <sub>PZL</sub> t <sub>PZH</sub>	16 Tap (see note)	10			40	80	ns
		15			30	60	
t <sub>THL</sub> t <sub>TLH</sub>	Output Transition Time	5			100	200	
		10			50	100	ns
		15			40	80	
t <sub>setup</sub>	Setup Time (WRITE	5		-100	-50		
ENABLE to CLOCK)	10		-50	-25		ns	
	15		-30	-15			
t <sub>setup</sub> Setup Time (DATA to CLOCK)	5		-100	-50			
	CLOCK)	10	]	-60	-30		ns
		15		-30	-15		
	Release Time (WRITE	5			50	100	
	ENABLE to CLOCK)	10			25	50	ns
		15			20	40	
t <sub>hold</sub>	Hold Time (DATA to	5			100	200	
	CLOCK)	10			50	100	ns
		15			25	50	
t <sub>W</sub>	Minimum Clock Pulse	5			90	180	
	Width	10			40	80	ns
		15			25	50	
f <sub>CL</sub> Maximum Clock Input Frequency		5		3	6		
	Frequency	10		6	12		MHz
		15		8	15		
t <sub>r</sub> t <sub>f</sub>	Maximum Clock Input Rise	5					
	or Fall Time	10		ι	Jnlimite	d	μs
		15					ĺ

(\*) Typical temperature coefficient for all V<sub>DD</sub> value is 0.3 %/°C. NOTE: Measured at the point of 10% change in output load of 50pF,  $R_L = 1K\Omega$  to  $V_{DD}$  for  $t_{PZL}$ ,  $t_{PLZ}$  and  $R_L = 1K\Omega$  to  $V_{SS}$  for  $t_{PHZ}$ 

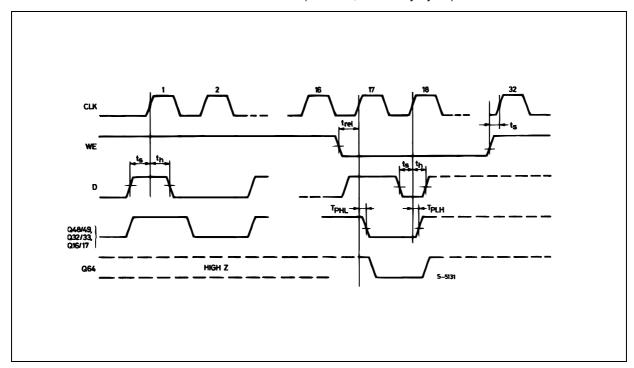
### **TEST CIRCUIT**



TEST	SWITCH
t <sub>PLH</sub> , t <sub>PHL</sub>	Open
t <sub>PZL</sub> , t <sub>PLZ</sub>	$V_{DD}$
t <sub>PZH</sub> , t <sub>PHZ</sub>	$V_{SS}$

 $C_L$  = 50pF or equivalent (includes jig and probe capacitance)  $R_L$  = 200 $K\Omega$   $R_T$  =  $Z_{OUT}$  of pulse generator (typically 50 $\Omega$ )

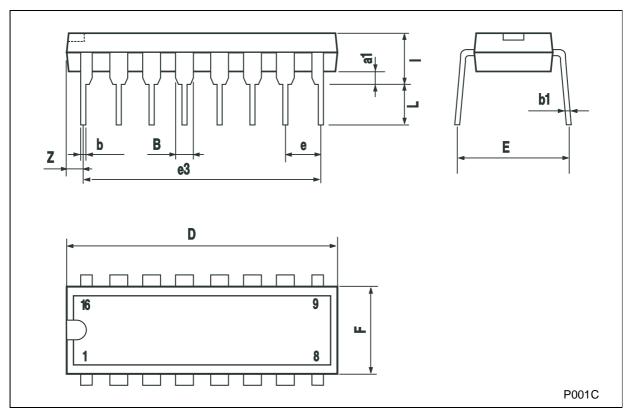
# WAVEFORM: PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)



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# Plastic DIP-16 (0.25) MECHANICAL DATA

DIM		mm.				
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
В	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
е		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



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