

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4076B** **MSI**

Quadruple D-type register with  
3-state outputs

Product specification  
File under Integrated Circuits, IC04

January 1995

Quadruple D-type register with 3-state outputs

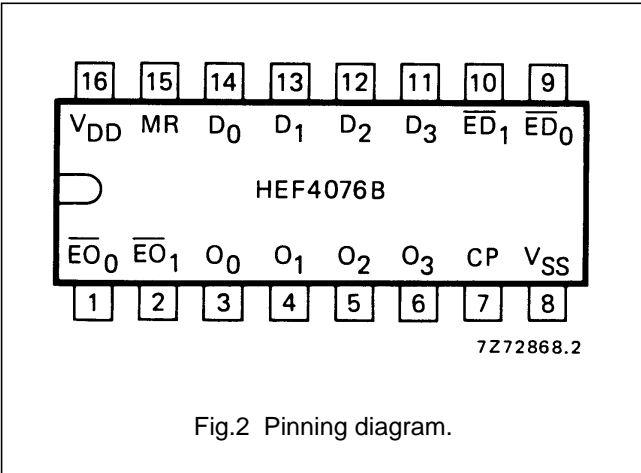
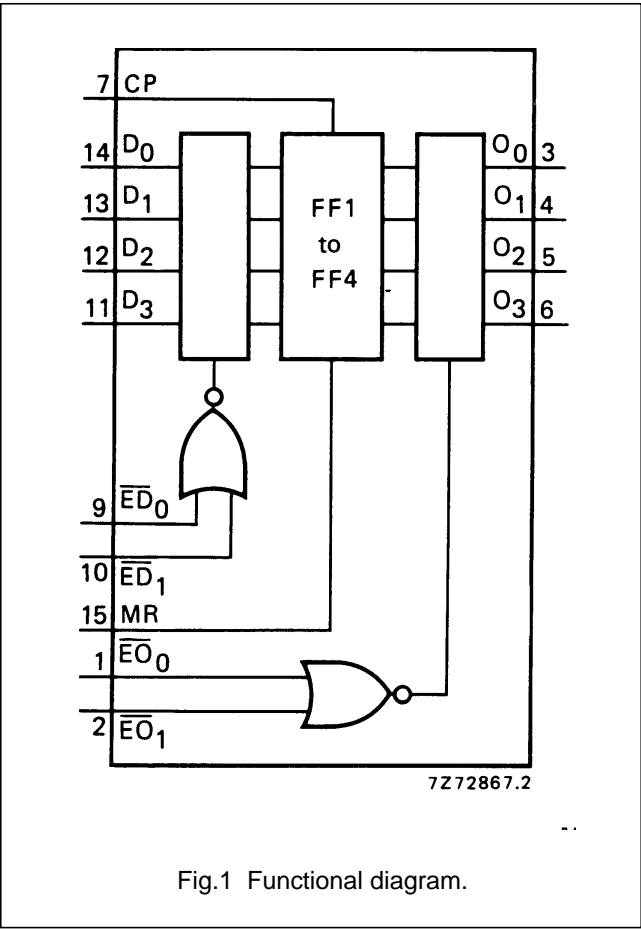
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DESCRIPTION

The HEF4076B is a quadruple edge-triggered D-type flip-flop with four data inputs ( $D_0$  to  $D_3$ ), two active LOW data enable inputs ( $\overline{ED}_0$  and  $\overline{ED}_1$ ), a common clock input (CP), four 3-state outputs ( $O_0$  to  $O_3$ ), two active LOW output enable inputs ( $\overline{EO}_0$  and  $\overline{EO}_1$ ), and an overriding asynchronous master reset input (MR).

Information on  $D_0$  to  $D_3$  is stored in the four flip-flops on the LOW to HIGH transition of CP if both  $\overline{ED}_0$  and  $\overline{ED}_1$  are LOW. A HIGH on either  $\overline{ED}_0$  or  $\overline{ED}_1$  prevents the flip-flops from changing on the LOW to HIGH transition of CP, independent of the information on  $D_0$  to  $D_3$ . When both  $\overline{EO}_0$  and  $\overline{EO}_1$  are LOW, the contents of the four flip-flops are available at  $O_0$  to  $O_3$ . A HIGH on either  $\overline{EO}_0$  or  $\overline{EO}_1$  forces  $O_0$  to  $O_3$  into the high impedance OFF-state. A HIGH on MR resets all four flip-flops, independent of all other input conditions.



PINNING

- $D_0$  to  $D_3$  data inputs
- $\overline{ED}_0$ ,  $\overline{ED}_1$  data enable inputs (active LOW)
- $\overline{EO}_0$ ,  $\overline{EO}_1$  output enable inputs (active LOW)
- CP clock input (LOW to HIGH, edge-triggered)
- MR master reset input
- $O_0$  to  $O_3$  data outputs

FAMILY DATA,  $I_{DD}$  LIMITS category MSI

See Family Specifications

## Quadruple D-type register with 3-state outputs

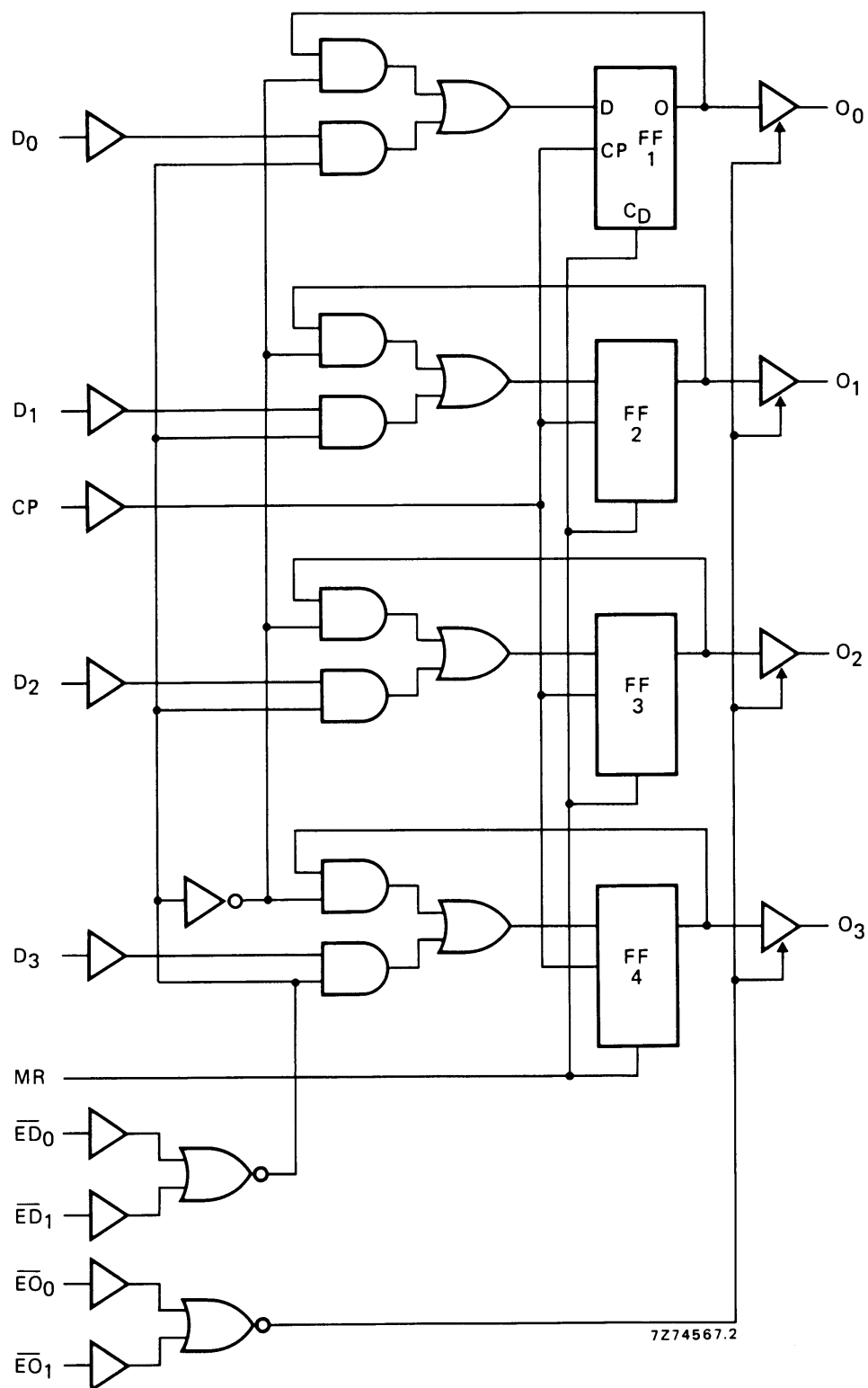
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Fig.3 Logic diagram.

## Quadruple D-type register with 3-state outputs

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## FUNCTION TABLE

INPUTS					OUTPUTS
MR	CP	$\overline{ED}_0$	$\overline{ED}_1$	$D_n$	$O_n$
H	X	X	X	X	L
L	$\nearrow$	H	X	X	no change
L	$\nearrow$	X	H	X	no change
L	$\nearrow$	L	L	H	H
L	$\nearrow$	L	L	L	L
L	$\searrow$	X	X	X	no change

## Notes

1.  $\overline{EO}_0 = \overline{EO}_1 = \text{LOW}$ When either  $\overline{EO}_0$  or  $\overline{EO}_1$  is HIGH, the outputs are disabled (high impedance OFF-state).

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

 $\nearrow$  = positive-going transition $\searrow$  = negative-going transition

## AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$ ; see also waveforms Fig.4

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays	5 10 15	$t_{PHL}$		150	305 ns	123 ns + (0,55 ns/pF) $C_L$
				60	120 ns	49 ns + (0,23 ns/pF) $C_L$
				45	85 ns	37 ns + (0,16 ns/pF) $C_L$
	5 10 15	$t_{PLH}$		160	320 ns	133 ns + (0,55 ns/pF) $C_L$
				65	130 ns	54 ns + (0,23 ns/pF) $C_L$
				45	90 ns	37 ns + (0,16 ns/pF) $C_L$
	5 10 15	$t_{PHL}$		95	190 ns	68 ns + (0,55 ns/pF) $C_L$
				40	85 ns	29 ns + (0,23 ns/pF) $C_L$
				30	65 ns	22 ns + (0,16 ns/pF) $C_L$
Output transition times	5 10 15	$t_{THL}$		60	120 ns	10 ns + (1,0 ns/pF) $C_L$
				30	60 ns	9 ns + (0,42 ns/pF) $C_L$
				20	40 ns	6 ns + (0,28 ns/pF) $C_L$
	5 10 15	$t_{TLH}$		60	120 ns	10 ns + (1,0 ns/pF) $C_L$
				30	60 ns	9 ns + (0,42 ns/pF) $C_L$
				20	40 ns	6 ns + (0,28 ns/pF) $C_L$
3-state propagation times	5 10 15	$t_{PHZ}$		50	105 ns	
				35	70 ns	
				30	65 ns	
	5 10 15	$t_{PLZ}$		45	90 ns	
				30	65 ns	
				30	60 ns	

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	V <sub>DD</sub> V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Output enable times $\overline{EO}_n \rightarrow O_n$ HIGH  LOW	5	$t_{PZH}$		65	130 ns	
	10			30	55 ns	
	15			20	40 ns	
	5	$t_{PZL}$		60	120 ns	
	10			25	50 ns	
	15			20	35 ns	

## AC CHARACTERISTICS

V<sub>SS</sub> = 0 V; T<sub>amb</sub> = 25 °C; C<sub>L</sub> = 50 pF; input transition times ≤ 20 ns

	V <sub>DD</sub> V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Set-up times D <sub>n</sub> → CP  $\overline{ED}_n \rightarrow CP$	5	$t_{su}$	10	−15	ns	see also waveforms Fig.4
	10		0	−10	ns	
	15		0	−5	ns	
	5	$t_{su}$	0	−50	ns	
	10		0	−20	ns	
	15		0	−15	ns	
Hold times D <sub>n</sub> → CP  $\overline{ED}_n \rightarrow CP$	5	$t_{hold}$	55	30	ns	
	10		20	10	ns	
	15		15	10	ns	
	5	$t_{hold}$	25	−25	ns	
	10		10	−10	ns	
	15		5	−5	ns	
Minimum clock pulse width; LOW	5	$t_{WCPL}$	120	60	ns	
	10		45	20	ns	
	15		30	15	ns	
Minimum MR pulse width; HIGH	5	$t_{WMRH}$	55	25	ns	
	10		30	15	ns	
	15		20	10	ns	
Recovery time for MR	5	$t_{RMR}$	90	45	ns	
	10		35	15	ns	
	15		20	10	ns	
Maximum clock pulse frequency	5	$f_{max}$	4	8	MHz	
	10		11	22	MHz	
	15		16	32	MHz	

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	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu$ W)	
Dynamic power dissipation per package (P)	5 10 15	$2200 f_i + \sum (f_o C_L) \times V_{DD}^2$ $9300 f_i + \sum (f_o C_L) \times V_{DD}^2$ $24\,500 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)

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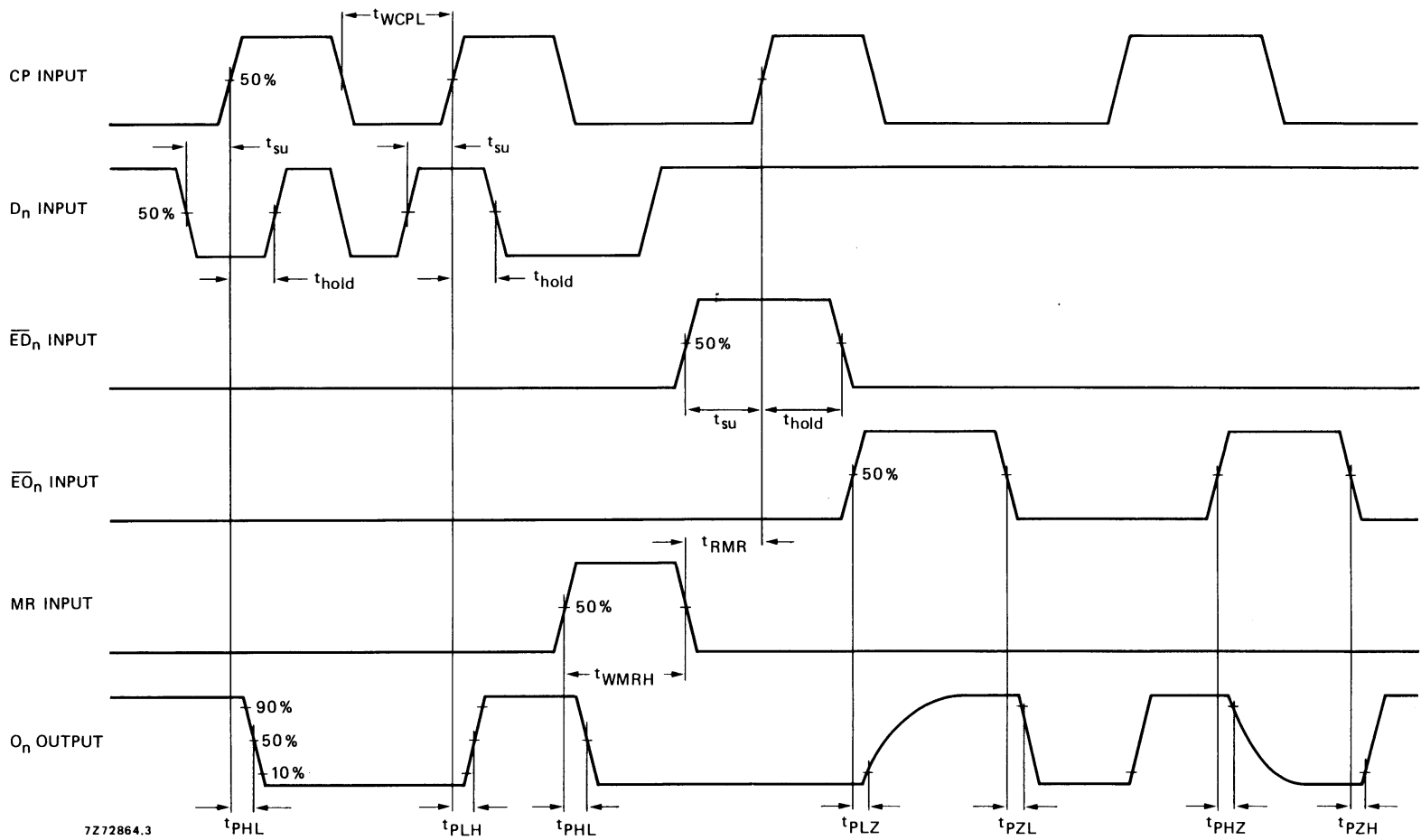


Fig.4 Waveforms showing propagation delays, output disable/enable times, minimum CP and MR pulse widths, set-up and hold times for D<sub>n</sub> to CP and  $\overline{ED}_n$  to CP, and recovery time for MR. Set-up and hold times are shown as positive values but may be specified as negative values.

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