

DATA SHEET

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- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4031B

MSI

64-stage static shift register

Product specification
File under Integrated Circuits, IC04

January 1995

64-stage static shift register

HEF4031B

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DESCRIPTION

The HEF4031B is an edge-triggered 64-stage static shift register with two serial data inputs (D_A , D_B), a data select input \bar{A}/B , a clock input (CP), a buffered clock output (CO), and buffered outputs from the 64th bit position (O_{63} , \bar{O}_{63}). The output O_{63} is capable of driving one TTL load.

Data from D_A or D_B , as determined by the state of \bar{A}/B , is shifted into the first shift register position and all the data in

the register is shifted one position to the right on the LOW to HIGH transition of CP. D_A is selected by a LOW, and D_B by a HIGH on \bar{A}/B . Registers can be cascaded either by connecting all CP inputs together or by driving CP of the most right-hand register with the system clock and connecting CO to CP of the preceding register. When the second technique is used in the recirculating mode, a flip-flop must be used to store O_{63} of the most right-hand register until the most left-hand register is clocked.

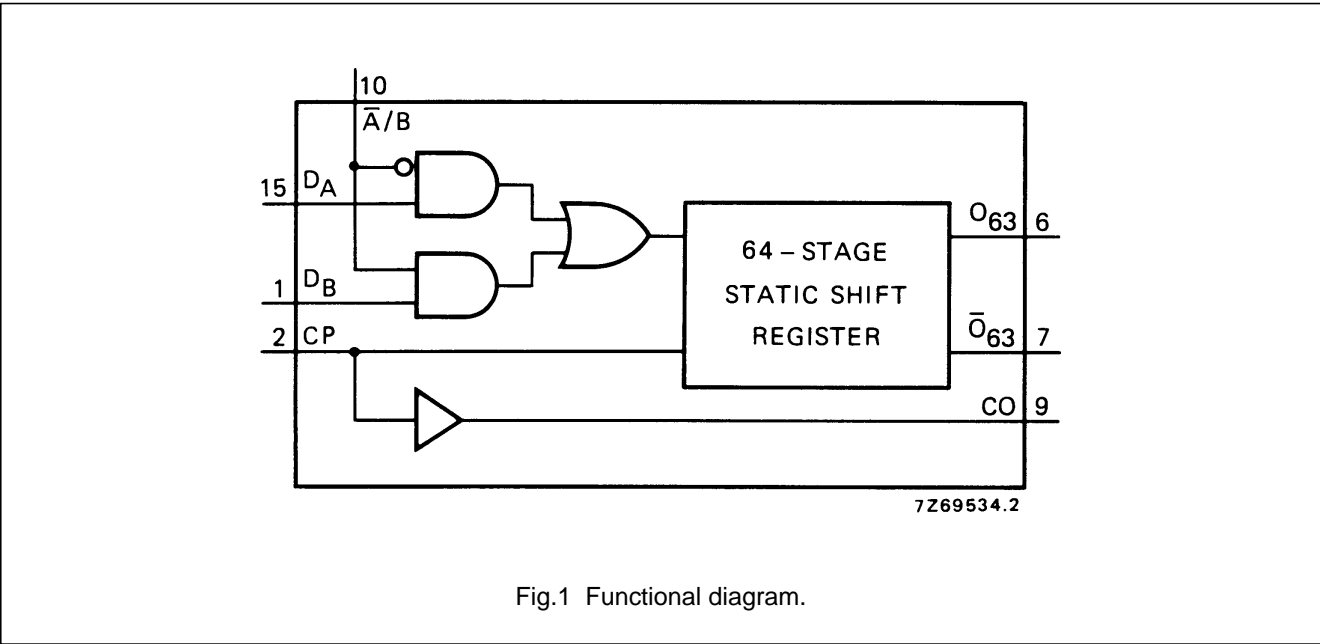


Fig.1 Functional diagram.

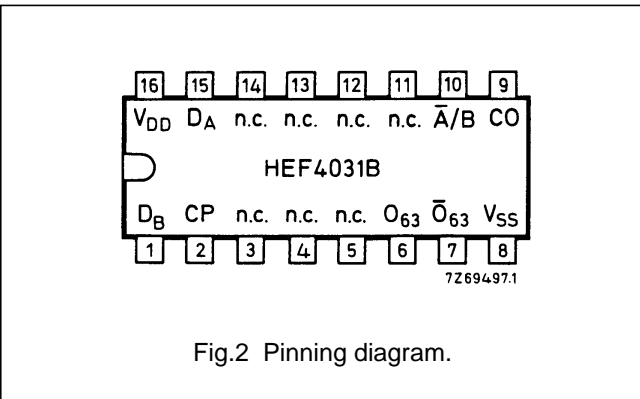


Fig.2 Pinning diagram.

PINNING

- D_A , D_B data inputs
- \bar{A}/B data select input
- CP clock input (LOW to HIGH edge-triggered)
- CO buffered clock output
- O_{63} buffered output from the 64th stage
- \bar{O}_{63} complementary buffered output from the 64th stage

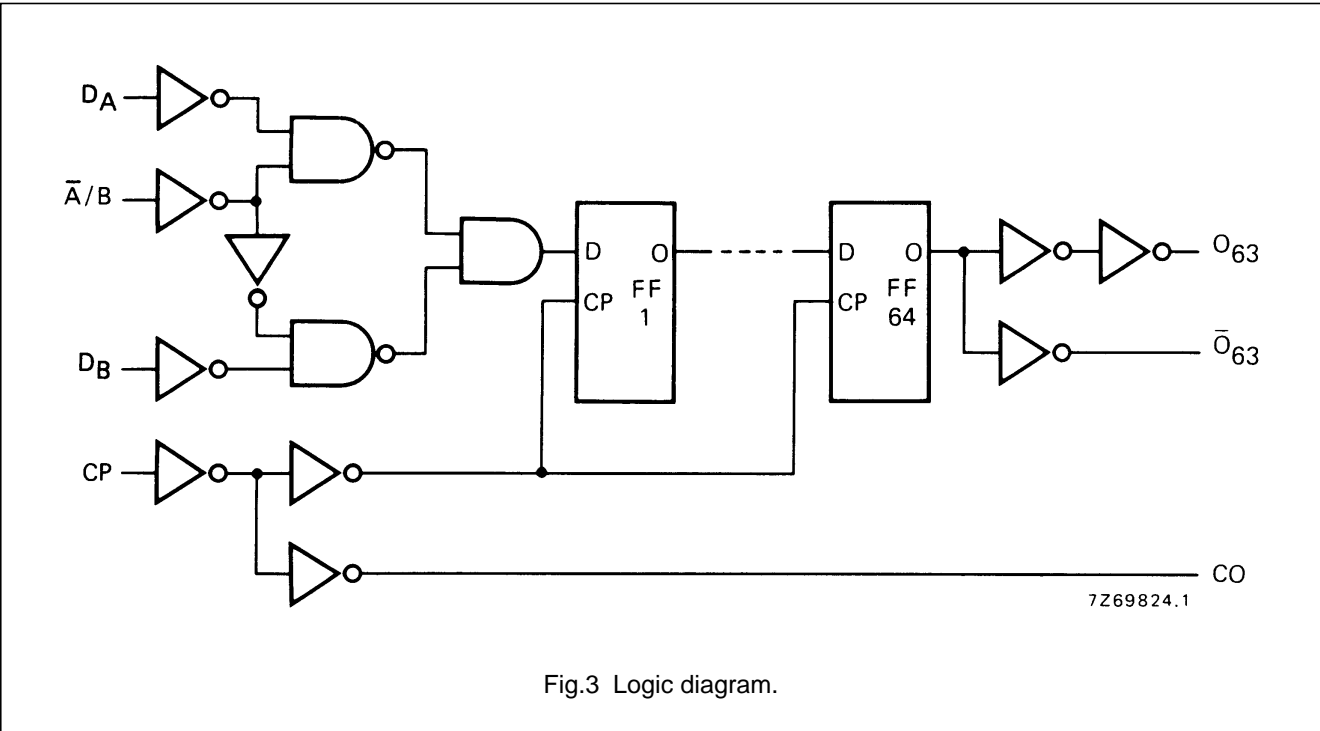
FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

- HEF4031BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4031BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4031BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

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DC CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD}

	V_{DD} V	V_{OH} V	V_{OL} V	SYMBOL	$T_{amb} (^{\circ}\text{C})$					
					-40		+ 25		+ 85	
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Output (source)	5	4, 6			1,0	0,85		0,65		mA
current	10	9,5		$-I_{OH}$	3,0	2,5		2,0		mA
HIGH; O_{63}	15	13,5			10,0	8,5		6,5		mA
HIGH; \bar{O}_{63}	5	2,5		$-I_{OH}$	3,0	2,5		2,0		mA
Output (sink)	4,75		0,4		2,7	2,3		1,8		mA
current	10		0,5	I_{OL}	9,5	8,0		6,3		mA
LOW; O_{63}	15		1,5		24,0	20,0		16,0		mA

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AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
CP \rightarrow O ₆₃	5			180	360 ns	167 ns + (0,26 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		65	130 ns	57 ns + (0,16 ns/pF) C _L
	15			45	90 ns	40 ns + (0,11 ns/pF) C _L
LOW to HIGH	5	t _{PLH}		170	340 ns	148 ns + (0,45 ns/pF) C _L
	10			65	130 ns	56 ns + (0,19 ns/pF) C _L
	15			45	90 ns	39 ns + (0,13 ns/pF) C _L
CP \rightarrow $\overline{\text{O}}_{63}$	5			190	380 ns	163 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		75	150 ns	64 ns + (0,23 ns/pF) C _L
	15			50	100 ns	42 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}		190	380 ns	163 ns + (0,55 ns/pF) C _L
	10			75	150 ns	64 ns + (0,23 ns/pF) C _L
	15			50	100 ns	42 ns + (0,16 ns/pF) C _L
CP \rightarrow CO	5			70	140 ns	43 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		35	70 ns	24 ns + (0,23 ns/pF) C _L
	15			25	50 ns	17 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}		55	110 ns	28 ns + (0,55 ns/pF) C _L
	10			30	60 ns	19 ns + (0,23 ns/pF) C _L
	15			25	50 ns	17 ns + (0,16 ns/pF) C _L
Output transition times; O ₆₃	5			25	50 ns	5 ns + (0,40 ns/pF) C _L
HIGH to LOW	10	t _{THL}		12	24 ns	3 ns + (0,18 ns/pF) C _L
	15			8	16 ns	2 ns + (0,13 ns/pF) C _L
LOW to HIGH	5	t _{TLH}		40	80 ns	8 ns + (0,65 ns/pF) C _L
	10			20	40 ns	5 ns + (0,30 ns/pF) C _L
	15			13	26 ns	3 ns + (0,20 ns/pF) C _L
Output transition times; $\overline{\text{O}}_{63}$, CO	5			60	120 ns	10 ns + (1,0 ns/pF) C _L
HIGH to LOW	10	t _{THL}		30	60 ns	9 ns + (0,42 ns/pF) C _L
	15			20	40 ns	6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5	t _{TLH}		60	120 ns	10 ns + (1,0 ns/pF) C _L
	10			30	60 ns	9 ns + (0,42 ns/pF) C _L
	15			20	40 ns	6 ns + (0,28 ns/pF) C _L

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	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Set-up times $D_A, D_B \rightarrow CP$	5 10 15	t_{su}	25 25 10	0 -5 -10	ns ns ns	see also waveforms Fig.4
$\bar{A}/B \rightarrow CP$	5 10 15	t_{su}	30 15 10	10 0 -5	ns ns ns	
Hold times $D_A, D_B \rightarrow CP$	5 10 15	t_{hold}	40 40 40	10 10 10	ns ns ns	
$\bar{A}/B \rightarrow CP$	5 10 15	t_{hold}	40 40 40	10 10 10	ns ns ns	
Minimum clock pulse width; LOW	5 10 15	t_{WCPL}	180 70 50	90 35 25	ns ns ns	
Maximum clock pulse frequency	5 10 15	f_{max}	2,5 7 10	5 14 20	MHz MHz MHz	

AC CHARACTERISTICS $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	$4000 f_i + \sum (f_o C_L) \times V_{DD}^2$ $19\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$ $54\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)

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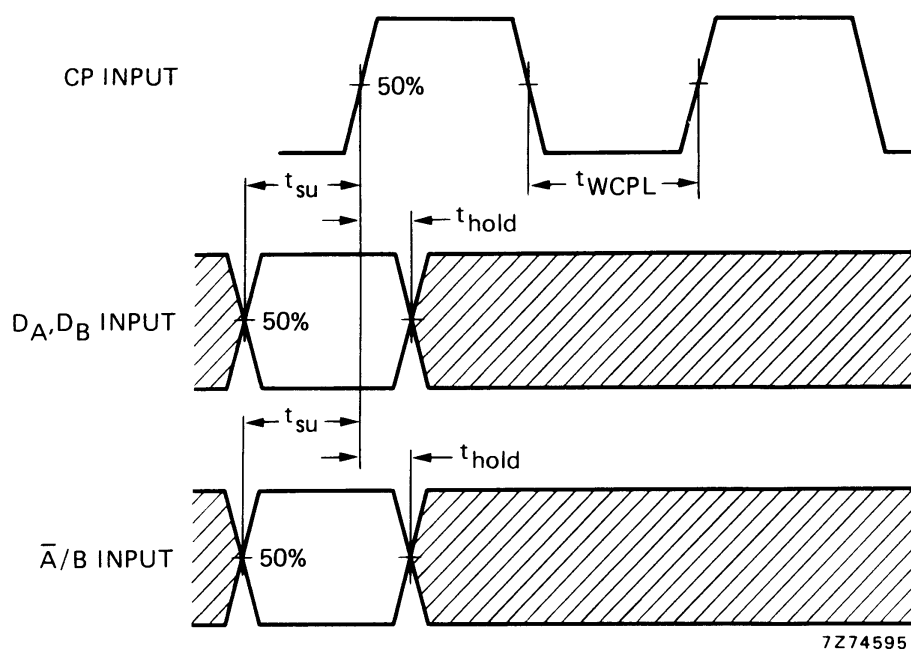
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Fig.4 Waveforms showing minimum clock pulse width, set-up and hold times for D_A , D_B to CP and \bar{A}/B to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

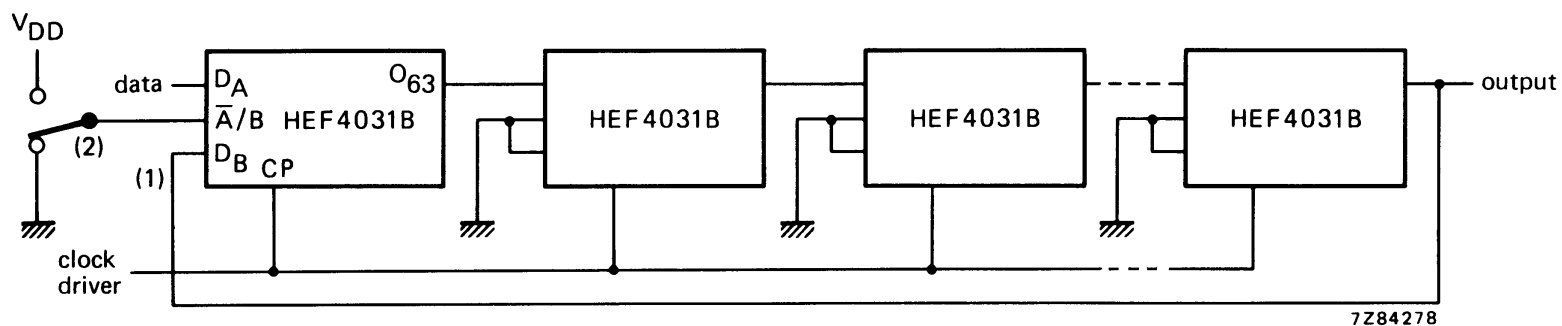
An example of an application for the HEF4031B is:

- Serial shift register.

64-stage static shift register

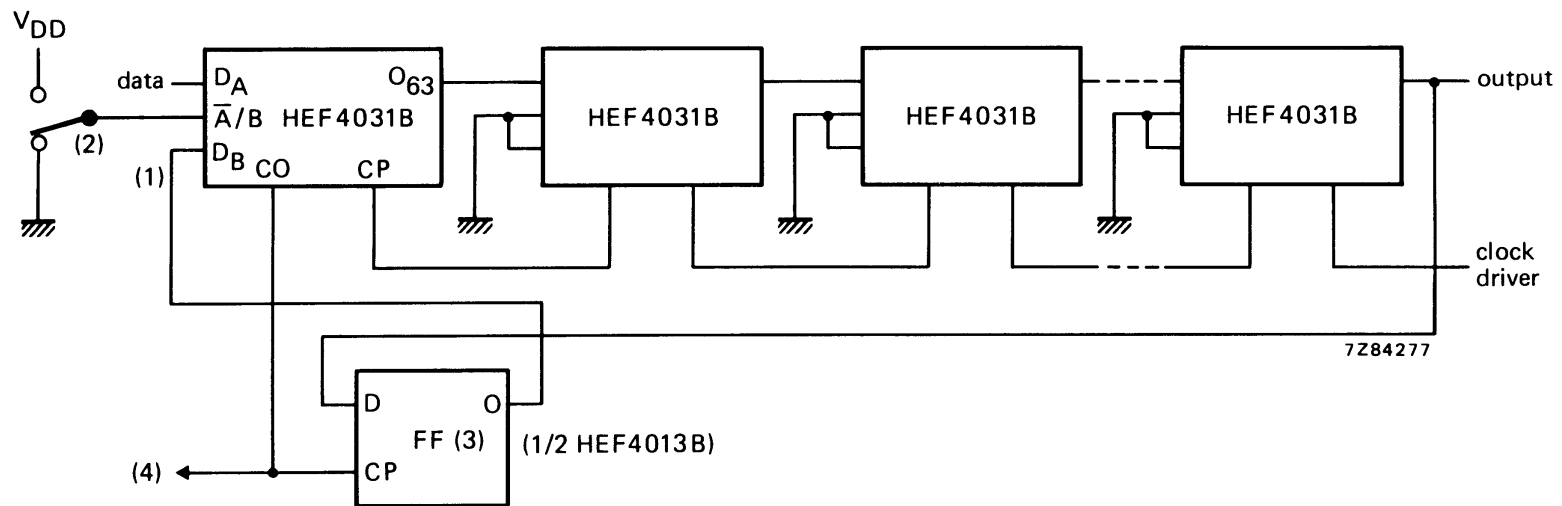
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APPLICATION INFORMATION



- (1) Recirculating input.
(2) Mode control: V_{DD} = recirculation; ground (V_{SS}) = new data.

Fig.5 Cascading using direct clocking for high speed operation (see clock rise and fall time requirements).



- (1) Recirculating input.
(2) Mode control: V_{DD} = recirculation; ground (V_{SS}) = new data.
(3) For recirculation mode only, FF to delay data until first register delayed clocking has occurred.
(4) Delayed clock-to-clock; new data into first register.

Fig.6 Cascading using delayed clocking for reduced clock drive requirements.

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