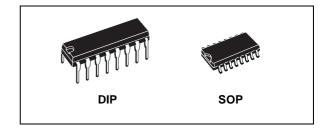


# BINARY RATE MULTIPLIER

- CASCADABLE IN MULTIPLES OF 4-BITS
- SET TO "15" INPUT AND "15" DETECT OUTPUT
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I<sub>1</sub> = 100nA (MAX) AT V<sub>DD</sub> = 18V T<sub>A</sub> = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



#### **ORDER CODES**

PACKAGE	TUBE	T&R
DIP	HCF4089BEY	
SOP	HCF4089BM1	HCF4089M013TR

#### **DESCRIPTION**

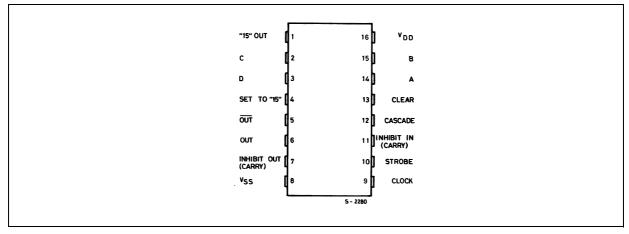
HCF4089B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. HCF4089B is a low power 4-bit digital rate multiplier that provides an output pulse rate that is the clock input pulse rate multiplied by 1/16 times the binary input. For example, when the binary input number is 13, ther will be 13 output pulses for every 16 input pulses.

HCF4089B has an internal synchronous 4-bit counter, which, together with one of the four

binary inputs bits, produces pulse trains as shown in the timing diagram.

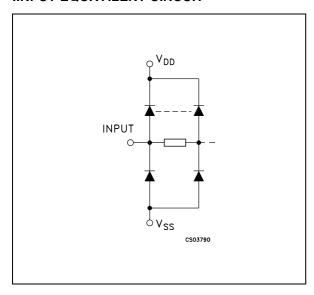
If more than one binary input bit is high, the resulting pulse train is a combination of the above separate pulse trains. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebrical and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversions, and frequency division.

#### **PIN CONNECTION**



September 2002 1/11

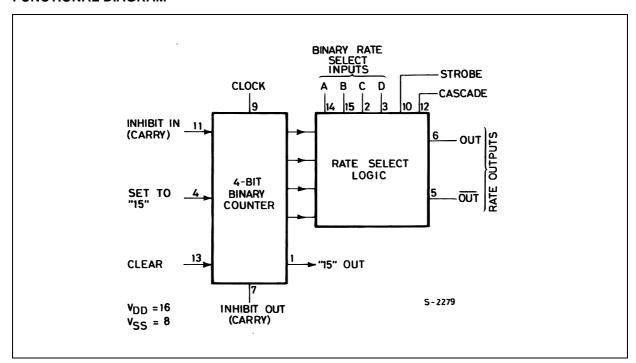
#### **IINPUT EQUIVALENT CIRCUIT**



#### **PIN DESCRIPTION**

PIN No	SYMBOL	NAME AND FUNCTION
14, 15, 2, 3	A, B, C, D	Binary Rate Select Inputs
5	OUT	Rate Output
6	OUT	Rate Output
4	SET TO "15"	Set Input
1	"15" OUT	Output
7	INHIBIT OUT (CARRY)	Inhibit Out (Carry)
13	CLEAR	Clear Input
12	CASCADE	Cascade
11	INHIBIT IN (CARRY)	Inhibit Input (Carry)
10	STROBE	Strobe
9	CLOCK	Clock Input
8	$V_{SS}$	Negative Supply Voltage
16	$V_{DD}$	Positive Supply Voltage

#### **FUNCTIONAL DIAGRAM**

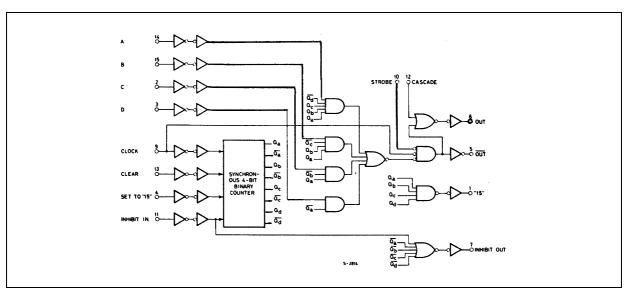


## **TRUTH TABLE**

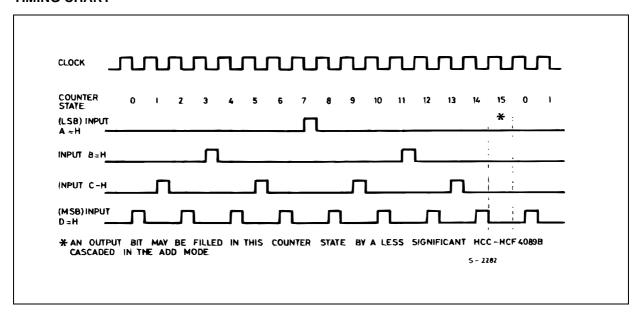
	INPUTS									OUTI	PUTS		
	Number of Pulses or Input Logic Level							Number	of Pulse: Le		ut Logic		
D	С	В	Α	СГОСК	INH IN	STR.	CAS.	CLEAR	SET	оит	OUT	INH OUT	"15" OUT
L	L	L	L	16	L	L	L	L	L	L	Н	1	1
L	L	L	Н	16	L	L	L	L	L	1	1	1	1
L	L	Η	L	16	L	L	L	L	L	2	2	1	1
L	L	Η	Н	16	L	L	L	L	L	3	3	1	1
L	Η	L	L	16	L	L	L	L	L	4	4	1	1
L	Η	L	Н	16	L	L	L	L	L	5	5	1	1
L	Η	Η	L	16	L	L	L	L	L	6	6	1	1
L	Н	Н	Н	16	L	L	L	L	L	7	7	1	1
Н	L	L	L	16	L	L	L	L	L	8	8	1	1
Н	L	L	Н	16	L	L	L	L	L	9	9	1	1
Н	L	Н	L	16	L	L	L	L	L	10	10	1	1
Н	L	Н	Н	16	L	L	L	L	L	11	11	1	1
Н	Н	L	L	16	L	L	L	L	L	12	12	1	1
Н	Н	L	Н	16	L	L	L	L	L	13	13	1	1
Н	Н	Н	L	16	L	L	L	L	L	14	14	1	1
Н	Н	Н	Н	16	L	L	L	L	L	15	15	1	1
Χ	Χ	Χ	Χ	16	Н	L	L	L	L	•	•	Н	•
Χ	Χ	Χ	Χ	16	L	Η	L	L	L	L	Н	1	1
Χ	Χ	Χ	Χ	16	L	L	Н	L	L	Н	*	1	1
Н	Χ	Χ	Χ	16	L	L	L	Н	L	16	16	Н	L
L	Χ	Χ	Χ	16	L	L	L	Н	L	L	Н	Н	L
Χ	Χ	Χ	Χ	16	L	L	L	L	Н	L	Н	L	Н

- X : Don't Care
- : Depends on internal state of counter
- \*: Output same as the first 16 lines of this truth table (depending on values of A, B, C, D)

#### **LOGIC DIAGRAM**



## **TIMING CHART**



#### **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	-0.5 to +22	V
VI	DC Input Voltage	-0.5 to V <sub>DD</sub> + 0.5	V
l <sub>l</sub>	DC Input Current	± 10	mA
$P_{D}$	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T <sub>op</sub>	Operating Temperature	-55 to +125	°C
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to  $V_{\mbox{\footnotesize SS}}$  pin voltage.

#### **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	Supply Voltage	3 to 20	V
V <sub>I</sub>	Input Voltage	0 to V <sub>DD</sub>	V
T <sub>op</sub>	Operating Temperature	-55 to 125	°C

#### **DC SPECIFICATIONS**

			Test Con	dition		Value							
Symbol	Parameter	Vı	v <sub>o</sub>	l <sub>o</sub>	V <sub>DD</sub>	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		Unit
		(V)	(V)	<b>(μA)</b>	(μ <b>A</b> ) (V)	Min.	Тур.	Max.	Min.	Max.	Min.	Max.	
ΙL	Quiescent Current	0/5			5		0.04	5		150		150	
		0/10			10		0.04	10		300		300	μΑ
		0/15			15		0.04	20		600		600	μΑ
		0/20			20		0.08	100		3000		3000	
$V_{OH}$	High Level Output	0/5		<1	5	4.95			4.95		4.95		
	Voltage	0/10		<1	10	9.95			9.95		9.95		V
		0/15		<1	15	14.95			14.95		14.95		
$V_{OL}$	Low Level Output	5/0		<1	5		0.05			0.05		0.05	
	Voltage	10/0		<1	10		0.05			0.05		0.05	V
		15/0		<1	15		0.05			0.05		0.05	
$V_{IH}$	High Level Input		0.5/4.5	<1	5	3.5			3.5		3.5		
	Voltage		1/9	<1	10	7			7		7		V
			1.5/13.5	<1	15	11			11		11		
$V_{IL}$	Low Level Input		4.5/0.5	<1	5			1.5		1.5		1.5	
	Voltage		9/1	<1	10			3		3		3	V
			13.5/1.5	<1	15			4		4		4	
I <sub>OH</sub>	Output Drive	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		
	Current	0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		mA
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		IIIA
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
$I_{OL}$	Output Sink	0/5	0.4	<1	5	0.44	1		0.36		0.36		
	Current	0/10	0.5	<1	10	1.1	2.6		0.9		0.9		mΑ
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I <sub>I</sub>	Input Leakage Current	0/18	Any In	put	18		±10 <sup>-5</sup>	±0.1		±1		±1	μΑ
C <sub>I</sub>	Input Capacitance		Any In	put			5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with  $V_{DD}$ =5V, 2V min. with  $V_{DD}$ =10V, 2.5V min. with  $V_{DD}$ =15V

# $\textbf{DYNAMIC ELECTRICAL CHARACTERISTICS} \; (\textbf{T}_{amb} = 25^{\circ} \textbf{C}, \;\; \textbf{C}_{L} = 50 \text{pF}, \; \textbf{R}_{L} = 200 \text{K}\Omega, \;\; \textbf{t}_{f} = \textbf{t}_{f} = 20 \; \text{ns})$

0	B	Test Condition		,	Unit		
Symbol	Parameter	V <sub>DD</sub> (V)		Min.	Тур.	Max.	
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay Time	5			110	220	
	CLOCK to OUT	10			55	110	ns
		15			45	90	
t <sub>PHL</sub> t <sub>PLH</sub>	PHL tPLH Propagation Delay Time	5			150	300	
	CLOCK or STROBE to	10			75	150	ns
	OUT	15			60	120	
t <sub>PHL</sub> t <sub>PLH</sub>		5			360	720	
	CLOCK to INHIBIT High	10			160	320	ns
	Level to Low Level	15			110	220	
t <sub>PHL</sub> t <sub>PLH</sub>	t <sub>PLH</sub> Propagation Delay Time LOW Level to HIGH Level	5			250	500	
		10			100	200	ns
		15			75	150	



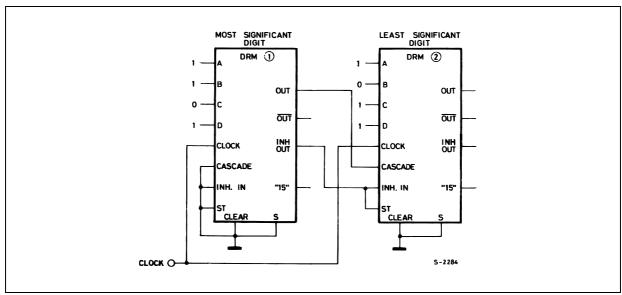
Cumbal	Danamartan	Test Condition		,	Value (*)			
Symbol	Parameter	V <sub>DD</sub> (V)		Min.	Тур.	Max.		
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay Time	5			380	760		
	CLĖAŘ to OUT	10			175	350	ns	
		15			130	260		
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay Time	5			300	600		
· · · · · · · · · · · · · · · · · · ·	CLOCK to "9" or "15" OUT	10			125	250	ns	
		15			90	180		
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay Time	5			90	180		
	CASCADE to OUT	10			45	90	ns	
		15			35	70		
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay Time	5			160	320		
	INHIBIT IN to INHIBIT	10			75	150	ns	
	OUT	15			55	110		
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay Time	5			330	660		
	SET to OUT	10			150	300	ns	
		15			110	220		
t <sub>THL</sub> t <sub>TLH</sub>	Transition Time	5			100	200		
	10			50	100	ns		
		15			40	80		
f <sub>CL</sub>	Maximum Clock	5		1.2	2.4			
	Frequency	10		2.5	5		MHz	
		15		3.5	7			
t <sub>W</sub>	Clock Pulse Width	5		330	165			
••		10		170	85		ns	
		15		100	50			
t <sub>r,</sub> t <sub>f</sub>	Clock Rise or Fall Time	5				15		
., .		10				15	μs	
		15				15		
t <sub>W</sub>	SET or CLEAR pulse	5		160	80			
	Width	10		90	45		ns	
		15		60	30			
t <sub>setup</sub>	INHIBIT Input Set-Up	5		100	50			
	Time, High Level to Low	10		40	20		ns	
	Level	15		20	10			
t <sub>R</sub>	INHIBIT Input Removal	5		240	120			
	Time	10		130	65		ns	
		15		110	55			
t <sub>R</sub>	Minimum SET Removal	5		150	75			
•	Time	10		80	40		ns	
		15		50	25			
t <sub>R</sub>	CLEAR Removal Time	5		60	30			
- *		10		40	20		ns	

(\*) Typical temperature coefficient for all V<sub>DD</sub> value is 0.3 %/°C.

#### **APPLICATION NOTES**

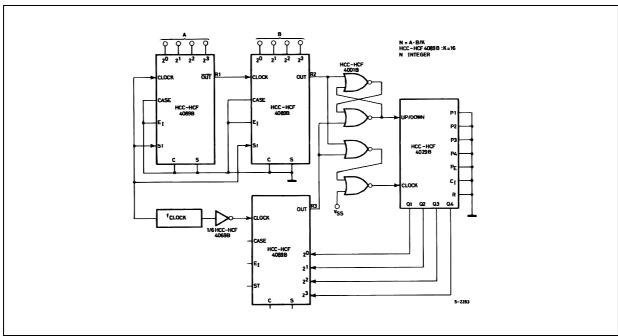
For words of more than 4 bits, HCF4089B device may be cascaded in two different modes : an ADD mode and a MULTIPLY mode.

#### TWO HCF4089B'S CASCADED IN THE "ADD" MODE WITH A PRESET NUMBER OF 189



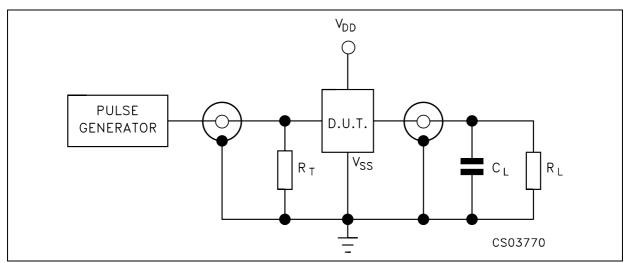
 $\frac{11}{16} + \frac{13}{256} = \frac{189}{256}$ 

# TWO HCF4089B'S CASCADED IN THE "MULTIPLY" MODE FOR MULTIPLICATION OF TWO VARIABLES A AND B WITH LOOP CIRCUIT CONTROL



When the loop stabilities rate R2 = rate R3, thus fclock( $\frac{A}{16} \bullet \frac{B}{16}$ ) = fclock ( $\frac{1}{16} \bullet \frac{N}{16}$ ) therefore N = AB

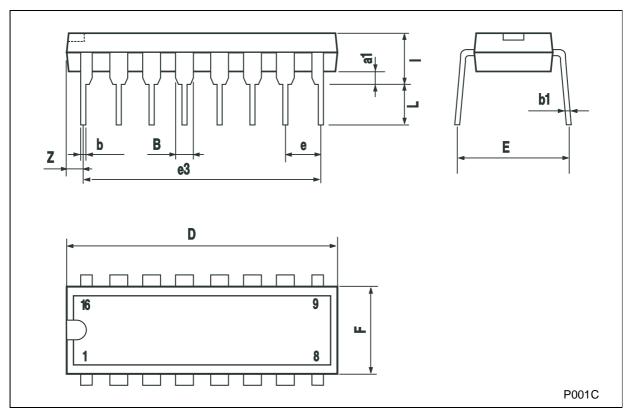
#### **TEST CIRCUIT**



 $C_L$  = 50pF or equivalent (includes jig and probe capacitance)  $R_L$  = 200K $\Omega$   $R_T$  =  $Z_{OUT}$  of pulse generator (typically 50 $\Omega$ )

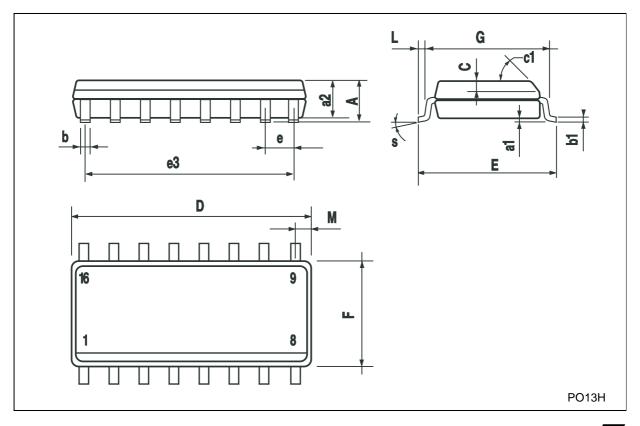
# Plastic DIP-16 (0.25) MECHANICAL DATA

DIM		mm.				
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
В	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
е		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



# **SO-16 MECHANICAL DATA**

DIM		mm.			inch	
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
А			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
С		0.5			0.019	
c1			45°	(typ.)		
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
е		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
М			0.62			0.024
S			8° (	max.)		•



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© http://www.st.com



This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.