intersil™

CD4043BMS, CD4044BMS

CMOS Quad 3 State R/S Latches

Features

- **High Voltage Types (20V Rating)**
- **Quad NOR R/S Latch- CD4043BMS**
- **Quad NAND R/S Latch - CD4044BMS**
- **3 State Outputs with Common Output ENABLE**
- **Separate SET and RESET Inputs for Each Latch**
- **NOR and NAND Configuration**
- **5V, 10V and 15V Parametric Ratings**
- **Standardized Symmetrical Output Characteristics**
- **100% Tested for Quiescent Current at 20V**
- **Maximum Input Current of $1\mu a$ at 18V Over Full Package-Temperature Range;**
  - **100nA at 18V and 25°C**
- **Noise Margin (Over Full Package Temperature Range):**
  - **1V at VDD = 5V**
  - **2V at VDD = 10V**
  - **2.5V at VDD = 15V**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications

- **Holding Register in Multi-Register System**
- **Four Bits of Independent Storage with Output ENABLE**
- **Strobed Register**
- **General Digital Logic**
- **CD4043BMS for Positive Logic Systems**
- **CD4044BMS for Negative Logic Systems**

Description

CD4043BMS types are quad cross-coupled 3-state CMOS NOR latches and the CD4044BMS types are quad cross-coupled 3-state CMOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or high on the ENABLE input connects the latch states to the Q outputs. A logic "0" or low on the ENABLE input disconnects the latch states from the Q outputs, results in an open circuit feature allows common busing of the outputs.
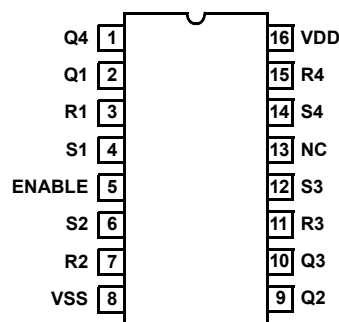
The CD4043BMS and CD4044BMS are supplied in these 16-lead outline packages:

Braze Seal DIP	*H4T	†H4T
Frit Seal DIP	*H1C	†HIE
Ceramic Flatpack	*H3X	†H6W
*CD4043B Only	†CD4044B Only	

Pinout

CD4043BMS
TOP VIEW

Pin			Pin
Q4	1	16	VDD
Q1	2	15	R4
R1	3	14	S4
S1	4	13	NC
ENABLE	5	12	S3
S2	6	11	R3
R2	7	10	Q3
VSS	8	9	Q2

NC = NO CONNECTION

CD4044BMS
TOP VIEW

Pin			Pin
Q4	1	16	VDD
NC	2	15	S4
S1	3	14	R4
R1	4	13	Q1
ENABLE	5	12	R3
R2	6	11	S3
S2	7	10	Q3
VSS	8	9	Q2
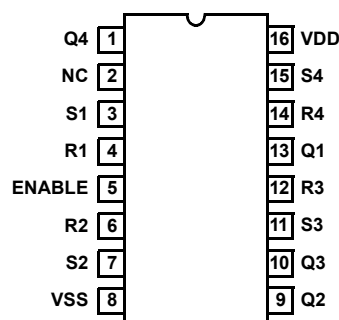
NC = NO CONNECTION

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . -0.5V to +20V
  (Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . .-0.5V to VDD +0.5V
DC Input Current, Any One Input . . . .±10mA
Operating Temperature Range. . . . . -55°C to +125°C
  Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . +265°C
  At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for
  10s Maximum

Reliability Information

	θ_{ja}	θ_{jc}
Thermal Resistance . . . .
  Ceramic DIP and FRIT Package . . . . .   80°C/W   20°C/W
  Flatpack Package . . . .   70°C/W   20°C/W
Maximum Package Power Dissipation (PD) at +125°C
  For TA = -55°C to +100°C (Package Type D, F, K) 500mW
  For TA = +100°C to +125°C (Package Type D, F, K) . . . . .Derate
                   Linearity at 12mW/^{o}C to 200mW
Device Dissipation per Output Transistor 100mW
  For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	μA
				2	+125°C	-	200	μA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	μA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10μA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	μA
				2	+125°C	-12	-	μA
			VDD = 18V	3	-55°C	-0.4	-	μA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	μA
				2	+125°C	-	12	μA
			VDD = 18V	3	-55°C	-	0.4	μA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Set or Reset to Q	TPHL TPLH	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Propagation Delay 3 - State Enable to Q	TPHZ TPZH	VDD = 5V, VIN = VDD or GND (Notes 2, 3)	9	+25°C	-	230	ns
			10, 11	+125°C, -55°C	-	311	ns
Propagation Delay 3 - State Enable to Q	TPLZ TPZL	VDD = 5V, VIN = VDD or GND (Notes 2, 3)	9	+25°C	-	180	ns
			10, 11	+125°C, -55°C	-	243	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

1. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Set or Reset to Q	TPLH TPHL	VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Propagation Delay 3 State Enable to Q	TPHZ TPZH	VDD = 10V	1, 2, 4	+25°C	-	110	ns
		VDD = 15V	1, 2, 4	+25°C	-	80	ns
Propagation Delay 3 State Enable to Q	TPLZ TPZL	VDD = 10V	1, 2, 4	+25°C	-	100	ns
		VDD = 15V	1, 2, 4	+25°C	-	70	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Set or Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	160	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.

2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.

3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10μA	1, 4	+25°C	-	$\pm$1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	$\pm$1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.   3. See Table 2 for +25°C limit.

2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.   4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR 50kHz	OSCILLATOR 25kHz
PART NUMBER CD4043BMS						
Static Burn-In 1 Note 1	1, 2, 9, 10, 13	3 - 8, 11, 12, 14, 15	16			
Static Burn-In 2 Note 1	1, 2, 9, 10, 13	8	3 - 7, 11, 12, 14 - 16			
Dynamic Burn-In Note 1	13	8	5, 16	1, 2, 9, 12	4, 6, 12, 14	3, 7, 11, 15
Irradiation Note 2	1, 2, 9, 10, 13	8	3 - 7, 11, 12, 14 - 16			
PART NUMBER CD4044BMS						
Static Burn-In 1 Note 1	1, 2, 9, 10, 13	3 - 8, 11, 12, 14, 15	16			
Static Burn-In 2 Note 1	1, 2, 9, 10, 13	8	3 - 7, 11, 12, 14 - 16			
Dynamic Burn-In Note 1	2	8	5, 16	1, 9, 10, 13	4, 6, 12, 14	3, 7, 11, 15
Irradiation Note 2	1, 2, 9, 10, 13	8	3 - 7, 11, 12, 14 - 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V

2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Functional Diagram
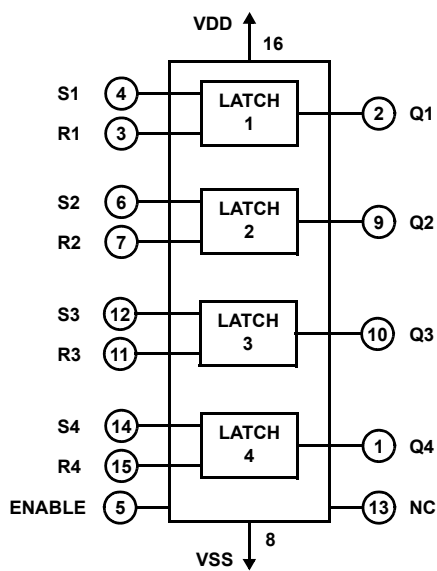
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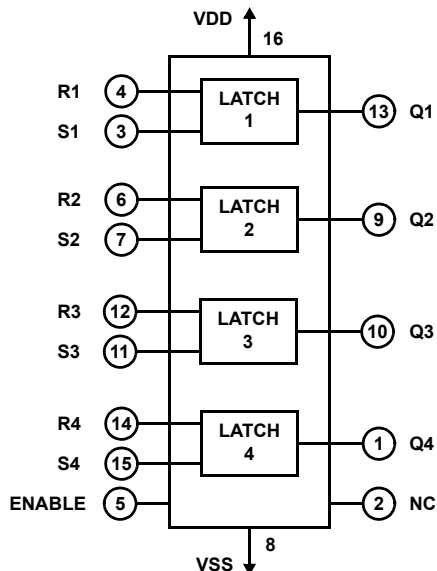
CD4044BMS

Logic Diagram
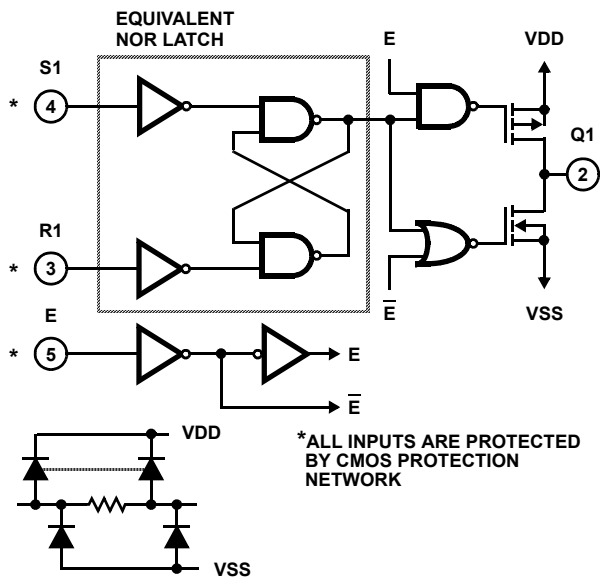
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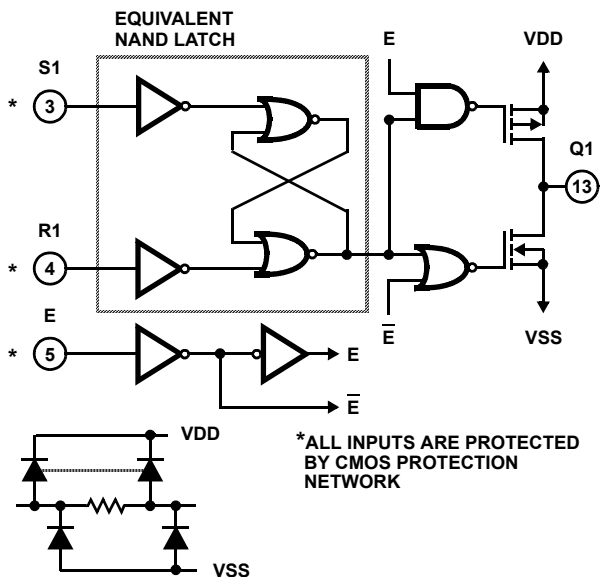
CD4044BMS

TRUTH TABLE

CD4043BMS

S	R	E	Q
X	X	O	OC*
O	O	1	NC**
1	O	1	1
O	1	1	O
1	1	1	Δ

* Open Circuit

** No Change

Δ Dominated by S = 1 input

CD4044BMS

S	R	E	Q
X	X	O	OC*
1	1	1	NC**
O	1	1	1
1	O	1	O
O	O	1	ΔΔ

* Open Circuit

** No Change

ΔΔ Dominated by R = O input

Typical Performance Characteristics
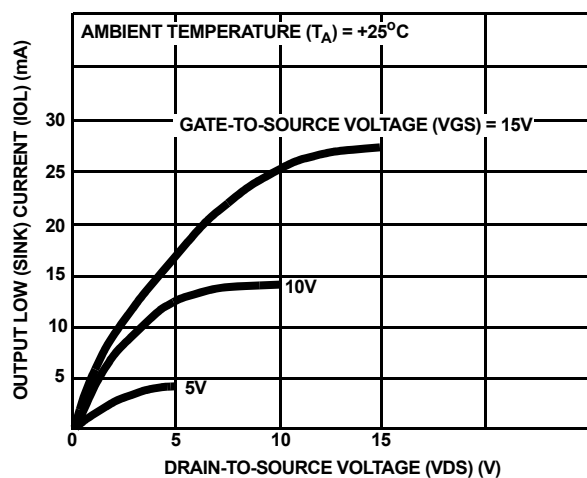
FIGURE 1. TYPICAL OUTPUT LOW (SINK) CURRENT
CHARACTERISTICS
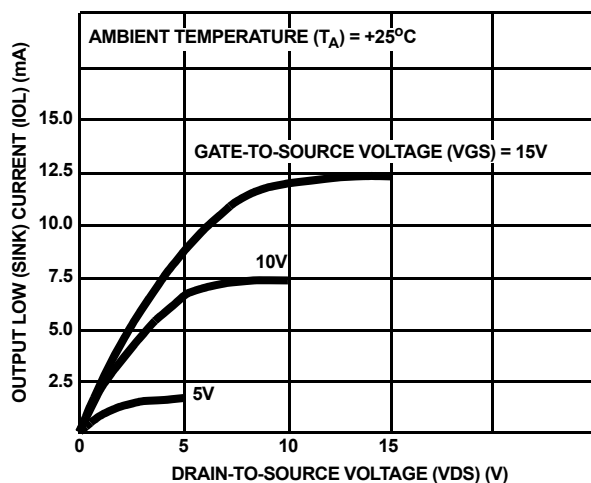
FIGURE 2. MINIMUM OUTPUT LOW (SINK) CURRENT
CHARACTERISTICS
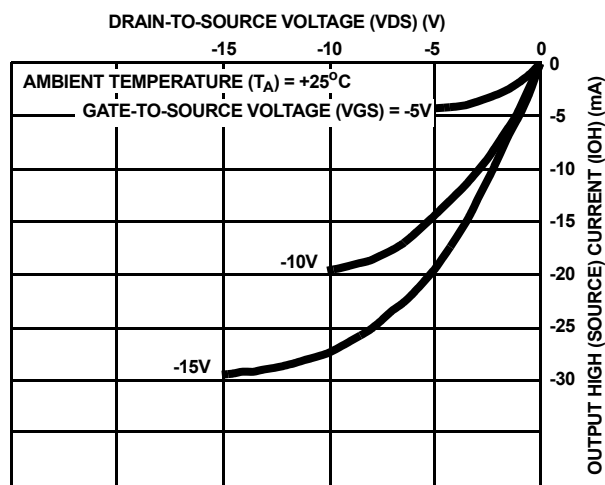
FIGURE 3. TYPICAL OUTPUT HIGH (SOURCE) CURRENT
CHARACTERISTICS
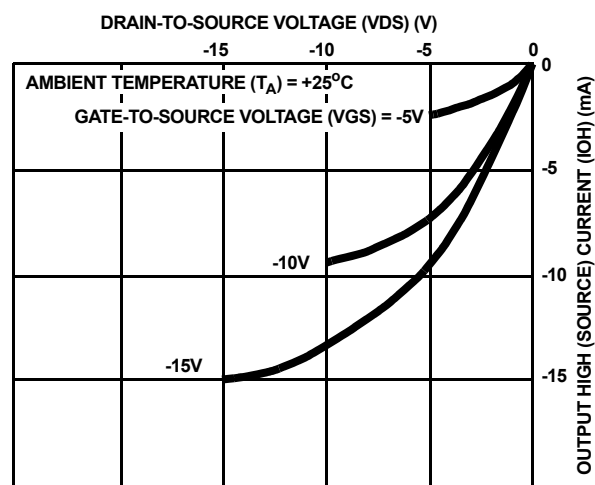
FIGURE 4. MINIMUM OUTPUT HIGH (SOURCE) CURRENT
CHARACTERISTICS
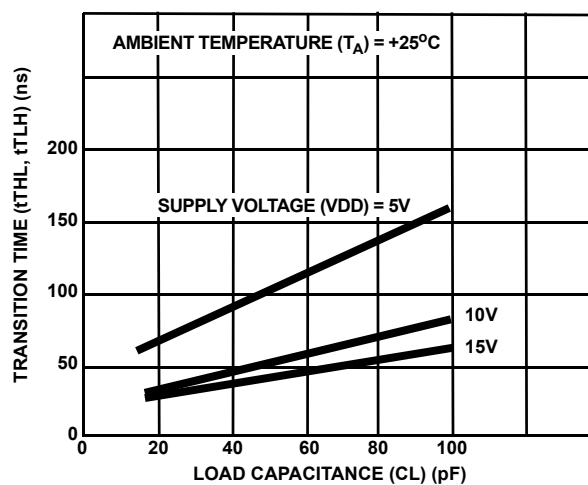
FIGURE 5. TYPICAL TRANSITION TIME AS A FUNCTION OF
LOAD CAPACITANCE
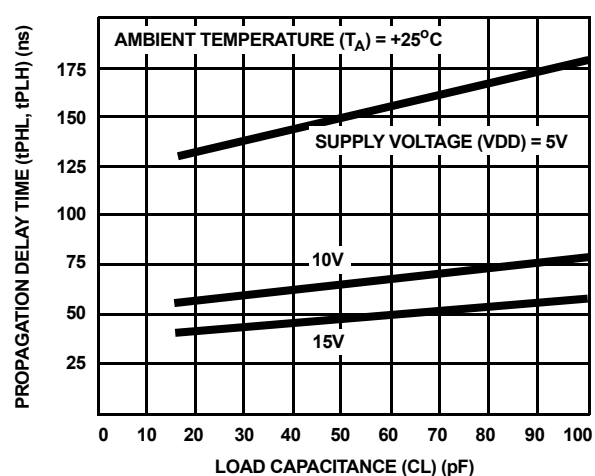
FIGURE 6. TYPICAL PROPAGATION DELAY TIME vs LOAD
CAPACITANCE - SET, RESET, to Q, $\overline{Q}$

Typical Performance Characteristics (Continued)
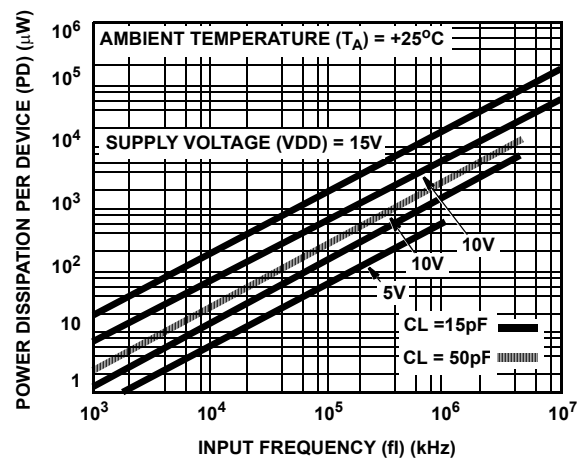
FIGURE 7. TYPICAL POWER DISSIPATION vs FREQUENCY

CD4044BMS   CD4043BMS
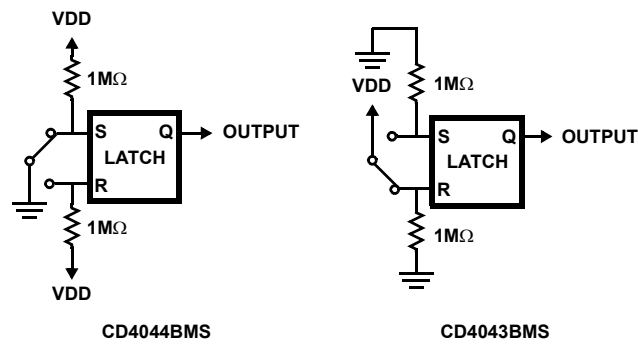
FIGURE 8. SWITCH BOUNCE ELIMINATOR

TEST	IN	$\overline{\text{IN}}$	A
tPHZ	VDD	VSS	VSS
tPLZ	VSS	VDD	VDD
tPZH	VDD	VSS	VSS
tPZL	VSS	VDD	VDD

Z = HIGH IMPEDANCE
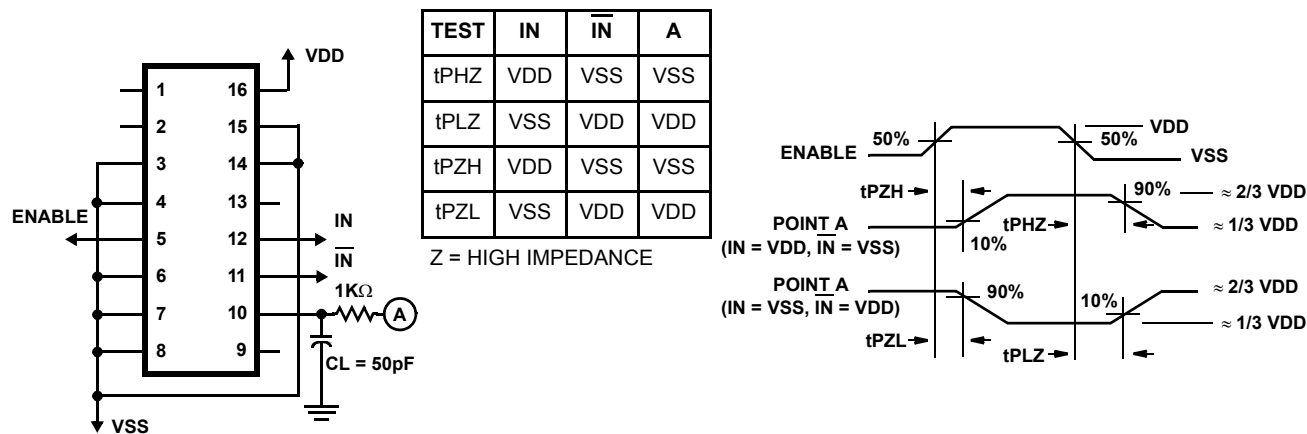
FIGURE 9. ENABLE PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORM
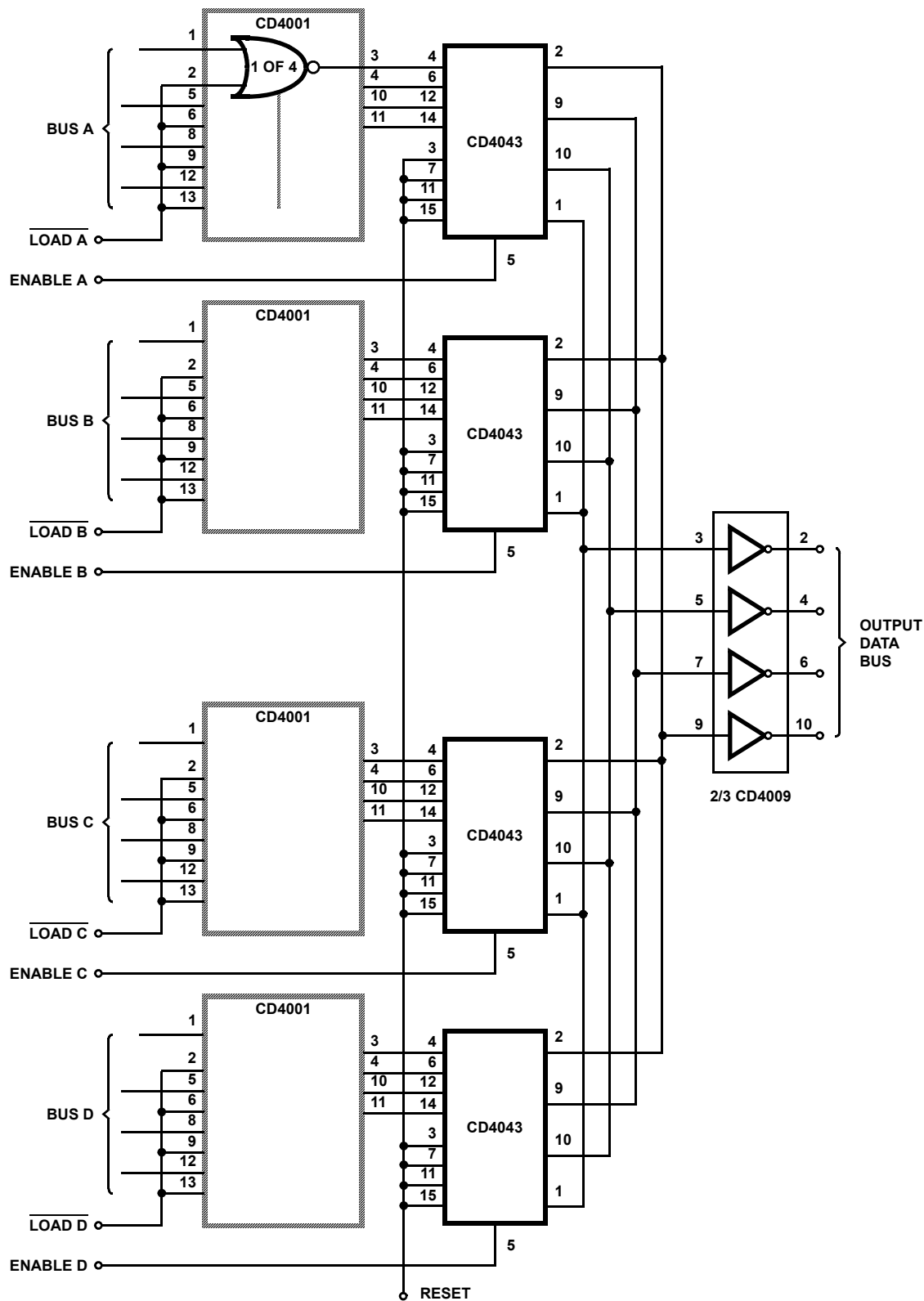
FIGURE 10. MULTIPLE BUS STORAGE

Chip Dimensions and Pad Layouts
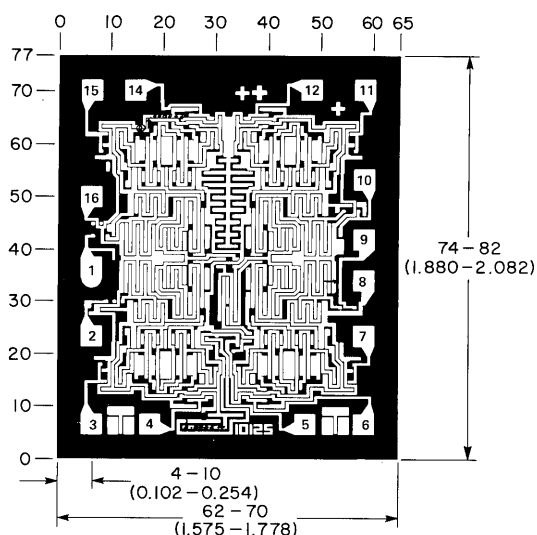
CD4043BMSH
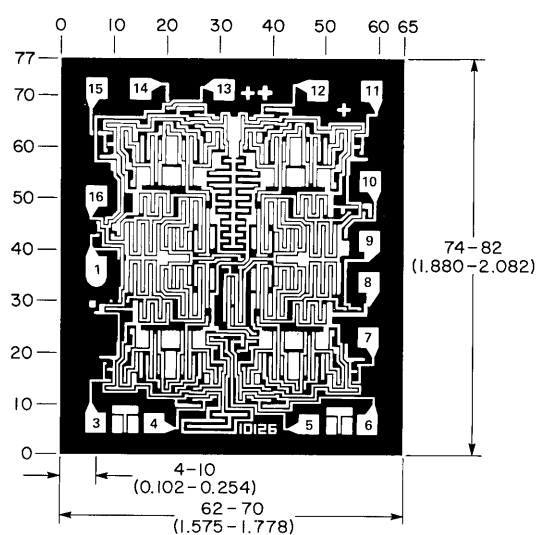
CD4044BMSH

Dimensions in parentheses are in millimeters
and are derived from the basic inch dimensions
as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches