MC14009AL
MC14009CL
MC14009CP
MC14010AL
MC14010CL
MC14010CP

HEX BUFFERS

The MC14009 hex inverter/buffer and MC14010 noninverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. Both devices can be used as current "sink" or "source" drivers, as CMOS-to-CMOS or CMOS-to-bipolar (TTL or DTL) logic level converters, or as multiplexers (1-to-6). The MC14009 also provides the invert function.

- Quiescent Power Dissipation = 50 nW/package typical
- High Current Sinking Capability
  8.0 mA minimum @ V_{OL} = 0.5 V and V_{DD} = 10 V
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14009/10 AL)
  3.0 Vdc to 16 Vdc (MC14009/10CL/CP)
- Wide CMOS-to-Bipolar Conversion Range –
  From MCMOS operating with specified supply voltage range to TTL or DTL operating with +3.0 V to +6.0 V supply. Conversion with logic output levels > 6.0 V is permitted if $V_{CC} \leq V_{DD}$.
- Pin for Pin Replacement for CD4009A – MC14009
  CD4010A – MC14010

McMOS

(LOW-POWER COMPLEMENTARY MOS)

HEX BUFFERS

Inverting – MC14009AL/CL/CP
Noninverting – MC14010AL/CL/CP

L SUFFIX
CERAMIC PACKAGE
CASE 620

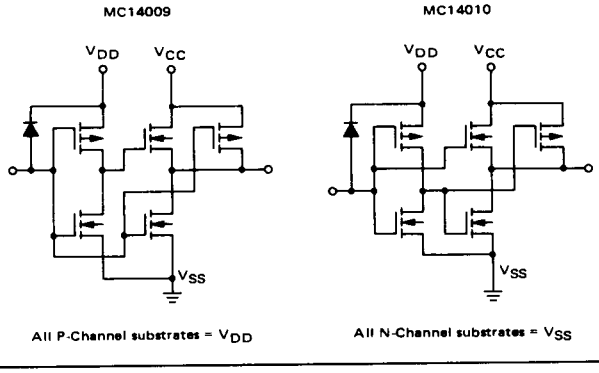
P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

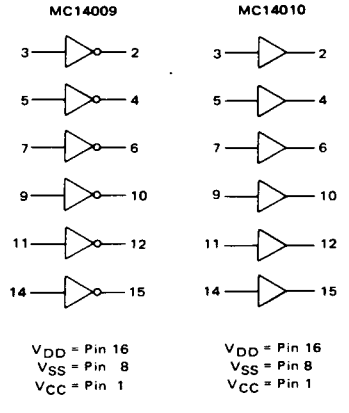
Rating	Symbol	Value	Unit
DC Supply Voltage ($V_{CC} \leq V_{DD}$) –AL Version	V_{DD}	+18 to –0.5	Vdc
CL,CP Version		+16 to –0.5	
Input Voltage, All Inputs	V_{in}	V_{DD} to –0.5	Vdc
DC Current Drain per Pin*	I	10	mAdc
Operating Temperature Range –AL Version	T_A	–55 to +125	°C
CL,CP Version		–40 to +85	
Storage Temperature Range	T_{stg}	–65 to +150	°C

*Buffered Outputs may supply higher current.

CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



LOGIC DIAGRAMS



See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	V_{CC} Vdc	MC14009/10AL							MC14009/10CL/CP							Unit
					-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
					Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage	1,2,3	V_{out}																	Vdc
MC14009																			
(V_{in} = 5.0 Vdc)			5.0	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
(V_{in} = 10 Vdc)			10	10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
(V_{in} = 15 Vdc)			15	–	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
MC14010 "0" Level																			
(V_{in} = 0 Vdc)			5.0	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
(V_{in} = 0 Vdc)			10	10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
(V_{in} = 0 Vdc)			15	–	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
MC14009																			Vdc
(V_{in} = 0 Vdc)			5.0	5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
(V_{in} = 0 Vdc)			10	10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
(V_{in} = 0 Vdc)			15	–	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
MC14010 "1" Level																			
(V_{in} = 5.0 Vdc)			5.0	5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
(V_{in} = 10 Vdc)			10	10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
(V_{in} = 15 Vdc)			15	–	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																	Vdc
MC14009																			
(V_{out} ≥3.5 Vdc)			5.0	5.0	1.0	–	1.0	2.0	–	0.9	–	1.0	–	1.0	2.0	–	0.9	–	
(V_{out} ≥7.0 Vdc)			10	10	2.0	–	2.0	3.0	–	1.2	–	2.0	–	2.0	3.0	–	1.9	–	
(V_{out} ≥10.5 Vdc)			15	15	–	–	–	4.5	–	–	–	–	–	–	4.5	–	–	–	
(V_{out} ≤1.5 Vdc)		V_{NH}	5.0	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} ≤3.0 Vdc)			10	10	2.9	–	3.0	4.5	–	3.0	–	2.9	–	3.0	4.5	–	3.0	–	
(V_{out} ≤4.5 Vdc)			15	15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
MC14010		V_{NL}																	Vdc
(V_{out} ≤1.5 Vdc)			5.0	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
(V_{out} ≤3.0 Vdc)			10	10	3.0	–	3.0	4.5	–	2.9	–	3.0	–	3.0	4.5	–	2.9	–	
(V_{out} ≤4.5 Vdc)			15	15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
(V_{out} ≥3.5 Vdc)		V_{NH}	5.0	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} ≥7.0 Vdc)			10	10	2.9	–	3.0	4.5	–	3.0	–	2.9	–	3.0	4.5	–	3.0	–	
(V_{out} ≥10.5 Vdc)			15	15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																			
	5	I_{OH}																	mAdc
(V_{OH} = 2.5 Vdc) Source			5.0	5.0	-1.85	–	-1.25	-1.75	–	-0.9	–	-1.5	–	-1.25	-1.75	–	-1.0	–	
(V_{OH} = 9.5 Vdc)			10	10	-0.9	–	-0.6	-0.8	–	-0.4	–	-0.72	–	-0.6	-0.8	–	-0.48	–	
(V_{OH} = 13.5 Vdc)			15	15	–	–	–	-5.0	–	–	–	–	–	–	-5.0	–	–	–	
	6	I_{OL}																	mAdc
(V_{OL} = 0.4 Vdc) Sink			5.0	5.0	3.75	–	3.0	4.0	–	2.1	–	3.6	–	3.0	4.0	–	2.4	–	
(V_{OL} = 0.5 Vdc)			10	10	10	–	8.0	10	–	5.6	–	9.6	–	8.0	10	–	6.4	–	
(V_{OL} = 1.5 Vdc)			15	15	–	–	–	35	–	–	–	–	–	–	35	–	–	–	
Input Current	–	I_{in}	–	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance MC14009	–	C_{in}	–	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pF
(V_{in} = 0) MC14010			–	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	
Quiescent Dissipation	7	P_D	5.0	–	–	1.5	–	0.05	1.5	–	100	–	15	–	0.15	15	–	210	μW
			10	–	–	5.0	–	0.1	5.0	–	300	–	50	–	0.5	50	–	700	
			15	–	–	–	–	0.15	–	–	–	–	–	–	0.85	–	–	–	
Turn-On Delay Time**	4	t_{PHL}																	ns
(C_L = 15 pF)																			
MC14009																			
t_{PHL} = (0.16 ns/pF) C_L + 12 ns			5.0	5.0	–	–	–	15	55	–	–	–	–	–	15	70	–	–	
t_{PHL} = (0.10 ns/pF) C_L + 8.0 ns			10	10	–	–	–	9.0	30	–	–	–	–	–	9.0	40	–	–	
t_{PHL} = (0.08 ns/pF) C_L + 6.0 ns			15	15	–	–	–	7.0	–	–	–	–	–	–	7.0	–	–	–	
t_{PHL} = (0.05 ns/pF) C_L + 7.0 ns			10	5.0	–	–	–	8.0	25	–	–	–	–	–	8.0	35	–	–	
t_{PHL} = (0.03 ns/pF) C_L + 5.0 ns			15	5.0	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	
MC14010																			
t_{PHL} = (0.38 ns/pF) C_L + 19 ns			5.0	5.0	–	–	–	25	55	–	–	–	–	–	25	70	–	–	
t_{PHL} = (0.08 ns/pF) C_L + 19 ns			10	10	–	–	–	20	30	–	–	–	–	–	20	40	–	–	
t_{PHL} = (0.06 ns/pF) C_L + 14 ns			15	15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
t_{PHL} = (0.08 ns/pF) C_L + 14 ns			10	5.0	–	–	–	15	25	–	–	–	–	–	15	35	–	–	
t_{PHL} = (0.09 ns/pF) C_L + 9.0 ns			15	5.0	–	–	–	10	–	–	–	–	–	–	10	–	–	–	
Turn-Off Delay Time**	4	t_{PLH}																	ns
(C_L = 15 pF)																			
MC14009/10																			
t_{PLH} = (1.0 ns/pF) C_L + 35 ns			5.0	5.0	–	–	–	50	80	–	–	–	–	–	50	100	–	–	
t_{PLH} = (0.40 ns/pF) C_L + 19 ns			10	10	–	–	–	25	55	–	–	–	–	–	25	70	–	–	
t_{PLH} = (0.34 ns/pF) C_L + 15 ns			15	15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
t_{PLH} = (0.36 ns/pF) C_L + 20 ns			10	5.0	–	–	–	25	30	–	–	–	–	–	25	40	–	–	
t_{PLH} = (0.16 ns/pF) C_L + 18 ns			15	5.0	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
Output Rise Time**	4	t_r																	ns
(C_L = 15 pF)																			
MC14009																			
t_r = (2.4 ns/pF) C_L + 44 ns			5.0	5.0	–	–	–	80	125	–	–	–	–	–	80	160	–	–	
t_r = (1.0 ns/pF) C_L + 20 ns			10	10	–	–	–	35	100	–	–	–	–	–	35	120	–	–	
t_r = (0.62 ns/pF) C_L + 20 ns			15	15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
MC14010																			
t_r = (1.6 ns/pF) C_L + 56 ns			5.0	5.0	–	–	–	80	125	–	–	–	–	–	80	160	–	–	
t_r = (0.76 ns/pF) C_L + 39 ns			10	10	–	–	–	50	100	–	–	–	–	–	50	120	–	–	
t_r = (0.6 ns/pF) C_L + 21 ns			15	15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
Output Fall Time **	4	t_f																	ns
(C_L = 15 pF)																			
MC14009																			
t_f = (0.22 ns/pF) C_L + 9.0 ns			5.0	5.0	–	–	–	13	45	–	–	–	–	–	13	60	–	–	
t_f = (0.10 ns/pF) C_L + 7.0 ns			10	10	–	–	–	9.0	40	–	–	–	–	–	9.0	50	–	–	
t_f = (0.07 ns/pF) C_L + 6.0 ns			15	15	–	–	–	7.0	–	–	–	–	–	–	7.0	–	–	–	
MC14010																			
t_f = (0.20 ns/pF) C_L + 22 ns			5.0	5.0	–	–	–	25	45	–	–	–	–	–	25	60	–	–	
t_f = (0.07 ns/pF) C_L + 15 ns			10	10	–	–	–	16	40	–	–	–	–	–	16	50	–	–	
t_f = (0.07 ns/pF) C_L + 9.0 ns			15	15	–	–	–	10	–	–	–	–	–	–	10	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change, from an ideal "1" or "0" input level before producing an output state change.
**The formula given is for the typical characteristics only.

FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

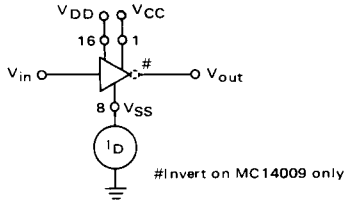


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS versus TEMPERATURE

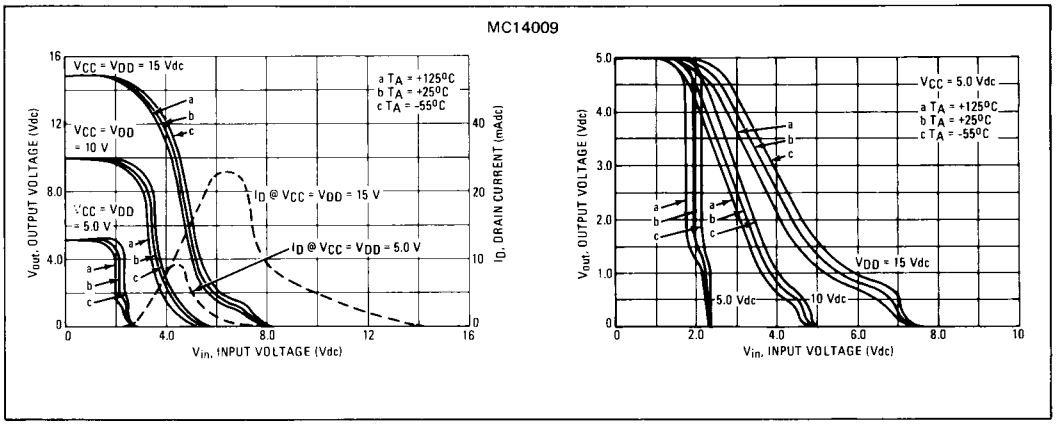


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

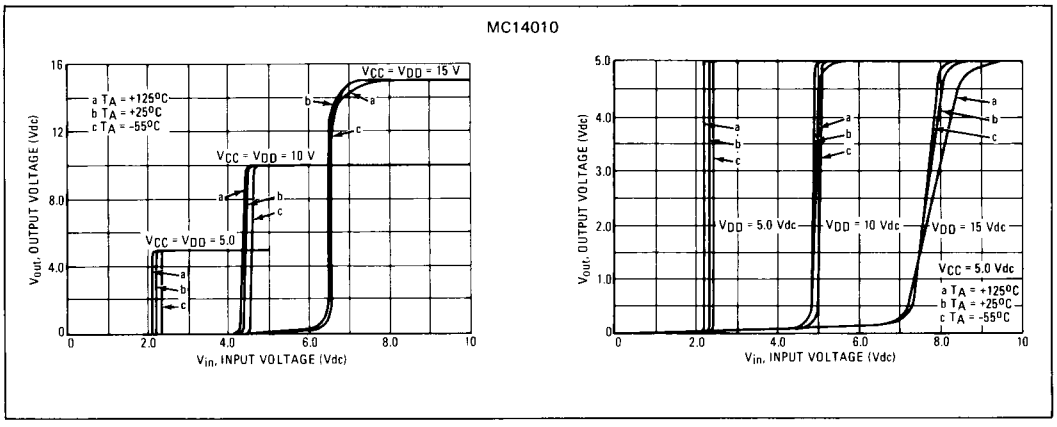


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

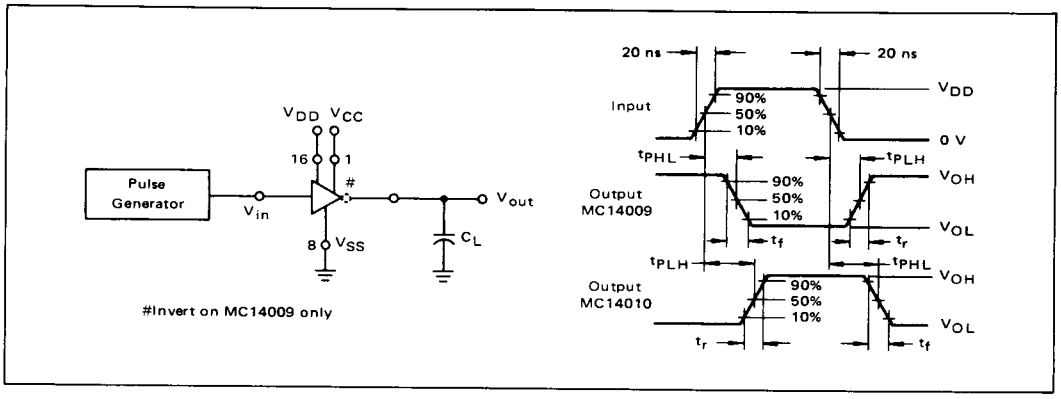
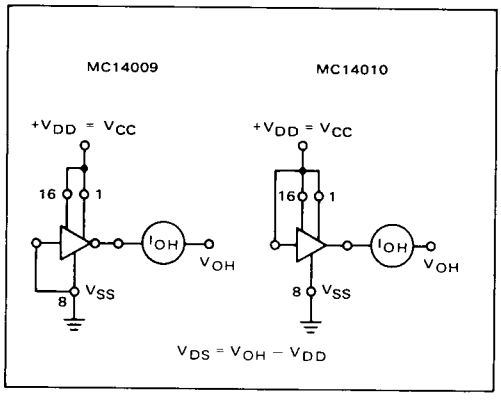


FIGURE 5 – TYPICAL OUTPUT SOURCE CHARACTERISTICS



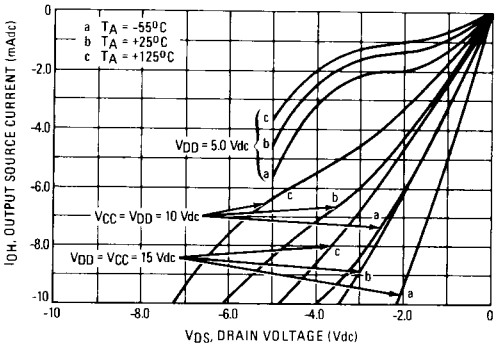
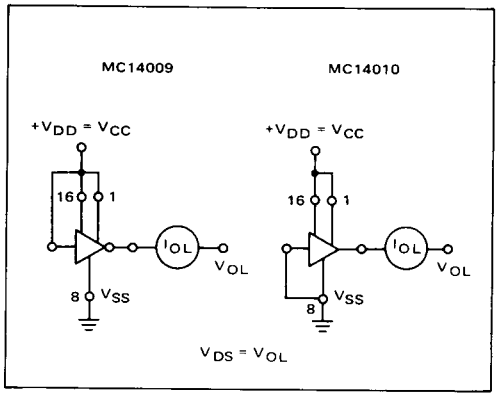


FIGURE 6 – TYPICAL OUTPUT SINK CHARACTERISTICS



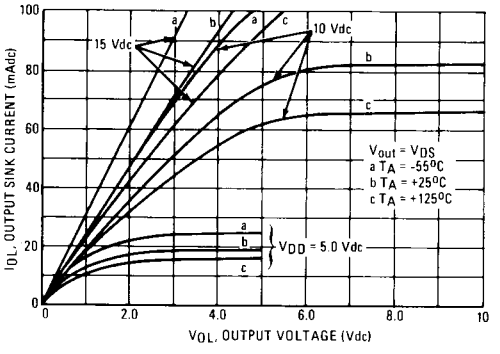


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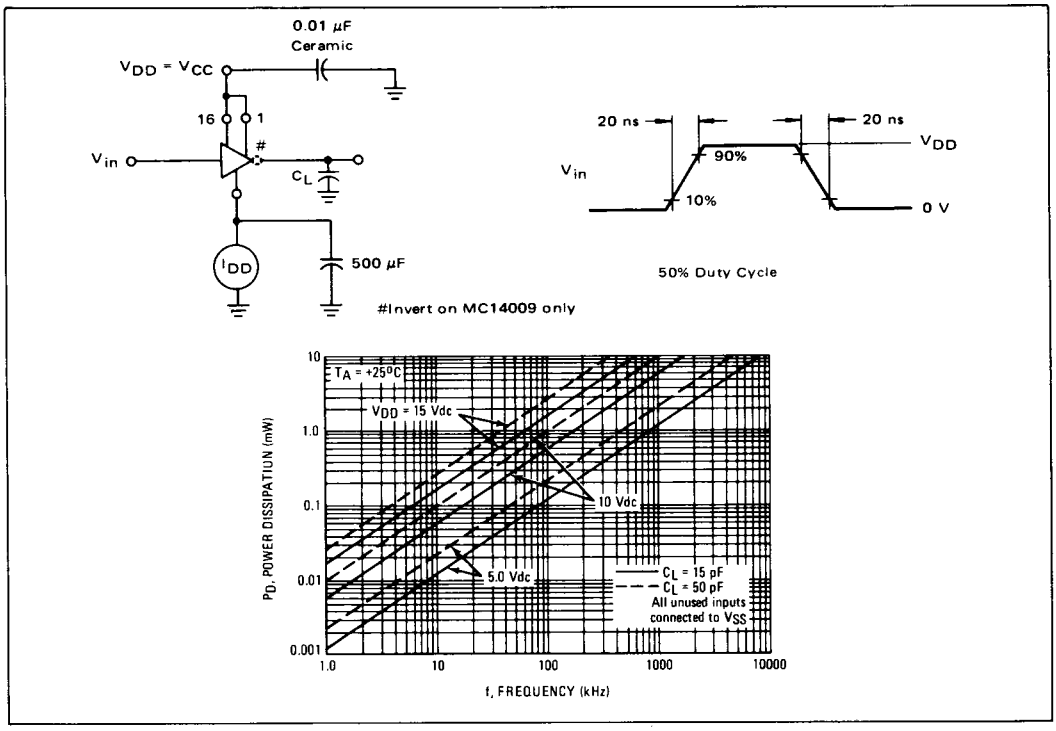
FIGURE 7 – TYPICAL DYNAMIC POWER DISSIPATION CHARACTERISTICS



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})