74LVC1G07 Buffer with open-drain output Rev. 13 — 11 May 2017

Product data sheet

General description

The 74LVC1G07 provides the non-inverting buffer.

The output of this device is an open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- · Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- -24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G07GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74LVC1G07GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74LVC1G07GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm	SOT886
74LVC1G07GF	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm	SOT891
74LVC1G07GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 x 1.0 x 0.35 mm	SOT1115
74LVC1G07GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 x 1.0 x 0.35 mm	SOT1202
74LVC1G07GX	-40 °C to +125 °C	X2SON5	plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 x 0.8 x 0.35 mm	SOT1226

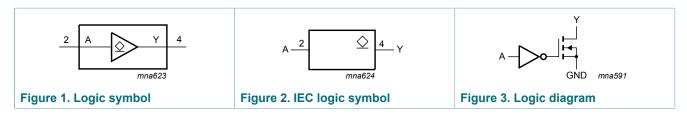
4 Marking

Table 2. Marking

Type number	Marking code ^[1]
74LVC1G07GW	VS
74LVC1G07GV	V07
74LVC1G07GM	VS
74LVC1G07GF	VS
74LVC1G07GN	VS
74LVC1G07GS	VS
74LVC1G07GX	VS

^[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5 Functional diagram



74LVC1G07

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6 Pinning information

6.1 Pinning





6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description		
	TSSOP5, SC-74A and X2SON5	XSON6		
n.c.	1	1	not connected	
Α	2	2	data input	
GND	3	3	ground (0 V)	
Υ	4	4	data output	
n.c.	-	5	not connected	
V _{CC}	5	6	supply voltage	

Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input A	Output Y
L	L
Н	Z

Limiting values 8

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V		-50	-	mA
VI	input voltage		[1]	-0.5	+6.5	V
I _{OK}	output clamping current	V _O < 0 V		-50	-	mA
V _O	output voltage	Active mode	[1]	-0.5	+6.5	V
		Power-down mode	[1] [2]	-0.5	+6.5	V
Io	output current	V _O = 0 V to 6.5 V		-	50	mA
I _{CC}	supply current			-	100	mA
I _{GND}	ground current			-100	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[3]	-	250	mW

The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		1.65	-	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage	Active mode	0	-	5.5	V
		Power-down mode; V _{CC} = 0 V	0	-	5.5	V
T _{amb}	ambient temperature		-40	-	+125	°C

74LVC1G07

When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation. For TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K. For XSON6 and X2SON5 package: above 118 $^{\circ}\text{C}$ the value of P $_{tot}$ derates linearly with 7.8 mW/K.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Δt/ΔV	input transition rise and	V _{CC} = 1.65 V to 2.7 V	-	-	20	ns/V
	fall rate	V _{CC} = 2.7 V to 5.5 V	-	-	10	ns/V

10 Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to	Unit	
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level	V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	0.65V _{CC}	-	V
	input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	0.7V _{CC}	-	V
V _{IL}	LOW-level	V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	-	0.35V _{CC}	V
	input voltage	V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	-	0.3V _{CC}	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}						
	output voltage	I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V	-	-	0.10	-	0.10	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.70	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.30	-	0.45	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.40	-	0.60	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.80	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.55	-	0.80	V
l _l	input leakage current	$V_1 = 5.5 \text{ V or GND};$ $V_{CC} = 0 \text{ V to } 5.5 \text{ V}$ [2]	-	±0.1	±1	-	±1	μΑ
l _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	±0.1	±2	-	±2	μΑ
I _{OFF}	power-off leakage current	V_{I} or $V_{O} = 5.5 \text{ V}$; $V_{CC} = 0 \text{ V}$	-	±0.1	±2	-	±2	μΑ
I _{cc}	supply current	V _I = 5.5 V or GND; I _O = 0 A; V _{CC} = 1.65 V to 5.5 V	-	0.1	4	-	4	μΑ
Δl _{CC}	additional supply current	per pin; $V_1 = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}; ^{[2]}$ $V_{CC} = 2.3 \text{ V to } 5.5 \text{ V}$	-	5	500	-	500	μΑ
C _I	input capacitance	V_{CC} = 3.3 V; V_{I} = GND to V_{CC}	-	5.0	-	-	-	pF

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All typical values are measured at T $_{amb}$ = 25 $^{\circ}C.$ These typical values are measured at V $_{CC}$ = 3.3 V.

11 Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd} propagation delay		A to Y; see Figure 8 [2]						
		V _{CC} = 1.65 V to 1.95 V	1.0	2.6	6.7	1.0	8.4	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	1.7	5.5	0.5	7.0	ns
		V _{CC} = 2.7 V	0.5	2.3	4.7	0.5	6.0	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	2.2	4.2	0.5	5.5	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	1.6	3.5	0.5	4.5	ns
C _{PD}	power dissipation capacitance	$V_1 = GND \text{ to } V_{CC}; V_{CC} = 3.3 \text{ V}$ [3]	-	7.0	-	-	-	pF

- Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.
- t_{pd} is the same as t_{PLZ} and t_{PZL} . C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} x V_{CC}^2 x f_i x N + \sum (C_L x V_{CC}^2 x f_o)$ where:

 f_i = input frequency in MHz;

 f_0 = output frequency in MHz;

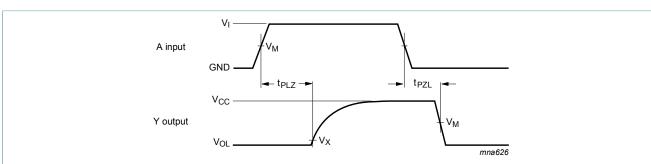
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs.}$

11.1 Waveforms and test circuit



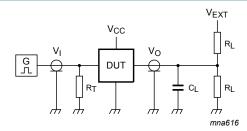
Measurement points are given in Table 9.

 V_{OL} is the typical output voltage level that occurs with the output load.

Figure 8. The input (A) to output (Y) propagation delays

Table 9. Measurement points

Supply voltage	Input	Output	
V _{CC}	V _M	V _M	V _X
1.65 V to 1.95 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.15 V
2.3 V to 2.7 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.15 V
2.7 V	1.5 V	1.5 V	V _{OL} + 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V _{OL} + 0.3 V
4.5 V to 5.5 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.3 V



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to the output impedance Z_0 of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Figure 9. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load	V _{EXT}	
V _{CC}	VI	t _r , t _f	CL	R _L	t _{PZL} , t _{PLZ}
1.65 V to 1.95 V	V _{CC}	≤ 2.0 ns	30 pF	1 kΩ	2V _{CC}
2.3 V to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	2V _{CC}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	6 V
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	2V _{CC}

12 Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm SOT353-1 = v (M) A detail X DIMENSIONS (mm are the original dimensions) D(1) E⁽¹⁾ Z⁽¹⁾ UNIT С ΗE Lp θ max. 0.30 0.25 1.35 2.25 0.46 0.1 1.0 2.25 0.60 0.15 0.65 0.425 mm 1.1

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

0.15

0.08

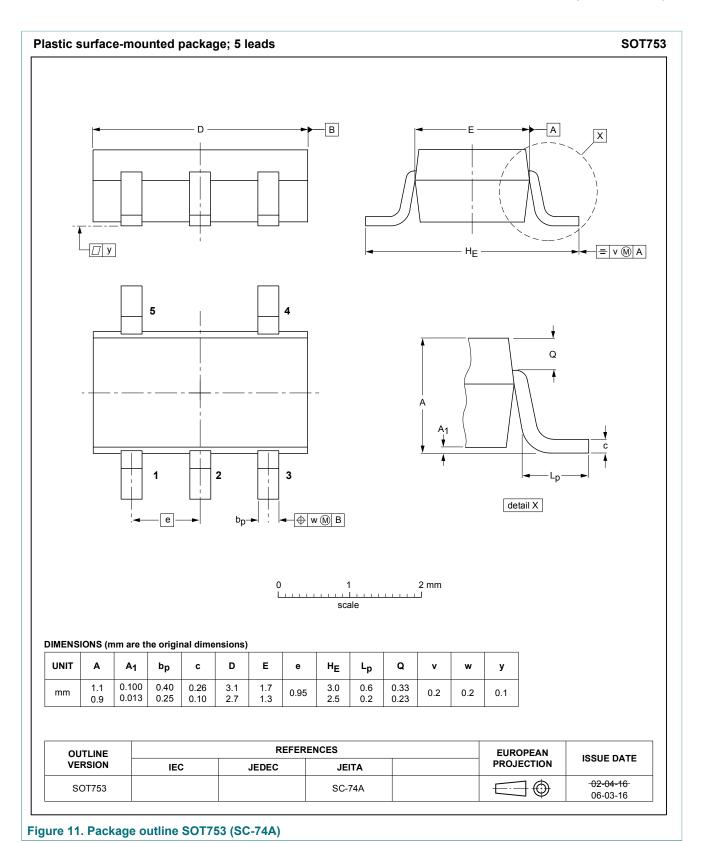
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OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	1330E DATE
SOT353-1		MO-203	SC-88A			-00-09-01 03-02-19

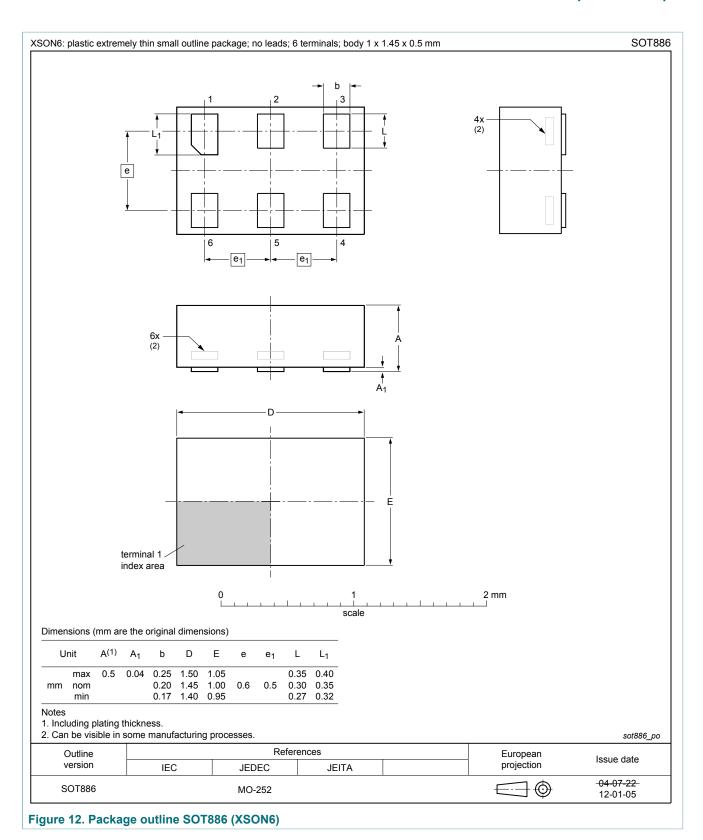
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Figure 10. Package outline SOT353-1 (TSSOP5)

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74LVC1G07



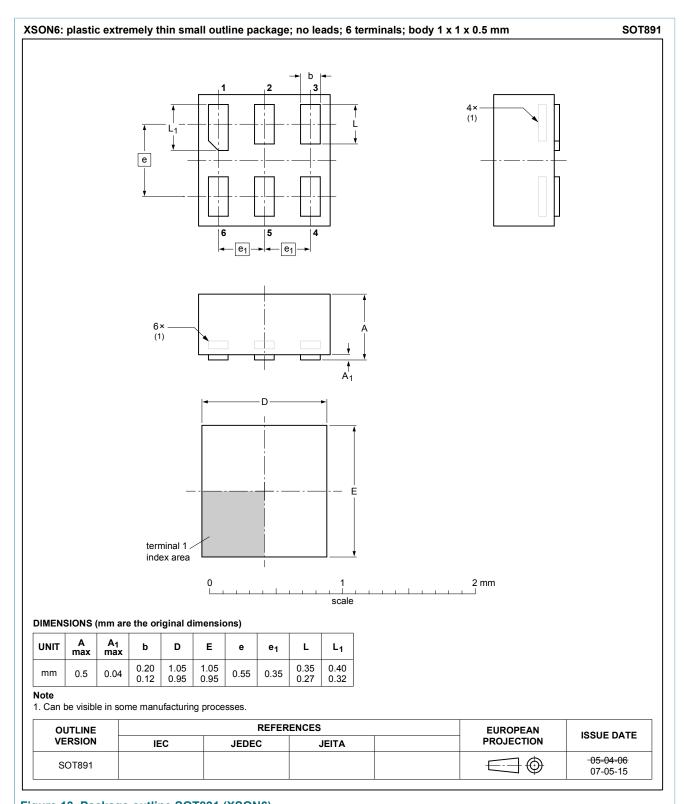


Figure 13. Package outline SOT891 (XSON6)

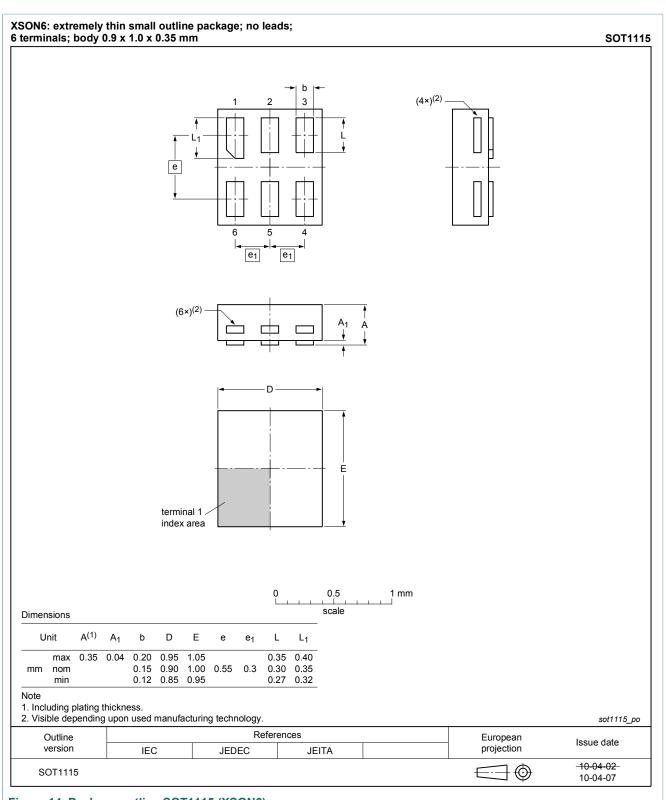
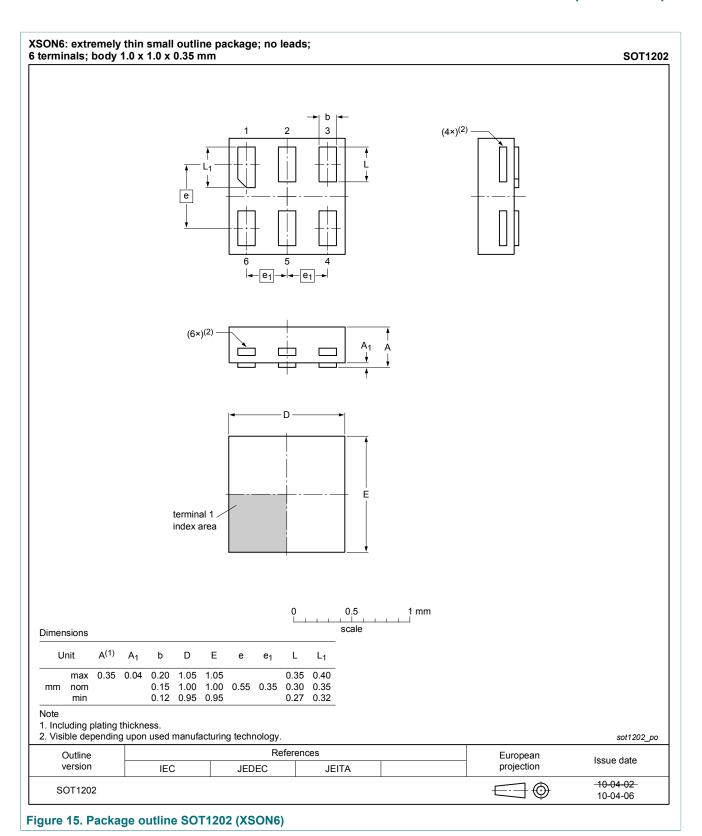
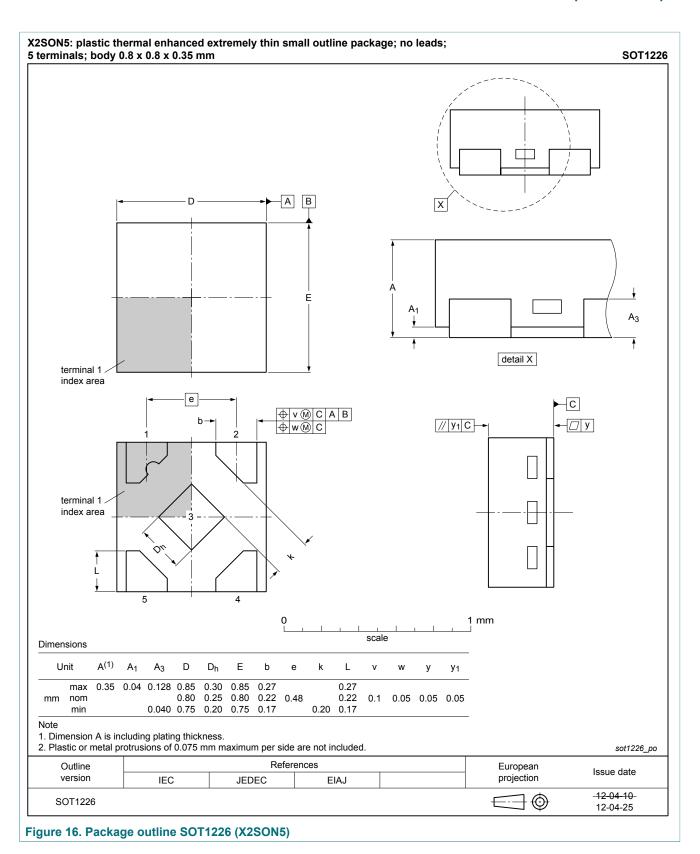


Figure 14. Package outline SOT1115 (XSON6)



74LVC1G07



13 Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74LVC1G07 v.13	20170511	Product data sheet	-	74LVC1G07 v.12	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 				
74LVC1G07 v.12	20161128	Product data sheet	-	74LVC1G07 v.11	
Modifications:	• <u>Table 7</u> : The maximum limits for leakage current and supply current have changed.				
74LVC1G07 v.11	20120629	Product data sheet	-	74LVC1G07 v.10	
Modifications:	 Added type number 74LVC1G07GX (SOT1226) Package outline drawing of SOT886 (Figure 12) modified. 				
74LVC1G07 v.10	20111207	Product data sheet	-	74LVC1G07 v.9	
Modifications:	Legal pages updated.				
74LVC1G07 v.9	20100824	Product data sheet	-	74LVC1G07 v.8	
74LVC1G07 v.8	20070717	Product data sheet	-	74LVC1G07 v.7	
74LVC1G07 v.7	20070515	Product data sheet	-	74LVC1G07 v.6	
74LVC1G07 v.6	20040907	Product specification	-	74LVC1G07 v.5	
74LVC1G07 v.5	20030307	Product specification	-	74LVC1G07 v.4	
74LVC1G07 v.4	20021002	Product specification	-	74LVC1G07 v.3	
74LVC1G07 v.3	20020528	Product specification	-	74LVC1G07 v.2	
74LVC1G07 v.2	20010406	Product specification	-	74LVC1G07 v.1	
74LVC1G07 v.1	20001122	Product specification	-	-	

15 Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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Nexperia 74LVC1G07

Buffer with open-drain output

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