4-Bit Parallel-In/Parallel-Out Shift Register

The MC14035B 4–bit shift register is constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. It consists of a 4–stage clocked serial–shift register with synchronous parallel inputs and buffered parallel outputs. The Parallel/Serial (P/S) input allows serial–right shifting of data or synchronous parallel loading via inputs Dp0 thru Dp3. The True/Complement (T/C) input determines whether the outputs display the Q or $\overline{\rm Q}$ outputs of the flip–flop stages. J–K logic forms the serial input to the first stage. With the J and K inputs connected together they operate as a serial "D" input.

This device may be effectively used for shift-right/shift-left registers, parallel-to-serial/serial-to-parallel conversion, sequence generation, up/down Johnson or ring counters, pseudo-random code generation, frequency and phase comparators, sample and hold registers, etc...

- 4-Stage Clocked Serial-Shift Operation
- Synchronous Parallel Loading of all Four Stages
- · J-K Serial Inputs on First Stage
- Asynchronous True/Complement Control of all Outputs
- · Fully Static Operation
- · Asynchronous Master Reset
- Data Transfer Occurs on the Positive-Going Clock Transition
- · No Limit on Clock Rise and Fall Times
- · All Inputs are Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	- 0.5 to + 18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
l _{in} , l _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8–Second Soldering)	260	°C

^{*} Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating:

Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

TRUTH TABLE

	Inp	t _n Output		
С	J	K	R	Q ₀
	0	0	0	0
	0	1	0	Q0 (n – 1)
	1	0	0	$\frac{Q0}{Q0} (n - 1)$
	1	1	0	1
_	Х	Х	0	Q0 (n – 1)
X	X	Х	1	0

X = Don't Care P/S = 0 = Serial Mode T/C = 1 = True Outputs

MC14035B



L SUFFIX CERAMIC CASE 620



P SUFFIX PLASTIC CASE 648



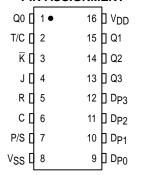
D SUFFIX SOIC CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic MC14XXXBCL Ceramic MC14XXXBD SOIC

 $T_A = -55^\circ$ to 125°C for all packages.

PIN ASSIGNMENT





ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

			V _{DD}	- 5	5°C		25°C		125	5°C	
Characteristic		Symbol	Vdc	Min	Max	Min	Тур#	Max	Min	Max	Unit
Output Voltage V _{in} = V _{DD} or 0	"0" Level	VOL	5.0 10 15	_ _ _	0.05 0.05 0.05	_ _ _	0 0 0	0.05 0.05 0.05	_ _ _	0.05 0.05 0.05	Vdc
$V_{in} = 0$ or V_{DD}	"1" Level	VOH	5.0 10 15	4.95 9.95 14.95	_ _ _	4.95 9.95 14.95	5.0 10 15	_ _ _	4.95 9.95 14.95	_ _ _	Vdc
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level	V _{IL}	5.0 10 15	_ _ _	1.5 3.0 4.0		2.25 4.50 6.75	1.5 3.0 4.0	_ _ _	1.5 3.0 4.0	Vdc
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$	"1" Level	VIH	5.0 10 15	3.5 7.0 11	_ _ _	3.5 7.0 11	2.75 5.50 8.25	_ _ _	3.5 7.0 11		Vdc
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	ЮН	5.0 5.0 10 15	- 3.0 - 0.64 - 1.6 - 4.2	_ _ _ _	- 2.4 - 0.51 - 1.3 - 3.4	- 4.2 - 0.88 - 2.25 - 8.8	 - - -	- 1.7 - 0.36 - 0.9 - 2.4	_ _ _ _	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	Sink	lOL	5.0 10 15	0.64 1.6 4.2	_ _ _	0.51 1.3 3.4	0.88 2.25 8.8	_ _ _	0.36 0.9 2.4	_ _ _	mAdc
Input Current		l _{in}	15	_	± 0.1	_	±0.00001	± 0.1	_	± 1.0	μAdc
Input Capacitance (V _{in} = 0)		C _{in}	_	_	_	_	5.0	7.5	_	_	pF
Quiescent Current (Per Package)		I _{DD}	5.0 10 15	_ _ _	5.0 10 20	_ _ _	0.005 0.010 0.015	5.0 10 20	_ _ _	150 300 600	μAdc
Total Supply Current**† (Dynamic plus Quiesce Per Package) (C _L = 50 pF on all outp buffers switching)		lΤ	5.0 10 15			$I_{T} = (2$.0 μA/kHz) f 2.0 μA/kHz) f 3.0 μA/kHz) f	+ IDD			μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μ A (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, $precautions\ must\ be\ taken\ to\ avoid\ applications\ of\ any\ voltage\ higher\ than\ maximum\ rated\ voltages\ to\ this\ high-impedance$ circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must

be left open.

^{**} The formulas given are for the typical characteristics only at 25°C.

[†]To calculate total supply current at loads other than 50 pF:

SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}, T_A = 25^{\circ}C$, See Figure 1)

Characteristic	Symbol	V _{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time T _{TLH} , T _{THL} = (1.5 ns/pF) C _L + 25 ns	tTLH, tTHL	5.0	_	100	200	ns
T_{TLH} , $T_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ T_{TLH} , $T_{THL} = (0.55 \text{ ns/pF}) C_L + 12.5 \text{ ns}$		10 15	_ _	50 40	100 80	
Propagation Delay Time, Clock or Reset to Q TPLH, TPHL = (1.75 ns/pF) CL + 223 ns TPLH, TPHL = (0.70 ns/pF) CL + 89 ns	^t PLH [,] ^t PHL	5.0 10		300 130	600 260	ns
T_{PLH} , $T_{PHL} = (0.53 \text{ ns/pF}) C_L + 67 \text{ ns}$		15	_	95	190	-
Clock Pulse Width	tWH	5.0 10 15	335 165 125	135 45 40	_ _ _	ns
Reset Pulse Width	tWH	5.0 10 15	400 175 130	80 40 35	_ _ _	ns
Reset Removal Time	^t rem	5.0 10 15	80 30 25	40 15 10	_ _ _	ns
Clock Pulse Rise and Fall Time	tTLH, tTHL	5.0 10 15		No Limit		_
Clock Pulse Frequency	f _{Cl}	5.0 10 15	_	2.5 6.0 10	1.2 2.0 3.0	MHz
J–K to Clock Setup Time	t _{su}	5.0 10 15	500 200 150	120 50 30	_ _ _	ns
Clock to J–K Hold Time	t _h	5.0 10 15	40 30 25	- 40 - 5 0	_ _ _	ns
P/S to Clock Setup Time	t _{su}	5.0 10 15	500 200 150	25 10 7.5	_ _ _	ns
Clock to P/S Hold Time	th	5.0 10 15	30 20 20	- 70 - 20 - 10	_ _ _	ns
Dp to Clock Setup Time	^t su	5.0 10 15	500 200 150	90 20 15	_ _ _	ns
Clock to Dp Hold Time	^t h	5.0 10 15	90 40 40	- 25 0 5	_ _ _	ns

^{*} The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

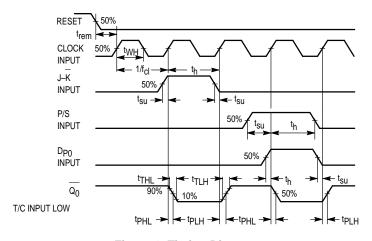
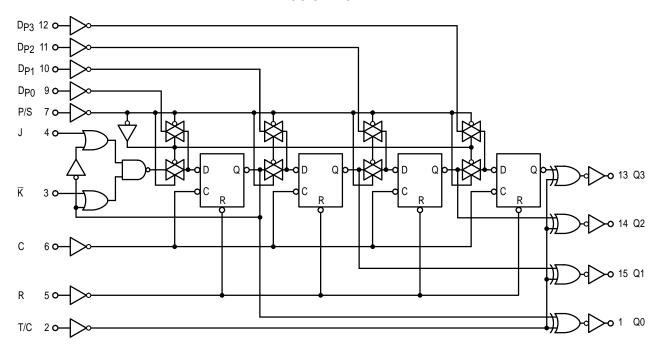
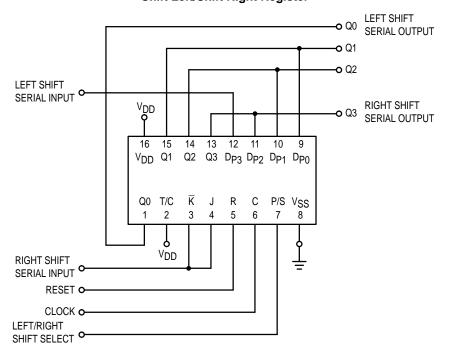


Figure 1. Timing Diagram

LOGIC DIAGRAM

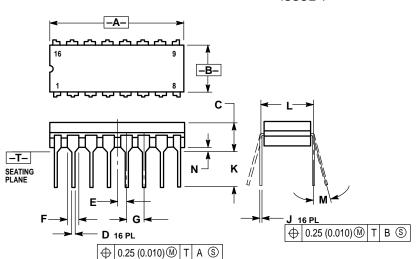


APPLICATION DIAGRAM Shift Left/Shift Right Register



OUTLINE DIMENSIONS

L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V



NOTES:

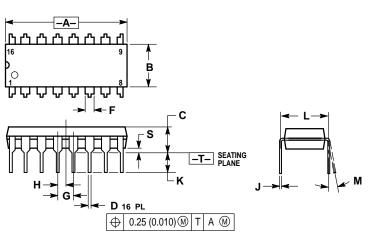
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

- ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: INCH.
 DIMENSION L TO CENTER OF LEAD WHEN
 FORMED PARALLEL.
 DIMENSION F MAY NARROW TO 0.76 (0.030)
 WHERE THE LEAD ENTERS THE CERAMIC

	INC	HES	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.750	0.785	19.05	19.93	
В	0.240	0.295	6.10	7.49	
C		0.200		5.08	
D	0.015	0.020	0.39	0.50	
Е	0.050 BSC		1.27 BSC		
F	0.055	0.065	1.40	1.65	
G	0.100	BSC	2.54 BSC		
Н	0.008	0.015	0.21	0.38	
K	0.125	0.170	3.18	4.31	
L	0.300 BSC		7.62	BSC	
M	0 °	15°	0 °	15°	
N	0.020	0.040	0.51	1.01	

P SUFFIX

PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: INCH.

 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

 5. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIMETERS				
DIM	MIN MAX		MIN	MAX			
Α	0.740	0.770	18.80	19.55			
В	0.250	0.270	6.35	6.85			
С	0.145	0.175	3.69	4.44			
D	0.015	0.021	0.39	0.53			
F	0.040	0.70	1.02	1.77			
G	0.100	BSC	2.54 BSC				
Н	0.050	BSC	1.27 BSC				
J	0.008	0.015	0.21	0.38			
K	0.110	0.130	2.80	3.30			
L	0.295	0.305	7.50	7.74			
M	0°	10°	0°	10 °			
S	0.020	0.040	0.51	1.01			

OUTLINE DIMENSIONS



- DIMENSIONING AND TOLERANCING PER ANSI
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

 MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	9.80	10.00	0.386	0.393	
В	3.80	4.00	0.150	0.157	
U	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27	BSC	0.050 BSC		
J	0.19	0.25	0.008	0.009	
K	0.10	0.25	0.004	0.009	
М	0°	7°	0°	7°	
Р	5.80	6.20	0.229	0.244	
R	0.25	0.50	0.010	0.019	

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JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298





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