# 74LVC3G06

# Triple inverter with open-drain output Rev. 12 — 15 December 2016

**Product data sheet** 

#### **General description** 1.

The 74LVC3G06 provides three inverting buffers.

The output of this device is an open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

Schmitt trigger action at all inputs makes the circuit tolerant for slower input rise and fall time.

This device is fully specified for partial power-down applications using I<sub>OFF</sub>. The I<sub>OFF</sub> circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

#### Features and benefits 2.

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - ◆ JESD8-7 (1.65 V to 1.95 V)
  - ◆ JESD8-5 (2.3 V to 2.7 V)
  - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- -24 mA output drive ( $V_{CC} = 3.0 \text{ V}$ )
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



Triple inverter with open-drain output

## 3. Ordering information

Table 1. Ordering information

Type number	Package						
	Temperature range	Name	Description	Version			
74LVC3G06DP	–40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2			
74LVC3G06DC	–40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1			
74LVC3G06GT	–40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 $\times$ 1.95 $\times$ 0.5 mm	SOT833-1			
74LVC3G06GF	–40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.5 mm	SOT1089			
74LVC3G06GD	–40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body $3 \times 2 \times 0.5$ mm				
74LVC3G06GM	C3G06GM -40 °C to +125 °C XQFN8 plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm		SOT902-2				
74LVC3G06GN	-40 °C to +125 °C	25 °C XSON8 extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm		SOT1116			
74LVC3G06GS	–40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	SOT1203			

## 4. Marking

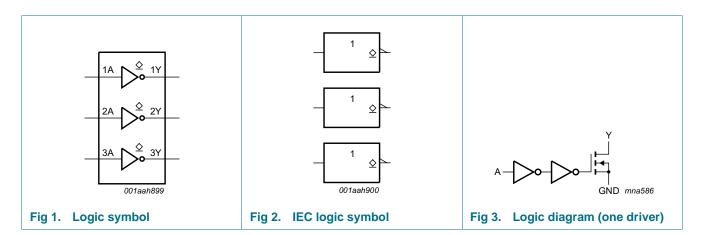
Table 2. Marking codes

Type number	Marking code[1]
74LVC3G06DP	V06
74LVC3G06DC	V06
74LVC3G06GT	V06
74LVC3G06GF	V6
74LVC3G06GD	V06
74LVC3G06GM	V06
74LVC3G06GN	V6
74LVC3G06GS	V6

<sup>[1]</sup> The pin 1 indicator is located on the lower left corner of the device, below the marking code.

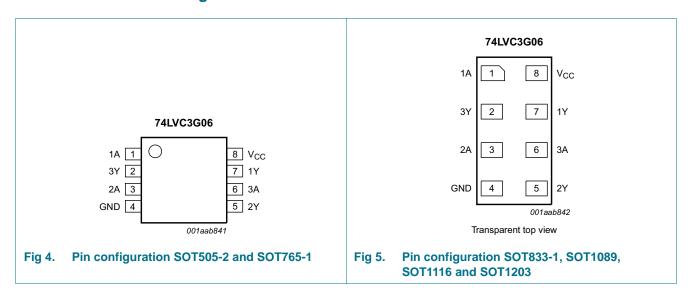
#### Triple inverter with open-drain output

## 5. Functional diagram

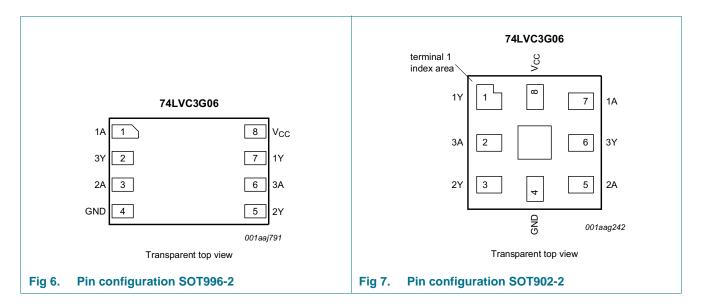


## 6. Pinning information

### 6.1 Pinning



#### Triple inverter with open-drain output



## 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description	
	SOT505-2, SOT765-1, SOT833-1, SOT1089, SOT996-2, SOT1116 and SOT1203	SOT902-2	
1A, 2A, 3A	1, 3, 6	7, 5, 2	data input
1Y, 2Y, 3Y	7, 5, 2	1, 3, 6	data output
GND	4	4	ground (0 V)
V <sub>CC</sub>	8	8	supply voltage

## 7. Functional description

Table 4. Function table [1]

Input nA	Output nY
L	Z
Н	L

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Triple inverter with open-drain output

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+6.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V		-50	-	mA
VI	input voltage		<u>[1]</u>	-0.5	+6.5	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V		-50	-	mA
Vo	output voltage	Active mode	<u>[1]</u>	-0.5	+6.5	V
		Power-down mode	[1][2]	-0.5	+6.5	V
Io	output current	V <sub>O</sub> = 0 V to 6.5 V		-	50	mA
I <sub>CC</sub>	supply current			-	100	mA
I <sub>GND</sub>	ground current			-100	-	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40  ^{\circ}\text{C} \text{ to } +125  ^{\circ}\text{C}$	[3]	-	250	mW

<sup>[1]</sup> The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	5.5	V
VI	input voltage		0	5.5	V
Vo	output voltage	Active mode	0	5.5	V
		Power-down mode; V <sub>CC</sub> = 0 V	0	5.5	V
T <sub>amb</sub>	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.65 V to 2.7 V	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 5.5 V	-	10	ns/V

<sup>[2]</sup> When  $V_{CC} = 0 \text{ V}$  (Power-down mode), the output voltage can be 5.5 V in normal operation.

<sup>[3]</sup> For TSSOP8 and VSSOP8 packages: above 110 °C the value of P<sub>tot</sub> derates linearly at 8.0 mW/K. For XSON8 and XQFN8 packages: above 118 °C the value of P<sub>tot</sub> derates linearly with 7.8 mW/K.

### Triple inverter with open-drain output

## 10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$T_{amb} = -40$	°C to +85 °C[1]		,			
V <sub>IH</sub>	HIGH-level input	V <sub>CC</sub> = 1.65 V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
	voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	$0.7 \times V_{CC}$	-	-	V
V <sub>IL</sub>	LOW-level input	V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
	voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	$0.3 \times V_{CC}$	V
V <sub>OL</sub>	LOW-level output	$V_I = V_{IH}$ or $V_{IL}$				
	voltage	$I_O = 100 \mu A$ ; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	-	0.10	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	V
		$I_{O} = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.30	V
		$I_{O}$ = 12 mA; $V_{CC}$ = 2.7 V	-	-	0.40	V
		$I_{O} = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	V
		$I_{O} = 32 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	[2] -	±0.1	±1	μА
l <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	±0.1	±2	μА
I <sub>OFF</sub>	power-off leakage current	$V_1 \text{ or } V_0 = 5.5 \text{ V}; V_{CC} = 0 \text{ V}$	-	±0.1	±2	μА
I <sub>CC</sub>	supply current	V <sub>I</sub> = 5.5 V or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 1.65 V to 5.5 V	-	0.1	4	μА
Δl <sub>CC</sub>	additional supply current	per pin; $V_I = V_{CC} - 0.6 \text{ V}$ ; $I_O = 0 \text{ A}$ ; $V_{CC} = 2.3 \text{ V}$ to 5.5 V	[2] -	5	500	μΑ
Cı	input capacitance		-	2.5	-	pF

### Triple inverter with open-drain output

 Table 7.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T <sub>amb</sub> = -40	0 °C to +125 °C					
V <sub>IH</sub>	HIGH-level input	V <sub>CC</sub> = 1.65 V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
	voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	$0.7 \times V_{CC}$	-	-	V
V <sub>IL</sub>	LOW-level input	V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
	voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	$0.3 \times V_{CC}$	V
V <sub>OL</sub>	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_{O}$ = 100 $\mu$ A; $V_{CC}$ = 1.65 V to 5.5 V	-	-	0.10	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.70	V
		$I_{O} = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.45	V
		$I_{O} = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	-	0.60	V
		$I_{O} = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.80	V
		$I_{O} = 32 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.80	V
l <sub>l</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	±1	μΑ
l <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±2	μΑ
I <sub>OFF</sub>	power-off leakage current	$V_{I}$ or $V_{O} = 5.5 \text{ V}$ ; $V_{CC} = 0 \text{ V}$	-	-	±2	μΑ
I <sub>CC</sub>	supply current	V <sub>I</sub> = 5.5 V or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 1.65 V to 5.5 V	-	-	4	μΑ
Δl <sub>CC</sub>	additional supply current	per pin; $V_I = V_{CC} - 0.6 \text{ V}$ ; $I_O = 0 \text{ A}$ ; $V_{CC} = 2.3 \text{ V}$ to 5.5 V	-	-	500	μΑ

<sup>[1]</sup> All typical values are measured at  $T_{amb}$  = 25 °C.

<sup>[2]</sup> These typical values are measured at  $V_{CC}$  = 3.3 V.

Triple inverter with open-drain output

## 11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 9.

Symbol	Parameter	Conditions	-40	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA to nY; see Figure 8						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	2.6	6.5	1.0	8.2	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	1.6	3.9	0.5	4.9	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.2	4.2	1.0	5.3	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.5	2.0	3.4	0.5	4.3	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	1.4	2.9	0.5	3.7	ns
C <sub>PD</sub>	power dissipation capacitance	$V_I = GND \text{ to } V_{CC}; V_{CC} = 3.3 \text{ V}$	-	5.9	-	-	-	pF

- [1] Typical values are measured at  $T_{amb} = 25$  °C and  $V_{CC} = 1.8$  V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.
- [2]  $t_{pd}$  is the same as  $t_{PLZ}$  and  $t_{PZL}$ .
- [3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

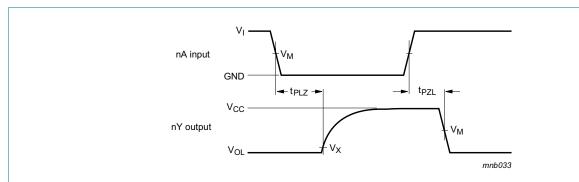
C<sub>L</sub> = output load capacitance in pF;

 $V_{CC}$  = supply voltage in V;

N = number of inputs switching;

 $\Sigma (C_L \times V_{CC}{}^2 \times f_o) = sum \ of \ outputs.$ 

#### 12. Waveforms



Measurement points are given in Table 9.

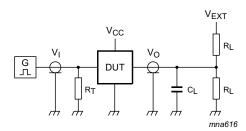
 $\ensuremath{V_{\text{OL}}}$  is the typical output voltage level that occurs with the output load.

Fig 8. The input (nA) to output (nY) propagation delays

#### Triple inverter with open-drain output

Table 9. Measurement points

Supply voltage	Input	Output		
V <sub>CC</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V <sub>OL</sub> + 0.15 V	
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V <sub>OL</sub> + 0.15 V	
2.7 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	
3.0 V to 3.6 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V <sub>OL</sub> + 0.3 V	



Test data is given in Table 10.

Definitions for test circuit:

R<sub>L</sub> = Load resistance.

 $C_L$  = Load capacitance including jig and probe capacitance.

 $R_T$  = Termination resistance should be equal to the output impedance  $Z_0$  of the pulse generator.

 $V_{EXT}$  = External voltage for measuring switching times.

Fig 9. Test circuit for measuring switching times

Table 10. Test data

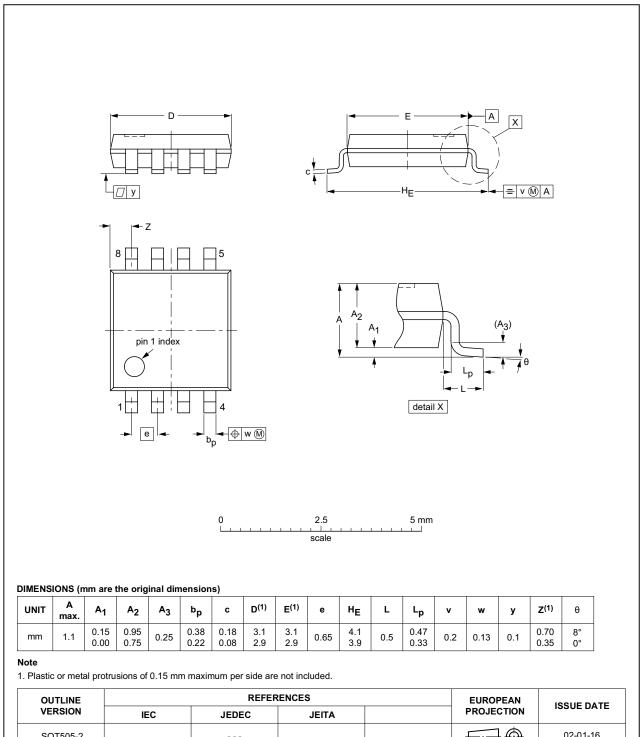
Supply voltage	Input		Load	V <sub>EXT</sub>	
V <sub>cc</sub>	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>
1.65 V to 1.95 V	V <sub>CC</sub>	≤ 2.0 ns	30 pF	1 kΩ	2 × V <sub>CC</sub>
2.3 V to 2.7 V	V <sub>CC</sub>	≤ 2.0 ns	30 pF	500 Ω	2 × V <sub>CC</sub>
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	6 V
4.5 V to 5.5 V	V <sub>CC</sub>	≤ 2.5 ns	50 pF	500 Ω	2 × V <sub>CC</sub>

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Triple inverter with open-drain output

## 13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT505-2					02-01-16
		•			

Fig 10. Package outline SOT505-2 (TSSOP8)

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Triple inverter with open-drain output

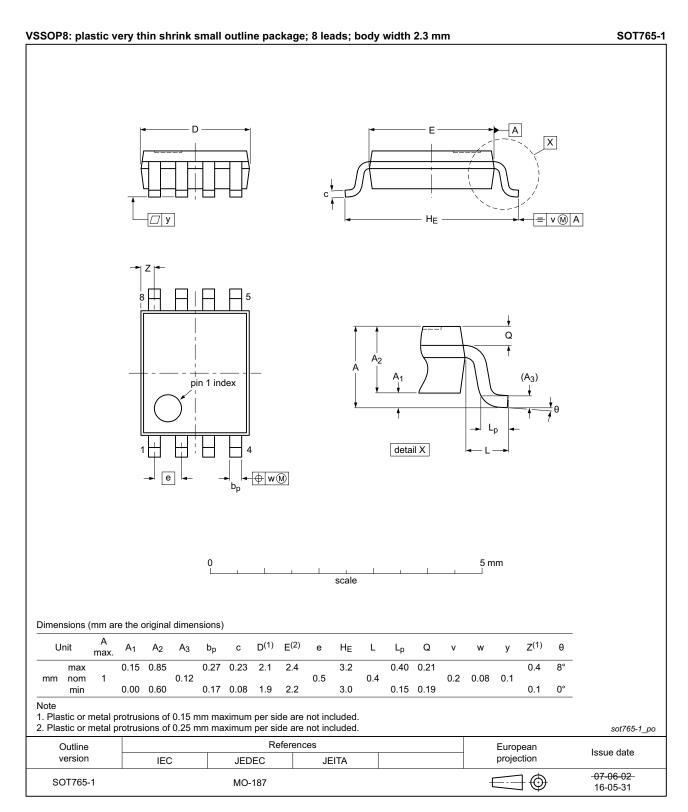


Fig 11. Package outline SOT765-1 (VSSOP8)

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Triple inverter with open-drain output

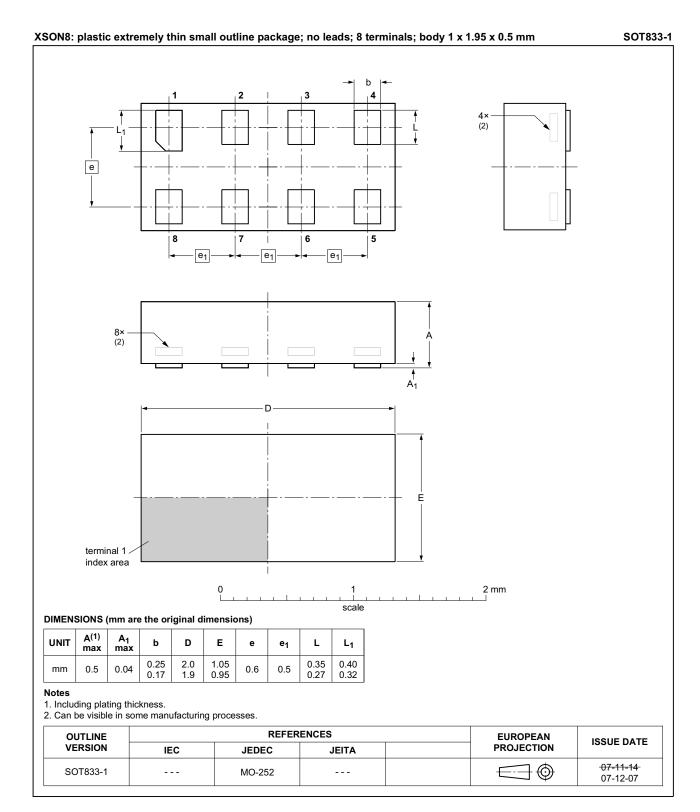


Fig 12. Package outline SOT833-1 (XSON8)

Triple inverter with open-drain output

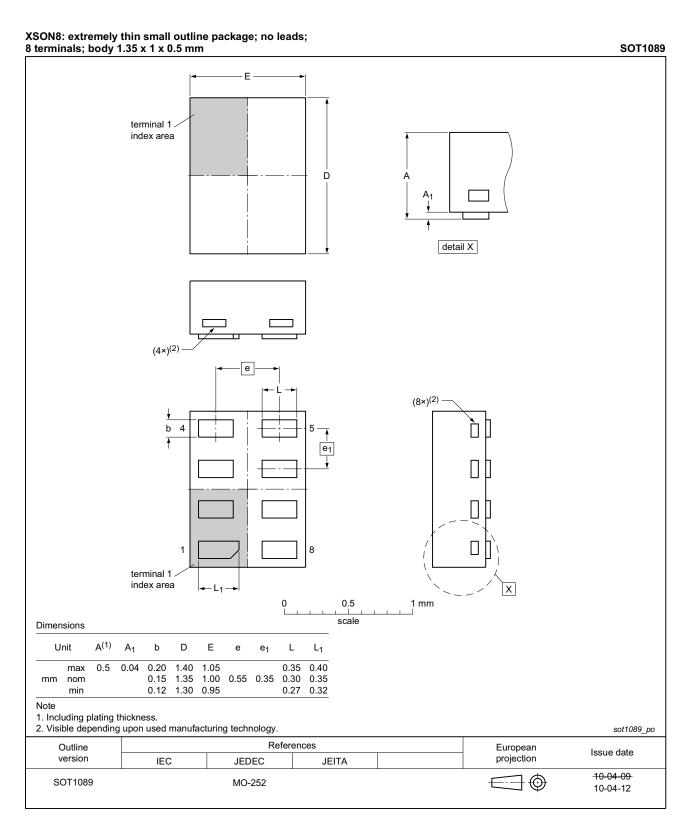


Fig 13. Package outline SOT1089 (XSON8)

Triple inverter with open-drain output

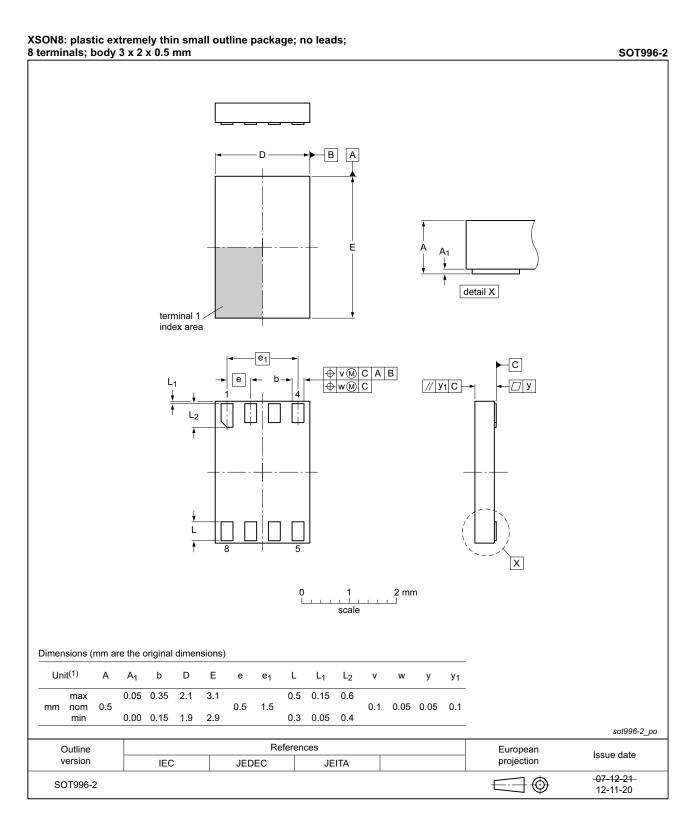


Fig 14. Package outline SOT996-2 (XSON8)

74LVC3G06

Triple inverter with open-drain output

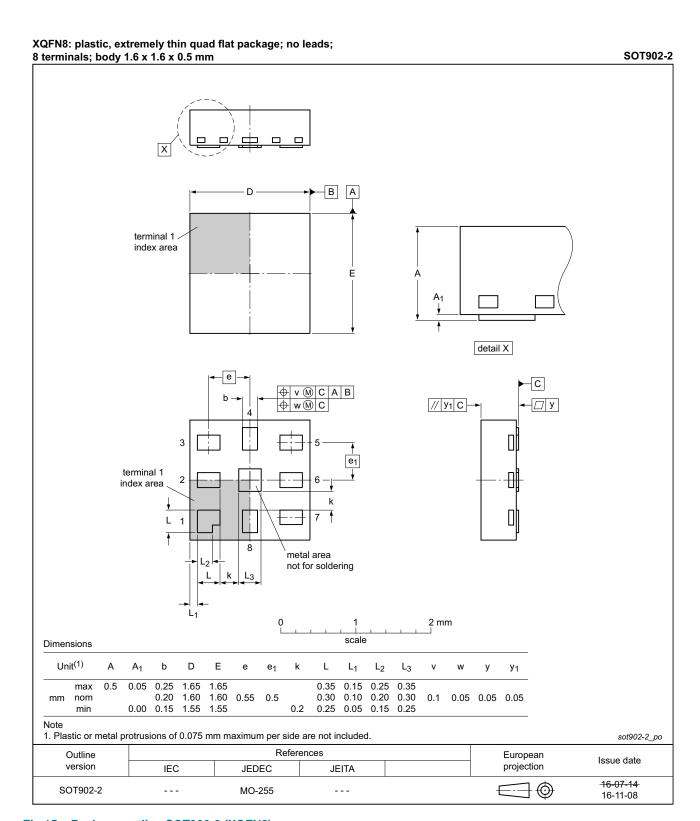


Fig 15. Package outline SOT902-2 (XQFN8)

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Triple inverter with open-drain output

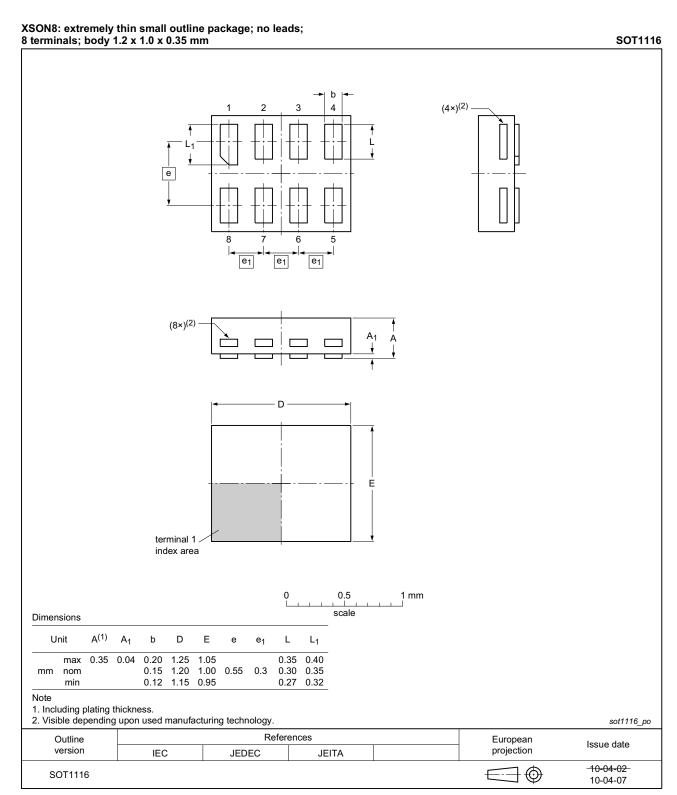


Fig 16. Package outline SOT1116 (XSON8)

74LVC3G06

Triple inverter with open-drain output

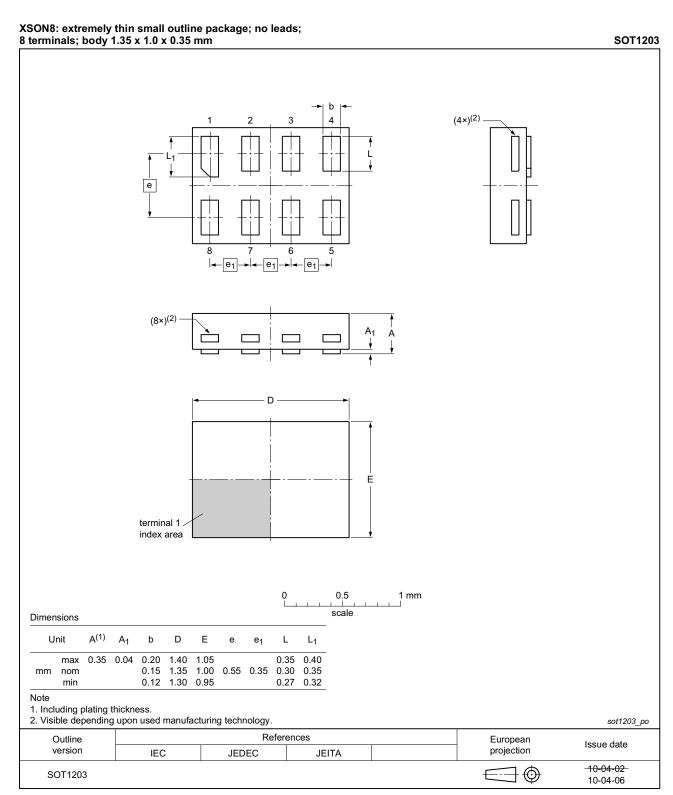


Fig 17. Package outline SOT1203 (XSON8)

### Triple inverter with open-drain output

## 14. Abbreviations

#### Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 15. Revision history

#### Table 12. Revision history

Release date	Data sheet status	Change notice	Supersedes
20161215	Product data sheet	-	74LVC3G06 v.11
• Table 7: The maximum limits for leakage current and supply current have changed.			
20130328	Product data sheet	-	74LVC3G06 v.10
<ul> <li>For type number 74</li> </ul>	LVC3G06GD XSON8U h	as changed to XSON8.	
20120627	Product data sheet	-	74LVC3G06 v.9
For type number 74LVC3G06GM the SOT code has changed to SOT902-2.			
20111123	Product data sheet	-	74LVC3G06 v.8
<ul> <li>Legal pages update</li> </ul>	d.		
20100809	Product data sheet	-	74LVC3G06 v.7
20090312	Product data sheet	-	74LVC3G06 v.6
20080403	Product data sheet	-	74LVC3G06 v.5
20070521	Product data sheet	-	74LVC3G06 v.4
20060302	Product data sheet	-	74LVC3G06 v.3
20050201	Product data sheet	-	74LVC3G06 v.2
20041021	Product data sheet	-	74LVC3G06 v.1
20040607	Product data sheet	-	-
	20161215  • Table 7: The maxim 20130328  • For type number 74 20120627  • For type number 74 20111123  • Legal pages update 20100809 20090312 20080403 20070521 20060302 20050201 20041021	20161215 Product data sheet  Table 7: The maximum limits for leakage curical c	20161215 Product data sheet -  • Table 7: The maximum limits for leakage current and supply current h 20130328 Product data sheet -  • For type number 74LVC3G06GD XSON8U has changed to XSON8.  20120627 Product data sheet -  • For type number 74LVC3G06GM the SOT code has changed to SOT 20111123 Product data sheet -  • Legal pages updated.  20100809 Product data sheet - 20090312 Product data sheet - 20080403 Product data sheet - 20070521 Product data sheet - 20060302 Product data sheet - 20050201 Product data sheet - 20041021 Product data sheet -

#### Triple inverter with open-drain output

## 16. Legal information

#### 16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

#### 16.2 Definitions

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## 18. Contents

**Nexperia** 

1	General description
2	Features and benefits
3	Ordering information 2
4	Marking 2
5	Functional diagram 3
6	Pinning information 3
6.1	Pinning
6.2	Pin description 4
7	Functional description 4
8	Limiting values 5
9	Recommended operating conditions 5
10	Static characteristics 6
11	Dynamic characteristics 8
12	Waveforms
13	Package outline
14	Abbreviations
15	Revision history
16	Legal information
16.1	Data sheet status
16.2	Definitions
16.3	Disclaimers
16.4	Trademarks20
17	Contact information 20
18	Contents 21