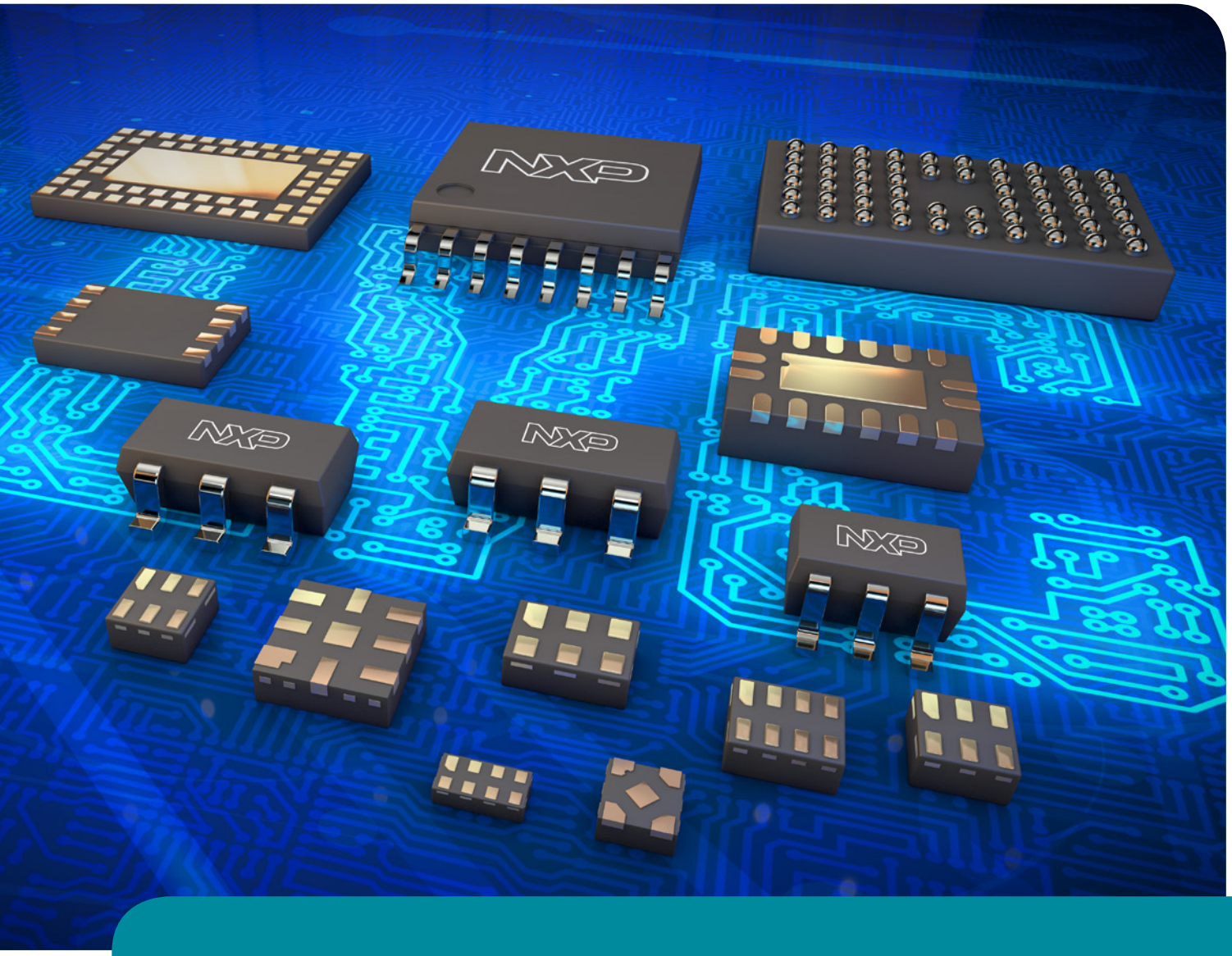
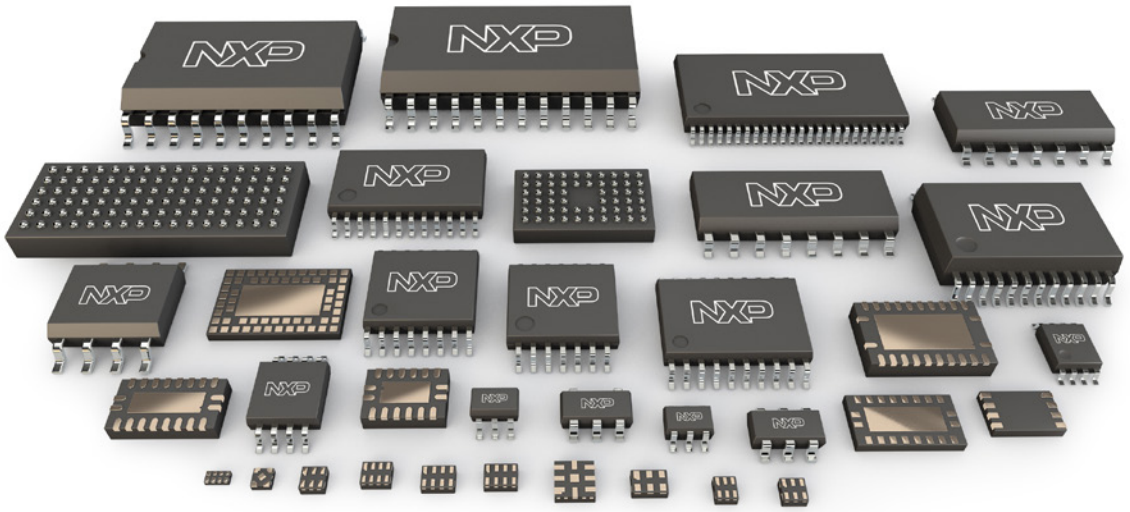


Low voltage CMOS family — LVC

Reliable solutions for mixed voltage applications



NXP offers the feature rich Low Voltage CMOS (LVC) logic portfolio to enable the migration of electronic solutions from 5.5 V to lower power mixed 5.5 V / 3.3 V and beyond. The LVC family includes Standard Logic functions with supply range 1.65 V to 3.3 V, as well as Mini Logic functions with supply range 1.65 V to 5.5 V.

Key features

- 4 ns typical propagation delay
- 24 mA balanced output drive
- Wide supply range
- 5 V tolerant I/O
- Series termination options
- Bus Hold options
- AEC-Q100 compliant options
- Fully specified (-40 to +125 °C)
- Pb-free, RoHS compliant and Dark Green

Benefits

- Low power consumption
- Suitable for driving transmission lines
- Migration path to lower voltage nodes

Applications

- Computing, servers
- Telecom and networking equipment
- Advanced bus interface
- Industrial
- Automotive

Power consumption is directly proportional to supply voltage. As a result there is a trend in most applications towards lower and lower supply voltage nodes. The LVC logic portfolio supports that trend. It is fully specified at the 1.8 V supply node (1.65 V to 1.95 V).

The migration to lower supply voltage often requires the solution to be compatible with legacy higher voltage applications. LVC includes several features to enable them to be used in mixed voltage applications.

The LVC portfolio is broad. It includes Standard and Mini Logic products available in the industry standard leaded packages, as well as innovative leadless packages.

Migration to lower voltage nodes

Migrating an application from 5.0 V to 3.3 V represents a 34% power savings. Similarly migrating from 3.3 V to 1.8 V represents a 45% power savings. These are considerable savings and as the major chip-set supply voltages decrease the LVC logic portfolio is available to support control logic, interface and general purpose i/o expansion needs.

LVC products include features that support the migration through mixed voltage to lower voltage nodes and partial power down applications. These features are, Over-voltage tolerant inputs and I_{OFF} circuitry.

Over-voltage tolerant inputs

These inputs include a modified ESD input structure that removes any diode between the input and the supply rail, without affecting ESD performance. As a result 5.0 V outputs from a legacy application can be applied to the input of an LVC device supplied with 3.3 V.

I_{OFF} circuitry

To reduce standby current many applications use advanced power management that powers down unused circuits within the application. To support this partial power down architecture a logic family must not have any leakage paths to the supply rails when the supply voltage (V_{CC}) is 0 V. LVC includes I_{OFF} circuitry that prevents current paths through inputs and outputs when V_{CC} = 0 V.

Inputs and outputs

Inputs

There are two types of input circuits in the LVC family.

Schmitt-trigger action input. This input has a small amount of hysteresis built into the input switching levels. The hysteresis is not formally specified but it does allow the input to be tolerant to input slew rates as high as 20 ns/V at V_{CC} = 1.65 V to 2.7 V and 10 ns/V at V_{CC} = 2.7 V to 5.5 V. The Schmitt-trigger action input may be preceded by a bus-hold cell to define unused inputs. This bus-hold cell does not affect the performance of the device.

Schmitt-trigger input. This input has much higher input hysteresis which is formally specified in the datasheet. The advantage of true Schmitt-trigger inputs is that they are tolerant to very slow edges. Figure 1 shows a side by side comparison of the IV characteristics of the Schmitt-trigger action input and the Schmitt-trigger input.

Outputs

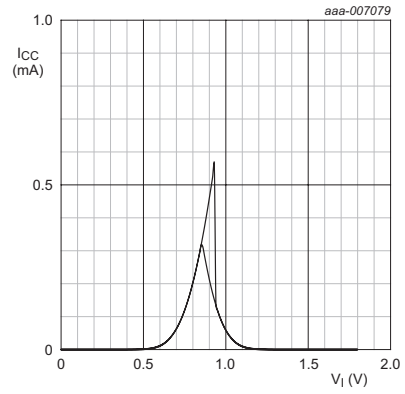
Three types of output drivers are used in the LVC family.

The ***standard output*** is used in the standard logic devices. It provides a balanced 24 mA output drive at 3.3 V.

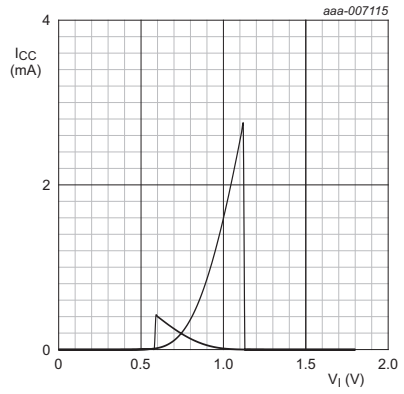
The ***source terminated output*** is used in standard logic devices that feature source termination for better matching in distributed load applications such as transmission lines. It has a balanced 12 mA output drive at 3.3 V.

The ***Mini Logic output*** is suitable for use over a wider supply voltage range. It provides a balanced 24 mA output drive at 3.3 V and a balanced 32 mA output drive at 5.0 V. Figure 2 shows a side by side comparison of the IV characteristics of all three outputs.

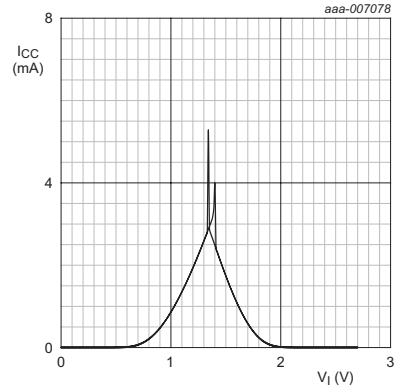
For more information about the bus hold or source termination feature visit:
www.youtube.com/user/LogicHeads



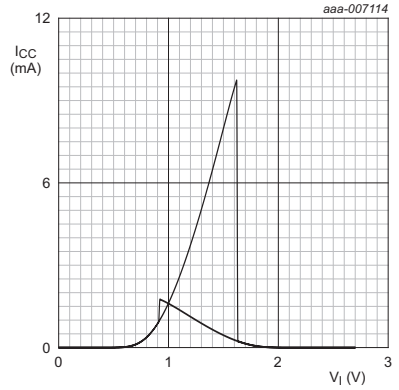
1.8 V Schmitt action



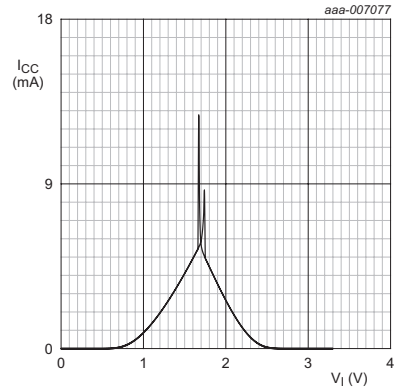
1.8 V Schmitt trigger



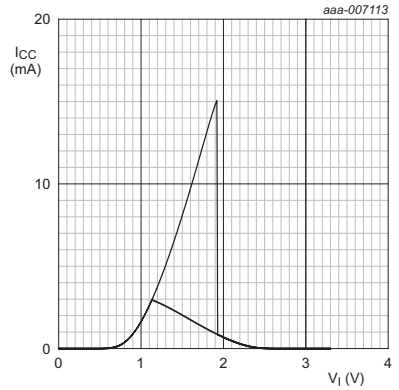
2.7 V Schmitt action



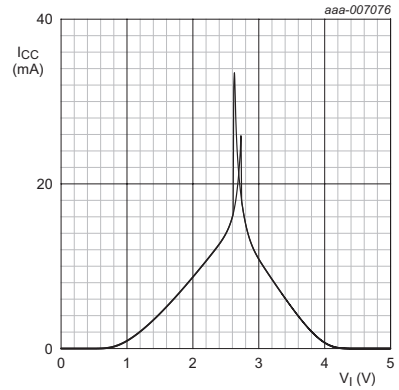
2.7 V Schmitt trigger



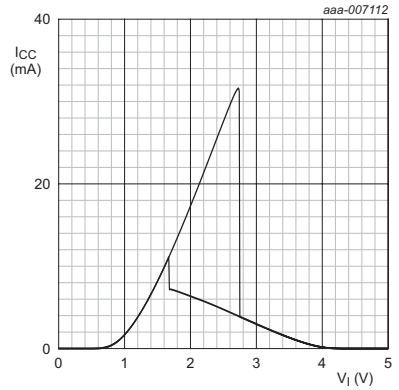
3.3 V Schmitt action



3.3 V Schmitt trigger

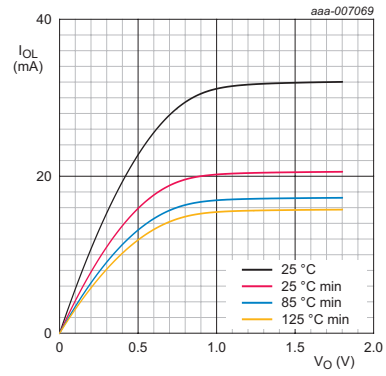


5.0 V Schmitt action

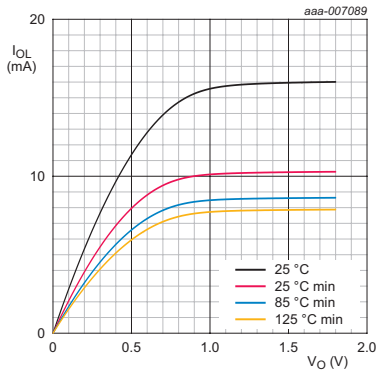


5.0 V Schmitt trigger

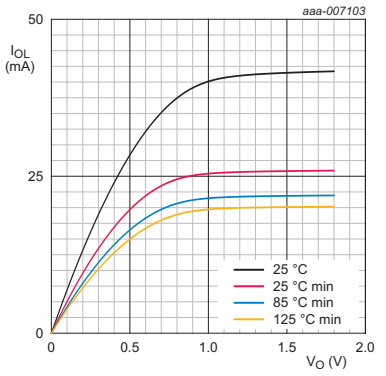
Figure 1: Comparison of typical Schmitt action v Schmitt trigger inputs



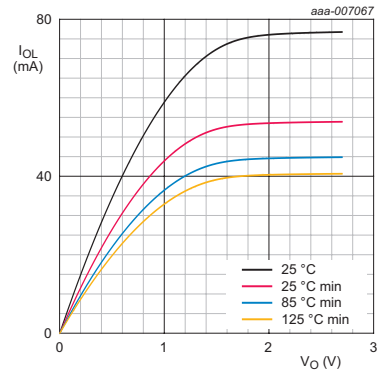
1.8 V Standard output



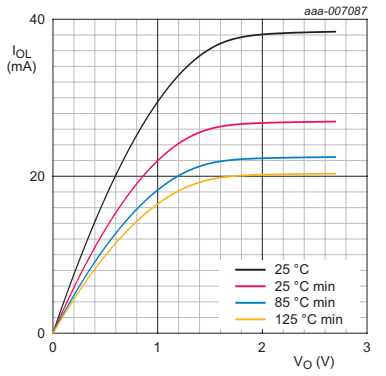
1.8 V terminated output



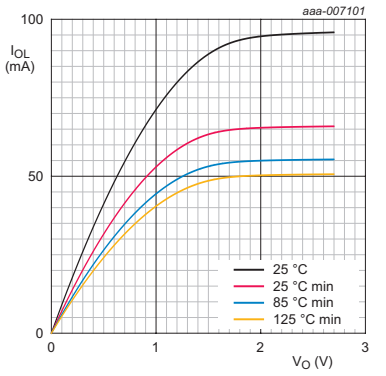
1.8 V Mini Logic output



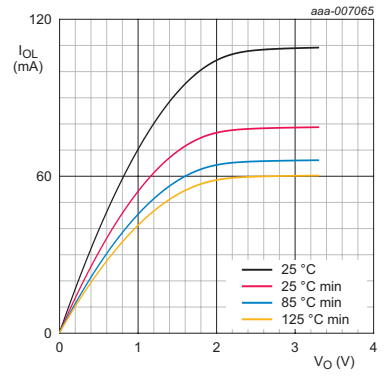
2.7 V Standard output



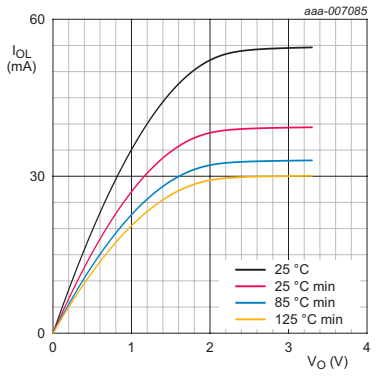
2.7 V terminated output



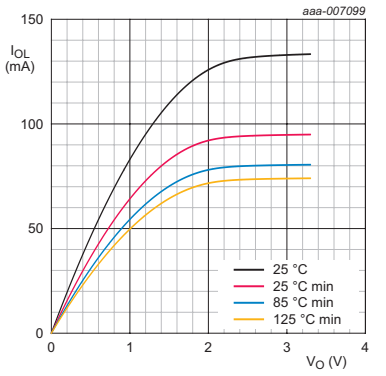
2.7 V Mini Logic output



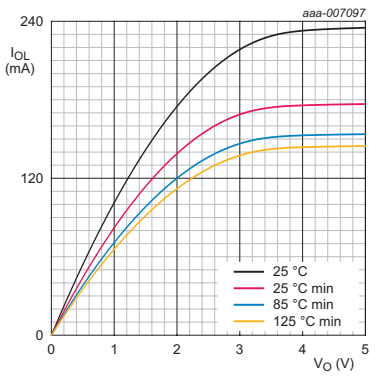
3.3 V Standard output



3.3 V terminated output

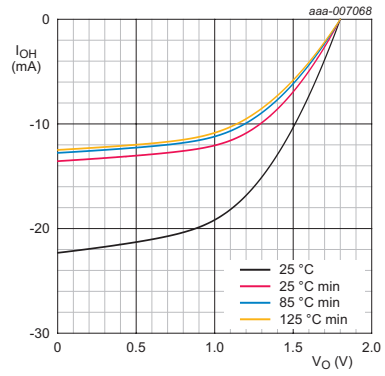


3.3 V Mini Logic output

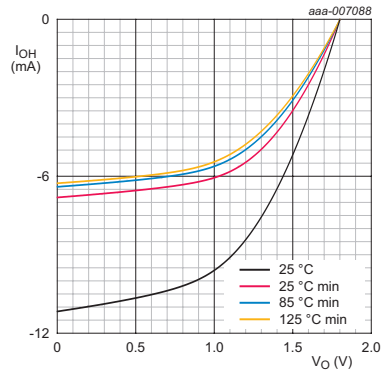


5.5 V Mini Logic output

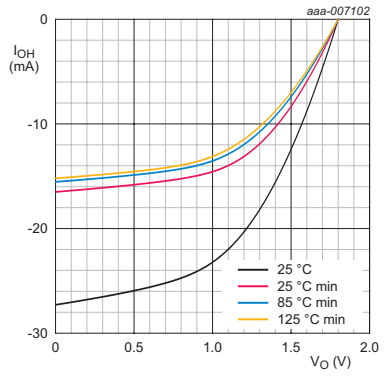
Figure 2a: Comparison of LVC outputs N-channel sink current (I_{OL})



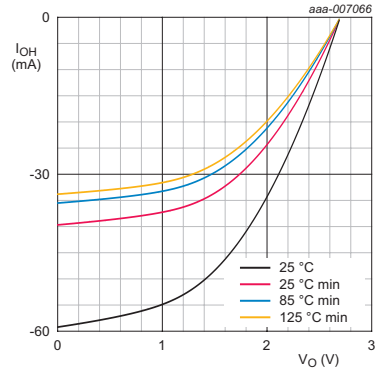
1.8 V Standard output



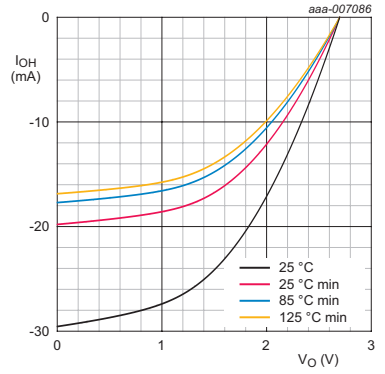
1.8 V terminated output



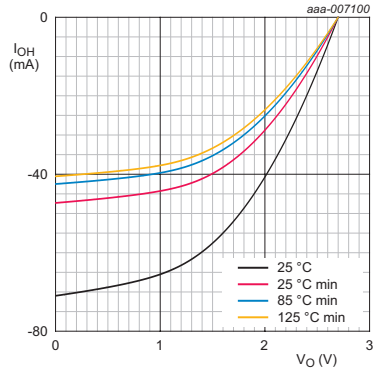
1.8 V Mini Logic output



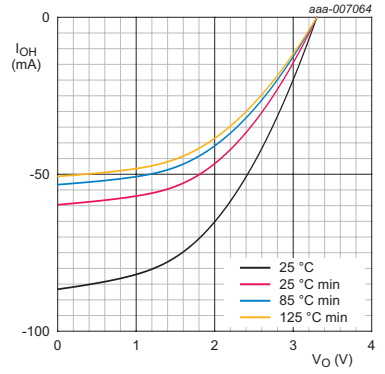
2.7 V Standard output



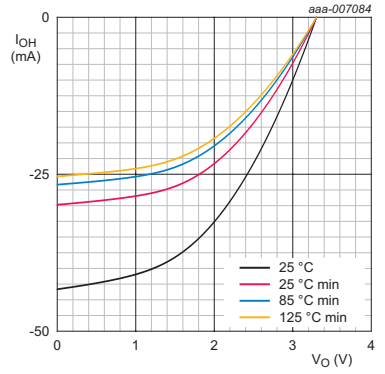
2.7 V terminated output



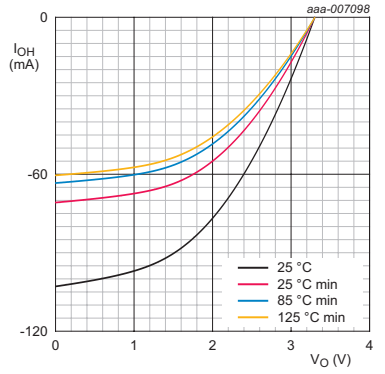
2.7 V Mini Logic output



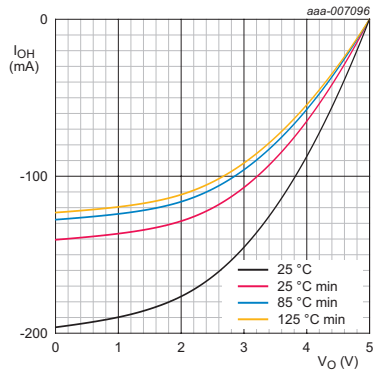
3.3 V Standard output



3.3 V terminated output



3.3 V Mini Logic output



5.5 V Mini Logic output

Figure 2b: Comparison of LVC outputs P-channel source current (I_{OH})

LVC standard logic functions and packages

Standard logic functions

LVC standard logic functions are suitable for use at supply voltage between 1.65 V to 3.6 V. They include a wide range of functions including analog switches, buffers/inverters, counters, decoders/de-multiplexers, multiplexers, flip-flops, gates, latches, level shifters, shift registers and transceivers.

		Features								Package (suffix)																
Type number	Description	Bus hold inputs	Schmitt trigger inputs	Schmitt trigger action	Over-voltage tolerant inputs	Open-drain output	Power-off protection (I_{OFF})	Source termination	Dual supply translator	SOT108-1 (D)	SOT109-1 (D)	SOT137-1 (D)	SOT163-1 (D)	SOT355-1 (PW)	SOT360-1 (PW)	SOT362-1 (DGG)	SOT402-1 (PW)	SOT403-1 (PW)	SOT536-1 (EC)	SOT702-1 (EV)	SOT762-1 (BQ)	SOT763-1 (BQ)	SOT764-1 (BQ)	SOT815-1 (BQ)	SOT1045-2 (BX)	SOT1134-2 (BX)
Analog switches																										
74LVC4066	quad single-pole, single-throw analog switch			•	•		•			•							•				•				
Buffers/inverters																										
74LVC04A	hex inverter			•	•					•							•				•				
74LVC06A	hex inverter; open-drain			•	•	•				•							•				•				
74LVC07A	hex buffer; open-drain			•	•	•				•							•				•				
74LVC14A	hex inverter Schmitt-trigger		•		•					•							•				•				
74LVC125A	quad buffer/line driver (3-state)			•	•		•			•							•				•				
74LVC126A	quad buffer/line driver (3-state)			•	•		•			•							•				•				
74LVC240A	octal inverter/line driver (3-state)			•	•		•						•		•								•			
74LVC241A	octal buffer/line driver (3-state)			•	•		•						•		•											
74LVC541A	octal buffer/line driver (3-state)			•	•		•						•		•								•			
74LVC827A	10-bit buffer/line driver (3-state)			•	•		•					•		•												
74LVC2244A	octal buffer/line driver with source termination (3-state)			•	•		•	•					•		•								•			
74LVC16240A	16-bit inverter/line driver (3-state)			•	•		•									•										
74LVC16241A	16-bit buffer/line driver (3-state)			•	•		•									•										
74LVC244A	octal buffer/line driver (3-state)			•	•		•						•		•								•		•	
74LVCH244A	octal buffer/line driver with bus hold (3-state)	•		•	•		•						•		•								•		•	
74LVC16244A	16-bit buffer/line driver (3-state)			•	•		•									•				•						•
74LVCH16244A	16-bit buffer/line driver with bus hold (3-state)	•		•	•		•									•				•						•
74LVC162244A	16-bit buffer/line driver with source termination (3-state)			•	•		•	•								•										
74LVCH162244A	16-bit buffer/line driver with bus hold and source termination (3-state)	•		•	•		•	•								•										
74LVCH16541A	16-bit buffer/line driver with bus hold (3-state)	•		•	•		•									•										
74LVCH32244A	32-bit buffer/line driver with bus hold (3-state)	•		•	•		•												•							
74LVCH322244A	32-bit buffer/line driver with bus hold and source termination (3-state)	•		•	•		•	•											•							
74LVCU04A	hex inverter; unbuffered			•	•					•							•				•					
Counters																										
74LVC161	presettable synchronous 4-bit binary counter; asynchronous reset			•	•						•							•				•				
74LVC163	presettable synchronous 4-bit binary counter; synchronous reset			•	•						•							•				•				
74LVC169	presettable synchronous 4-bit binary up/down counter			•	•						•							•				•				

Standard logic functions (continued)

Type number	Description	Features								Package (suffix)																
		Bus hold inputs	Schmitt trigger inputs	Schmitt trigger action	Over-voltage tolerant inputs	Open-drain output	Power-off protection (I_{OFF})	Source termination	Dual supply translator	SOT108-1 (D)	SOT109-1 (D)	SOT137-1 (D)	SOT163-1 (D)	SOT355-1 (PW)	SOT360-1 (PW)	SOT362-1 (DGG)	SOT402-1 (PW)	SOT403-1 (PW)	SOT536-1 (EC)	SOT702-1 (EV)	SOT762-1 (BQ)	SOT763-1 (BQ)	SOT764-1 (BQ)	SOT815-1 (BQ)	SOT1045-2 (BX)	SOT1134-2 (BX)
Demultiplexers																										
74LVC138A	3-to-8 line decoder/demultiplexer; inverting			•	•						•							•				•				
74LVC139	dual 2-to-4 line decoder/ demultiplexer			•	•						•							•				•				
Multiplexers																										
74LVC157	quad 2-input multiplexer			•	•						•							•				•				
74LVC257	quad 2-input multiplexer (3-State)			•	•		•				•							•				•				
Flip-flops																										
74LVC74A	dual D-type flip-flop with set and reset; positive-edge trigger			•	•					•							•				•					
74LVC273	octal D-type flip-flop with reset; positive-edge trigger			•	•								•		•								•			
74LVC374A	octal D-type flip-flop; positive-edge trigger (3-state)			•	•		•						•		•								•			
74LVC377	octal D-type flip-flop with data enable; positive-edge trigger			•	•								•		•								•			
74LVC574A	octal D-type flip-flop; positive-edge trigger (3-state)			•	•		•						•		•								•			
74LVC821A	10-bit D-type flip-flop; positive-edge trigger (3-state)			•	•		•					•		•										•		
74LVC823A	9-bit D-type flip-flop; positive-edge trigger (3-state)			•	•		•					•		•										•		
74LVC16374A	16-bit D-type flip-flop; positive-edge trigger (3-state)			•	•		•									•										•
74LVCH16374A	32-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)	•		•	•		•									•										•
74LVCH32374A	16-bit D-type flip-flop with bus hold and source termination; positive-edge trigger (3-state)	•		•	•		•	•											•							
74LVCH162374A	16-bit D-type flip-flop with bus hold and source termination; positive-edge trigger (3-state)	•		•	•		•	•								•										
Gates																										
74LVC00A	quad 2-input NAND gate			•	•					•							•				•					
74LVC02A	quad 2-input NOR gate			•	•					•							•				•					
74LVC08A	quad 2-input AND gate			•	•					•							•				•					
74LVC10A	triple 3-input NAND gate			•	•					•							•				•					
74LVC11	triple 3-input AND gate			•	•					•							•				•					
74LVC30A	8-input NAND gate			•	•					•							•				•					
74LVC32A	quad 2-input OR gate			•	•					•							•				•					
74LVC38A	quad 2-input NAND gate; open-drain			•	•	•				•							•				•					
74LVC86A	quad 2-input EXCLUSIVE-OR gate			•	•					•							•				•					
74LVC132A	quad 2-input NAND gate Schmitt-trigger		•		•					•							•				•					
74LVC332	triple 3-input OR gate			•	•					•							•				•					
Latches																										
74LVC373A	octal D-type transparent latch (3-state)			•	•		•						•		•								•			

Standard logic functions (continued)

Type number	Description	Features								Package (suffix)																
		Bus hold inputs	Schmitt trigger inputs	Schmitt trigger action	Over-voltage tolerant inputs	Open-drain output	Power-off protection (I_{OFF})	Source termination	Dual supply translator	SOT108-1 (D)	SOT109-1 (D)	SOT137-1 (D)	SOT163-1 (D)	SOT355-1 (PW)	SOT360-1 (PW)	SOT362-1 (DGG)	SOT402-1 (PW)	SOT403-1 (PW)	SOT536-1 (EC)	SOT702-1 (EV)	SOT762-1 (BQ)	SOT763-1 (BQ)	SOT764-1 (BQ)	SOT815-1 (BQ)	SOT1045-2 (BX)	SOT1134-2 (BX)
74LVC573A	octal D-type transparent latch (3-state)			•	•		•						•		•								•		•	
74LVC841A	10-bit D-type transparent latch (3-state)			•	•		•					•		•										•		
74LVC16373A	16-bit D-type transparent latch (3-state)			•	•		•									•										
74LVCH16373A	16-bit D-type transparent latch with bus hold (3-state)	•		•	•		•									•										
74LVC162373A	16-bit D-type transparent latch with source termination (3-state)	•		•	•		•	•								•										
74LVCH162373A	16-bit D-type transparent latch with bus hold and source termination (3-state)	•		•	•		•	•								•										
74LVCH32373A	32-bit D-type transparent latch (3-state)	•		•	•		•												•							
Level shifters																										
74LVC4245A	8-bit dual-supply voltage translating transceiver (3-state)			•	•		•		•			•		•										•		
74LVC8T245	8-bit dual-supply voltage translating transceiver (3-state)			•	•		•		•					•										•		
74LVCH8T245	8-bit dual-supply voltage translating transceiver with bus hold (3-state)	•		•	•		•		•					•										•		
Shift registers																										
74LVC594	8-bit serial-in/parallel-out shift register with output storage register			•	•		•				•							•				•				
74LVC595	8-bit serial-in/parallel-out shift register with output storage register (3-state)			•	•		•				•							•				•				
Transceivers																										
74LVC543	octal registered transceiver (3-state)			•	•		•					•		•										•		
74LVC544A	octal registered transceiver; inverting (3-state)			•	•		•					•		•												
74LVC646A	octal registered transceiver (3-state)			•	•		•					•		•												
74LVC2245A	octal transceiver with source termination (3-state)			•	•		•	•					•		•								•			
74LVC2952A	octal registered transceiver with source termination (3-state)			•	•		•	•						•												
74LVC32245A	32-bit transceiver (3-state)			•	•		•												•							
74LVC245A	octal transceiver (3-state)			•	•		•						•		•								•		•	
74LVCH245A	octal transceiver with bus hold (3-state)	•		•	•		•						•		•								•		•	
74LVC16245A	16-bit transceiver (3-state)			•	•		•									•				•						
74LVCH16245A	16-bit transceiver with bus hold (3-state)	•		•	•		•									•				•						•
74LVC162245A	16-bit transceiver with source termination (3-state)			•	•		•	•								•										
74LVCH162245A	16-bit transceiver with bus hold and source termination (3-state)	•		•	•		•	•								•										
74LVCH32245A	32-bit transceiver with bus hold (3-state)	•		•	•		•												•							
74LVCH322245A	32-bit transceiver with bus hold and source termination (3-state)	•		•	•		•	•											•							

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www.nxp.com/products/logic/analog_switches/
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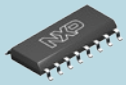
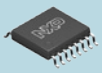
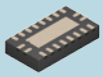
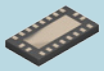
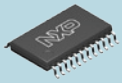
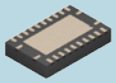
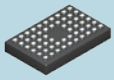
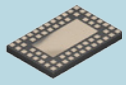
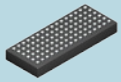
www.nxp.com/products/logic/transceivers/

Standard logic packages

Package suffix	D	PW	BQ	D	PW	BQ	D	PW	BQ
	14-pin	14-pin	14-pin	16-pin	16-pin	16-pin	20-pin	20-pin	20-pin
									
Package	SOT108-1	SOT402-1	SOT762-1	SOT109-1	SOT403-1	SOT763-1	SOT163-1	SOT360-1	SOT764-1
Width (mm)	6.00	6.40	2.50	6.00	6.40	2.50	10.30	6.40	2.50
Length (mm)	8.65	5.00	3.00	9.90	5.00	3.50	12.80	6.50	4.50
Height (mm)	1.75	1.10	1.00	1.75	1.10	1.00	2.65	1.10	1.00
Pitch (mm)	1.27	0.65	0.50	1.27	0.65	0.50	1.27	0.65	0.5

Package suffix	BX	D	PW	BQ	DGG	EV	BX	EC
	20-pin	24-pin	24-pin	24-pin	48-pin	56-pin	60-pin	96-pin
								
Package	SOT1045-1	SOT137-1	SOT355-1	SOT815-1	SOT362-1	SOT702-1	SOT1134-2	SOT536-1
Width (mm)	2.50	10.30	6.40	3.50	8.10	4.50	4.00	5.50
Length (mm)	4.50	15.40	7.80	5.50	12.50	7.00	6.00	13.50
Height (mm)	0.50	2.65	1.10	1.00	1.20	1.00	0.50	1.50
Pitch (mm)	0.50	1.27	0.65	0.50	0.50	0.65	0.50	0.80

Further information about packages can be found at: www.nxp.com/packages/

LVC mini logic functions and packages

Mini-logic functions

LVC Mini-Logic functions are suitable for use at supply voltage between 1.65 V to 5.5 V. They include a wide range of functions including analog switches, buffers/inverters, decoders/de-multiplexers, multiplexers, gates, configurable logic and level shifters.

Type number	Description	Features							Package (suffix)																
		Bus hold inputs	Schmitt trigger inputs	Schmitt trigger action	Over-voltage tolerant inputs	Open-drain output	Power-off protection (I_{OFF})	Dual supply translator	SOT353-1 (GW)	SOT363 (GW)	SOT457 (GV)	SOT505-2 (DP)	SOT753 (GV)	SOT765-1 (DC)	SOT833-1 (GT)	SOT886 (GM)	SOT891 (GF)	SOT902-2 (GM)	SOT996-2 (GD)	SOT1089 (GF)	SOT1115 (GN)	SOT1116 (GN)	SOT1202 (GS)	SOT1203 (GS)	SOT1226 (GX)
Analog switches																									
74LVC1G53	single-pole, double-throw analog switch			•	•							•		•	•			•	•	•		•		•	
74LVC1G66	single-pole, single-throw analog switch			•	•				•				•			•	•				•		•		
74LVC1G384	single-pole, single-throw analog switch			•	•				•				•			•	•				•		•		
74LVC1G3157	single-pole, double-throw analog switch			•	•					•	•					•	•				•		•		
74LVC2G53	single-pole, double-throw analog switch			•	•							•		•	•			•	•	•		•		•	
74LVC2G66	dual, single-pole, single throw analog switch			•	•							•		•	•			•	•						
74LVCV2G66	dual, single-pole, single-throw analog switch; over-voltage tolerant i/o's			•	•							•		•					•						
Buffers/inverters																									
74LVC1G04	single inverter			•	•		•		•				•			•	•				•		•		•
74LVC1G06	single inverter; open-drain			•	•	•	•		•				•			•	•				•		•		•
74LVC1G07	single buffer; open-drain			•	•	•	•		•				•			•	•				•		•		•
74LVC1G14	single inverter Schmitt-trigger		•		•		•		•				•			•	•				•		•		•
74LVC1G17	single buffer Schmitt-trigger		•		•		•		•				•			•	•				•		•		•
74LVC1G34	single buffer			•	•		•		•				•			•	•				•		•		•
74LVC1G125	single buffer/line driver; 3-state			•	•		•		•				•			•	•				•		•		
74LVC1G126	single buffer/line driver; 3-state			•	•		•		•				•			•	•				•		•		
74LVC1GU04	single inverter; unbuffered			•	•		•		•				•			•	•				•		•		•
74LVC2G04	dual inverter			•	•		•			•	•					•	•				•		•		
74LVC2G06	dual inverter; open-drain			•	•	•	•			•	•					•	•				•		•		
74LVC2G07	dual buffer; open-drain			•	•	•	•			•	•					•	•				•		•		
74LVC2G14	dual inverter Schmitt-trigger		•		•		•			•	•					•	•				•		•		
74LVC2G17	dual buffer Schmitt-trigger		•		•		•			•	•					•	•				•		•		

Mini logic functions (continued)

Type number	Description	Features							Package (suffix)																
		Bus hold inputs	Schmitt trigger inputs	Schmitt trigger action	Over-voltage tolerant inputs	Open-drain output	Power-off protection (I_{OFF})	Dual supply translator	SOT353-1 (GW)	SOT363 (GW)	SOT457 (GV)	SOT505-2 (DP)	SOT753 (GV)	SOT765-1 (DC)	SOT833-1 (GT)	SOT886 (GM)	SOT891 (GF)	SOT902-2 (GM)	SOT996-2 (GD)	SOT1089 (GF)	SOT1115 (GN)	SOT1116 (GN)	SOT1202 (GS)	SOT1203 (GS)	SOT1226 (GX)
74LVC2G34	dual buffer			•	•		•			•	•					•	•				•		•		
74LVC2G125	dual buffer/line driver; 3-state			•	•		•					•		•	•			•	•	•		•		•	
74LVC2G126	dual buffer/line driver; 3-state			•	•		•					•		•	•			•	•	•		•		•	
74LVC2G240	dual inverter/line driver; 3-state			•	•		•					•		•	•			•	•	•		•			
74LVC2G241	dual buffer/line driver; 3-state			•	•		•					•		•	•			•	•	•		•		•	
74LVC2GU04	dual inverter; unbuffered			•	•		•			•	•					•	•				•		•		
74LVC3G04	triple inverter			•	•		•					•		•	•			•	•	•		•		•	
74LVC3G06	triple inverter; open-drain			•	•	•	•					•		•	•			•	•	•		•		•	
74LVC3G07	triple buffer; open-drain			•	•	•	•					•		•	•			•	•	•		•		•	
74LVC3G34	triple buffer			•	•		•					•		•	•			•	•	•		•		•	
74LVC3G14	triple inverter Schmitt-trigger		•		•		•					•		•	•			•	•	•		•		•	
74LVC3G17	triple buffer Schmitt-trigger		•		•		•					•		•	•			•	•	•		•		•	
74LVC3GU04	triple inverter; unbuffered			•	•		•					•		•	•			•	•	•		•		•	
Demultiplexers																									
74LVC1G18	1-to-2 demultiplexer; 3-state			•	•		•			•	•														
74LVC1G19	1-to-2 decoder/demultiplexer			•	•		•			•	•					•	•				•		•		
Multiplexers																									
74LVC1G157	single 2-input multiplexer			•	•		•			•	•					•	•				•		•		
Gates																									
74LVC1G00	single 2-input NAND gate			•	•		•		•				•			•	•				•		•		•
74LVC1G02	single 2-input NOR gate			•	•		•		•				•			•	•				•		•		•
74LVC1G08	single 2-input AND gate			•	•		•		•				•			•	•				•		•		•
74LVC1G10	single 3-input NAND gate			•	•		•			•	•					•	•				•		•		
74LVC1G11	single 3-input AND gate			•	•		•			•	•					•	•				•		•		
74LVC1G27	single 3-input NOR gate			•	•		•			•	•					•	•				•		•		
74LVC1G32	single 2-input OR gate			•	•		•		•				•			•	•				•		•		
74LVC1G38	single 2-input NAND gate; open-drain			•	•	•	•		•				•			•	•				•		•		
74LVC1G86	single 2-input EXCLUSIVE-OR gate			•	•		•		•				•			•	•				•		•		
74LVC1G332	single 3-input OR gate			•	•		•			•	•					•	•				•		•		
74LVC1G386	single 3-Input EXCLUSIVE-OR gate			•	•		•			•	•														

Mini logic functions (continued)

Type number	Description	Features							Package (suffix)																
		Bus hold inputs	Schmitt trigger inputs	Schmitt trigger action	Over-voltage tolerant inputs	Open-drain output	Power-off protection (I_{OFF})	Dual supply translator	SOT353-1 (GW)	SOT363 (GW)	SOT457 (GV)	SOT505-2 (DP)	SOT753 (GV)	SOT765-1 (DC)	SOT833-1 (GT)	SOT886 (GM)	SOT891 (GF)	SOT902-2 (GM)	SOT996-2 (GD)	SOT1089 (GF)	SOT1115 (GN)	SOT1116 (GN)	SOT1202 (GS)	SOT1203 (GS)	SOT1226 (GX)
74LVC1GX04	crystal driver			•	•		•			•	•														
74LVC2G00	dual 2-input NAND gate			•	•		•					•		•	•			•	•	•		•		•	
74LVC2G02	dual 2-input NOR gate			•	•		•					•		•	•			•	•	•		•		•	
74LVC2G08	dual 2-input AND gate			•	•		•					•		•	•			•	•	•		•		•	
74LVC2G32	dual 2-input OR gate			•	•		•					•		•	•			•	•	•		•		•	
74LVC2G38	dual 2-input NAND gate; open-drain			•	•	•	•					•		•	•			•	•	•		•		•	
74LVC2G86	dual 2-input EXCLUSIVE-OR gate			•	•		•					•		•	•			•	•	•		•		•	
Configurable																									
74LVC1G57	configurable gate; Schmitt trigger		•		•		•			•	•					•	•				•		•		
74LVC1G58	configurable gate; Schmitt trigger		•		•		•			•	•					•	•				•		•		
74LVC1G97	configurable gate; Schmitt trigger		•		•		•			•	•					•	•				•		•		
74LVC1G98	configurable gate; Schmitt trigger		•		•		•			•	•					•	•				•		•		
74LVC1G99	configurable gate; Schmitt trigger		•		•		•					•			•			•	•	•		•		•	
Level shifters																									
74LVC1T45	single level translating transceiver; 3-state			•	•		•	•		•						•	•				•		•		
74LVCH1T45	single translating transceiver with bus hold; 3-state	•		•	•		•	•		•						•	•				•		•		
74LVC2T45	dual level translating transceiver; 3-state			•	•		•	•						•	•			•	•	•		•		•	
74LVCH2T45	dual translating transceiver with bus hold; 3-state	•		•	•		•	•						•	•			•	•	•		•		•	

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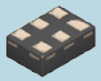
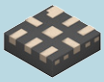
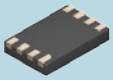
Mini logic packages

Package suffix	GW	GV	GX	GW	GV	GM	GF	GN	GS
	5-pin	5-pin	5-pin	6-pin	6-pin	6-pin	6-pin	6-pin	6-pin
									
Package	SOT353-1	SOT753	SOT1226	SOT363	SOT457	SOT886	SOT891	SO1115	SOT1202
Width (mm)	2.10	2.75	0.80	2.10	2.75	1.00	1.00	1.00	1.00
Length (mm)	2.00	2.90	0.80	2.00	2.90	1.45	1.00	0.90	1.00
Height (mm)	1.00	1.00	0.35	1.00	1.00	0.50	0.50	0.35	0.35
Pitch (mm)	0.65	0.95	0.50	0.65	0.95	0.50	0.35	0.30	0.35

Package suffix	DP	DC	GT	GM	GD	GF	GN	GS
	8-pin	8-pin	8-pin	8-pin	8-pin	8-pin	8-pin	8-pin
								
Package	SOT505-2	SOT765-1	SOT833-1	SOT902-2	SOT996-2	SOT1089	SOT1116	SOT1203
Width (mm)	4.00	3.10	1.00	1.60	3.00	1.00	1.00	1.00
Length (mm)	3.00	2.00	1.95	1.60	2.00	1.35	1.20	1.35
Height (mm)	1.10	1.00	0.50	0.50	0.50	0.50	0.35	0.35
Pitch (mm)	0.65	0.50	0.50	0.50	0.50	0.35	0.30	0.35

Further information about packages can be found at: www.nxp.com/packages/

NOTES

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