

# CD4028B Types

## BCD-to-Decimal Decoder

High-Voltage Types (20-Volt Rating)

■ CD4028B types are BCD-to-decimal or binary-to-octal decoders consisting of buffering on all 4 inputs, decoding logic gates, and 10 output buffers. A BCD code applied to the four inputs, A through D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7 if D = "0". High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

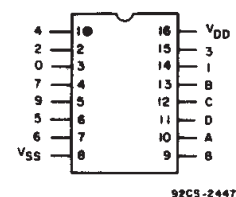
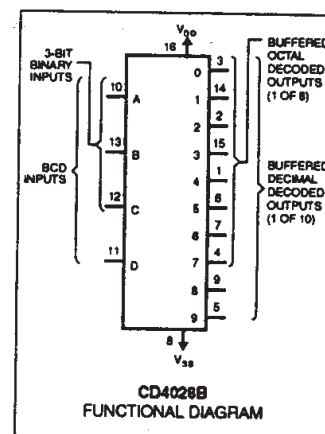
The CD4028B-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

### Features:

- BCD-to-decimal decoding or binary-to-octal decoding
- High decoded output drive capability
- "Positive logic" inputs and outputs. . . . . decoded outputs go high on selection
- Medium-speed operation. . . . .  
 $t_{PHL}, t_{PLH} = 80 \text{ ns (typ.) @ } V_{DD} = 10 \text{ V}$
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of  $1 \mu\text{A}$  at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):  
1 V at  $V_{DD} = 5 \text{ V}$   
2 V at  $V_{DD} = 10 \text{ V}$   
2.5 V at  $V_{DD} = 15 \text{ V}$
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

- Code conversion    ■ Indicator-tube decoder
- Address decoding—memory selection control



Top View  
TERMINAL DIAGRAM

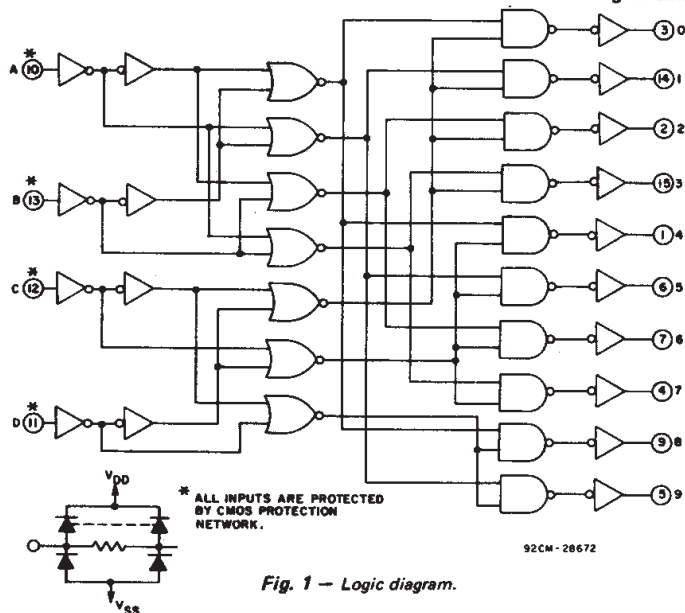


Fig. 1 - Logic diagram.

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )

Voltages referenced to  $V_{SS}$  Terminal) . . . . . -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5V to  $V_{DD} + 0.5\text{V}$

DC INPUT CURRENT, ANY ONE INPUT . . . . .  $\pm 10\text{mA}$

POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For  $T_A = -55^\circ\text{C}$  to  $+100^\circ\text{C}$  . . . . . 500mW

For  $T_A = +100^\circ\text{C}$  to  $+125^\circ\text{C}$  . . . . . Derate Linearly at  $12\text{mW}/^\circ\text{C}$  to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

For  $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$  . . . . . 100mW

OPERATING-TEMPERATURE RANGE ( $T_A$ ) . . . . .  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE ( $T_{stg}$ ) . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance  $1/16 \pm 1/32$  inch ( $1.59 \pm 0.79\text{mm}$ ) from case for 10s max . . . . .  $+265^\circ\text{C}$

TABLE I - TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

1 = HIGH LEVEL

0 = LOW LEVEL

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### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range (For $T_A$ = Full Package Temperature Range)	3	18	V

### STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)					+25			
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current I <sub>OL</sub> Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I <sub>OH</sub> Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	1	—	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V <sub>OH</sub> Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V <sub>IL</sub> Max.	0.5, 4.5	—	5	1.5				—	—	1.5	V
	1, 9	—	10	3				—	—	3	
	1.5, 13.5	—	15	4				—	—	4	
Input High Voltage, V <sub>IH</sub> Min.	0.5, 4.5	—	5	3.5				3.5	—	—	V
	1, 9	—	10	7				7	—	—	
	1.5, 13.5	—	15	11				11	—	—	
Input Current I <sub>IN</sub> Max.	—	0,18	18	±0,1	±0,1	±1	±1	—	±10 <sup>-5</sup>	±0,1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ C$ ,  $C_L = 50$  pF,  
Input  $t_r, t_f = 20$  ns,  $R_L = 200$  k $\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
	$V_{DD}$ (V)	Typ.	Max.	
Propagation Delay Time: $t_{PHL}, t_{PLH}$	5	175	350	ns
	10	80	160	
	15	60	120	
Transition Time $t_{THL}, t_{TLH}$	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, $C_{IN}$	—	5	7.5	pF

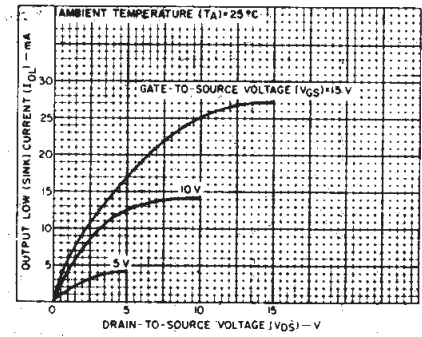


Fig. 2 — Typical output low (sink) current characteristics.

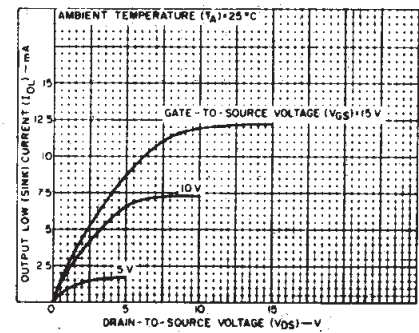


Fig. 3 — Minimum output low (sink) current characteristics.

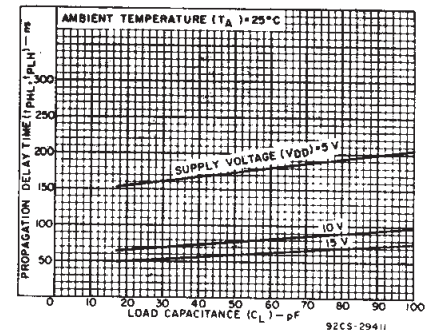


Fig. 4 — Typical propagation delay time as a function of load capacitance.

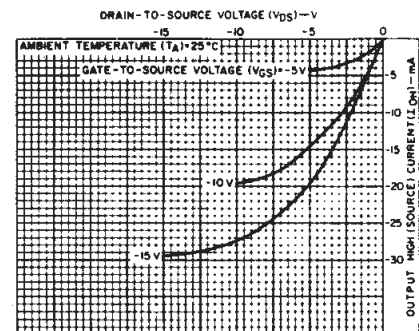


Fig. 5 — Typical output high (source) current characteristics.

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TABLE II – CODE CONVERSION CHART

INPUTS				INPUT CODES						OUTPUT NUMBER																	
				Hexa - Decimal		Decimal																					
				4BIT BINARY	4BIT GRAY	EXCESS-3	EXCESS-3 GRAY	AIKEN	4-2-1																		
D	C	B	A									0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0					0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1					1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	2	3			0	2	2		0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	3	2	0	3	3				0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	4	7	1	4	4				0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	5	6	2			3			0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	6	4	3	1		4			0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	7	5	4	2					0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	8	15	5						0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	9	14	6			5			0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	10	12	7	9		6			0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	11	13	8		5				0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	12	8	9	5	6				0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	13	9		6	7	7			0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	14	11		8	8	8			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	15	10		7	9	9			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

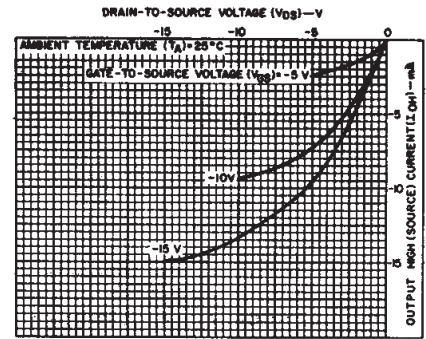


Fig. 6 – Minimum output high (source) current characteristics.

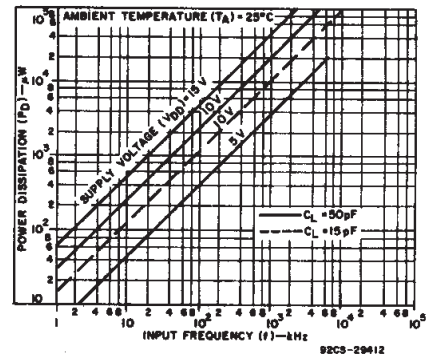


Fig. 7 – Typical dynamic power dissipation as a function of input frequency.

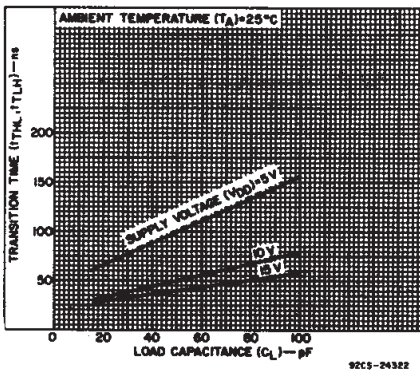


Fig. 8 – Typical transition time as a function of load capacitance.

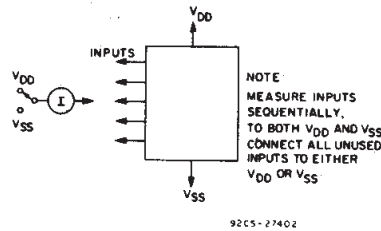


Fig. 9 – Input current test circuit.

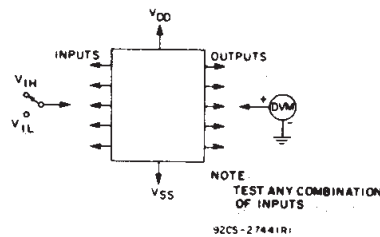


Fig. 11 – Input voltage test circuit.

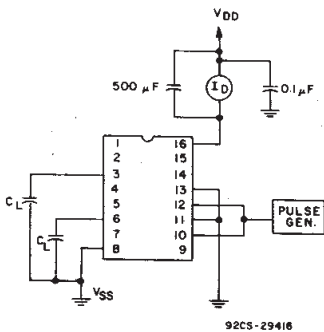


Fig. 10 – Dynamic power dissipation test circuit.

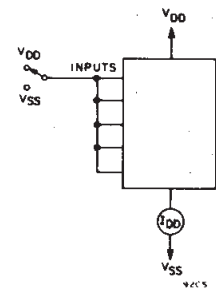


Fig. 12 – Quiescent device current test circuit.

## TYPICAL APPLICATIONS

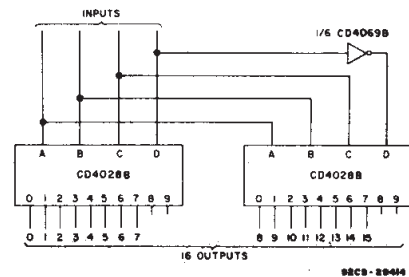
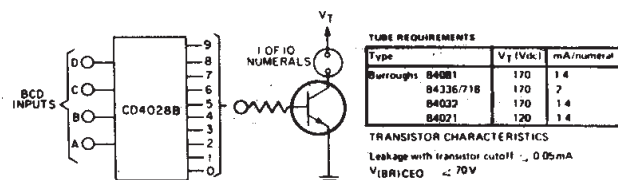


Fig. 13 – Code conversion circuit.

The circuit shown in Fig.13 converts any 4-bit code to a decimal or hexadecimal code. Table 2 shows a number of codes and the decimal or hexadecimal number in these codes which must be applied to the input terminals of the CD4028B to select a particular output. For example: in order to get a high on output No. 8 the input must be either an 8 expressed in 4-Bit Binary code, a 15 expressed in 4-Bit Gray code, or a 5 expressed in Excess-3 code.

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^(Trademark) Burroughs Corp.

92CS-29413

Fig. 14 — Neon readout (Nixie Tube<sup>^</sup>) display application.

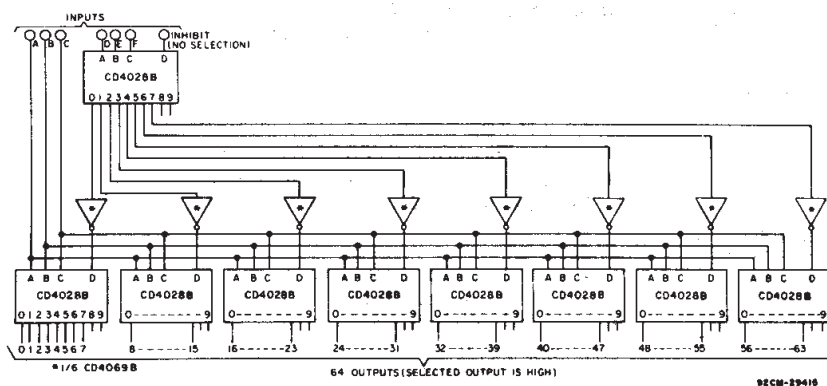
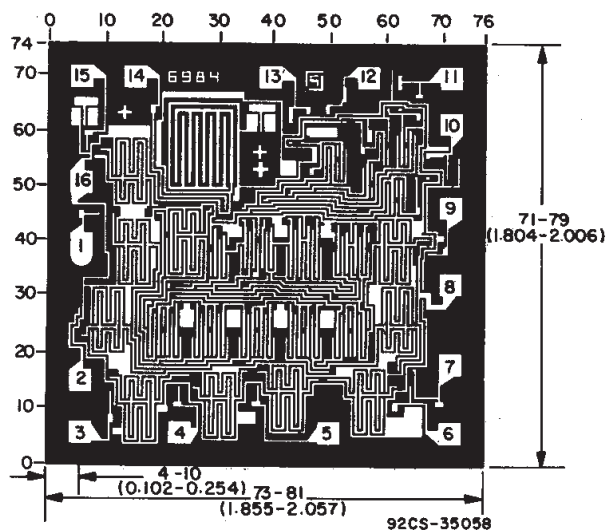


Fig. 15 — 6-bit binary to 1-of-64 address decoder.



CD4028BH  
DIMENSIONS AND PAD LAYOUT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD4028BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4028BF	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4028BF3A	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4028BM	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4028BM96	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4028BMT	ACTIVE	SOIC	D	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4028BNSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4028BPW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4028BPWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

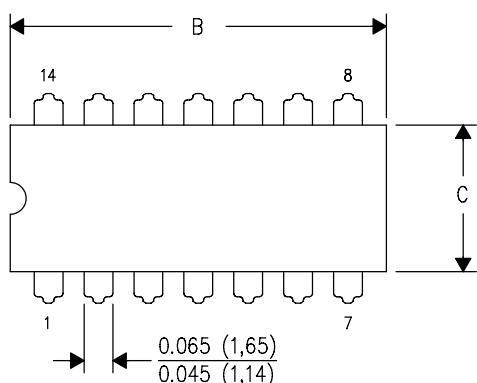
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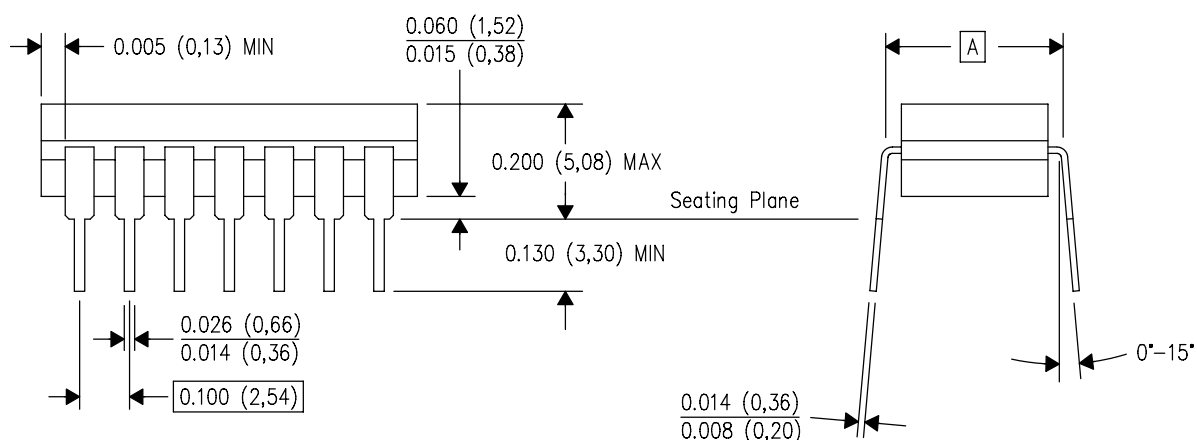
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



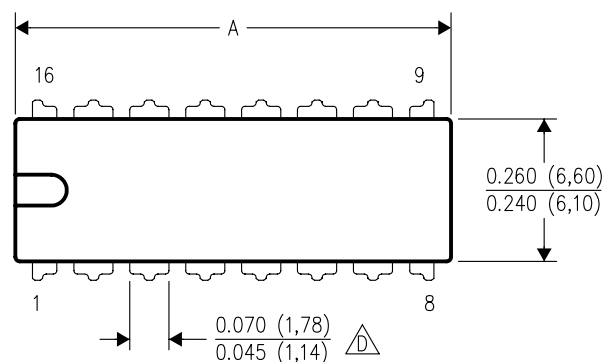
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

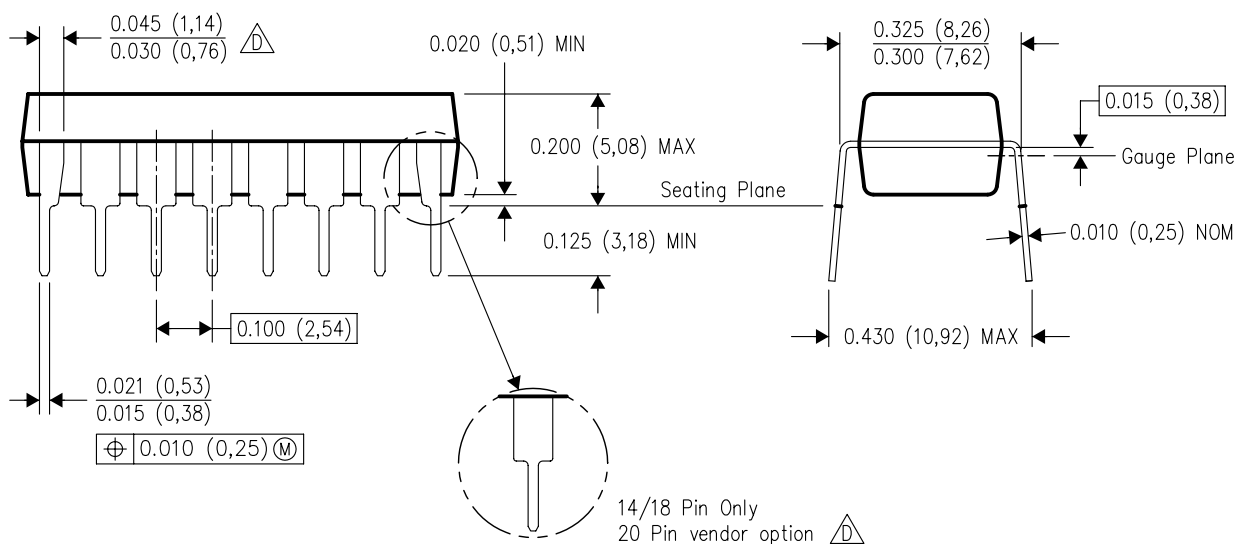
N (R-PDIP-T\*\*)

16 PINS SHOWN



## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

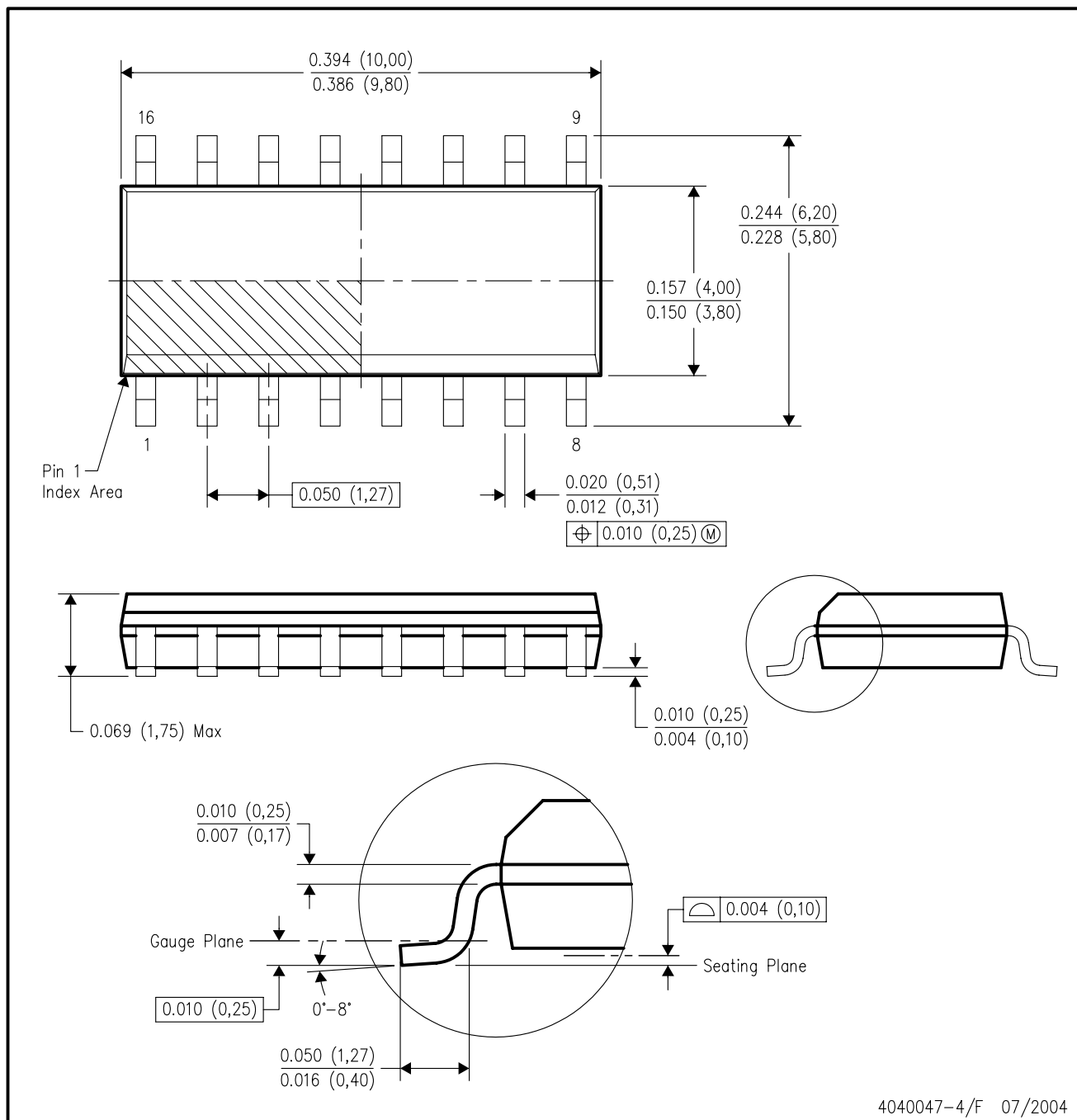


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/F 07/2004

## NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-012 variation AC.

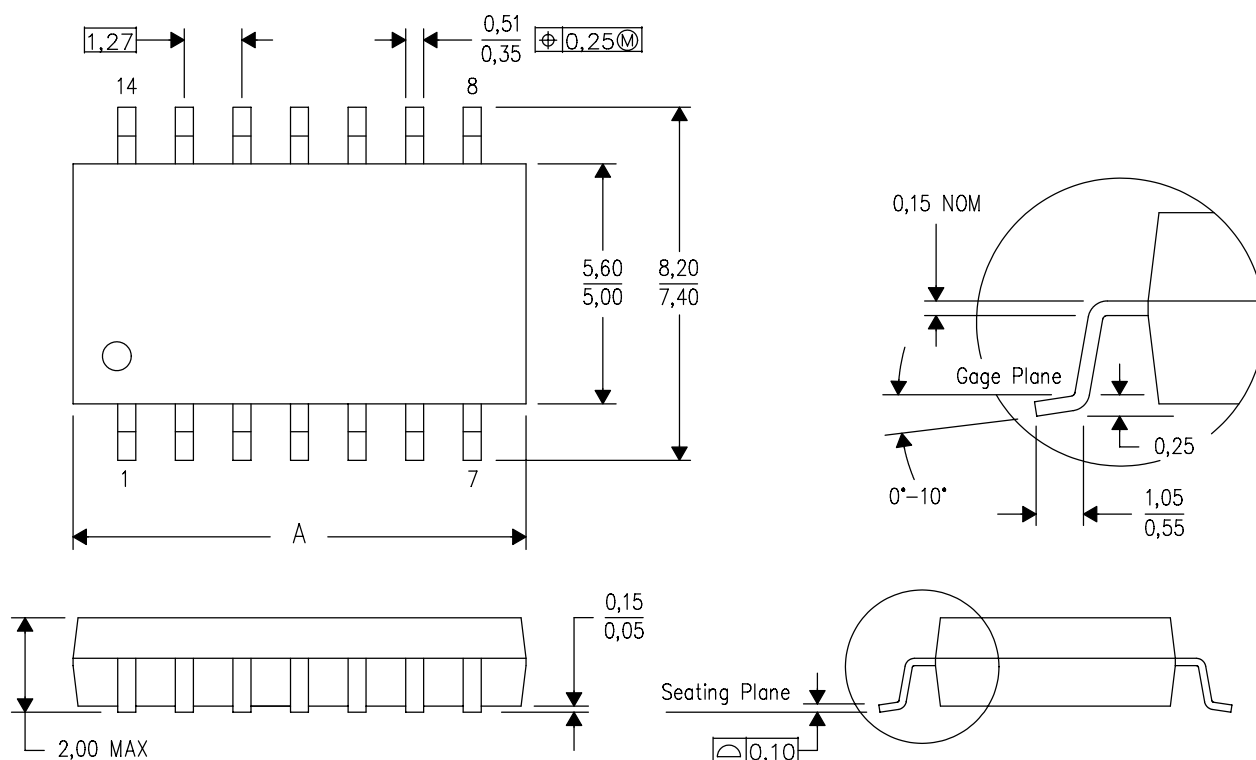


# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

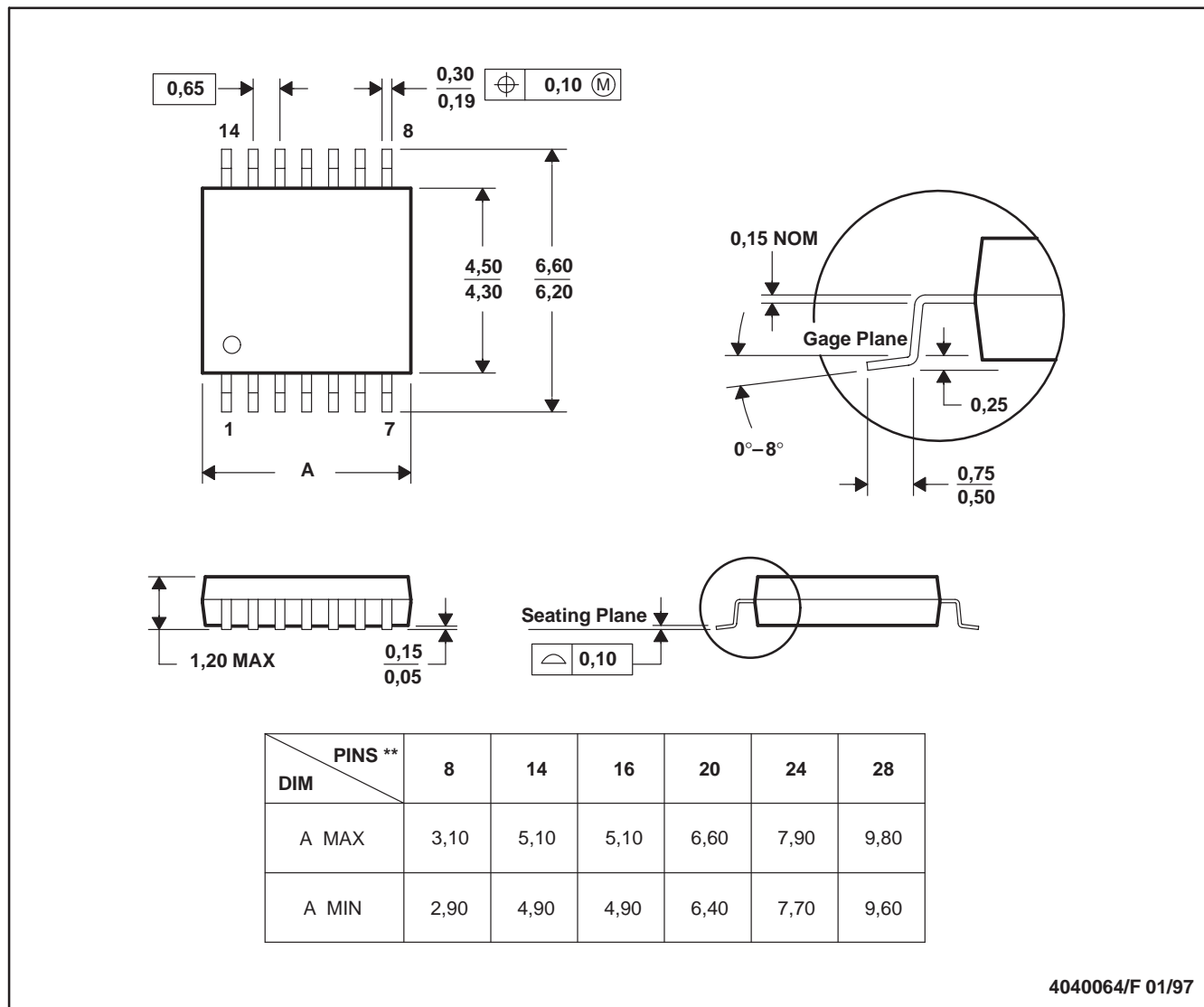
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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