Vittorio Zaccaria

Assistant Professor

I am an assistant professor at Politecnico di Milano and I have worked in processor architecture research and development for one of the top semiconductor companies in the world.
Throughout the years at Politecnico, I discovered that I love teaching by making students passionate about computer engineering. I like matching conventional methods for teaching with novel technology such as live-coding, program simulation and information graphics.

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WORK ADDRESS

RESEARCH AREAS

- Many core architectures
- Power and performance modeling of computer architectures
- Embedded systems
- Machine learning and design space exploration
- Performance optimization
- Novel teaching methods for CS

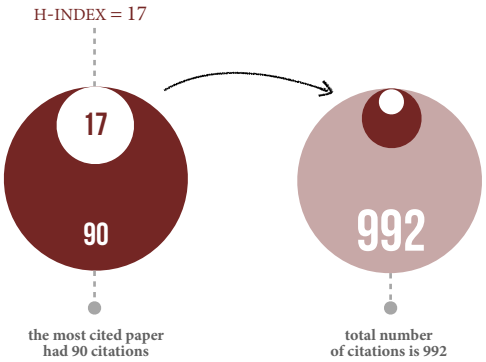
ACHIEVEMENTS

- Journals: 14 (6 TRANSACTIONS)
- Conferences: 36 (3 DAC/ASPDAC) (9 DATE)
- Book Chapters: 10
- Patent applications: 4 (2 GRANTED)
- Books: 1

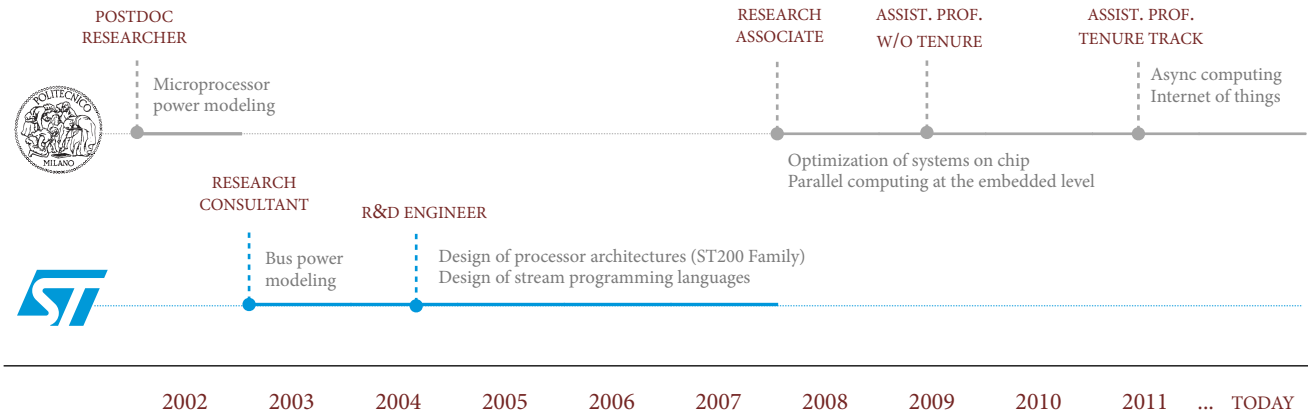
48%
of co-authors are from external institutions

CITATION INDICES*

* Google Scholar, 7 Dec 2013 - Circle area proportional to values



WORK EXPERIENCE



PROFESSIONAL ACTIVITY

INSTITUTIONAL ACTIVITY

- **In 2013 - Member** of the '*commissione per il riconoscimento dei crediti acquisiti dagli studenti decaduti, A.A. 2013/2014*'.
- **Since 2010**, appointed lecturer (***titolare***) of "Informatica B", a 7 credits undergraduate course for mechanical engineers at Politecnico.
- **Since 2007 he co-advised** the work of several Ph.D. students and undergraduate thesis works.

PARTICIPATION TO EUROPEAN PROJECTS

- 2010-2013 — **FP7 project 2PARMA — Leader of tasks 3.3 and 5.4.**
- 2008-2010 — **FP7 project MULTICUBE** — Involved in the **technical management**

AWARDS

- **2010 — Hipeac paper award** for a paper published at the Design Automation Conference
- **2012** — 2nd runner up at the **Idea2Product Global Competition** for creating a valuable opportunity for product commercialization of research results

COLLABORATIONS

- **Multinational companies**: STMicroelectronics, DS2 (now Marvell), Esteco, CoWare (now Synopsys),
- **Research centers:** IMEC (*Belgium*), Fraunhofer Institute (*Germany*)
- **Universities:** University of Cantabria (*Spain*), NTUA (*Greece*)

DEVELOPMENT OF SYSTEMS

- **Project lead of MOST** (MultiObjective System Optimizer), a software technology used by several companies (STM, GMV) and in several european projects, among which CONTREX and 2PARMA
- **Project lead of Multicube Explorer** — an open source processor optimization framework
- **Member of the ST200-ISS team** — a production-grade instruction set simulator for the ST200 VLIW processor family (functional and timing behavior models).
- **Lead developer of Chained** — a library for easily converting *continuation passing style* programs to use *promises.*

VITTORIO ZACCARIA

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EDUCATION

2001: Ph.D. in Computer Engineering (*Dottorato di Ricerca in Ingegneria Informatica e Automatica*), Politecnico di Milano, Italy

1998: Ms. in Computer Engineering (*Laurea in Ingegneria Informatica*), Politecnico di Milano, Italy

CURRENT POSITION

Assistant Professor (tenure-track), Politecnico di Milano, Italy

AREAS OF SPECIALIZATION

Computer aided design of digital circuits with emphasis on multi-processor design space exploration and network-on-chip design, low-power and high-performance design of parallel processor architectures and advanced parallel programming paradigms, compilation and simulation methodologies for multi-processor-based systems.

APPOINTMENTS HELD

2011-today: *Assistant Professor* (tenure-track), Politecnico di Milano, Italy

- Involved in the technical management of the European Project FP7 titled "PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures" (2PARMA).
- Investigating techniques for advanced design space exploration of many-core architectures, response-surface modelling, run-time management, parallel programming models, virtual platform design, audio processing.
- Leading research and development activities for MOST, an advanced tool for design space exploration.

2009-2011: *Assistant Professor* (without tenure), Politecnico di Milano, Italy

- Involved in the technical management of the European Project FP7 titled "PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures" (2PARMA).
- Involved in the management of the European Project FP7 titled "Multi-objective design space exploration of multi-processor SoC architectures for embedded multimedia applications" (MULTICUBE).
- Introducing advanced techniques for managing run-time variability in automatic design space exploration for multi-processors.
- Leading research and development activities for Multicube Explorer, a tool for design space exploration (open-source since 2009).

2007-2009: *Research Associate*, Politecnico di Milano, Italy

- Involved in the management of the European Project FP7 titled "Multi-objective design space exploration of multi-processor SoC architectures for embedded multimedia applications" (MULTICUBE).
- Introduced advanced techniques for managing design of experiments and response surface methods in automatic design space exploration for multi-processors.
- Extended classical design space exploration to tackle the problem of process-variability-aware design of multi-processors.
- Leading research and development activities for Multicube Explorer, an advanced tool for design space exploration (open-source since 2009).
- Leading research and development activities on the *stream programming* paradigm with applications to advanced, parallel architectures such as the IBM Cell and multi-core x86 processors.

2004-2007: *RD Engineer*, STMicroelectronics, Switzerland.

- Architectural specification and development of ST200 processors, including symmetric multi-processing, virtualization and secure storage.
- Development of extensions to industrial network-on-chip architectures.
- Development of the simulation platform infrastructure for the ST200 processor family and streaming architectures.
- Benchmarking of streaming and multi-processor architectures.

2003-2004: *Research Consultant*, STMicroelectronics, Milan.

- High-level modeling and characterization of power consumption of industrial networks-on-chip, among which AMBA and STBUS.
- Development of tools and methodologies for supporting industrial, low-power STBUS network-on-chip.

2002-2002: *Post-Doc Researcher*, Politecnico di Milano

- Investigated power estimation at the system level for systems-on-chip.
- Investigated design space power/performance exploration at the system level for systems-on-chip.

1999-2002: *Ph.D. Candidate*, Politecnico di Milano

- Developed an analytical, micro-processor power consumption model for VLIW architectures.
- Successfully modeled the instruction-level energy consumption of the ST200 processors, jointly designed by HPLabs and STMicroelectronics.
- Defined innovative register file write inhibition schemes that exploit the forwarding paths in VLIW processors for reducing power.
- Specified and implemented novel dynamic power management policies for general purpose operating systems.
- Defined a design exploration framework to enable an efficient fine-tuning of the configurable modules of an embedded system.

GRANTS AND FUNDING

2007-2008: *Research Grant* from Politecnico di Milano.

- Project: "Multi-Objective Design Space Exploration of Multi-Processor SOC Architectures for Embedded Multimedia Applications".

2002: *Post-Doc Grant* from Politecnico di Milano.

- Project: "Power estimation and exploration of the architectural space at the system level for systems-on-chip".

1999-2002: *Ph.D. Fellowship* from STMicroelectronics.

- Project: "Methodologies for Power Estimation for VLIW Machines".

2002: *Young Researcher Grant* from the Italian Government.

- Project "Methodologies for Power Estimation and Optimization in Embedded Processor Systems".

AWARD, PRIZES ACADEMIC HONORS

2012 - *2nd runner up at the Idea2Product Global Competition 2012*

- for creating a valuable opportunity for product commercialization of research results.

2010 - *HiPEAC Paper Award*

- paper "A Correlation-Based Design Space Exploration Methodology for Multiprocessor Systems-on-Chip", by Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Aleksandar Brankovic, Jovana Jovic and Cristina Silvano, published at DAC 2010.

2002 - *Dimitris N. Chorafas Foundation award*

- for the outstanding contribution of his research work to the state of the art

Graduate students co-advised

Since 2001, he co-advised the following students in their Master-equivalent theses:

- Simone Borgio and Davide Bosisio, *OpenStreamC - a development framework for streaming applications*
- Zhong Yi Hu, *Power modeling of Networks-on-chip*
- Fabrizio Lucini, *Specification and design of a prefetch unit for translating code at run-time*
- Simone Valsecchi, *An algorithm for the efficient exploration of the architectural design space for microprocessor-based systems*
- Gianluca Palermo, *A methodology for architectural exploration and information encoding for low-power digital systems*
- Alessandro Molgora and Claudio Lozza, *Low-power state encoding techniques for finite state machines*
- Marco Gavazzi, *Low-power VLIW re-scheduling algorithms*
- Lorenzo Salvemini, *An architectural exploration methodology for low-power digital systems*

- Andrea Bona, *A design of experiments methodology in a power estimation flow for VLIW processors*

He is also technically (though not formally) overseeing (or has overseen) part of the work of the following Ph. D. students:

- Edoardo Paone, Politecnico di Milano
- Giovanni Mariani, ALaRI - University of Lugano
- Fabrizio Castro, Politecnico di Milano.

RESEARCH EXPERIENCE

The principal research activities have been focused on the interaction of architecture, compiler and operating system towards the design of optimal embedded systems under performance and power consumption constraints. The research effort started during the doctoral studies and it has been directed towards the power estimation and optimization of processor based embedded architectures. The competences acquired in this period became a seminal basis for an industrial R&D effort towards the optimal power/performance implementation of a broad range of embedded parallel systems. This research effort spanned several levels of abstraction, from the specification and implementation of parallel and virtualized architectures up to compiler techniques for parallelism extraction.

Power estimation techniques

In this activity he introduced a set of innovative software power estimation methodologies to support the design of low power embedded applications based on high-performance Very Long Instruction Word (VLIW) microprocessors. He developed an analytical model that takes into account several software-level parameters (such as instruction ordering, pipeline stall probability and instruction cache miss probability) as well as micro-architectural-level ones (such as pipeline stage power consumption per instruction) providing an efficient software-based power estimation tool with accuracy very close to those given by RT or gate-level simulation approaches. He applied the instruction-level model to a real world industrial VLIW processor jointly designed by HPLabs and STMicroelectronics. The methodology has then been adopted by STMicroelectronics as a reference work-flow for industrial power estimation.

Power optimization techniques

In this research he defined a novel set of power minimization techniques operating at the hardware, software and system-level. Three main topics have been devised:

- Definition of register file write inhibition scheme that exploits the forwarding paths in VLIW processors.
- Specification and implementation of novel dynamic power management policies for general purpose operating systems.
- Definition of a design exploration framework to enable an efficient fine-tuning of the configurable modules of an embedded system.

The latter topic evolved into a new system-level design methodology for the efficient exploration of the architectural parameters of the memory sub-systems, from the energy-delay joint perspective. The main goal of this methodology is to find the best configuration of the memory hierarchy without performing the exhaustive analysis of the parameters space. In this context, he introduced optimization methodologies ranging from traditional design of experiments and response surface methods to advanced heuristics such as particle swarm optimization. This project has generated innovative methodologies and tools for the multi-objective optimization domain which are still in evolution. The Multicube Explorer analysis framework (see section on Expertise) is an example of such research tools developed in support of this activity.

Parallel systems

In this context, he led two main activities of industrial research and development that eventually produced a set of innovative tools for processor and application design and patents:

- *Specification, validation and architectural exploration for embedded shared-memory multi-processor systems.* This

task has been carried out at several levels of abstraction by developing software tools and models for performance estimation of a cache coherent processor system. Moreover he studied and created new run-time and operating system components including co-hosted infrastructures. The ST200-ISS simulator is one of the research tools developed in support of this activity.

- *Development of stream programming languages and architectures*. During this activity, he studied and created a parallel programming framework for industrial multi-processor architectures. The activity involved the specification and implementation of an advanced parallel language and compiler suitable for developing streaming-based programs for the embedded and cluster-based multi-processor domain. Several prototypes applications such as software radio systems have been developed and currently drive the industrial evolution of this project. The industrial xSTreamC compiler and the nSTream simulator (T2) are the tools developed in support of this activity. The tool has been released in the public domain in September 2008.

Secure systems, cryptography

In this activity, he has been responsible for the specification and implementation of secure storage extensions for embedded processors. He developed software tools and methodologies that are currently used by industrial research and production groups for supporting next generation processors. As a side task, he has also been involved in the study and implementation of performance and power models for cryptographic applications as well as novel cryptographic power attack techniques based on cache-miss induction.

Networks on Chip

In this activity he has led the specification, planning and implementation of the power characterization and high-level power estimation work-flows for the STBus Network on Chip. The STBus is a high-performance, low-latency on chip parameterizable network supported by production grade specification and synthesis tools.

CURRENT RESEARCH GOALS

The research goals that he is currently pursuing are:

Design space exploration of hardware/software systems

Platform-based design represents the most widely used approach to design System-On-Chip (SoC) applications. In this scenario, Design Space Exploration (DSE) allows to find the best trade-offs in terms of the selected figures of merit (e.g. energy consumption, task throughput and area occupation) by efficiently tuning, either at design time or at run-time, the system hardware and software parameters. This research is aimed at defining system models and innovative DSE methodologies to target the following goals:

- Accurate performance and power modeling characterization of applications with emphasis on parallel processors architectures and network-on-chips.

- Optimal tuning of the memory hierarchy, processor parallelism (intra and inter-task) and processor interconnection network.

- Optimal software task mapping and scheduling onto the target processor units and optimal communication scheduling.

- Run-time design space exploration for trading-off quality-of-service with actual power constraints.

- Robust optimization with respect to several levels of uncertainties such as workload variability, model estimation accuracy and manufacturing process variability.

- Power-conscious micro-architectural optimizations.

Methodologies and tools for developing embedded parallel applications

The stream programming paradigm is an emerging technology for developing applications for modern, distributed memory

The stream programming paradigm is an emerging technology for developing applications for modern, distributed memory parallel processors. Several examples of this kind of applications range from MPEG decoders and graphics pipelines to complex base-band elaboration systems and software radios. The current development frameworks (e.g. StreamIt, Brook) lack of efficient interaction with the underlaying physical resources and the operating system, thus being hardly scalable, generalizable and dynamic. This research activity aims at:

- Study a new framework to provide the missing synergy between the operating system, the streaming compiler and the architecture, enabling a wide range of run-time optimizations.
- Create suitable virtualization abstractions of the streaming primitives at the OS level.
- Identify suitable formats for transferring information about the actual data-flows associated to the applications from the compiler to the OS to enable run-time re-mapping and trading-off performance with power consumption.

CURRENT TEACHING GOALS

The teaching goals derive from the past industrial and academic experience and span the interaction of architecture, compiler and operating system towards the design of embedded applications. In this context several course topics can be devised ranging from the analysis and design of parallel architectures up to advanced compilation techniques, for extracting parallelism from a given application, and embedded operating systems for parallel processors. Several subtopics may play a significant role such as hardware/software co-design and parallel programming techniques. An overview of these topics can be introduced in undergraduate courses while an in-depth analysis and study of the state of the art would be introduced at the graduate level.

A strong effort towards the implementation of supporting software tools is planned. Those tools would enable students to gain an in-depth, practical experience on the course topics.

PROFESSIONAL ACTIVITIES

National and international research projects

> **2010-present**

- Actively involved in the technical management of the European Project FP7 titled “PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures” (2PARMA, Project coordinator: Cristina Silvano). In particular he is *development team leader* for MOST, an advanced production-grade language and interpreter supporting design space exploration. He is also overseeing integration activities of design space exploration tools within the context of the project itself.

> **2008-2010**

- Actively involved in the technical management of the European Project FP7 titled “Multi-objective design space exploration of multi-processor SoC architectures for embedded multimedia applications” (MULTICUBE, Project coordinator: Cristina Silvano). In particular he was *development team leader* for Multicube Explorer, an advanced tool for design space exploration of configurable systems.

Conference and workshop organization

- Session chair - System-level Design of Multi-Cores, DATE 2010 - Dresden, Germany.
- Session chair - On-Chip Communic. for Multi-Core Platforms, DATE 09 - Nice, France.
- Local committee, MICRO 2008.

Program committee membership

- The 4th International Workshop on Adaptive Self-tuning Computing Systems, (co-located with HIPEAC 2014).

- TPC, NoCArch 2012.
- Program Co-Chair, 2PARMA 2012 Workshop (co-located with ARCS 2012).
- TPC, 2PARMA 2011 Workshop (co-located with ARCS 2011).
- TPC, NoCArch 2010.
- TPC, 2PARMA 2010 Workshop (co-located with ARCS 2010).
- TPC, DATE 2010 - Track A8 (Multi-Core Platforms).
- TPC, NoCArch 2009.
- TPC, DATE 2009 - Track A8 (Multi-Core Platforms).
- TPC, NoCArch 2008.

Referee services

- IEEE Transactions on Computer Aided Design of Integrated Circuits.
- IEEE Transactions on Very Large Scale of Integration Circuits.
- DATE conference.
- IC-SAMOS and SASP.
- Journal of Low Power Electronics - JOLPE.

INNOVATION, TECHNOLOGY TRANSFER PATENTS

He produced significant public-domain and industrial technology transfer by developing the following projects:

1. *Multicube Explorer* — an architectural exploration framework retargetable to different processor-based architectures and exploration algorithms. The tool contains also advanced algorithms for DoE generation and response surface modeling. It is scheduled to go open-source in January 2009 — open-source.
2. *xSTreamC compiler and nSTream simulator* — a development toolchain for applications based on the stream oriented programming model. The toolchain has been released open-source in October 2008 — open-source.
3. *ST200-ISS* — a production-grade instruction set simulator for the ST200 VLIW processor family (functional and timing behavior models). Kernel, device components, cache-coherency, secure-storage, co-hosting — proprietary.
4. Tools for run-time power estimation of STBus proprietary bus technology (C/SystemC). These tools are currently part of the internal STBus product work-flow — proprietary.

KNOWN LANGUAGES

- Italian: Native
- English: TOEFL iBT Score: **100** (maximum is 120) — January 23, 2009

- French: Basic skills

JOURNALS

1. G. Mariani, G. Palermo, V. Zaccaria and C. Silvano, *ARTE: An Application-specific Run-Time managEment framework for multi-cores based on queuing models*, **Parallel Computing**, pp. 504 to 519 - September 2013. [issn]

2. G. Mariani, G. Palermo, V. Zaccaria and C. Silvano, *Design Space Exploration and Run-time Resource Management for Multi-cores*, **ACM Transactions on Embedded Computing Systems (TECS)**, pp. 20:1 to 20:27 - September 2013. [doi and issn]

3. S. Marceglia, A. Bona, V. Zaccaria, C. Pagliari and F. Pinciroli, *How might the iPad change healthcare?*, **Journal of the Royal Society of Medicine**, pp. 233 to 241 - June 2012. [doi and issn]

4. G. Palermo, C. Silvano and V. Zaccaria, *A Variability-Aware Robust Design Space Exploration Methodology for on-Chip Multiprocessors Subject to Application Specific Constraints*, **ACM Transactions in Embedded Computing Systems**, pp. 29:1 to 29:28 - July 2012. [doi and issn]

5. G. Mariani, G. Palermo, C. Silvano and V. Zaccaria, *OSCAR: an Optimization Methodology Exploiting Spatial Correlation in Multi-core Design Spaces*, **IEEE Transactions on Computer Aided Design of Integrated Circuits**, pp. 740 to 753 - May 2012. [doi and issn]

6. C. Ykman-Couvreur, P. Avasare, G. Mariani, G. Palermo, C. Silvano and V. Zaccaria, *Linking run-time resource management of embedded multi-core platforms with automated design-time exploration*, **Computers Digital Techniques, IET**, pp. 123 to 135 - March 2011. [doi and issn]

7. G. Palermo, C. Silvano and V. Zaccaria, *ReSPIR: A Response Surface-based Pareto Iterative Refinement for Application-Specific Design Space Exploration*, **IEEE Transactions on Computer Aided Design of Integrated Circuits**, pp. 1816 to 1829 - December 2009. [doi and issn]

8. A. Bona, M. Sami, D. Sciuto, C. Silvano, V. Zaccaria and R. Zafalon, *Reducing the Complexity of Instruction-Level Power Models for VLIW Processors*, **Design Automation for Embedded Systems**, pp. 49 to 67 - July 2006. [doi and issn]

9. G. Palermo, C. Silvano and V. Zaccaria, *Multi-Objective Design Space Exploration of Embedded Systems*, **Journal of Embedded Computing**, pp. 305 to 316 - 2005. [issn]

10. C. Silvano, M. Monchiero, G. Palermo, M. Sami, V. Zaccaria and R. Zafalon, *Low-Power Branch Prediction Techniques for VLIW Architectures: A Compiler-Hints Based Approach*, **Integration, The VLSI Journal**, pp. 515 to 524 - January 2005. [doi and issn]

11. M. Sami, D. Sciuto, C. Silvano and V. Zaccaria, *An Instruction-Level Energy Model for Embedded VLIW Architectures*, **IEEE Transactions on Computer Aided Design of Integrated Circuits**, pp. 998 to 1010 - September 2002. [doi and issn]

12. L. Benini, D. Bruni, M. Chinosi, C. Silvano, V. Zaccaria and R. Zafalon, *A Framework for Modeling and Estimating the Energy Dissipation of VLIW-based Embedded Systems*, **Design Automation for Embedded Systems**, pp. 183 to 203 - October 2002. [doi and issn]

13. W. Fornaciari, D. Sciuto, C. Silvano and V. Zaccaria, *A Sensitivity-Based Design Space Exploration Methodology for Embedded Systems*, **Design Automation for Embedded Systems**, pp. 7 to 33 - September 2002. [doi and issn]

14. M. Sami, D. Sciuto, C. Silvano, V. Zaccaria and R. Zafalon, *Low-Power Data Forwarding for VLIW Embedded Architectures*, **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, pp. 614 to 622 - October 2002. [doi and issn]

BOOKS

1. V. Zaccaria, M. Sami, D. Sciuto and C. Silvano, **Power Estimation and Optimization Methodologies for VLIW-based Embedded Systems**, 203 pages - Kluwer Academic Publishers - Boston/Dordrecht/London, April 2003. [isbn]

PATENTS

1. A. Pagni, F. Lucini, D. Pietro Pau, A. Borneo and V. Zaccaria, *Process for translating instructions for an arm-type processor into instructions for a LX-type processor; relative translator device and computer program product* - 2007 - number: **US 7,243,213** - type: **granted** - [url]

2. M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, D. Pietro Pau and R. Zafalon, *Processor architecture* - 2005 - number: **US 6,889,317** - type: **granted** - [url]

3. A. Pagni, F. Lucini, D. Pietro Pau, A. Borneo and V. Zaccaria, *Process for translating instructions for an arm-type processor into instructions for a LX-type processor; relative translator device and computer program product* - 2004 - number: **US 225,869** - type: **(A1 - application)** - [url]

4. M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, D. Pietro Pau and R. Zafalon, *Processor architecture* - 2002 - number: **US 124,155** - type: **(A1 - application)** - [url]

CONFERENCES

1. G. Mariani, G. Palermo, V. Zaccaria and C. Silvano, *DeSpErate: Speeding-up Design Space Exploration by using Predictive Simulation Scheduling*, **Proceedings of DATE 2014: International Conference on Design, Automation and Test in Europe**, **Accepted for publication** (awaiting production).

2. G. Mariani, V. Mihai Sima, G. Palermo, V. Zaccaria, G. Marchiri, C. Silvano and K. Bertels, *Run-time Optimization of a Dynamically Reconfigurable Embedded System Through Performance Prediction*, **Proceedings of FPL 2013: International Conference on Field Programmable Logic and Applications**, pp. 1 to 8 - Porto, Portugal September 2013. [doi]

3. A. Ashouri, V. Zaccaria, S. Xydis, G. Palermo and C. Silvano, *A Framework for Compiler Level Statistical Analysis over Customized VLIW Architecture*, **Proceedings of VLSI-SoC 2013: International Conference on Very Large Scale Integration and System-on-Chip**, pp. 124 to 129 - Instanbul, Turkey October 2013. [doi]

4. E. Paone, N. Vahabi, V. Zaccaria, C. Silvano, D. Melpignano, G. Haugou and T. Lepley, *Improving Simulation Speed and Accuracy for Many-Core Embedded Platforms with Ensemble Models*, **Proceedings of DATE 2013: International Conference on Design, Automation and Test in Europe**, pp. 671 to 676 - March 2013. [isbn]

5. S. Xydis, G. Palermo, V. Zaccaria and C. Silvano, *A Meta-Model Assisted Coprocessor Synthesis Framework for Compiler/Architecture Parameters Customization.*, **Proceedings of DATE 2013: International Conference on Design, Automation and Test in Europe**, pp. 659 - March 2013. [isbn]

6. E. Paone, G. Palermo, V. Zaccaria, C. Silvano, D. Melpignano, G. Haugou and T. Lepley, *An Exploration Methodology for a Customizable OpenCL Stereo-Matching Application Targeted to an Industrial Multi-Cluster Architecture*, **Proceedings of CODES+ISSS 2012: International Conference on Hardware/Software codesign and System Synthesis**, pp. 503 to 512 - 2012. [doi and isbn]

7. G. Mariani, V. Mihai Sima, G. Palermo, V. Zaccaria, C. Silvano and K. Bertels, *Using multi-objective design space exploration to enable run-time resource management for reconfigurable architectures*, **Proceedings of DATE 2012: IEEE Design, Automation and Test Conference in Europe**, pp. 1379 to 1384 - Dresden, Germany March 12-16, 2012. [isbn]

8. C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, E. Speziale, D. Melpignano, J M. Zins, D. Siorpaes, H. Huebert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-Couvreur, A. Bartzas, D. Soudris, T. Kempf, G. Ascheid, H. Meyr, J. Ansari, P. Mahonen and B. Vanthournout, *Parallel Paradigms and Run-time Management Techniques for Many-core Architectures: 2PARMA Approach*, **Proceedings of INDIN 2011: IEEE Conference on Industrial Informatics**, pp. 835 to 840 - Caparicia, Lisbon Portugal July 26-29, 2011. [doi]

9. G. Mariani, G. Palermo, V. Zaccaria and C. Silvano, *ARTE: an Application-specific Run-Time Management Framework for Multi-core Systems*, **Proceedings of SASP 2011: IEEE Symposium on Application Specific Processors**, pp. 86 to 93 - San Diego, CA - USA June 5-6, 2011. [doi]

10. C. Silvano, W. Fornaciari, G. Palermo, V. Zaccaria, F. Castro, M. Martinez, S. Bocchio, R. Zafalon, P. Avasare, G. Vanmeerbeeck, C. Ykman-Couvreur, M. Wouters, C. Kavka, L. Onesti, A. Turco, U. Bondi, G. Mariani, H. Posadas, E. Villar, C. Wu, F. Dongrui, Z. Hao and T. Shibin, *MULTICUBE: Multi-Objective Design Space Exploration of Multi-Core Architectures*, **Proceedings of ISVLSI 2010: IEEE Annual Symposium on VLSI**, pp. 488 to 493 - Lixouri, Kefalonia - Greece July 5-7, 2010. [doi]

11. C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, A Di. Biagio, E. Speziale, M. Tartara, D. Siorpaes, H. Huebert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-Couvreur, A. Bartzas, S. Xydis, D. Soudris, T. Kempf, G. Ascheid, R Leupers H. Meyr, J. Ansari, P. Mahonen and B. Vanthournout, *2PARMA: Parallel Paradigms and Run-time Management Techniques for Many-Core Architectures*, **Proceedings of ISVLSI 2010: IEEE Annual Symposium on VLSI**, pp. 494 to 499 - Lixouri, Kefalonia - Greece July 5-7, 2010. [doi]

12. G. Mariani, A. Brankovic, J. Jovic, G. Palermo, V. Zaccaria and C. Silvano, *A Correlation-based Design Space Exploration Methodology for Multi-Processor Systems-on-Chip*, **Proceedings of DAC 2010: Design Automation Conference**, pp. 120 to 125 - Anaheim, CA - USA June 13-18, 2010. [doi]

13. A. Gellert, A. Florea, L. Vintan, G. Palermo, V. Zaccaria and C. Silvano, *Energy-Performance Design Space Exploration of SMT Architectures Exploiting Selective Load Value Predictions*, **Proceedings of DATE 2010: IEEE Design, Automation and Test Conference in Europe**, pp. 271 to 274 - Dresden, Germany March 8-12, 2010. [isbn]

14. G. Mariani, P. Avasare, G. Vanmeerbeeck, C. Ykman-Couvreur, G. Palermo, C. Silvano and V. Zaccaria, *An industrial design space exploration framework for supporting run-time resource management on multi-core systems*, **Proceedings of DATE 2010: IEEE Design, Automation and Test Conference in Europe**, pp. 196 to 201 - Dresden, Germany March 8-12, 2010. [isbn]

15. G. Mariani, G. Palermo, C. Silvano and V. Zaccaria, *A Design Space Exploration Methodology Supporting Run-Time Resource Management for Multi-Processors System on-Chip*, **Proceedings of IEEE Symposium on Application Specific Processors 2009**, pp. 21 to 28 - San Francisco, CA - USA July 27-28, 2009. [doi]

16. G. Mariani, G. Palermo, C. Silvano and V. Zaccaria, *Meta-model Assisted Optimization for Design Space Exploration of Multi-Processor Systems-on-Chip*, **Proceedings of Euromicro Conference on Digital System Design (DSD)**, pp. 383 to 389 - Patras, Greece August 27-29, 2009. [doi]

17. G. Mariani, G. Palermo, C. Silvano and V. Zaccaria, *Multiprocessor System-on-Chip Design Space Exploration based on Multi-level Modeling Techniques*, **Proceedings of IEEE IC-SAMOS'09 - International Conference on Embedded Computer Systems: Architectures, MOdeling, and Simulation**, pp. 118 to 124 - Samos, Greece July 20-23, 2009. [doi]

18. G. Palermo, C. Silvano and V. Zaccaria, *Variability-Aware Robust Design Space Exploration of Chip Multiprocessor Architectures*, **Proceedings of IEEE/ACM ASPDAC 2009: Asia and South Pacific Design Automation Conference**, pp. 323 to 328 - Yokohama, Japan January 19-22, 2009. [doi]

19. G. Mariani, G. Palermo, C. Silvano and V. Zaccaria, *An Efficient Design Space Exploration Methodology for Multi-Cluster VLIW Architectures based on Artificial Neural Networks*, **Proceedings of IFIP VLSI-SOC 2008: International Conference on Very Large Scale Integration**, pp. 213 to 218 - Rhodes Island, Greece October 13-15,

2008.

20. G. Palermo, C. Silvano and V. Zaccaria, *Discrete Particle Swarm Optimization for Multi-objective Design Space Exploration*, **Proceedings of DSD 2008: IEEE Euromicro Conference on Digital System Design Architectures, Methods and Tools**, pp. 641 to 644 - Parma, Italy September 2-5, 2008. [doi]

21. G. Palermo, C. Silvano and V. Zaccaria, *An Efficient Design Space Exploration Methodology for Multiprocessor SoC Architectures based on Response Surface Methods*, **Proceedings of IC-SAMOS 2008: International Conference on Embedded Computer Systems Architectures, Modeling and Simulation**, pp. 150 to 157 - Samos, Greece July 21-24, 2008. [doi]

22. G. Palermo, C. Silvano and V. Zaccaria, *An Efficient Design Space Exploration Methodology for On-Chip Multiprocessors Subject to Application-Specific Constraints*, **Proceedings of SASP 2008: IEEE Symposium on Application Specific Processors**, pp. 75 to 82 - Anaheim, CA - USA June 8-9, 2008. [doi]

23. G. Bertoni, V. Zaccaria, L. Breveglieri, M. Monchiero and G. Palermo, *AES Power Attack Based on Induced Cache Miss and Countermeasure*, **Proceedings of ITCC 2005: International conference on Information Technology**, pp. 586 to 591 - Las Vegas, NV - USA April 4-6, 2005. [doi]

24. A. Bona, V. Zaccaria and R. Zafalon, *System Level Power Modeling and Simulation of High-End Industrial Network-on-Chip*, **Proceedings of DATE 2004: IEEE Design, Automation and Test Conference in Europe**, pp. 318 to 323 - Paris - France February 16-20, 2004. [doi]

25. M. Monchiero, G. Palermo, M. Sami, C. Silvano, V. Zaccaria and R. Zafalon, *Power-Aware Branch Prediction Techniques: A Compiler-Hints Based Approach for VLIW Processors*, **Proceedings of GLSVLSI 2004: Great Lakes Symposium on VLSI**, pp. 440 to 443 - Boston, MA - USA April 26-28, 2004. [doi]

26. G. Palermo, C. Silvano and V. Zaccaria, *Power-Performance System-Level Exploration of a MicroSPARC2-Based Embedded Architecture*, **Proceedings of DATE 2003 Designers Forum: IEEE Design, Automation and Test Conference in Europe**, pp. 20182 - Munich, Germany March 3-7, 2003. [doi]

27. G. Bertoni, A. Bircan, L. Breveglieri, P. Fragneto, M. Macchetti and V. Zaccaria, *About the performance of the advanced encryption standard in embedded systems with cache memory*, **Proceedings of ISCAS 2003: IEEE Int. Symposium on Circuits and Systems**, pp. 145 to 148 - Bangkok, Thailand May 25-29, 2003. [doi]

28. G. Palermo, C. Silvano, S. Valsecchi and V. Zaccaria, *A System-Level Methodology for Fast Multi-Objective Design Space Exploration*, **Proceedings of GLSVLSI 2003: Great Lakes Symposium on VLSI**, pp. 92 to 95 - Washington, DC - USA April 28-29, 2003. [doi]

29. G. Palermo, C. Silvano, V. Zaccaria and R. Zafalon, *Branch Prediction Techniques for Low-Power VLIW Processors*, **Proceedings of GLSVLSI 2003: Great Lakes Symposium on VLSI**, pp. 225 to 228 - Washington, DC - USA April 28-29, 2003. [doi]

30. L. Salvemini, M. Sami, D. Sciuto, C. Silvano, V. Zaccaria and R. Zafalon, *A Methodology for the Efficient Architectural Exploration of Energy-Delay Trade-offs for Embedded Systems*, **Proceedings of SAC 2003: Symposium on Applied Computing**, pp. 672 to 678 - Melbourne, FL - USA March 9-12, 2003. [doi and isbn]

31. A. Bona, M. Sami, D. Sciuto, C. Silvano, V. Zaccaria and R. Zafalon, *Energy estimation and optimization of embedded VLIW processors based on instruction clustering*, **Proceedings of DAC 2002: Design Automation Conference**, pp. 886 to 891 - New Orleans, LA - USA June 10-14, 2002. [doi]

32. A. Bona, M. Sami, D. Sciuto, C. Silvano, V. Zaccaria and R. Zafalon, *An instruction-level methodology for power estimation and optimization of embedded VLIW cores*, **Proceedings of DATE 2002: IEEE Design, Automation and Test Conference in Europe**, pp. 1128 to 1128 - Paris, France March 4-8, 2002. [doi]

33. W. Fornaciari, D. Sciuto, C. Silvano and V. Zaccaria, *A Design Framework to Efficiently Explore Energy-Delay Tradeoffs*, **Proceedings of CODES 2001: 9th ACM/IEEE International Symposium on Hardware/Software Co-**

Design, pp. 260 to 265 - Copenhagen, Denmark April 25-27, 2001. [doi]

34. W. Fornaciari, D. Sciuto, C. Silvano and V. Zaccaria, *Fast System-Level Exploration of Memory Architectures Driven by Energy-Delay Metrics*, **Proceedings of ISCAS 2001: IEEE Int. Symposium on Circuits and Systems**, pp. 502 to 505 - Sydney, Australia May 6-9, 2001. [doi]

35. M. Sami, D. Sciuto, C. Silvano, V. Zaccaria and R. Zafalon, *Exploiting Data Forwarding to Reduce the Power Budget of VLIW Embedded Processors*, **Proceedings of DATE 2001: IEEE Design, Automation and Test Conference in Europe**, pp. 252 to 257 - Munich, Germany March 13-16, 2001. [doi]

36. M. Sami, D. Sciuto, C. Silvano and V. Zaccaria, *Instruction-Level Power Estimation for Embedded VLIW Cores*, **Proceedings of CODES-2000: 8th ACM/IEEE International Workshop on Hardware/Software Co-Design**, pp. 34 to 38 - San Diego, CA - USA May 3-5, 2000. [doi]

37. M. Sami, D. Sciuto, C. Silvano and V. Zaccaria, *Power Exploration for Embedded VLIW Architectures*, **Proceedings of ICCAD-2000: IEEE/ACM Int. Conference on Computer Aided Design**, pp. 498 to 503 - San Jose, CA - USA November 5-9, 2000. [doi]

BOOK CHAPTERS

1. C. Silvano, W. Fornaciari, G. Palermo, V. Zaccaria, F. Castro, M. Martinez, S. Bocchio, R. Zafalon, P. Avasare, G. Vanmeerbeeck, C. Ykman-Couvreur, M. Wouters, C. Kavka, L. Onesti, A. Turco, U. Bondi, G. Mariani, H. Posadas, E. Villar, C. Wu, F. Dongrui, Z. Hao and T. Shibin, *MULTICUBE: Multi-Objective Design Space Exploration of Multi-Core Architectures*, **Lecture Notes in Electrical Engineering, Vol. 57 - Selected Papers from VLSI 2010 Annual Symposium, N. Voros et al. (Eds.)**, pp. 47 to 63 - 2011. [isbn]

2. C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, A Di. Biagio, E. Speziale, M. Tartara, D. Melpignano, J M. Zins, D. Siorpaes, H. Huebert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-Couvreur, A. Bartzas, S. Xydis, D. Soudris, T. Kempf, G. Ascheid, R Leupers H. Meyr, J. Ansari, P. Mahonen and B. Vanthournout, *2PARMA: Parallel Paradigms and Run-time Management Techniques for Many-Core Architectures*, **Lecture Notes in Electrical Engineering, Vol. 57 - Selected Papers from VLSI 2010 Annual Symposium, N. Voros et al. (Eds.)**, pp. 65 to 79 - 2011. [isbn]

3. G. Mariani, C. Ykman-Couvreur, P. Avasare, G. Vanmeerbeeck, G. Palermo, C. Silvano and V. Zaccaria, *Design Space Exploration for Run-time Management of a Reconfigurable System for Video Streaming*, **Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.)**, pp. 189 to 204 - 2011. [isbn]

4. C. Kavka, L. Onesti, E. Rigoni, A. Turco, S. Bocchio, F. Castro, G. Palermo, C. Silvano, V. Zaccaria, G. Mariani, F. Dongrui, Z. Hao and T. Shibin, *Design Space Exploration of Parallel Architectures*, **Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.)**, pp. 171 to 187 - 2011. [isbn]

5. P. Avasare, C. Ykman-Couvreur, G. Vanmeerbeeck, G. Mariani, G. Palermo, C. Silvano and V. Zaccaria, *Design Space Exploration Supporting Run-Time Resource Management*, **Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.)**, pp. 93 to 107 - 2011. [isbn]

6. G. Palermo, C. Silvano, V. Zaccaria, E. Rigoni, C. Kavka, A. Turco and G. Mariani, *Response Surface Modeling for Design Space Exploration of Embedded Systems*, **Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.)**, pp. 75 to 91 - 2011. [isbn]

7. E. Rigoni, C. Kavka, A. Turco, G. Palermo, C. Silvano, V. Zaccaria and G. Mariani, *Optimization Algorithms for Design Space Exploration of Embedded Systems*, **Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.)**, pp. 51 to 73 - 2011. [isbn]

8. C. Silvano, W. Fornaciari, G. Palermo, V. Zaccaria, F. Castro, M. Martinez, S. Bocchio, R. Zafalon, P. Avasare, G. Vanmeerbeeck, C. Ykman-Couvreur, M. Wouters, C. Kavka, L. Onesti, A. Turco, U. Bondi, G. Mariani, H. Posadas, E. Villar, C. Wu, F. Dongrui and Z. Hao, *The MULTICUBE Design Flow*, **Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.)**, pp. 3 to 17 - 2011. [isbn]

9. G. Bertoni, L. Breveglieri, M. Monchiero, G. Palermo and V. Zaccaria, *A Power Attack Methodology to AES Based on Induced Cache Misses: Procedure, Evaluation and Possible Countermeasures*, **New Trends in Cryptographic Systems, N. Nedjah and L.M. Mourelle (Eds.)**, pp. 37 to 52 - 2006. [isbn]

10. A. Bona, V. Zaccaria and R. Zafalon, *System Level Power Modeling and Simulation of High-End Industrial Network-on-Chip*, **Ultra Low-Power Electronics and Design, E. Macii (ed.)**, pp. 233 to 254 - 2004. [isbn]

WORKSHOPS

1. C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, E. Speziale, D. Melpignano, J.M. Zins, H. Hubert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-Couvreur, I. Anagnostopoulos, A. Bartzas, D. Soudris, T. Kempf, G. Ascheid, J. Ansari, P. Mahonen and B. Vanthournout, *Parallel paradigms and run-time management techniques for many-core architectures: the 2PARMA approach*, **Proceedings of INA-OCMC 2012: Interconnection Network Architecture: On-Chip, Multi-Chip**, pp. 39 to 42 - Paris, France January 2012. [doi and isbn]

2. G. Mariani, G. Palermo, V. Zaccaria and C. Silvano, *Evaluating Run-time Resource Management Policies for Multi-core Embedded Platforms with the EMME Evaluation Framework*, **Proceedings of the ARCS Workshops 2012**, pp. 363 to 374 - February 2012. [isbn]

3. C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, E. Speziale, D. Melpignano, J.M. Zins, H. Hubert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-Couvreur, I. Anagnostopoulos, A. Bartzas, D. Soudris, T. Kempf, G. Ascheid, J. Ansari, P. Mahonen and B. Vanthournout, *Invited paper: Parallel programming and run-time resource management framework for many-core platforms: The 2PARMA approach*, **Proceedings of ReCoSoC 2011: Reconfigurable Communication-centric Systems-on-Chip**, pp. 1 to 7 - June 2011. [doi]

4. D. Matos, G. Palermo, V. Zaccaria, C. Reinbrecht, A. Susin, C. Silvano and L. Carro, *Floorplanning-aware design space exploration for application-specific hierarchical networks on-chip*, **Proceedings of NoCArc 2011: 4th International Workshop on Network on Chip Architectures**, pp. 31 to 36 - Porto Alegre, Brazil December 4-5, 2011. [doi]

5. V. Zaccaria, G. Palermo, F. Castro, C. Silvano and G. Mariani, *Multicube Explorer: An Open Source Framework for Design Space Exploration of Chip Multi-Processors*, **Proceedings of 2PARMA: Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures**, pp. 325 to 331 - Hannover, Germany February 22, 2010. [isbn]

6. A Dhutta. Choudury, G. Palermo, C. Silvano and V. Zaccaria, *Yield Enhancement by Robust Application-specific Mapping on Network-on-Chips*, **Proceedings of NoCArc '09: International Workshop on Network on Chip Architectures**, pp. 37 to 42 - New York, NY - USA December 12, 2009. [doi]

7. G. Palermo, C. Silvano and V. Zaccaria, *A DoE/RSM-based Strategy for an Efficient Design Space Exploration targeted to CMPs*, **Proceedings of RAPIDO 2009: Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools** - Paphos, Cyprus January 25, 2009.

8. V. Zaccaria, *Data Flow Deadlock Avoidance for Streaming Applications Mapped on Network-on-Chips*, **Workshop on Streaming Systems: From Web and Enterprise to Multicore (in conjunction with IEEE/ACM Micro-41), Como, Italy** - November 8, 2008.

9. G. Palermo, C. Silvano and V. Zaccaria, *Robust Optimization of SoC Architectures: A Multi-Scenario Approach*,

Proceedings of ESTIMEDIA 2008: IEEE/ACM/IFIP Workshop on Embedded Systems for Real-Time Multimedia, pp. 7 to 12 - Atlanta, GA - USA October 23-24, 2008. [doi]

10. A. Bona, V. Zaccaria and R. Zafalon, *Low Effort, High Accuracy Network-on-Chip Power Macro Modeling*, **Proceedings of PATMOS 2004: IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation**, pp. 541 to 552 - Isle of Santorini, Greece September 15-17, 2004. [doi]

11. G. Palermo, C. Silvano and V. Zaccaria, *A Flexible Framework for Fast Multi-Objective Design Space Exploration of Embedded Systems*, **Proceedings of PATMOS 2003: IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation**, pp. 249 to 258 - Torino, Italy September 10-12, 2003. [doi]

12. L. Benini, D. Bruni, M. Chinosi, C. Silvano, V. Zaccaria and R. Zafalon, *A Power Modeling and Estimation Framework for VLIW-based Embedded Systems*, **Proceedings of PATMOS 2001: IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation** - Yverdon-les-Bains, Switzerland September 26-28, 2001.

13. W. Fornaciari, V. Piuri, A. Prestileo and V. Zaccaria, *An Agent-based Approach to Full Interoperability and Allocation Transparency in Distributed File Systems*, **Proceedings of MATA 2001: Third International Workshop On Mobile Agents For Telecommunication Applications**, pp. 153 to 162 - Monreal, Canada August 14-16, 2001. [doi]