# Textured Mesh Reconstruction of Indoor Environments Using RGB-D Camera

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*Dr. Daniel D. Lee*
Supervisor of Thesis

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*Dr. Camillo J. Taylor*
Graduate Group Chairperson

# Abstract

Your abstract goes here... ...

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# Chapter 1

# Introduction

## 1.1 Motivation and Goals

As robots continue to be incorporated into human environments, the need for intelligent and high-speed reasoning about the objects around them increases dramatically. At the simplest level, mobile robots need to create a map of their environment for navigation. At a higher level, some robots need to recognize distinct objects in their environment, track object movement, and have some intuitive sense of object geometry that is easily stored and processed. Even more importantly, robots must be able to efficiently generate adaptable models of their environment, or worldview, from sensor data in real time. Many different methods for representing the world have been proposed and implemented, and they will be discussed below in more detail. Like the human brain, the robot should also be able to perform these low level functions with only minimal intervention from higher cognitive functions. Such technology also has potential uses beyond robotics. Applications may include easily modeling indoor

environments for interior design concepts, generating 3D tours or maps for various buildings, or low resolution rough mapping of archaeological excavations.

This thesis is intended to work towards such a system based on RGB-D cameras, triangle meshes, and the powerful parallel computing capability modern Graphics Processing Units (GPUs) offer. RGB-D cameras like Microsoft's Kinect provide a great low cost solution for capturing 3D environments. Triangle meshes are efficient to store, simple to manipulate and refine, and very versatile. Meshes have the added benefit of being well suited to GPU hardware (which was originally designed for just that purpose). This thesis lays out a robust, high-speed GPU based pipeline that converts raw RGB and depth frames into a 3D textured mesh representation of large planar surfaces in the field of view.

## 1.2  Related Work

A great variety of methods have been applied to RGB-D camera data in an effort to construct a coherent worldview. Each has advantages and disadvantages.

### 1.2.1  Worldview Storage Models

**Point Cloud Models**   The simplest approach to storing RGB-D data is as a raw point cloud. Each point is stored in a self contained data structure containing at least the point's position and color information. E.g.

$$P_i = \{pos_x, pos_y, pos_z, red, green, blue\}$$

This approach allows a complete record of the raw data to be stored very easily, but the size of the data stored will grow very quickly, and simply storing the data linearly results in very slow queries.

Nearest neighbor approximations have recently become a popular approach for speeding queries on large point clouds[20]. However, achieving reliably fast queries usually requires some form of hierarchical tree structure like K-d trees[23] or octrees[41]. K-d trees are much more adaptable and usually more efficient in terms of memory storage, but octrees have a significant advantage when it comes to incrementally building a point cloud because points can very easily be inserted into the appropriate octree leaf node with no duplication or restructuring. K-d trees are better suited for compressing point clouds offline.

**Voxel Space Models**   Perhaps the most robust and impressive real-time surface reconstruction algorithm to date is Microsoft's Kinect Fusion[21, 13]. An open source implementation called KinFu is also available[28]. Kinect Fusion uses a bounded 3D voxel space where each voxel stores the distance to the nearest detected surface or empty space (the default). Figure 1.1 shows the workflow of the Kinect Fusion system. The point cloud generated by each RGB-D frame is projected into the voxel space and each point updates nearby voxels' distance to nearest surface metric. Implicit surfaces can then be rendered by raycasting through the voxel space and detecting the distance sign crossover point. This results in very high resolution and fidelity reconstructions of the implicit surfaces in the environment. The primary disadvantage of this approach is the workspace size is limited by memory and compute resources which scale with

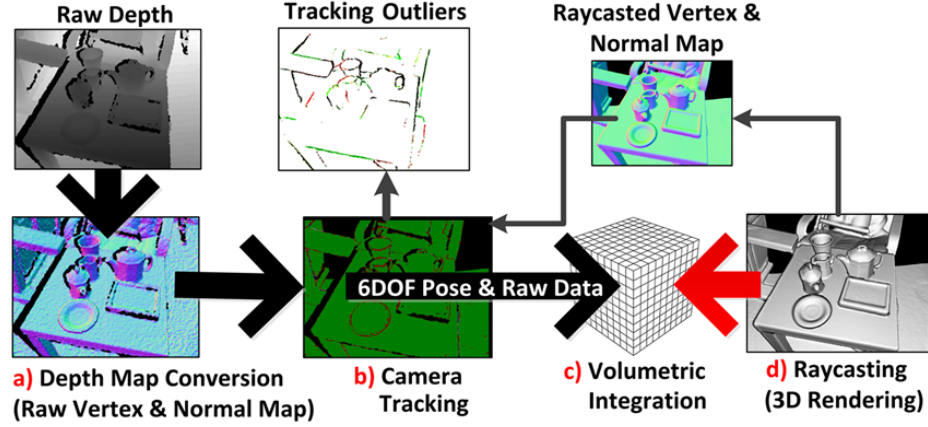the resolution and dimensions of the voxel space.



Figure 1.1: Kinect Fusion Tracking and Reconstruction Pipeline. Reproduced from[13]

A spacial extension of this system called Kintinuous was introduced in 2012[40, 1]. Kintinuous uses a mobile voxel space which periodically relocates based on camera motion. Voxels that move outside the space are converted to a triangular mesh using a greedy mesh triangulation procedure described by Marton *et al.*[19].

Others have attempted to use sparse voxel octrees (SVOs) to represent larger unbounded spaces using voxels of varying resolution[16, 31]. This approach is very amenable to human environments like buildings which are dominated by free space. However, all of these approaches are still limited to storing discrete data points and contain no inherent information about coherent objects or regions.

**Point Cloud Offline Processing** Point clouds can also be processed offline to extract surfaces and objects. These systems are not burdened by the strict requirements of real-time computation so they generally can produce more globally optimal solutions than their online counterparts. These systems generally target unordered

point clouds. Marton *et al.* proposed an incremental approach to triangulation of noisy point clouds[19]. The approach was amenable to introduction of new registered RGB-D frames by only triangulating points that did not correlate with existing mesh models, but the implementation was far too slow for real-time applications. Ma and Others have introduced a system for planar simplification of dense point clouds using a QuadTree based algorithm[18, 17] and texture maps. This thesis will rely heavily on this innovation. Other approaches worked towards implicit surfaces like parameterized smooth surface fits [12] or Poisson surfaces[14, 5].

### 1.2.2 Real-Time Processing

A crucial part of this thesis is achieving high speed plane segmentation. Many different researchers have created efficient parallel GPU implementations of common segmentation approaches like Markov Random Fields[3], the Potts model[2], parallelized graph-based approaches[39], seeded region growth (SRG)[27], and region growth based on local smoothness constraints[30]. However, this thesis parallelizes an algorithm by Holz *et al.* [10] based on clustering in normal space. This approach is superior for application in this thesis because it can readily detect large planes and solve them globally in a very data parallel manner.

### 1.2.3 Additional Resources

Although this thesis focuses on detecting and representing only planar elements, the envisioned worldview generating pipeline would need several additional components

and capabilities to be successful. Additionally, many data processing technologies exist that can improve the quality of the input data through more sophisticated filtering.

**RGB-D Filtering**  The Kinect sensor provides its own set of filtering challenges. Khoshelham and Elberink provided a very useful in depth analysis of Kinect accuracy and resolution specifically with indoor mapping applications in mind[15]. Without some amount of preprocessing and filtering, quantization of the depth data and the fact that resolution and accuracy decrease with increasing distance from the sensor would completely prevent this thesis's pipeline from producing any usable results.

This thesis uses bilateral filtering of the depth image[26, 36]. A simple Gaussian filter is used to smooth local point normals, but other methods exist that could improve results if they could be implemented efficiently in parallel. One such method is adaptively computing filter windows using integral images[11]. Kinect data also is notoriously full of holes from washed out areas, shadows and other noise related effects. Some research makes an effort to fill these holes[6, 33, 42], but this thesis is geared towards progressive improvement of the world model and hopes that any holes will be patched by other viewing angles.

**3D SLAM**  This thesis only deals with processing the current frame, but it was designed with an eye towards creating a closed loop system to integrate data from multiple frames. To accomplish this, a Simultaneous Localization and Mapping (SLAM) system will be needed. SLAM has been practically implemented using a Kinect using

a GPU [35, 34]. Whelan *et al* did fantastic work in comparing multiple SLAM methods combining RGB feature tracking and full point cloud registration algorithms[1].

**Mesh Processing and Modification**   One future direction for this work is to incorporate new information into existing meshes through efficient topology changes and resolution modification. The graphics community offers a wide range of insight into these methods, ranging from tracking surfaces through complex topology evolution[4], modeling deformable solids[32], Mesh subdivision and simplification approaches[29], and texture re-mapping or the effects of image warping[9, 8, 38, 25, 7].

## 1.3   Thesis Organization

The remainder of this thesis is organized as follows. Chapter 2 will review some basic precepts of parallel algorithm design, along with specific optimization considerations for programming GPUs with CUDA. Chapter 3 will provide an overview of the system design as well as break down the pipeline into sub-modules to be explored in much more detail in Chapter 4. Finally, Chapters 5 and 6 will provide performance analysis, conclusions, and areas of potential improvement for future work.

# Chapter 2

# Parallel Programming Paradigms

This chapter will provide and introduction to the fundamentals parallel programming. The remaining chapters will assume a working knowledge of parallel algorithms, GPU architecture, and CUDA optimization techniques.

## 2.1 Principles of Parallel Programming

As the physical limits of transistor size are being reached, the trend in computing has been away from making processors faster and towards parallel processing. The introduction of General Purpose Graphics Processing Units have made data parallel algorithms a very attractive approach to accelerating computationally intensive tasks. However, migrating from sequential computing to parallel platforms is not always simple or even wise. The following are some principles to keep in mind when considering using GPU acceleration.

**Keep data parallel**  Parallel computing is best suited to performing simple operations on large numbers of independent data elements, such as n-body simulations and per-pixel image processing operations. Aside from these trivial cases, adapting sequential algorithms to a GPU architecture efficiently can be challenging. Not all loops are easily parallelizable.

**Memory is a bottleneck**  Computing with thousands of cores in a GPU makes memory I/O into a major bottleneck. Usually the data transfer to and from the parallel device will take much longer than the actual compute time. Be extremely conscious or memory usage.

**Minimize code divergence**  On most architectures, parallel code runs in batches for increased efficiency. If the code is full of if/then/else statements, the divergent execution paths can dramatically impact performance.

**Avoid sequential operations and synchronization**  Atomic operations that must be performed in order or synchronizations between concurrent threads of execution can be very slow. The more the threads can be independent of each other, the more efficiently the hardware will be able to execute them in parallel.

**Be mindful of the hardware**  When writing performance critical code, understanding the underlying architecture can be a big help. Understanding how the code will actually be distributed and executed across multiple processors will make optimization much easier.

## 2.2 Parallel Algorithm Building Blocks

Just as there are fundamental building blocks of sequential computing like search, recursion, and iteration, many parallel algorithms make use of primitive operations like reduce, scan, and stream compact.

### 2.2.1 Reduction

Reduction is any operation on an array of elements that computes a single result. Common examples include sums, average, min, max, and product. In sequential terms, implementing reduction is very simple. Using sum as an example, algorithm 1 shows how this might be implemented.

**Data**: n element array X
**Result**: sum of elements in X
i = 0;
sum = 0;
**while** $i$ ¡ $n$ **do**
    sum += X[i];
    i++;
**end**

**Algorithm 1:** Sequential Sum

Notice that in the sequential algorithm, the accumulator's value at each iteration depends on the value in the previous iteration. To perform a parallel sum, the associative property of the operator can be exploited to break group the operation into a structured set of binary operations that can be performed in parallel (Figure 2.1).

This parallel reduction method will work for any associative binary operator.
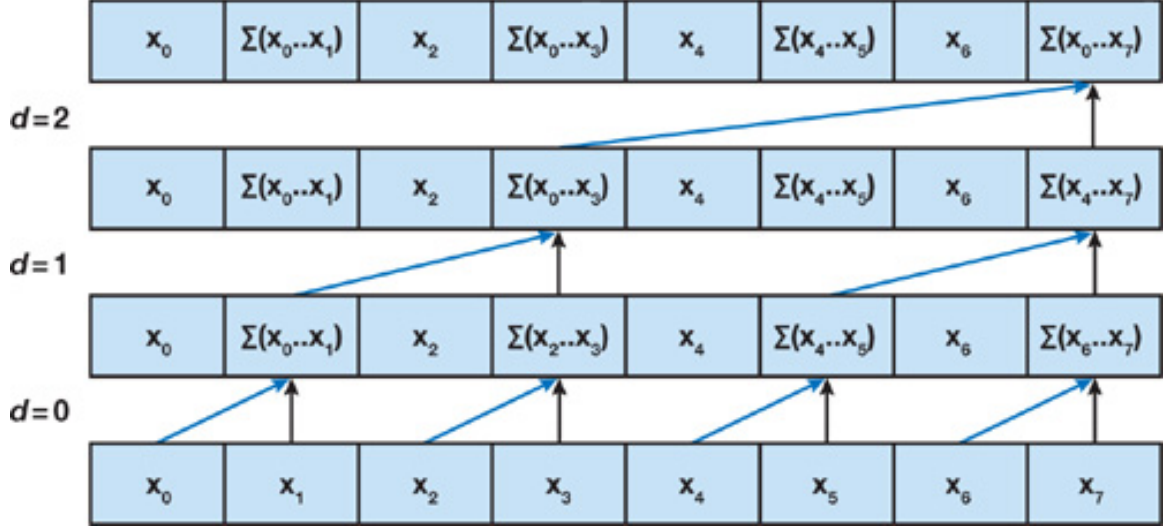
Figure 2.1: Parallel Reduction. Reproduced from[22]

## 2.2.2 Scan

The scan operation is similar to a performing a cumulative sum operation on an array. There are two forms of scan: exclusive and inclusive. Usually the term scan refers to an exclusive scan.

Given an associative binary operator $\oplus$ with identity value $I$ and an array of $n$ items $[a_0, a_1, \ldots a_{n-1}]$, an exclusive scan returns the array:

$$[I, a_0, (a_0 \oplus a_1), (a_0 \oplus a_1 \oplus a_2), \ldots, (a_0 \oplus a_1 \oplus \ldots \oplus a_{n-2})]$$

An inclusive scan returns the shifted result:

$$[a_0, (a_0 \oplus a_1), (a_0 \oplus a_1 \oplus a_2), \ldots, (a_0 \oplus a_1 \oplus \ldots \oplus a_{n-1})]$$

The sequential implementation of a sum scan is trivial and outlined in Algorithm 2.

**Data**: n element array X
**Result**: array Y contains exclusive scan of X
i = 1;
Y[0] = 0;
**while** $i < n$ **do**
  | Y[i] = Y[i-1] + X[i-1];
  | i++;
**end**

**Algorithm 2:** Sequential Sum

To perform a parallel scan in a work efficient manner, first a reduction is performed

on the array as in Figure 2.1. Then, the last element of the array is set to 0, and a

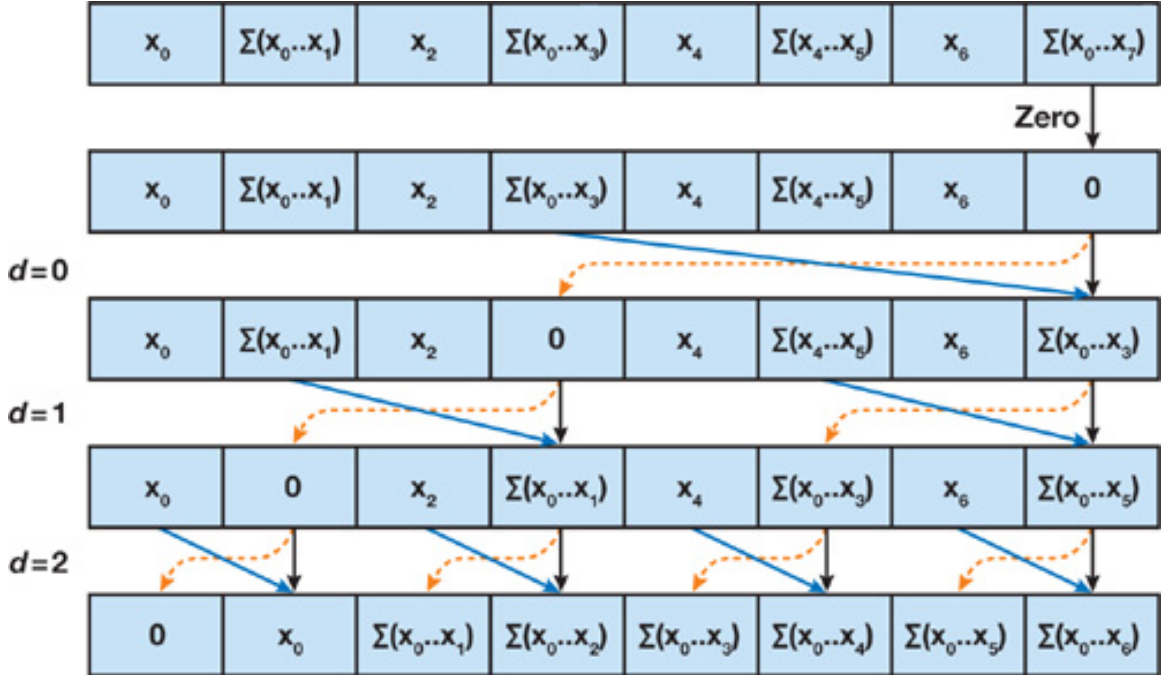series of swaps and sums are performed as shown in Figure 2.2.



Figure 2.2: Down-sweep phase of parallel sum scan. Reproduced from[22]

## 2.3 Stream Compaction

In parallel computing, stream compaction is a useful tool for selecting a subset of data

and compressing it into a coherent memory block. For example, stream compaction

could be used to transfer all of the odd elements in array A of Figure 2.3 and place them in order compressed at the start of array B.
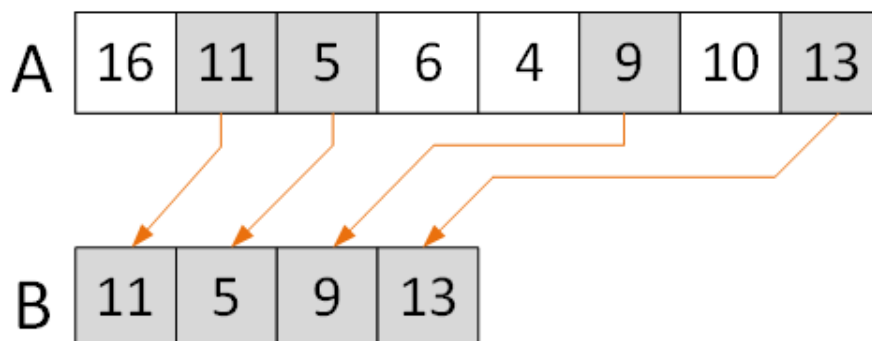


Figure 2.3: Example of stream compacting odd valued integers

Accomplishing this is surprisingly simple. As shown in Figure 2.4, a secondary array of flags is created. This array has a 1 for every odd number in array A and 0 for all others. An exclusive scan is performed on the flag array. Notice that every flagged element now has a unique zero-based index associated with it. The flagged elements are then "scattered" by the computed index. The scatter function is outlined in Algorithm 3.

**Data**: input array A and scanned flag array F, both of length n
**Result**: output stream compacted array B
**foreach** *i=0...n-1 in parallel* **do**
   **if** *isFlagged(A[i])* **then**
      B[F[i]] = A[i];
   **end**
**end**

**Algorithm 3:** Sequential Sum

## 2.4   Programming with CUDA

CUDA is a C/C++ based programming language created by NVIDIA to expose the general compute functionality of their GPU processors.
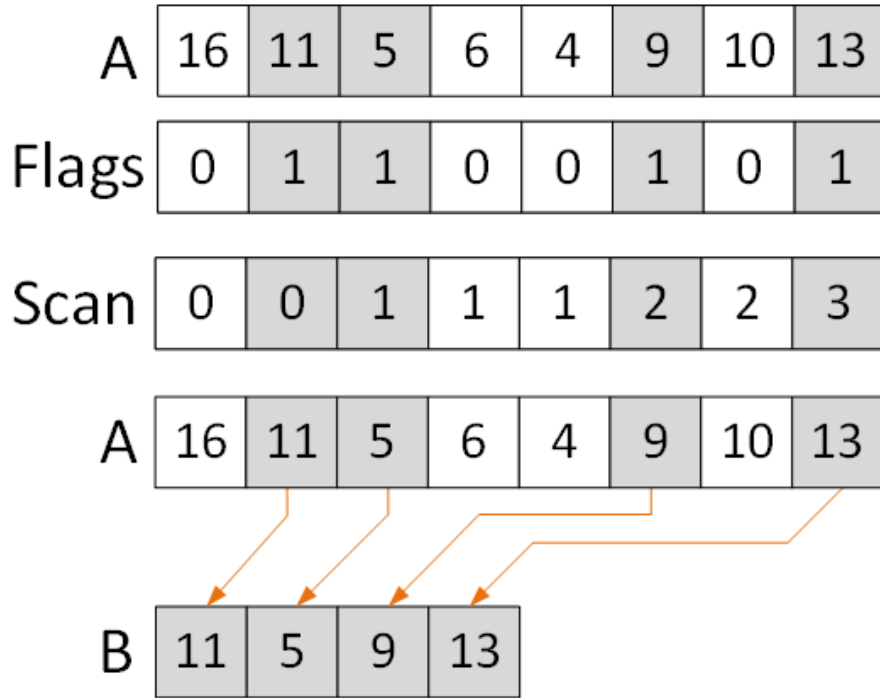
Figure 2.4: How stream compaction works (Scan and Scatter)

### 2.4.1 CUDA GPU Architecture

CUDA divides the computer into host and device. The host refers to the CPU and all memory it has access to, and the device refers to the GPU and its memory banks. Memory transfers between the host and GPU are started and managed by the host.

A piece of code that runs in parallel on the device is called a kernel. Figure 2.5 shows how kernels are organized. Each individual running process is called a "thread". Threads are organized into "blocks" of up to 1024 threads on modern architectures. Blocks are then grouped into "grids". Within each block, threads are executed in groups of 32 threads called "warps". Every thread in a single warp executes simultaneously on a single processor core. The device memory architecture is depicted in Figure 2.6. Global memory, constant memory, and texture memory are all accessible

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by any thread in the kernel. The primary difference between these memories . Every thread also has access to a limited amount of memory which is shared between all threads in a block. Shared memory is much faster than global memory access, and can be used to accelerate kernels that need to share data between threads locally. Finally each thread has access to its own local register memory.

## 2.4.2   Optimizing CUDA Code

Optimizing CUDA kernels is very application dependent and difficult to provide a universal manual for. However, there are several key underlying GPU architecture features that should be highlighted which can have a dramatic impact on performance.

**Global Memory Coalesced Access**   Global memory is designed in such a way that each half warp can load 64 consecutive bytes in memory as a single parallel read, provided the memory chunk is also 64-byte aligned. This is just enough memory to load an array of 16 consecutively floats at once (one per thread per half warp). To achieve peak memory bandwidth, reads and writes from global DRAM should be grouped into large consecutive chunks of memory. Because of this, it is sometimes extremely beneficial to utilized structure of array (SoA) data storage schemes as opposed to the more typical array of structures model (AoS).

**Shared Memory Optimization**   Shared memory is much faster than global memory, so it can be instrumental in optimizing kernels. For example, instead of performing a reduction or scan in global memory, the entire array can be loaded into shared

memory in a single read operation. The operation would then be performed in shared memory and the results written back in a single coalesced DRAM write. However, shared memory is limited. If too much is used, the number of blocks that can be simultaneously executed on a multiprocessor could go down, preventing the kernel from fully utilizing the GPU hardware. Also, this provides motivation for restricting the size of input data. If all of the data to be processed can be loaded into a single block, shared memory becomes much easier to utilize.

Shared memory is divided into banks, where successive 32-bit words are assigned to successive banks. Shared memory access is done per bank, so if every thread in a warp reads from a different bank, regardless of the ordering, no bank conflicts occur. If two or more threads try to read from the same bank simultaneously, the reads are serialized which reduced the shared memory bandwidth utilization. The exception to this rule is when all threads read from the same bank. This triggers a special broadcast mode that has no bandwidth penalty.

**Warp Partitioning and Divergent Code**   As mentioned above, threads are actually executed in groups of 32 threads called warps. All threads in a warp take the same amount of time to operate. So if only one thread in a warp is actually doing any work, 31 threads will be idle and waste GPU hardware. Minimizing intra-warp code divergence in will go a long way towards fully utilizing hardware. Also, if possible retire entire warps early to free up resources for warps in the execution queue.
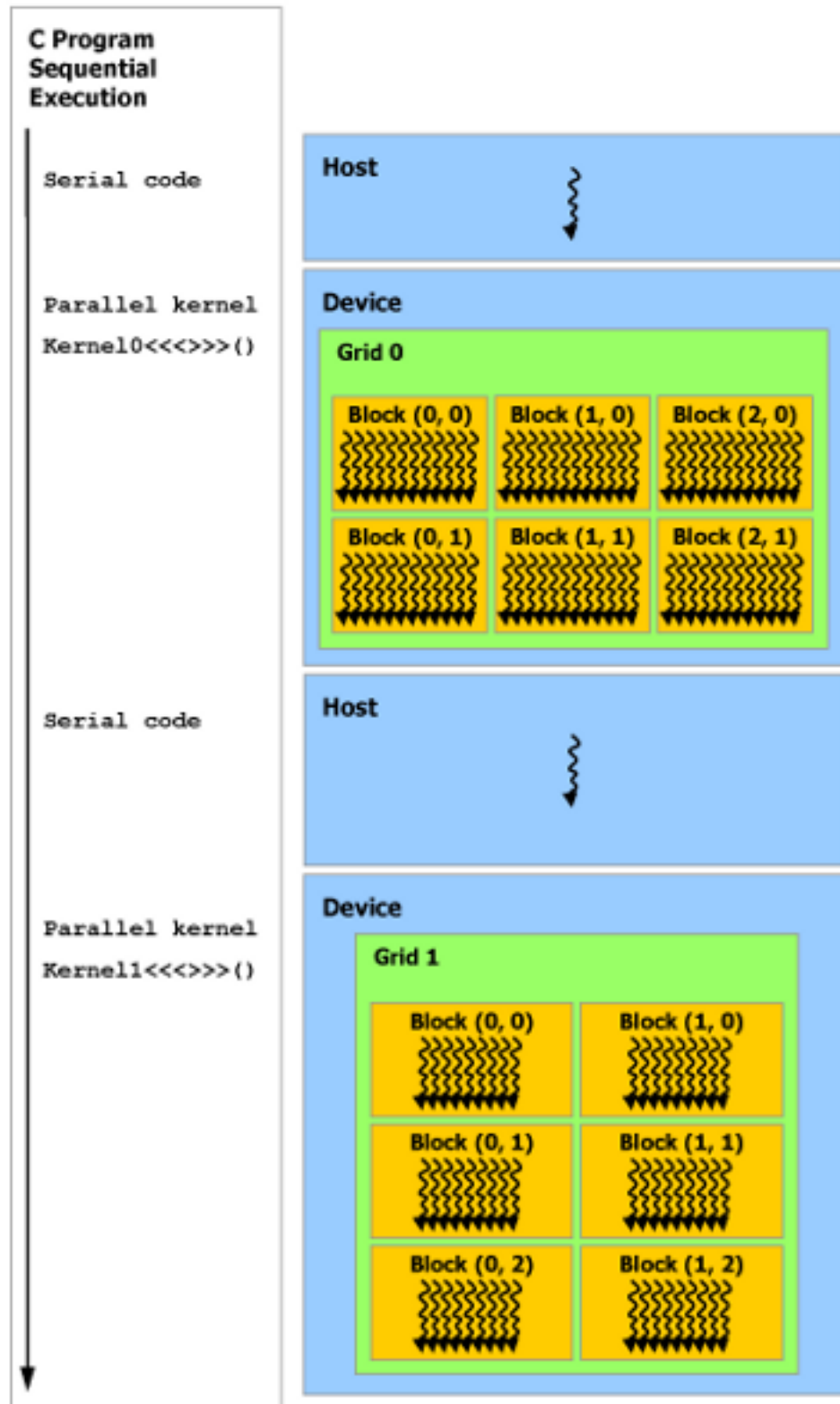
Figure 2.5: CUDA Kernel Organization. Reproduced from [24]
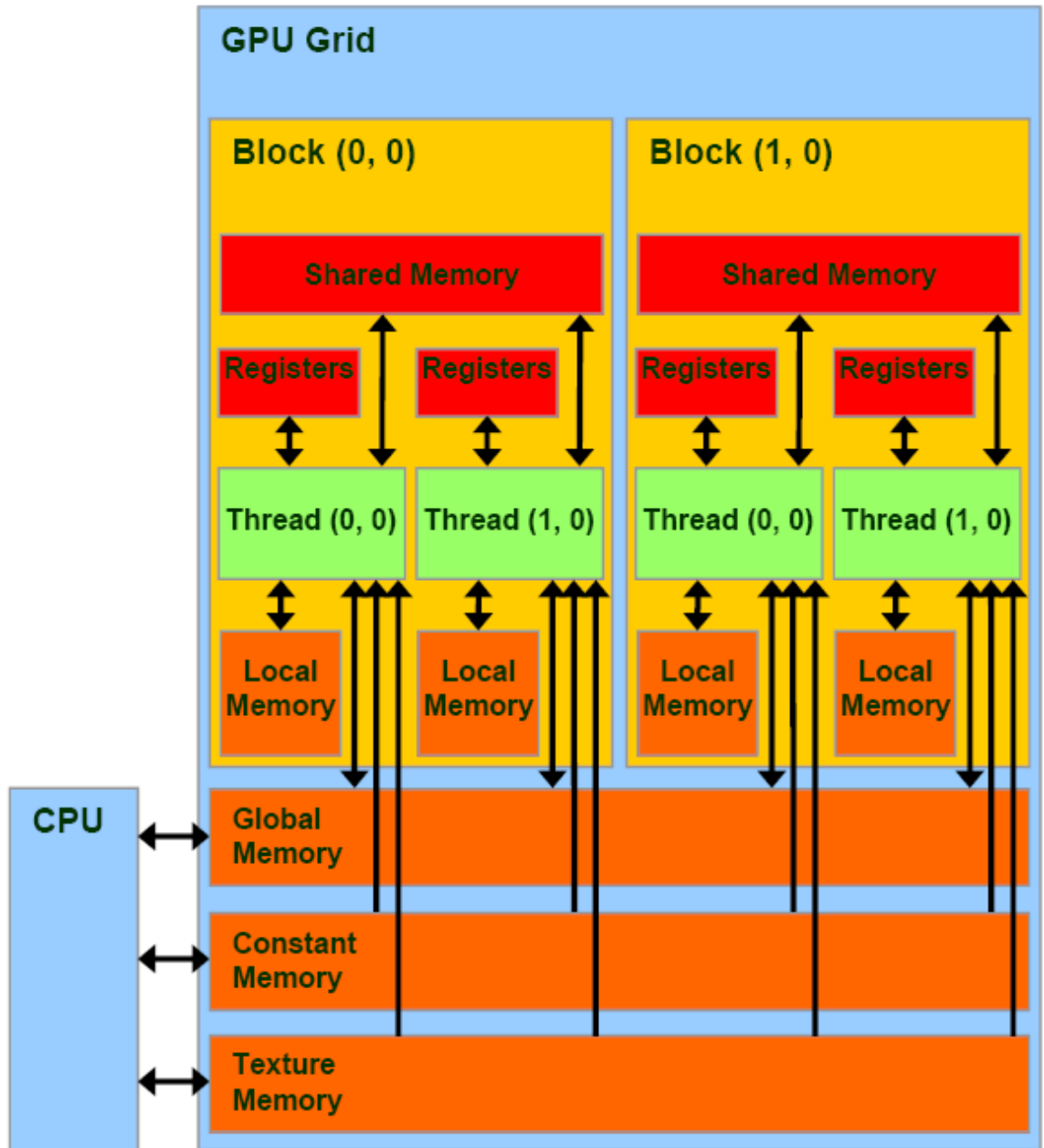
Figure 2.6: CUDA Memory Organization. Reproduced from [37]

# Chapter 3

# Problem Formulation and

# Approach

## 3.1  Problem Specification

## 3.2  High Level System Design

## 3.3  Plane Detection and Meshing Pipeline Design

# Chapter 4

# Implementation

## 4.1 RGBD Framework

## 4.2 Preprocessing

## 4.3 Plane Segmentation

## 4.4 Mesh Generation

# Chapter 5

# Performance Analysis

# Chapter 6

# Conclusions and Future Work

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