2. Characterization of the preamplifier

Figure 3 shows a diagram of the hybrid preamplifier with legs (pins) identified.

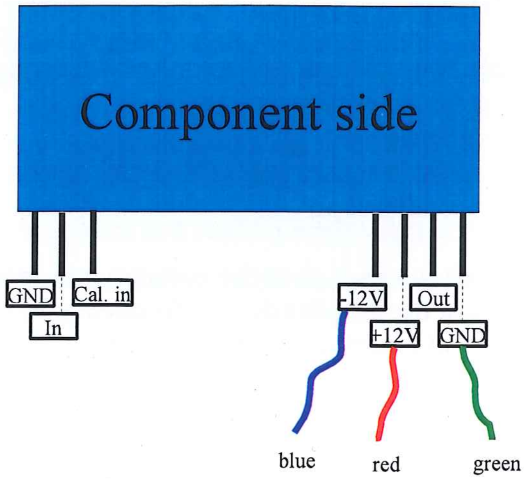


Illustration 3. Layout of the preamplifier hybrid board.

Figure 4 shows the schematics of a low noise charge integrating amplifier. T1 is a high gain stage powered by a JFET transistor.

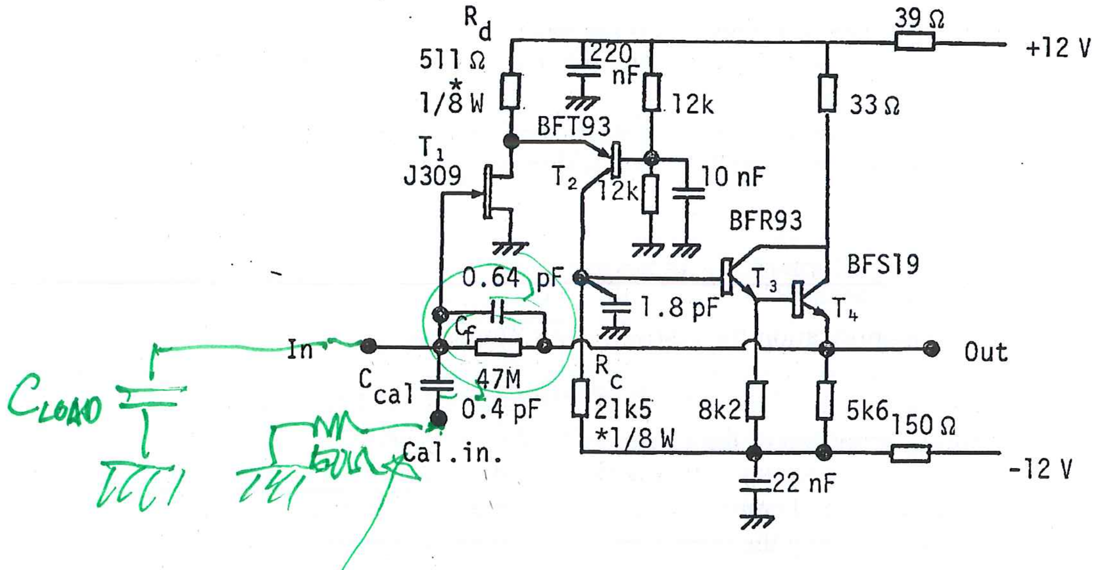
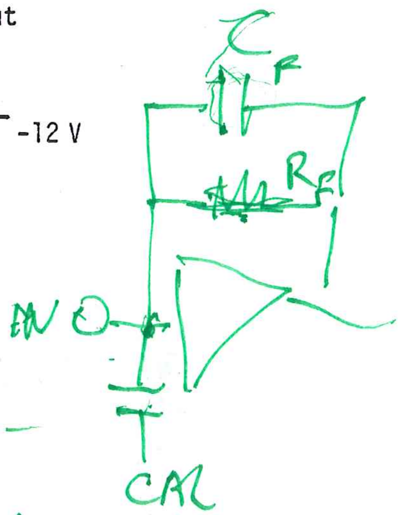


Illustration 4. Schematics of the preamplifier hybrid board.



V_{cal}

$Q_{CAL} \sim 2500 \cdot e^-$

169.254. ~~166.185~~
192.91

Task:

- Get familiar with the Vero board (the brown board with a lot of holes).
    - ✔ Connections on the board. Note the two external components on the board (a 50 Ohm resistor, 100 nF capacitor). What is the purpose of the components?
    - ✔ Notice that there are plenty of unequipped places on the board where external components can be easily be plugged in.

- Use a lab power supply with two voltages, a pulse generator giving with square pulses and a oscilloscope get the amplifier running.
    - ✔ Connect voltage to voltage pins
    - ✔ Connect a small amplitude square pulse (10-20 mV, 1kHz) to Cal. in.
    - ✔ Study the output on oscilloscope

Use a Digital Volt Meter (DVM) to check that the voltages you intend to apply to the amplifier are correct! Check the amplitude and frequency of the signal applied to Cal_in. (This is a good exercise to get familiar with the oscilloscope)

- Study the amplifier gain, rise time and noise as a function of load capacitance (between input and ground) .
    - ✔ Determine the size of the calibration charge you are going to injected into the preamplifier. The charge is injected by a square pulse over the calibration capacitance Cal. in. Select an injected charge between 1-2 MIP in 300 micrometer silicon (between 25000 electrons and 50000 electrons). amplitude
    - ✔ Measure ~~gain~~, rise time and noise vs. input capacitance (1-100 pF) and note down the values in a table.
    - ✔ Plot the gain, rise time and noise vs. input capacitance.
    - ✔ Plot the ENC vs. capacitance, fit the data with a straight line and extract the ENC noise (offset) at 0pF and the noise slope in ENC/pF.

ENC = Equivalent Noise Charge, the number of electrons one would have to collect from a silicon sensor in order to create a signal equivalent to the noise of this sensor.

- Study the preamplifier performance with a Spectroscopy Amplifier (SA) and a Pulse Height Analyzer (PHA).
    - ✔ Adjust the amplification for 1 MIP to ~2V amplitude on the spectroscopy amplifier output.
    - ✔ Do a 3pt gain calibration with 1, 2, 3 MIP test pulse to determine the calibration parameters of the PHA → Plot the gain curve
    - ✔ Measure the noise for two shaping times (long and short) for a medium large capacitance and compare the result with the oscilloscope measurement. → Add the measurement to the plot made with oscilloscope.

? Do the measurements with two different shaping times give indications for the source of the noise (serial, parallel?)

pF	Amp	RT	Noise (RMS)
1			
⋮			
100			

Measurement of full chain sensor + amplifier=detector

Task:

- Measure the performance with the sensor DC-coupled to the preamplifier with radioactive source

  =HV

  - ✔ Bias the sensor from the backplane. Feed the backplane bias through a low-pass filter with a cutoff frequency <10Hz. Build the filter in the "creative corner" on the VERO board.
  - ✔ Apply bias to fully deplete the silicon sensor (the depletion voltage you have determined during sensor characterization)
  - ✔ Acquire a spectrum with the PHA with and without source

- Plot the PHA spectrum and explain what you see

? What were the major problems in the detector performance and how can the the detector be improved ?

Sicium 137

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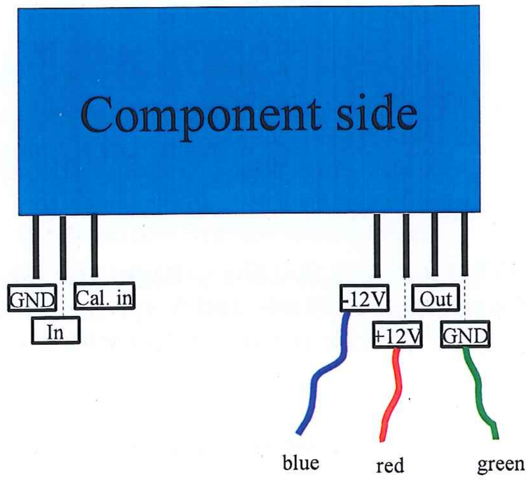

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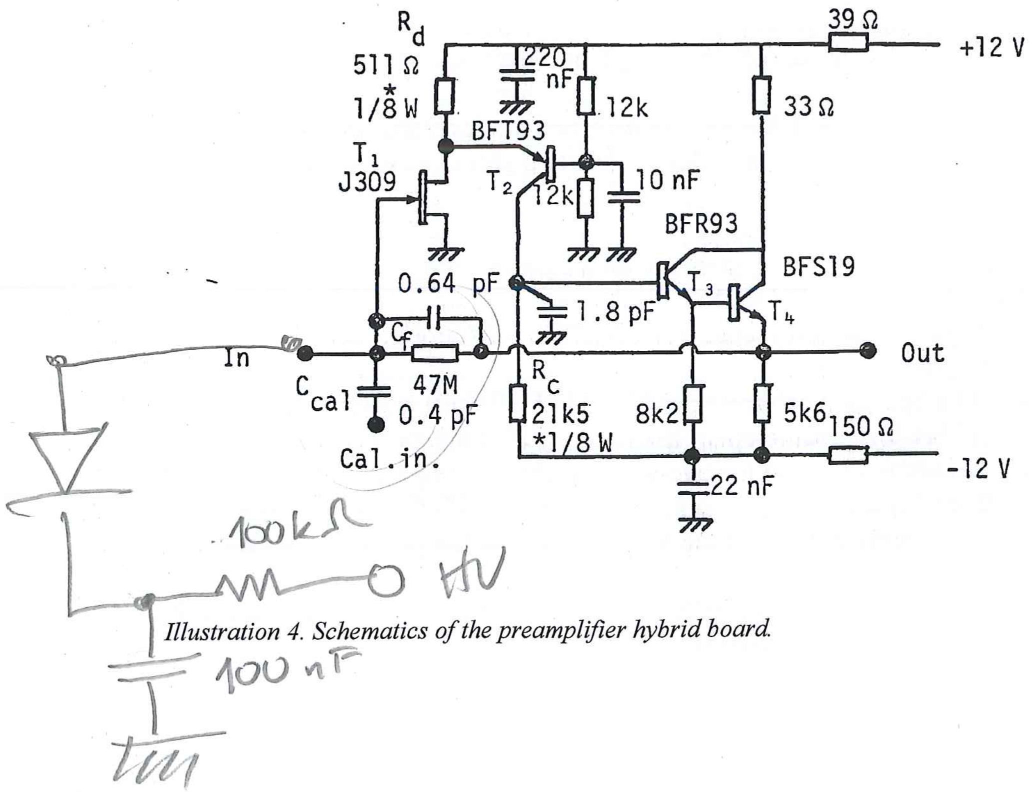

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