

Week 14

Thin Film Transistors 2

Ambipolar and Other Transistor Architectures

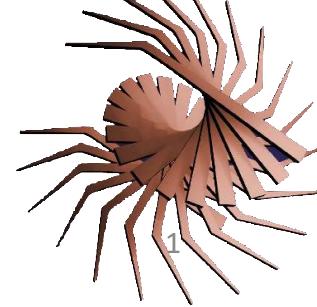
Materials & Morphology

Reliability

Applications

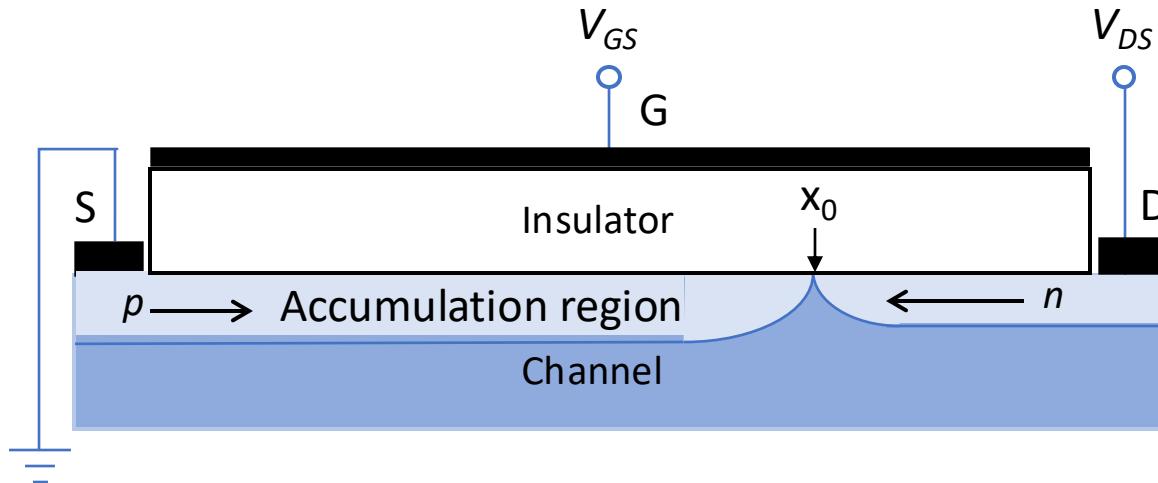
Chapter 9.2, 9.4 - 9.8

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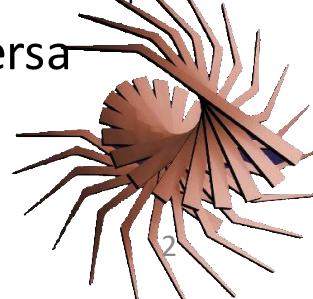
Ambipolar OTFTs

- Channel capable of supporting both electron and hole transport
- Advantage: Complementary logic possible with a single structure

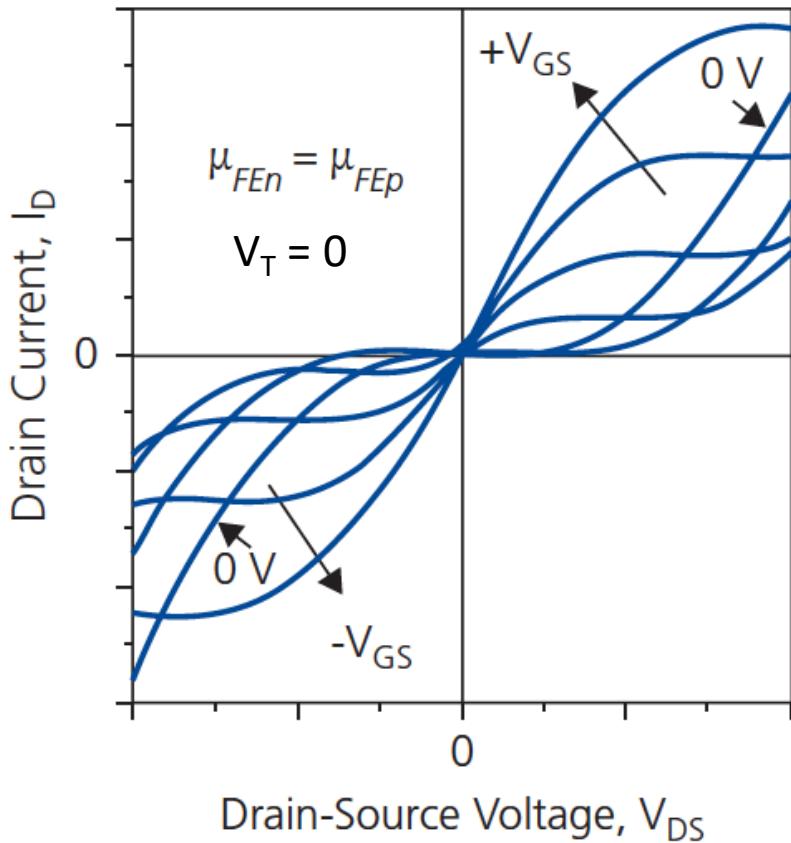


Strategies for achieving bipolar action:

- Use material with both high μ_{FE_n} and μ_{FE_p} with contacts in the **middle of the energy gap** (i.e. use ambipolar conducting organics)
- Use a bilayer, one with higher electron vs. hole mobility and vice versa
- Use a blend of electron and hole transporting materials



Ambipolar transfer characteristics



Example: $V_{Tp} < V_{Tn}$

Linear regime

$$I_D = \frac{WC_i}{L} \mu_{FEn} \left(V_{GS} - V_{Tn} - \frac{V_{DS}}{2} \right) V_{DS}$$

$$\begin{cases} 0 \leq V_{DS} \leq V_{DSsat} \\ V_{GS} > V_{Tn} \end{cases}$$

Saturation regime

$$I_D = \frac{WC_i}{2L} \mu_{FEn} (V_{GS} - V_{Tn})^2$$

$$\begin{cases} V_{DS} \geq V_{GS} - V_{Tn} \\ V_{DS} \leq V_{GS} - V_{Tp} \end{cases}$$

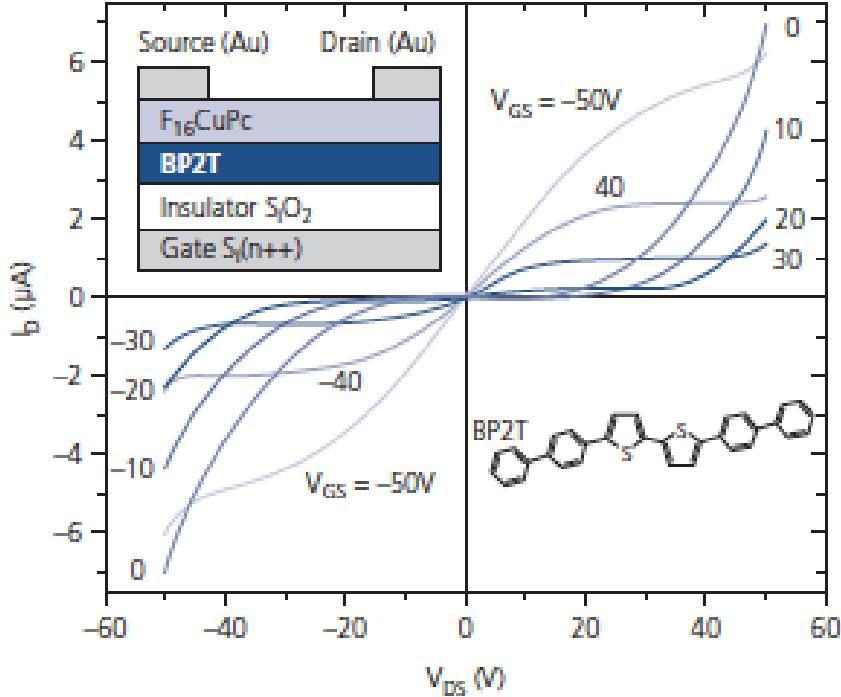
ronics orrest

Ambipolar (quadratic) regime

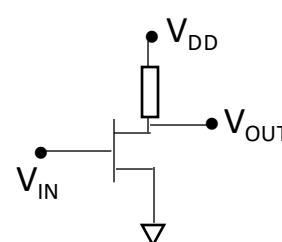
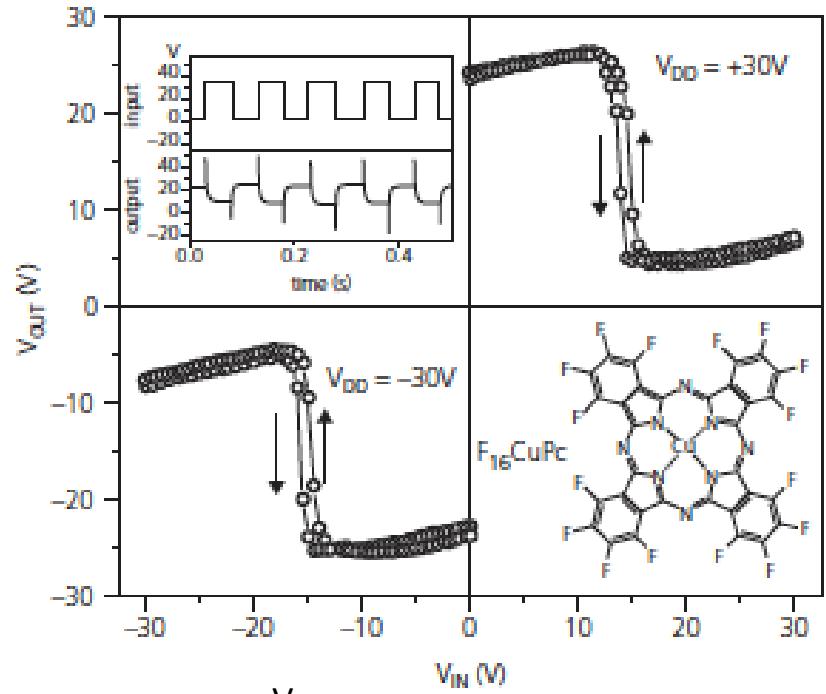
$$I_D = \frac{WC_i}{2L} \left\{ \mu_{FEn} (V_{GS} - V_{Tn})^2 + \mu_{FEp} (V_{DS} - V_{GS} + V_{Tp})^2 \right\}$$

$$V_{DS} \geq V_{GS} - V_{Tp} \geq V_{GS} - V_{Tn}$$

Bilayer ambipolar OTFT

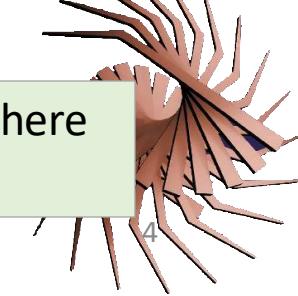


Common source amplifier response



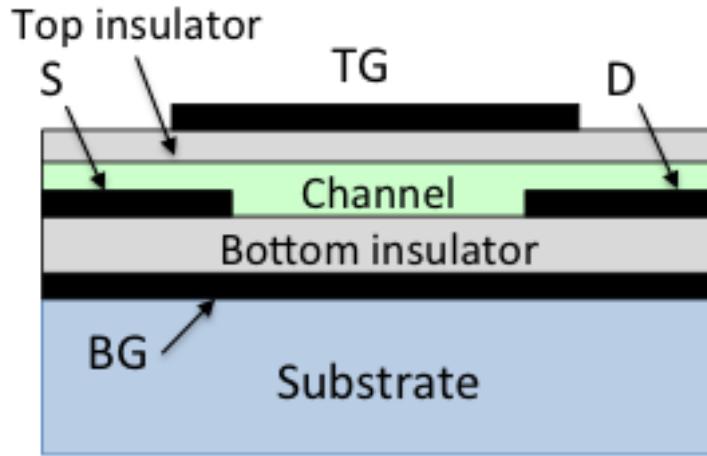
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Disadvantage of the ambipolar OTFT: I_{on}/I_{off} is small since no condition where one carrier type is completely absent.



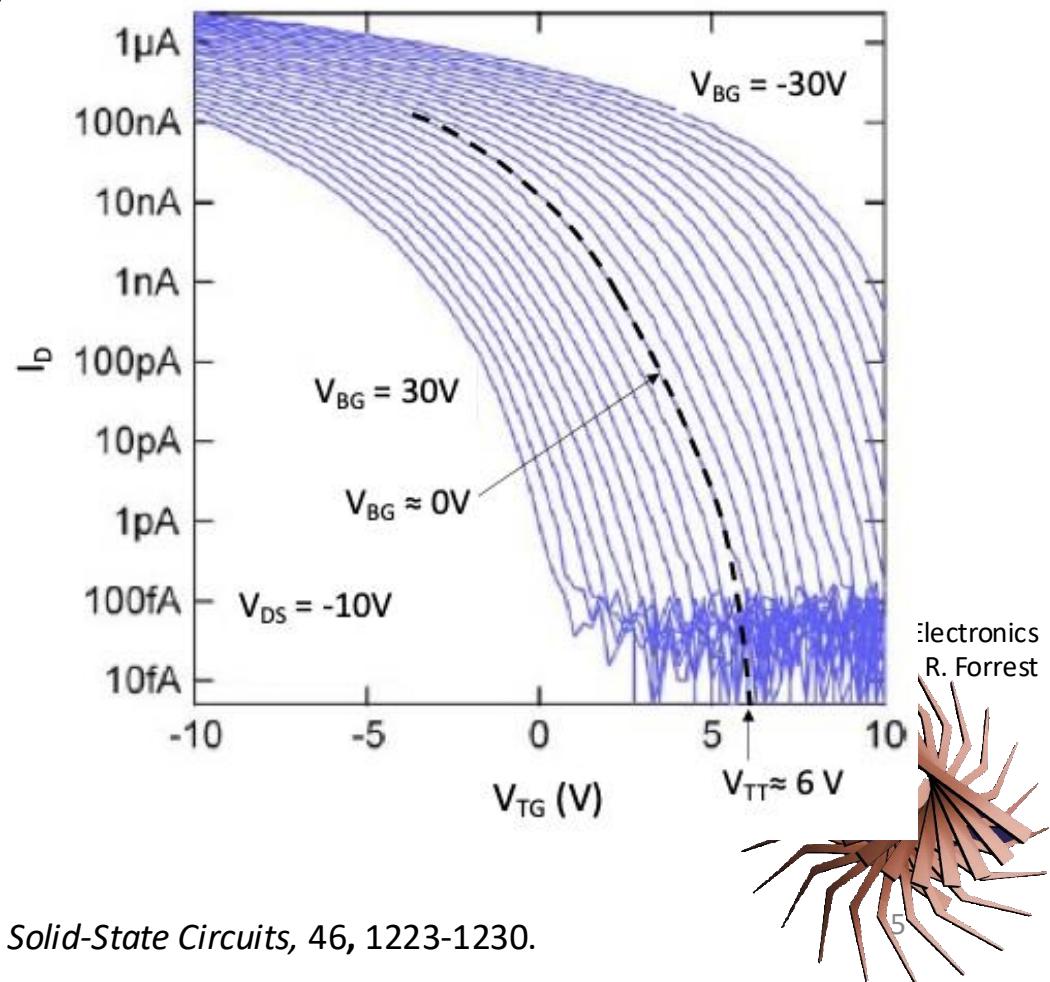
Dual gate transistors

- Useful for adjusting V_T due to extra bias control of the second (bottom) gate
- In conventional CMOS technology, this is the “body potential”
- Important for controlling large ICs

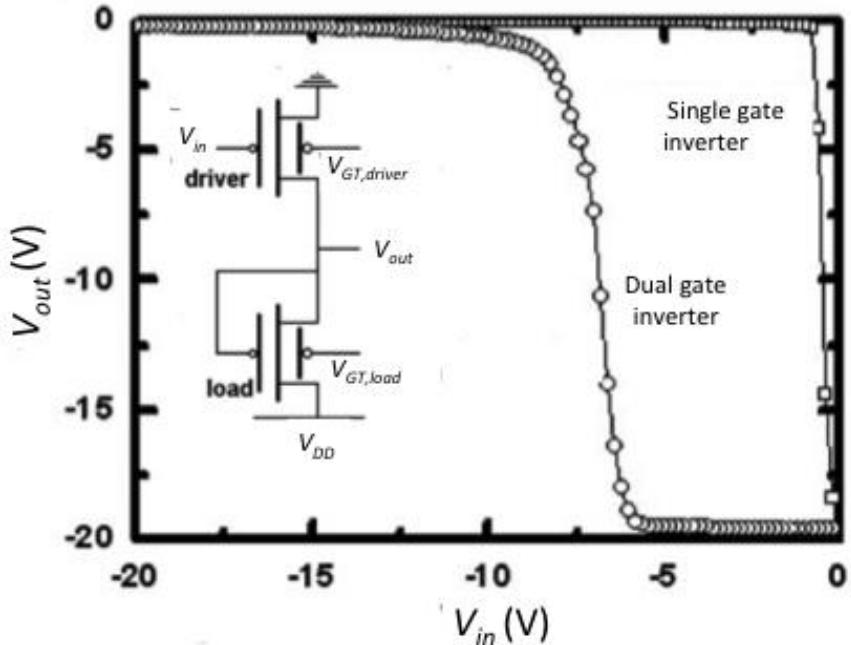


Shift in top gate threshold related to bottom gate voltage:

$$\Delta V_{TT} = \frac{C_B}{C_T} V_{GB}$$



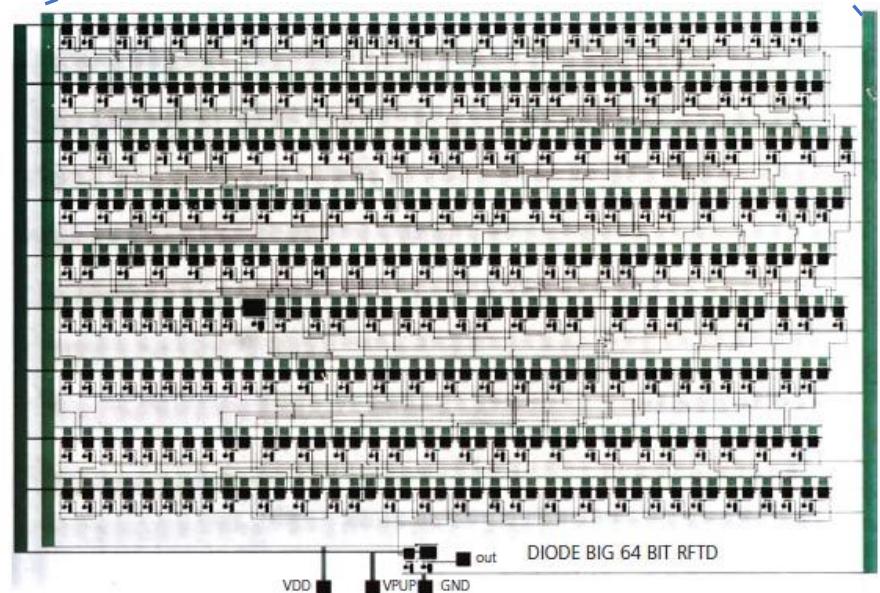
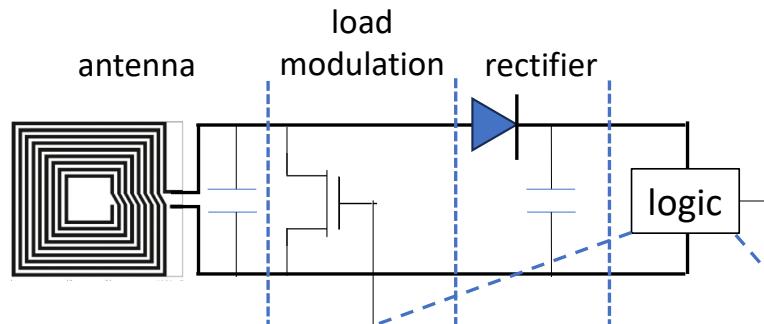
Dual gate control in an RFID transponder



Improved noise margin

Control of circuit gain

Spijkman et al. Appl. Phys. Lett., **92** 143304 (2008)

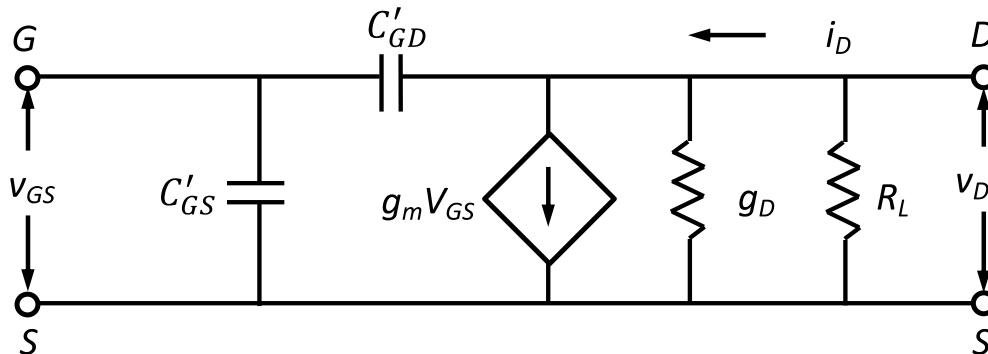


Photograph of a 64-bit RFID transponder operating at 4.3 kb/s using dual gate inverter logic.

Myny et al. IEEE J. Sol. State Circuits, **46**, 1223 (2011)

OTFT Bandwidth

Small signal equivalent circuit



C'_{GS} = total gate-source capacitance (including parasitics)

C'_{GD} = total gate-drain capacitance

R_L = external load resistance

$$\text{Small signal input (gate) current: } i_{GS} = WLC_G \frac{\partial v_{GS}}{\partial t} \Big|_{V_{DS}} = j\omega(WLC_G)v_{GS} = j2\pi f(WLC_G)v_{GS}$$

$$\text{Small signal output (drain) current: } i_D \approx g_m v_{GS}$$

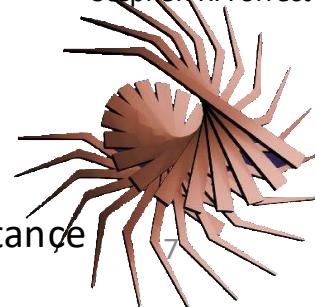
The maximum transistor bandwidth is reached when the current gain $\left| \frac{i_D}{i_G} \right| = 1$

From these expressions, we get the cutoff, or transfer frequency:

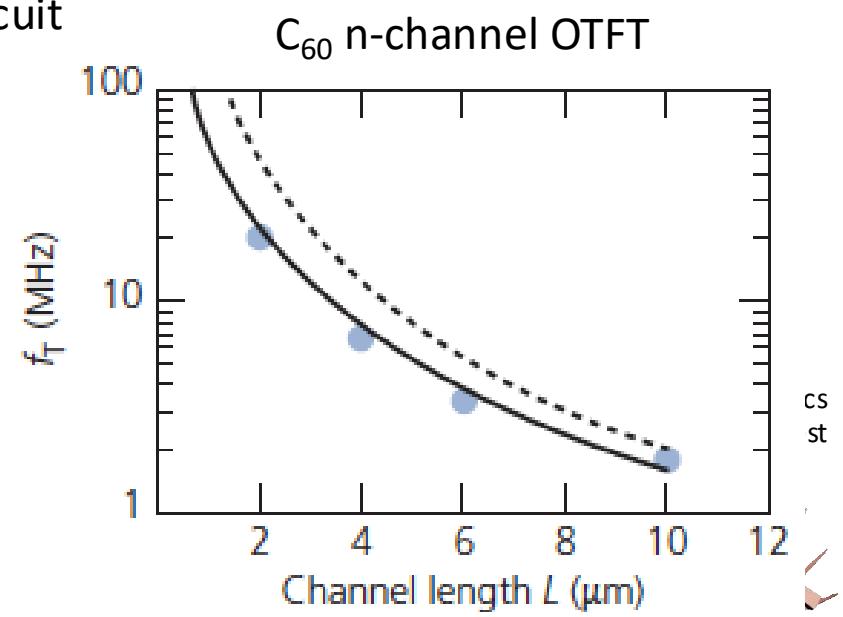
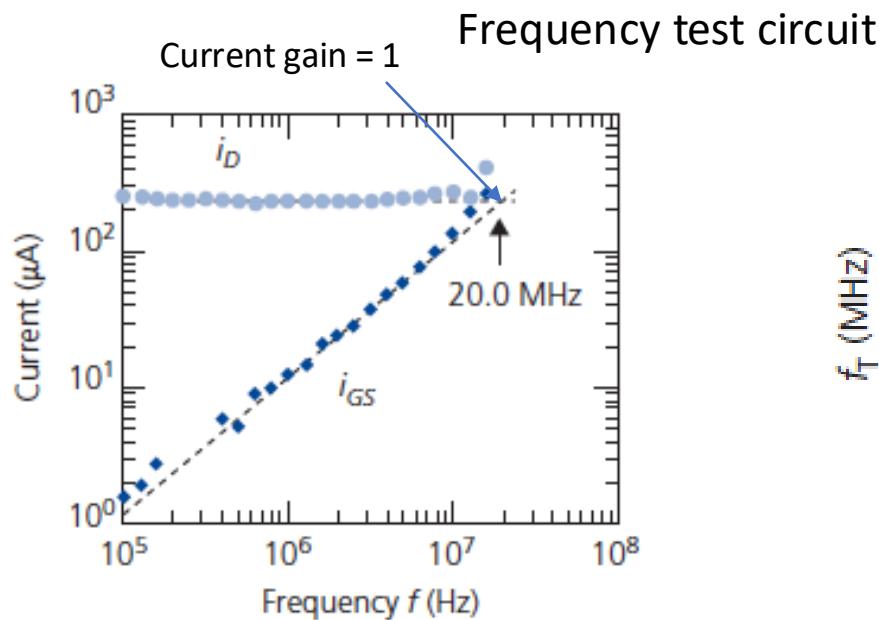
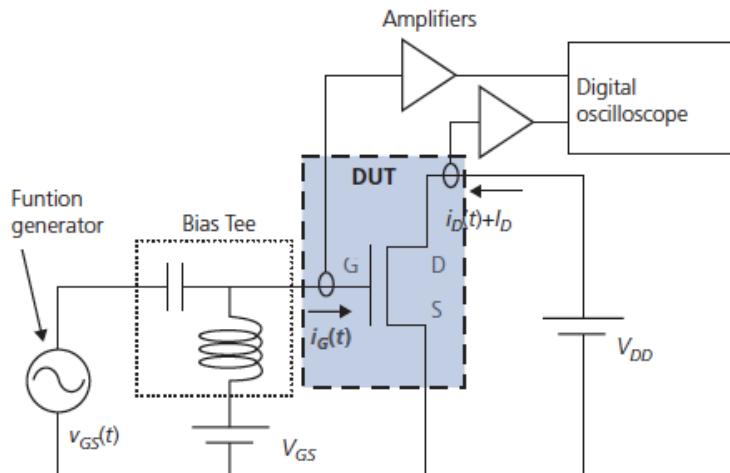
$$f_T = \frac{g_m}{2\pi WLC_G} \Rightarrow \frac{g_m}{2\pi WL(C_{GS} + C_M)}$$

C_M = Miller capacitance

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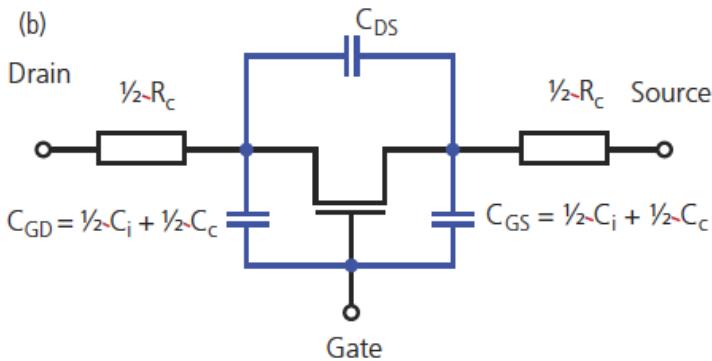
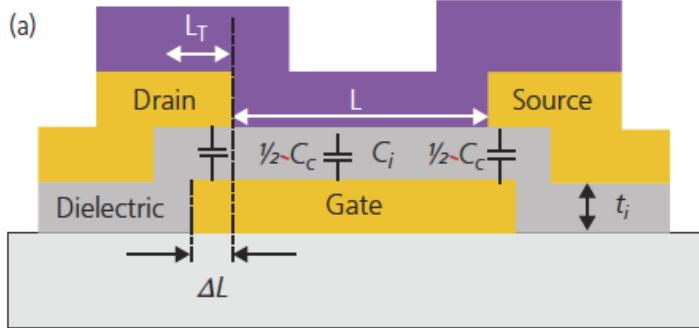


Example: High Bandwidth OTFT



Contact Resistance Limits OTFT Performance

Sources of Parasitic Resistance and Capacitance

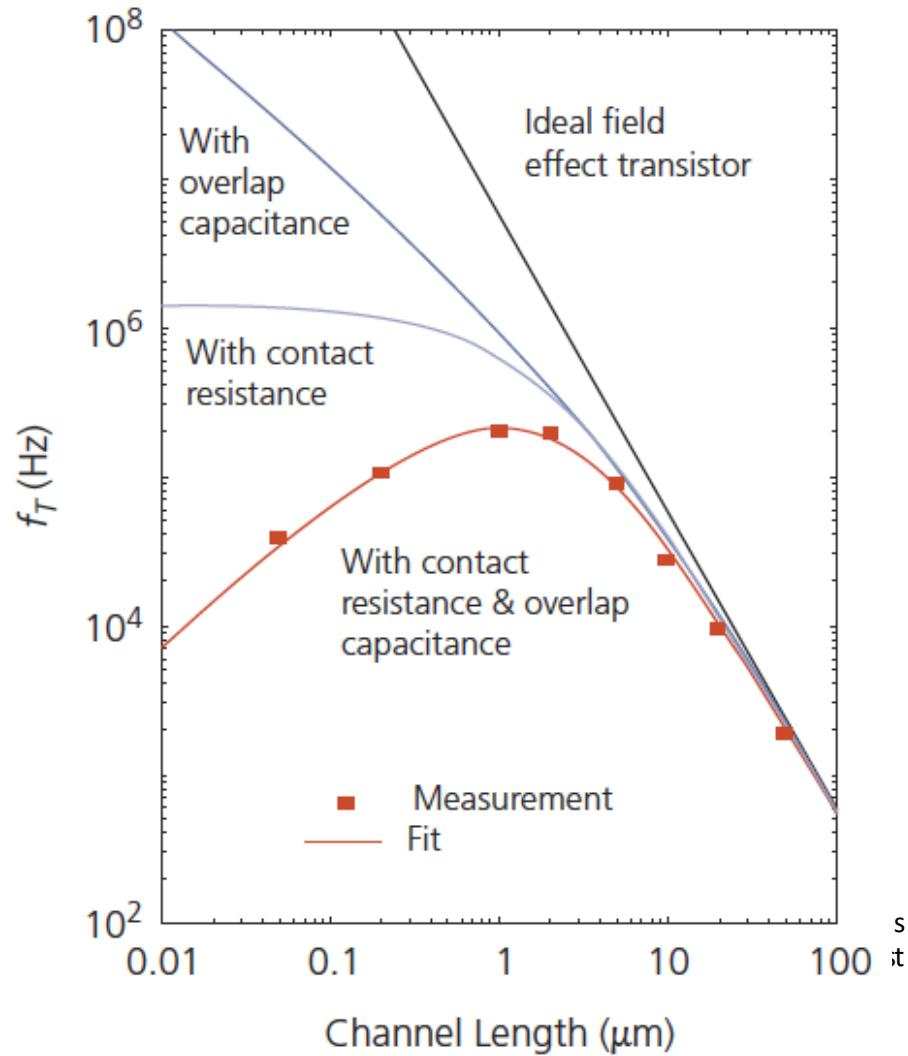


This leads to corrected transconductance and output conductance...

$$g'_m = \frac{g_m}{1 + r_s g_m} \quad g'_D = \frac{g_D}{1 + (r_s + r_D) g_D}$$

... and frequency response

$$f_T = \frac{\mu_{FE0} (V_{GS} - V_T)}{2\pi L (L + \Delta L)} \left[\frac{1}{1 + W \mu_{FE0} C_G (V_{GS} - V_T) R_C / L} \right]$$



Hoppe, et al., Organic Electron., **11**, 626 (2010)

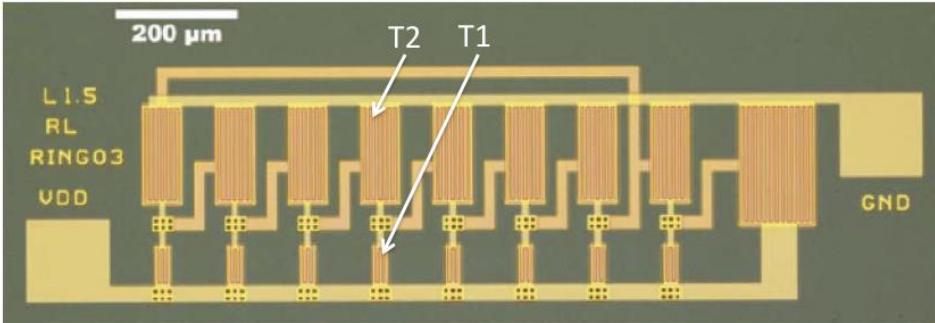
$$R_C = r_s + r_D$$



Performance has come a long way



7 stage ring oscillator

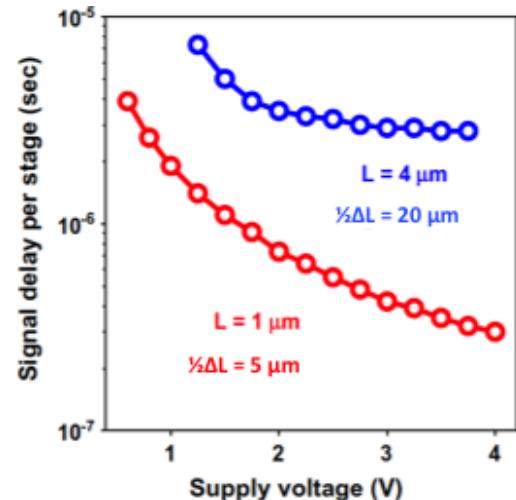


Smith et al., Appl. Phys. Lett., 93, 253301 (2008)

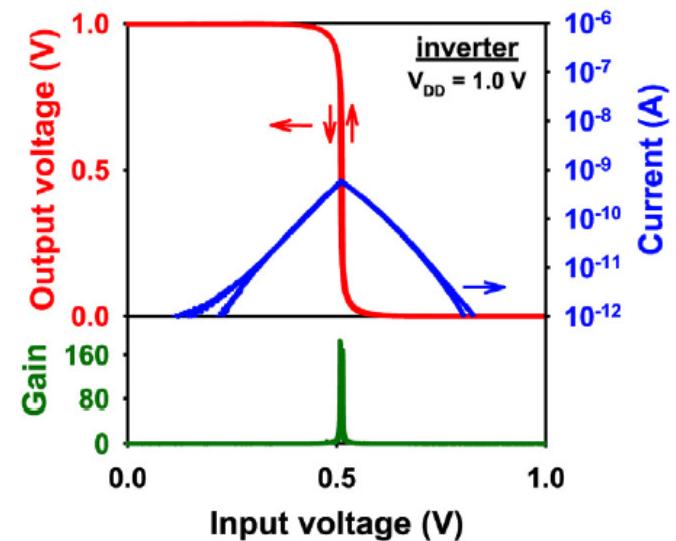
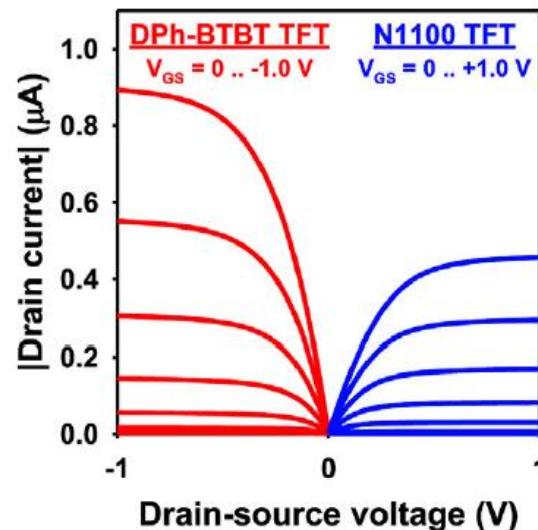
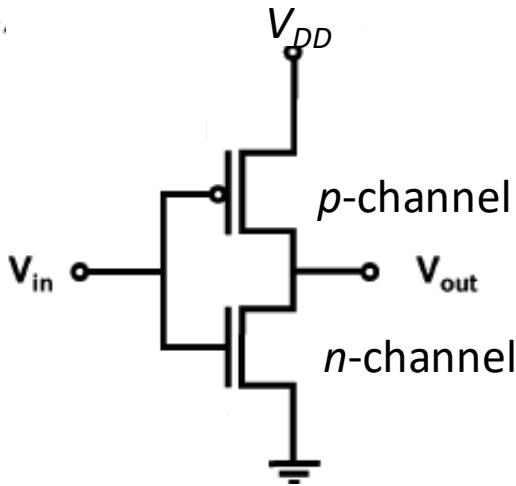
Oscillation frequency
a function of the
delay per gate

$$2f_{osc} = 1/N\tau_{delay}$$

$$f_{delay} = (2\tau_{delay})^{-1} < f_T$$

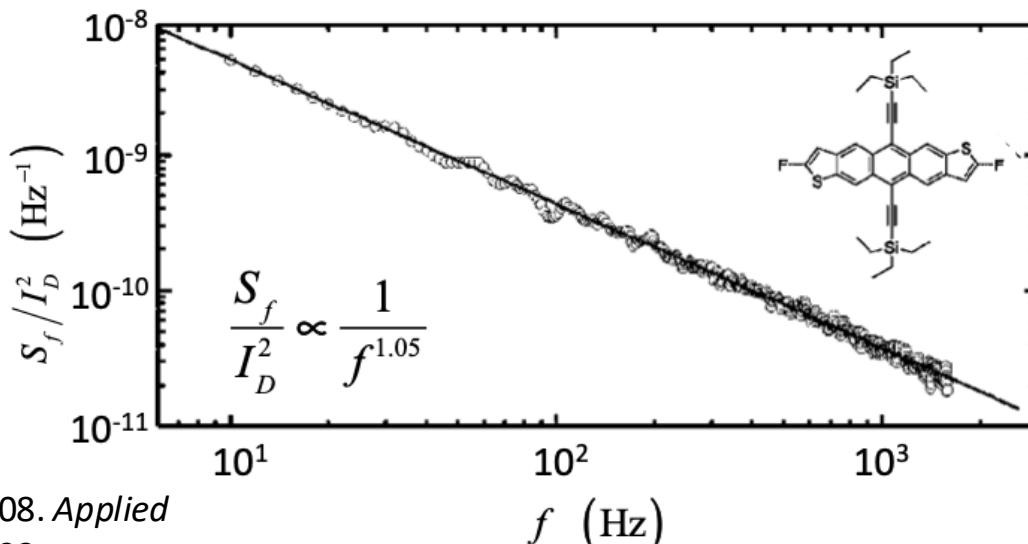
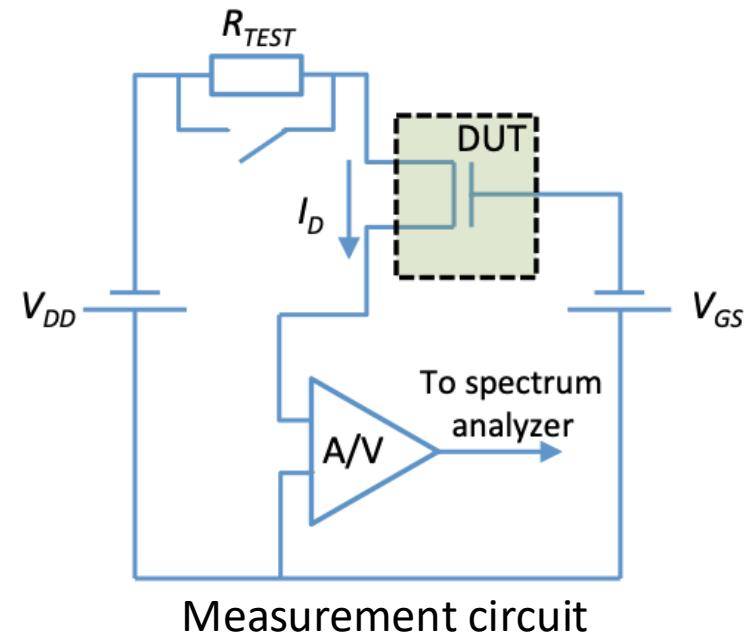
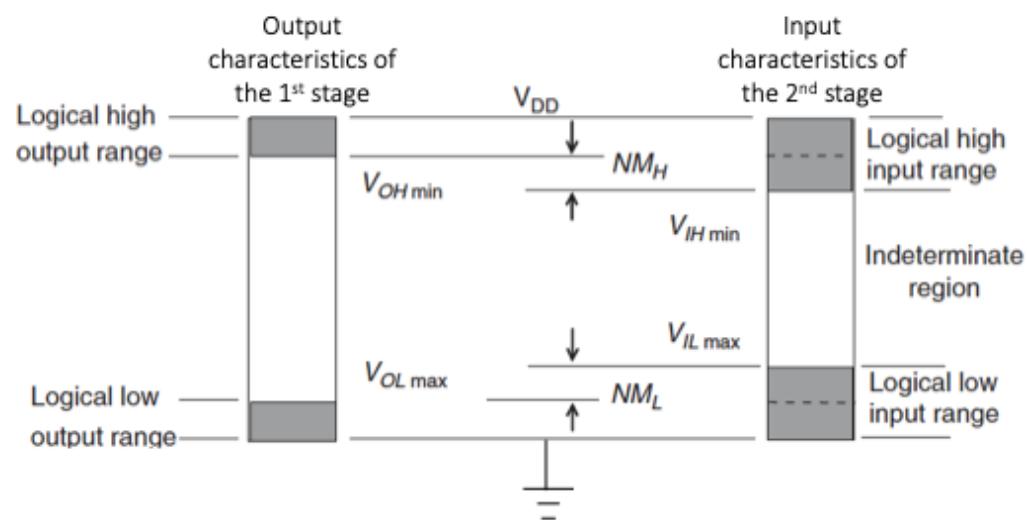


Zschieschang, et al., Org. Electron., 14, 1516 (2013).

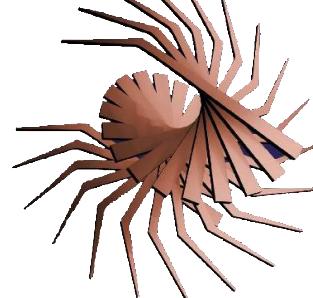


Zschieschang, et al., Organic Electronics, 49, 179 (2017).

Noise measurement and margin

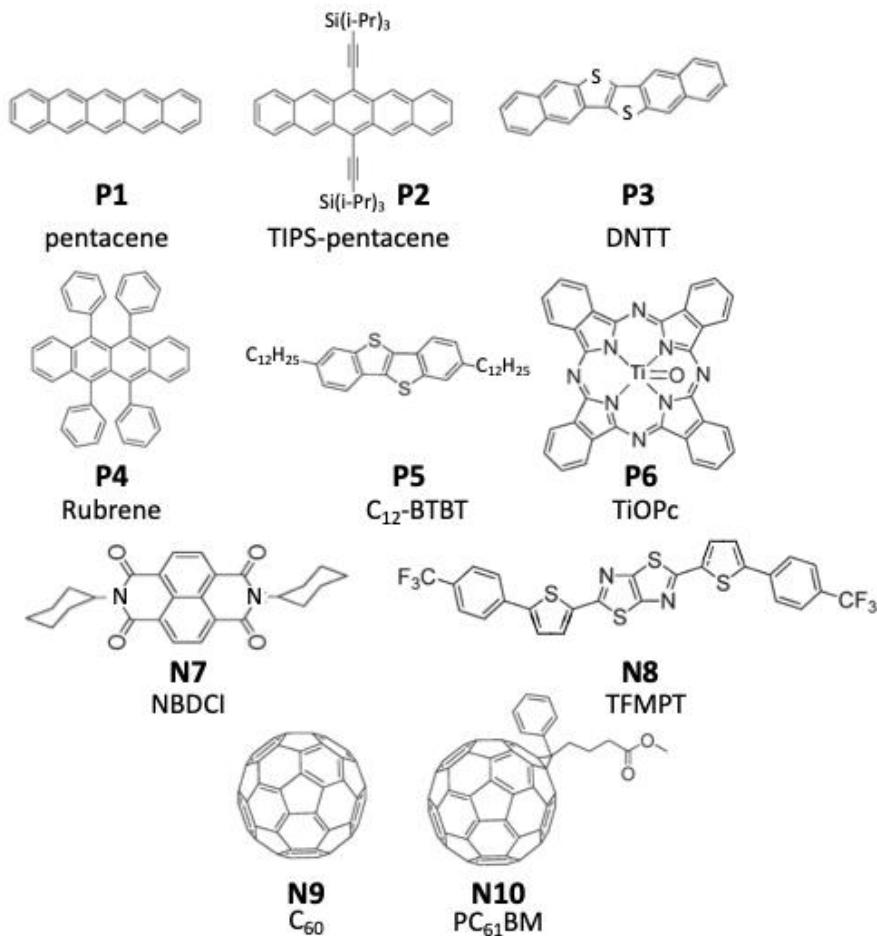


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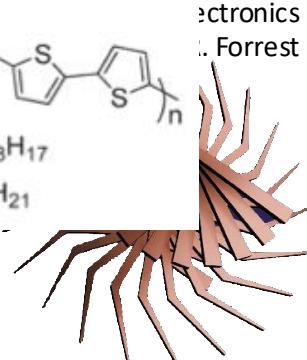
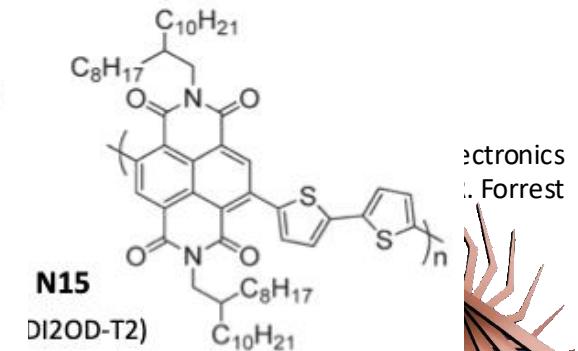
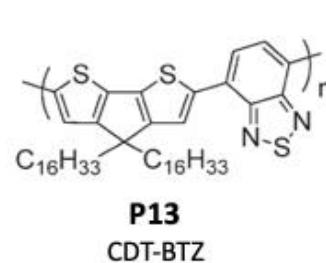
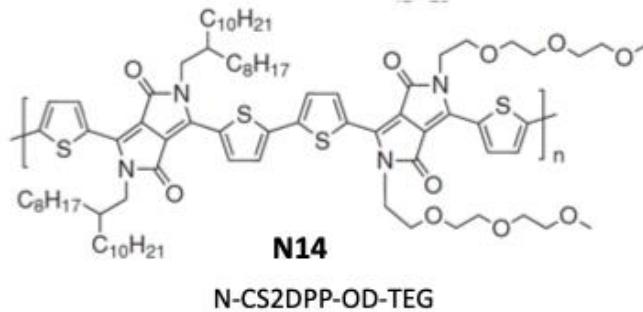
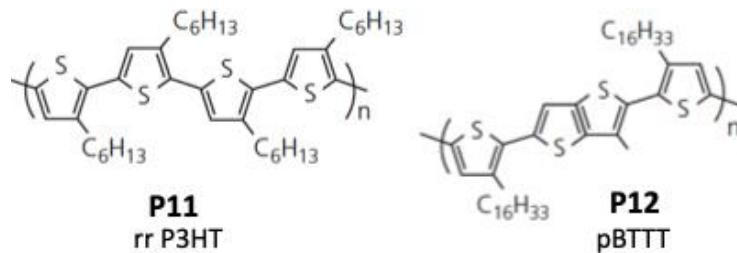
Example channel materials

Small molecule

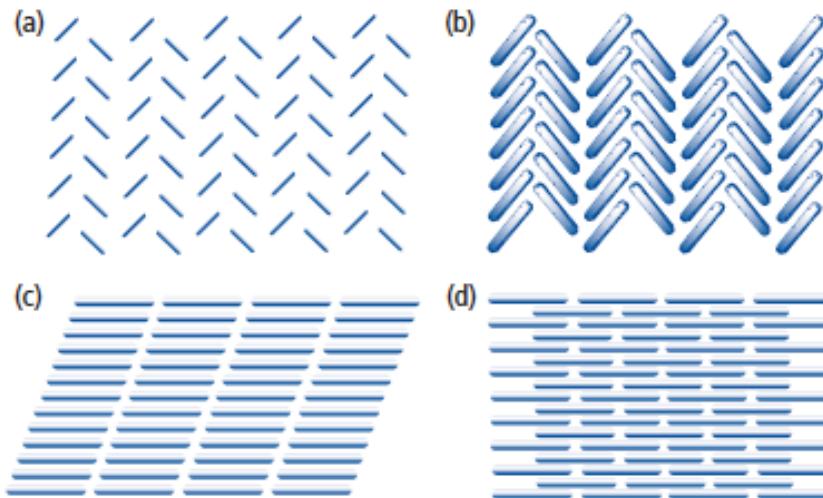


N = n-channel
P = p-channel

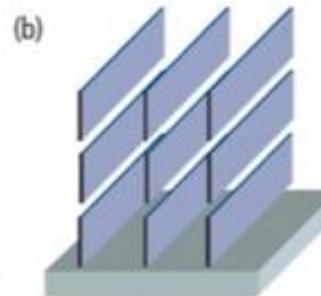
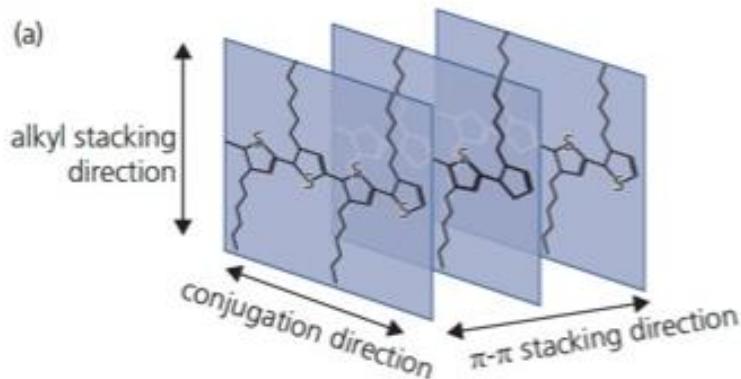
Polymer



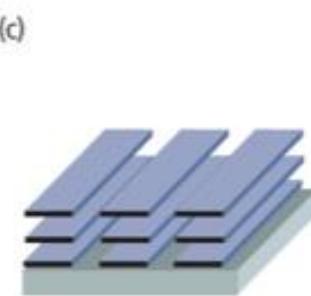
Highest mobilities when π -stacking is in the transistor plane



Different, common organic stacking motifs
(see Chapter 2)

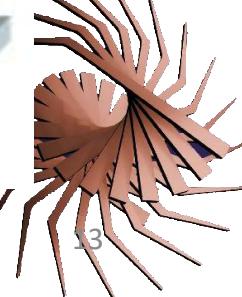


best vertical
conduction



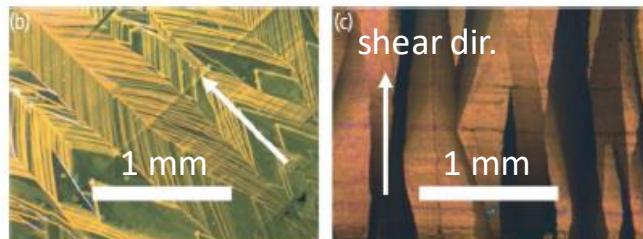
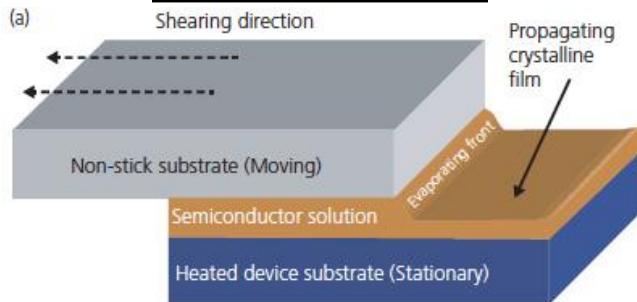
best in-plane
conduction

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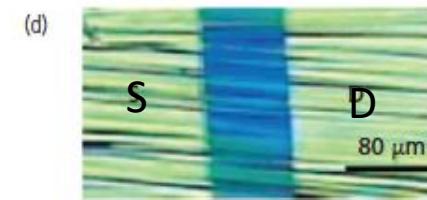
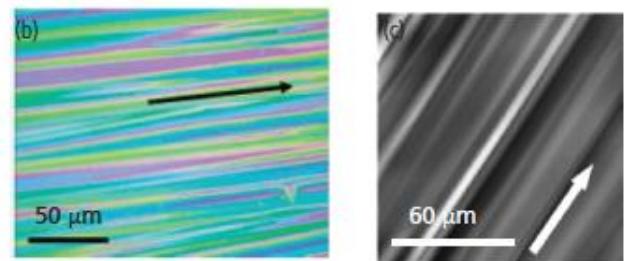
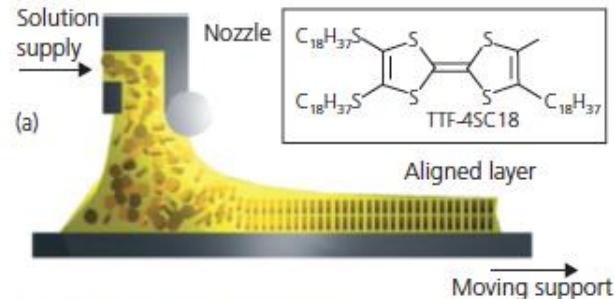
Methods for Orienting the Semiconductor

solution shearing



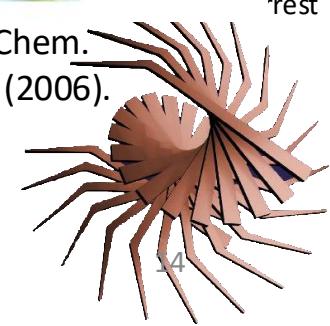
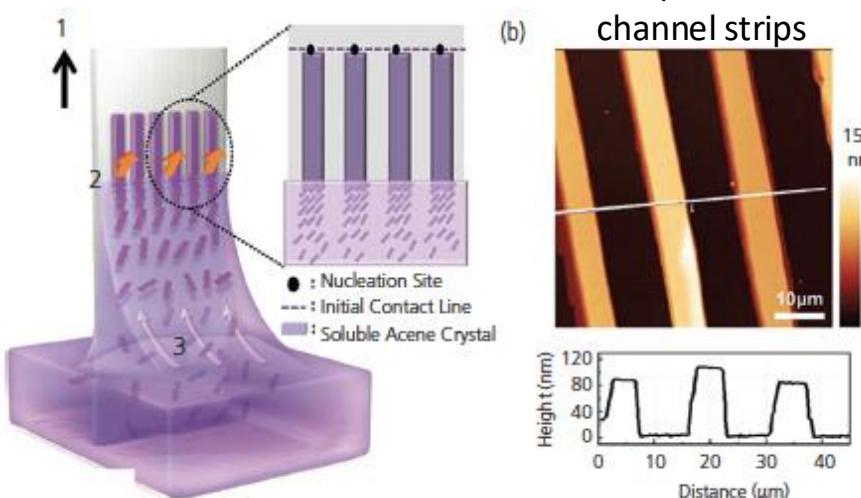
Liu, et al., Z. Adv. Materials, **21**, 1217 (2009)

zone casting



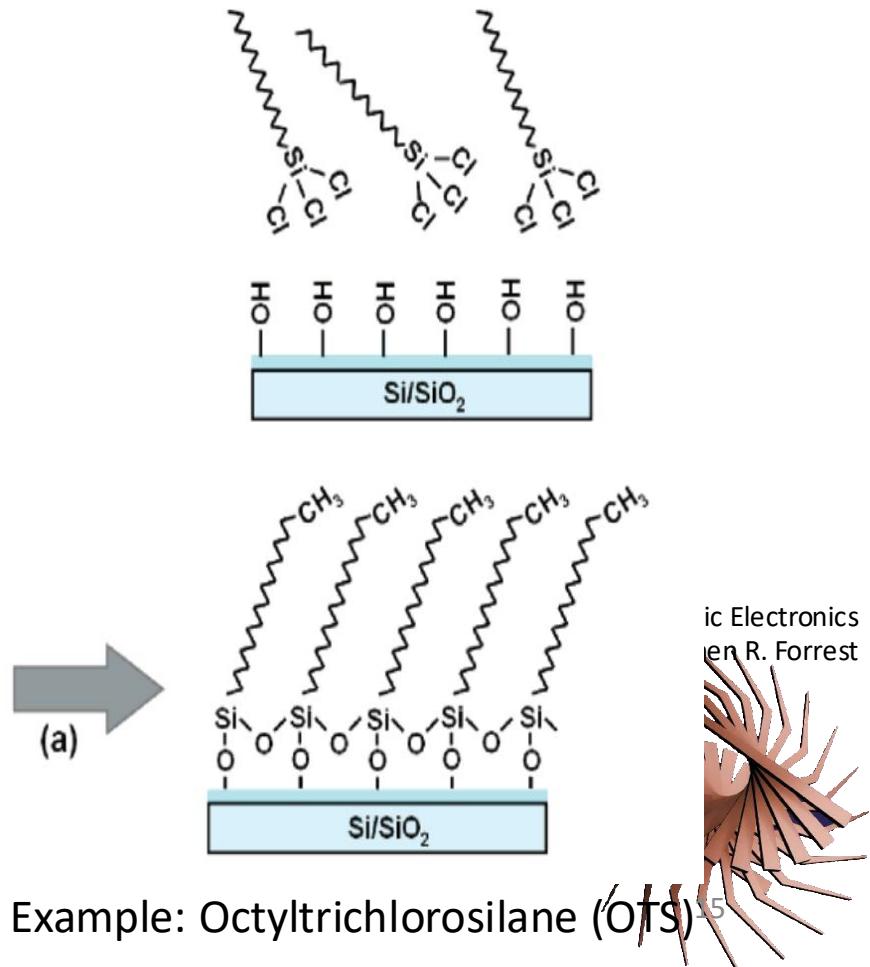
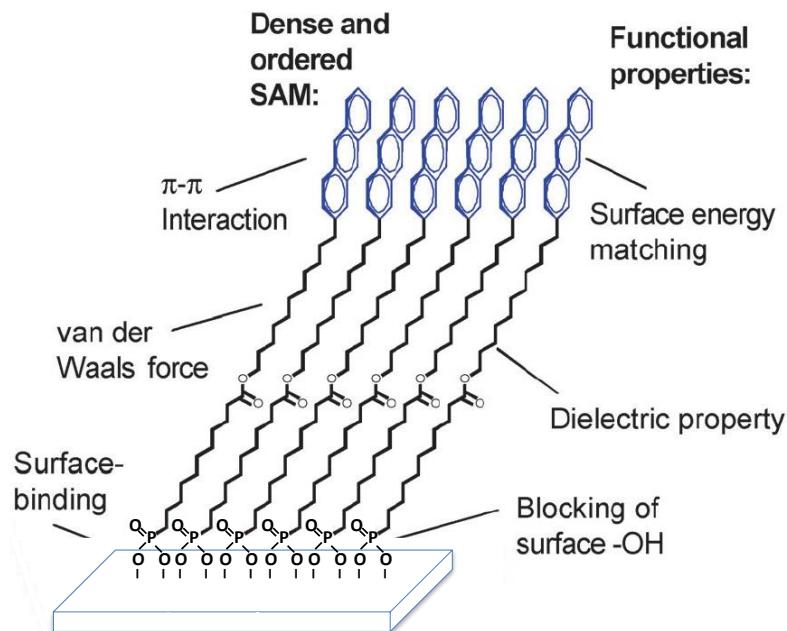
Miskiewicz, et al. Chem. Materials, **18**, 4724 (2006).

Jang et al., Adv. Functional Mater., **22**, 1005 (2012)



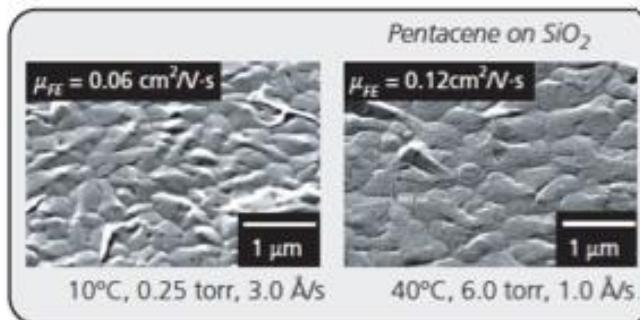
Achieving Optimal Morphologies

- Method 1: Control during growth by VTE, OVPD, solution
- Method 2: Use Self Assembled Monolayer (SAM) functionalization to initiate growth of desired structures by vapor or solution deposition

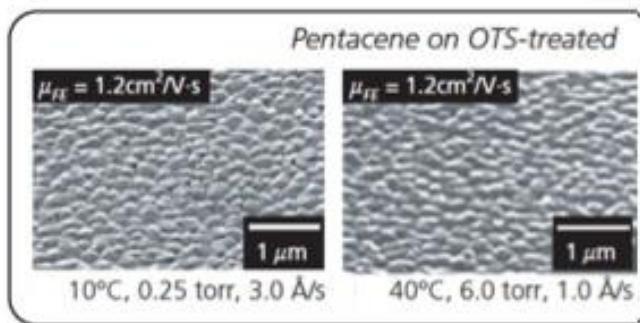


Achieving morphology through growth conditions & surface preparation

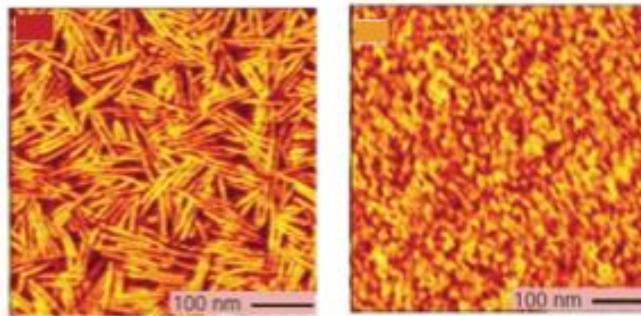
OVPD growth of pentacene



M. Shtein, et al. 2002. *App. Physics Letters*, **81**, 268-270.

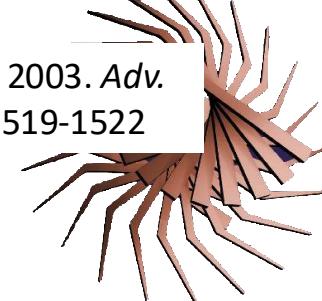


Solution growth of P3HT
on HDMS-functionalized
 SiO_2

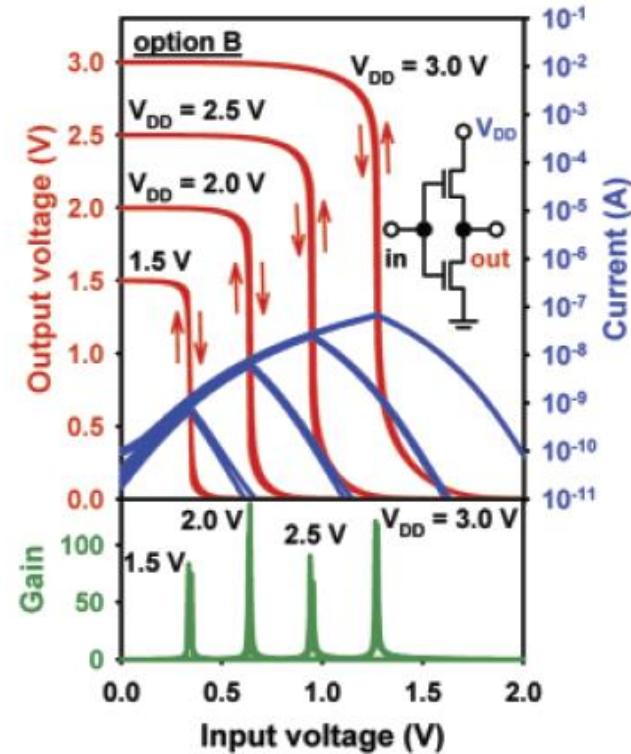
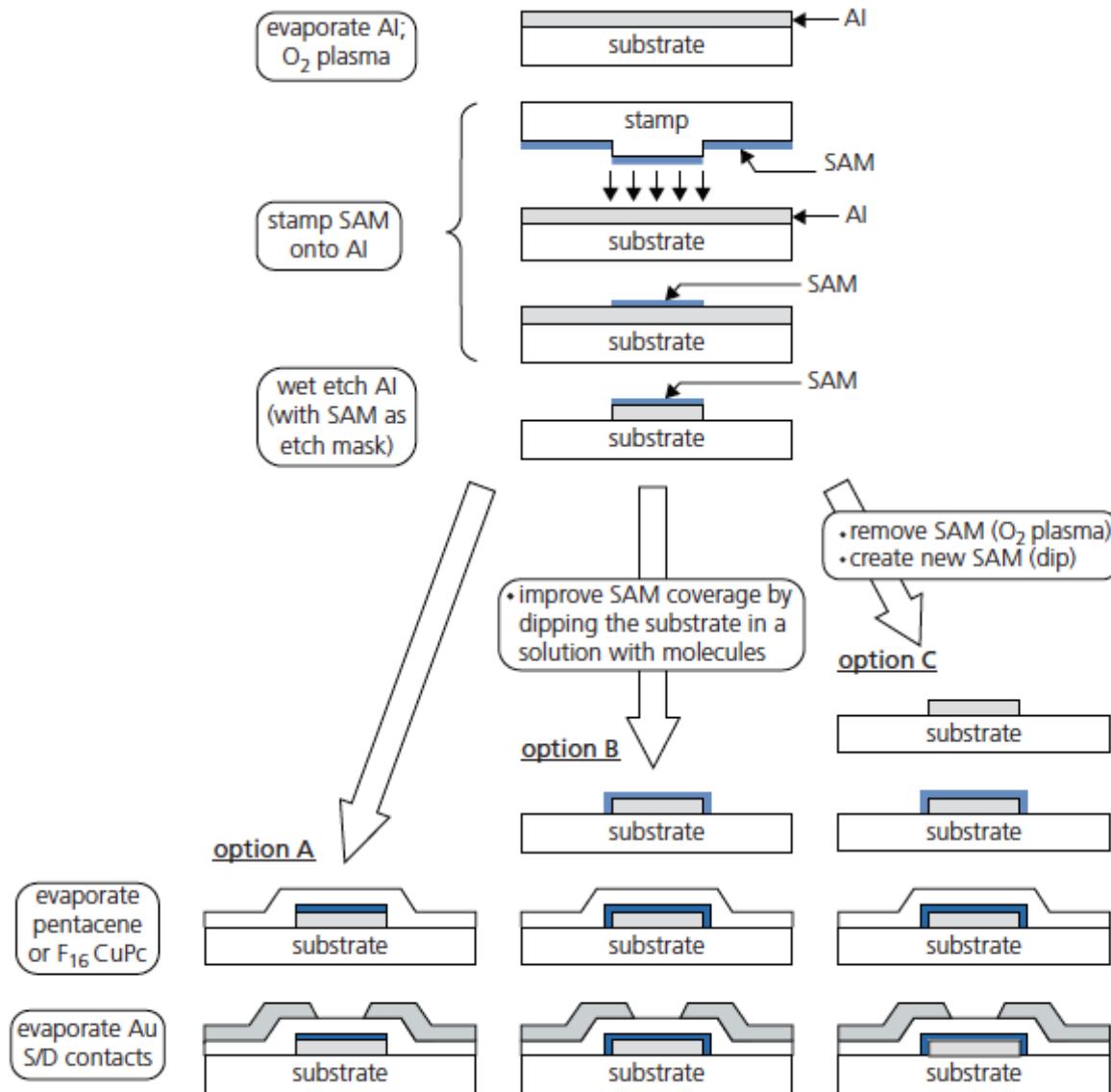


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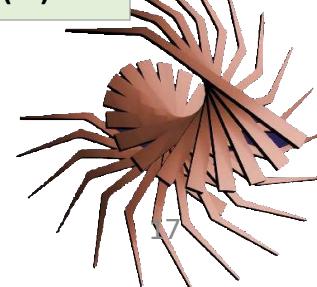
R. J. Kline, et al. 2003. *Adv. Materials*, **15**, 1519-1522



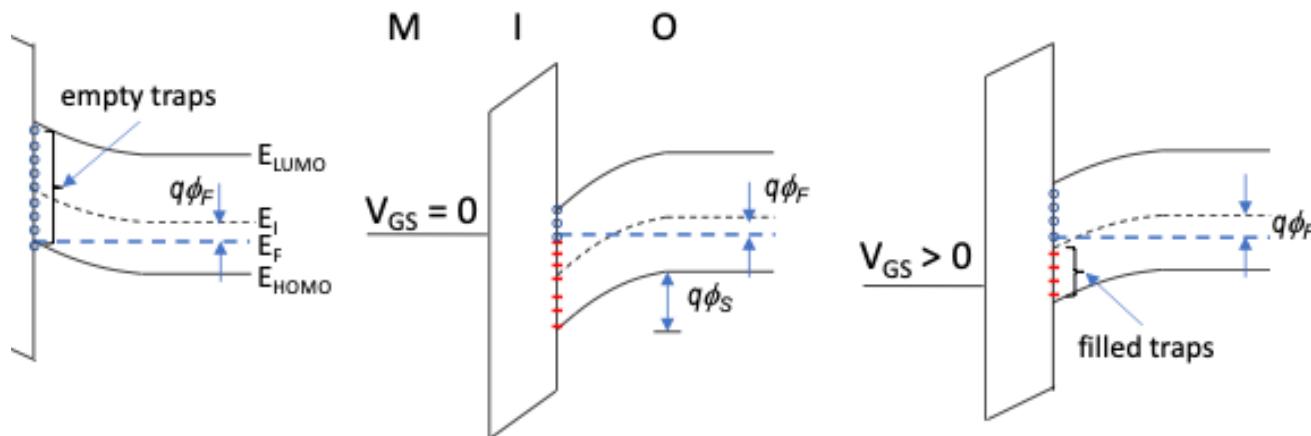
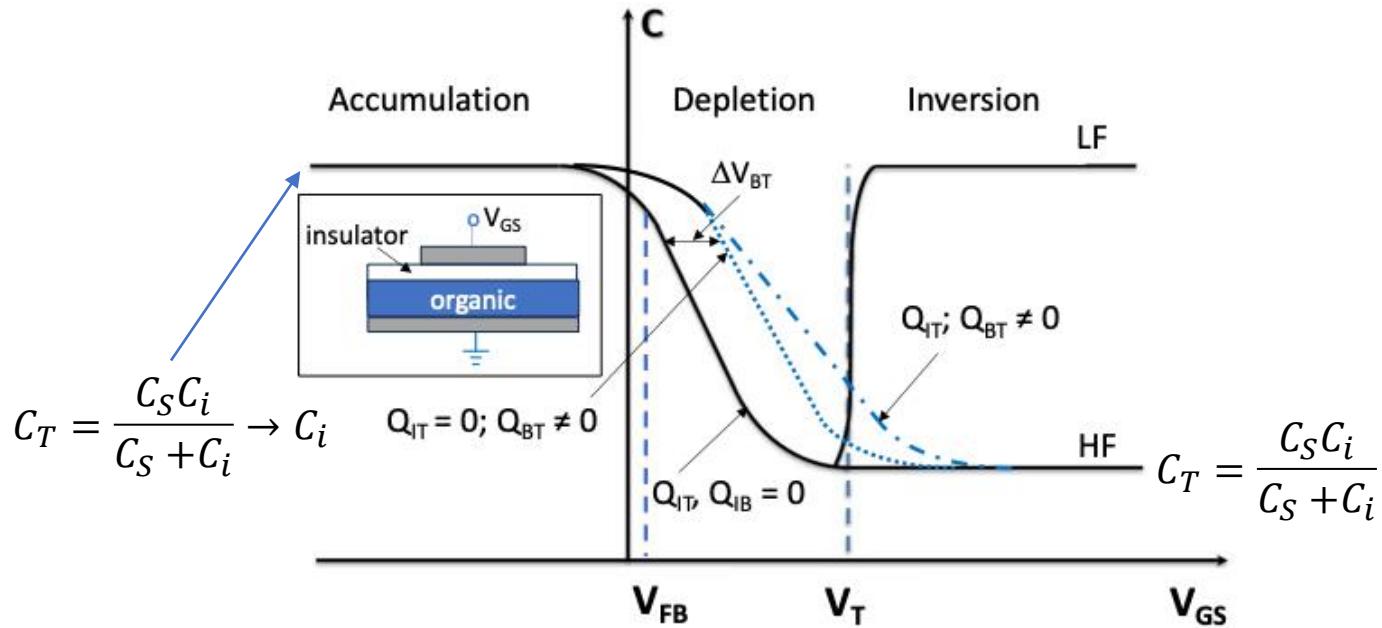
Contact Printing Initiated by SAM



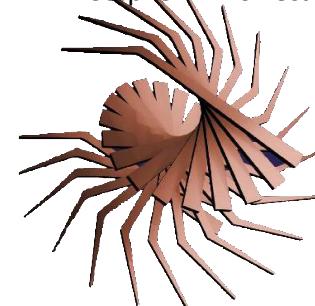
Pentacene (p)
F₁₆CuPc (n)



Interpreting gate C-V characteristics

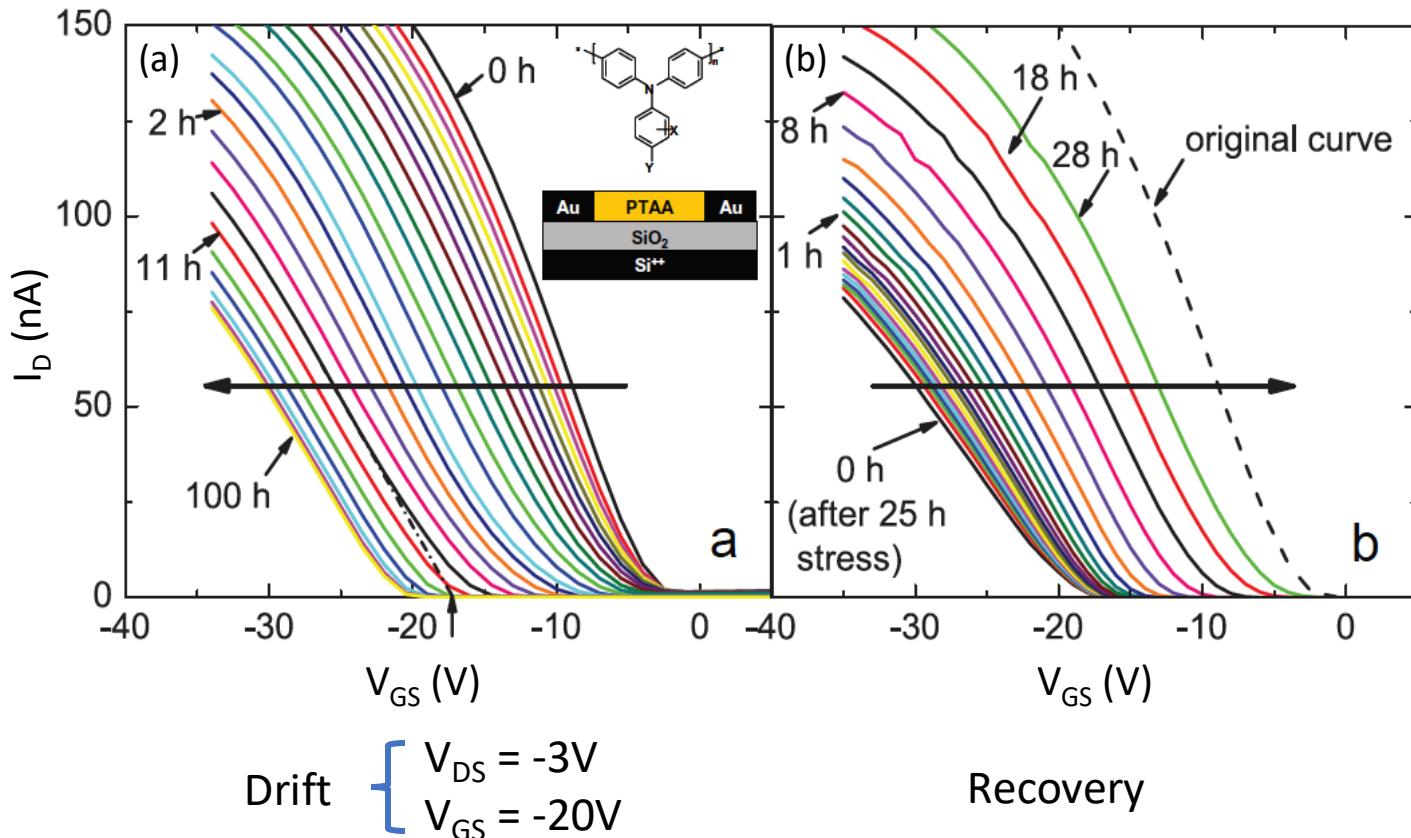


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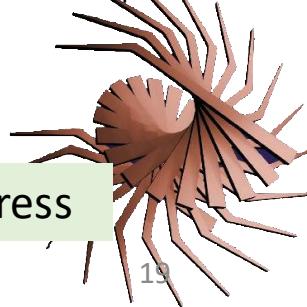


OTFT Stability

- Threshold voltage drift the primary source of circuit failure
 - Decreasing noise margin
 - Increasing leakage



Original transfer characteristics (and V_T) partially recovered following stress



Threshold voltage drift over time

(see Ch. 6.7 & 7.8)

- Drift due to charges migrating in insulator or channel toward the interface
 - Surface traps at the channel
 - Traps within the semiconductor bulk
 - Charge (ions) drifting within the insulator

$$\Delta V_T(t) = \Delta V_T(\infty) \left(1 - \exp\left(-\frac{t}{\tau}\right)^m \right)$$

Empirical voltage drift expression:
Stretched exponential

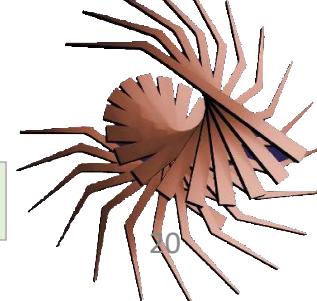
$m = T/T_0$ for exponential trap distribution given by:

$$h_{tr}(E) = h_{tr0} \exp(-E/E_T)$$

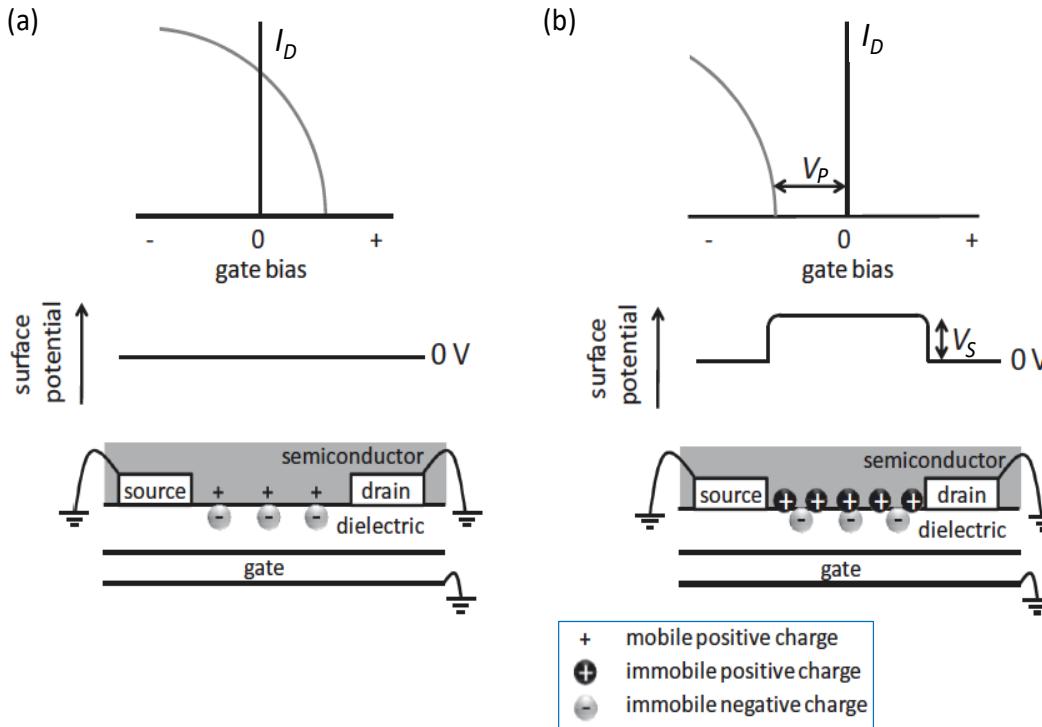
⇒ Time constant for drift

$$\tau = (2\pi\nu)^{-1} \exp(E_T/k_B T)$$

Drift occurs over an extended time, and is thermally activated



Water results in ionic charge at interface \Rightarrow charge trapping

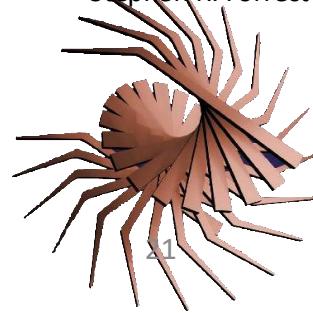


Water is the main problem: Proton generation

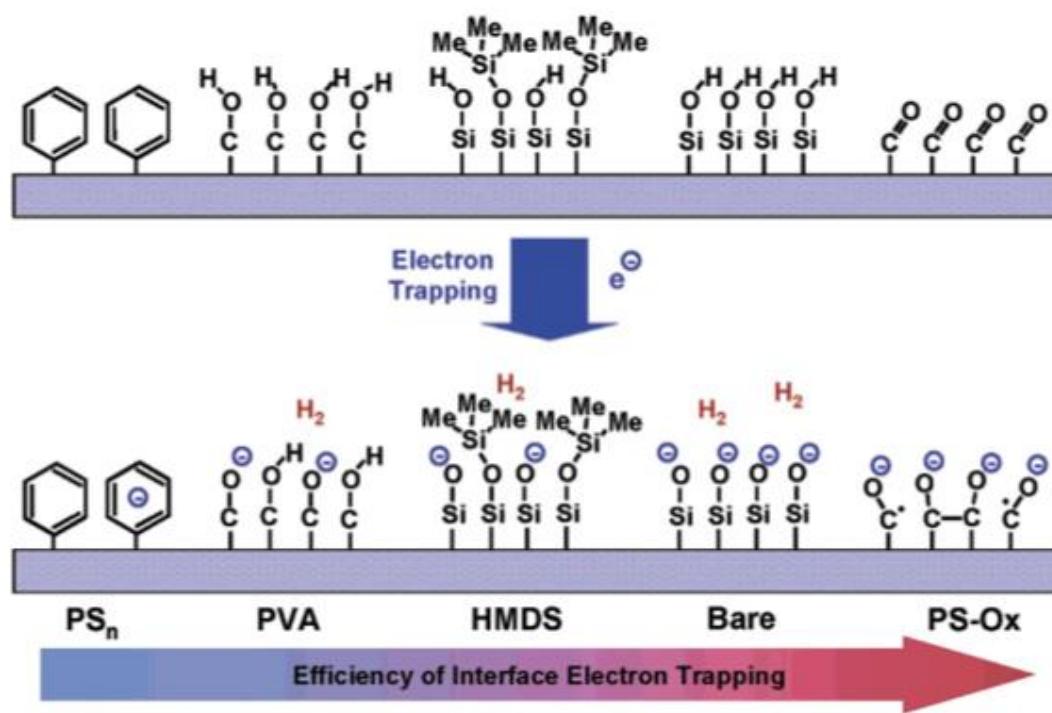


Mathijessen et al., Adv. Mater. **22**, 5105 (2010)

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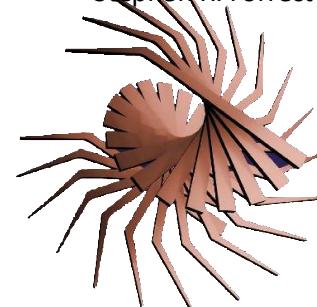


SAMs can passivate the SiO₂ surface and reduce ΔV_T .

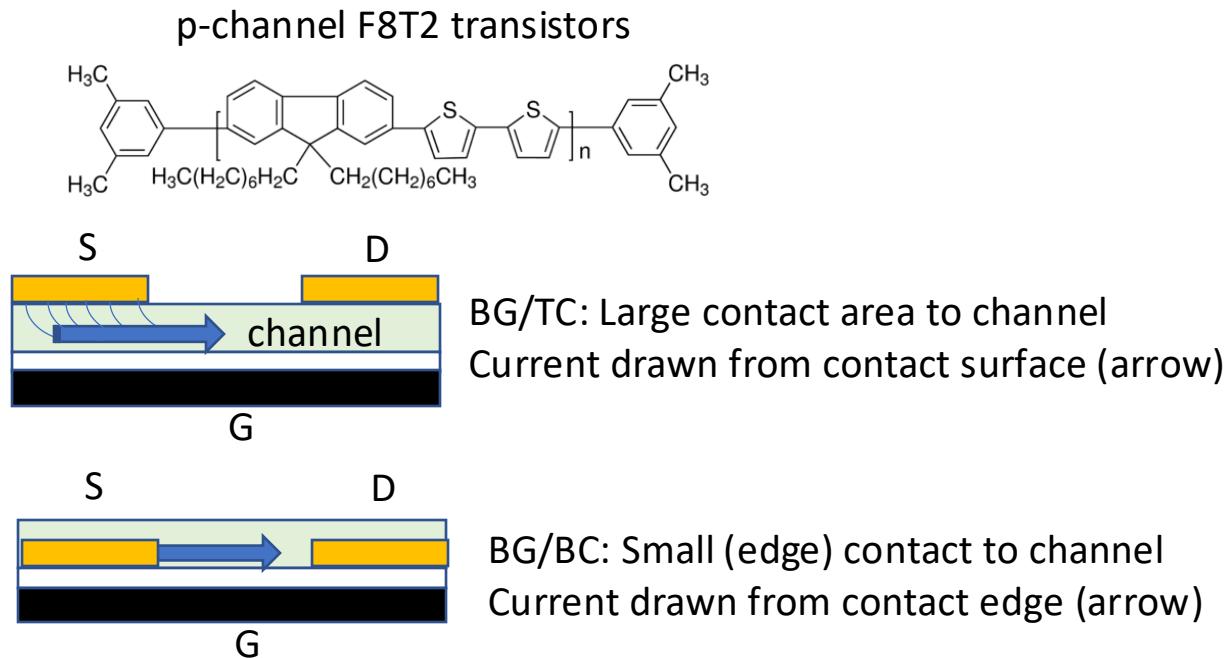
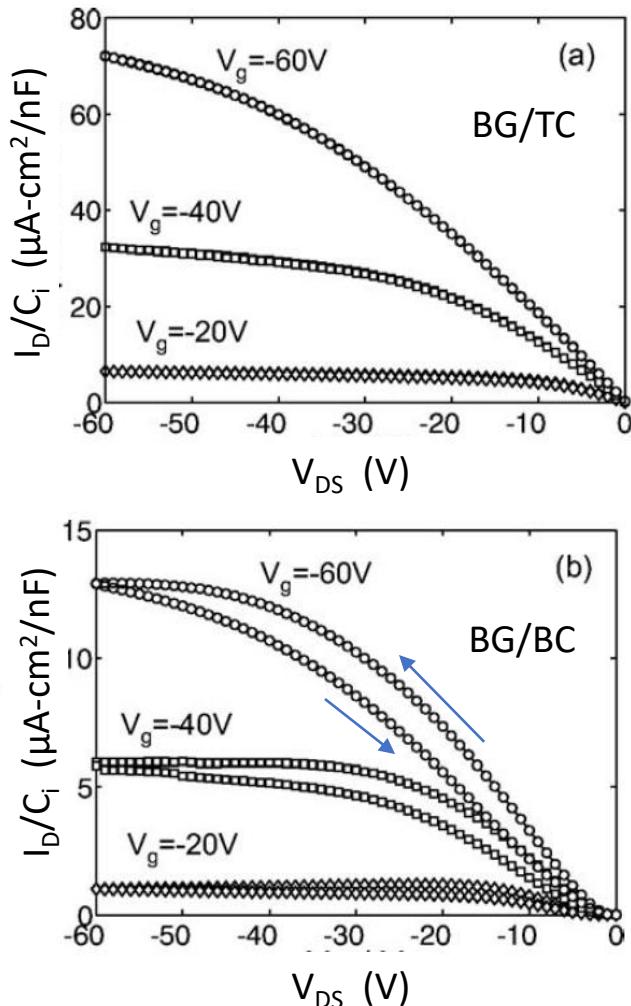


M.-H. Yoon, et al. 2006. *JACS*, 128, 12851-12869

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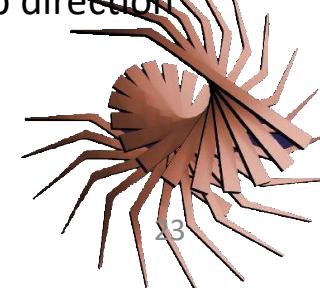
Hysteresis: Another failure mode



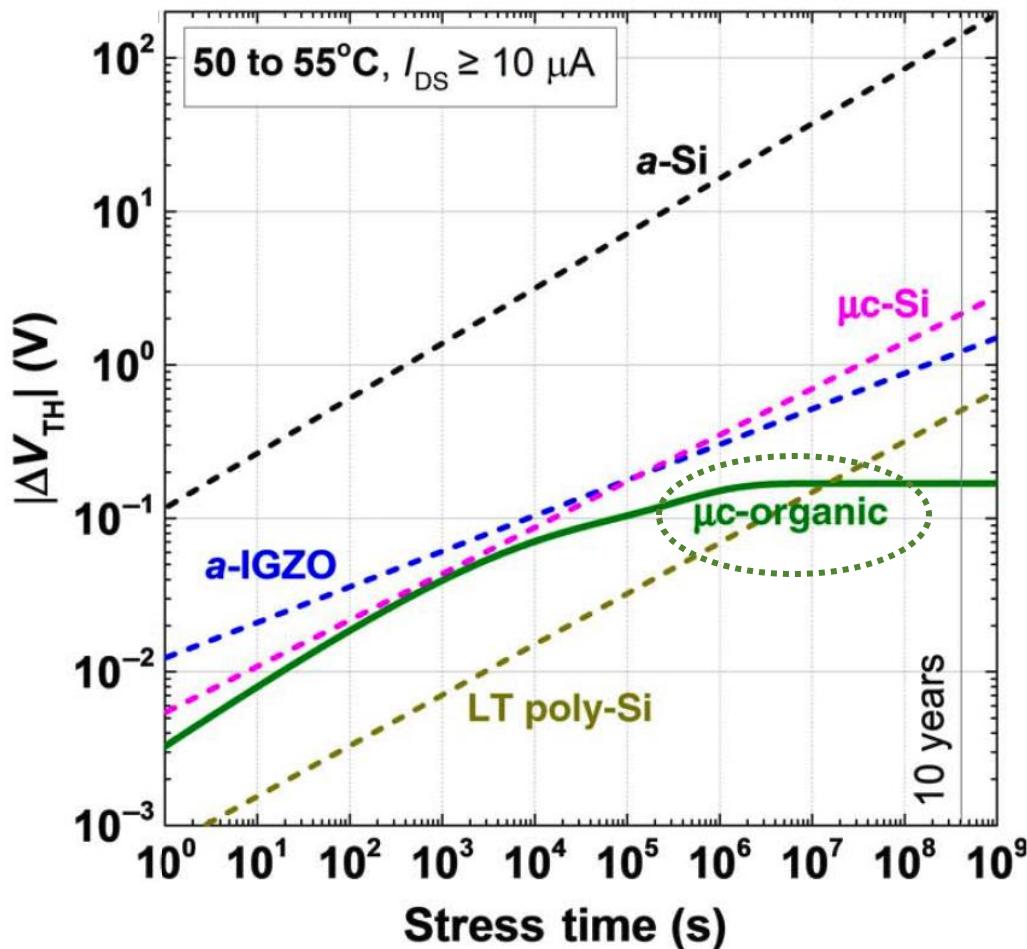
Drain contact trapping

Contact only via edge of the electrodes increases the current density, resulting in defect formation and charge trapping. This induces changes in V_T and I_{DS} , depending on sweep direction (arrows)

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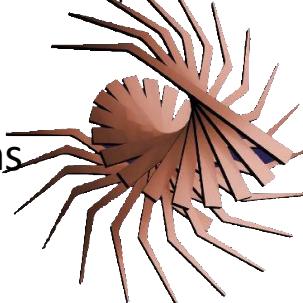


Comparison of TFT Reliabilities



Jia, et al. Science Adv. 4, eaao1705, (2018)

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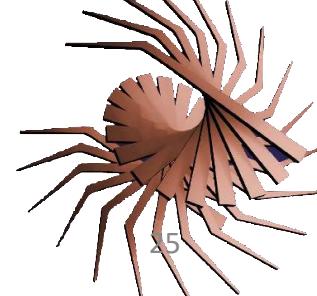
Caveats (and there are many):

- Devices from different labs may be based on different standards and conditions
- Device selection not necessarily based on same characteristics
- Performance can vary over a wide range in any technology

Applications must exploit advantages, and cannot be vulnerable to disadvantages

To review....

- PROs
 - Flexible, conformable, ultralight
 - Can be made over very large areas
 - Suitable for large scale R2R manufacture
- CONS
 - Cannot source large currents
 - Characteristics drift over long periods in operation
 - Limited bandwidth (≤ 1 MHz in many cases)



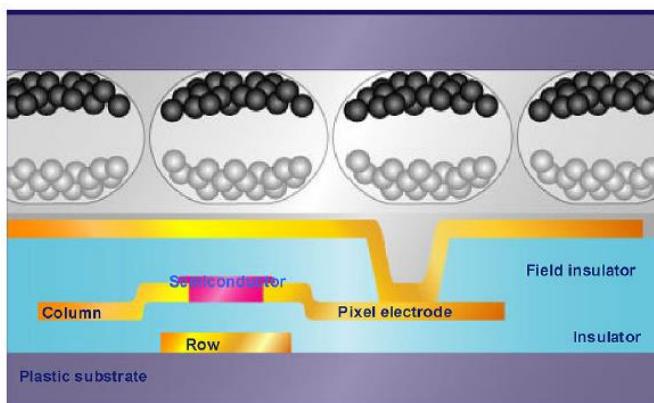
Voltage driven display backplanes

- Electrophoretic displays

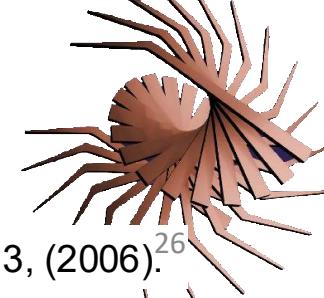


320 x 240 QVGA display
Display pixels are voltage (not current) driven

QVGA=quarter video graphics array



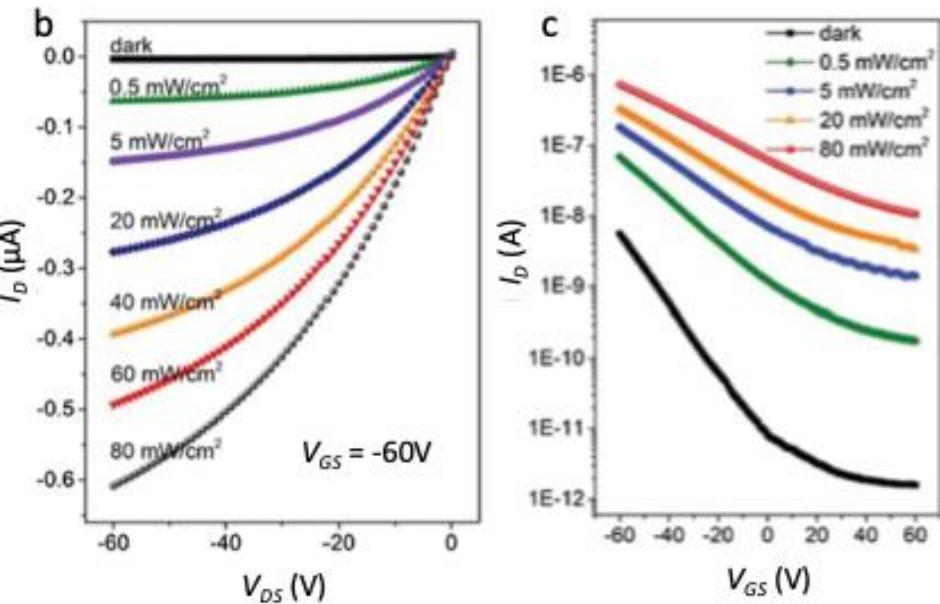
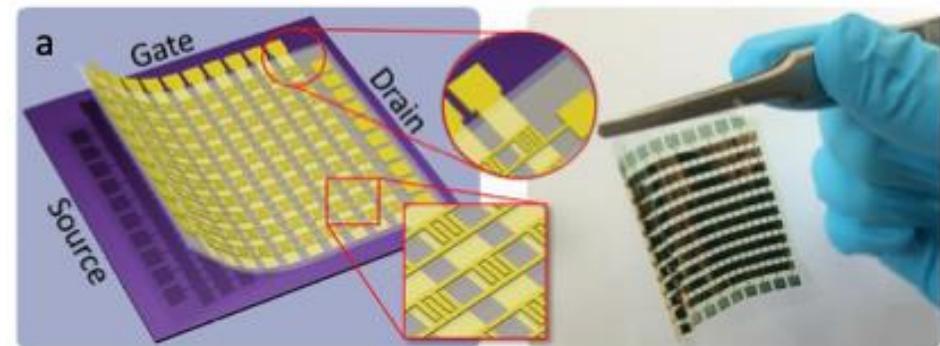
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G. Gelinck et al J. Soc. Info. Display, 14, 113, (2006).

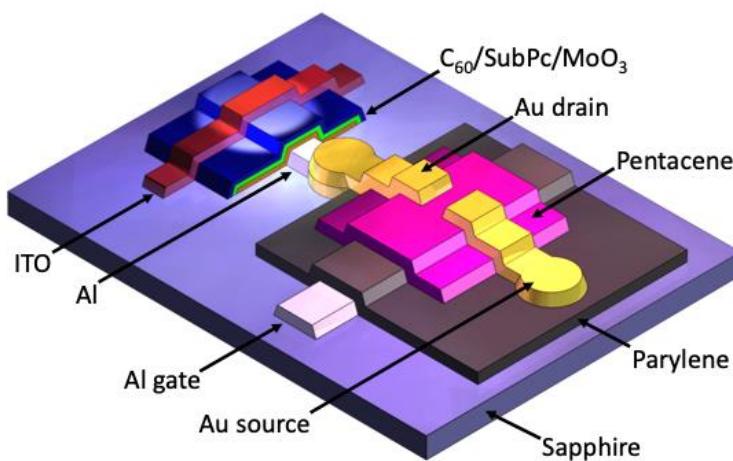
Imaging devices

Phototransistor imaging array



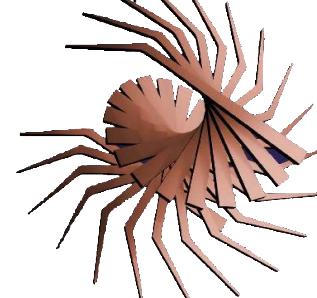
Y. Chu, et al, J. 2016. *Advanced Science*, 3

Passive pixel sensor element for detector arrays

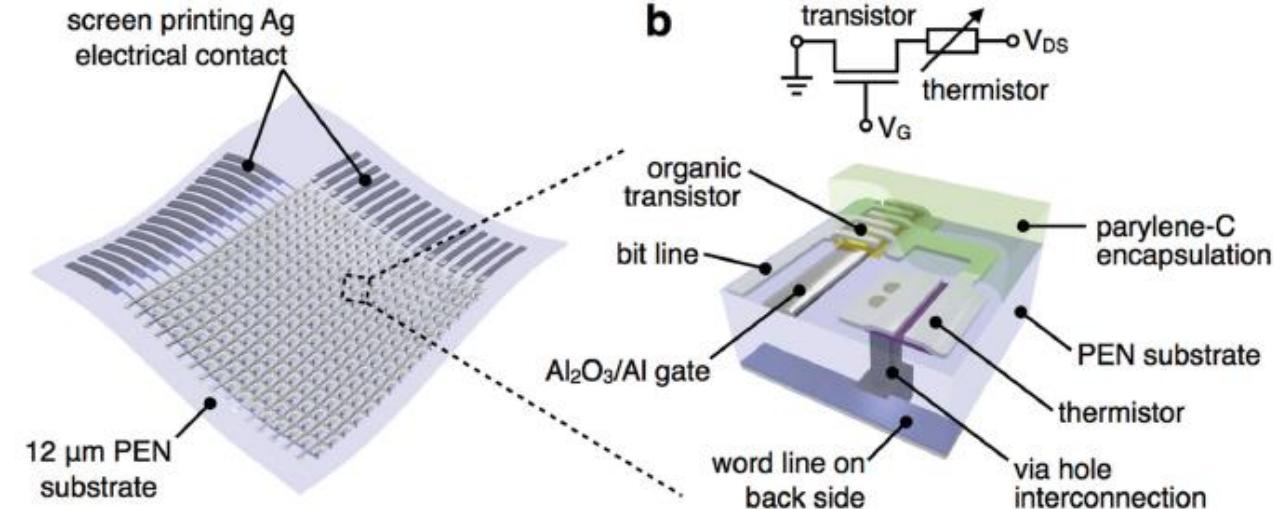


X. Tong, & S. R. Forrest, 2011. *Org. Electron.*, **12**, 1822-1825.

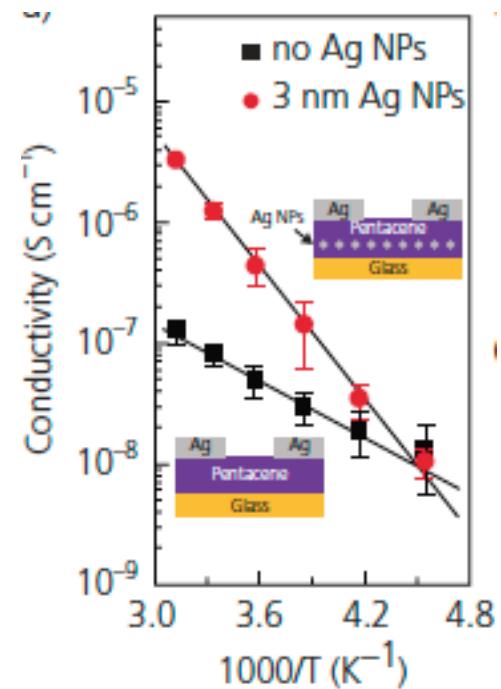
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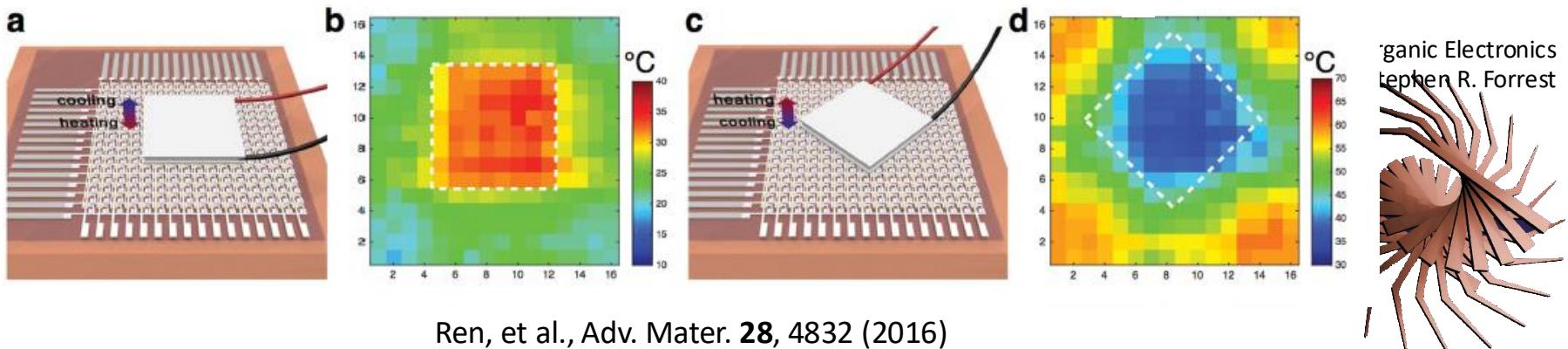
Thermal Position Sensing



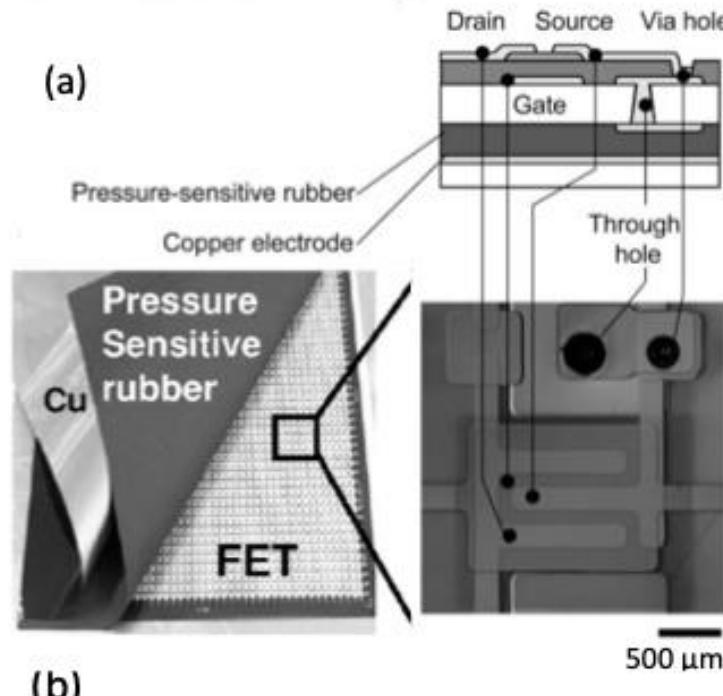
Array used for detecting position of thermal source



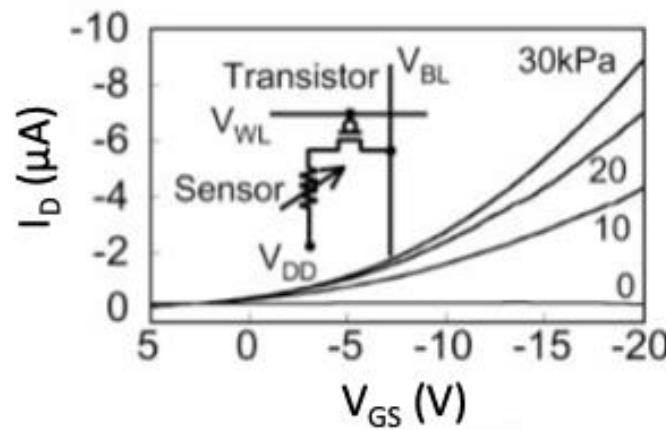
Sensing element: channel resistance with a Ag NP layer



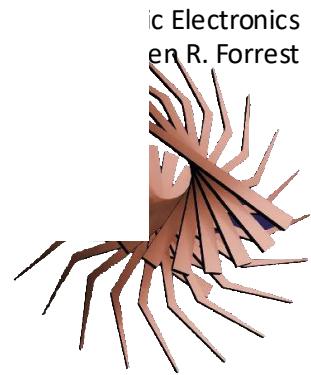
Tactile sensor arrays



(b)



Y. Noguchi, et al.. 2006. *Applied Physics Letters*, 89, 253507



Chemical sensing

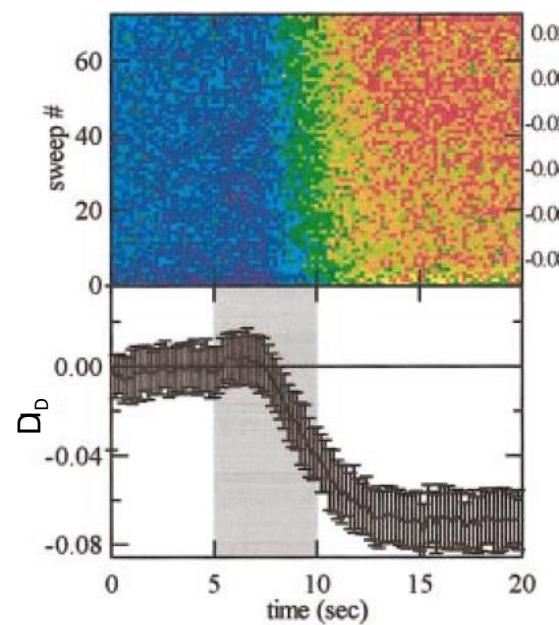
- OTFTs have demonstrated voltage drifts due to water.
- Are there other analytes that can be sensed?
- Sensor attributes
 - Fast
 - Sensitive to small doses
 - Reversible
 - Specific

α -6T transistor

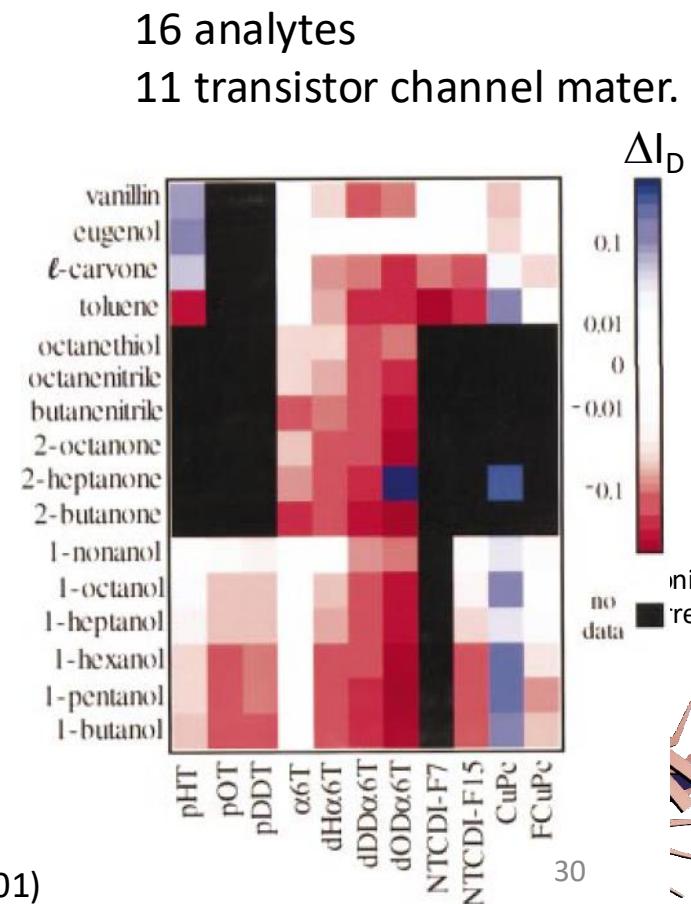
Analyte: 1-hexanol

Exposure: 5 s

Recovery: 1 min

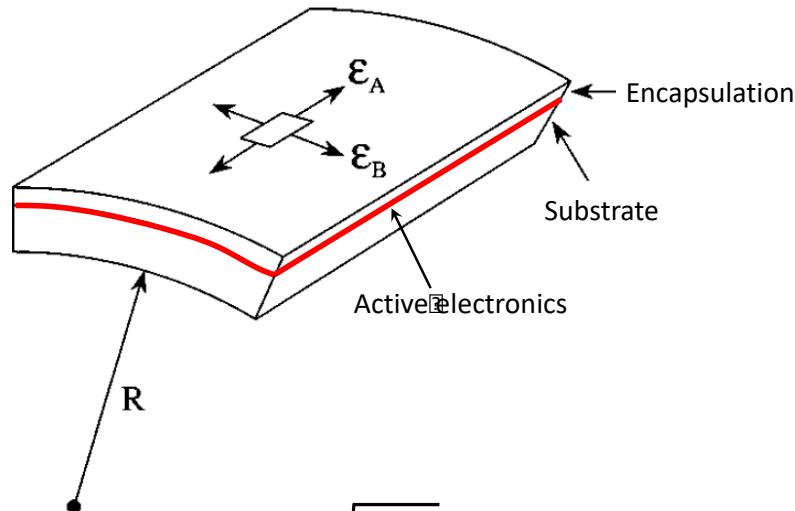


B. Crone *et al.*, 78, 2229, (2001)



Bendable Electronics

Placing active electronics at the neutral strain point
⇒ minimal stress to circuits on bending even over sharp angles

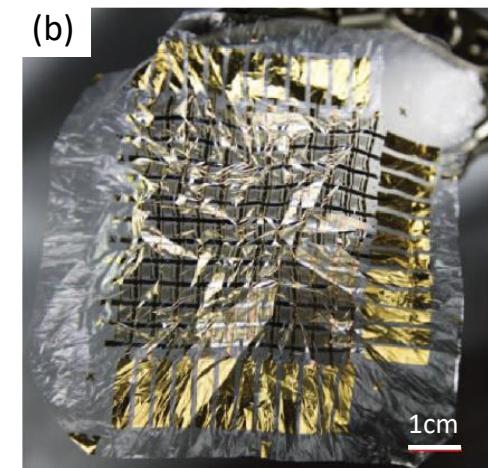


Neutral strain:
$$\frac{d_{sub}}{d_e} = \sqrt{\frac{Y_e}{Y_{sub}}}$$

Y = Young's modulus (measure of material stiffness)

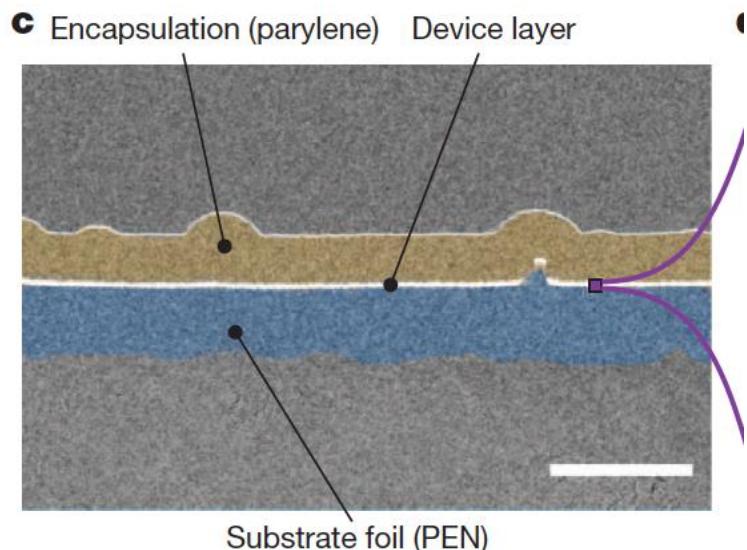
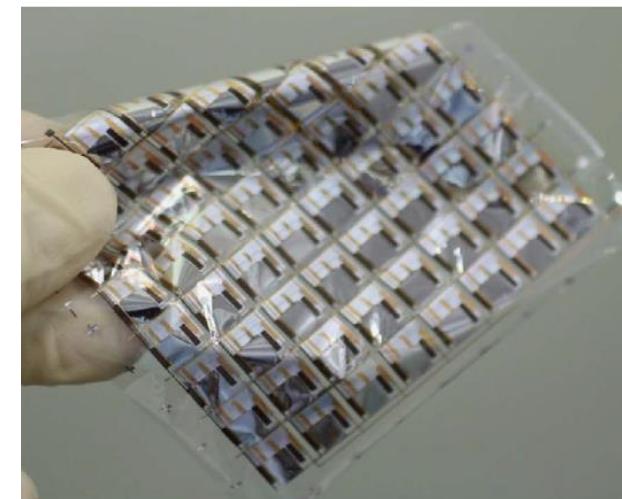
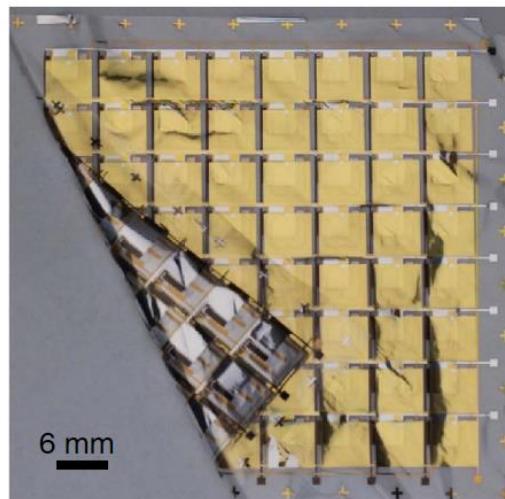
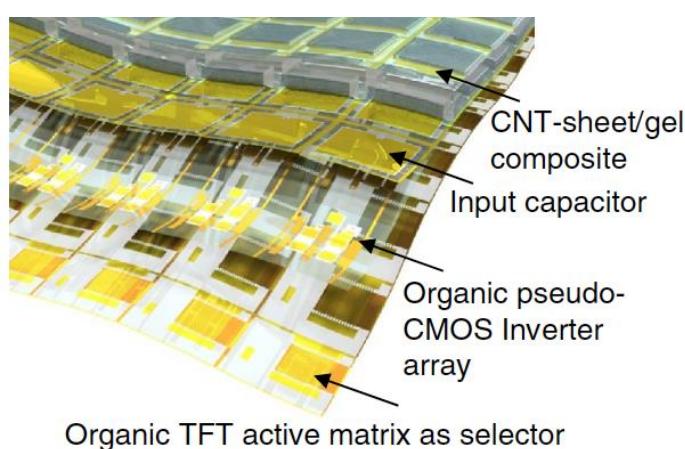
$$Y = \frac{F L_0}{A \Delta L}$$

F = force to extend solid
 L_0 = original length
 ΔL = length change
 A = cross sectional area perpendicular to F

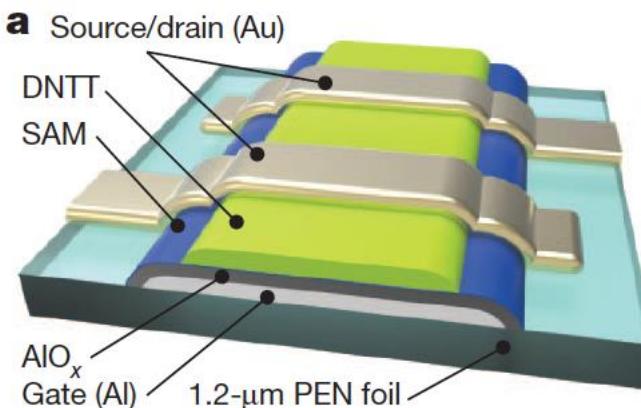


12x12 array of tactile pixels

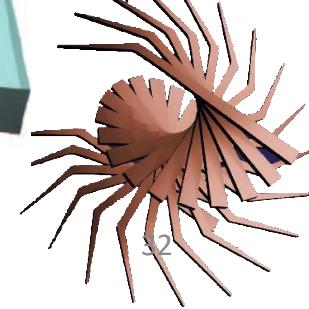
“Imperceptible” Electronics



Substrates are 1 μm thick!

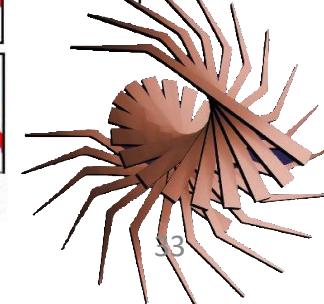
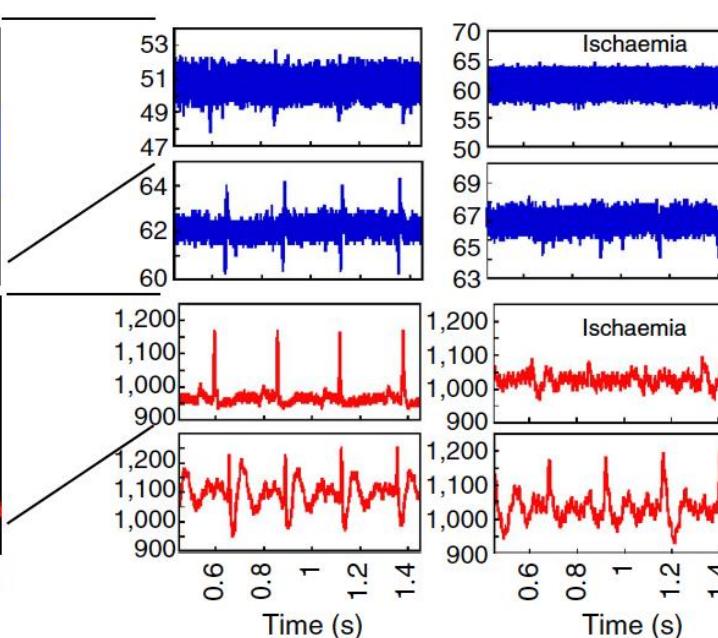
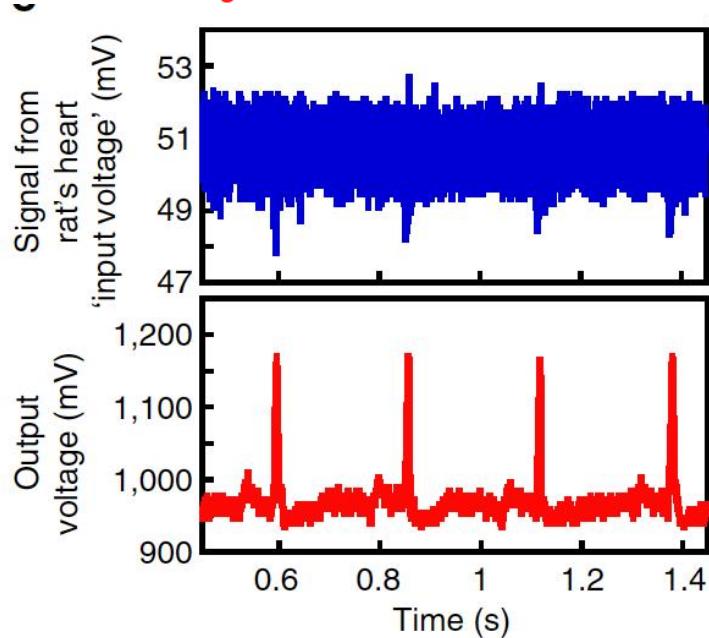
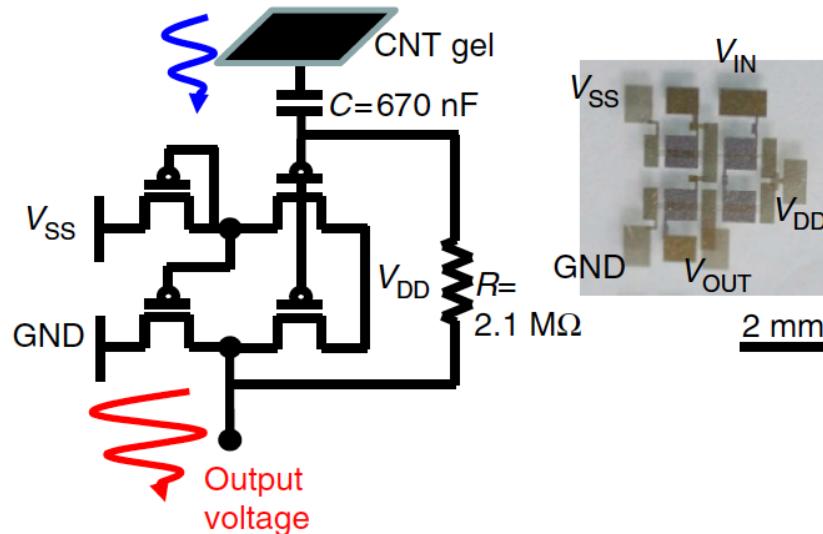


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In Vivo Cardiac Monitoring

Input biosignal from the heart



What we learned

- OTFTs have made extraordinary progress since their first demonstration in 1986
- Their properties can be modified through chemical design
- Morphology is key to high performance
- Very small gate transistors are common in BG/TC configurations
- Very large circuits demonstrated (100's of transistors)
- Reliability depends on exposure to contaminants
- Most promising applications in sensing and medicine
- But....there is no “killer app” yet identified that can drive this technology to a commercial success

