Goals

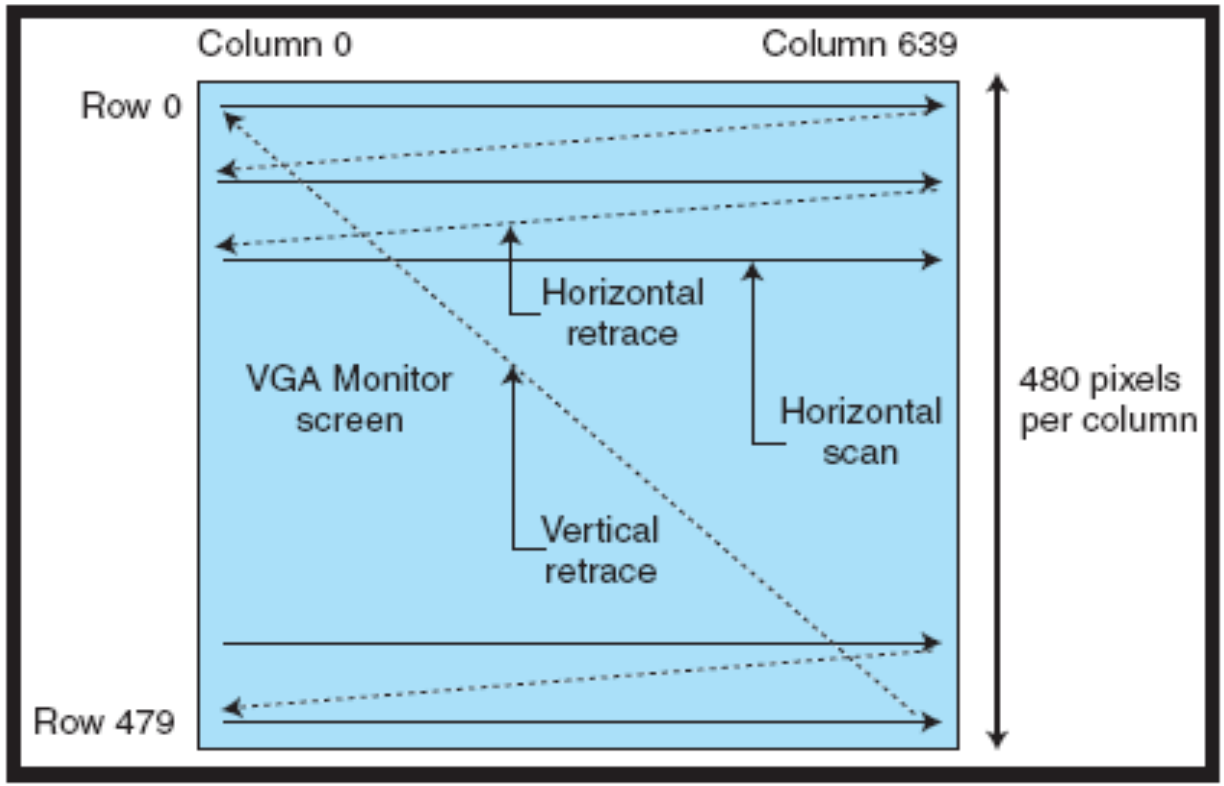
- Learn how to use the FPGA to output to the VGA Adapter.
- On completion, you will know how to:
  - Create a Verilog module to drive a VGA display.
  - Display 8 different colors sequentially, controlled by the push button.

VGA Display Basics

- A 640x480 VGA screen is shown to the right.

- Pixels are drawn left to right to create a “line” and then, lines are drawn top to bottom to create a “frame”.

- To program an FPGA to drive the display, timing the signals for the VGA monitor is essential.

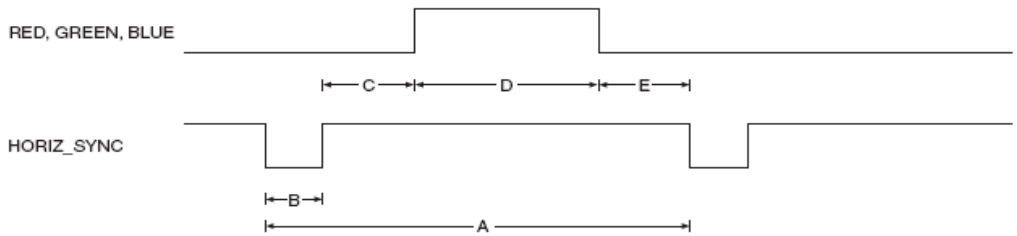


VGA Timing Diagram

- The Horizontal and Vertical refresh cycles' timing is given in terms of time (s). You will have to convert these into counts based on clock cycles.

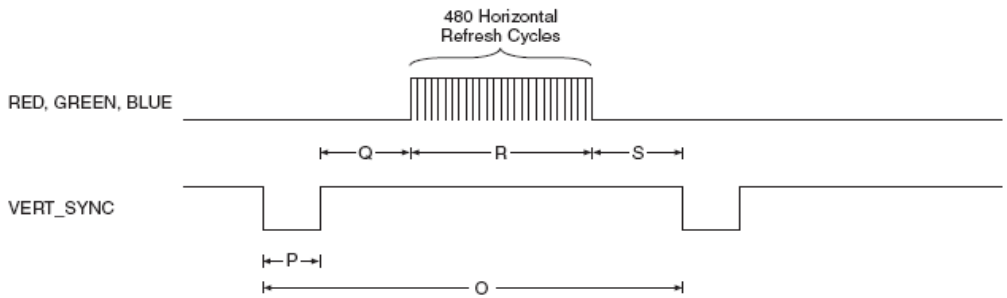
- Notice that timing for the Vertical Refresh can be calculated as multiples of Horizontal refresh cycles.

Figure 13. Horizontal Refresh Cycle



Parameters	A	B	C	D	E
Time	31.77 µs	3.77 µs	1.89 µs	25.17 µs	0.94 µs

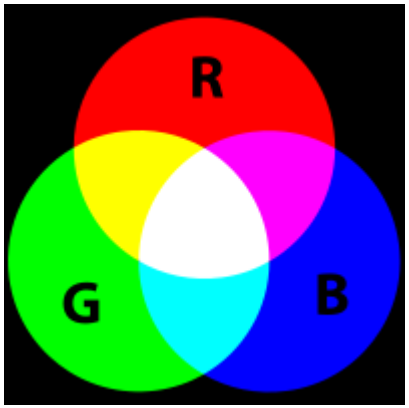
Figure 14. Vertical Refresh Cycle



Parameters	O	P	Q	R	S
Time	16.6 ms	64 µs	1.02 ms	15.25 ms	0.35 ms

http://www.altera.com/literature/univ/upds.pdf

Video D/A Converter



(0, 0, 0) is black

(255, 255, 255) is white

(255, 0, 0) is red

(0, 255, 0) is green

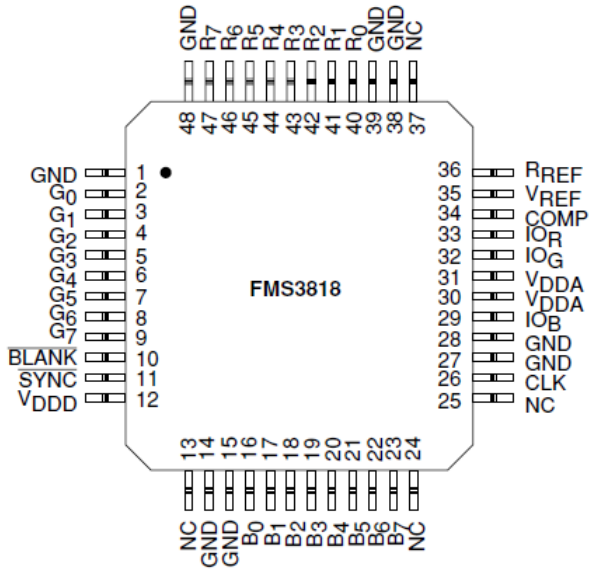
(0, 0, 255) is blue

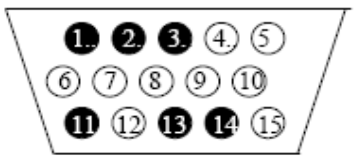
(255, 255, 0) is yellow

(0, 255, 255) is cyan

(255, 0, 255) is magenta

Digital 8-bit per channel





Signal	D-Sub Connector Pin
RED	1
GREEN	2
BLUE	3
GND	6, 7, 8, 10, 11
HORIZ_SYNC	13
VERT_SYNC	14
No Connect	4, 5, 9, 15

http://www.fairchildsemi.com/ds/FM%2FFMS3818.pdf