



# Goals

- Learn how to use the FPGA to display PS/2 input on VGA monitor
- Learn how to initialize and use memory on the FPGA

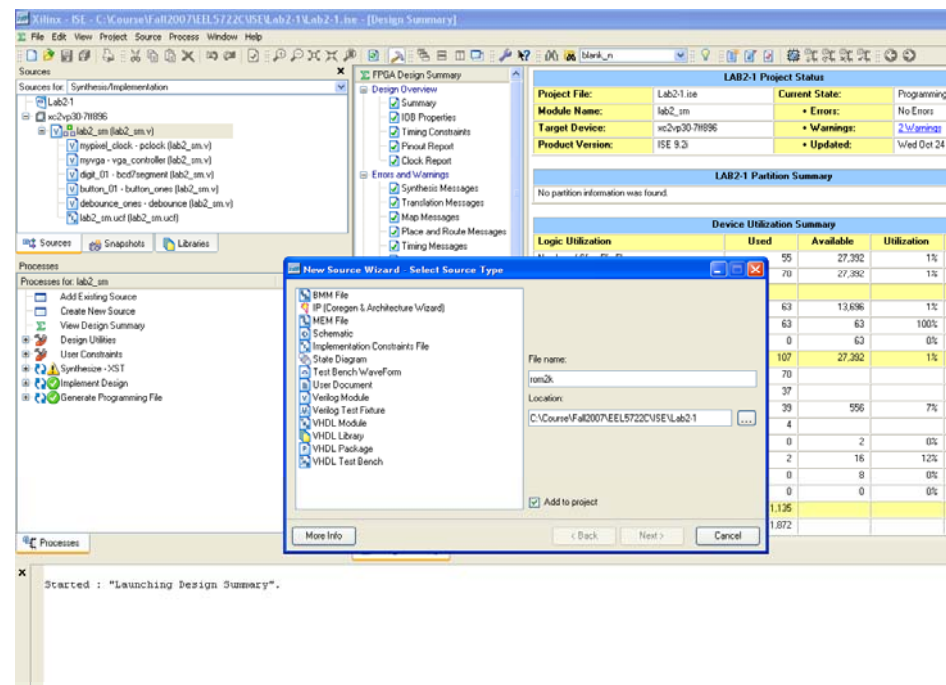


# Procedure

- Use FPGA memory to store a character map.
- Use Coregen to generate the memory module, use the given .coe file to initialize the memory content with the character map.
- Instantiate the memory in the top level module and access it using the provided address and data buses.
- Pin assignment:
  - Lab 2 UCF for the VGA.
  - Lab 3 UCF for the keyboard.

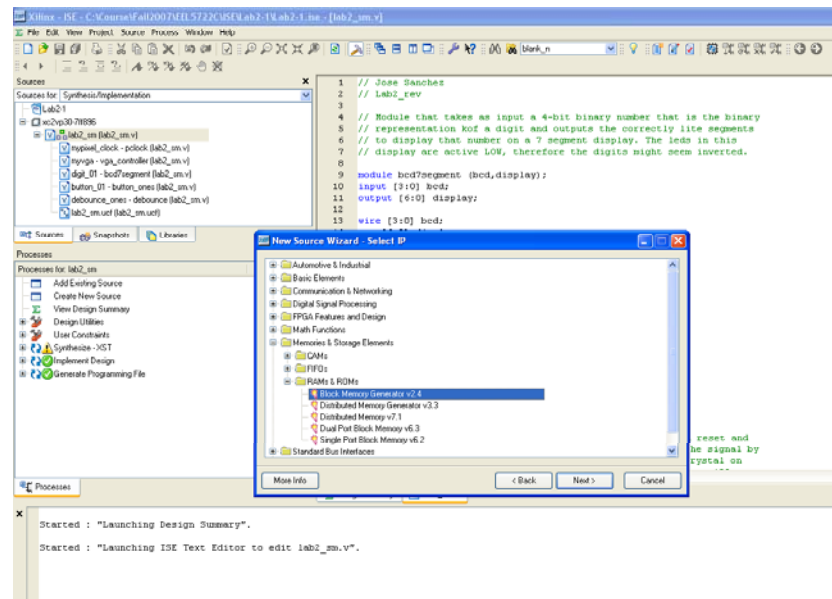
# Using Xilinx Coregen

1. Select *Project->new source->IP* (coregen & architecture wizard) ->Next



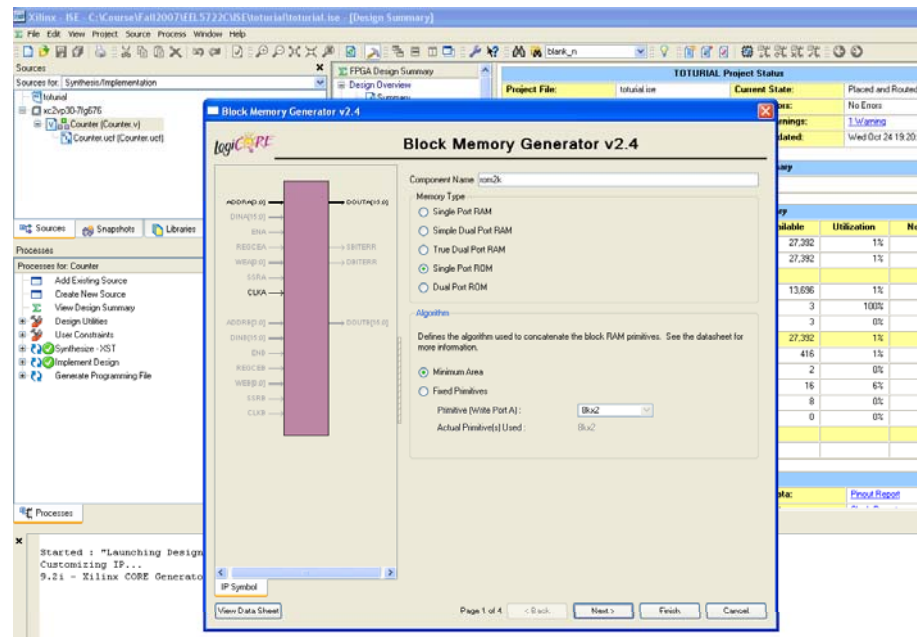
Age Group	Percentage
18-24	~35%
25-34	~25%
35-44	~15%
45-54	~10%
55-64	~8%
65-74	~5%
75-84	~3%
85+	~2%

2. Select *Memories & Storage Elements* -> *RAM & ROM* -> *Block Memory Generator v2.4* -> *Next* -> *Finish*



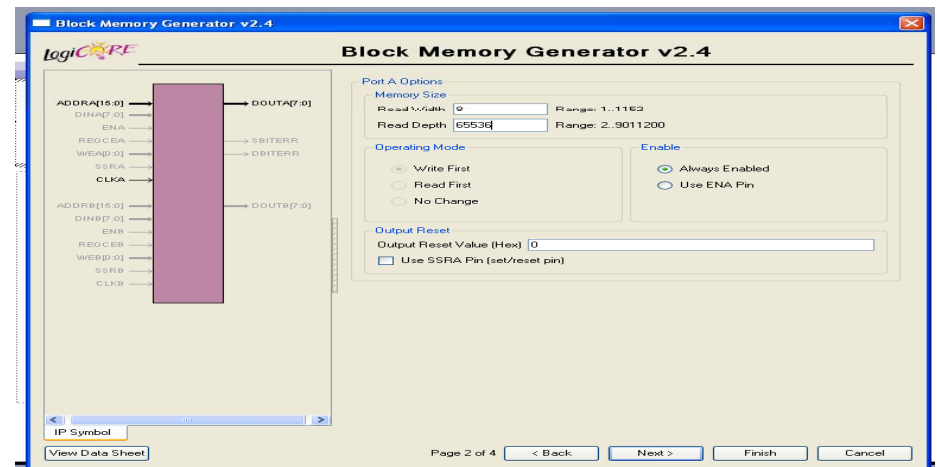
# Using Xilinx Coregen

## 3. Select *Memory Type: Signal Port ROM* *Algorithm: Minimum Area -> Next*



# Using Xilinx Coregen

4. Select *Memory size: Read Width:8; Read Depth128; Enable: Always Enable; Output Reset:0* ->Next
- 5 Select Initial File using the “*Character\_map.coe*” ->Next->Finish
6. Select *Edit->Languages Template-> Coregen-> Verilog Component Instantiation*, you can see the new generated core interface definition.
7. Use the core as regular module





# Description of Assignment

- Use the Keyboard to get input
- Pressing any of the number keys (0-9) on the keyboard should display that number in the upper-left corner of the VGA monitor
- Pressing the Enter (Return) Key should clear the screen to a blank screen
- Pressing any other key should display the character “E” on the monitor
- You are free to choose the color of the character displayed
- You can use the *character\_map.coe* file provided, which defines the “font” for the characters