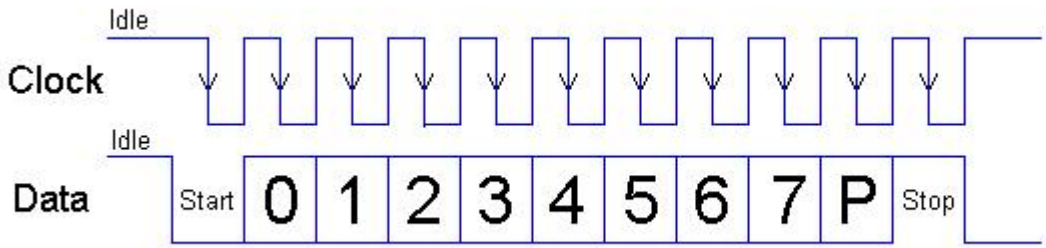
# Goals

- Learn how to use the FPGA to accept input from a PS/2 keyboard
- On completion, you will know how to:
  - Create a Verilog/VHDL module for an interface to a PS/2 keyboard
  - Display numbers on the LEDs when the corresponding key is pressed on the keyboard

# PS/2 Timing Diagram




PS/2 keyboard's connector


1. KBD Clock
2. GND
3. KBD Data
4. N/C
5. +5V (VCC)
6. N/C

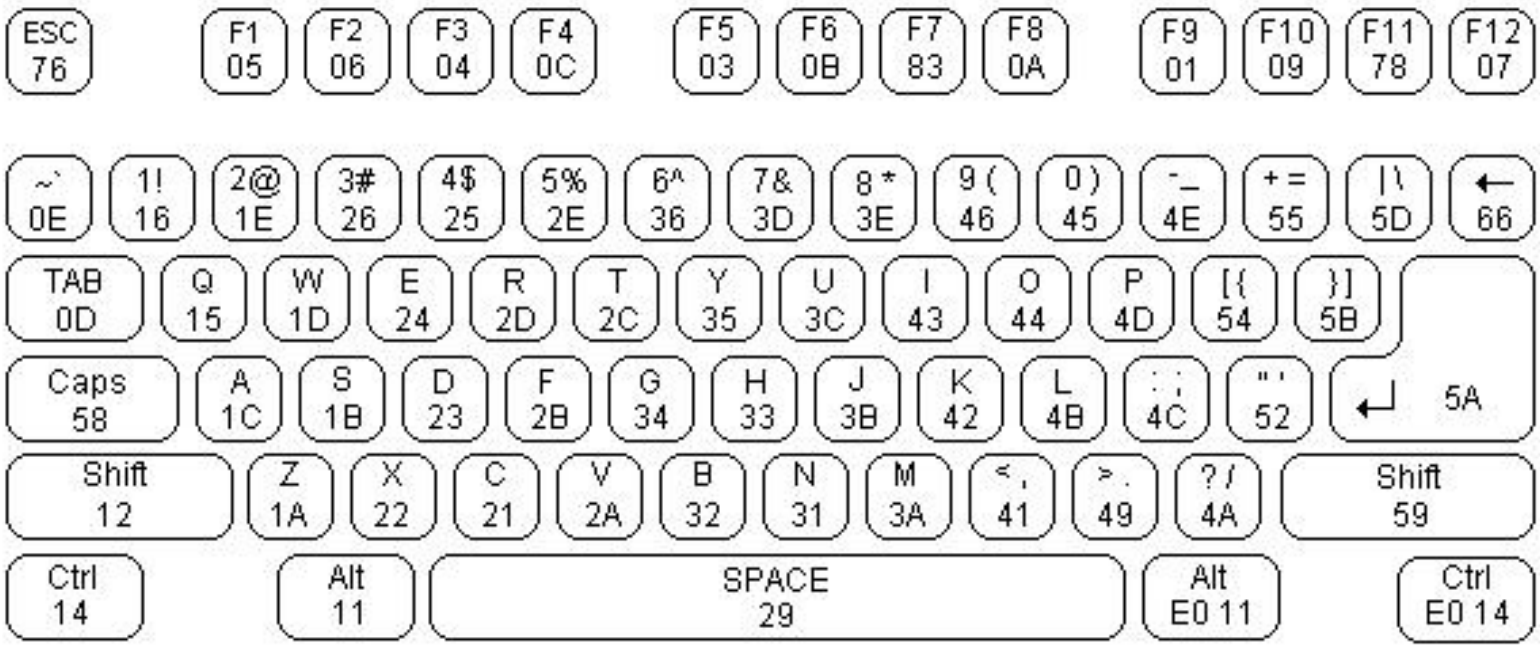
The signal from the Keyboard to the Host is shown above. Note the Start and Stop bits at the beginning and end and the Parity bit P (odd parity) just before the Stop bit.

Also note that when the Keyboard Clock signal is held low by the HOST, the keyboard buffers input, but holds it temporarily.

Please see the website referenced below for the diagram for the signals sent by the host.

Figure from: http://www.beyondlogic.org/keyboard/keybrd.htm

# Keyboard Scan Codes




The above figure shows the scan codes sent by the Keyboard. You will have to read in these codes and convert the code to a format suitable for displaying on the LEDs

Figure from: http://www.beyondlogic.org/keyboard/keybrd.htm