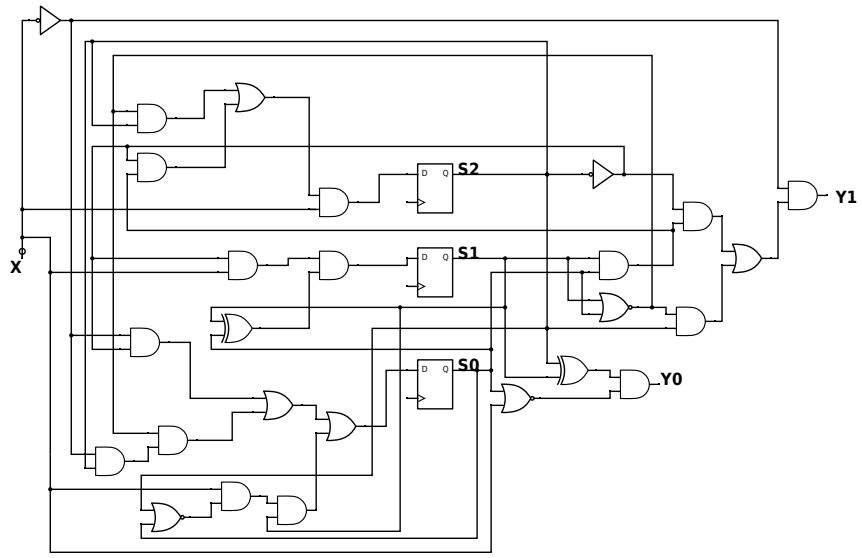
0.1 Experiment 4 (Analysis of a Sequential Circuit)

0.1.1 Aim

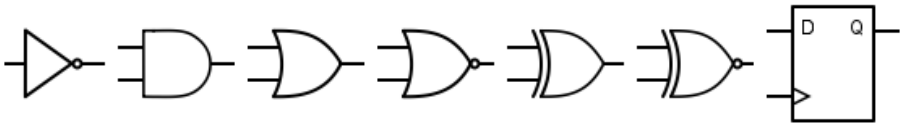
In this experiment, your knowledge to analyze a sequential circuit which is explained in section 3.4 of the course book will be tested.

0.1.2 Problems:

Let there be an input X, a 2-bit output Y_1Y_0 and a sequential circuit connecting these two as shown below.



- Initially, all state register values are zero ($S_2 = 0, S_1 = 0, S_0 = 0$).
- The reset should be synchronous to the falling edge of the clock.



Note: Components given above are inverter, and, or, nor, xor, xnor and state register, respectively.

0.1.3 Preliminary Work

Before the experiment, you should prepare the following materials:

1. State the inputs and outputs of the state registers.

2. State the inputs and outputs of the combinational block of the sequential circuit.
3. Write each output (including next state bits) as a function of the inputs.
4. Draw the truth table for the combinational circuit (Hint: use the functions in the previous step).
5. Draw the finite state machine by using the table obtained in previous step.
6. How many unreachable states does the finite state machine contain? (No explanation, only short answer)
7. Briefly explain the relation between the input and the output. (Hint: which patterns in the input results in different outputs)
8. Write the **behavioral level** verilog code for the corresponding finite state machine.
9. Write the verilog code for the testbench waveform in order to test different input combinations. (keep the initial state as State 0, i.e. $S_2S_1S_0 = 000$)

Then, submit your preliminary work.