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Experiment 4 (Analysis of a Sequential Circuit)

Preliminary Work:

Step 1: State the inputs and outputs of the state registers.

Inputs: N_2 , N_1 , N_0

Outputs: S_2 , S_1 , S_0

Step 2: State the inputs and outputs of the combinational block.

Inputs: X

Outputs: Y_1 , Y_0

Step 3: Write each output (including next state bits) as a function of the inputs.

$N_2 = S_2S_1'S_0'X + S_2'S_1S_0X$
$N_1 = S_2'S_1'S_0X + S_2'S_1S_0'X$
$N_0 = S_2'X' + S_2S_1'S_0'X' + S_2'S_1S_0'X$
$Y_1 = S_2'S_1S_0X' + S_2S_1'S_0'X'$
$Y_0 = S_2'S_1S_0'X' + S_2S_1'S_0'X'$

Step 4: Draw the truth table for the combinational circuit.

#	S2	S1	S0	X	N2	N1	N0	Y1	Y0
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	0	0
2	0	0	1	0	0	0	1	0	0
3	0	0	1	1	0	1	0	0	0
4	0	1	0	0	0	0	1	0	1
5	0	1	0	1	0	1	1	0	0
6	0	1	1	0	0	0	1	1	0
7	0	1	1	1	1	0	0	0	0
8	1	0	0	0	0	0	1	1	1
9	1	0	0	1	1	0	0	0	0
10	1	0	1	0	0	0	0	0	0
11	1	0	1	1	0	0	0	0	0
12	1	1	0	0	0	0	0	0	0
13	1	1	0	1	0	0	0	0	0
14	1	1	1	0	0	0	0	0	0
15	1	1	1	1	0	0	0	0	0

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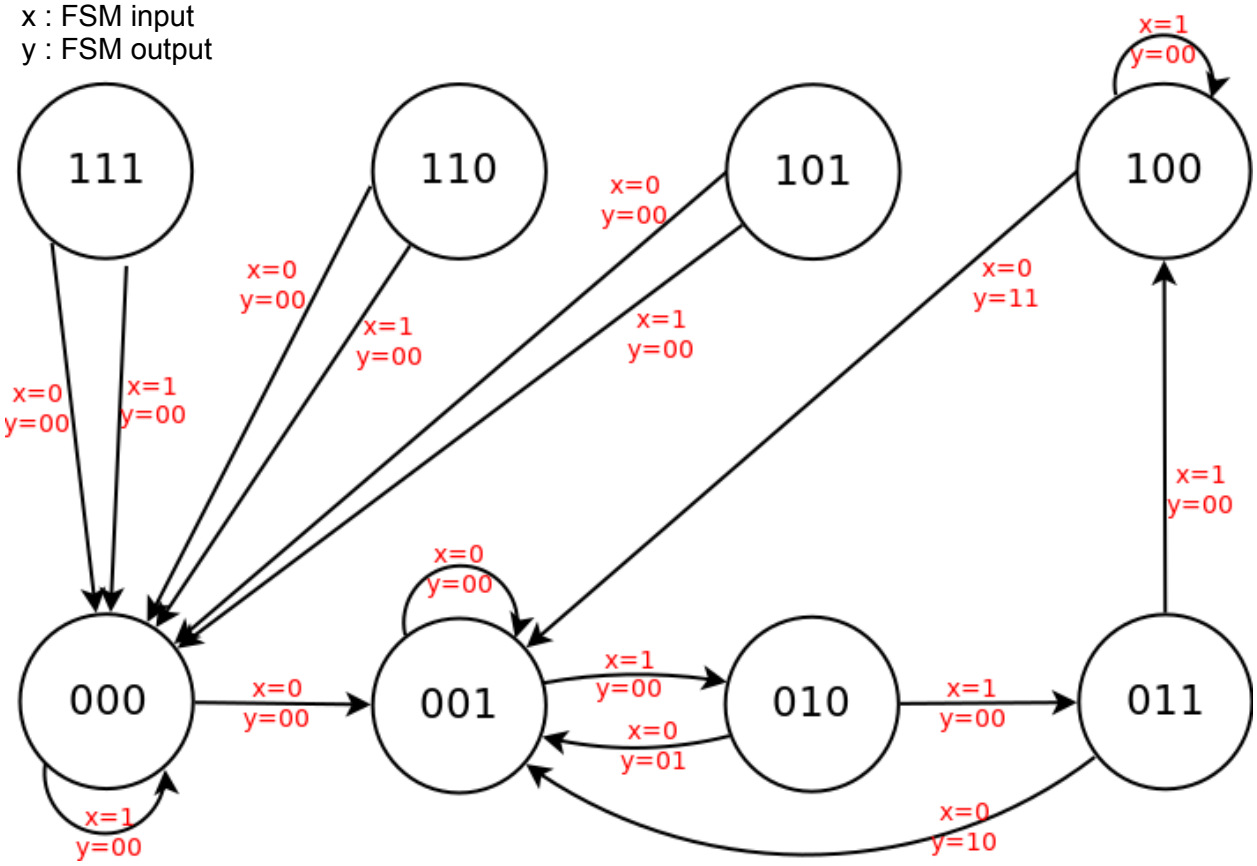
Step 5: Draw the finite state machine by using the truth table.

x : FSM input
y : FSM output



NOTE: There is a reset which is not shown in the FSM above. Whenever reset is HIGH, the state becomes initial state which is 000.(Reset is synchronous to the falling edge of the clock.)

Step 6: How many unreachable states does the finite state machine contain? (No explanation, only short answer)

# of Unreachable States: 3

Step 7: Briefly explain the relation between the input and the output.

Explanation: The output detects input patterns such as 010 , 0110 , 01110 , 01...10. When there is one 1 between 0s, it gives 01. When there are two 1s between 0s, it gives 10. When there are 3 or more 1s between 0s, it gives 11. For the other patterns, it gives 00. Also, it ignores the initial 1s of sequence.