Transistor circuits basics

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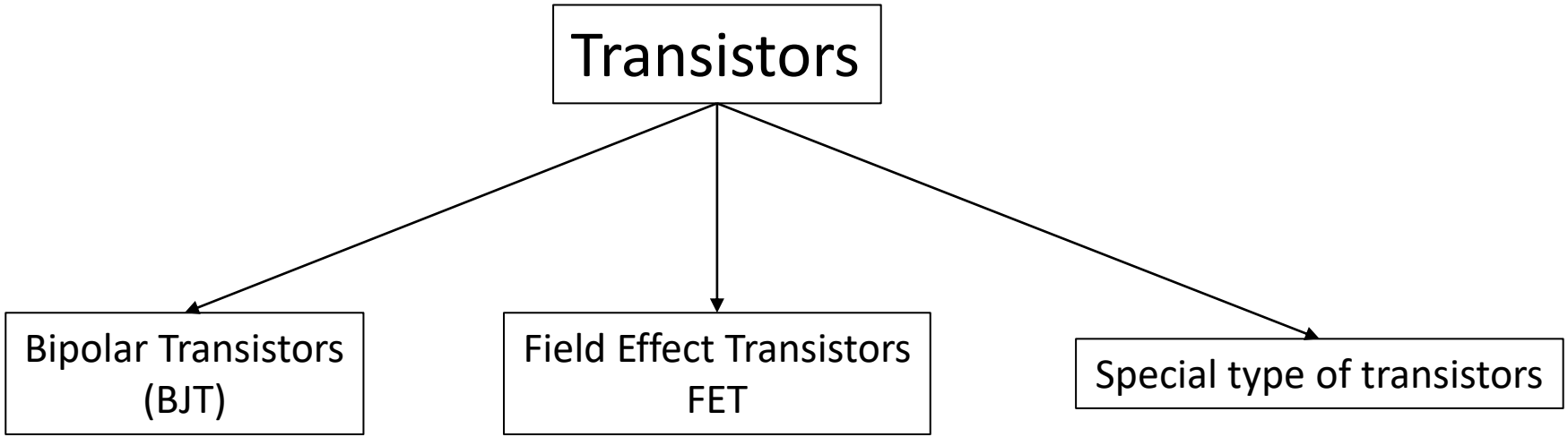
What is a transistor?

A ***transistor*** is a semiconductor device used to amplify or switch electronic signals and electrical power (WikipediA).

The ***transistor*** is the most important example of an “active” component!

Transistors are used in almost every electric circuit you can imagine. For example, you find transistors in switching circuits, amplifier circuits, oscillator circuits, current source circuits, voltage- regulator circuits, power- supply circuits, digital logic ICs, and almost any circuit that uses small control signals to control larger currents.

Classification of transistors



ITMO

Field Effect Transistors

Field-effect transistor

A **field-effect transistor** is a semiconductor device in which the amount of current flowing through a conductive channel is controlled by the field generated by the voltage at the control electrode.

Martin "John" M. Atalla

Dawon Kahng
강대원

Born	May 4, 1931[1] Keijō, Chōsen
Died	May 13, 1992 (aged 61)[2] New Brunswick, New Jersey, U.S.
Citizenship	South Korean (renounced) United States
Occupation	Electrical engineer
Known for	MOSFET (MOS transistor) PMOS and NMOS Schottky diode Nanolayer-base transistor Floating-gate MOSFET Floating-gate memory Reprogrammable ROM

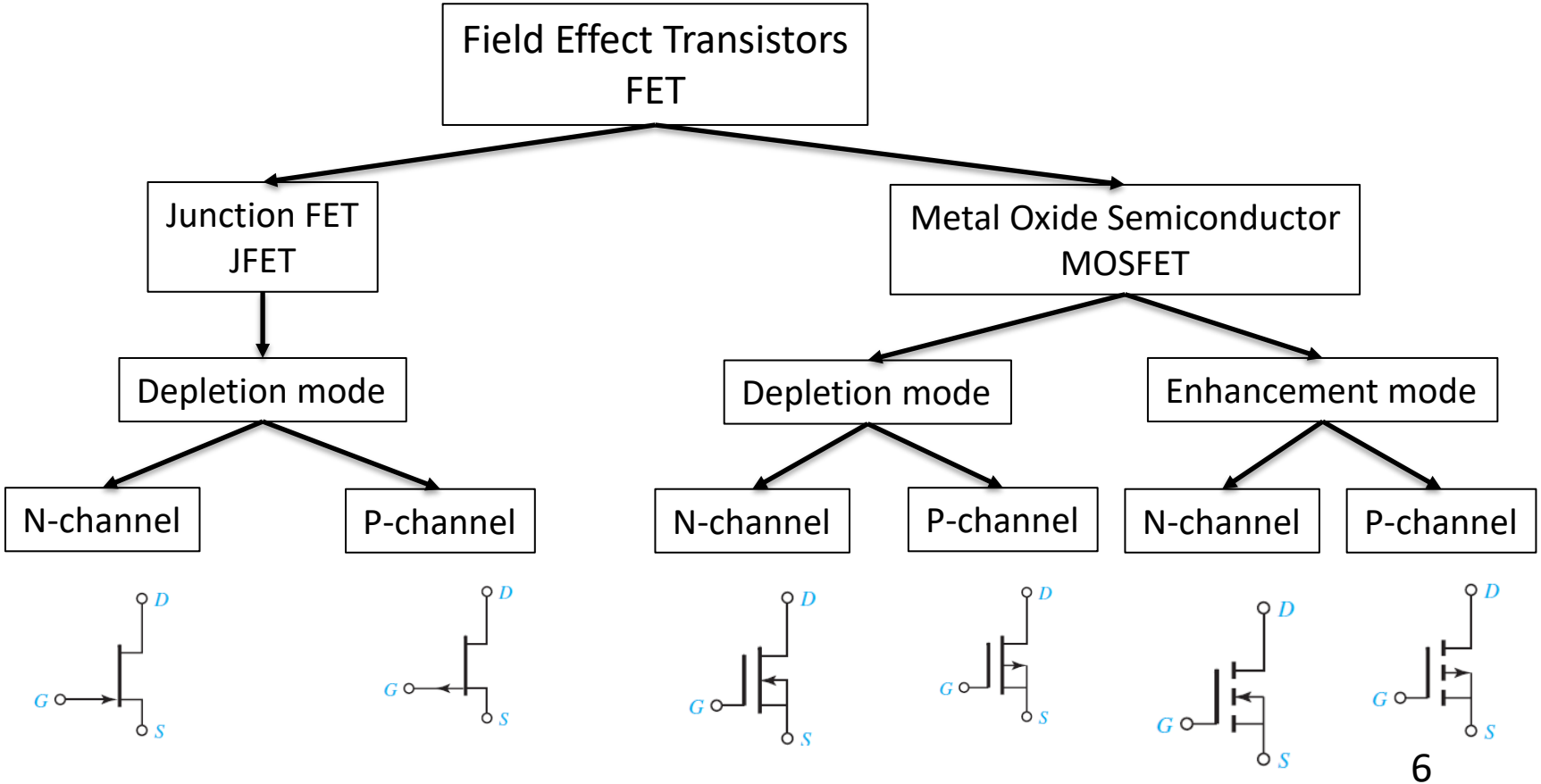
Оскар Хайль

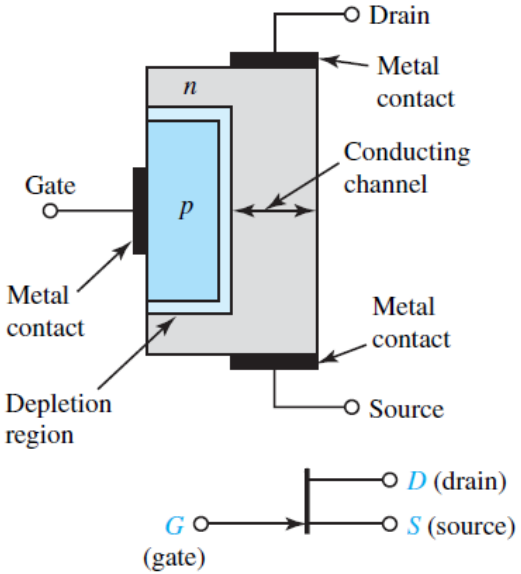
Дата рождения	20 марта 1908
Место рождения	Лангвиден, Кайзерслаутерн, Рейнланд-Пфальц
Дата смерти	15 мая 1994 (86 лет)
Место смерти	Сан-Матео, Сан-Матео, Калифорния, США
Страна	Германия
Альма-матер	Гёттингенский университет

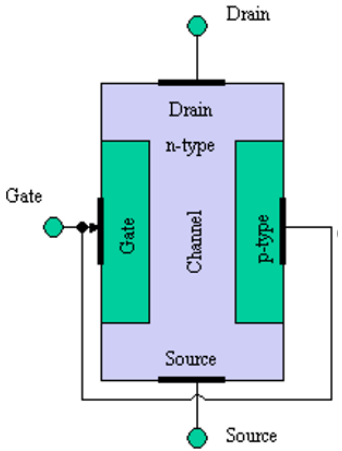
J. E. Lilienfeld

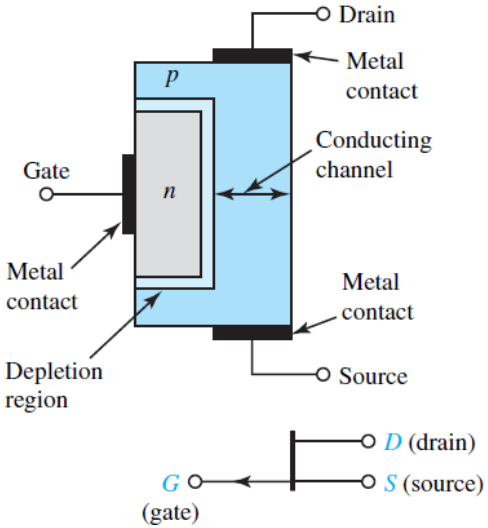
Born	April 18, 1882 Lemberg, Galicia, Austro-Hungarian Empire
Died	August 28, 1963 (aged 81) Charlotte Amalie, Virgin Islands, U.S.
Citizenship	Austro-Hungarian (1882 – September 1919) Polish (1919–1934) American (1934–1963)
Alma mater	Friedrich-Wilhelms-Universität
Known for	Field-effect transistor Electrolytic capacitor
Scientific career	
Fields	Physicist Electrical engineer
Institutions	Leipzig University Amrad, Inc Ergon Research Laboratories
Doctoral advisor	Max Planck Emil Warburg
Other academic advisors	Jacobus Henricus van 't Hoff

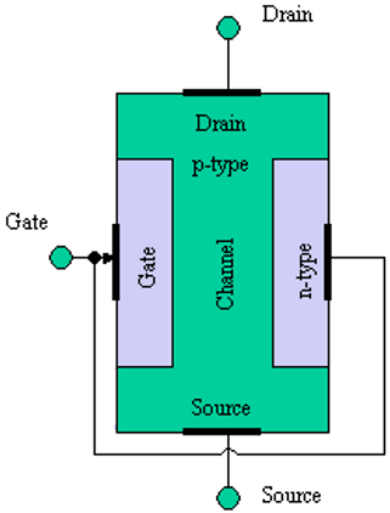
Classification of transistors



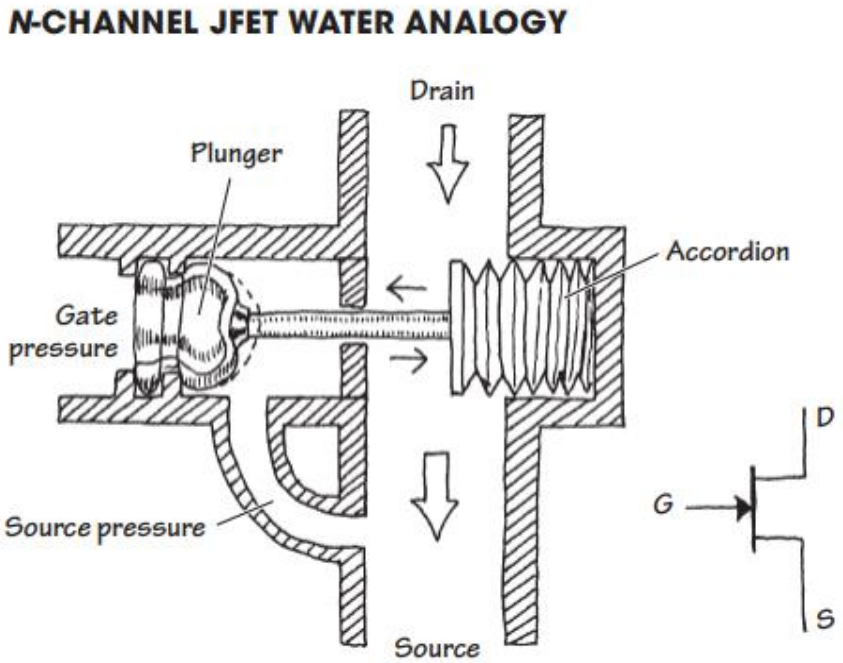

Drain
Metal contact
n
Conducting channel
Gate
p
Metal contact
Metal contact
Depletion region
Source
D (drain)
G (gate)
S (source)

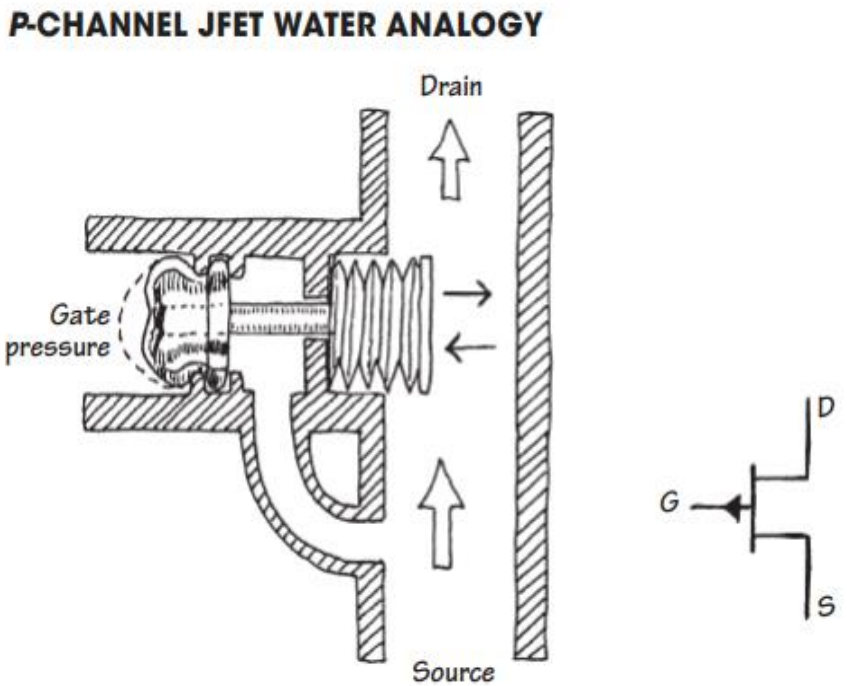

Drain
Drain
n-type
Gate
Gate
Channel
p-type
Source
Source


Drain
Metal contact
p
Conducting channel
Gate
n
Metal contact
Metal contact
Depletion region
Source
D (drain)
G (gate)
S (source)

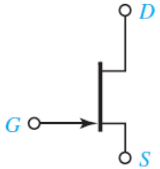

Drain
Drain
p-type
Gate
Gate
Channel
n-type
Source
Source

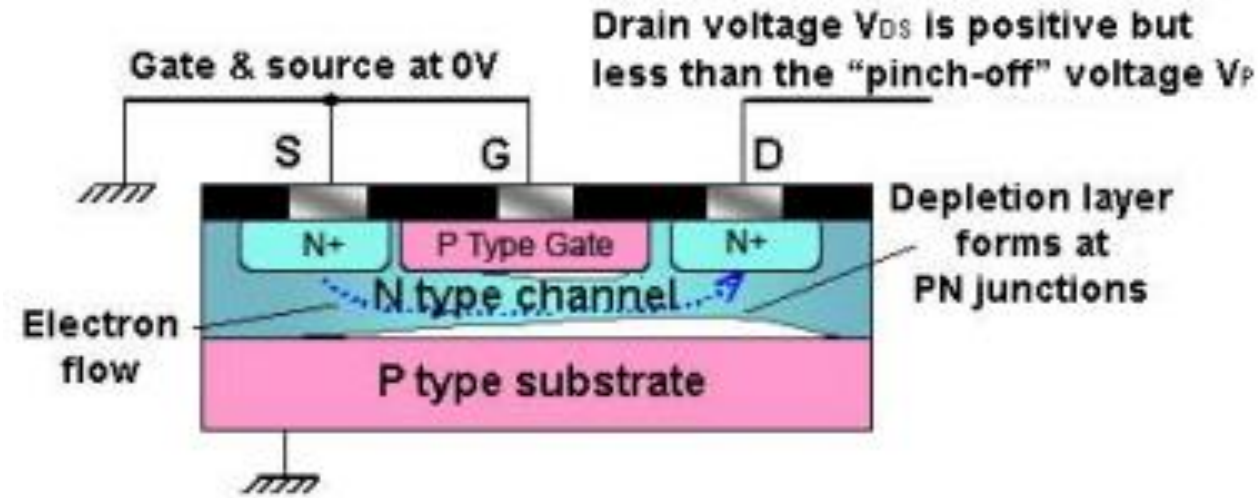
Water analogs of the JFET



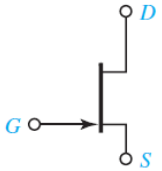


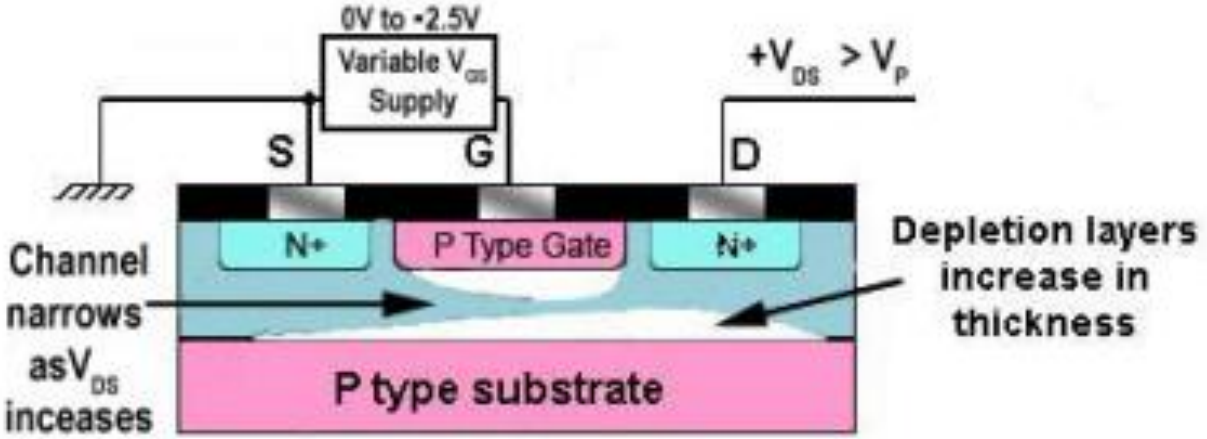
JFETs operation

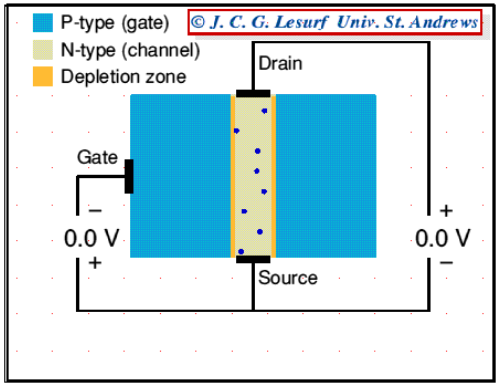




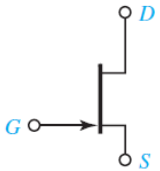
JFETs operation



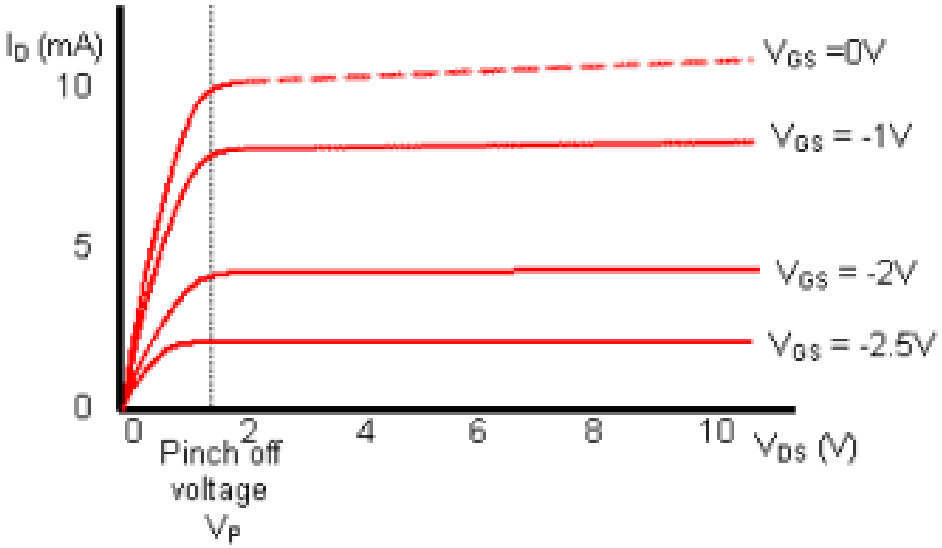




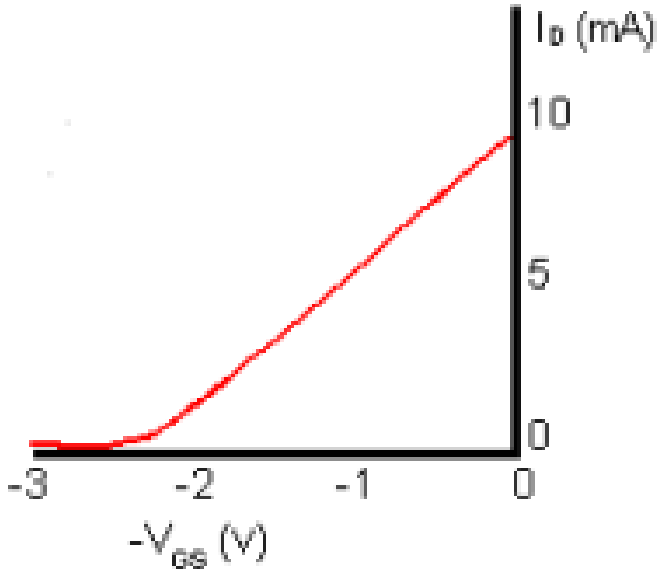
JFET Characteristics



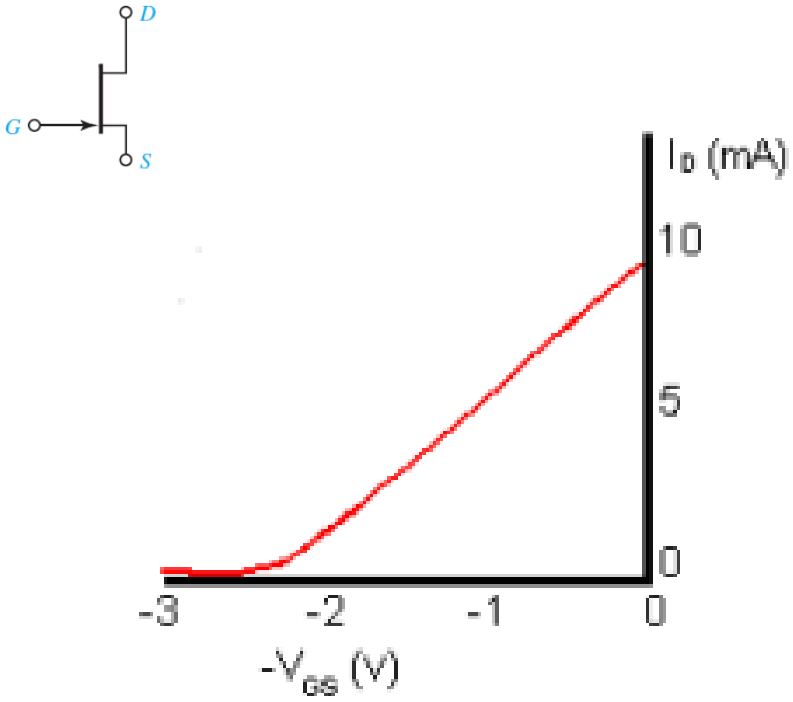
Output Characteristics

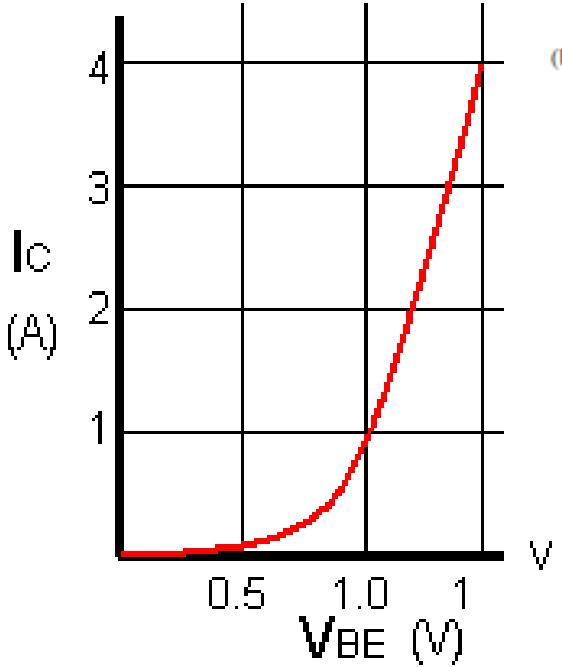


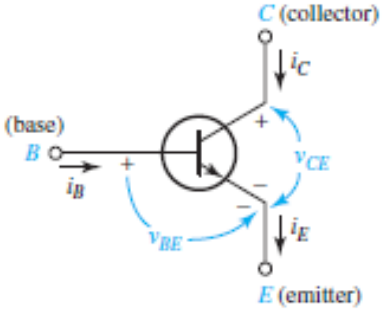
Transconductance characteristic



Transconductance characteristic





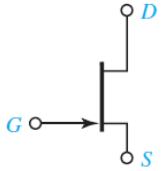


Characteristics of JFET

Output Characteristics or "drain" characteristic of a JFET

ohmic region:

$$I_D = K(2(U_{GS} - U_P)U_{DS} - {U_{DS}}^2) \qquad K = \frac{I_{DSS}}{{U_P}^2}$$



saturation area:

$$U_{DS} \geq U_{GS} - U_P \quad I_D = K(2(U_{GS} - U_P)U_{DS} - {U_{DS}}^2)$$

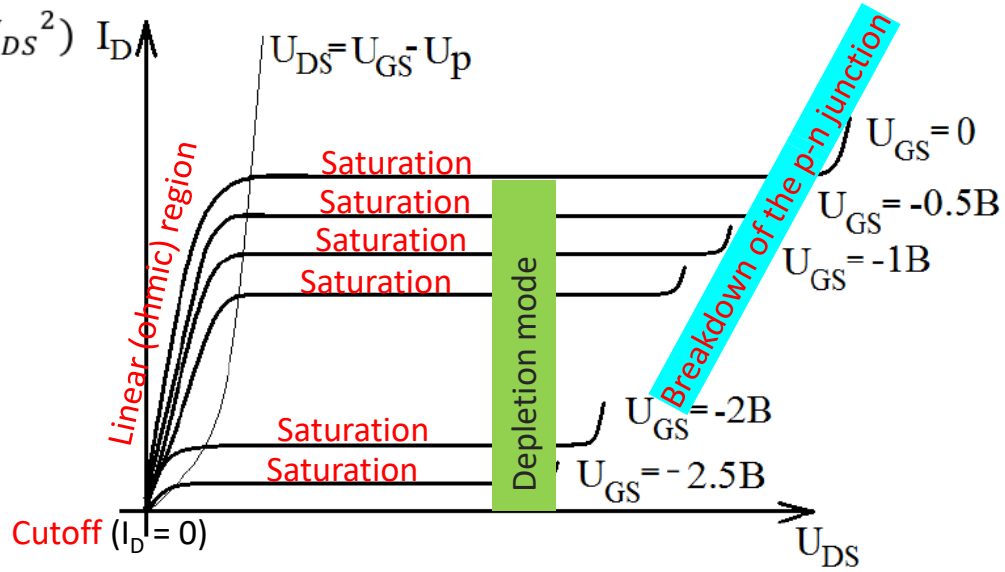
$$U_{DS} = U_{GS} - U_P \quad I_D = K(U_{GS} - U_P)^2$$

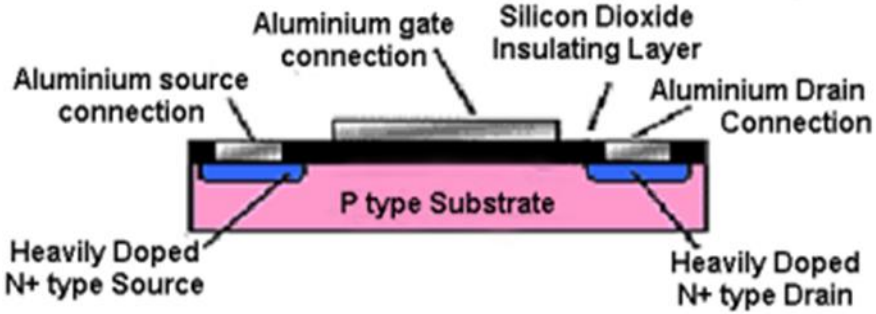
cutoff area:

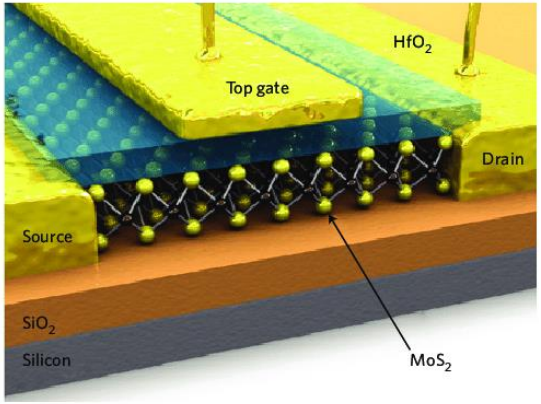
$$U_{GS} = U_{DS} + U_P \qquad I_D = K{U_{DS}}^2$$

$$U_{GS} < U_P \qquad I_D \approx 0$$

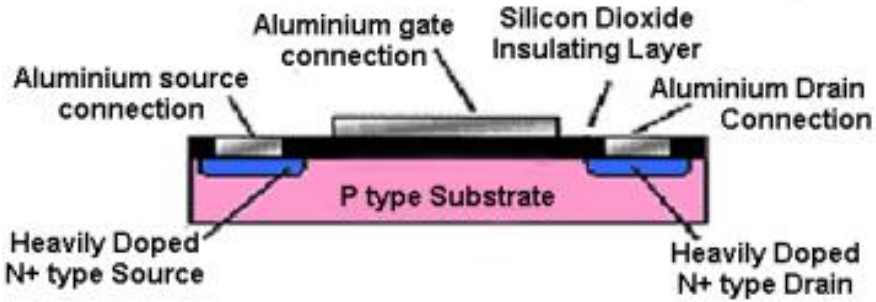
$$g_f = \frac{\Delta I_D}{\Delta U_{GS}}$$

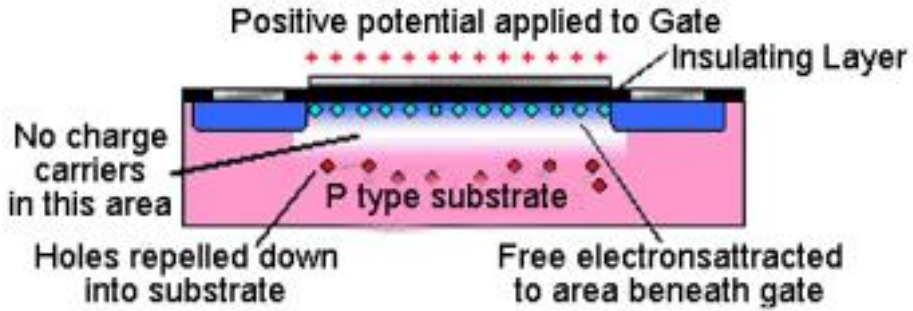


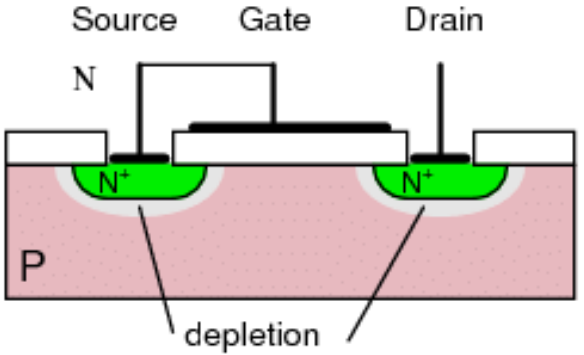


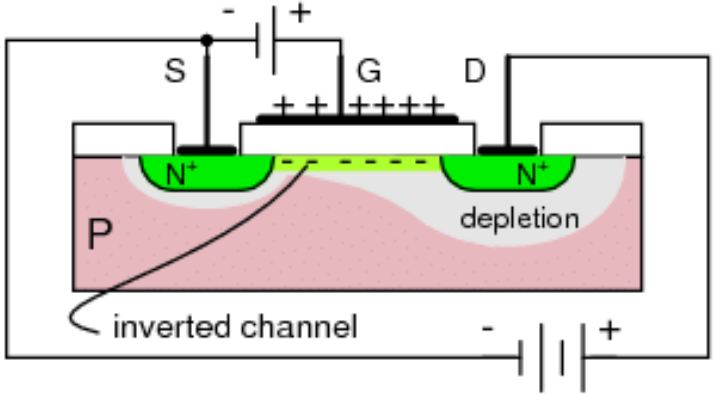


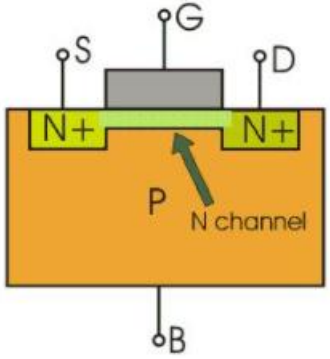
Schematic illustration of HfO 2-top-gated monolayer MoS 2 FET device. Optical image of a CMOS device. The device consists of one FET and defined by three gold leads that serve as gate, source and drain contacts.

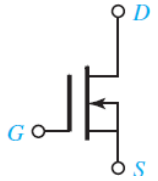

Aluminium gate connection
Silicon Dioxide Insulating Layer
Aluminium source connection
Aluminium Drain Connection
P type Substrate
Heavily Doped N+ type Source
Heavily Doped N+ type Drain

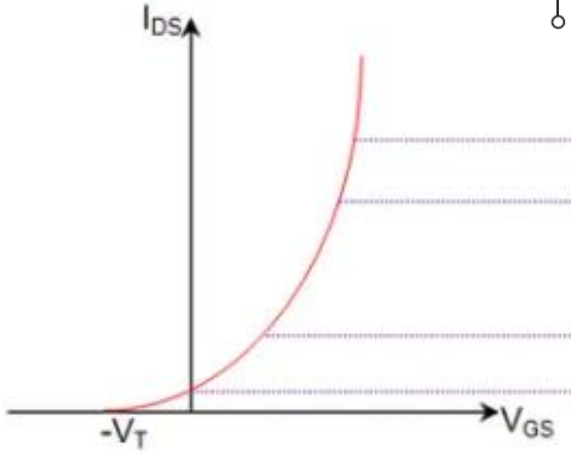

Positive potential applied to Gate
Insulating Layer
No charge carriers in this area
P type substrate
Holes repelled down into substrate
Free electronsattracted to area beneath gate

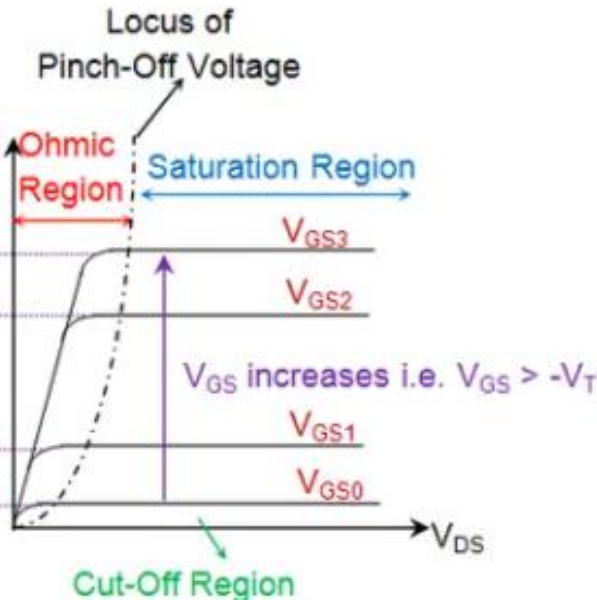

Source
Gate
Drain
N
N+
N+
P
depletion

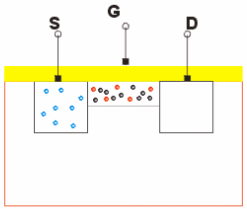

-
+
S
G
D
N+
N+
P
depletion
inverted channel
-
+

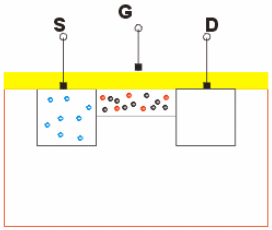

G
S
D
N+
N+
P
N channel
B

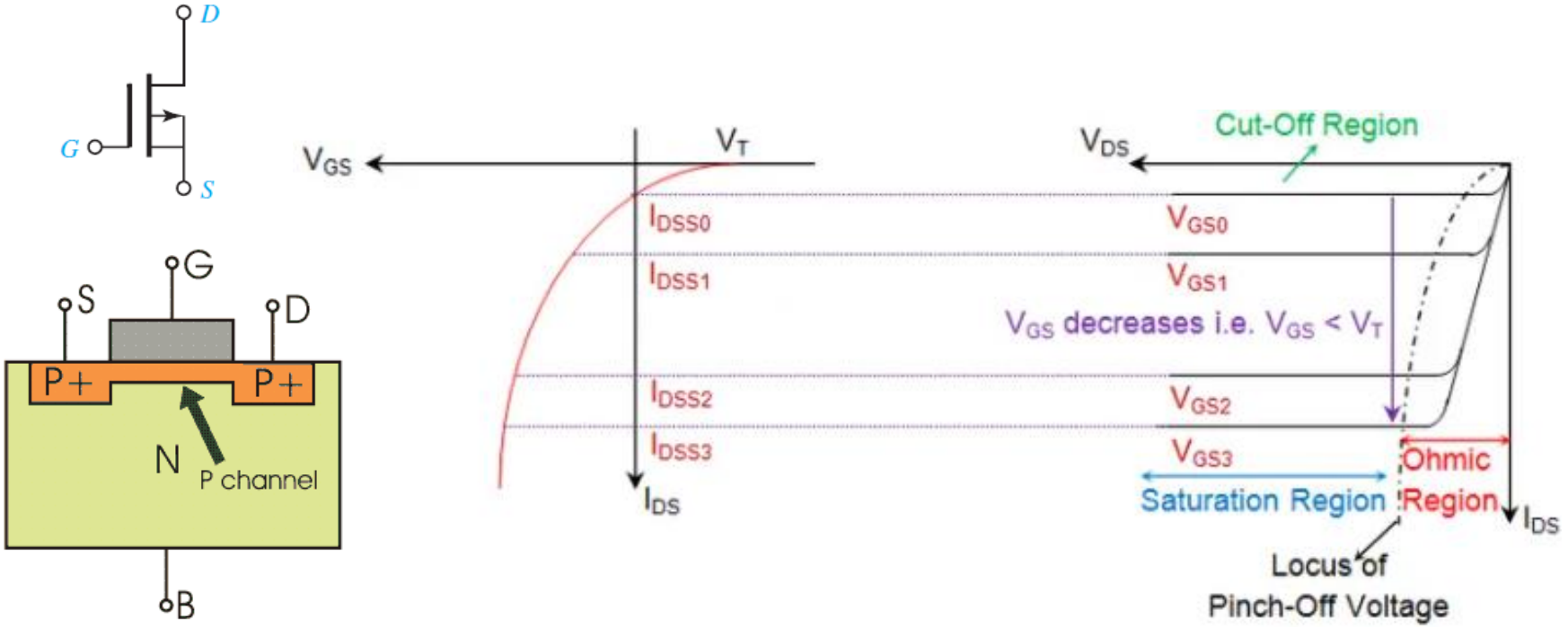

D
G
S


I_{DS}
$-V_T$
V_{GS}

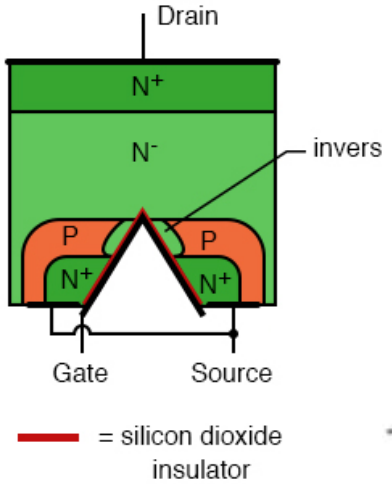

Locus of
Pinch-Off Voltage
I_{DS}
Ohmic
Region
Saturation Region
I_{DSS3}
V_{GS3}
I_{DSS2}
V_{GS2}
V_{GS} increases i.e. $V_{GS} > -V_T$
I_{DSS1}
V_{GS1}
I_{DSS0}
V_{GS0}
V_{DS}
Cut-Off Region


S
G
D

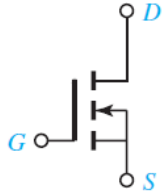

S
G
D

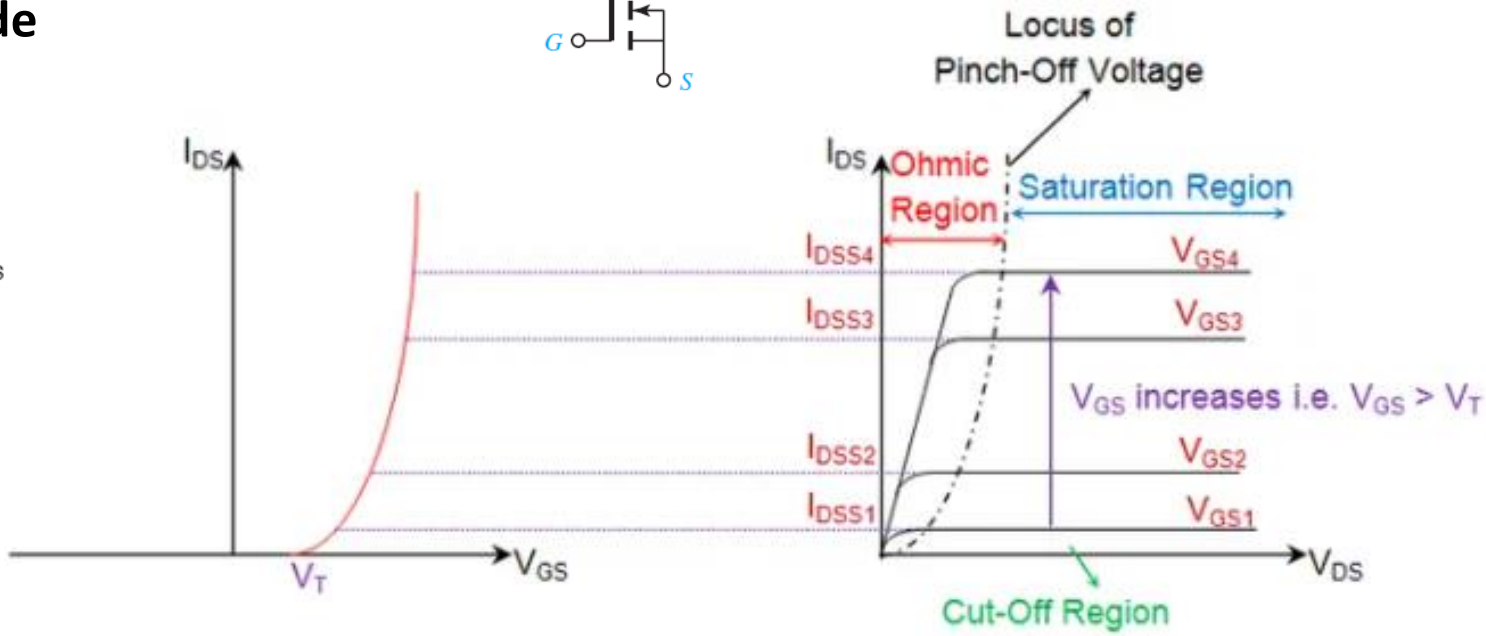

D
G
S
G
S
D
P+
P+
N
P channel
B
VGS
VT
IDSS0
IDSS1
IDSS2
IDSS3
IDS
VDS
Cut-Off Region
VGS0
VGS1
VGS decreases i.e. VGS < VT
VGS2
VGS3
Saturation Region
Ohmic Region
IDS
Locus of
Pinch-Off Voltage

Enhancement mode

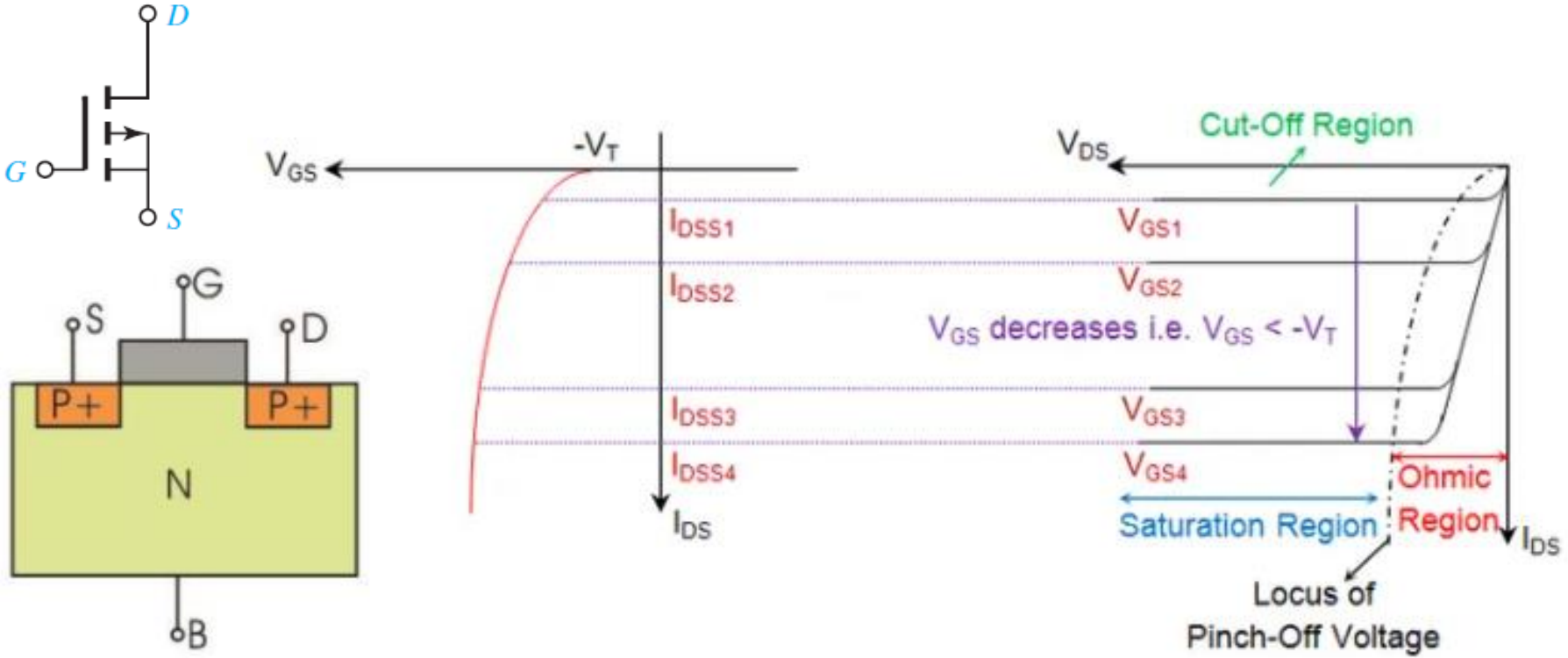


V-MOSFET





p-channel Enhancement-type MOSFET

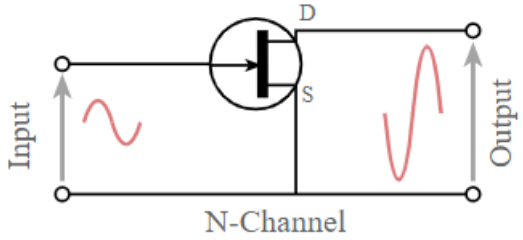


Region of MOSFET Operation

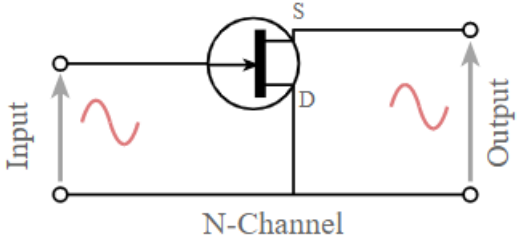
Kind of MOSFET	Region of Operation		
	Cut-Off	Ohmic/Linear	Saturation
n-channel Enhancement-type	$V_{GS} < V_T$	$V_{GS} > V_T$ and $V_{DS} < V_P$	$V_{GS} > V_T$ and $V_{DS} > V_P$
p-channel Enhancement-type	$V_{GS} > -V_T$	$V_{GS} < -V_T$ and $V_{DS} > -V_P$	$V_{GS} < -V_T$ and $V_{DS} < -V_P$
n-channel Depletion-type	$V_{GS} < -V_T$	$V_{GS} > -V_T$ and $V_{DS} < V_P$	$V_{GS} > -V_T$ and $V_{DS} > V_P$
p-channel Depletion-type	$V_{GS} > V_T$	$V_{GS} < V_T$ and $V_{DS} > -V_P$	$V_{GS} < V_T$ and $V_{DS} < -V_P$

FET configuration basics

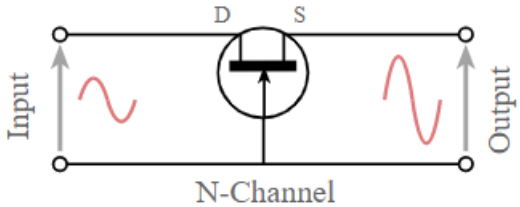
Common source



Common drain:

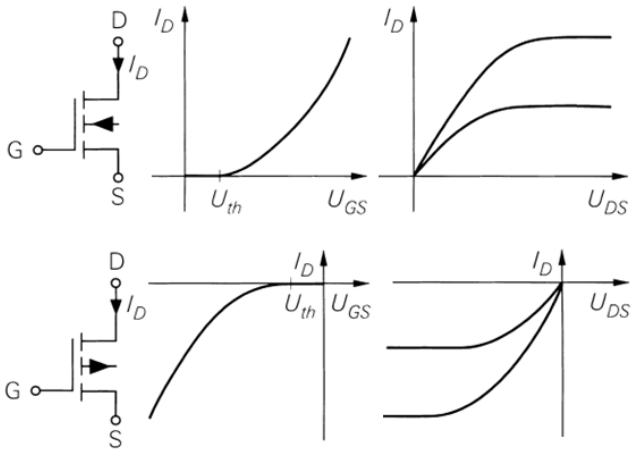


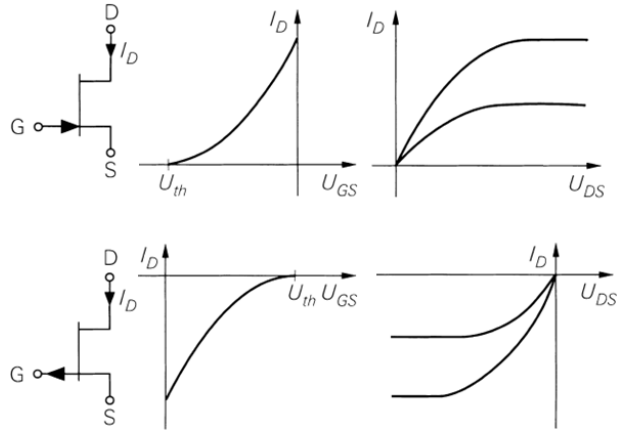
Common gate

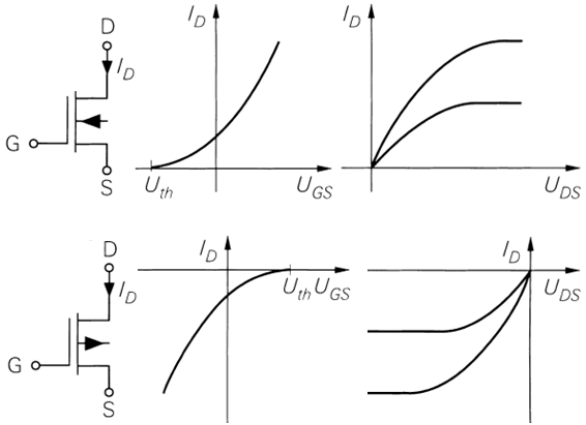


FET CONFIGURATION	COMMON GATE	COMMON DRAIN (SOURCE FOLLOWER)	COMMON SOURCE
Voltage gain	High	Low	Medium
Current gain	Low	High	Medium
Power gain	Low	Medium	High
Input resistance	Low	High	Medium
Output resistance	High	Low	Medium
Input / output phase relationship	0°	0°	180°

Comparison FET



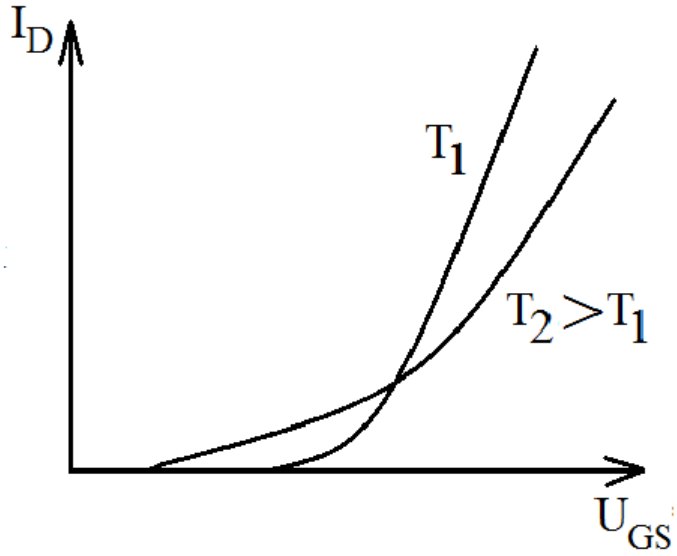




Comparison FET

Type FET	n-channel	p-channel
Enhancement-type MOSFET	$U_{th} > 0$ $U_{GS} > U_{th}$ $U_{DS} > 0$ $I_D > 0$	$U_{th} < 0$ $U_{GS} < U_{th}$ $U_{DS} < 0$ $I_D < 0$
Depletion-type MOSFET	$U_{th} < 0$ $U_{GS} > U_{th}$ $U_{DS} > 0$ $I_D > 0$	$U_{th} > 0$ $U_{GS} < U_{th}$ $U_{DS} < 0$ $I_D < 0$
JFET	$U_{th} < 0$ $U_{th} < U_{GS} < 0$ $U_{DS} > 0$ $I_D > 0$	$U_{th} > 0$ $0 < U_{GS} < U_{th}$ $U_{DS} < 0$ $I_D < 0$

FET Temperature dependence



When the temperature rises

- the drain current is proportional to the mobility of free main charge carriers
- the mobility of free majority charge carriers decreases

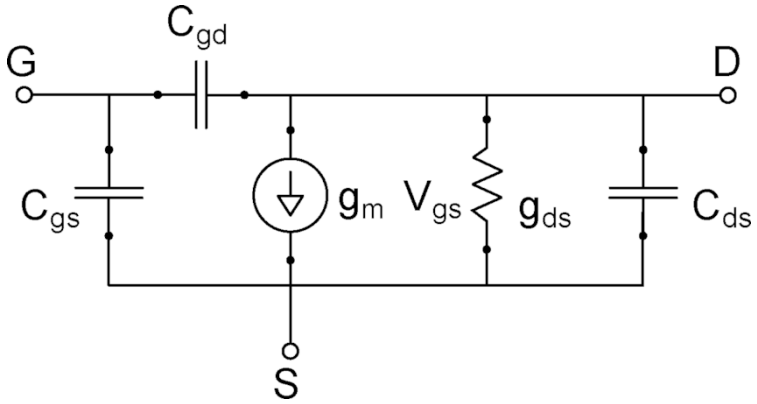
→ there is a decrease in drain current with increasing temperature

- the band gap in semiconductors decreases
- the height of the potential barrier decreases
- the width of the p-n junction decreases
- the depth of penetration of the depleted growth into the conducting channel decreases

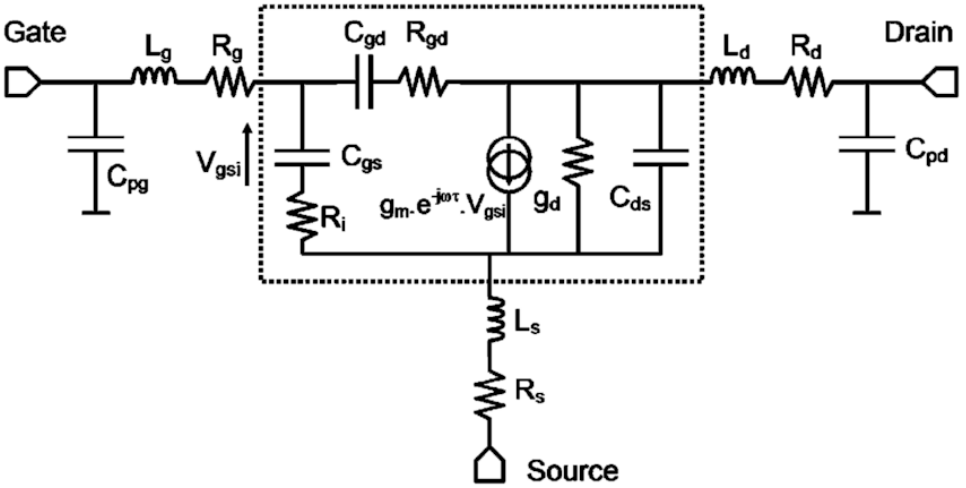
→ for field-effect transistors with a control p-n-junction channel current increases

Equivalent circuit of the MOSFET

Small-signal models



Large-signal models



$$I_G = 0$$

$$I_D = \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2\left(1 + \lambda V_{DS}\right)$$

Transconductance:

$$g_m = \frac{2I_D}{V_{GS} - V_{TN}} = \sqrt{2K_n I_D}$$

Output resistance:

$$r_o = \frac{1}{g_o} = \frac{1 + \lambda V_{DS}}{\lambda I_D} \cong \frac{1}{\lambda I_D}$$

Main characteristic equivalent circuit

Transconductance:

$$g_m = \frac{\Delta I_D}{\Delta V_{DS}} = \frac{1}{R_{DS}}$$

It is the ratio of change in drain current to the change in gate source voltage at constant drain source voltage.

Output resistance:

$$r_o = \frac{1}{g_o} = \frac{1+\lambda V_{DS}}{\lambda I_D} \cong \frac{1}{\lambda I_D}$$

It is the ratio of change in AC drain source voltage to the change in AC drain current at constant gate source voltage

I_D - drain current, A

U_{GS} - voltage gate-source, V

U_{DS} - voltage drain-sources, V

R_{DS} - channel resistance, Ohm

U_P - cut-off voltage (ID = 0), V

I_{DSS} - initial saturation current, A

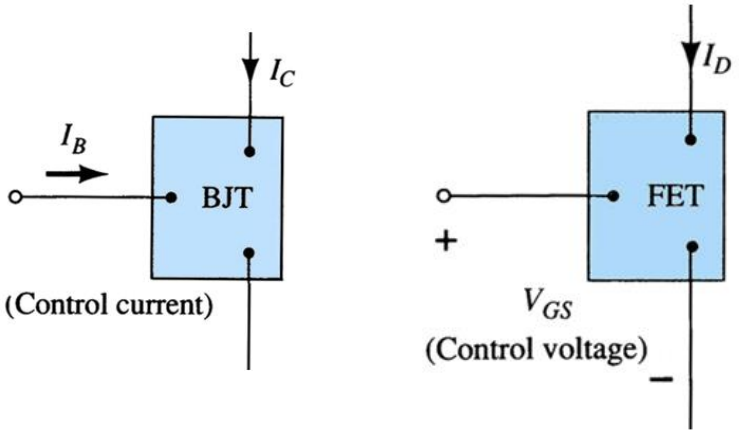
$1/\lambda$ - Early Voltage for FET, V

$$K = \frac{I_{DSS}}{U_P{}^2}$$

Comparison BJT and FET

Current-controlled amplifiers

Voltage-controlled amplifiers



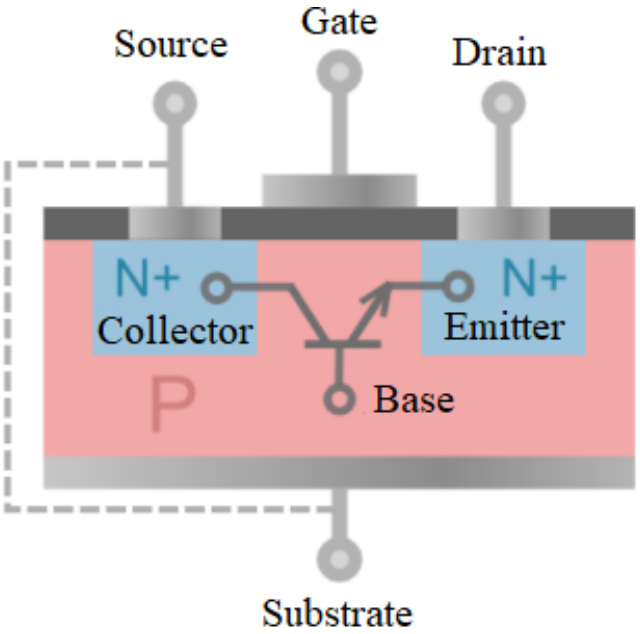
Advantages of FET

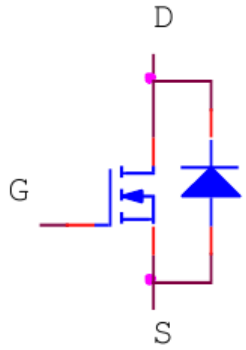
High input impedance (MΩ)
Temperature stable than BJT
Smaller than BJT
Can be fabricated with fewer processing
BJT is bipolar – conduction both hole and electron
FET is unipolar – uses only one type of current carrier
Less noise compare to BJT
Usually use as logic switch

Disadvantages of FET

Easy to damage compare to BJT

Parasitic bipolar transistor in the MOSFET





In the manufacture of powerful MOS transistors, a "parasitic" bipolar transistor appears in their structure. In order to neutralize its influence, the substrate is short-circuited with the source. This is equivalent to shorting the base and emitter of the parasitic transistor. As a result, the voltage between the base and the emitter of the bipolar transistor will never reach the required voltage for it to open (about 0.6V is required for the PN junction inside the device to begin to conduct).

The main parameters of FET

I_{dmax} is the maximum drain current at which there is no thermal breakdown of the transistor structure;

U_{DSOmax} - maximum drain - source voltage, at which no breakdown of the transistor structure occurs (measured at UGS = 0);

U_{GSmax} - maximum gate - source voltage, at which no breakdown of the insulating layer between the gate and the channel occurs;

I_{Smax} - maximum reverse diode current;

P_{dmax} - maximum power dissipation;

I_{DSSmax} - drain leakage current in cutoff mode;

I_{GSSF} - gate current forward;

I_{GSSB} - gate reverse current;

U_{GST} - gate-source threshold voltage;

g_f is the slope of the transfer characteristic;

R_{ONmim} - minimum drain-to-source resistance in the ohmic region;

C_{GS} - gate - source capacitance;

C_{GD} - capacitance gate - drain;

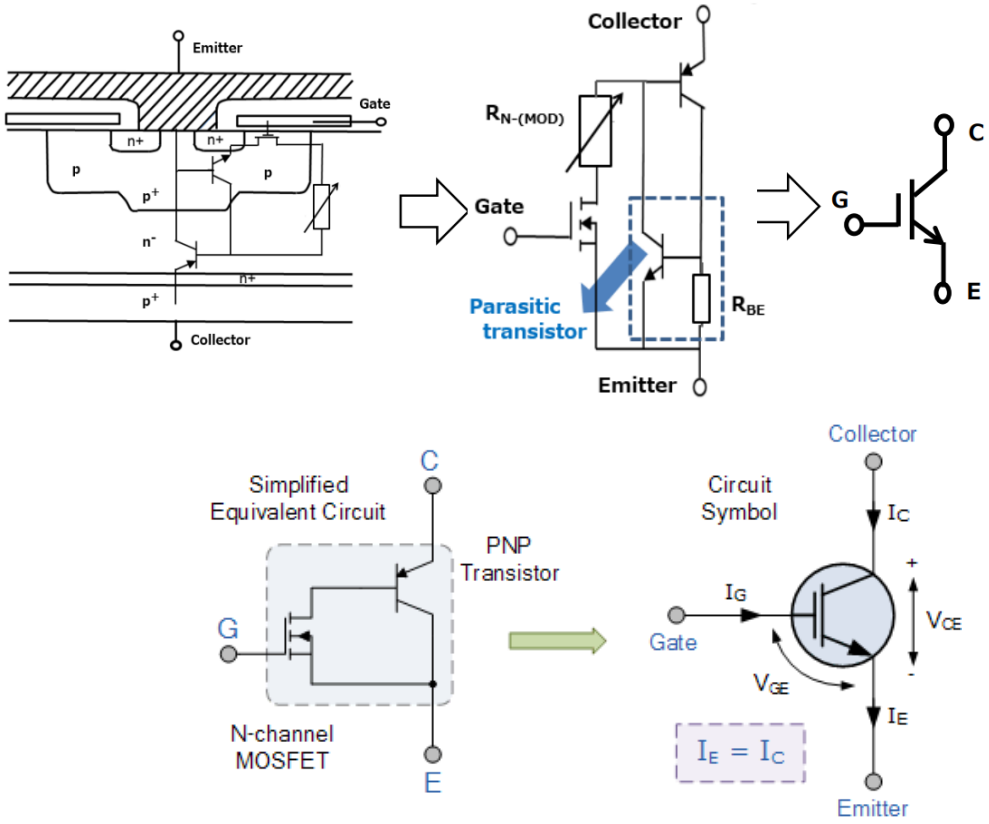
Q_{GS} - charge of the gate - source capacitance;

Q_{GD} - charge capacitance gate - drain;

t_r is the transistor unlocking time;

t_f - transistor turn-off time.

IGBT- Insulated Gate Bipolar transistor



IGBT combines the advantages of two main types of transistors:

from MOSFET:

- ✓ high input impedance
- ✓ low control power
- ✓ voltage control

from bipolar transistors:

- ✓ low on-state residual voltages
- ✓ witching characteristics and conductivity
- ✓ low losses in the open state at high currents and high voltages;

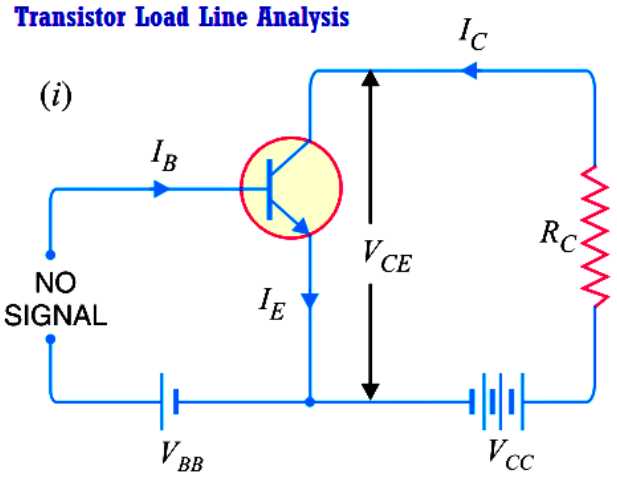
IGBT comparison table

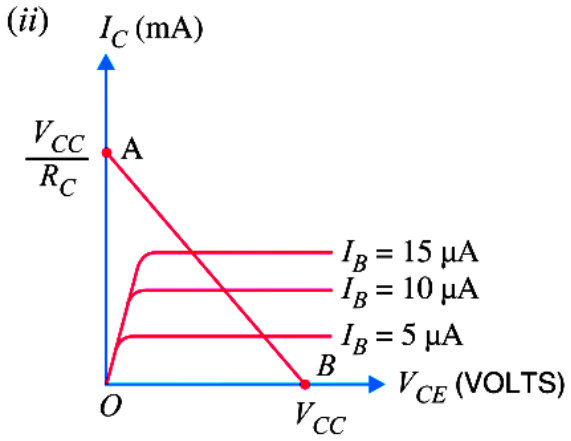
Device characteristic	Power bipolar	Power MOSFET	IGBT
Voltage rating	High <1 kV	High <1 kV	Very high >1 kV
Current rating	High <500 A	High >500 A	High >500 A
Input drive	Current ratio h_{FE} ~ 20–200	Voltage V_{GS} ~ 3–10 V	Voltage V_{GE} ~ 4–8 V
Input impedance	Low	High	High
Output impedance	Low	Medium	Low
Switching speed	Slow (µs)	Fast (ns)	Medium
Cost	Low	Medium	High

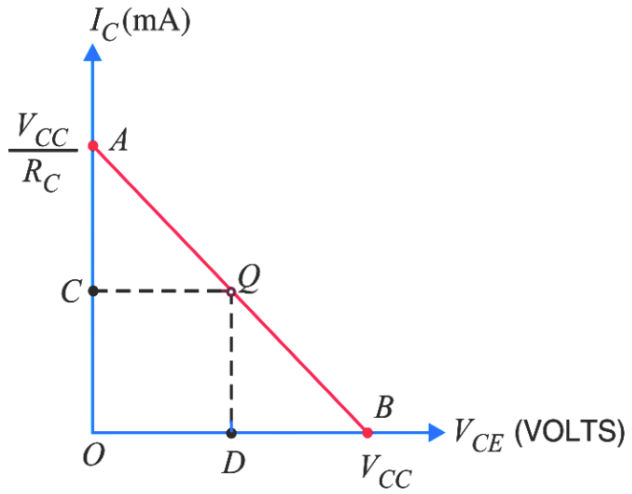
ITMO

BJT, JFETs, MOSFET amplifier configurations

Q-point







The value of collector emitter voltage at any given time will be

$$V_{CE} = V_{CC} - I_C R_C$$

(*A*) When collector-emitter voltage *VCE* = 0, the collector current is maximum and is equal to $I_{C\,MAX} = {}^{V_{CC}}/_{R_C}$

(B) When the collector current $I_C = 0$, then collector-emitter voltage is maximum and is equal to $V_{CE} = V_{CC} - I_C R_C = V_{CC}$

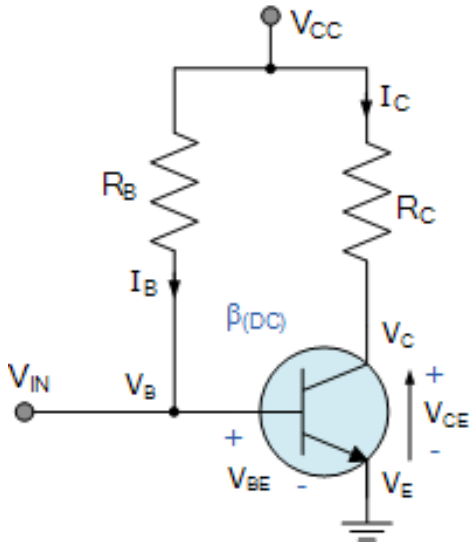
ITMO

BJT biasing

Different Methods for Transistor Biasing

1. *Base Bias or Fixed Current Bias*
It is not a very satisfactory method because bias voltages and currents do not remain constant during transistor operation.
2. Base Bias with Emitter Feedback
This circuit achieves good stability of dc operating point against changes in β with the help of emitter resistor which causes degeneration to take place.
3. Base Bias with Collector Feedback
It is also known as collector-to-base bias or collector feedback bias. It provides better bias stability.
*4. Base Bias with Collector And Emitter Feedback*s
It is a combination of (2) and (3) above.
5. Emitter Bias with Two Supplies
This circuit uses both a positive and a negative supply voltage. Here, base is at approximately 0 volt i.e. V B ≅ 0.
6. Voltage Divider Bias
It is most widely used in linear discrete circuits because it provides good bias stability. It is also called universal bias circuit or base bias with one supply.

Fixed Base Biasing a Transistor



$V_C = V_{CC} - (I_C R_C)$

$V_{CE} = V_C - V_E$

$V_E = 0v$

$V_B = V_{BE}$

$I_B = \frac{V_{CC} - V_{BE}}{R_B}$

$I_C = \beta_{(DC)} I_B$

$I_E = (I_C + I_B) \cong I_C$

Usage:

Due to the inherent drawbacks, fixed bias is rarely used in linear circuits (i.e., those circuits which use the transistor as a current source). Instead, it is often used in circuits where transistor is used as a switch.

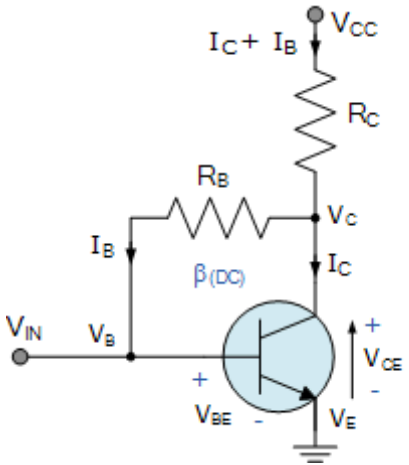
Advantages:

- ✓ Operating point can be shifted easily anywhere in the active region by merely changing the base resistor (RB).
- ✓ A very small number of components are required.

Disadvantages:

- ✓ Poor stabilization
- ✓ High stability factor(S=+1 because I_B is constant so $dI_B/dI_C = 0$), hence prone to thermal runaway

Collector Feedback Biasing a Transistor



$$V_C = V_{CC} - R_C(I_C + I_B)$$
$$V_E = 0v$$
$$V_B = V_{BE}$$
$$I_B = \frac{V_C - V_B}{R_B}$$
$$I_C = \beta_{(DC)} I_B$$
$$I_E = (I_C + I_B) \cong I_C$$

Usage:

The feedback also decreases the input impedance of the amplifier as seen from the base, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted.

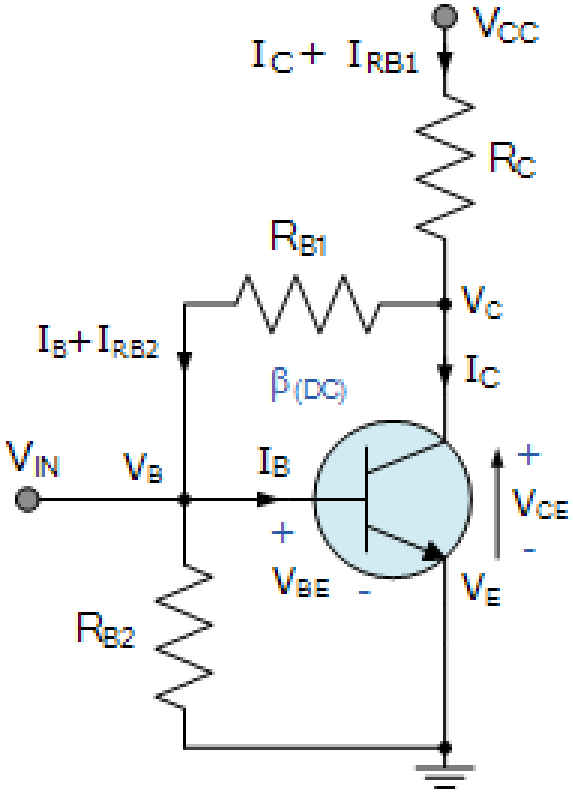
Advantages:

- ✓ Better stabilization compared to fixed bias

Disadvantages:

- ✓ This circuit provides negative feedback which reduces the gain of the amplifier.

Dual Feedback Transistor Biasing

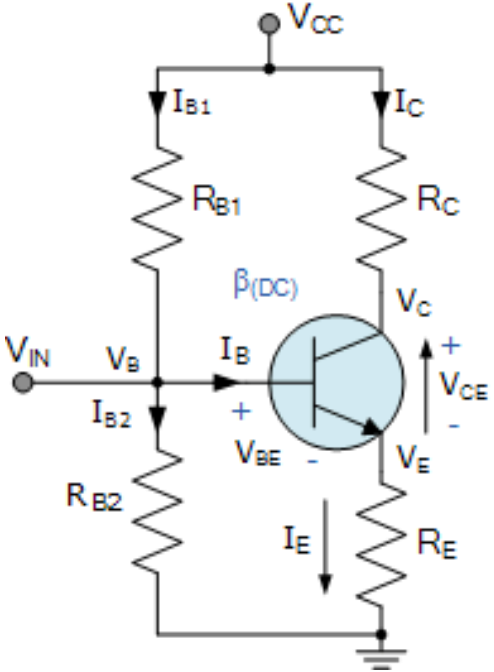


$$V_C = V_{CC} - R_C(I_C + I_{B1})$$
$$V_E = 0v$$
$$V_B = V_{BE}$$
$$I_{RB2} = \frac{V_B}{R_{B2}}$$
$$I_{RB1} = I_B + I_{RB2} = \frac{V_C - V_B}{R_{B1}}$$
$$I_C = \beta_{(DC)} I_B$$
$$I_E = (I_C + I_B) \cong I_C$$

Advantages:

- ✓ Self biasing configuration is that the two resistors provide both automatic biasing and R_f feedback at the same time

Voltage Divider Transistor Biasing



$$V_C = V_{CC} - R_C I_C = (V_E + V_{CE})$$
$$V_E = I_E R_E = V_B - V_{BE}$$
$$V_{CE} = V_C - V_E = V_{CC} - (I_C R_C + I_E R_E)$$
$$V_B = V_{BE} + V_E = V_{RB2} = \left(\frac{R_{B2}}{R_{B1}+R_{B2}}\right) V_{CC}$$
$$I_{B2} = \frac{V_B}{R_{B2}}$$
$$I_{B1} = I_B + I_{B2} = \frac{V_{CC} - V_B}{R_{B1}}$$
$$R_B = \frac{R_{B1} \times R_{B2}}{R_{B1}+R_{B2}} \qquad I_B = \frac{V_B - V_{BE}}{R_B + (1+\beta)R_E}$$
$$I_C = \beta_{(DC)} I_B$$
$$I_E = I_C + I_B = \frac{V_E}{R_E}$$

This voltage divider biasing configuration is the most widely used transistor biasing method.

If $I_C \uparrow \Rightarrow I_E \uparrow \Rightarrow V_{RE} \uparrow \Rightarrow V_{BE} \downarrow \Rightarrow I_B \downarrow \Rightarrow I_C \downarrow$

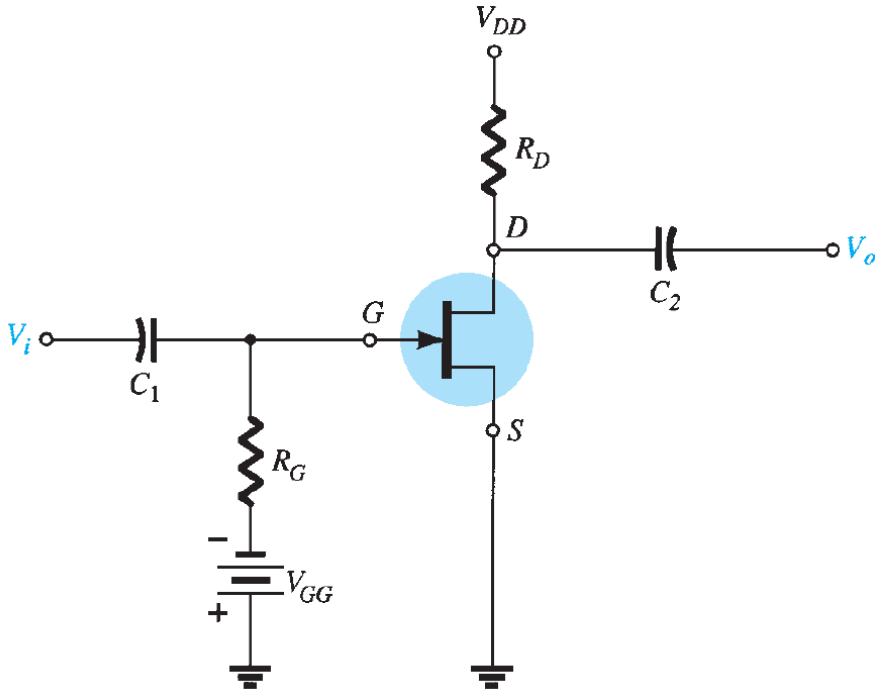
Advantages:

In this kind of biasing, I_C is resistant to the changes in both β as well as V_{BE}, which results in a stability factor of 1 (theoretically), the maximum possible thermal stability.

ITMO

FET biasing

Fixed-Bias Configuration



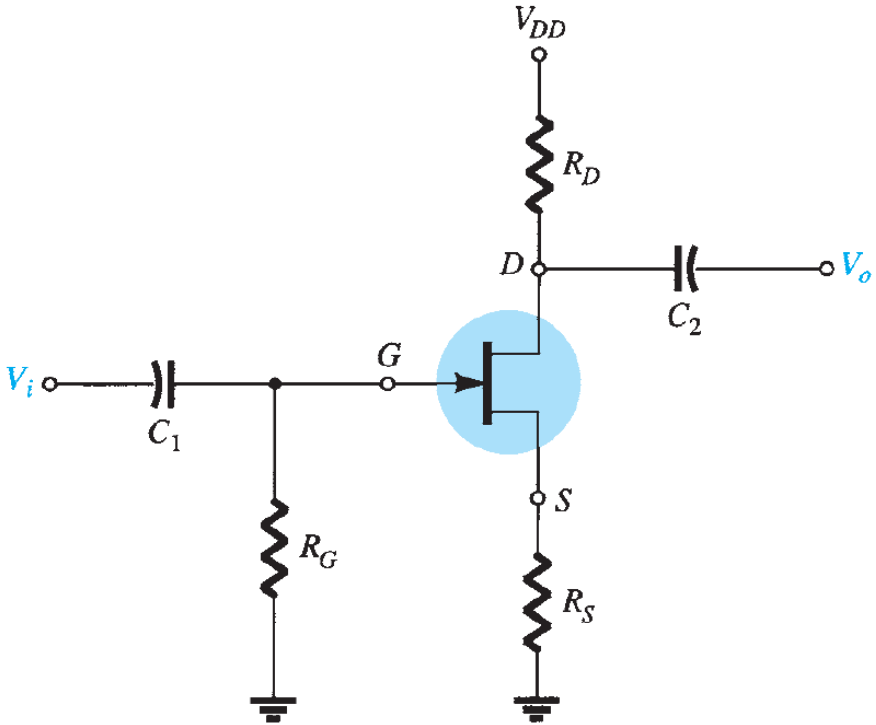
$$I_G \cong 0A$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_S = 0, \quad V_D = V_{DS}, \quad V_{GS} = -V_{GG}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

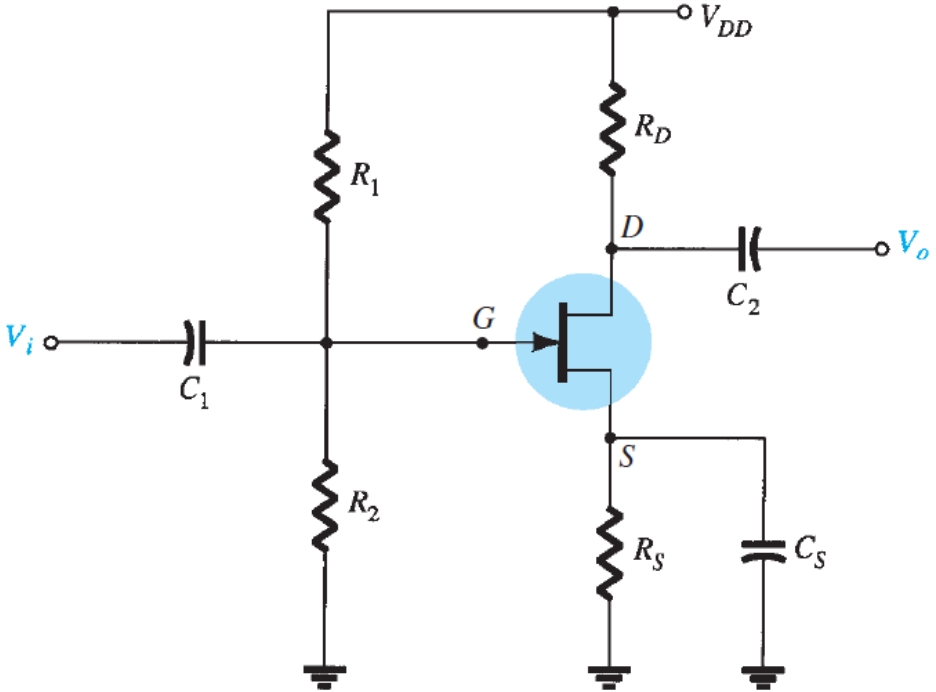
Self-Bias Configuration



$$V_{GS} = -I_D R_S$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Voltage-Divider Bias



$$I_G = 0\ A$$
$$I_{R1} = I_{R2}$$

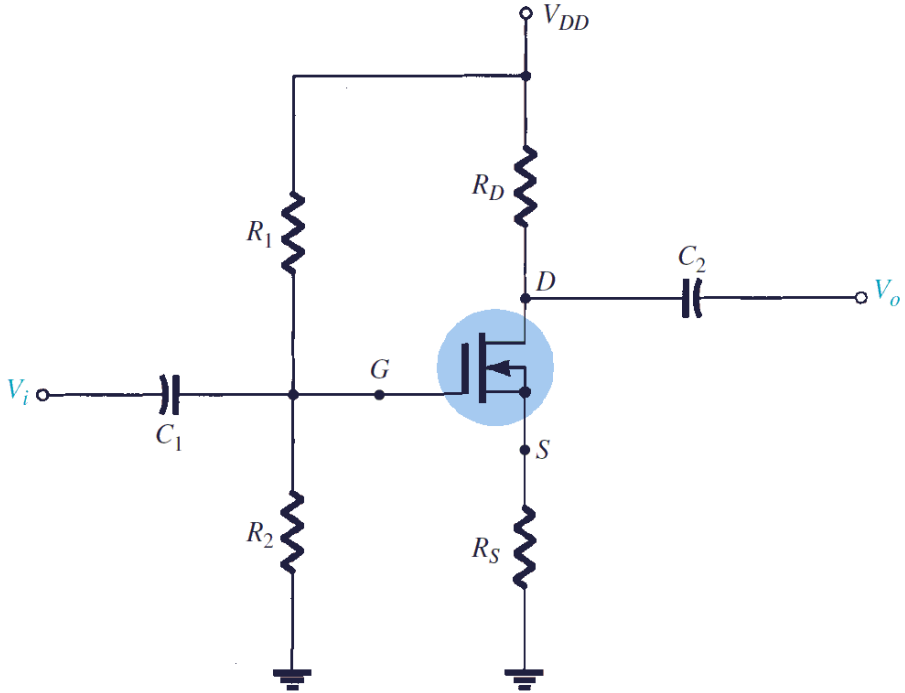
V_G is equal to the voltage across divider resistor R_2:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

D-Type MOSFET Bias Circuits

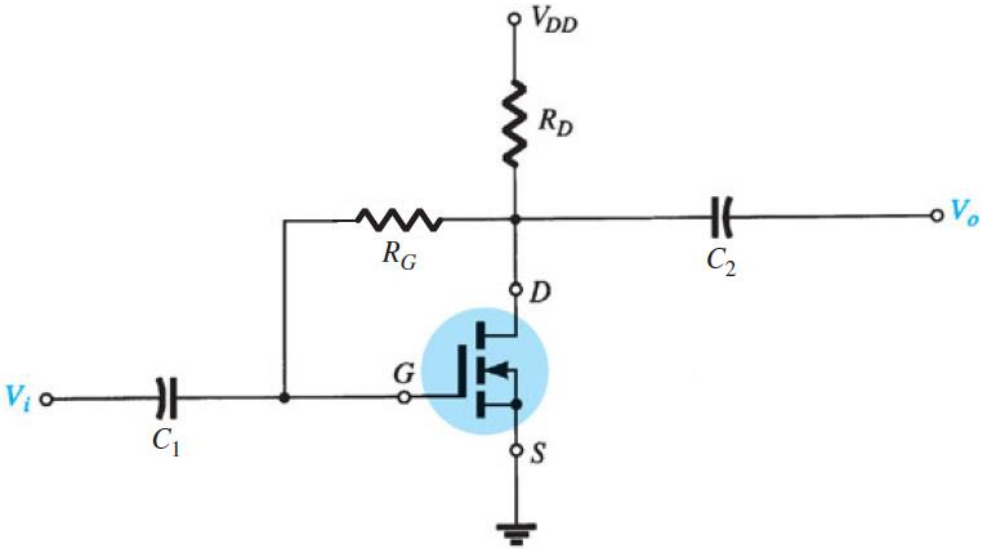
Depletion-type MOSFET



Depletion-type MOSFET bias circuits are similar to those used to bias JFETs. The only difference is that depletion-type MOSFETs can operate with positive values of V_{GS} and with I_D values that exceed I_{DSS}.

Feedback Bias Circuit

Enhancement-type MOSFET



The transfer characteristic for the e-type MOSFET is very different from that of a simple JFET or the d-type MOSFET. So:

$$I_D = k(V_{GS} - V_{GS(\mathrm{Th})})^2$$

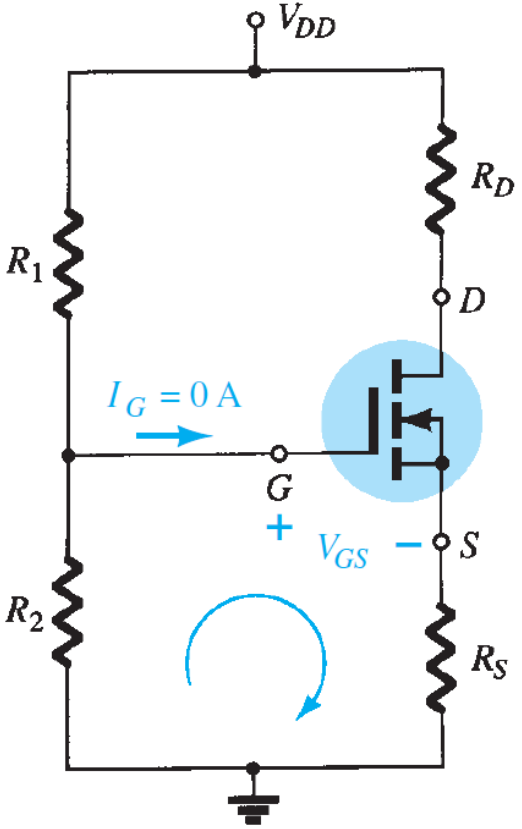
$$I_G = 0\ \mathrm{A}$$

$$V_{RG} = 0\ \mathrm{V}$$

$$V_{DS} = V_{GS}$$

$$\mathbf{V_{GS} = V_{DD} - I_D R_D}$$

Voltage-Divider Biasing

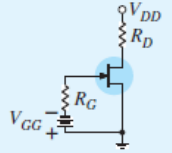
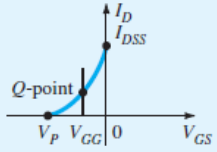
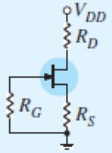
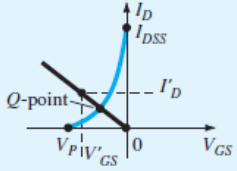
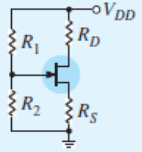
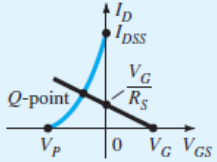
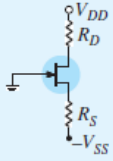
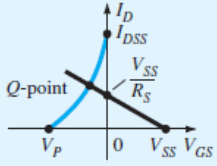
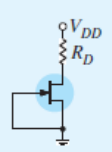
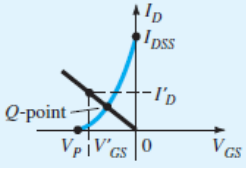


$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

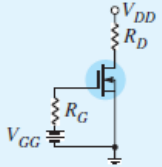
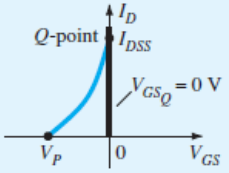
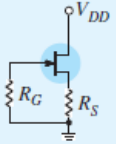
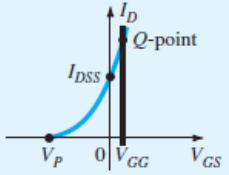
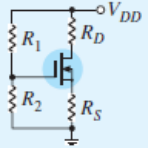
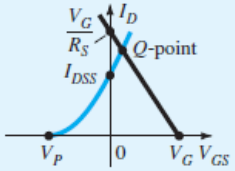
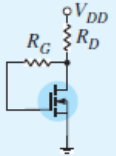
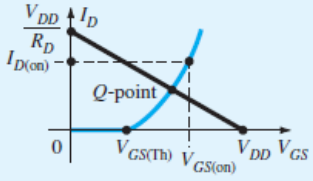
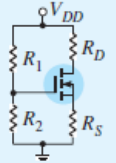
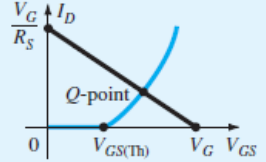
$$V_{GS} = V_G - I_D R_S$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

FET Bias Configurations. Part 1

Type	Configuration	Pertinent Equations	Graphical Solution
JFET Fixed-bias		$V_{GS_Q} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Common-gate		$V_{GS} = V_{SS} - I_D R_S$ $V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$	
JFET ($R_D = 0\ \Omega$)		$V_{GS} = -I_D R_S$ $V_D = V_{DD}$ $V_S = I_D R_S$ $V_{DS} = V_{DD} - I_S R_S$	

FET Bias Configurations. Part 2

JFET Special case ($V_{GS_Q} = 0$ V)		$V_{GS_Q} = 0$ V $I_{D_Q} = I_{DSS}$	
Depletion-type MOSFET Fixed-bias (and MESFETs)		$V_{GS_Q} = +V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
Depletion-type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_S R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
Enhancement type MOSFET Feedback configuration (and MESFETs)		$V_{GS} = V_{DS}$ $V_{GS} = V_{DD} - I_D R_D$	
Enhancement type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$	

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Thank you for your attention!