



Digital circuits design basics. Transistor Switch. Logis Families.

Nikolay Nikolaev

(nanikolaev@itmo.ru)

Nikolai Poliakov

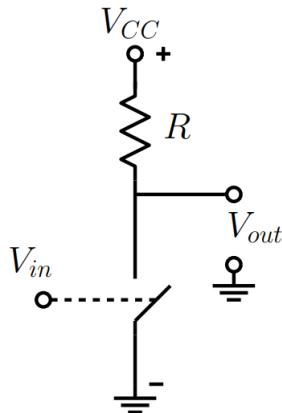
(polyakov_n_a@itmo.ru)

Arina Arbuzina

(arbyzina99@gmail.com)

- Transistor switches
- Logic families:
 - Diode-Resistor Logic;
 - Resistor-Transistor Logic;
 - Diode-Transistor Logic;
 - Transistor-Transistor Logic;
 - Metal Oxide Semiconductor Field Effect Transistor Logic;
 - Combinational Logic.

Transistor switches



Only two levels of signals are used in digital circuits:

- “low”
- “high”.

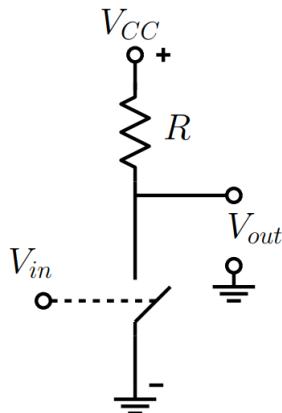
For $V_{in} = 0$ the switch is open and $V_{out} = V_{CC}$.

For $V_{in} = 1$ the switch is close and $V_{out} = 0$ (for ideal switch $R_{SW} = 0$).

Circuit in which a high input yields a low output and a low input yields a high output, is called as an *inverter*.

As switch we can use mechanical switch, but we can't control it by V_{in} .

Transistor switches



Only two levels of signals are used in digital circuits:

- “low”
- “high”.

For $V_{in} = 0$ the switch is open and $V_{out} = V_{CC}$.

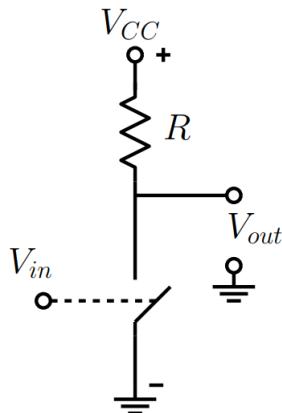
For $V_{in} = 1$ the switch is close and $V_{out} = 0$ (for ideal switch $R_{SW} = 0$).

Circuit in which a high input yields a low output and a low input yields a high output, is called as an *inverter*.

As switch we can use mechanical switch, but we can't control it by V_{in} .

What should we do?

Transistor switches



Only two levels of signals are used in digital circuits:

- “low”
- “high”.

For $V_{in} = 0$ the switch is open and $V_{out} = V_{CC}$.

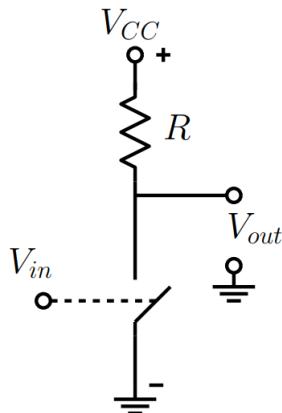
For $V_{in} = 1$ the switch is close and $V_{out} = 0$ (for ideal switch $R_{SW} = 0$).

Circuit in which a high input yields a low output and a low input yields a high output, is called as an *inverter*.

As switch we can use mechanical switch, but we can't control it by V_{in} .

What should we do? Which electronic components can we use?

Transistor switches



Only two levels of signals are used in digital circuits:

- “low”
- “high”.

For $V_{in} = 0$ the switch is open and $V_{out} = V_{CC}$.

For $V_{in} = 1$ the switch is close and $V_{out} = 0$ (for ideal switch $R_{SW} = 0$).

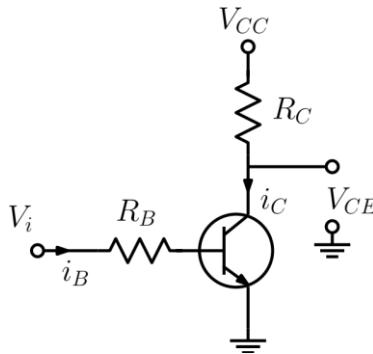
Circuit in which a high input yields a low output and a low input yields a high output, is called as an *inverter*.

As switch we can use mechanical switch, but we can't control it by V_{in} .

What should we do? Which electronic components can we use?

For instance we can use a **transistor**.

Transistor switches

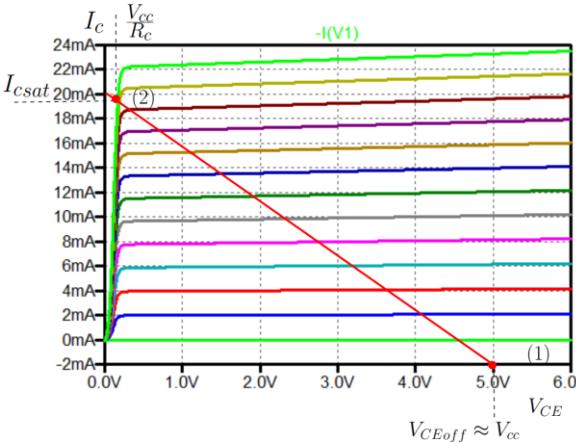


The transistor switch is the basic element of logic circuits.
We consider a typical inverter circuit using a bipolar transistor.

For this scheme we have

$$V_{CE} = V_{CC} - R_C i_C$$

$$V_{BE} = V_i - R_B i_B$$

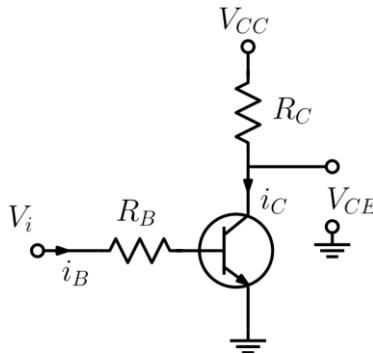


When $V_{in} = 0$ (logic zero) the base current is zero and the transistor is closed $V_{out} \cong V_{CC}$ (operating point 1).

Only very small value of collector current ($I_{C_{off}} \cong I_{CE0}$) flows. I_{CE0} - is a collector current for $i_B = 0$.

$$V_{out} = V_{CC} - R_C i_C \cong V_{CC}$$

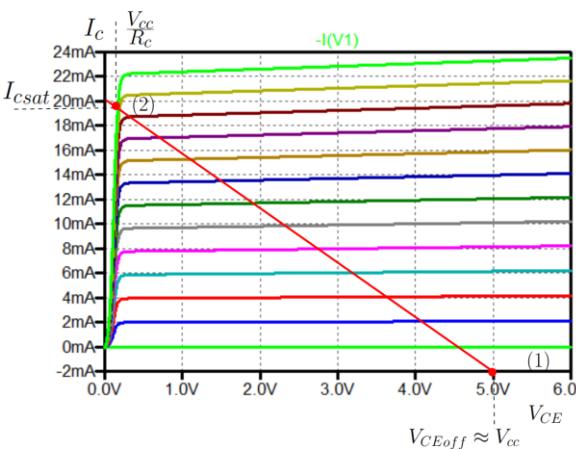
Transistor switches



If V_{in} is logic 1 level (+5 V) then

$$I_{B_{sat}} = \frac{V_i - V_{BE}}{R_B}$$

$V_{BE} \cong 0.7 \text{ V}$ which is the *threshold voltage*.



i_B must be chosen to drive the transistor into saturation (operating point 2). For current $i_B > 20 \text{ mA}$ the transistor is said to be *saturated* (transistor is on).

In saturated state $V_{CE_{sat}} \cong 0.2 \dots 0.3 \text{ V}$.

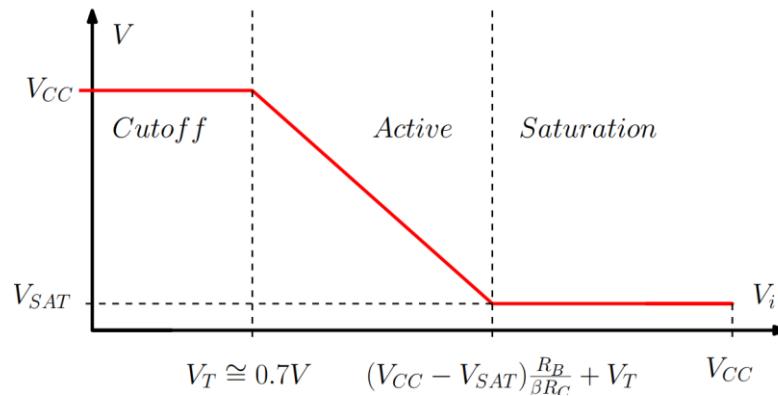
The power dissipated in the transistor is very small

$$P = V_{CE} i_c + V_{BE} i_B \cong V_{CE} i_c$$

Because $V_{CE} \cong 0$ or $i_c \cong 0$.

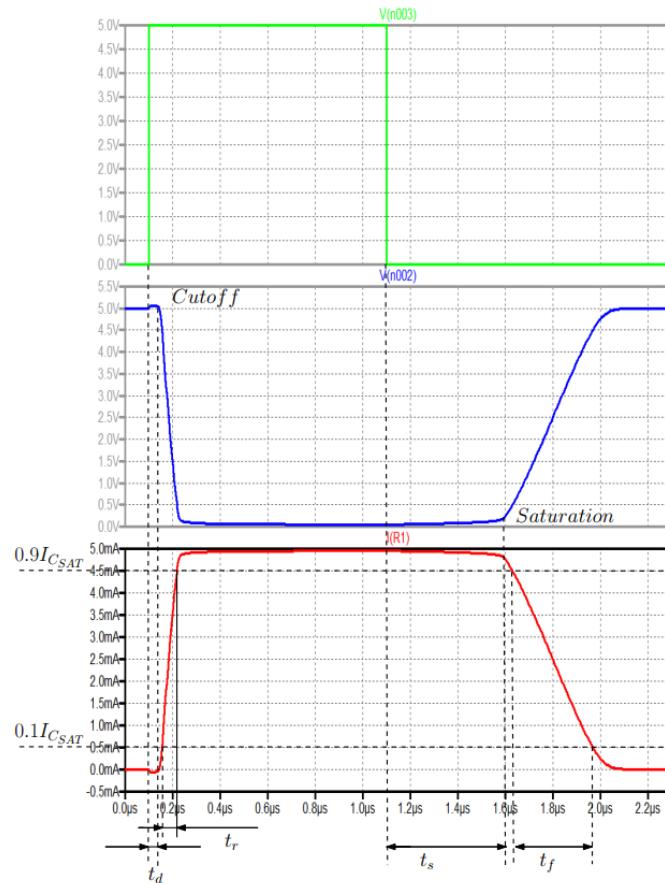
Transistor switches

The transfer characteristic of a BJT switch



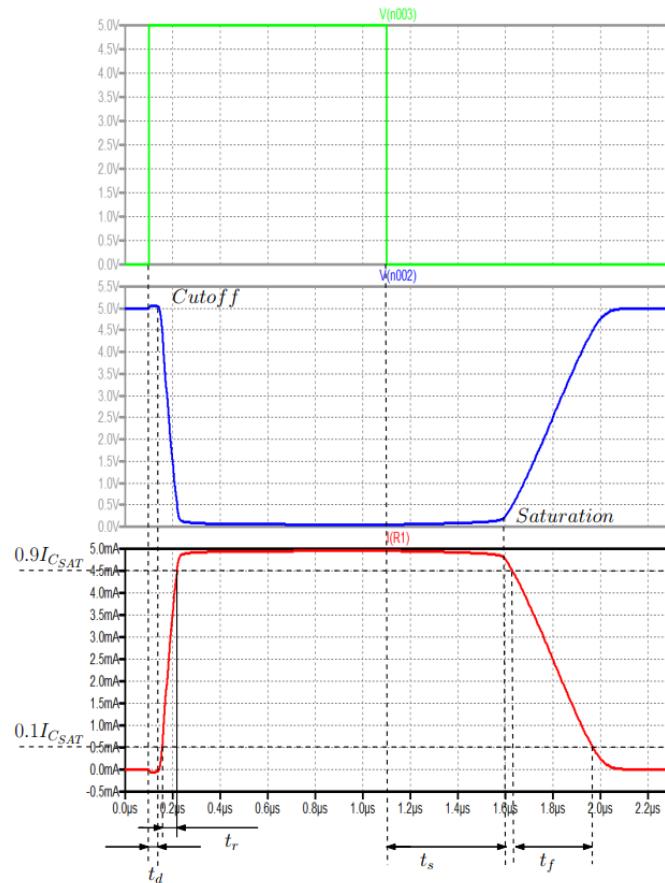
Transistor switches

- Propagation delay t_d is a certain amount of delay for a change to occur. It is defined here as the time to change from 0 to 10 % of the final value.



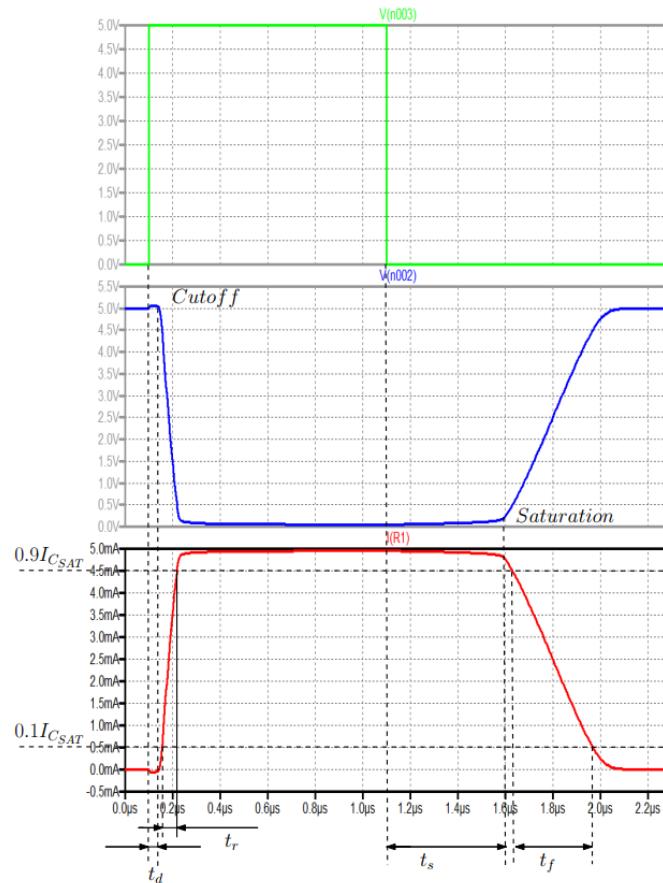
Transistor switches

- Propagation delay t_d is a certain amount of delay for a change to occur. It is defined here as the time to change from 0 to 10 % of the final value.
- Rise time t_r is the time needed to change from 10 to 90% of the final level.



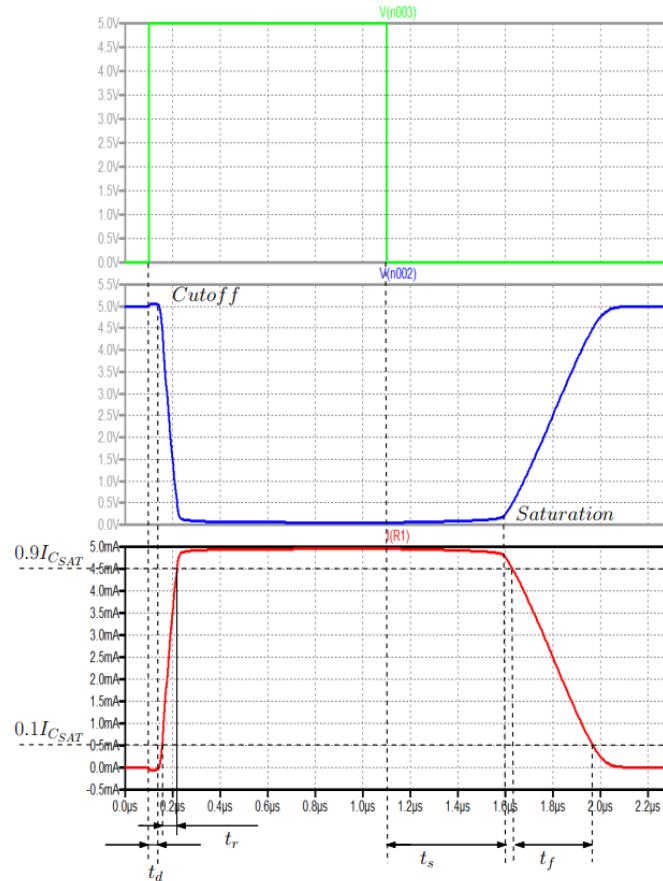
Transistor switches

- Propagation delay t_d is a certain amount of delay for a change to occur. It is defined here as the time to change from 0 to 10 % of the final value.
- Rise time t_r is the time needed to change from 10 to 90% of the final level.
- Propagation delay t_s occurs when the input pulse returns to 0 V (i.e., logic level 0). This is a result of the time required to remove charge stored in the base region before the transistor begins to switch out of saturation and is usually longer than t_d .



Transistor switches

- Propagation delay t_d is a certain amount of delay for a change to occur. It is defined here as the time to change from 0 to 10 % of the final value.
- Rise time t_r is the time needed to change from 10 to 90% of the final level.
- Propagation delay t_s occurs when the input pulse returns to 0 V (i.e., logic level 0). This is a result of the time required to remove charge stored in the base region before the transistor begins to switch out of saturation and is usually longer than t_d .
- Fall time t_f is the time required for the output voltage and the collector current to change state. That is the time required to switch through the active region from saturation to cutoff.



Transistor switch. Conclusion

The bipolar transistor is a very commonly used switch in digital electronic circuits. It is a three-terminal semiconductor component that allows an input signal at one of its terminals to cause the other two terminals to become a short or an open circuit.

In an electronic circuit, the input signal (1 or 0) is usually applied to the base of the transistor, which causes the collector–emitter junction to become a short or an open circuit.

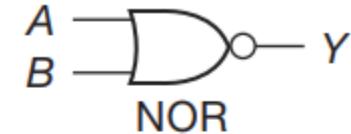
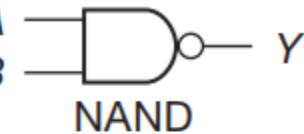
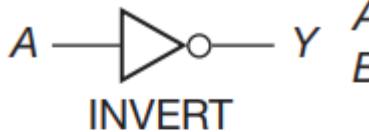
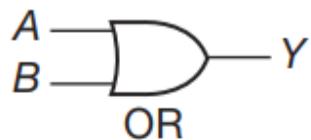
The rules of transistor switching are as follows:

1. In an NPN transistor, applying a positive voltage from base to emitter causes the collector-to-emitter junction to short (this is called “turning the transistor ON”). Applying a negative voltage or 0 V from base to emitter causes the collector-to-emitter junction to open (this is called “turning the transistor OFF”).
2. In a PNP transistor, applying a negative voltage from base to emitter turns it ON. Applying a positive voltage or 0 V from base to emitter turns it OFF.

iTMO

Logis Families.

Logic elements



inputs		output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

inputs		output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

A	Y
0	1
1	0

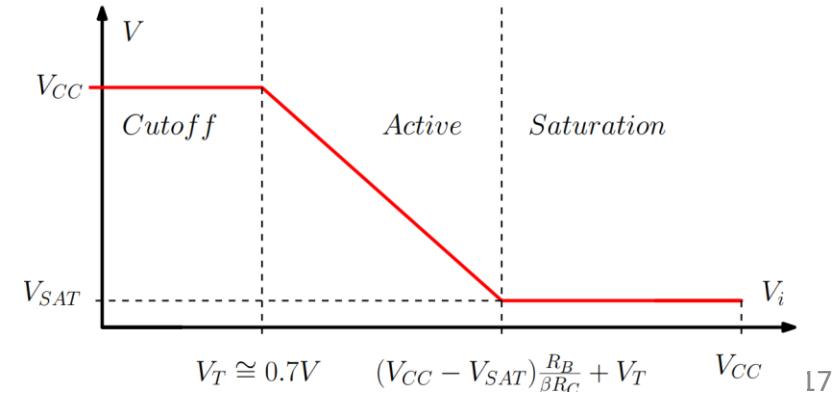
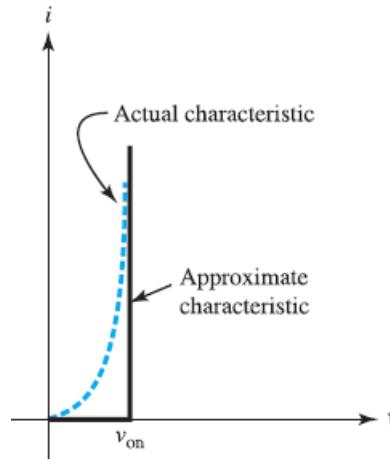
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Logic Families

Main concepts for analysis digital schemes are follows from forward diode voltage and switch mode of BJT transistor (we will suppose we use silicone discrete components):

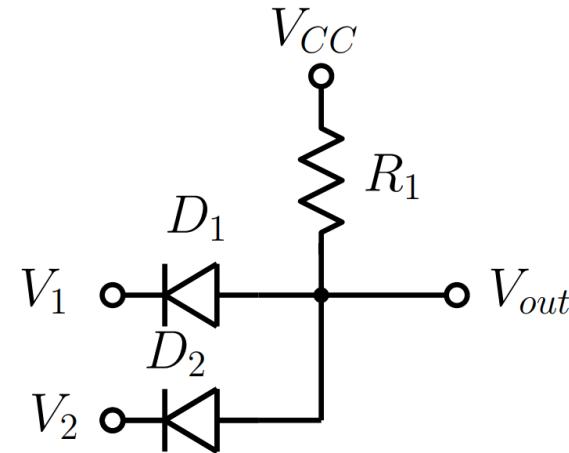
1. Threshold voltage of p-n junction is 0.7 V;
2. In saturated state for BJT is true $V_{CE_{sat}} \cong 0.2 \dots 0.3 \text{ V}$
3. In cutoff region BJT is closed ($I_c = I_e = I_b = 0$)



Diode-Resistor Logic (DRL) Gates.

The diode-resistor logic circuits consist of diodes and resistors only.

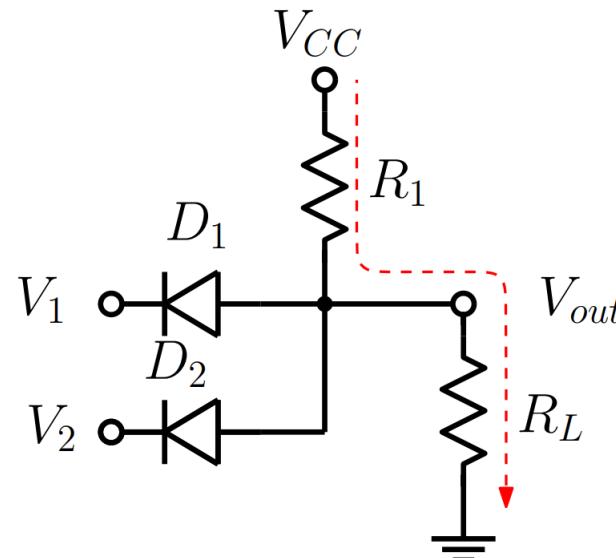
1. AND Gate



V_1	V_2	V_{out}
1	1	1
1	0	0
0	1	0
0	0	0

Diode-Resistor Logic (DRL) Gates. **AND Gate.**

1.1. $V_1 = V_2 = 1$



V_1	V_2	V_{out}
1	1	1
1	0	0
0	1	0
0	0	0

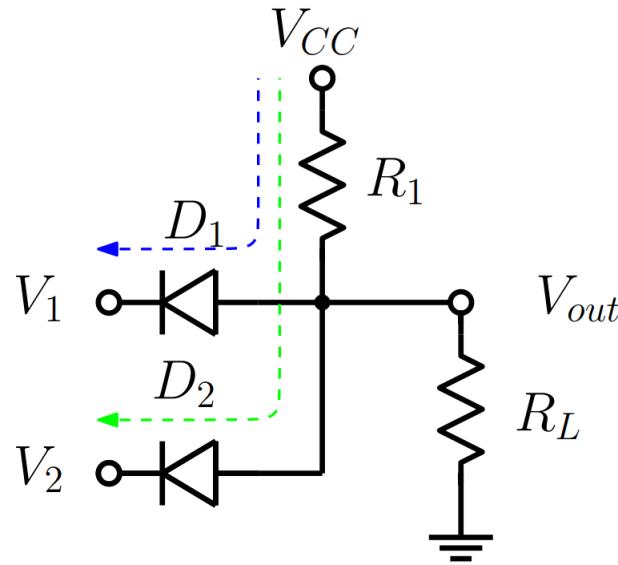
for $R_L \gg R_1$

$$V_{out} \cong V_{CC}$$

Logic Families. DRL.

Diode-Resistor Logic (DRL) Gates. **AND Gate.**

1.2. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 0$;



V_1	V_2	V_{out}
1	1	1
1	0	0
0	1	0
0	0	0

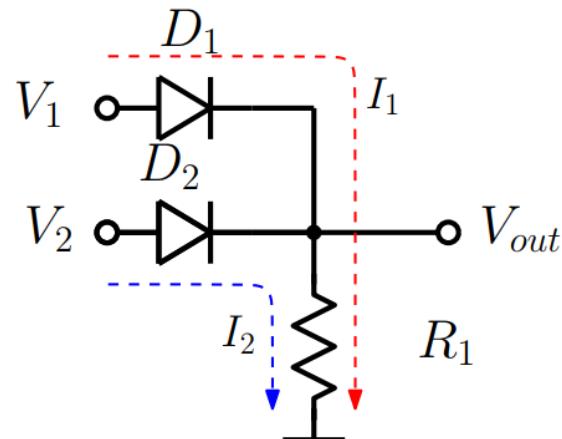
$$V_{out} = V_1 + V_{D_1}$$

$$V_{out} = V_2 + V_{D_2}$$

Diode-Resistor Logic (DRL) Gates.

2. OR Gate.

2.1. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 1$;



V_1	V_2	V_{out}
1	1	1
1	0	1
0	1	1
0	0	0

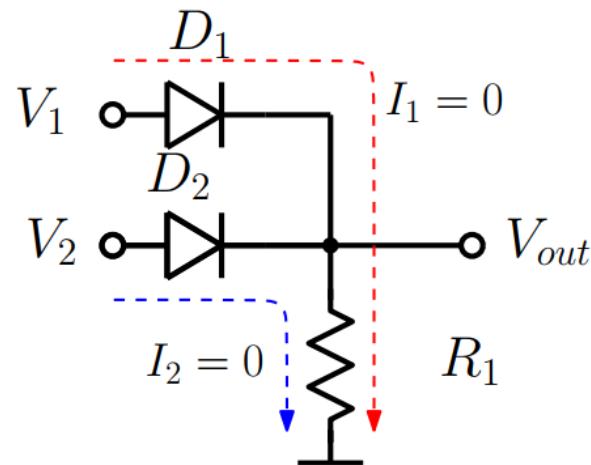
$$V_{out} = V_1 - V_{VD_1}$$

$$V_{out} = V_2 - V_{VD_2}$$

Diode-Resistor Logic (DRL) Gates.

2. OR Gate.

2.2. $V_1 = V_2 = 0$;

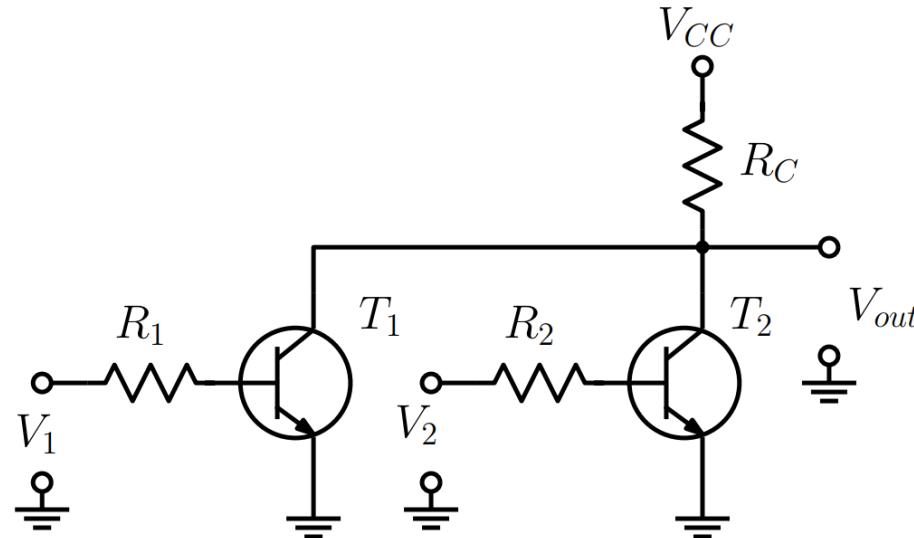


V_1	V_2	V_{out}
1	1	1
1	0	1
0	1	1
(0)	(0)	(0)

$$V_{out} = 0$$

Resistor-Transistor Logic (RTL) Gates.

1. NOR Gate.

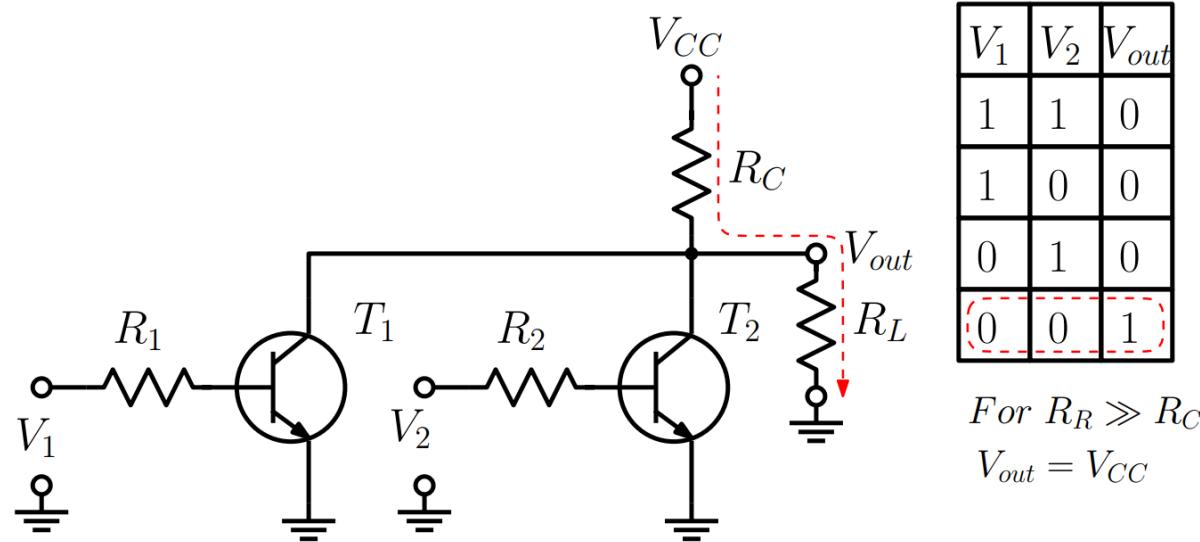


V_1	V_2	V_{out}
1	1	0
1	0	0
0	1	0
0	0	1

Resistor-Transistor Logic (RTL) Gates.

1. NOR Gate.

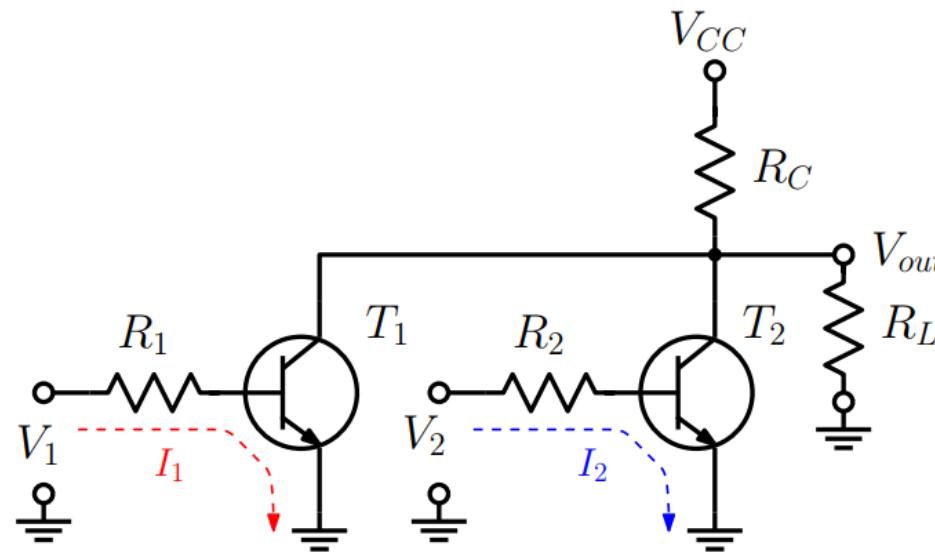
1.1. $V_1 = V_2 = 0$;



Resistor-Transistor Logic (RTL) Gates.

1. NOR Gate.

1.1. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 1$;

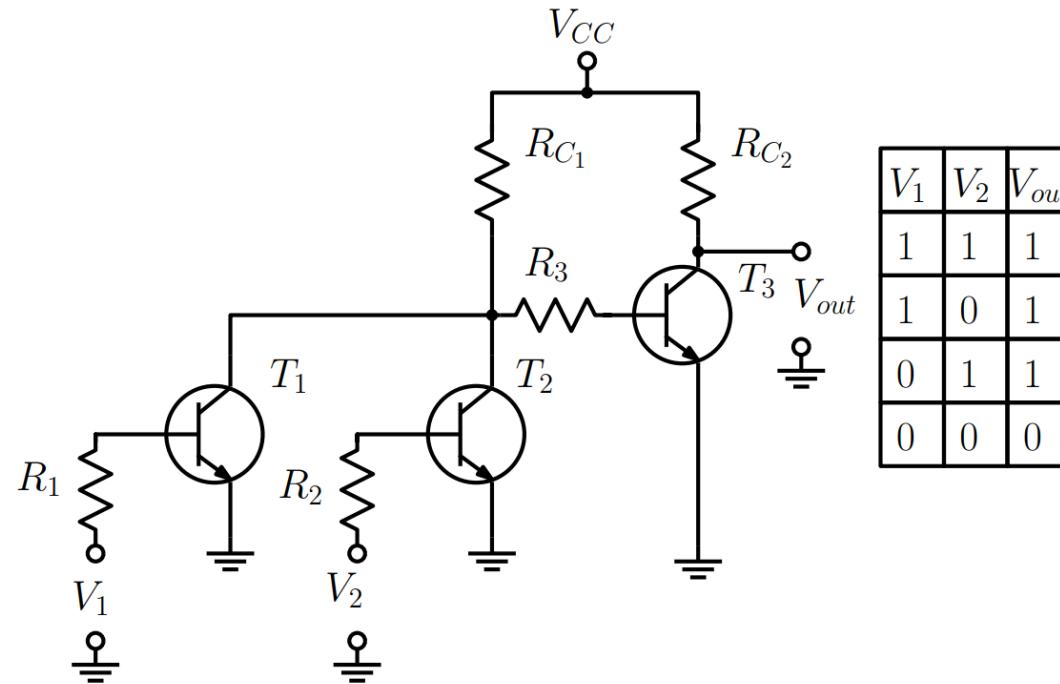


V_1	V_2	V_{out}
1	1	0
1	0	0
0	1	0
0	0	1

$$V_{out} = V_{CESAT}$$

Resistor-Transistor Logic (RTL) Gates.

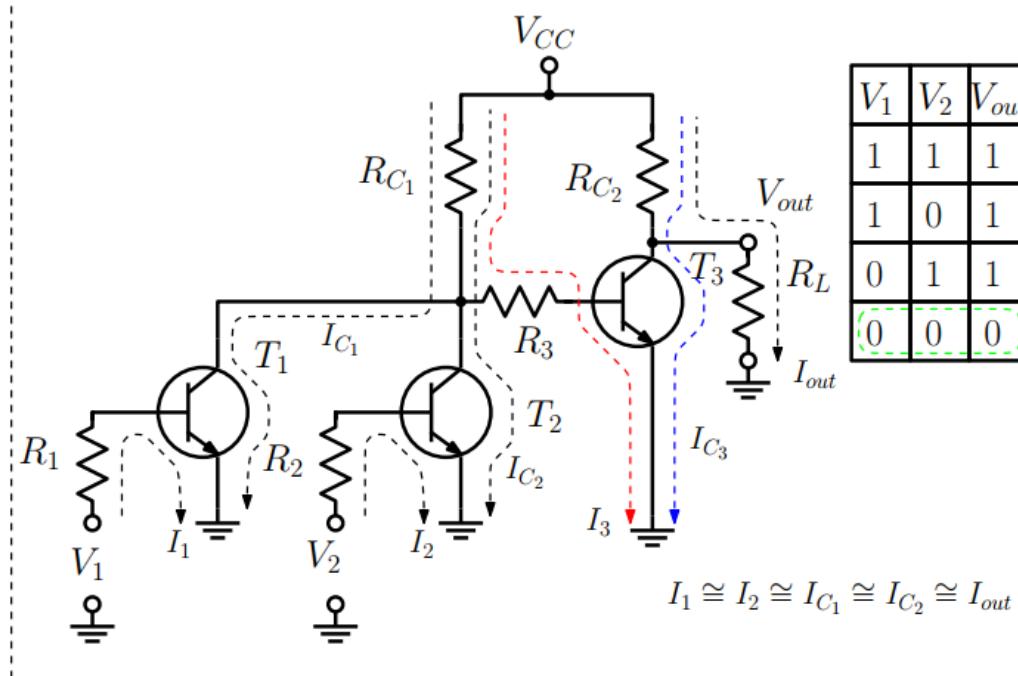
2. OR Gate.



Resistor-Transistor Logic (RTL) Gates.

2. OR Gate.

2.1. $V_1 = V_2 = 0$;

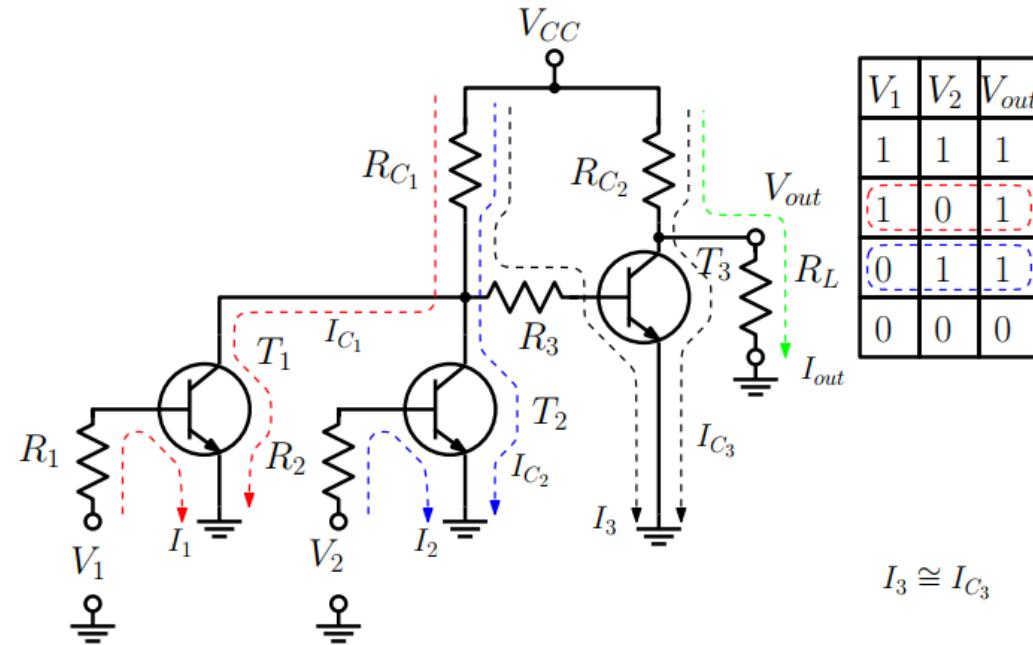


Logic Families. RTL.

Resistor-Transistor Logic (RTL) Gates.

2. OR Gate.

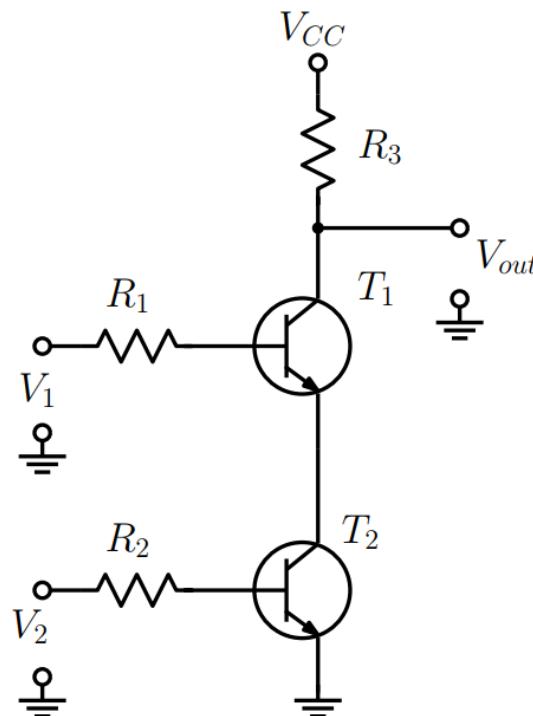
2.2. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 1$;



Logic Families. RTL.

Resistor-Transistor Logic (RTL) Gates.

3. NAND Gate.

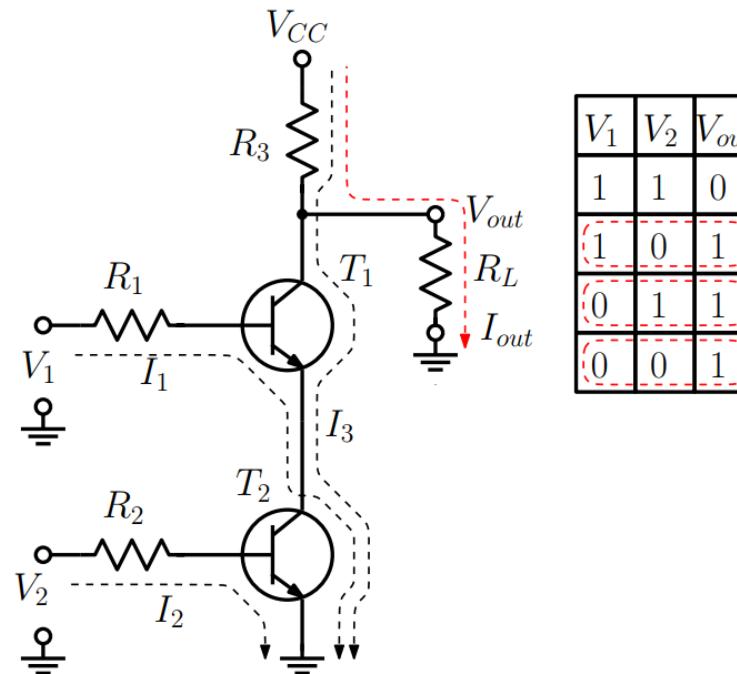


V_1	V_2	V_{out}
1	1	0
1	0	1
0	1	1
0	0	1

Resistor-Transistor Logic (RTL) Gates.

3. NAND Gate.

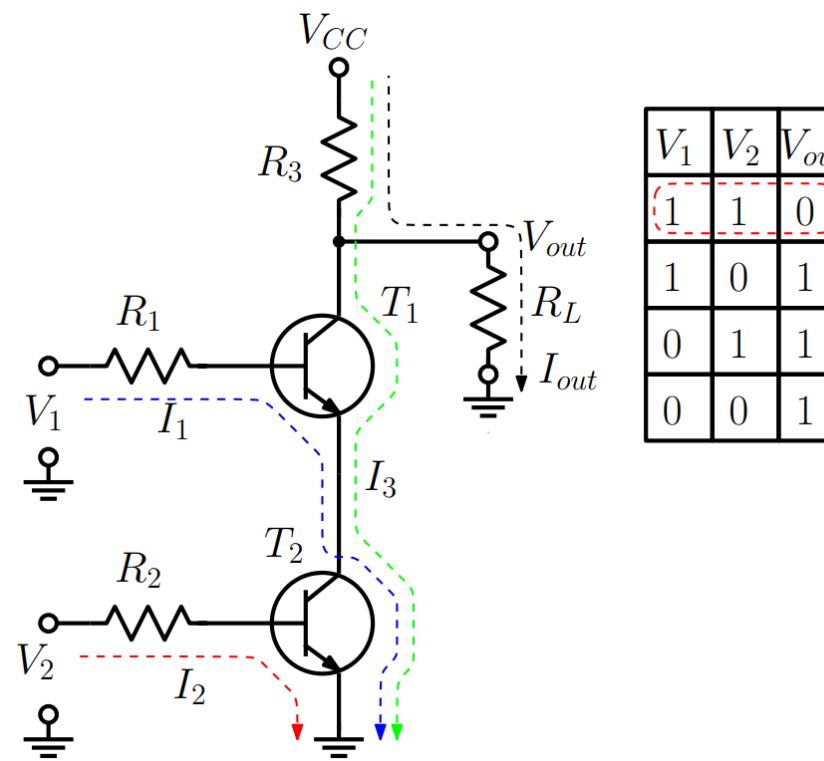
3.1. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 0$;



Resistor-Transistor Logic (RTL) Gates.

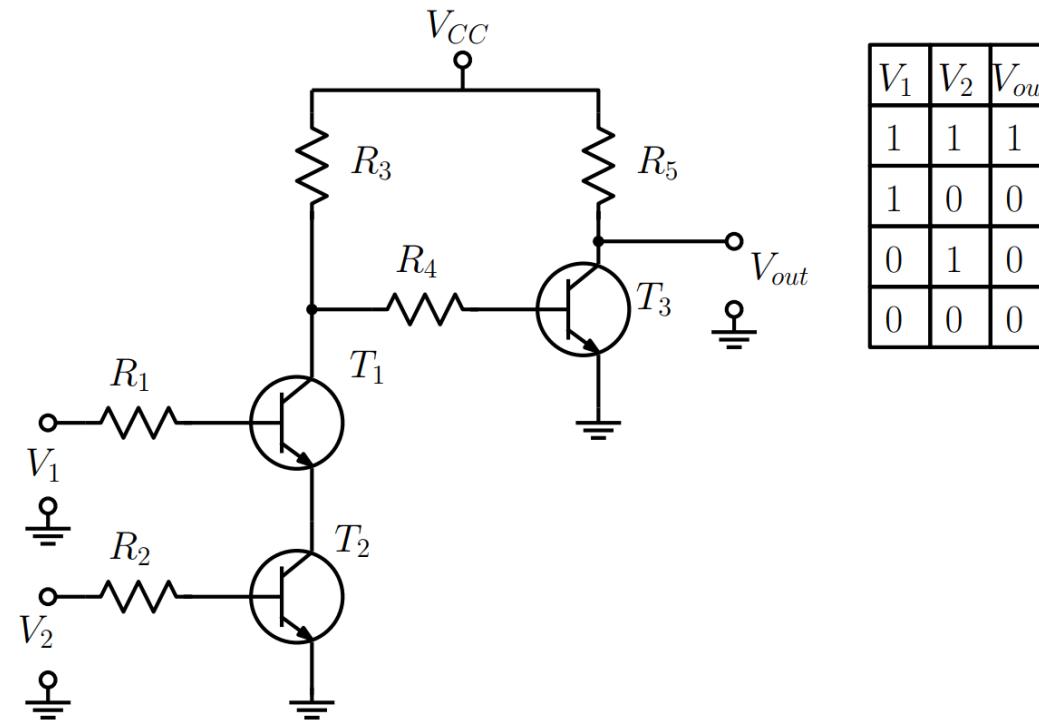
3. NAND Gate.

3.2. $V_1 = V_2 = 1$;



Resistor-Transistor Logic (RTL) Gates.

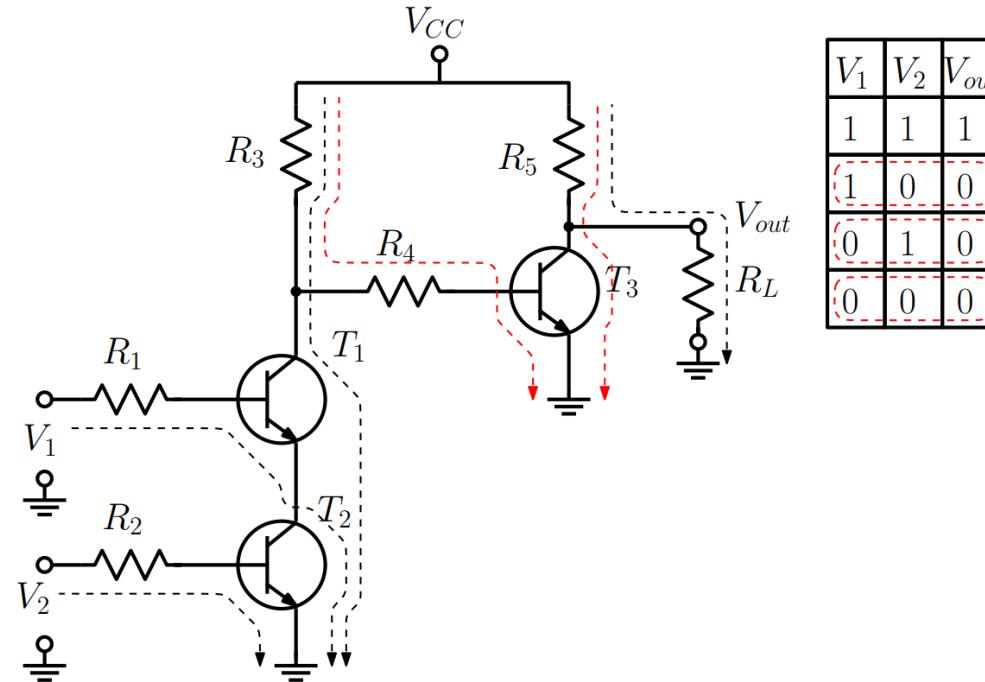
4. AND Gate.



Resistor-Transistor Logic (RTL) Gates.

4. AND Gate.

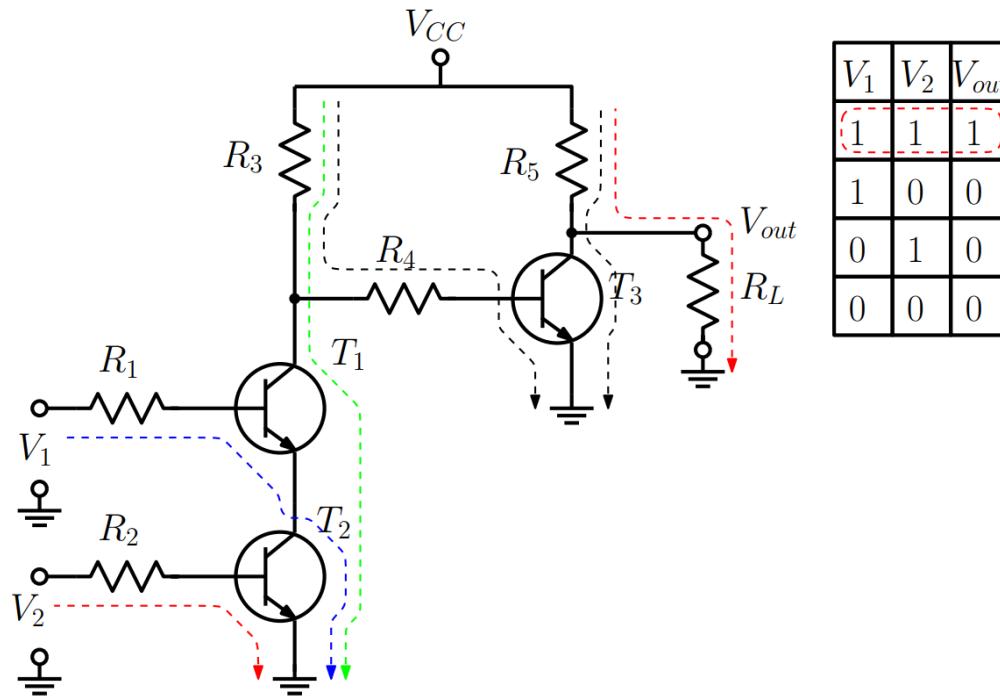
4.1. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 0$;



Resistor-Transistor Logic (RTL) Gates.

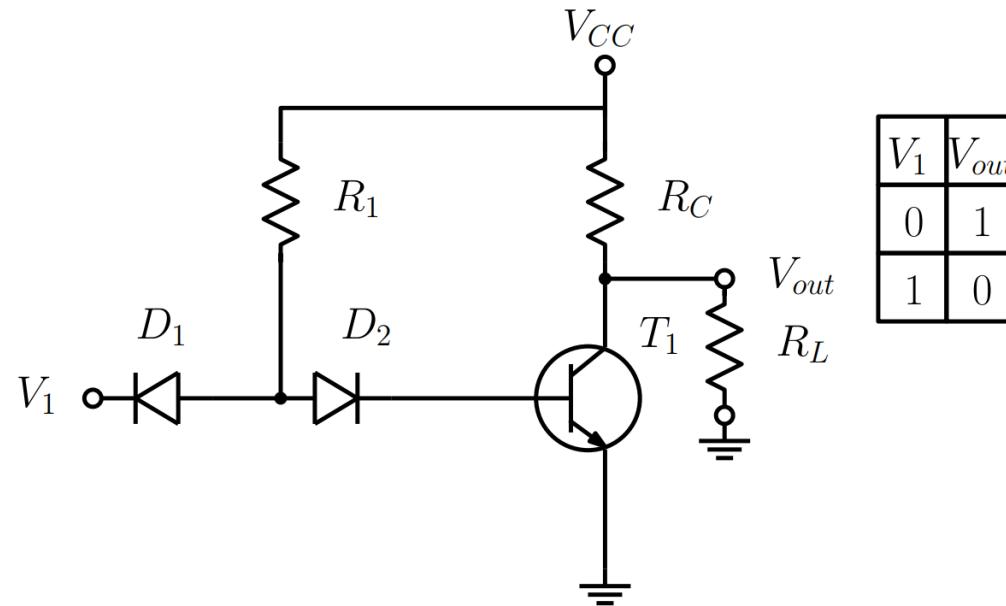
4. AND Gate.

4.2. $V_1 = V_2 = 1$;



Diode-Transistor Logic (DTL) Gates.

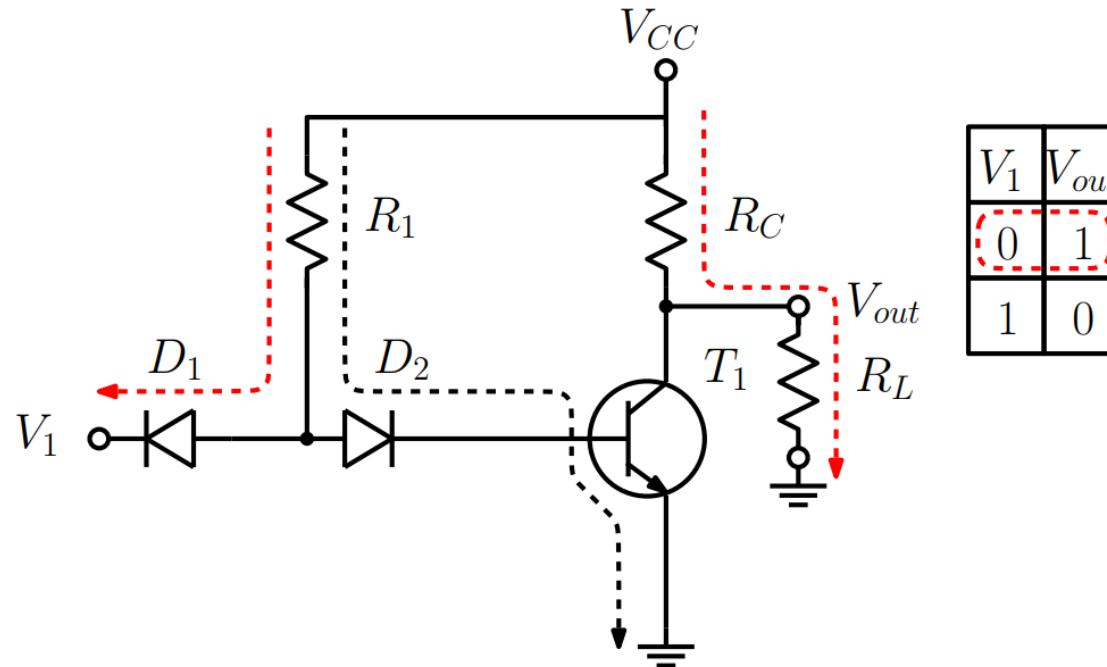
1. Inverter.



Logic Families. DTL.

Diode-Transistor Logic (DTL) Gates.

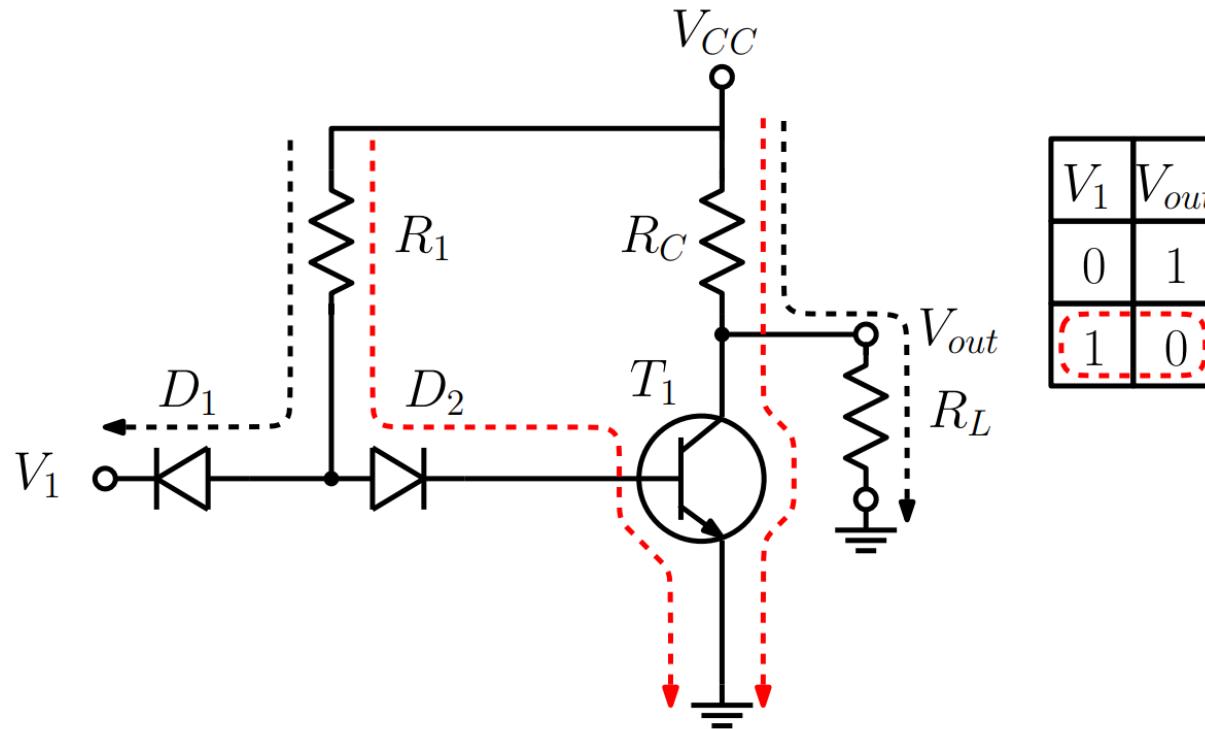
1.1. Inverter. $V_1 = 0$;



Logic Families. DTL.

Diode-Transistor Logic (DTL) Gates.

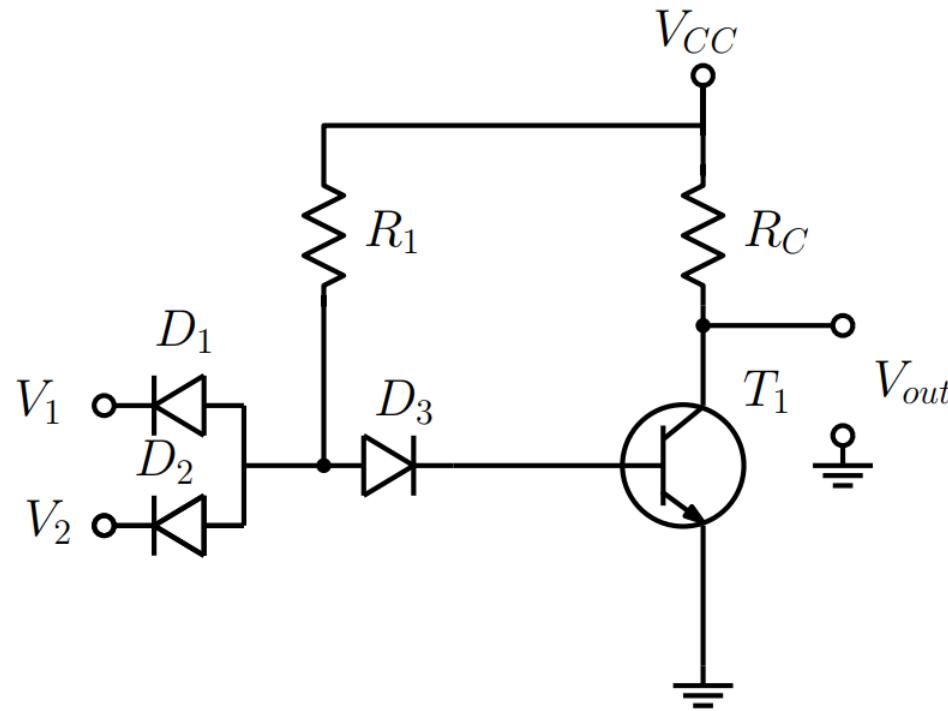
1.2. Inverter. $V_1 = 1$;



Logic Families. DTL.

Diode-Transistor Logic (DTL) Gates.

2. NAND Gate.



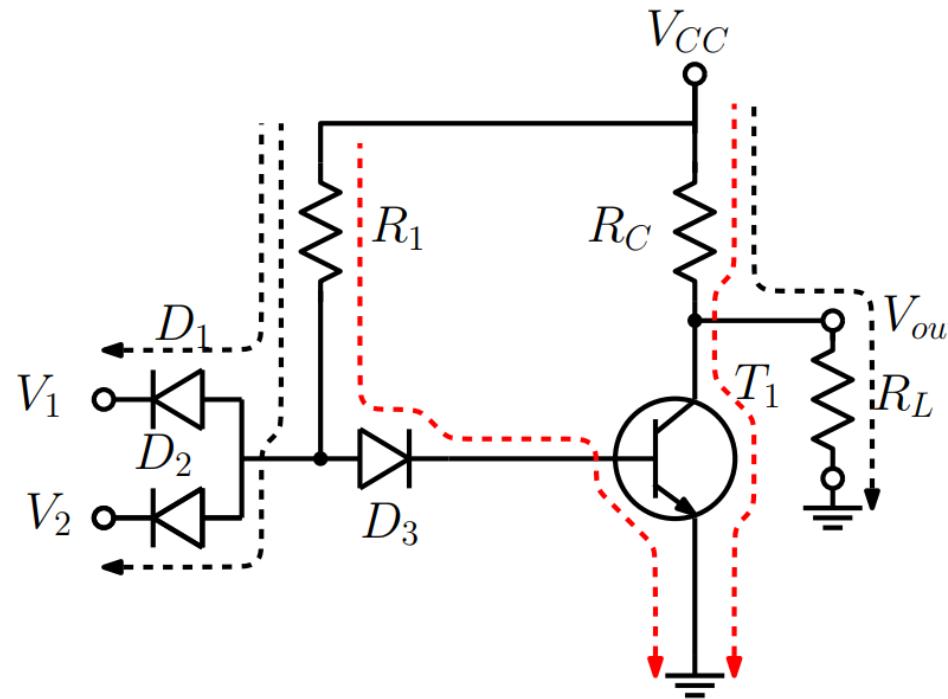
V_1	V_2	V_{out}
1	1	0
1	0	1
0	1	1
0	0	1

Logic Families. DTL.

Diode-Transistor Logic (DTL) Gates.

2. NAND Gate.

2.1. $V_1 = V_2 = 1$;

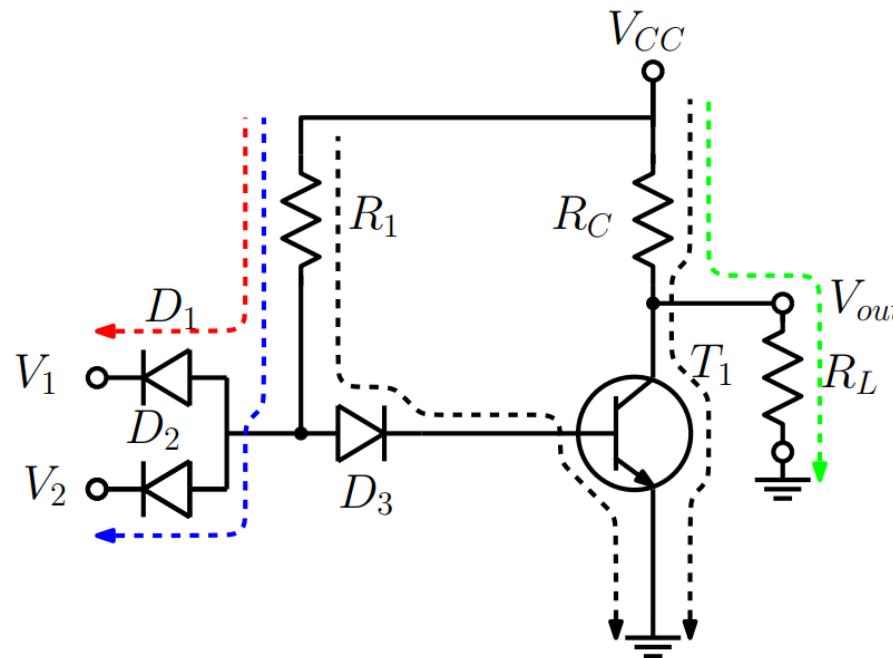


V_1	V_2	V_{out}
1	1	0
1	0	1
0	1	1
0	0	1

Diode-Transistor Logic (DTL) Gates.

2. NAND Gate.

2.1. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 0$;

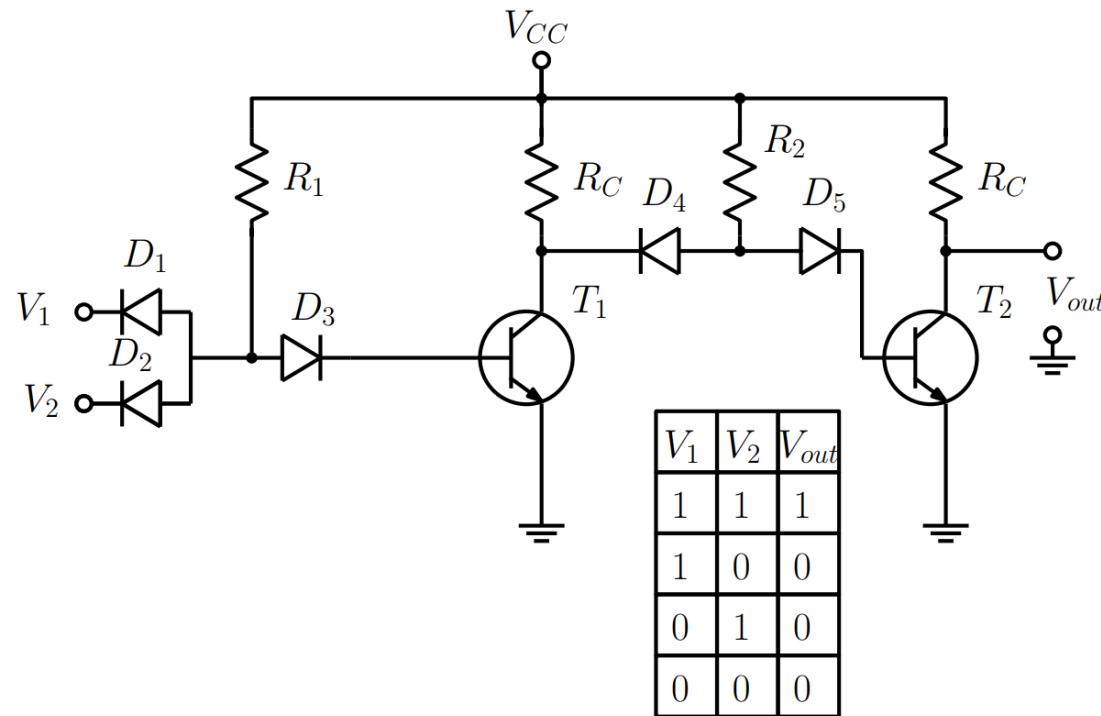


V_1	V_2	V_{out}
1	1	0
1	0	1
0	1	1
0	0	1

Logic Families. DTL.

Diode-Transistor Logic (DTL) Gates.

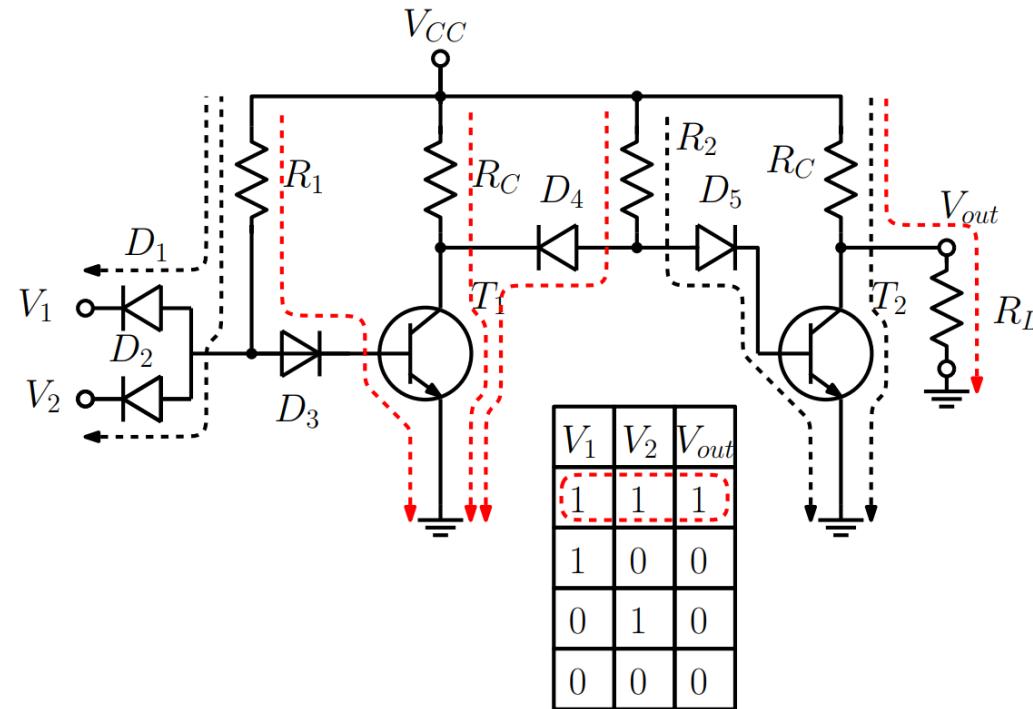
3. AND Gate.



Diode-Transistor Logic (DTL) Gates.

3. AND Gate.

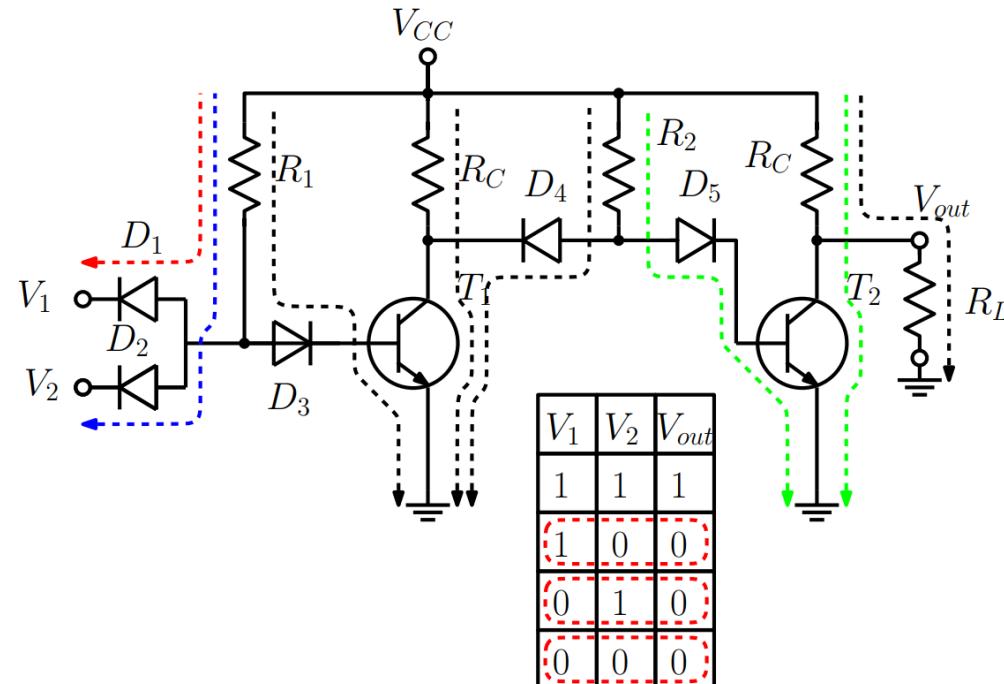
3.1. $V_1 = V_2 = 1$;



Diode-Transistor Logic (DTL) Gates.

3. AND Gate.

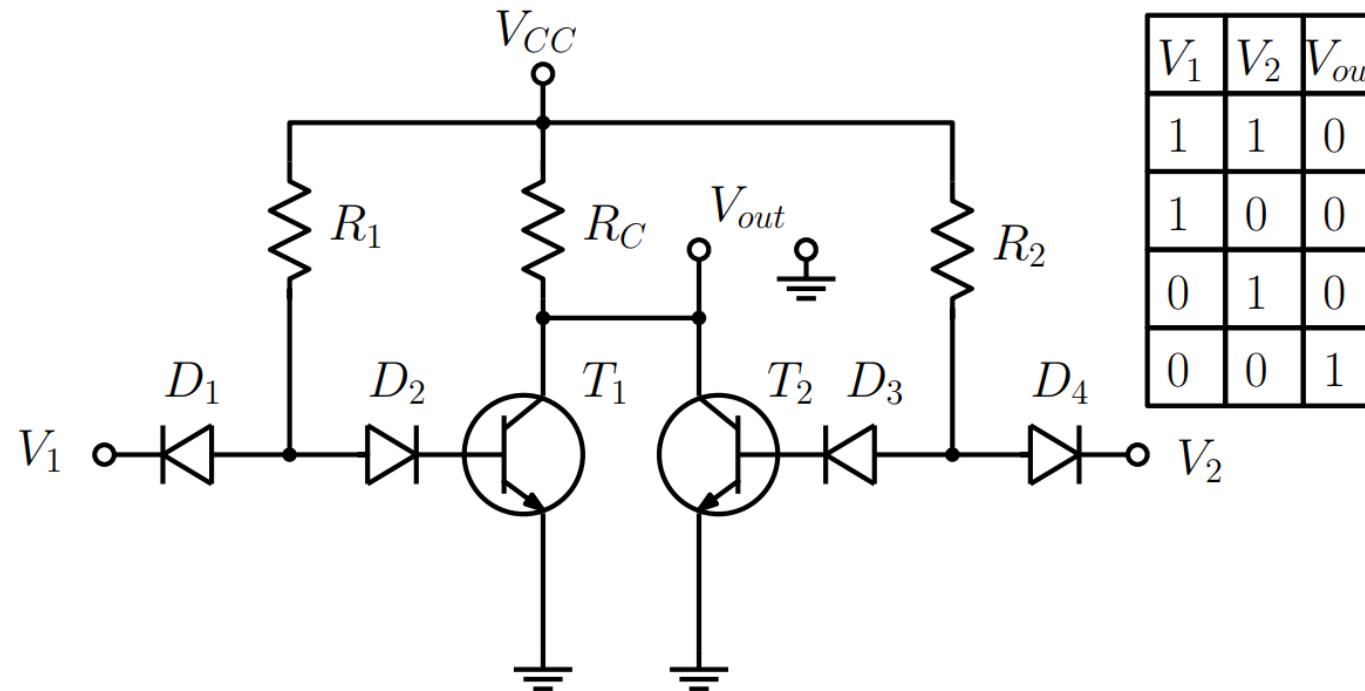
3.2. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 0$;



Logic Families. DTL.

Diode-Transistor Logic (DTL) Gates.

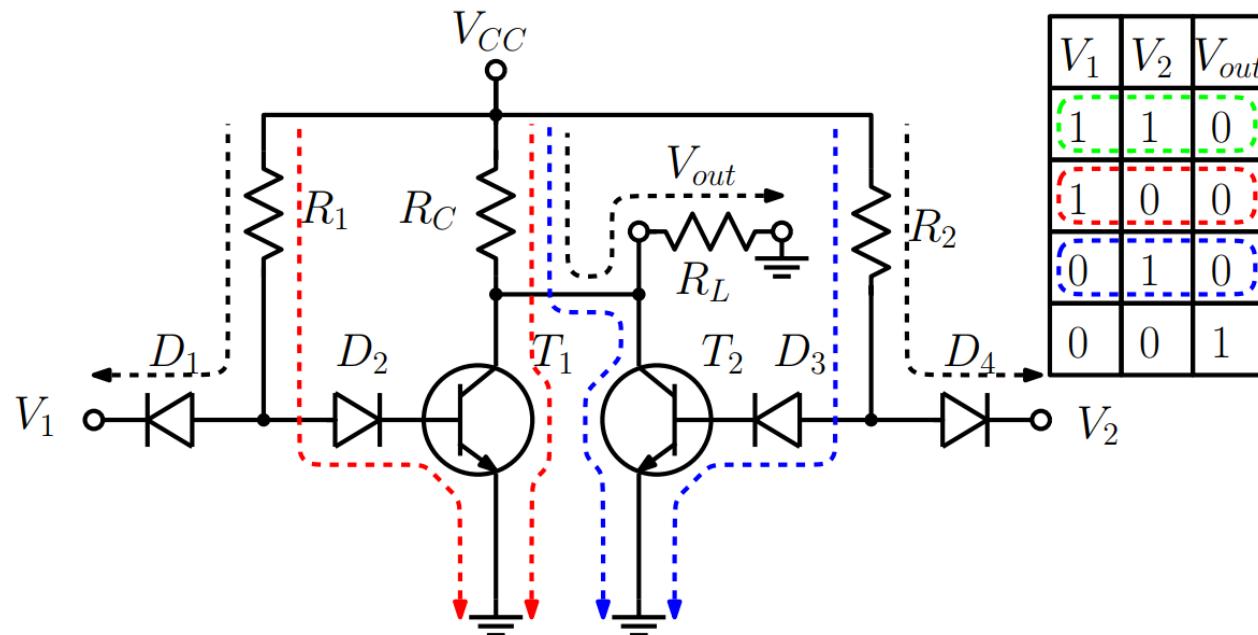
4. NOR Gate.



Diode-Transistor Logic (DTL) Gates.

4. NOR Gate.

4.1. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 1$;



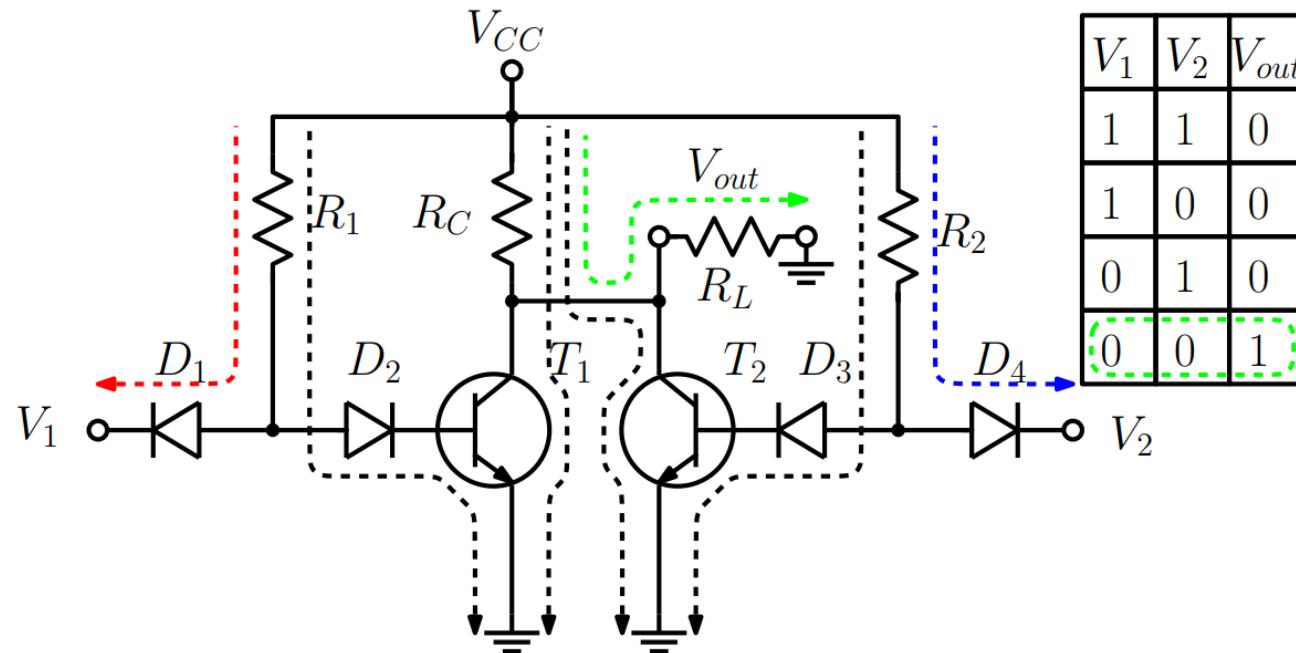
Logic Families. DTL.

ITMO

Diode-Transistor Logic (DTL) Gates.

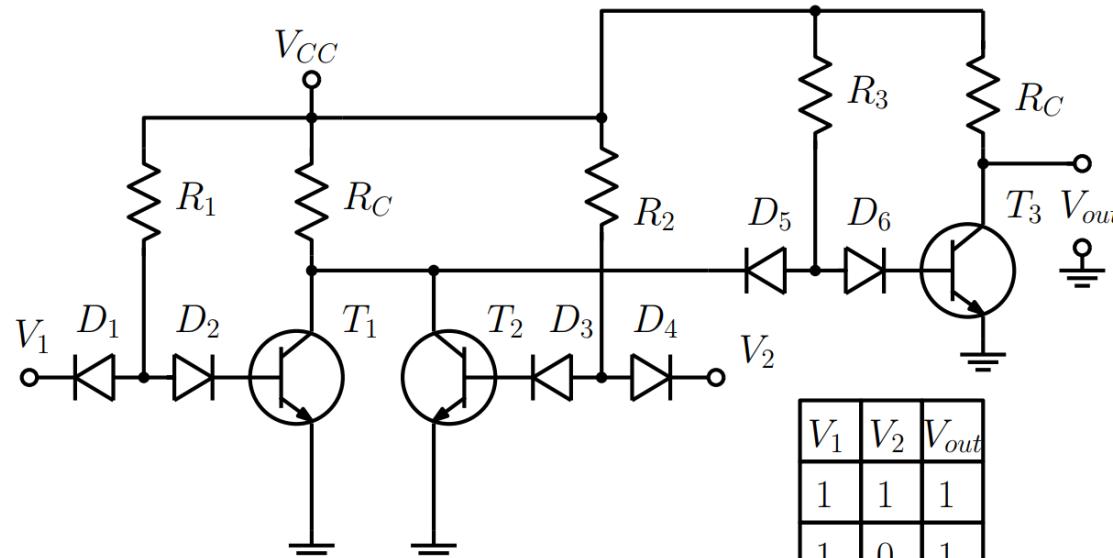
4. NOR Gate.

4.2. $V_1 = V_2 = 0$;



Diode-Transistor Logic (DTL) Gates.

5. OR Gate.



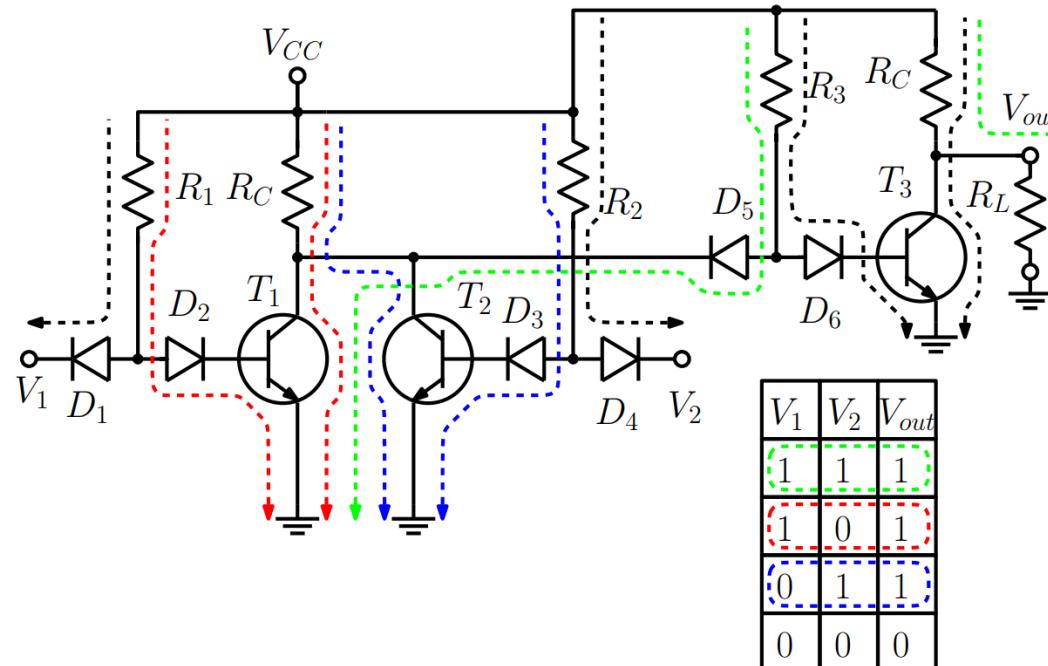
V_1	V_2	V_{out}
1	1	1
1	0	1
0	1	1
0	0	0

Logic Families. DTL.

Diode-Transistor Logic (DTL) Gates.

5. OR Gate.

5.1. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 1$;

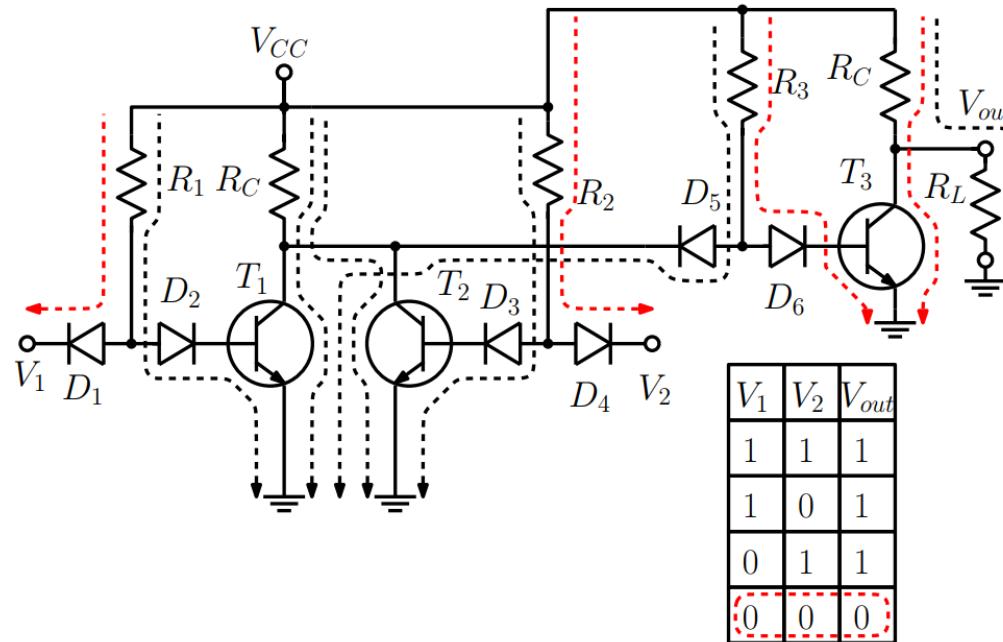


Logic Families. DTL.

Diode-Transistor Logic (DTL) Gates.

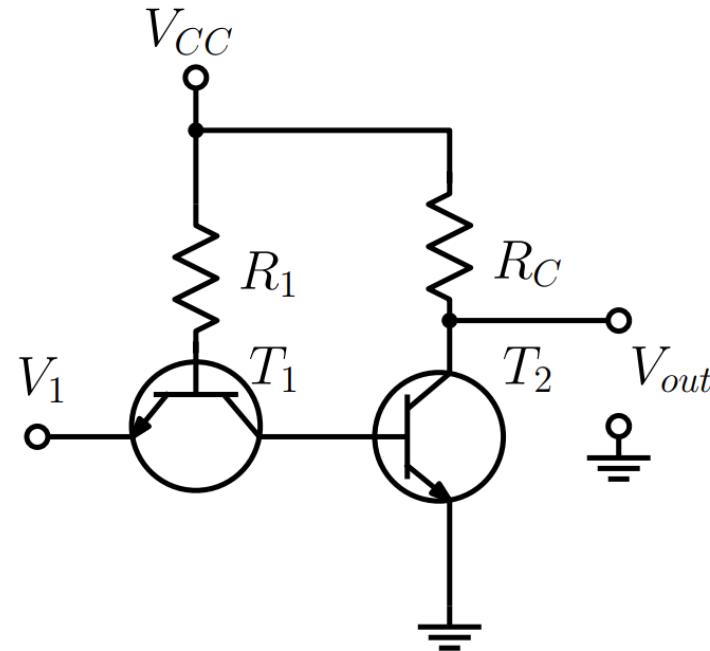
5. OR Gate.

5.2. $V_1 = V_2 = 0$;



Transistor-Transistor Logic (TTL) Gates.

1. Inverter.



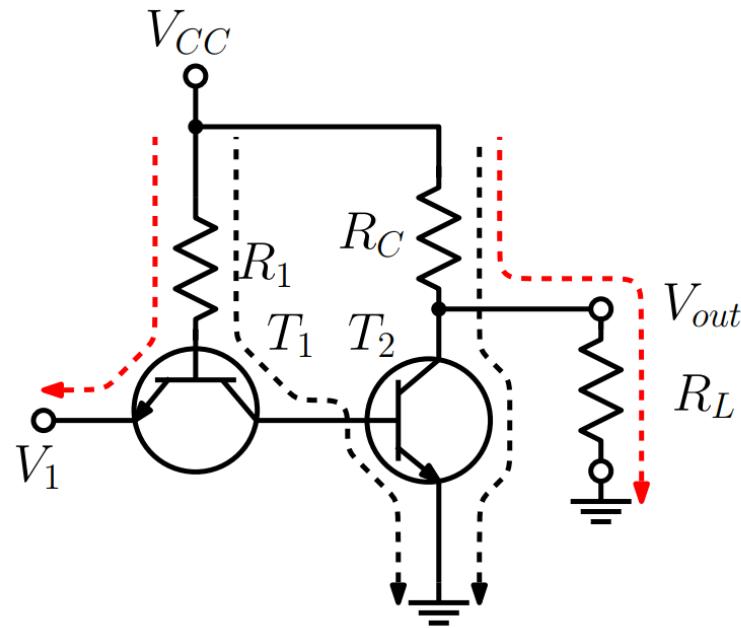
V_1	V_{out}
0	1
1	0

Logic Families. TTL.

Transistor-Transistor Logic (TTL) Gates.

1. Inverter.

1.1. $V_1 = 0$;



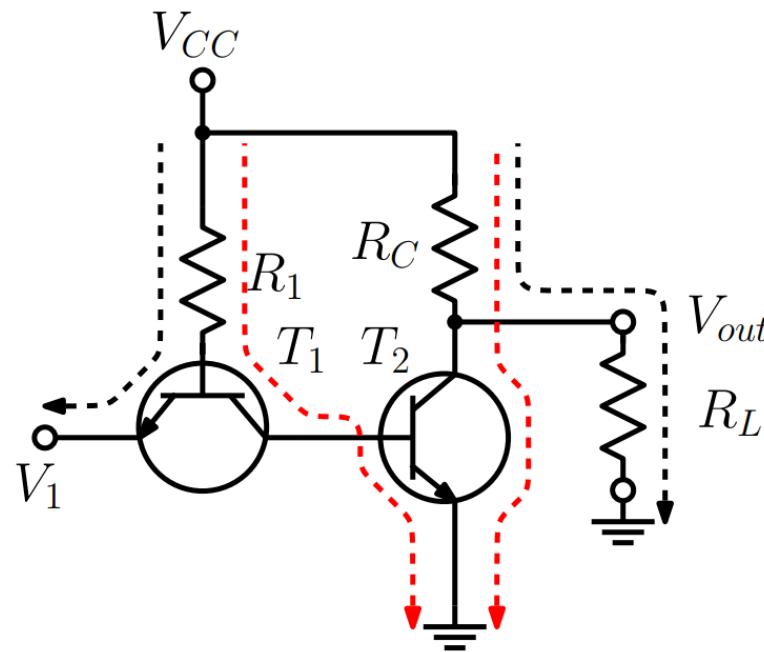
V_1	V_{out}
0	1
1	0

Logic Families. TTL.

Transistor-Transistor Logic (TTL) Gates.

1. Inverter.

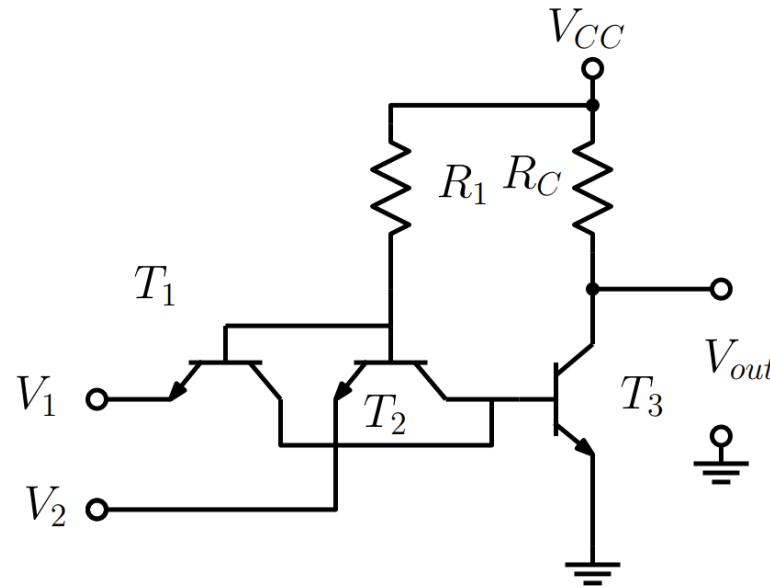
1.2. $V_1 = 1$;



V_1	V_{out}
0	1
1	0

Transistor-Transistor Logic (TTL) Gates.

2. NAND Gate.



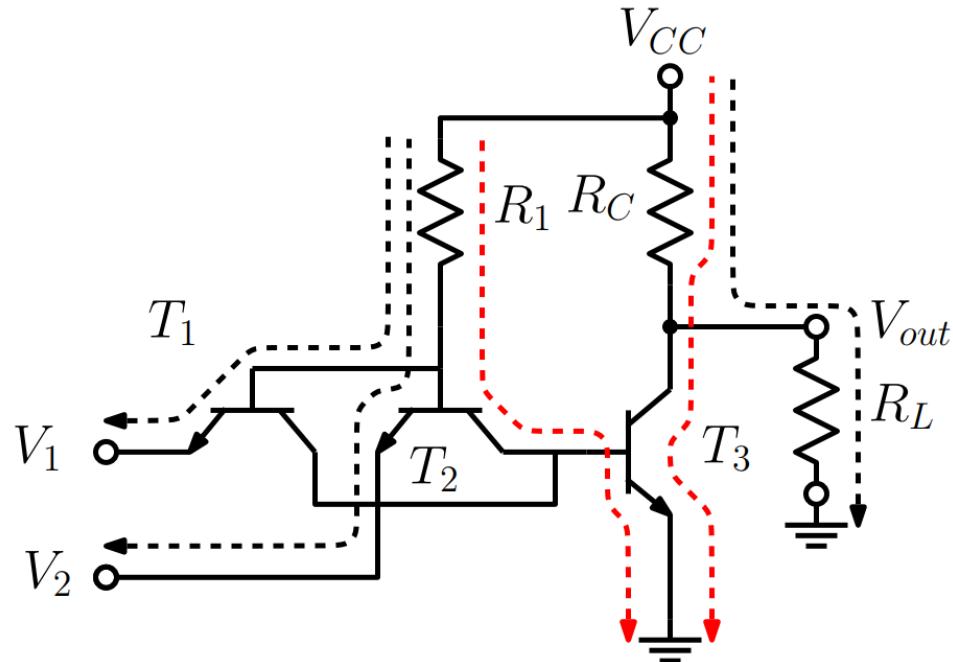
V_1	V_2	V_{out}
1	1	0
1	0	1
0	1	1
0	0	1

Logic Families. TTL.

Transistor-Transistor Logic (TTL) Gates.

2. NAND Gate.

2.1. $V_1 = V_2 = 1$;



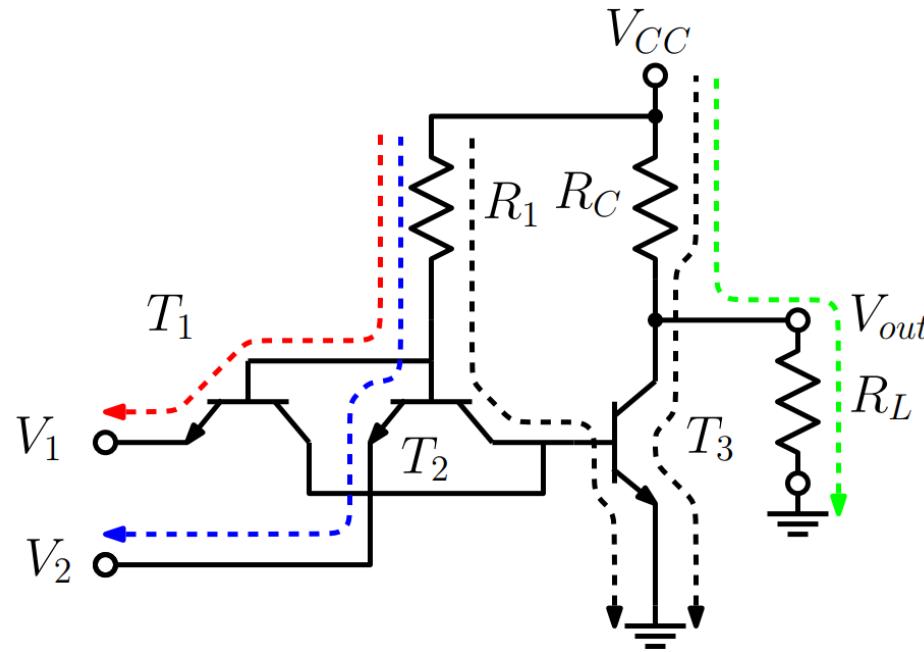
V_1	V_2	V_{out}
1	1	0
1	0	1
0	1	1
0	0	1

Logic Families. TTL.

Transistor-Transistor Logic (TTL) Gates.

2. NAND Gate.

2.2. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 0$;



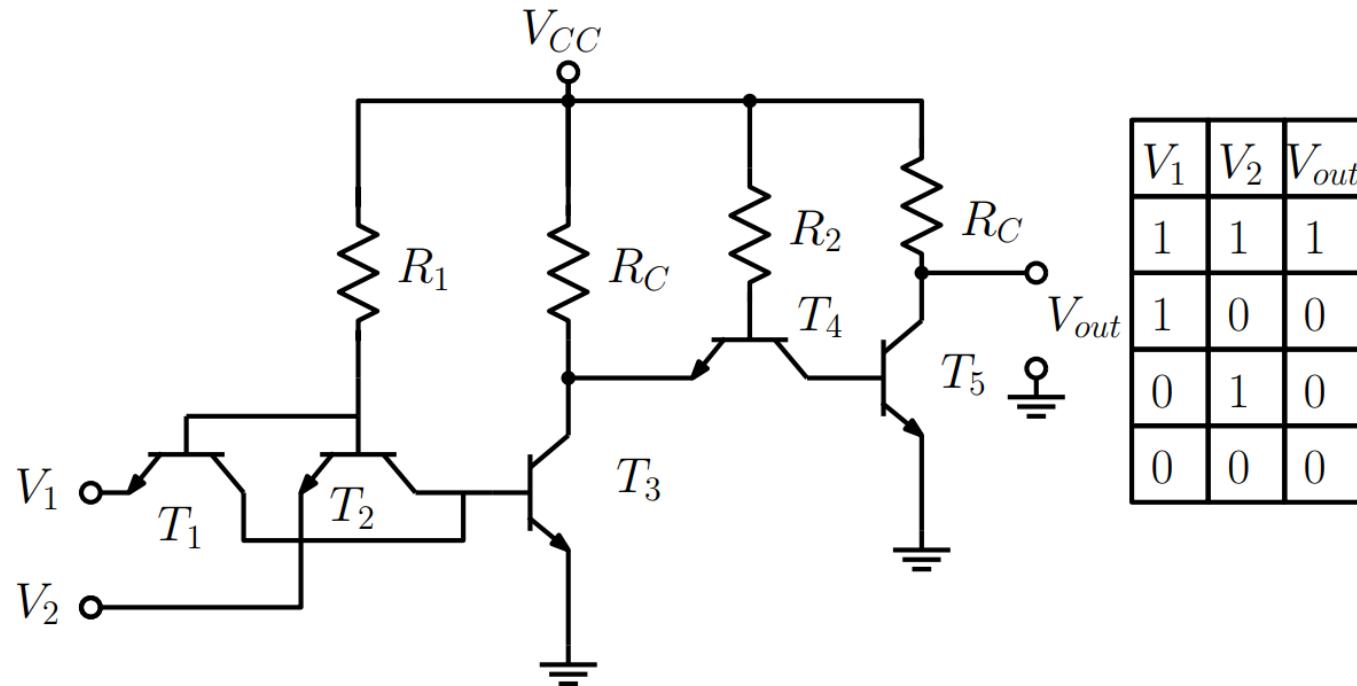
V_1	V_2	V_{out}
1	1	0
1	0	1
0	1	1
0	0	1

Logic Families. TTL.

ITMO

Transistor-Transistor Logic (TTL) Gates.

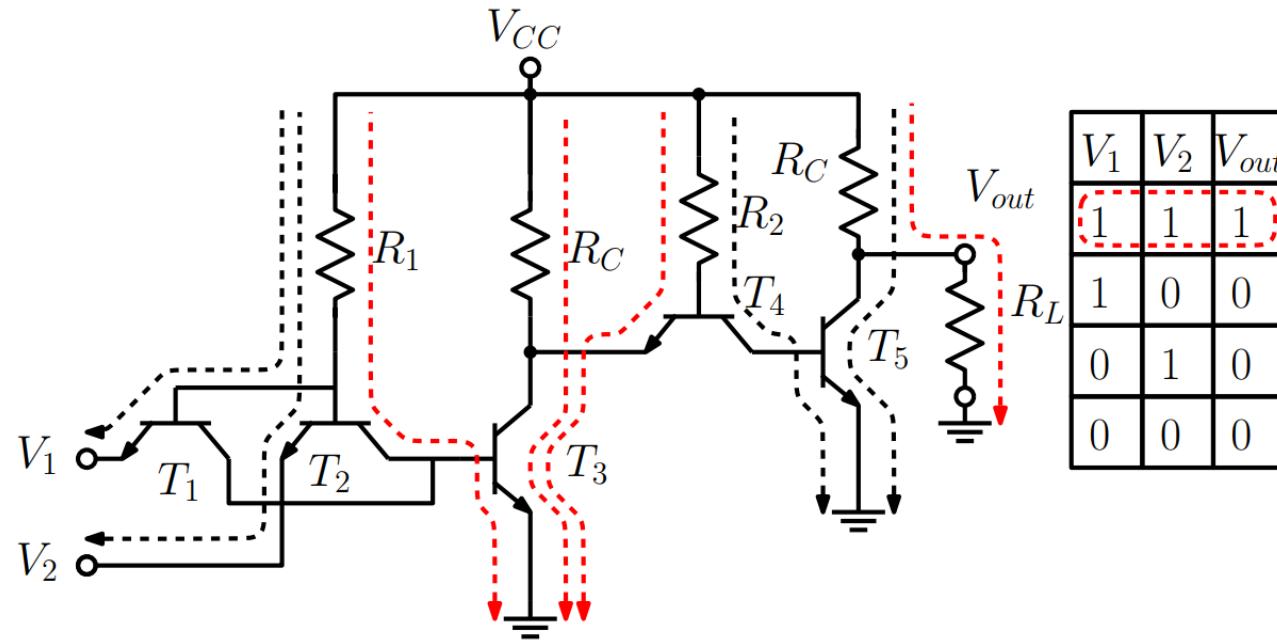
3. AND Gate.



Transistor-Transistor Logic (TTL) Gates.

3. AND Gate.

3.1. $V_1 = V_2 = 1$;

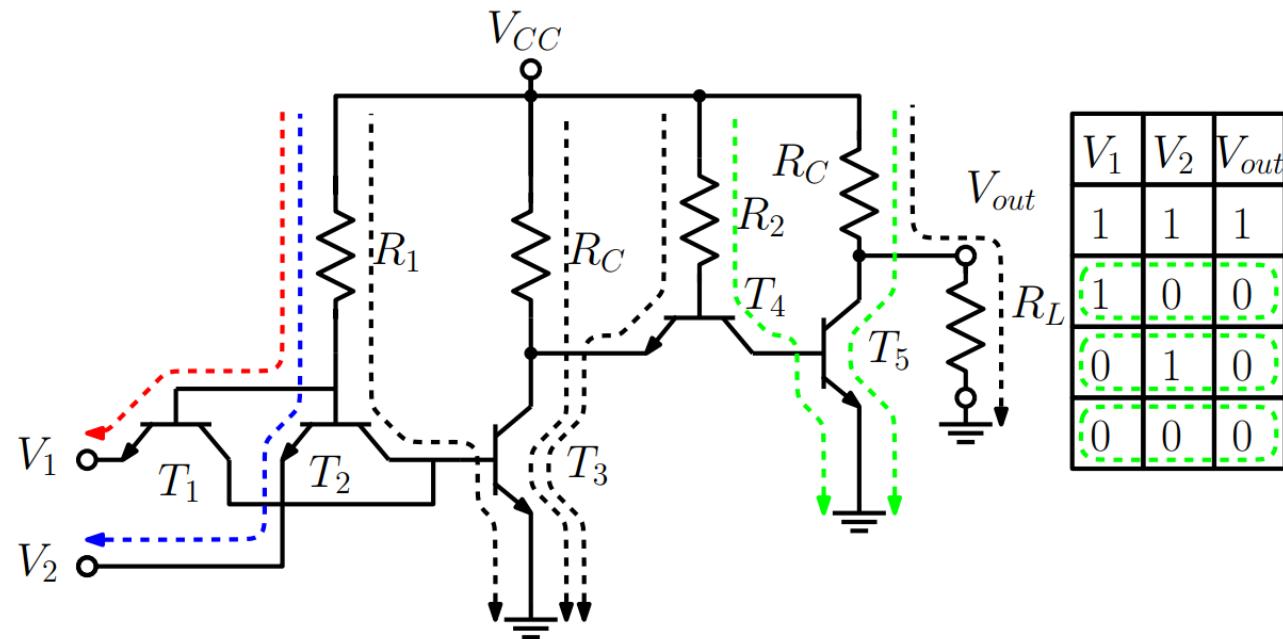


Logic Families. TTL.

Transistor-Transistor Logic (TTL) Gates.

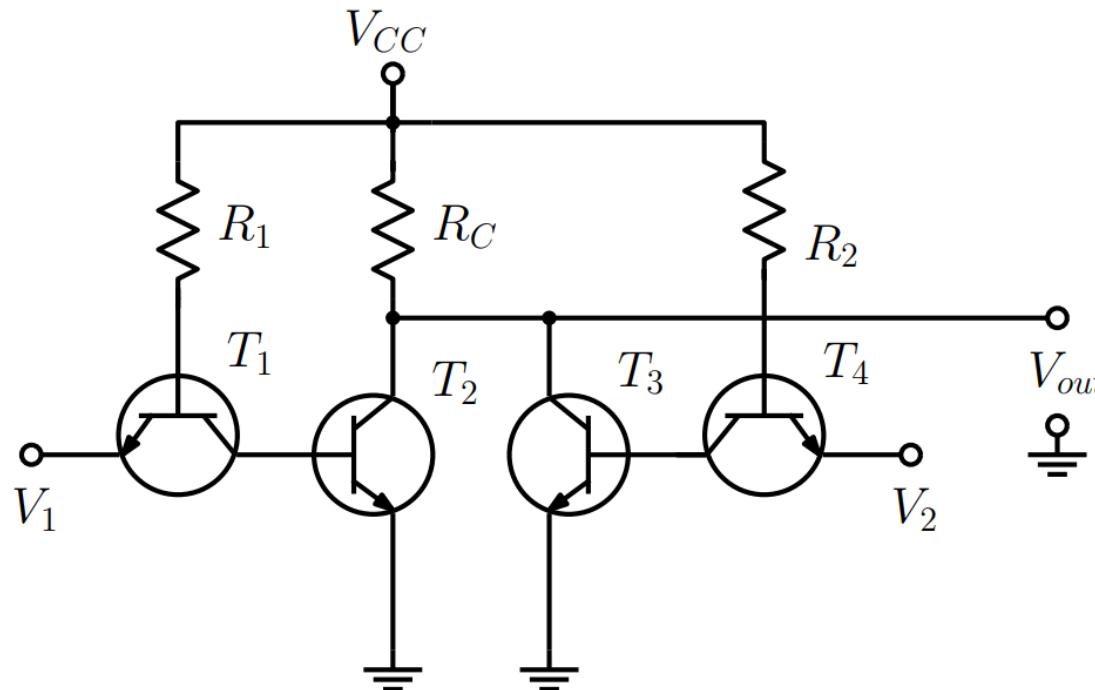
3. AND Gate.

3.2. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 0$;



Transistor-Transistor Logic (TTL) Gates.

4. NOR Gate.



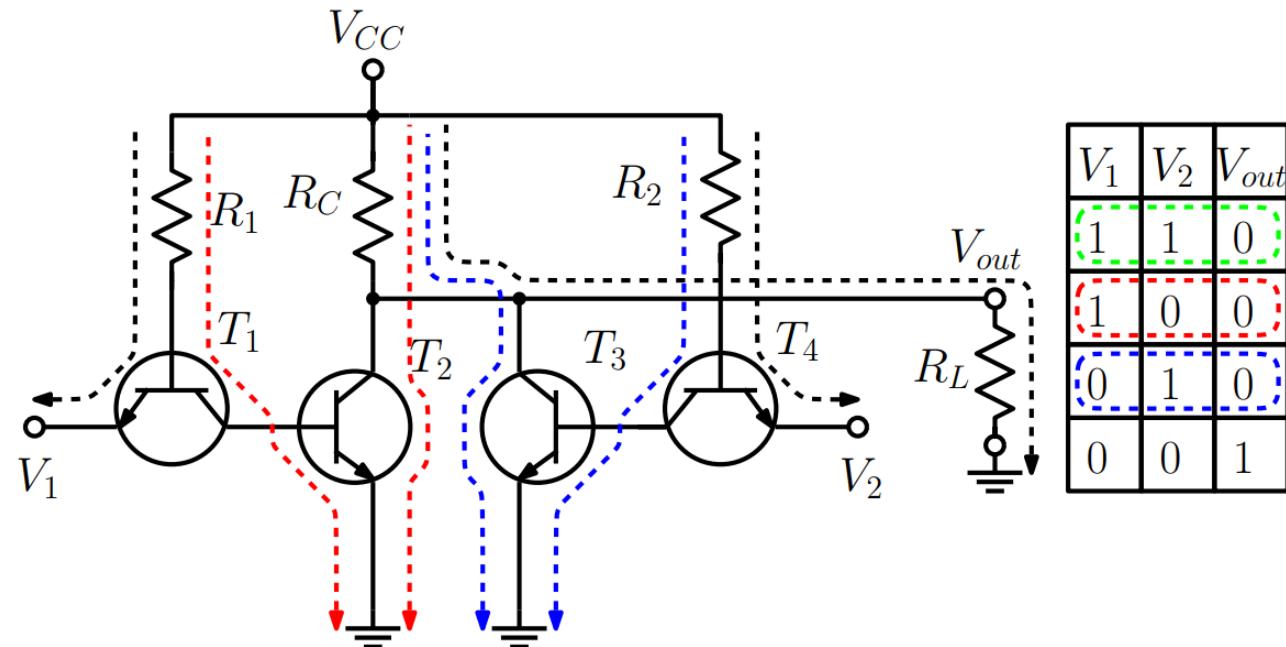
Logic Families. TTL.

ITMO

Transistor-Transistor Logic (TTL) Gates.

4. NOR Gate.

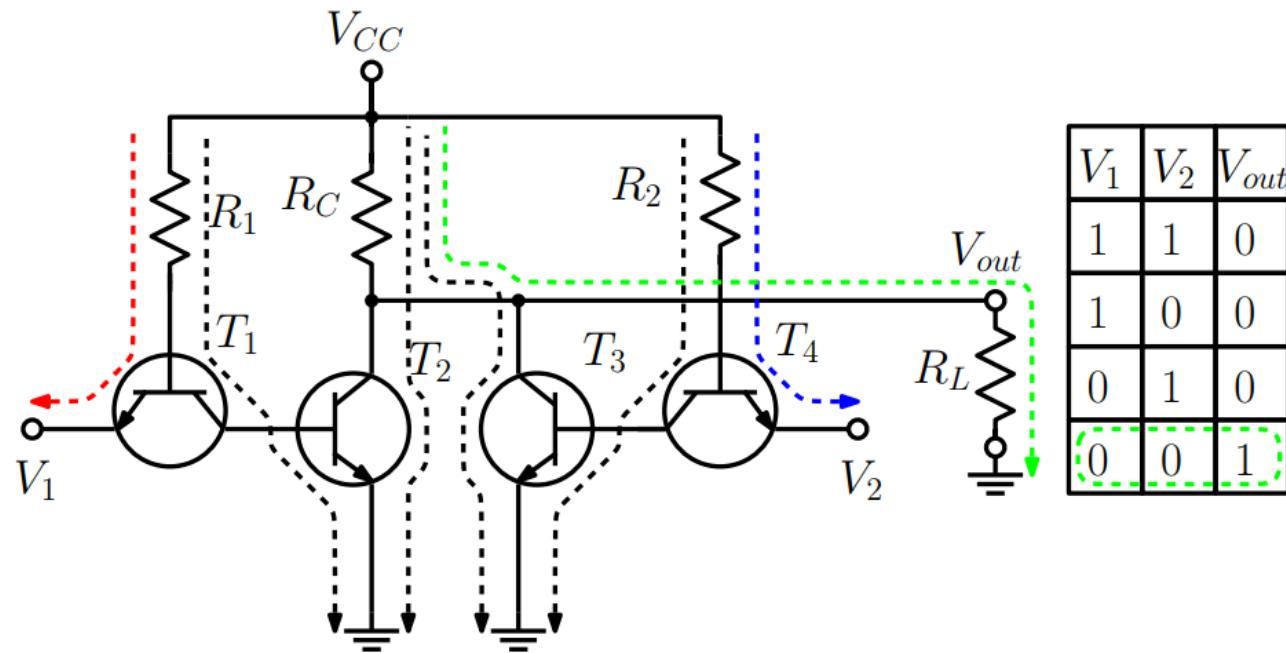
4.1. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 1$;



Transistor-Transistor Logic (TTL) Gates.

4. NOR Gate.

4.2. $V_1 = V_2 = 0$;

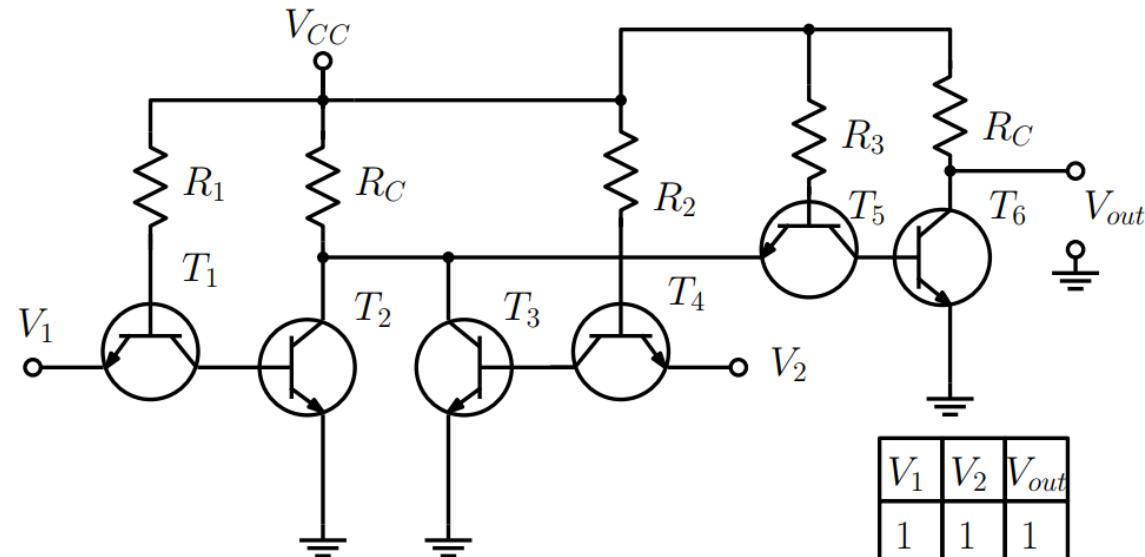


Logic Families. TTL.

ITMO

Transistor-Transistor Logic (TTL) Gates.

5. OR Gate.

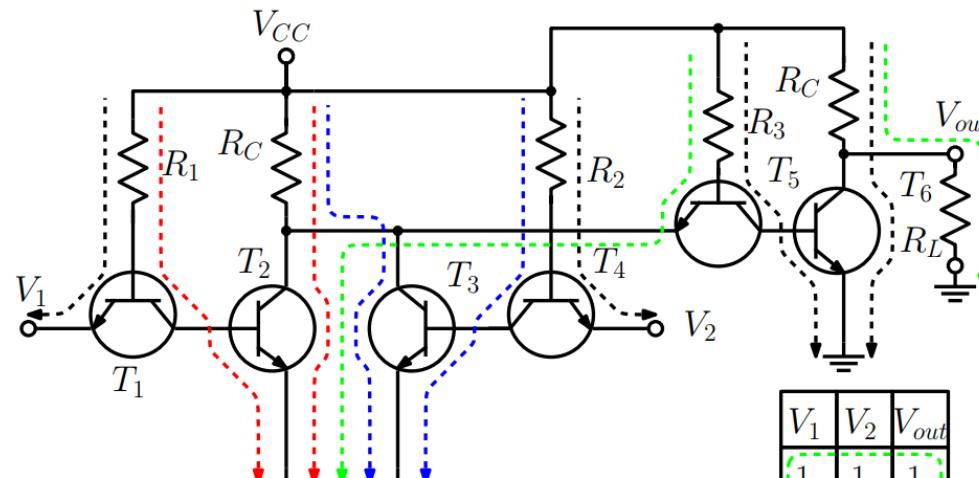


V_1	V_2	V_{out}
1	1	1
1	0	1
0	1	1
0	0	0

Transistor-Transistor Logic (TTL) Gates.

5. OR Gate.

5.1. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 1$;



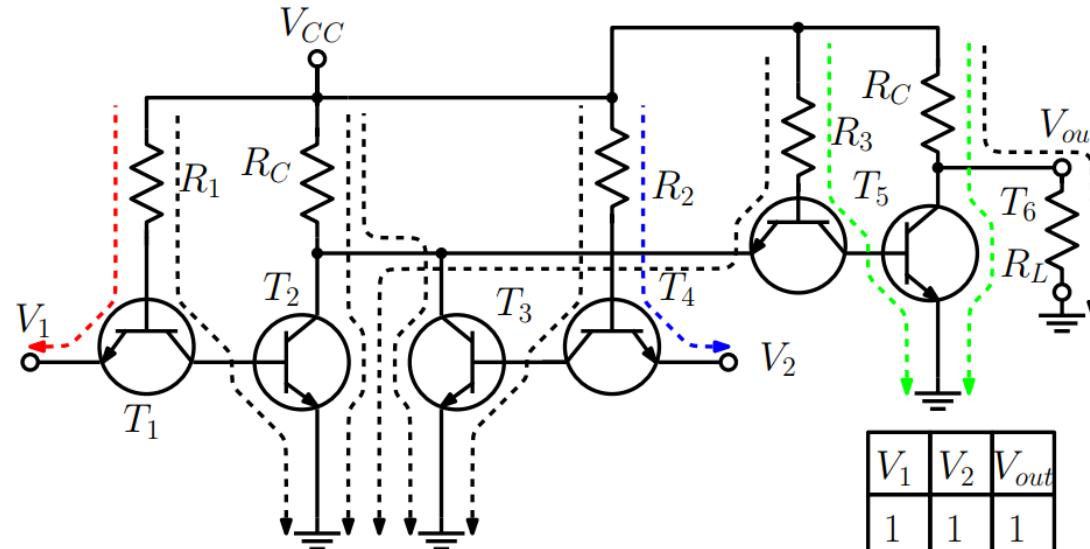
V_1	V_2	V_{out}
1	1	1
1	0	1
0	1	1
0	0	0

Logic Families. TTL.

Transistor-Transistor Logic (TTL) Gates.

5. OR Gate.

5.2. $V_1 = V_2 = 0$;

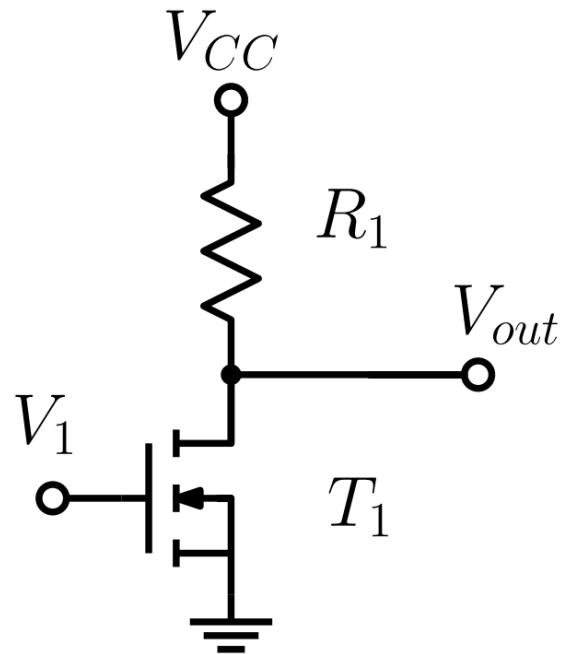


V_1	V_2	V_{out}
1	1	1
1	0	1
0	1	1
0	0	0

Logic Families. N-MOSFET.

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Gates.

1. N-MOSFET inverter.

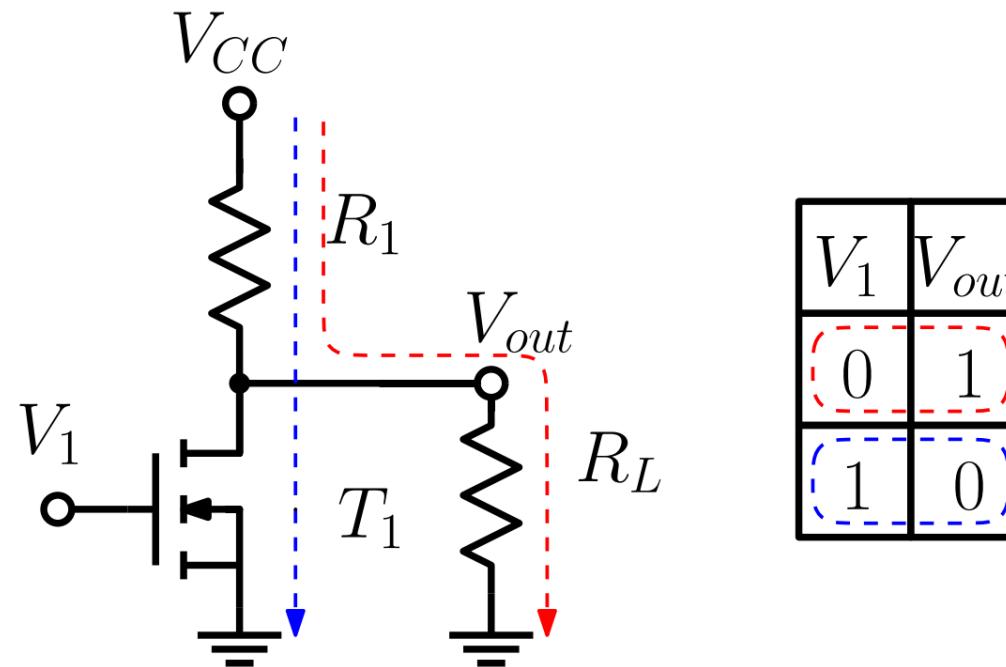


V_1	V_{out}
0	1
1	0

Logic Families. N-MOSFET.

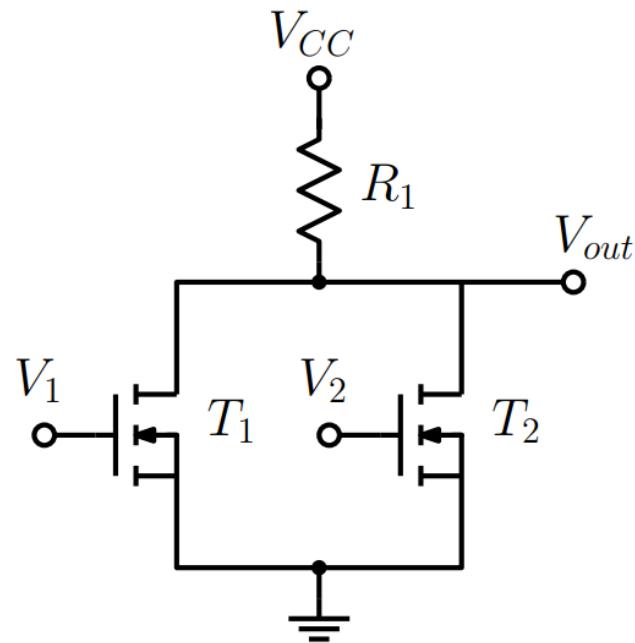
Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Gates.

1. N-MOSFET inverter.



Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Gates.

2. NOR Gate.



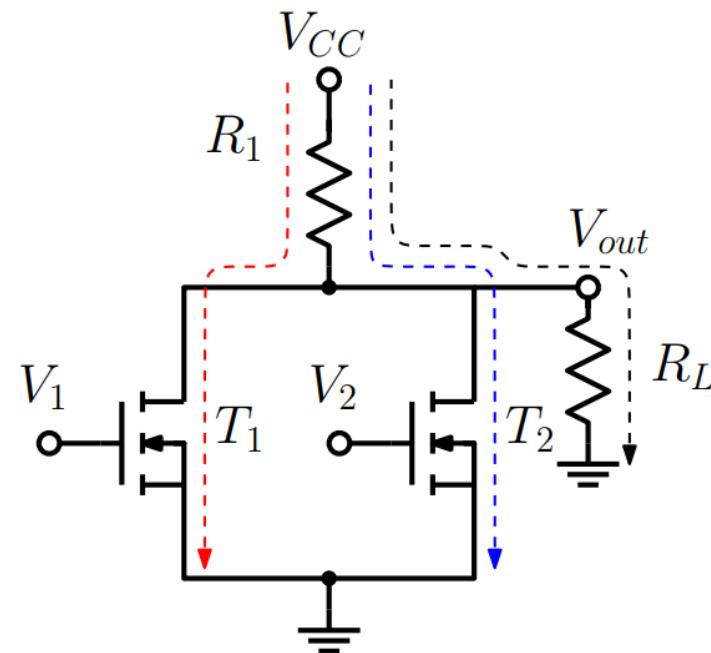
V_1	V_2	V_{out}
1	1	0
1	0	0
0	1	0
0	0	1

Logic Families. N-MOSFET.

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Gates.

2. NOR Gate.

2.1. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 1$;



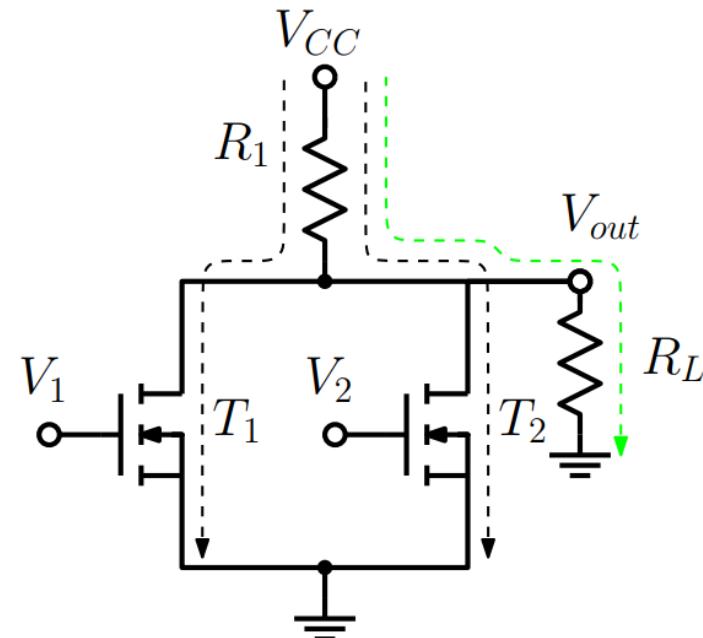
V_1	V_2	V_{out}
1	1	0
1	0	0
0	1	0
0	0	1

Logic Families. N-MOSFET.

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Gates.

2. NOR Gate.

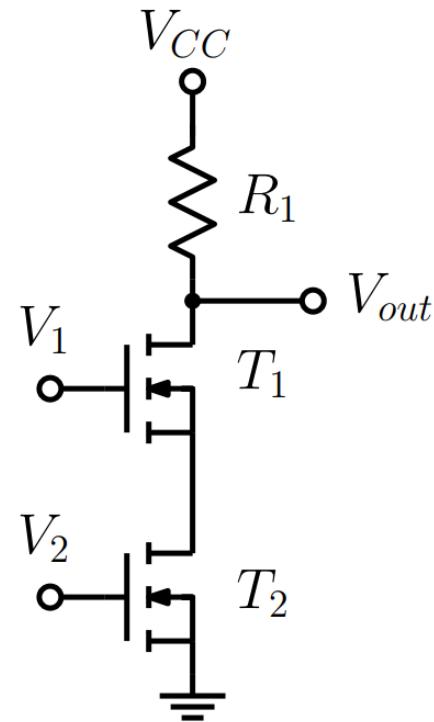
2.2. $V_1 = V_2 = 0$;



V_1	V_2	V_{out}
1	1	0
1	0	0
0	1	0
0	0	1

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Gates.

3. NAND Gate.

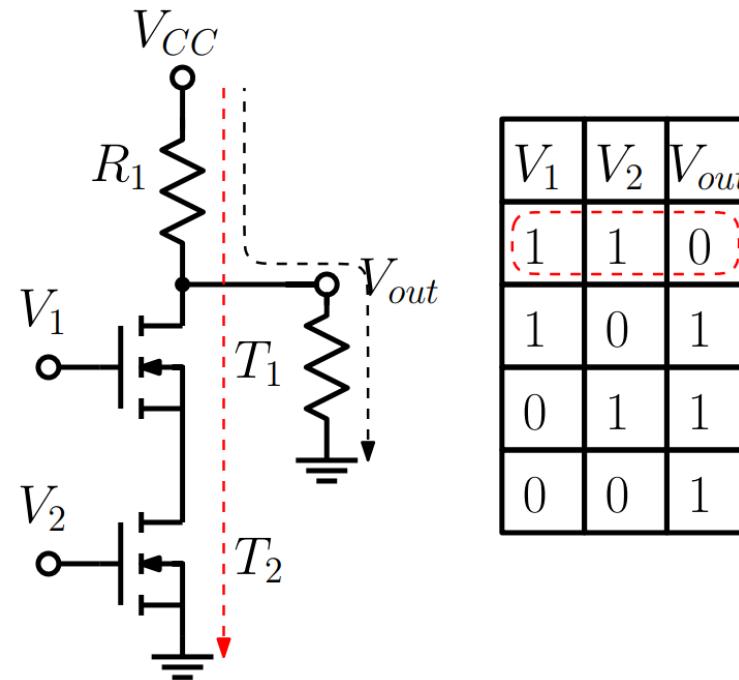


V_1	V_2	V_{out}
1	1	0
1	0	1
0	1	1
0	0	1

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Gates.

3. NAND Gate.

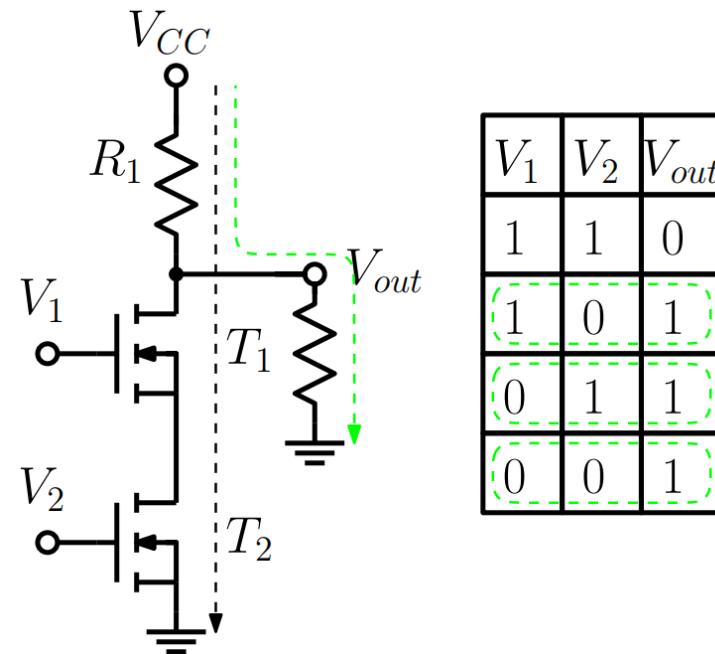
3.1. $V_1 = V_2 = 1$;



Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Gates.

3. NAND Gate.

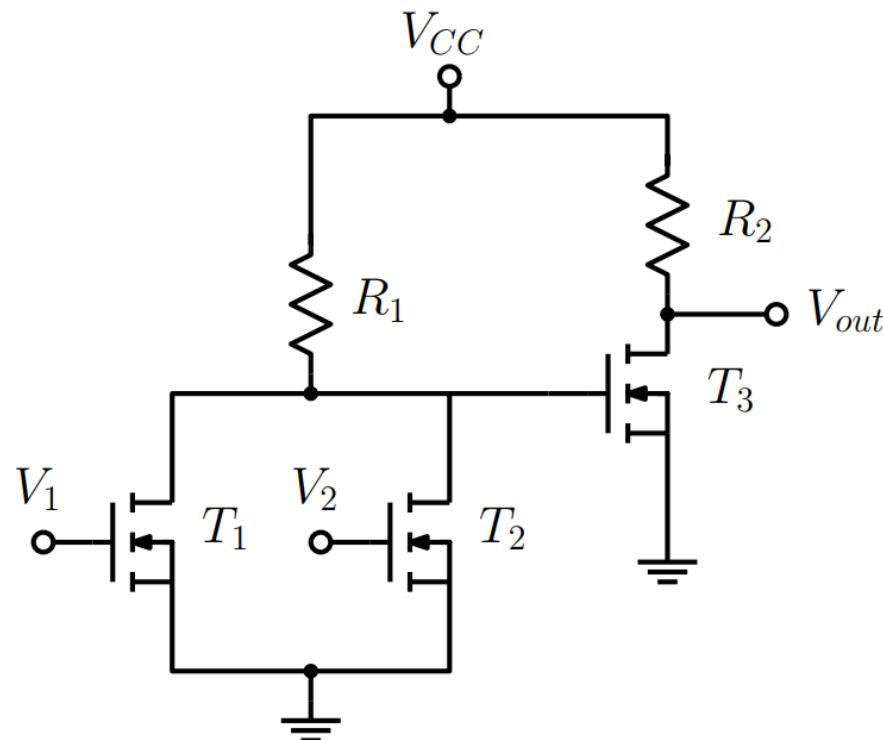
3.2. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 0$;



Logic Families. N-MOSFET.

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Gates.

4. OR Gate.



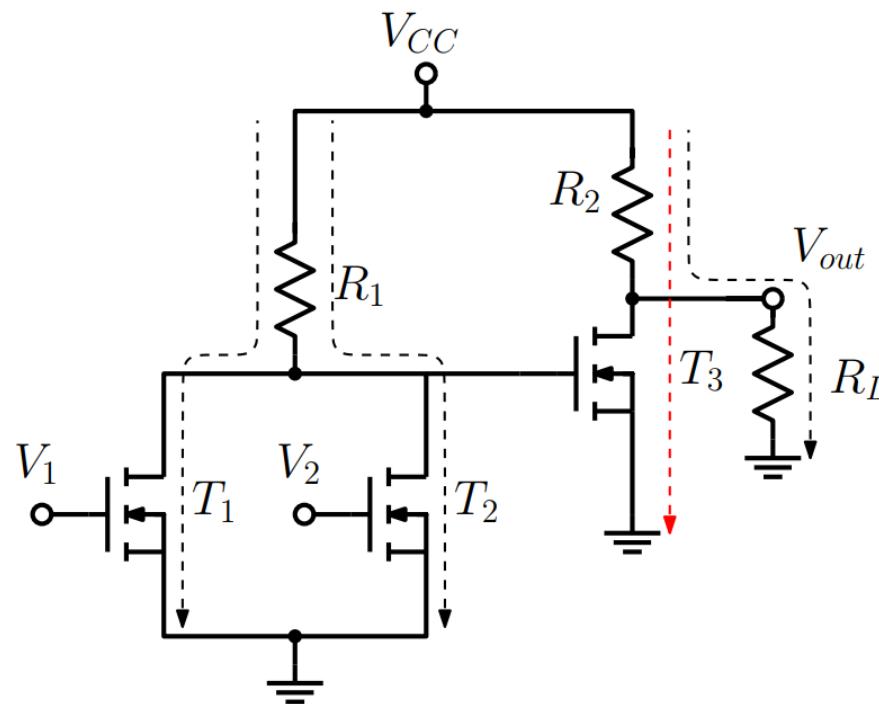
V ₁	V ₂	V _{out}
1	1	1
1	0	1
0	1	1
0	0	0

Logic Families. N-MOSFET.

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Gates.

4. OR Gate.

4.1. $V_1 = V_2 = 0$;

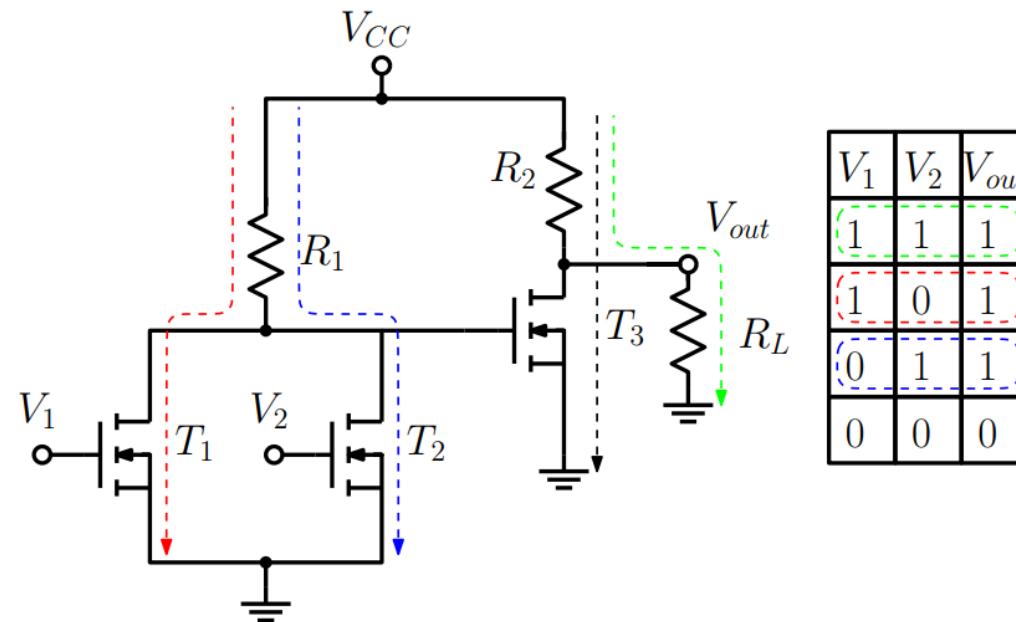


V_1	V_2	V_{out}
1	1	1
1	0	1
0	1	1
0	0	0

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Gates.

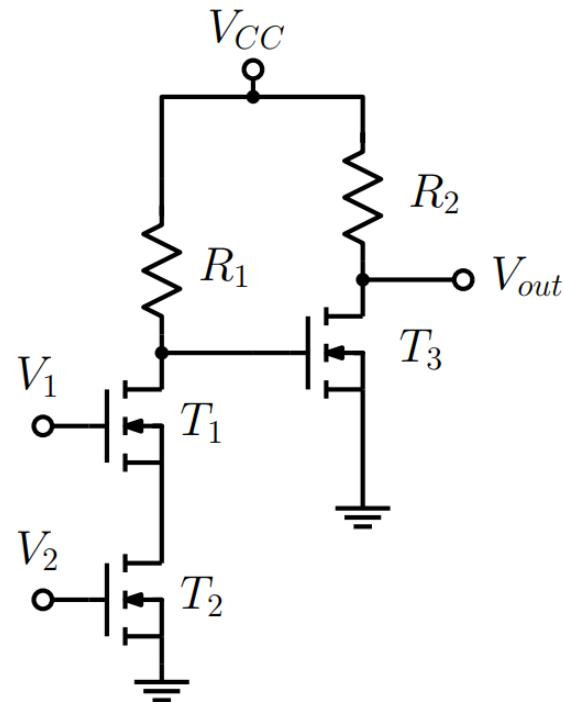
4. OR Gate.

4.2. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 1$;



Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Gates.

5. AND Gate.



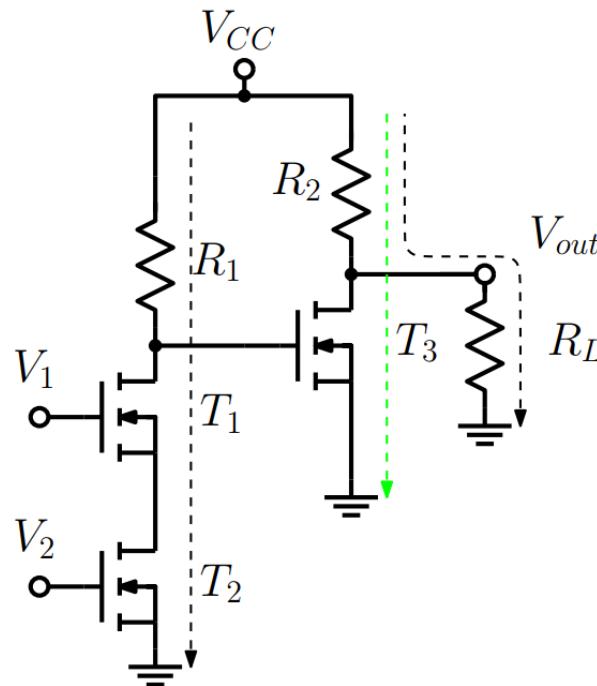
V ₁	V ₂	V _{out}
1	1	1
1	0	0
0	1	0
0	0	0

Logic Families. N-MOSFET.

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Gates.

5. AND Gate.

5.1. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 0$;

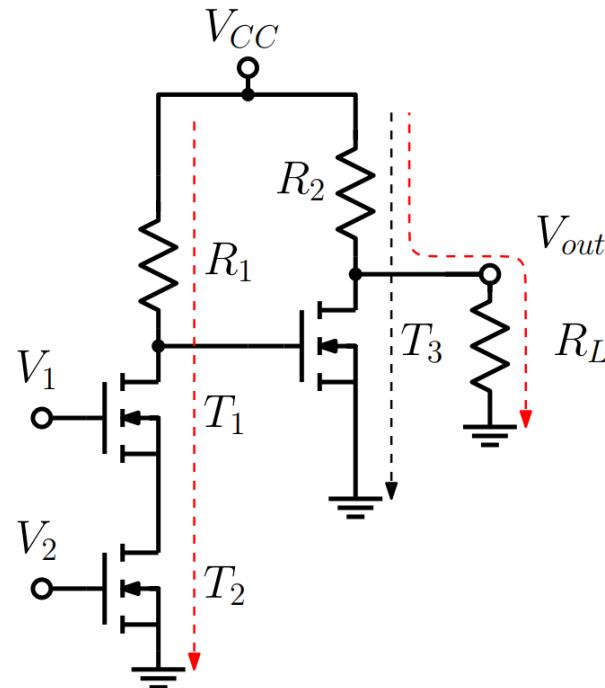


V_1	V_2	V_{out}
1	1	1
1	0	0
0	1	0
0	0	0

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Gates.

5. AND Gate.

5.2. $V_1 = V_2 = 1$;

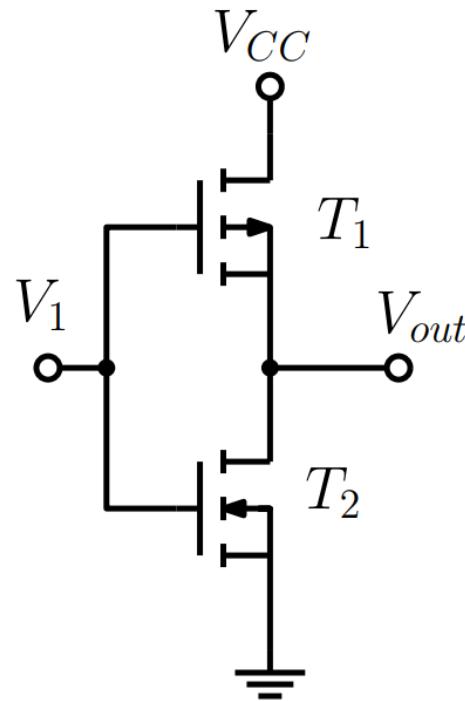


V ₁	V ₂	V _{out}
1	1	1
1	0	0
0	1	0
0	0	0

Logic Families. CMOS.

Combinational Logic Gates (CMOS).

1. CMOS inverter.

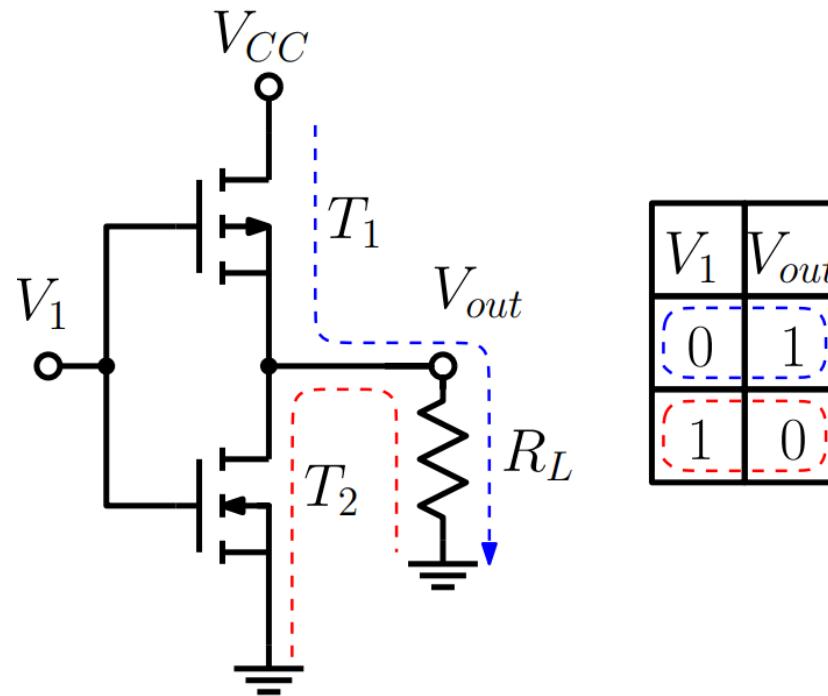


V_1	V_{out}
0	1
1	0

Logic Families. CMOS.

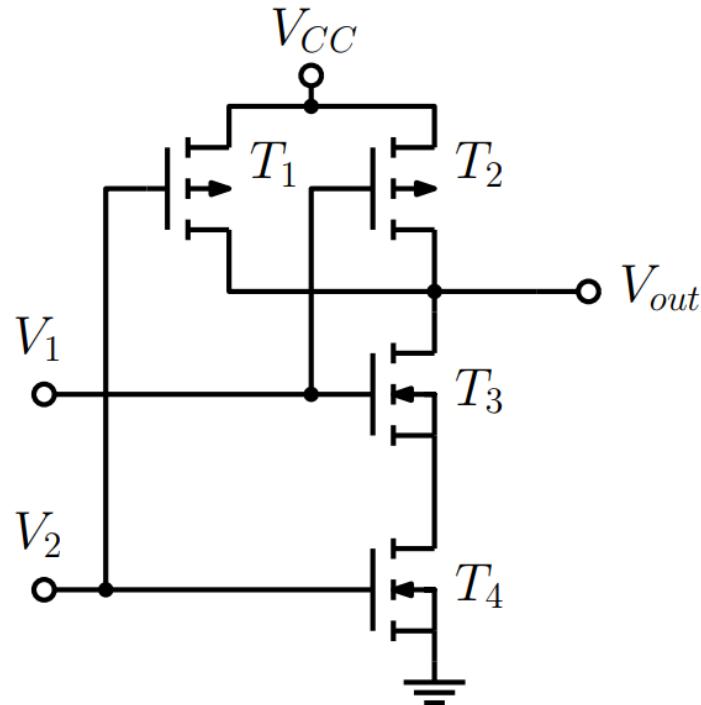
Combinational Logic Gates (CMOS).

1. CMOS inverter.



Combinational Logic Gates (CMOS).

2. NAND gate.



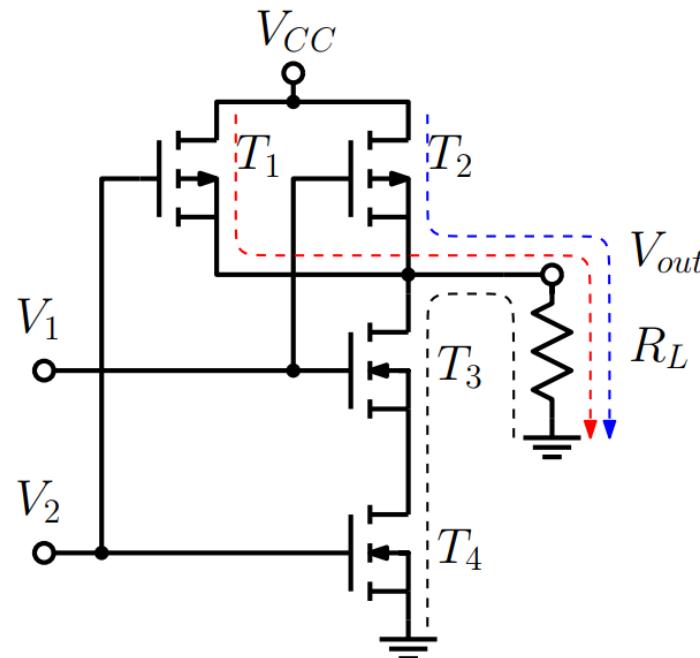
V_1	V_2	V_{out}
1	1	0
1	0	1
0	1	1
0	0	1

Logic Families. CMOS.

Combinational Logic Gates (CMOS).

2. NAND.

2.1. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 0$;

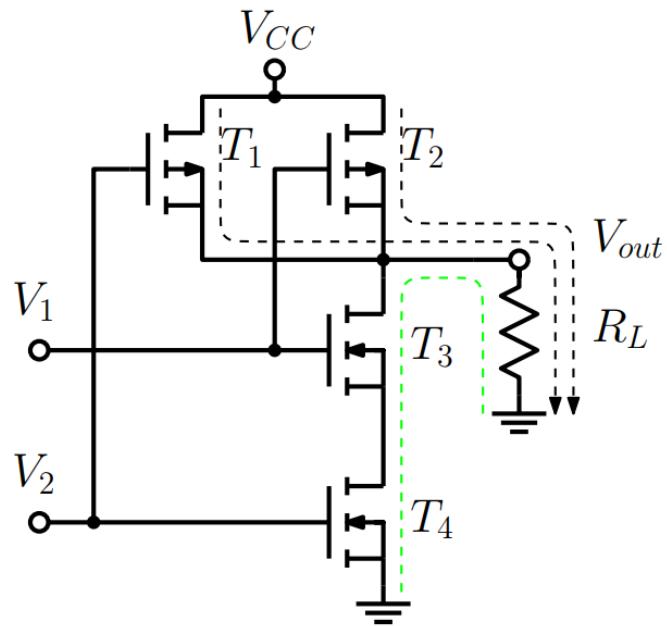


V_1	V_2	V_{out}
1	1	0
1	0	1
0	1	1
0	0	1

Combinational Logic Gates (CMOS).

2. NAND.

2.2. $V_1 = V_2 = 1$;



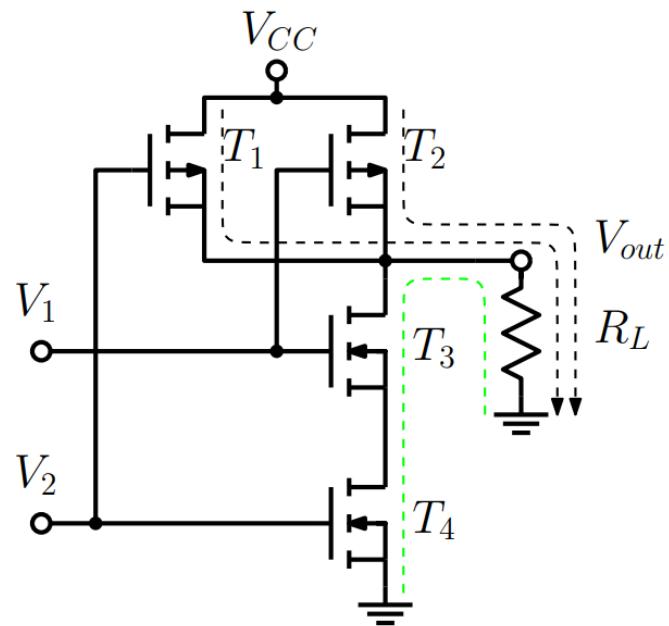
V_1	V_2	V_{out}
1	1	0
1	0	1
0	1	1
0	0	1

Logic Families. CMOS.

Combinational Logic Gates (CMOS).

2. NAND.

2.2. $V_1 = V_2 = 1$;

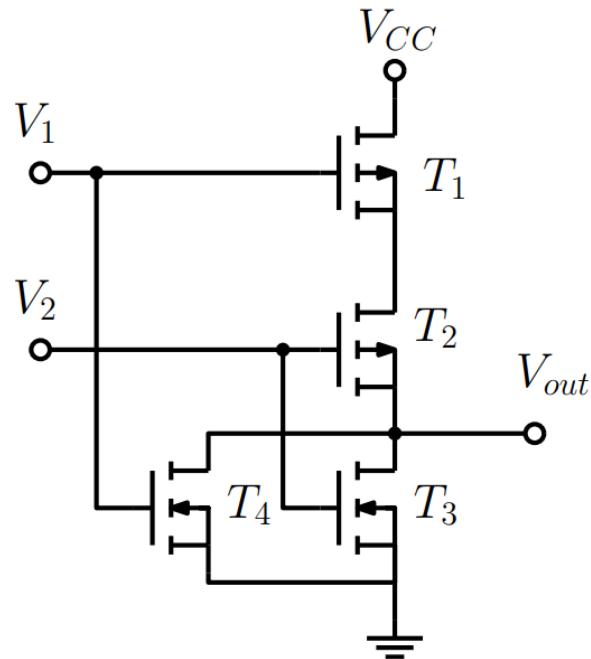


V_1	V_2	V_{out}
1	1	0
1	0	1
0	1	1
0	0	1

Logic Families. CMOS.

Combinational Logic Gates (CMOS).

3. NOR gate.

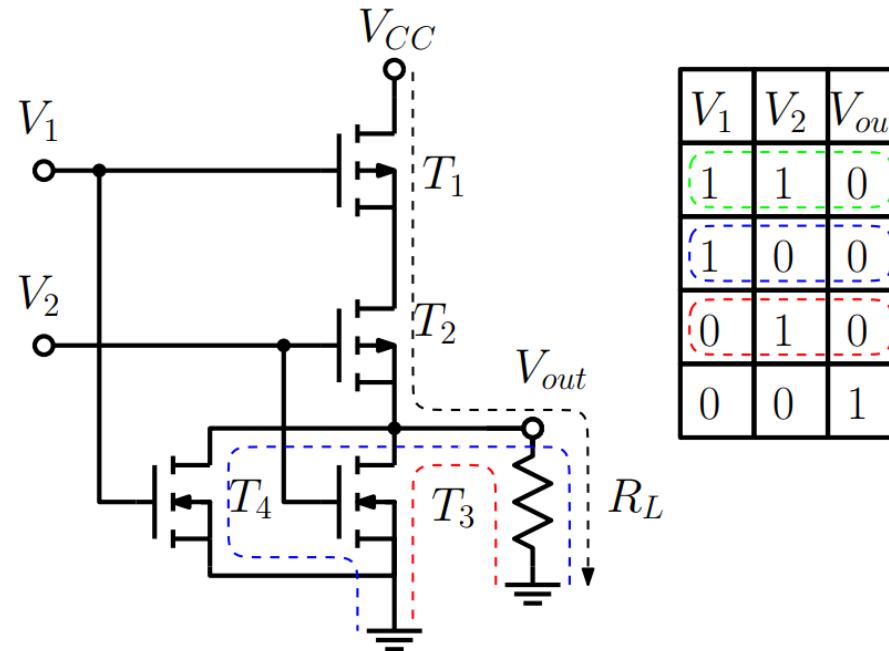


V_1	V_2	V_{out}
1	1	0
1	0	0
0	1	0
0	0	1

Combinational Logic Gates (CMOS).

3. NOR.

3.1. $V_1 = 1$ and $V_2 = 0$; $V_1 = 0$ and $V_2 = 1$ or $V_1 = V_2 = 1$;

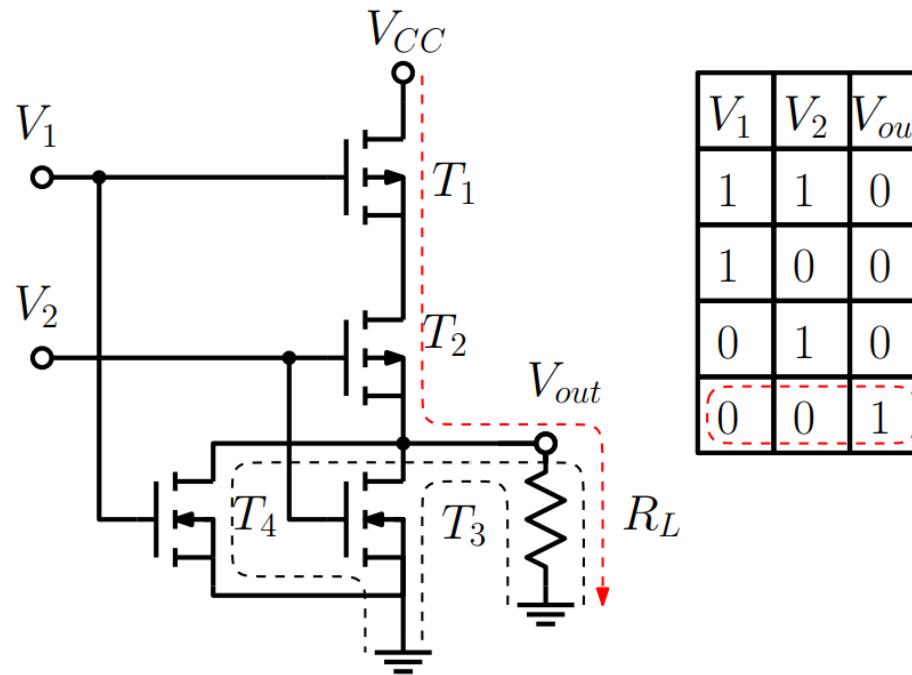


Logic Families. CMOS.

Combinational Logic Gates (CMOS).

3. NOR.

3.2. $V_1 = V_2 = 0$;



References

1. Sarma M. S. Introduction to electrical engineering. – New York : Oxford University Press, 2001. – C. 715-716.
2. Tokheim R. L. Digital Electronics: Principles and Applications, 8th Edition. – McGraw-Hill, Inc., 2014.
3. Kleitz W. Digital Electronics: A practical approach with VHDL. – Prentice Hall, 2011.
4. Harris S., Harris D. Digital design and computer architecture: arm edition. – Morgan Kaufmann, 2015.
5. Paul Scherz, Simon Monk. Practical Electronics for Inventors, Fourth Edition. - McGraw-Hill, Inc., 2016.

iTMO

Thank you for your attention!