Laboratory work №4
Simple digital circuits design and simulation

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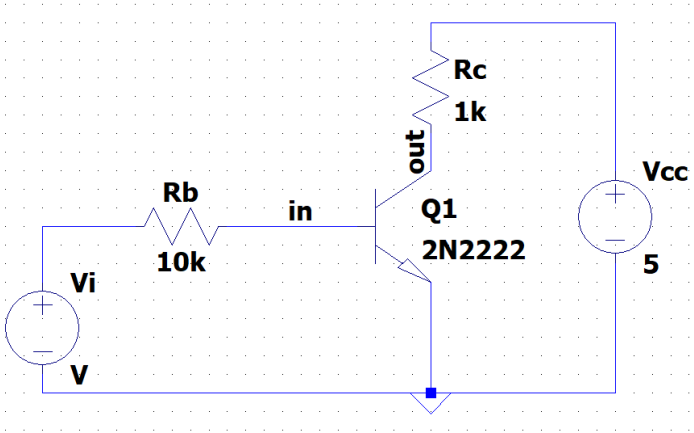
1. A typical inverter circuit using a bipolar transistor.

A typical inverter circuit using a bipolar transistor is shown in Figure 1.



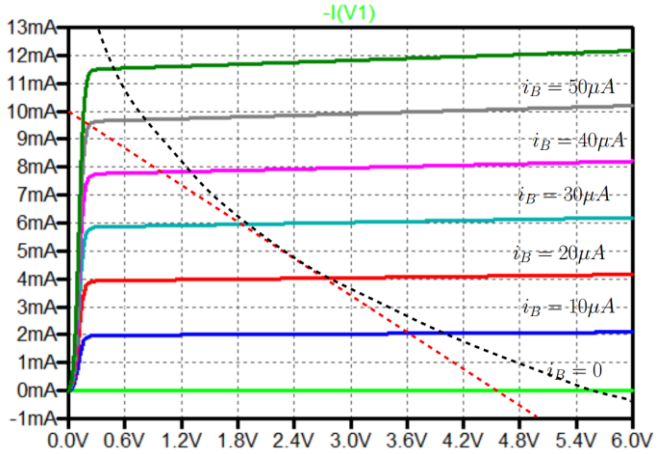
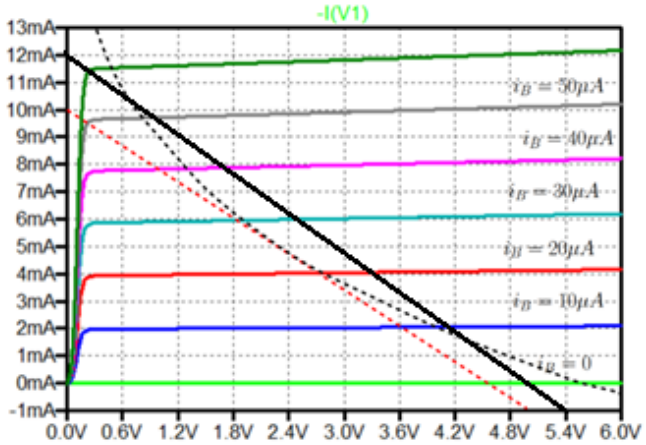
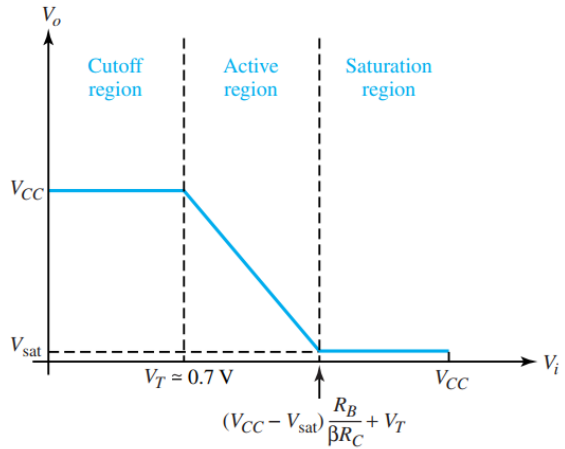
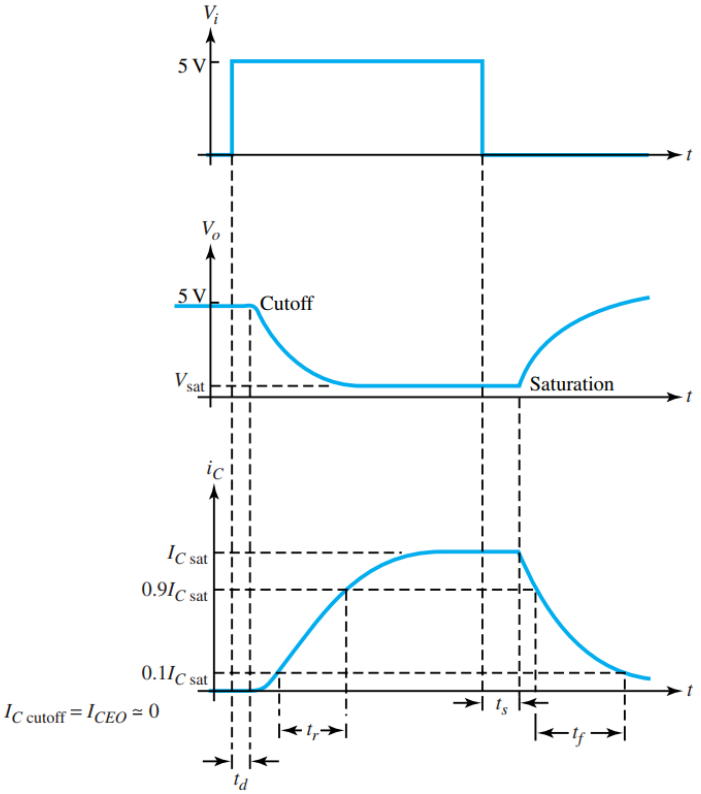


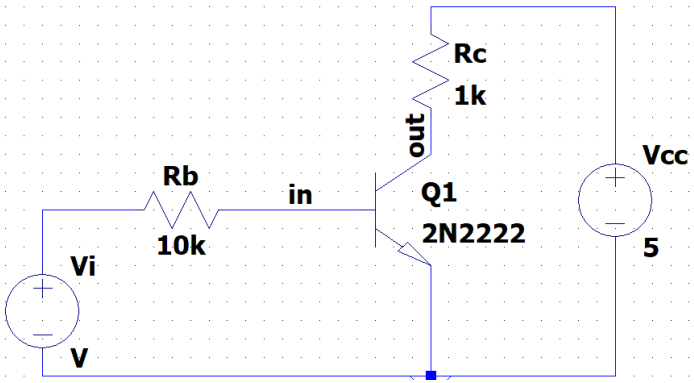
Figure 1 - A typical inverter circuit and volt-ampere characteristic

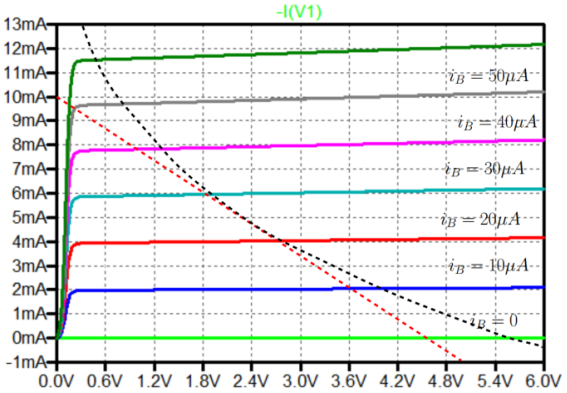

-I(V1)
13mA
12mA
11mA
10mA
9mA
8mA
7mA
6mA
5mA
4mA
3mA
2mA
1mA
0mA
-1mA
0.0V 0.6V 1.2V 1.8V 2.4V 3.0V 3.6V 4.2V 4.8V 5.4V 6.0V
$i_B = 50\mu A$
$i_B = 40\mu A$
$i_B = 30\mu A$
$i_B = 20\mu A$
$i_B = 10\mu A$
$i_B = 0$


V_o
Cutoff region
Active region
Saturation region
V_{CC}
V_{sat}
$V_T \simeq 0.7$ V
V_{CC}
V_i
$(V_{CC} - V_{sat})\dfrac{R_B}{\beta R_C} + V_T$


V_i
5 V
t
V_o
5 V
Cutoff
V_{sat}
Saturation
t
i_C
$I_{C\,sat}$
$0.9I_{C\,sat}$
$0.1I_{C\,sat}$
t
$I_{C\,cutoff} = I_{CEO} \simeq 0$
t_s
t_r
t_f
t_d

Transistor switch mode





Consider main relationships for transistor switch.

For output load line drawing we need to consider Kirchhoff's voltage law for output circuit

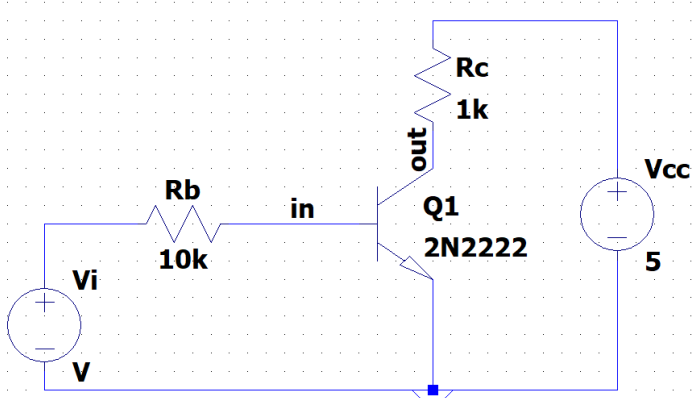
$$V_{CE} = V_{CC} - R_C i_C$$

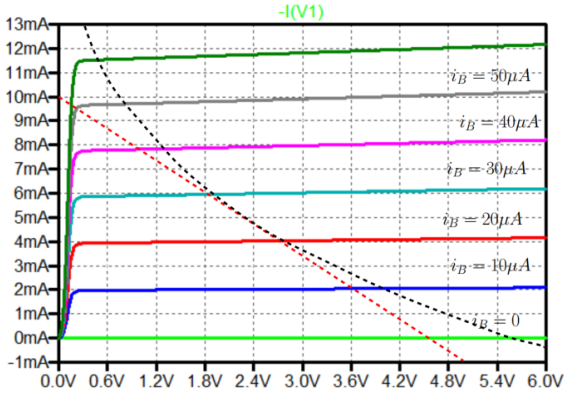
For input load line drawing we need to consider Kirchhoff's voltage law for input circuit

$$V_{BE} = V_i - R_B i_B$$

Consider levels of analog input signals – as logic "0" we consider signal over 0 V and as logic "1" we consider signal over 5 V.

Transistor switch mode





For logic 0 the base current is zero. Transistor is said to be cut off (off), only a very small value of collector current flows. In cut off state for output voltage we have logical 1 level

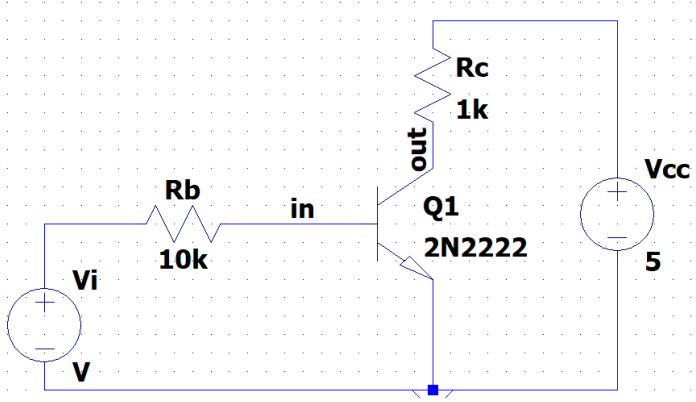
$$V_{out} = V_{CE_{cut\,off}} \cong V_{CC} - R_C i_{CE0} \cong V_{CC} = 5\,V.$$

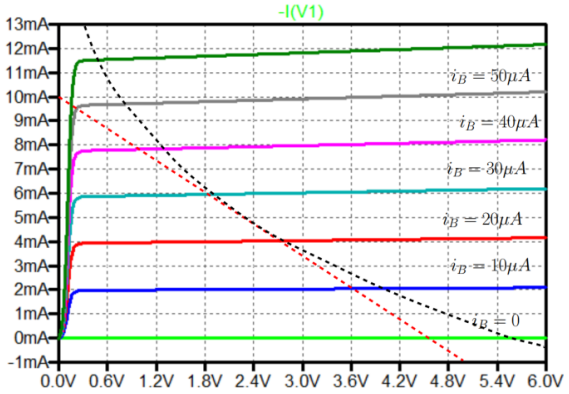
For logic 1 the base current is not zero

$$I_{B_{sat}} = \frac{V_i - V_{BE}}{R_B}$$

where $V_{BE} \cong 0.7\,V$ which is the threshold voltage. R_B is chosen to drive the transistor into saturation.

Transistor switch mode





In the saturated state $V_{CE_{sat}} = 0.2 \ldots 0.3\ V$ (this is typically value).

$$I_{C_{sat}} = \frac{V_{CC} - V_{CE_{sat}}}{R_C} \cong \frac{V_{CC}}{R_C}.$$

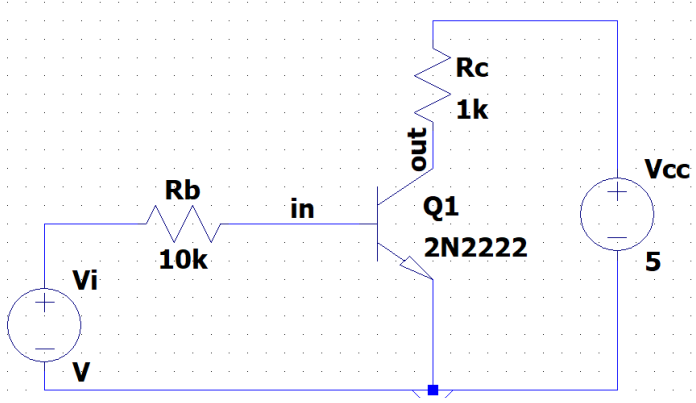
It can be shown that saturation will occur when

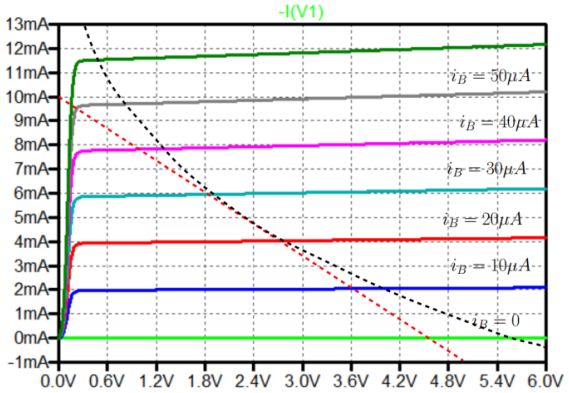
$$\frac{V_i - V_{BE}}{R_B} > \frac{V_{CC} - V_{CE_{sat}}}{\beta R_C}.$$

Since $i_C \cong \beta i_B + I_{CE0}$, then for saturated state we need $i_{B_{sat}} > {}^{i_{C_{sat}}}/_{\beta}$, such as

$$I_{C_{sat}} = \frac{V_{CC} - V_{CE_{sat}}}{R_C}$$

Transistor switch mode





then

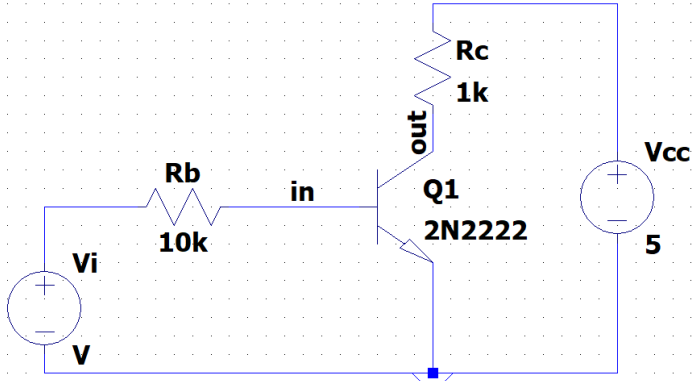
$$I_{B_{sat}} = \frac{V_{CC} - V_{CE_{sat}}}{\beta R_C}$$

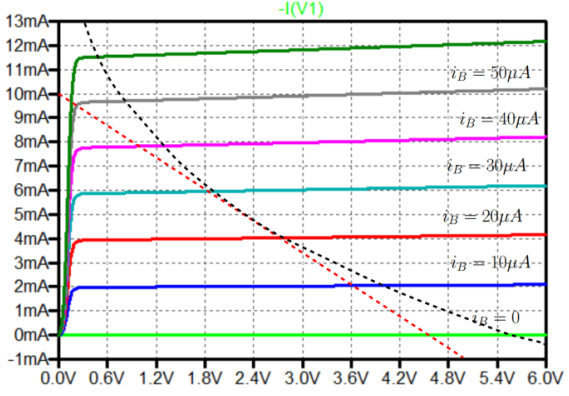
We choose current value as

$$i_B = k\frac{V_{CC} - V_{CE_{sat}}}{\beta R_C}$$

where k is a coefficient of desired overdrive (usually $k = 2 \ldots 3$).

Transistor switch mode





For example, we consider transistor 2N2222.

We need to choose current value I_C it must be not more than maximum value of transistor current $I_{C_{max}}$ (for 2N2222 $I_{C_{max}} = 0.6\ A$, see table from datasheet).

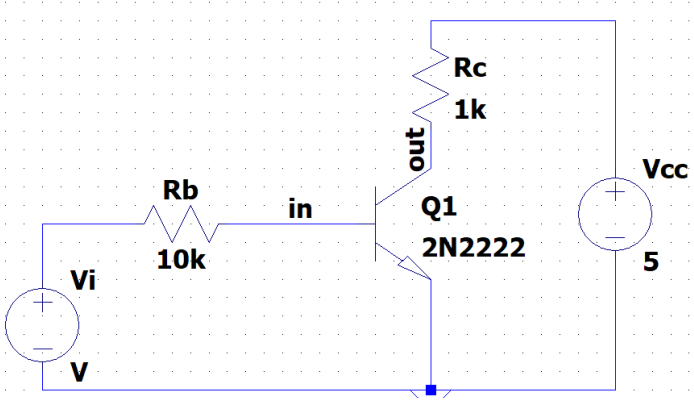
We choose $I_C = 10\ mA$. Then for R_C we have

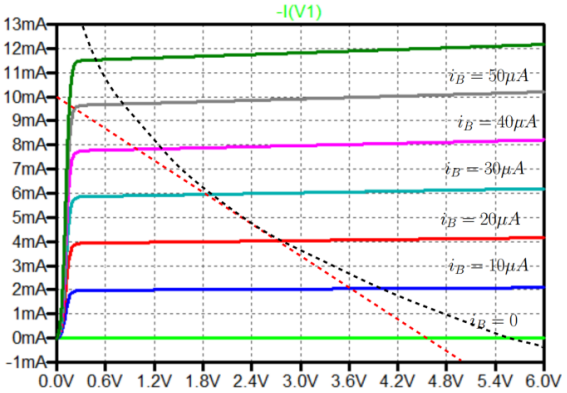
$$R_C = \frac{V_{CC} - V_{CE_{sat}}}{I_C} \cong \frac{V_{CC}}{I_C} = \frac{5}{0.01} = 500\ \Omega.$$

Now we can plot load line on the output volt–ampere characteristic (VAC) and maximum collector dissipation line.

Collector Current	I_C	600	mA
Power Dissipation	P_{tot}	625	mW

Transistor switch mode





Chose value of i_B

$$i_B = k\frac{V_{CC} - V_{CE_{sat}}}{\beta R_C} \cong k\frac{V_{CC}}{\beta R_C}$$

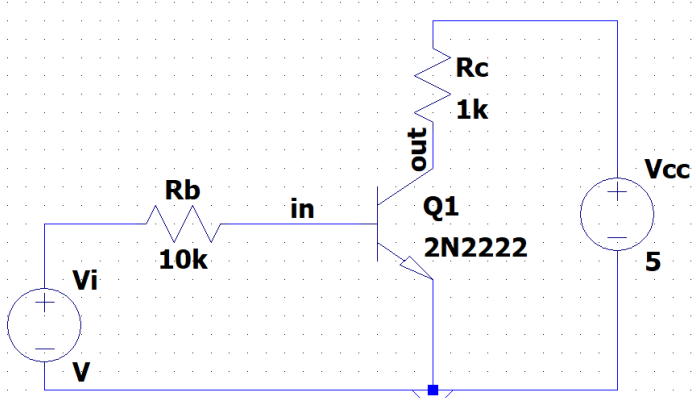
For $k = 3$ and $\beta = 100$ (we found this value in transistor datasheet) we have

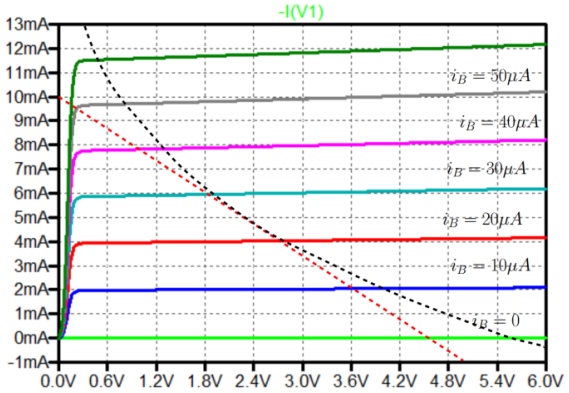
$$i_B = k\frac{V_{CC} - V_{CE_{sat}}}{\beta R_C} = 3\frac{5}{100*500} = 0.3\ mA.$$

Now we need find value of R_B

$$R_B = \frac{V_i - V_{BE}}{I_B},$$

Transistor switch mode



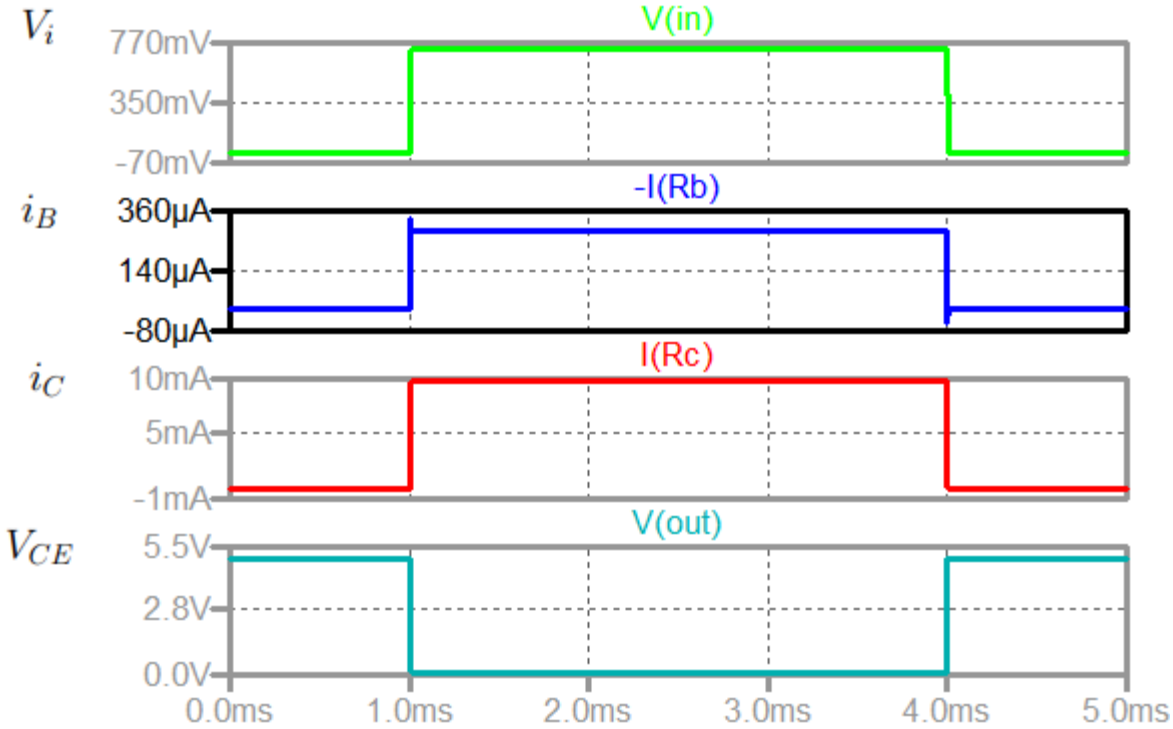


For $V_i = 5\ V$ we have

$$R_B = \frac{V_i - V_{BE}}{I_B} = \frac{5 - 0.7}{0.0003} = 14333.3\ \Omega$$

We chose $R_B = 15\ k\Omega$.

Transistor switch mode



Transistor switch mode

Basic level of first part of laboratory work is to simulate the typical inverter circuit using a bipolar transistor.

You should make an inverter circuit in LTspice:

- Choose transistor model;
- Make calculations parameters of resistors (without neglecting small value of $V_{CE_{sat}} = 0.2 \dots 0.3\ V$);
- Make simulations of inverter circuit.

2. Combinational Logic Circuits

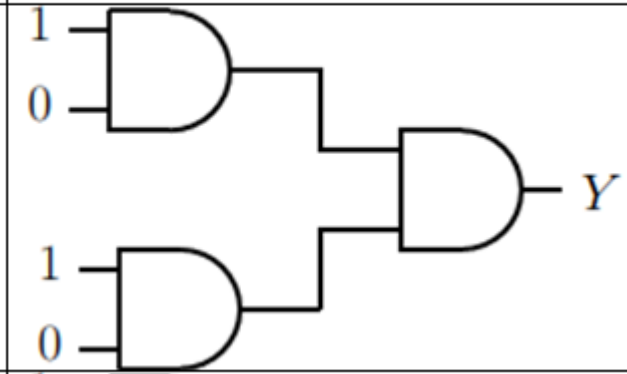
Choose you circuit variant from Table 2.

You should build circuit diagram in LtSpice and make simulations.

In the report you should draw your circuit, true table, Boolean function and simulation results from LtSpice.

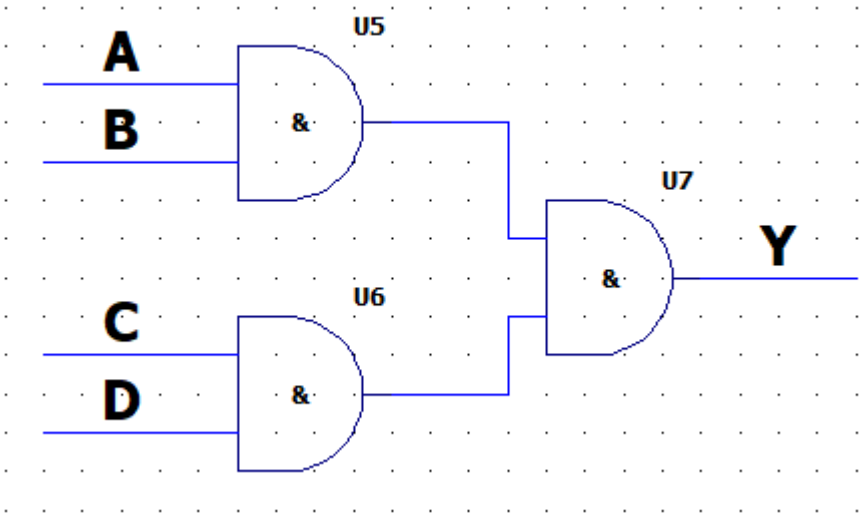
Combinational Logic Circuits

First step – you find your logic scheme from laboratory work assignment and write true table.

№	Circuit	N
1		1
2	1	1

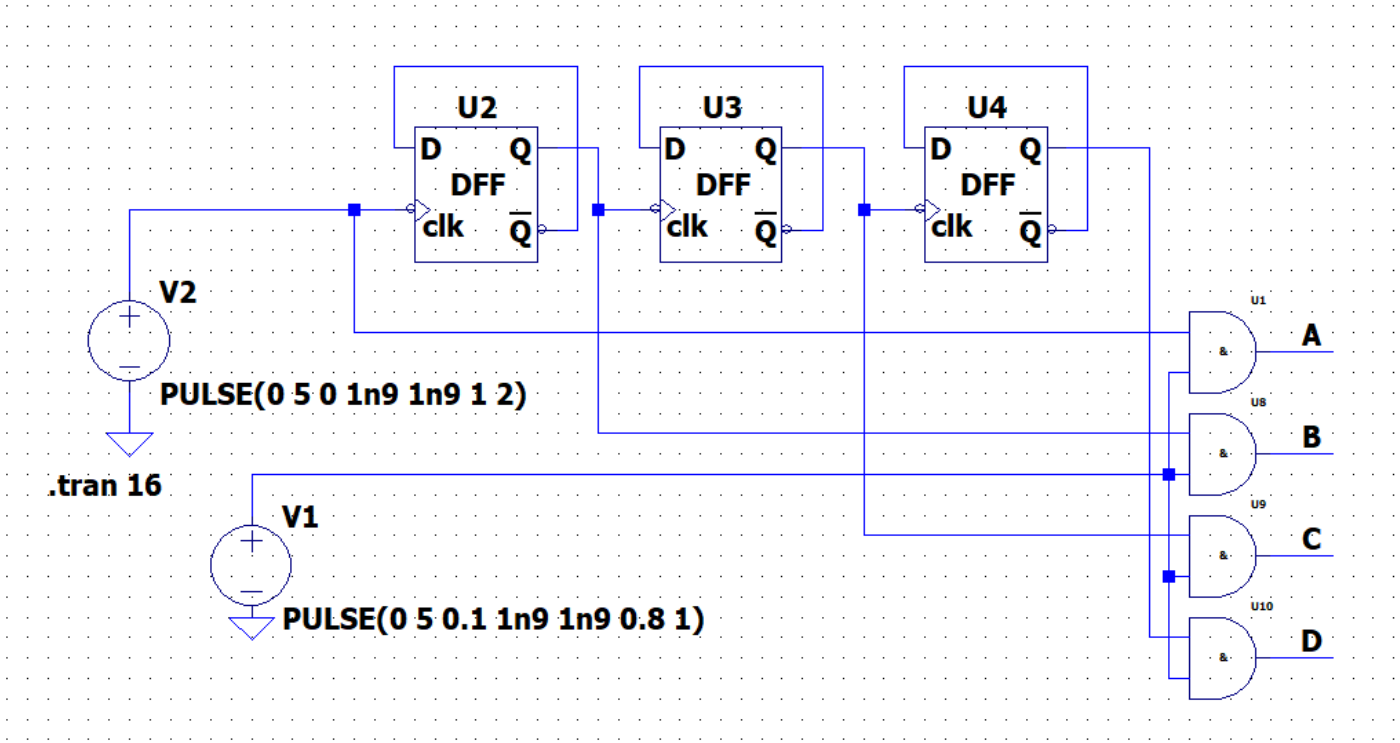
№	A	B	C	D	Y
1	1	1	1	1	
2	0	1	1	1	
3	1	0	1	1	
4	0	0	1	1	
5	1	1	0	1	
6	0	1	0	1	
7	1	0	0	1	
8	0	0	0	1	
9	1	1	1	0	
10	0	1	1	0	
11	1	0	1	0	
12	0	0	1	0	
13	1	1	0	0	
14	0	1	0	0	
15	1	0	0	0	
16	0	0	0	0	

Combinational Logic Circuits

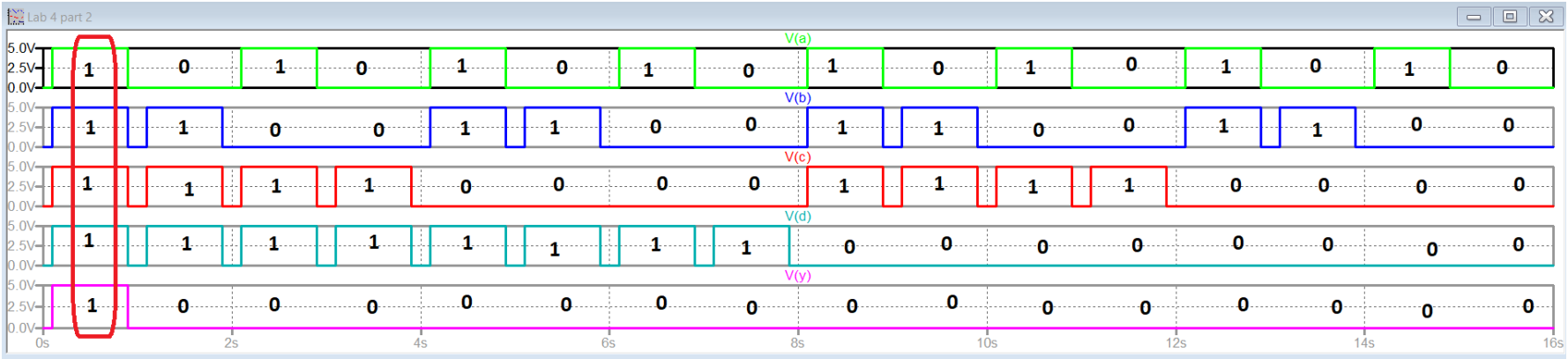


Input signals you can generate by using voltage source or by using our generator.

Combinational Logic Circuits



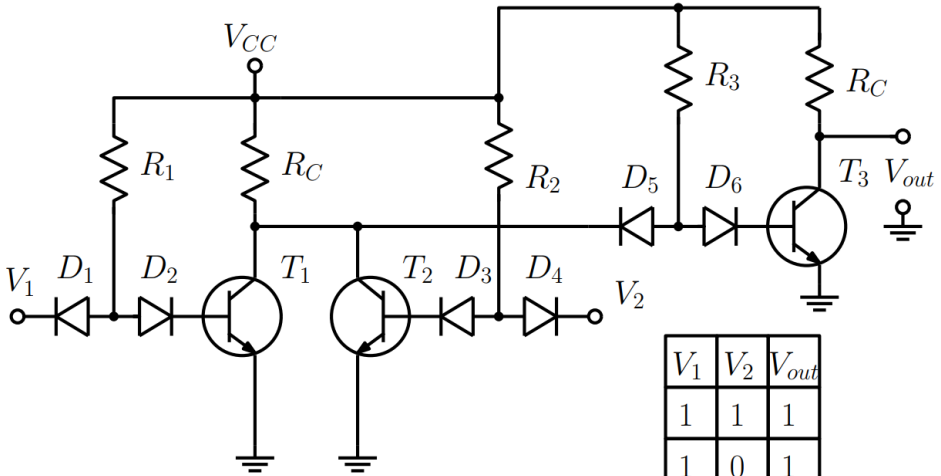
Third step – You should make simulation of your scheme.



Final step – You should make the laboratory report.

3 Logic families

In this part we consider the simplest schematic decisions for logic families.
For example, we consider the most complicated example of DTL family.



V_1	V_2	V_{out}
1	1	1
1	0	1
0	1	1
0	0	0

First of all we suppose that we have power supply $V_{cc} = 10\ V$ and we need to have $I_C = 10\ mA$.

We will use npn transistor 2N2222.

We need to find the datasheet for transistor and find common-emitter current gain.

2N2222 / 2N2222A

NPN Silicon Epitaxial Planar Transistor
for switching and AF amplifier applications.

The transistor is subdivided into one group according to its DC current gain.

On special request, these transistors can be manufactured in different pin configurations.

2N2222 / 2N2222A

Characteristics at T_a = 25 °C

Parameter		Symbol	Min.	Max.	Unit
DC Current Gain					
at V_{CE} = 10 V, I_C = 0.1 mA		h_{FE}	35	-	-
at V_{CE} = 10 V, I_C = 1 mA		h_{FE}	50	-	-
at V_{CE} = 10 V, I_C = 10 mA		h_{FE}	75	-	-
at V_{CE} = 10 V, I_C = 150 mA		h_{FE}	100	300	-
at V_{CE} = 10 V, I_C = 500 mA	2N2222	h_{FE}	30	-	-
	2N2222A	h_{FE}	40	-	-
Collector Base Cutoff Current					
at V_{CB} = 50 V	2N2222	I_{CBO}	-	10	nA
at V_{CB} = 60 V	2N2222A		-	10	
Collector Base Breakdown Voltage					

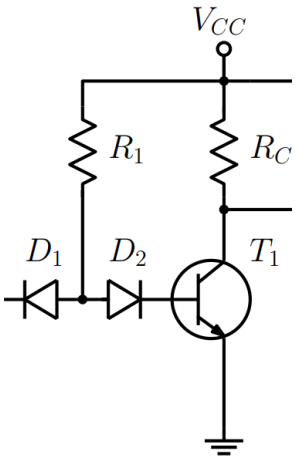
$$h_{FE} = 75$$

We can find resistance of collector resistor R_C.

$$R_C = \frac{V_{CC} - V_{CE_{sat}}}{I_C}$$

V_{CC} - we know and $V_{CE_{sat}} \approx 0.2\ V$.

$$R_C = \frac{10 - 0.2}{10 \cdot 10^{-3}} = 980\ \Omega$$



Now we can find the base current, we know that in active region

$$I_C = h_{FE} I_B$$

or for I_B we have

$$I_B = \frac{I_C}{h_{FE}}$$

We have h_{FE} and I_C

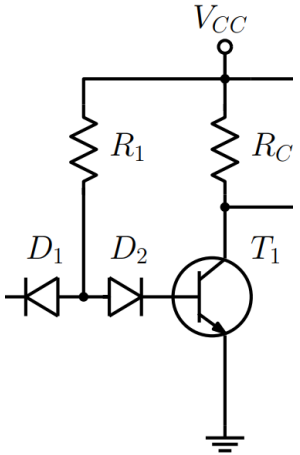
$$I_B = \frac{10 \cdot 10^{-3}}{75} = 0{,}13\ mA$$

This is minimal value of base current. We should choose $I_{B_{sat}} = (2 \dots 5) I_B$.
We choose $I_{B_{sat}}$=0.5 mA.

Now we can find resistance of base resistor

$$R_B = \frac{V_{CC} - V_{VD} - V_{BE}}{I_{B_{sat}}}$$

where we can use $V_{VD} \approx 0.6\ V$ and $V_{BE} \approx 0.6\ V$

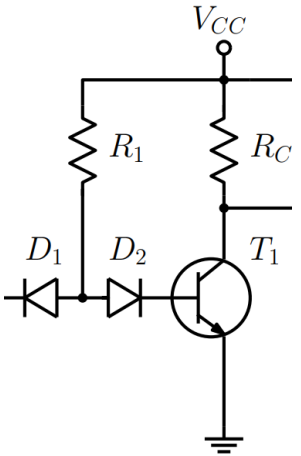


Now we have

$$R_B = \frac{10 - 0.7 - 0.7}{10 \cdot 10^{-3}} = 17.6\ k\Omega$$

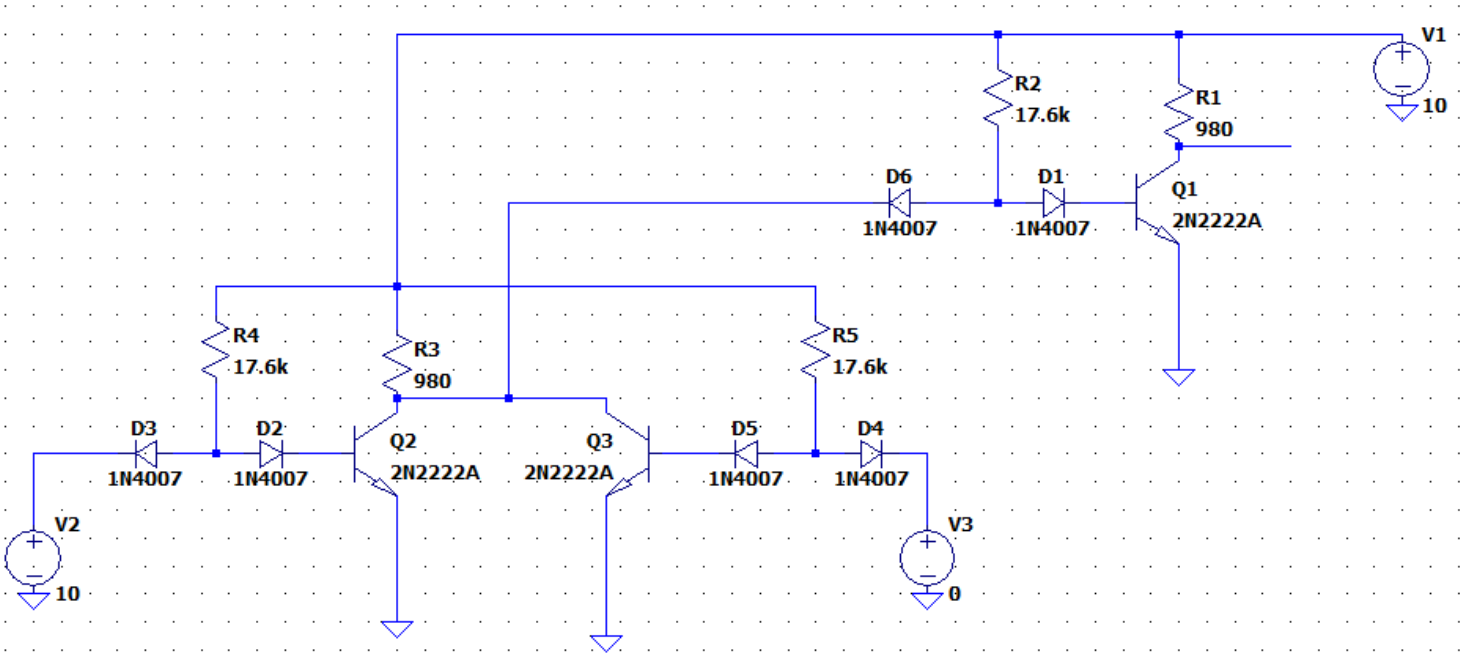
As a diode we chose commonly used diode 1N4007.

We chose all parameters of three transistor switches are equal.



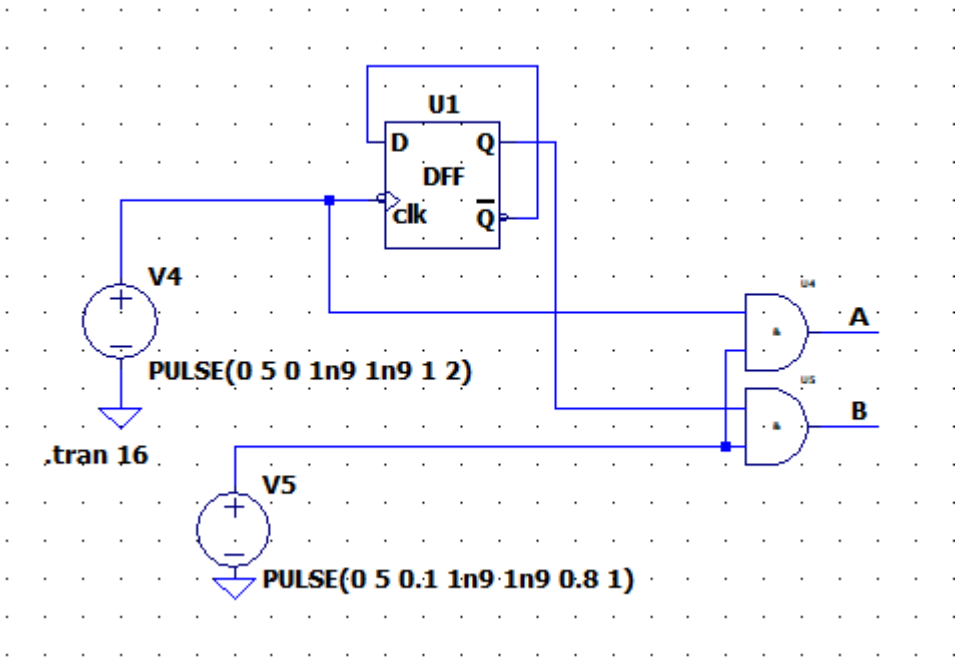
Logic families

Now we cam make scheme in LtSpice



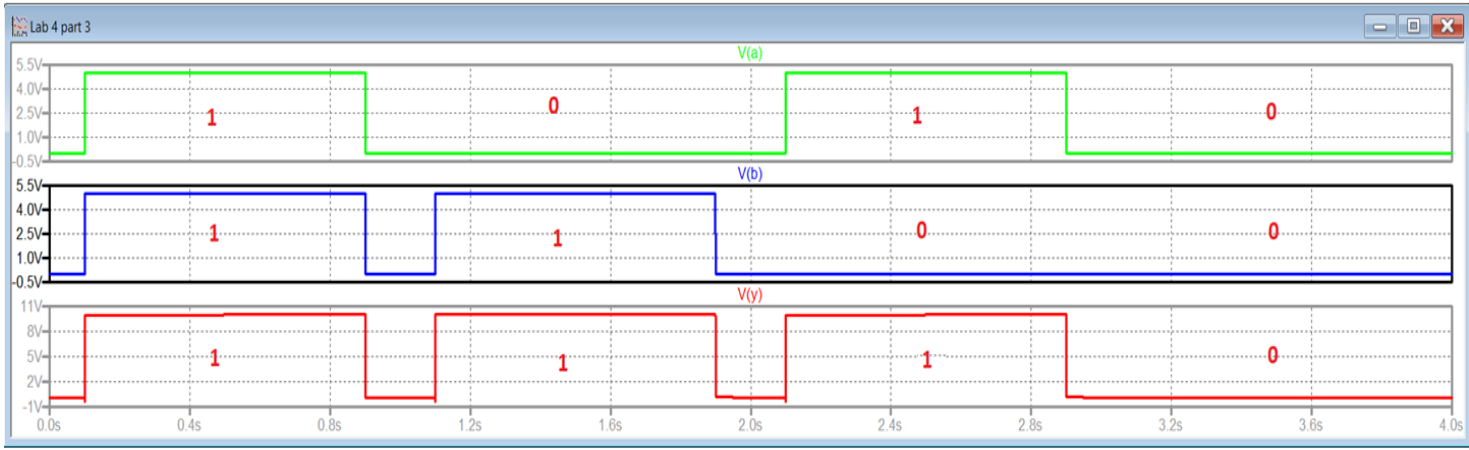
Logic families

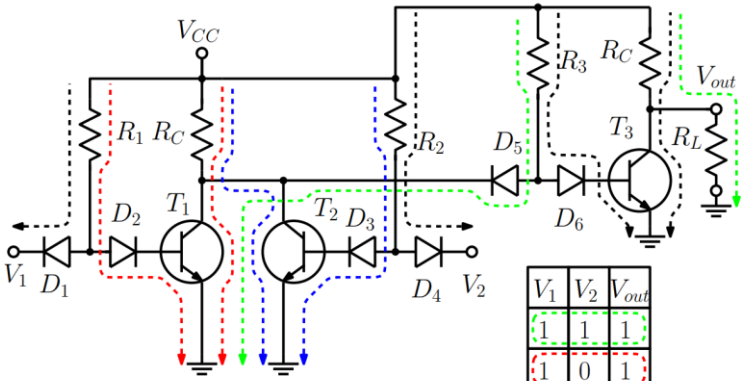
You can simulate input signals by voltage sources or use our simple generator.



Logic families

Simulation results





V_1	V_2	V_{out}
1	1	1
1	0	1
0	1	1
0	0	0

Final step – You should prepare the laboratory report.

ITMO

Thank you for your attention!