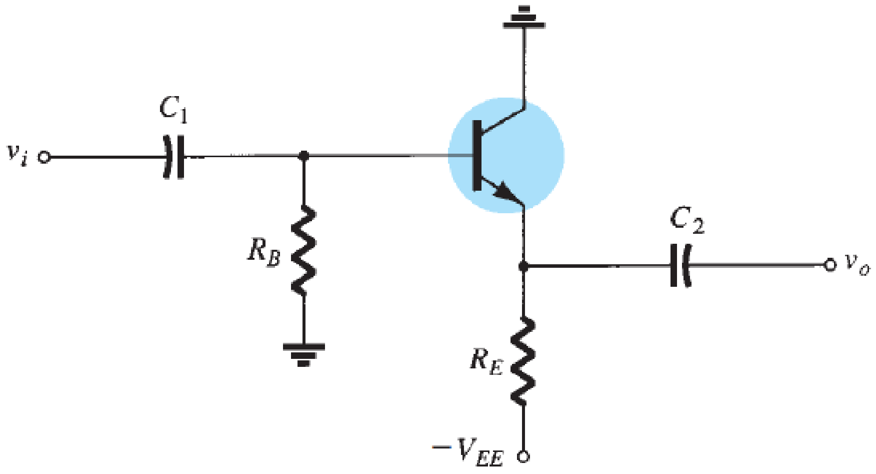
Amplifier configurations

Nikolay Nikolaev (nanikolaev@itmo.ru)
Nikolai Poliakov (polyakov_n_a@itmo.ru)

Emitter-follower configuration

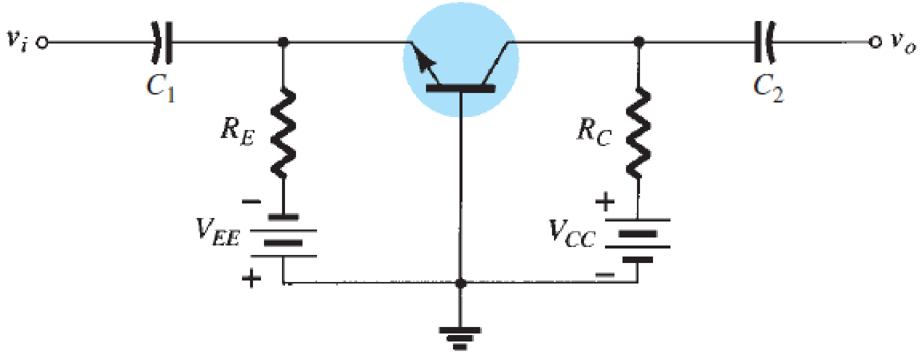


$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$V_{CE} = V_{EE} - I_E R_E$$

$$A_i = \frac{I_{out}}{I_{in}} = \frac{I_E}{I_B} = \beta \gg 1$$

Common-base configuration



$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E)$$

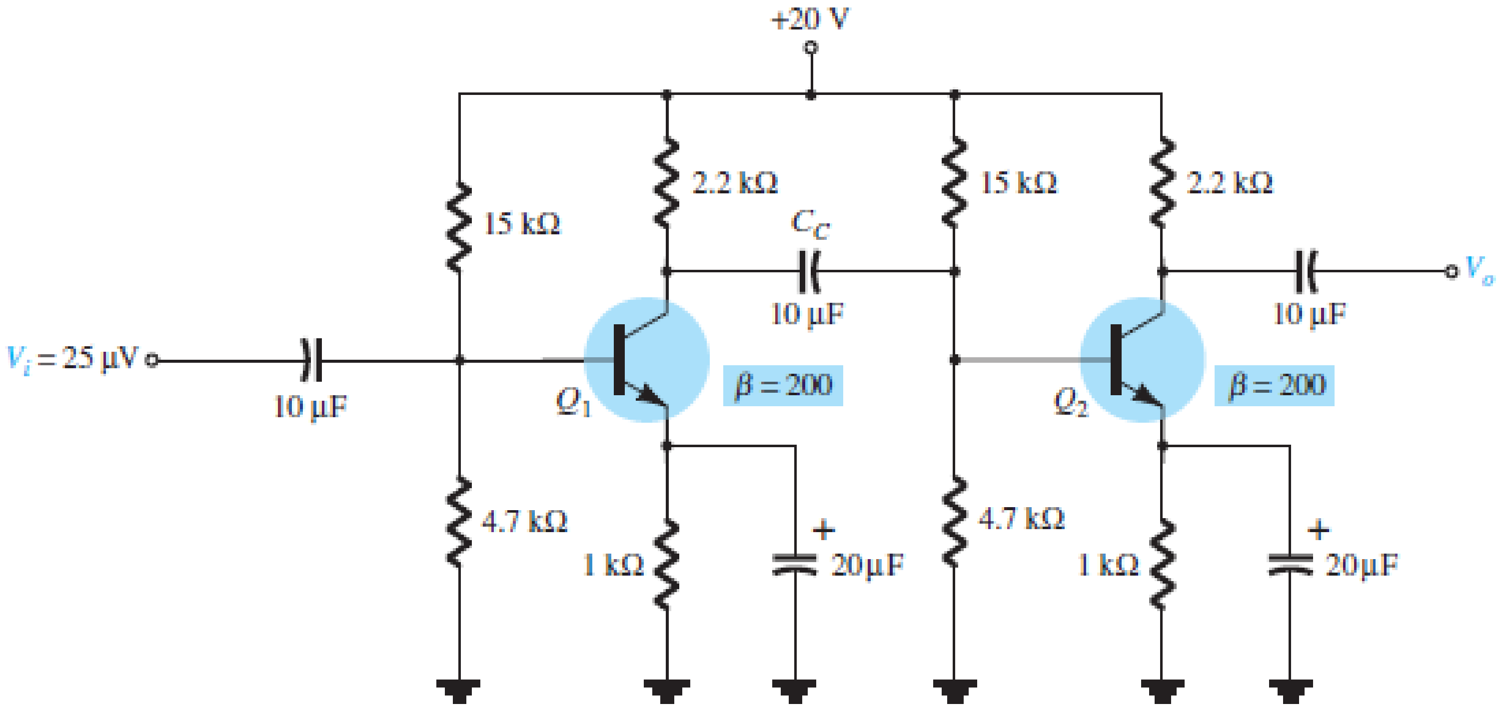
$$V_{CB} = V_{CC} - I_C R_C$$

$$A_i = \frac{I_{out}}{I_{in}} = \frac{I_C}{I_E} = \alpha \cong 1$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{V_C}{V_E} = \frac{R_C I_C}{R_E I_E} \cong \frac{R_C}{R_E}$$

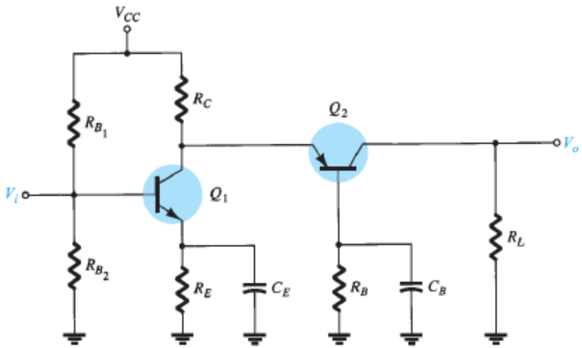
Given dynamic emitter resistance, are, we get

$$A_v =\cong \frac{R_C}{r_E}$$

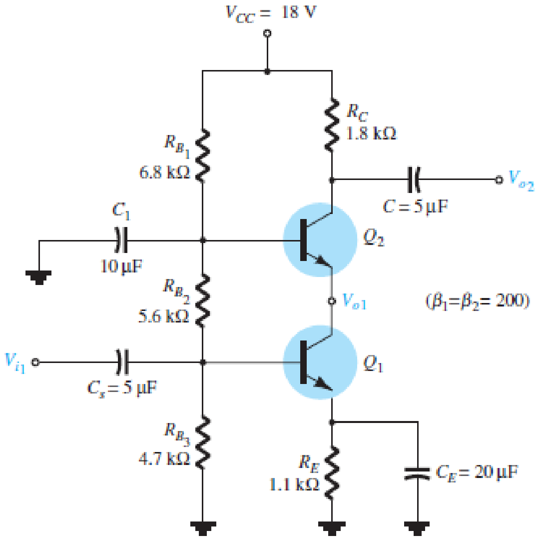

+20 V
2.2 kΩ
15 kΩ
C_C
15 kΩ
2.2 kΩ
10 μF
10 μF
V_o
V_i = 25 μV
10 μF
Q_1
β = 200
Q_2
β = 200
4.7 kΩ
1 kΩ
20μF
4.7 kΩ
1 kΩ
20μF

Cascode Connection

Cascode configuration



Practical cascode circuit



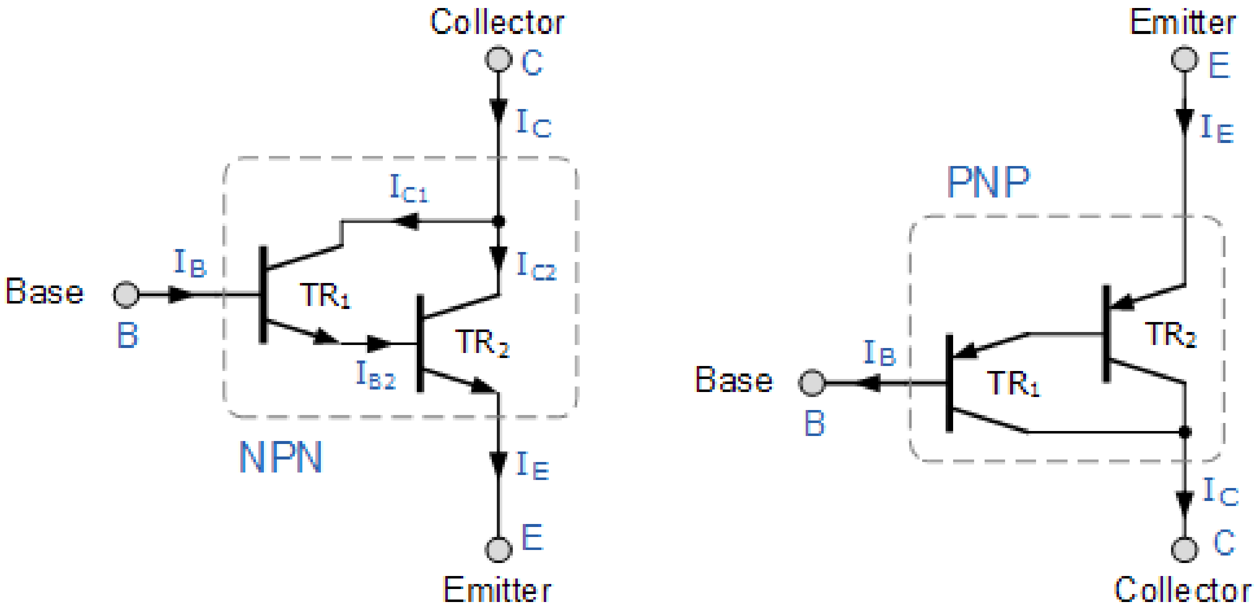
Advantages:

- ✓ The bandwidth is high due to the elimination of the Miller Effect.
- ✓ Due to the cascode connection between two transistors the overall gain of the system is high.
- ✓ Even the parts of the count for both the transistors are low.

Disadvantages:

- ✓ The presence of two transistors requires a high amount of voltage supply.
- ✓ The sufficient amount ofcollector-emitter voltage must be supplied to both the transistor which strikes lesser the limit on the supply voltage.

Darlington connection. Darlington pair

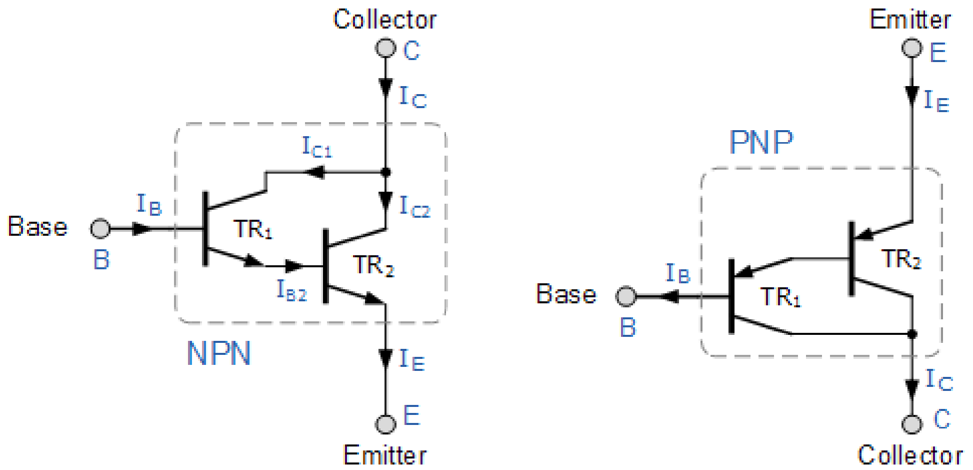


$$\beta_D = \beta_1 \beta_2$$

Advantage

- ✓ Very high current gain
- ✓ Very high input impedance for overall circuit
- ✓ Convenient and easy circuit configuration to use

Darlington connection. Darlington pair

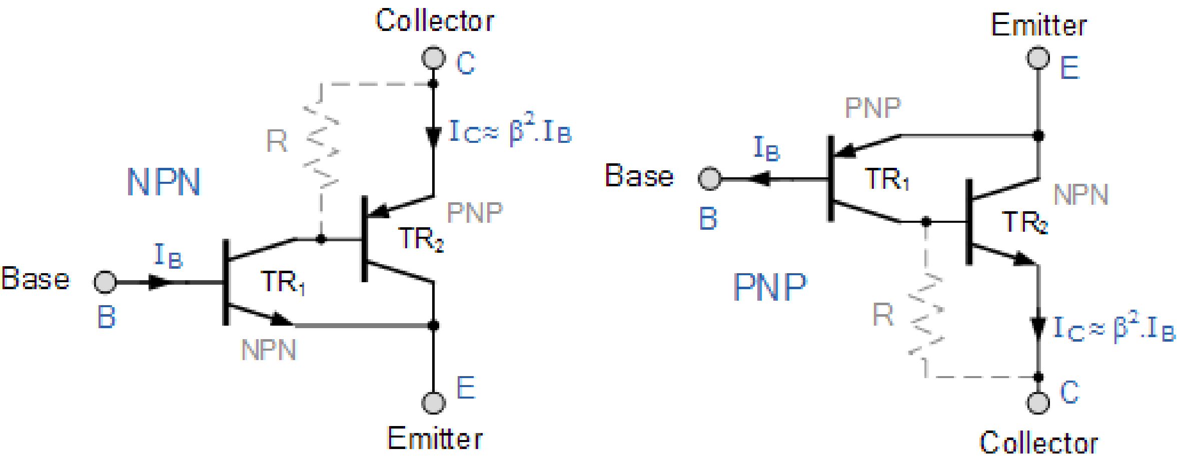


$$\beta_D = \beta_1 \beta_2$$

Disadvantage

- ✓ Slow switching speed
- ✓ Limited bandwidth
- ✓ Introduces a phase shift that can give rise to problems at certain frequencies in circuit using negative feedback
- ✓ Higher overall base-emitter voltage = 2 x Vbe.
- ✓ High saturation voltage (typically around 0.7 V) which can lead to high levels of power dissipation in some applications

Sziklai Pair



Advantage

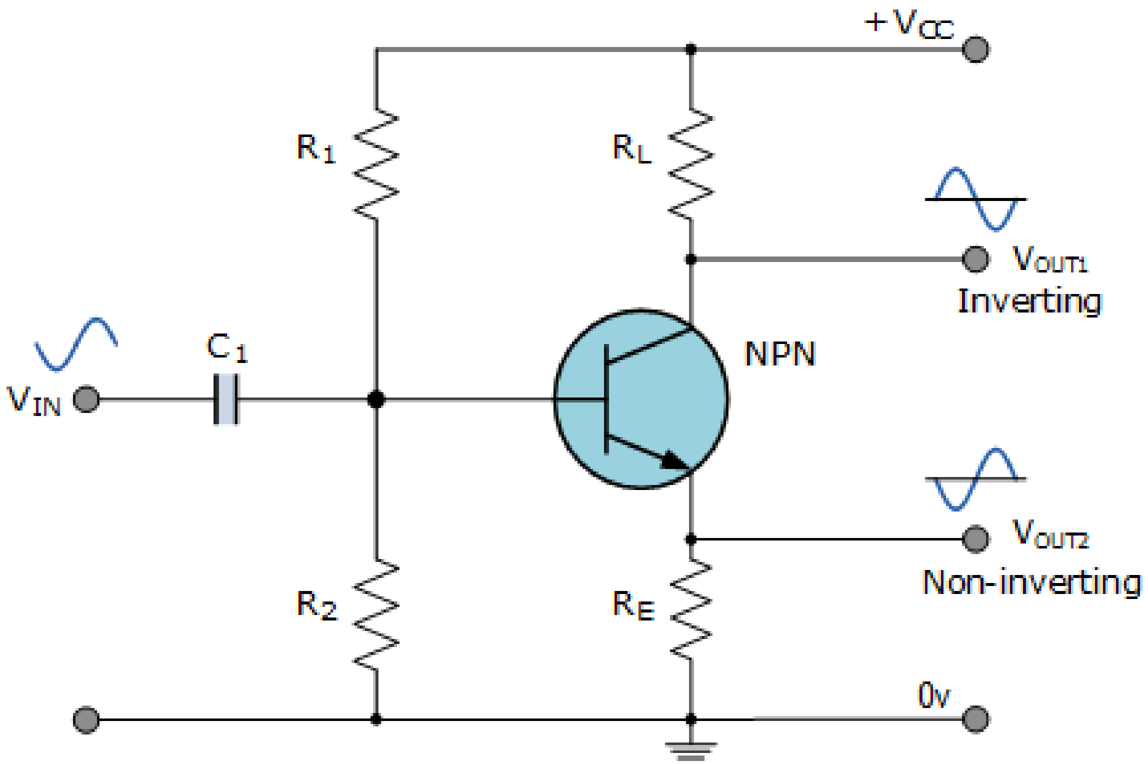
- ✓ Very high current gain
- ✓ Very high input impedance for overall circuit
- ✓ Convenient and easy circuit configuration to use
- ✓ Low overall base-emitter voltage = 1 x Vbe.

$$\beta_S = \beta_1 \beta_2$$

Disadvantage

- ✓ Slow switching speed
- ✓ Limited bandwidth
- ✓ High saturation voltage (typically around 0.7 V) which can lead to high levels of power dissipation in some applications

Phase Splitter Configuration



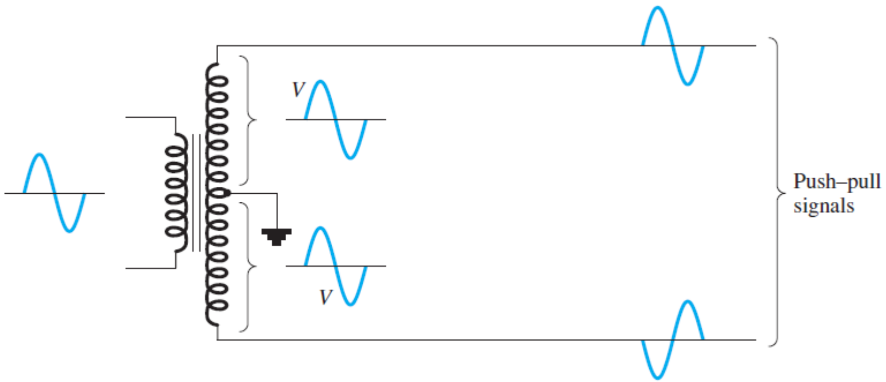
For common emitter

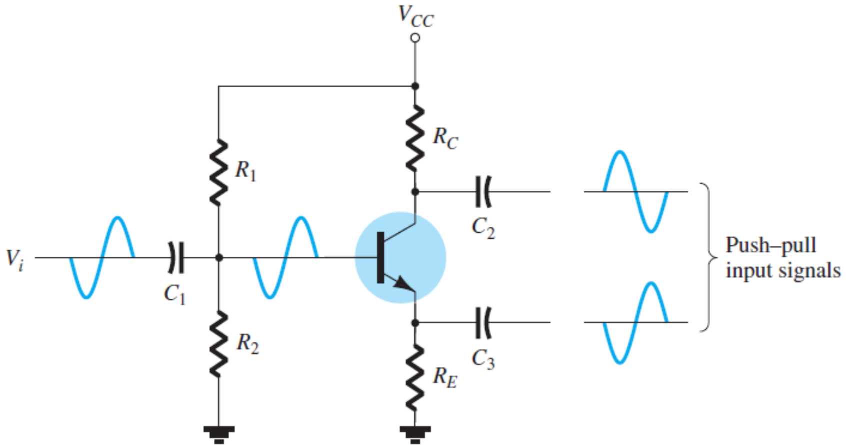
$$A_v = -\frac{R_L}{R_E}$$

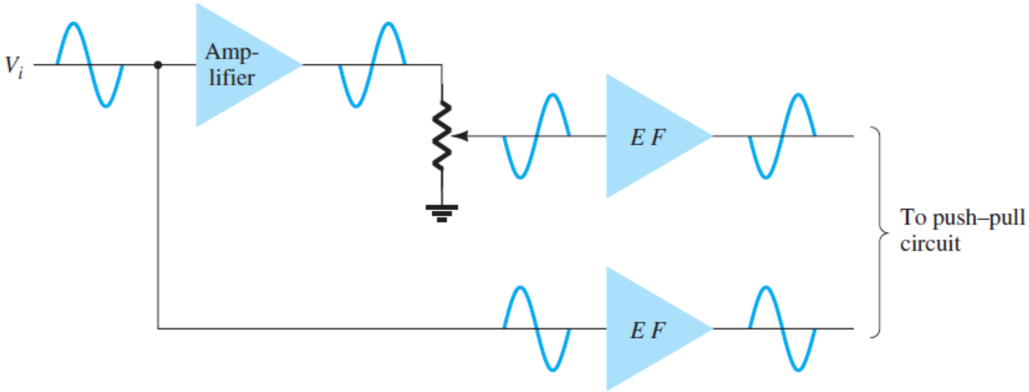
For common collector

$$A_v = 1$$

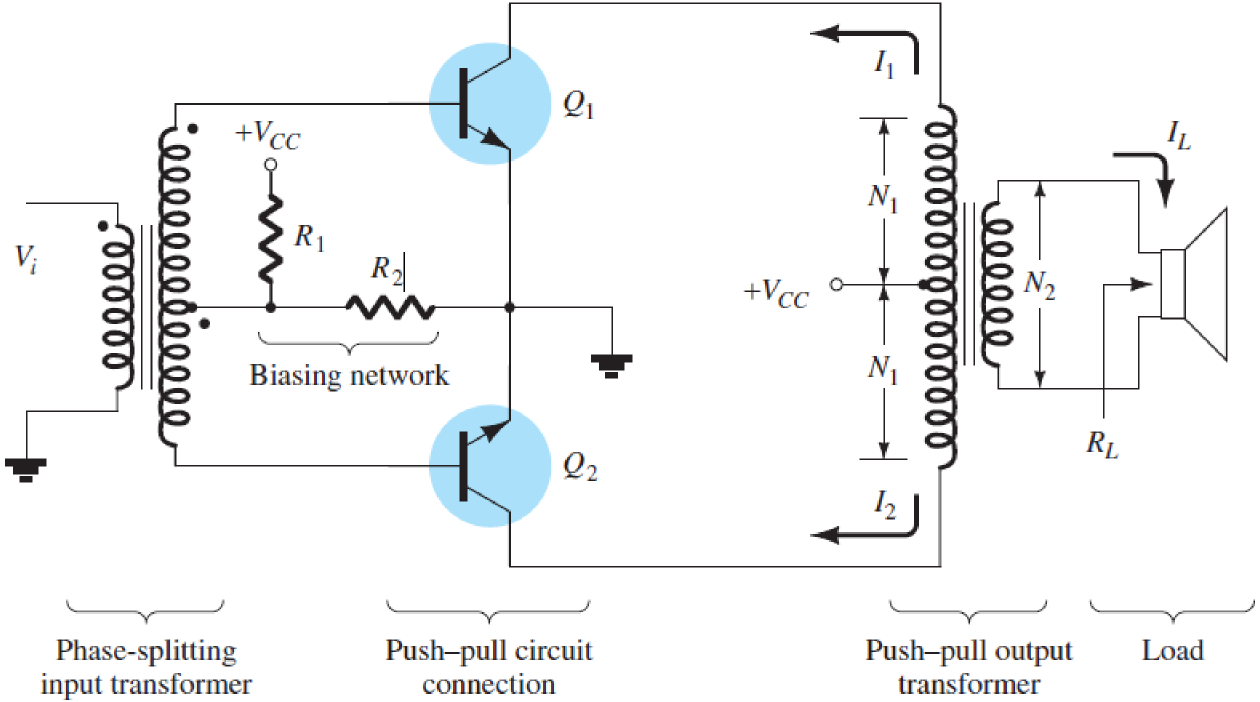
Phase-inverted scheme



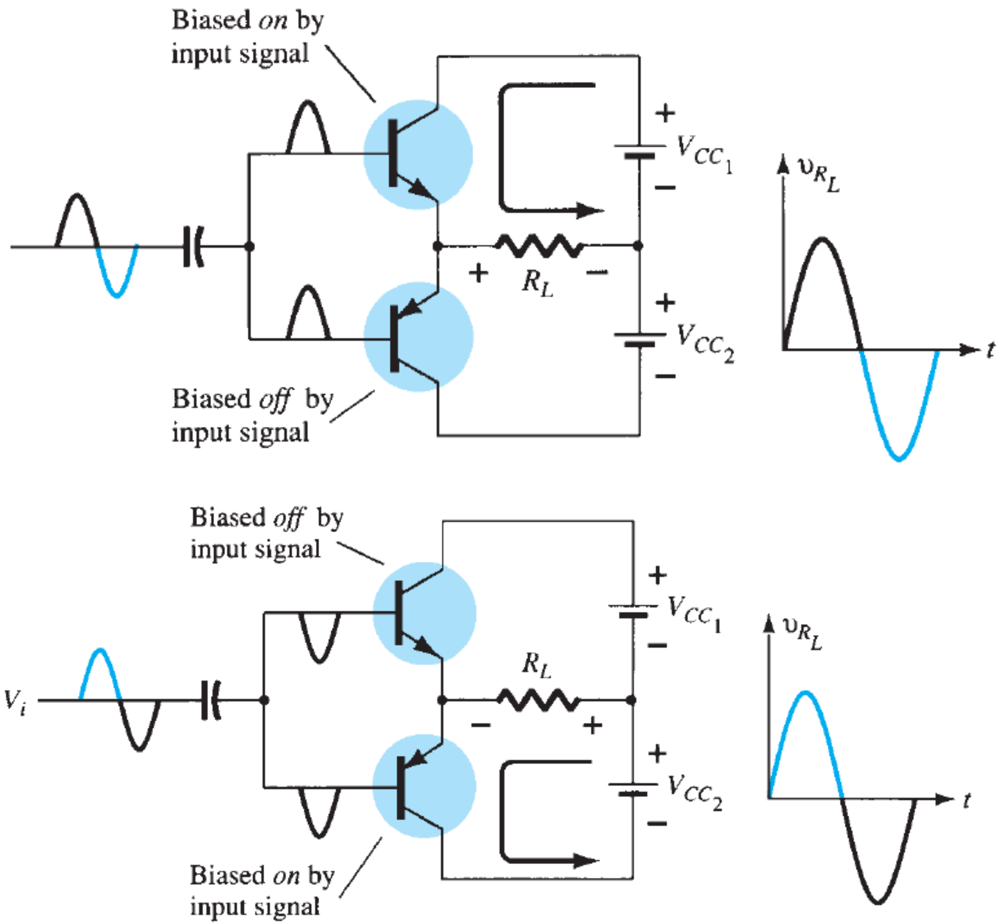


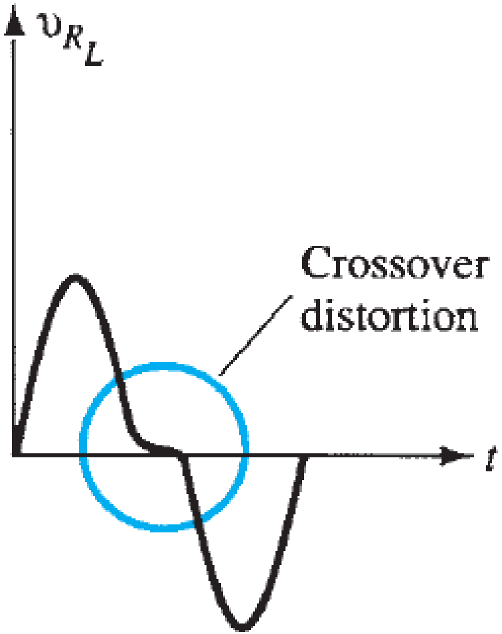


Transformer-Coupled Push–Pull Circuits

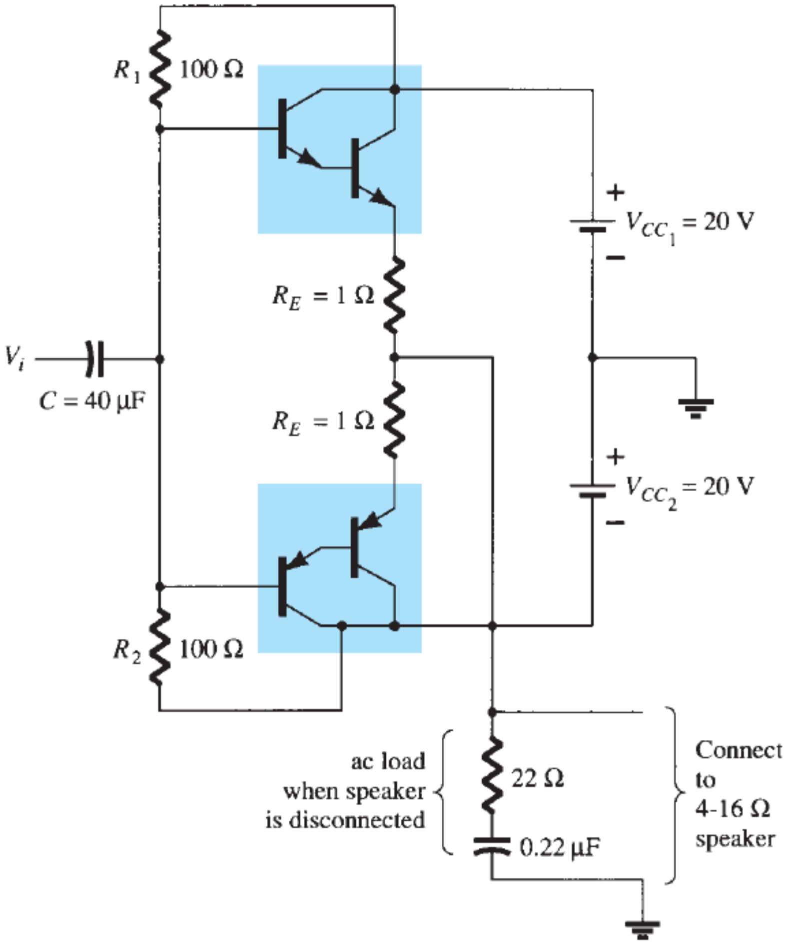


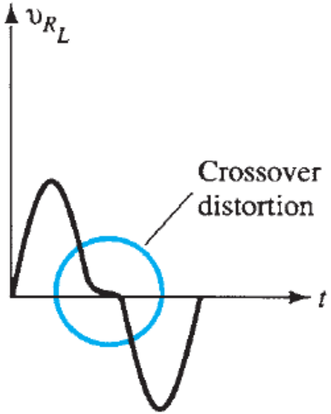
Complementary-Symmetry Circuits



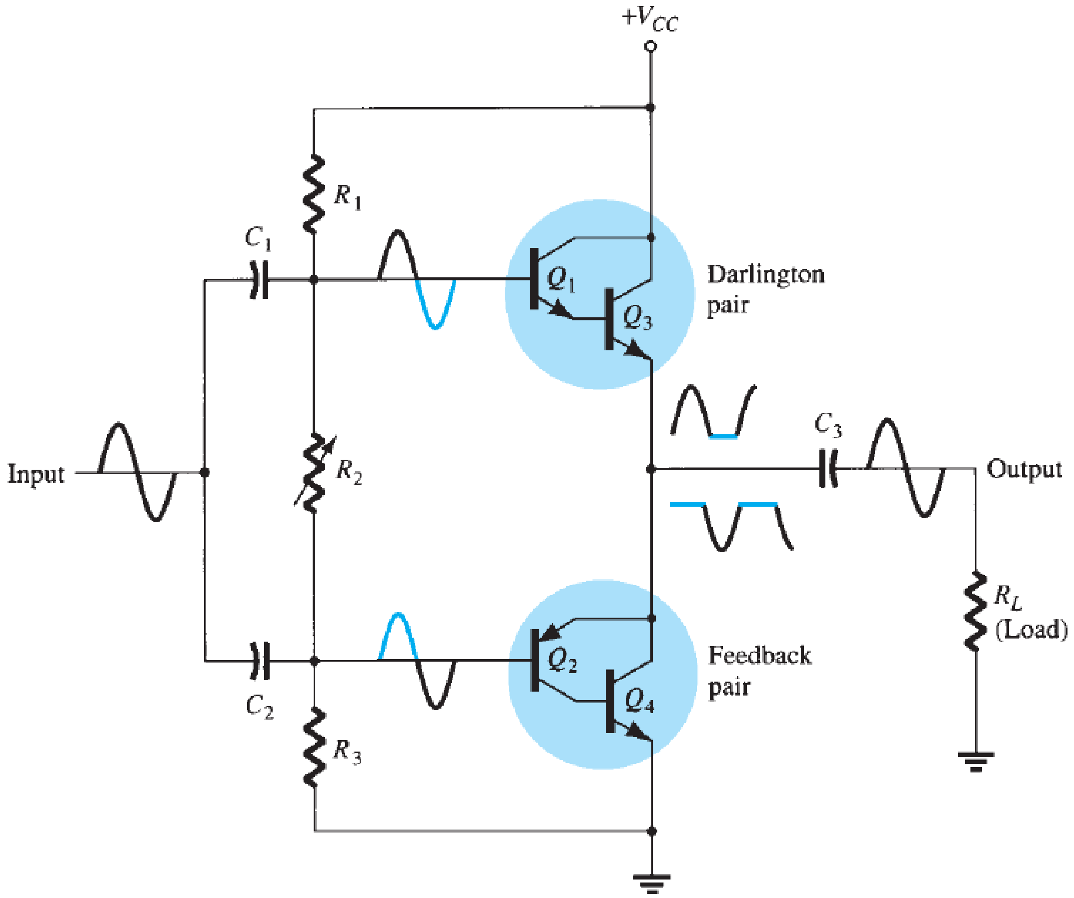


Quasi-Complementary Push–Pull Amplifier

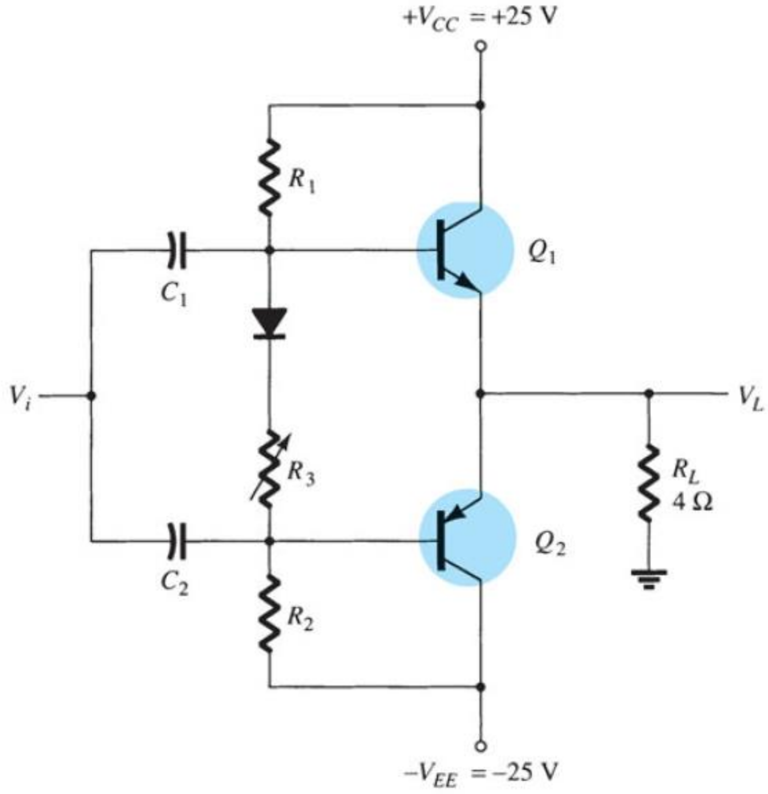


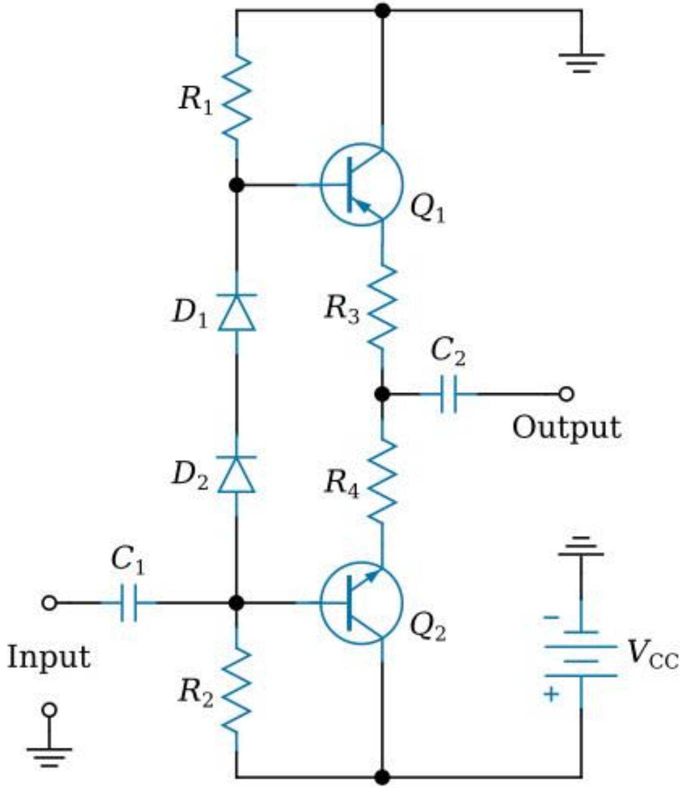


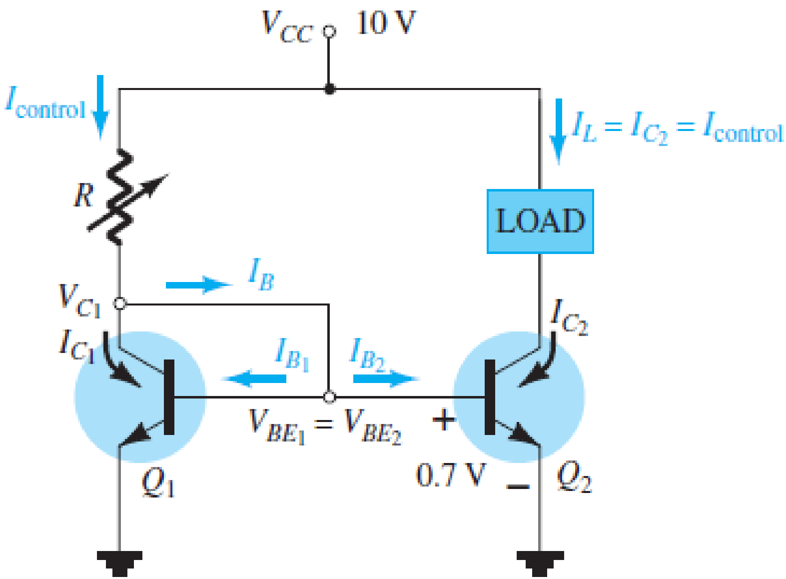
Complementary-Symmetry Circuits

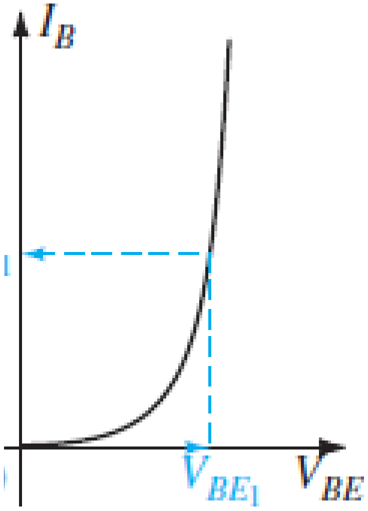


Complementary-Symmetry Circuits









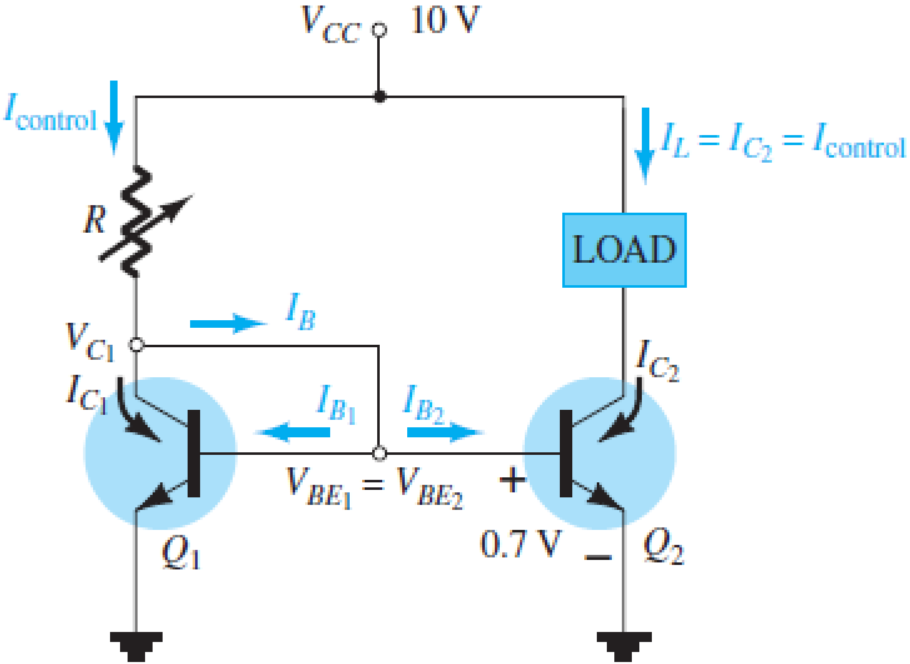
$$\boxed{I_{control} = \frac{V_{CC} - V_{BE}}{R}}$$

$$I_B = I_{B_1} + I_{B_2}$$
$$I_{B_1} = I_{B_2}$$
$$I_B = I_{B_1} + I_{B_1} = 2I_{B_1}$$

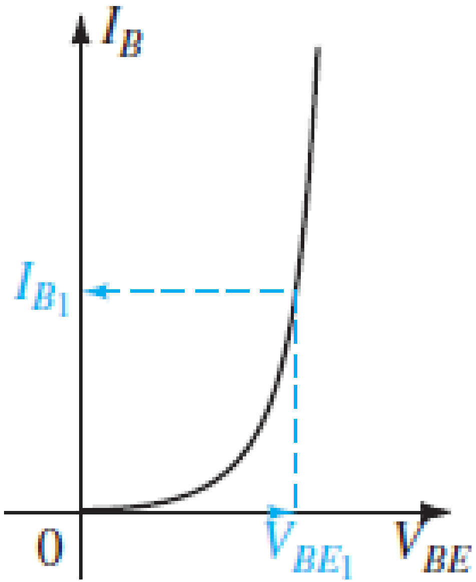
$$I_{control} = I_{C_1} + I_B = I_{C_1} + 2I_{B_1}$$
$$I_{C_1} = \beta_1 I_{B_1}$$
$$I_{control} = \beta_1 I_{B_1} + 2I_{B_1} = (\beta_1 + 2)I_{B_1}$$
$$I_{control} \cong \beta_1 I_{B_1}$$

$$I_{B_1} = \frac{I_{control}}{\beta_1}$$

Current mirrors



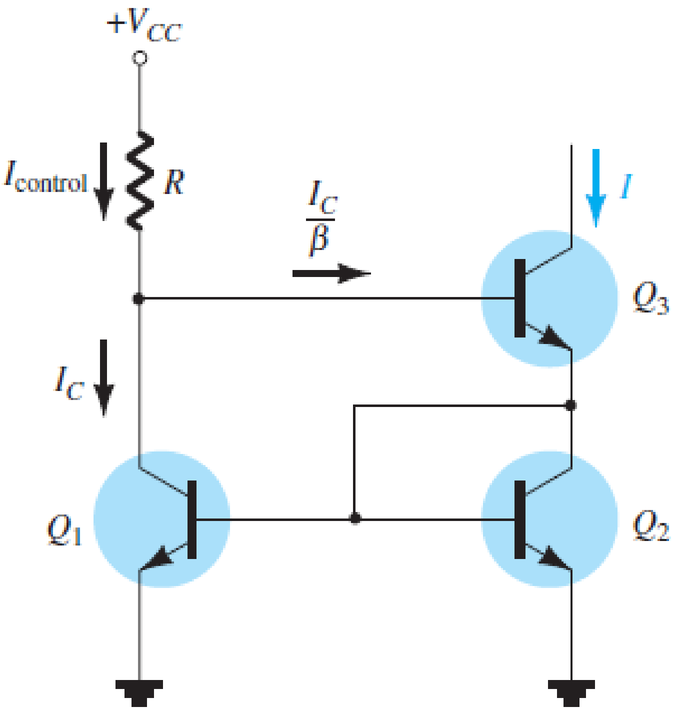
$$I_{B2} = \frac{I_{C2}}{\beta_2} = \frac{I_L}{\beta_2}$$

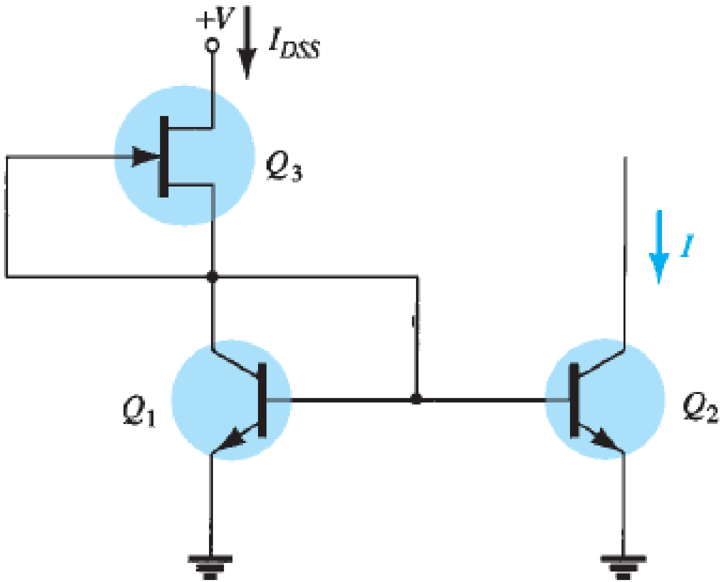


$$I_L \uparrow I_{C_2} \uparrow I_{B_2} \uparrow V_{BE_2} \uparrow V_{CE_1} \downarrow, I_R \downarrow, I_B \downarrow, I_{B_2} \downarrow I_{C_2} \downarrow I_L \downarrow$$

Note

Current mirrors 2

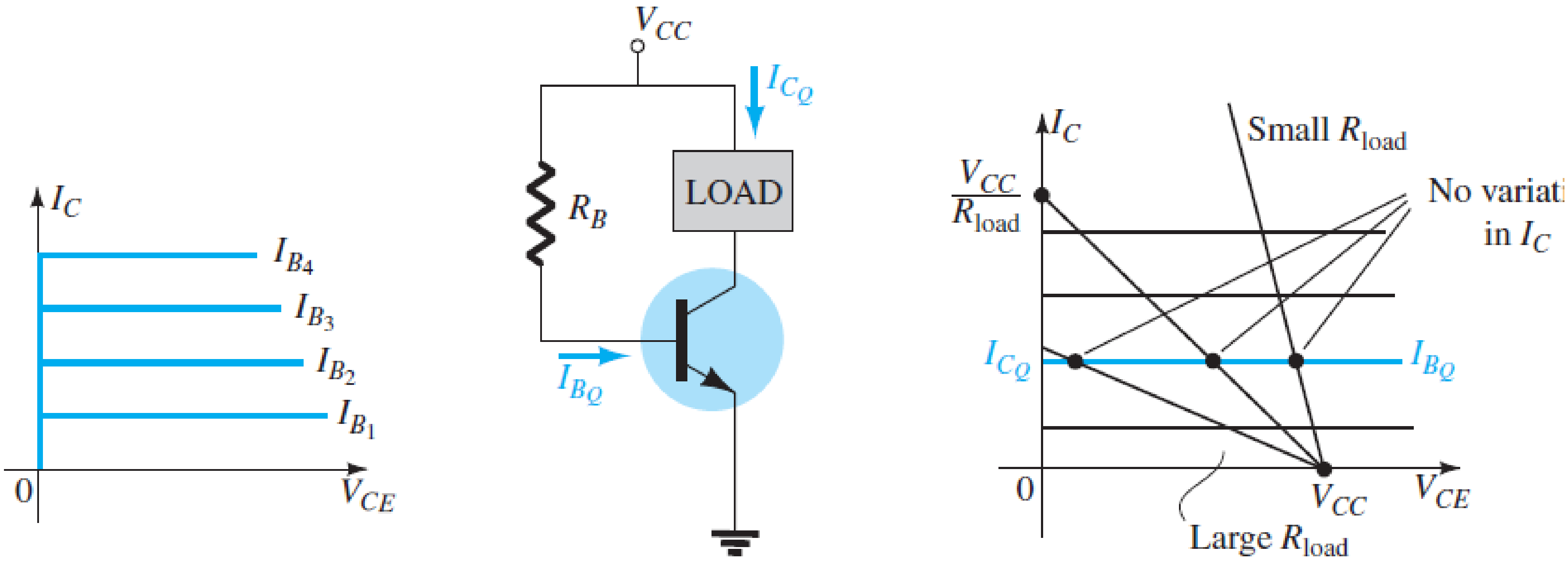




$$I_{\text{control}} = \frac{V_{CC} - 2V_{BE}}{R} \approx I_C + \frac{I_C}{\beta} = \frac{\beta + 1}{\beta} I_C \approx I_C$$

$$I = I_{DSS}$$

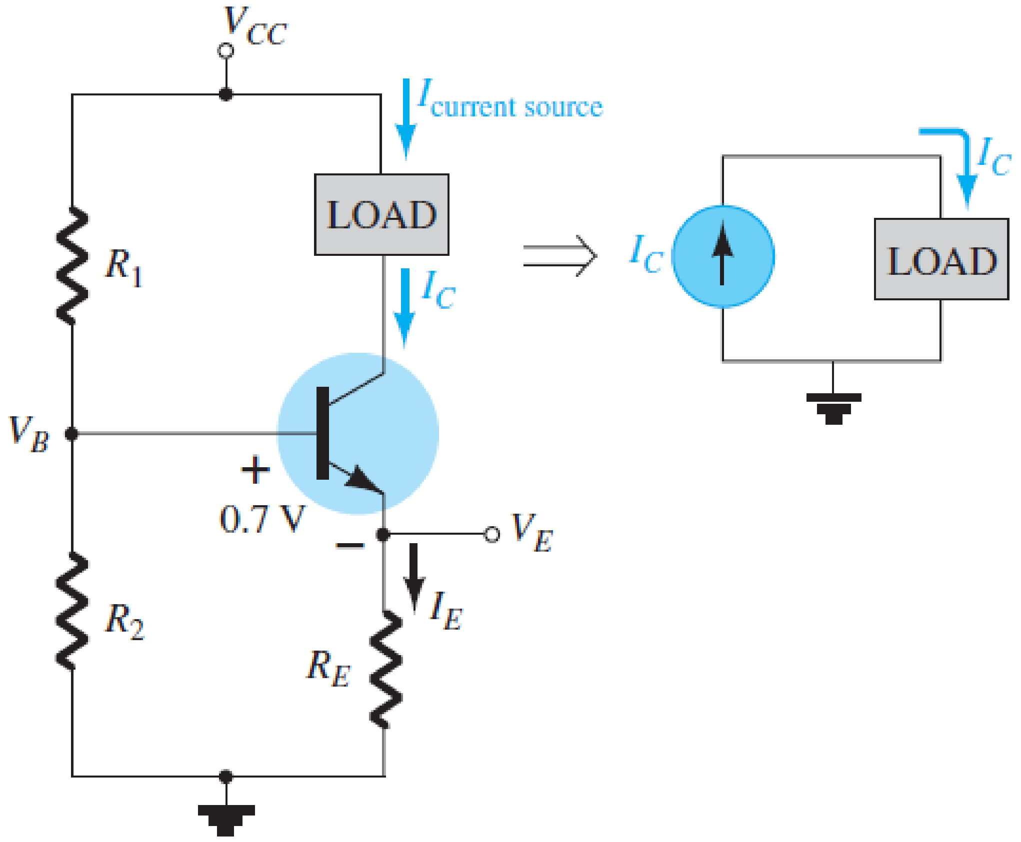
Maintaining a Fixed Load Current



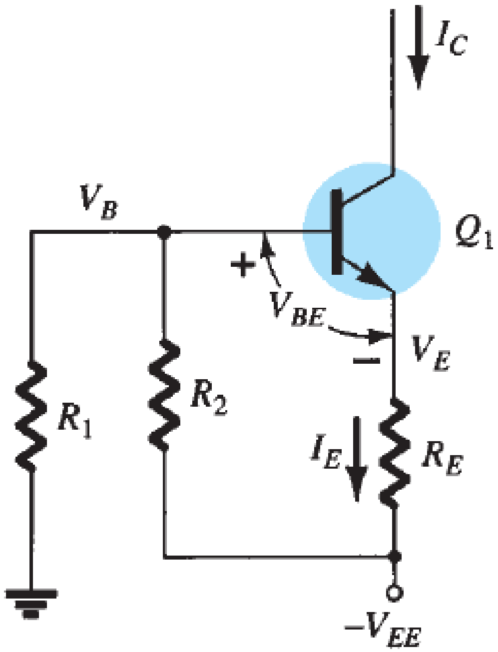
$$V_E = V_B - 0.7\text{ V}$$

$$I_C \cong I_E = \frac{V_E}{R_E} = \frac{V_B - 0.7\text{ V}}{R_E}$$

Maintaining a Fixed Load Current



Current source circuits

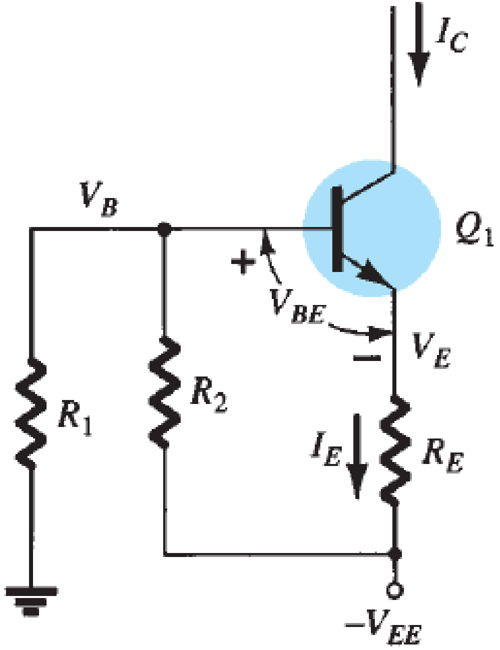


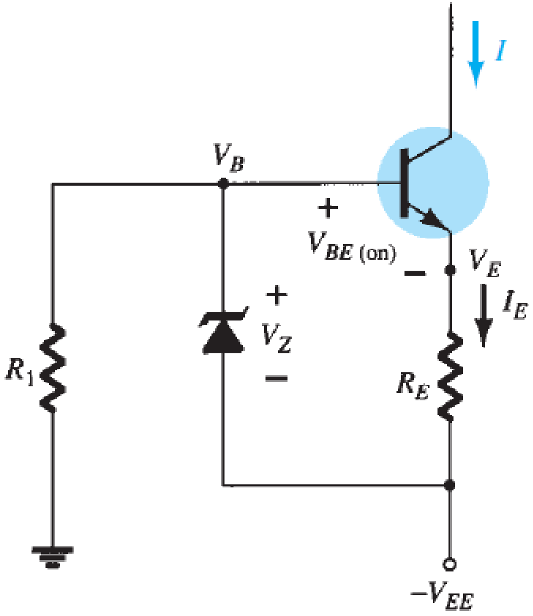
$$V_B = \frac{R_1}{R_1 + R_2}(-V_{EE})$$

$$V_E = V_B - 0.7\ \text{V}$$

$$I_E = \frac{V_E - (-V_{EE})}{R_E} \approx I_C$$

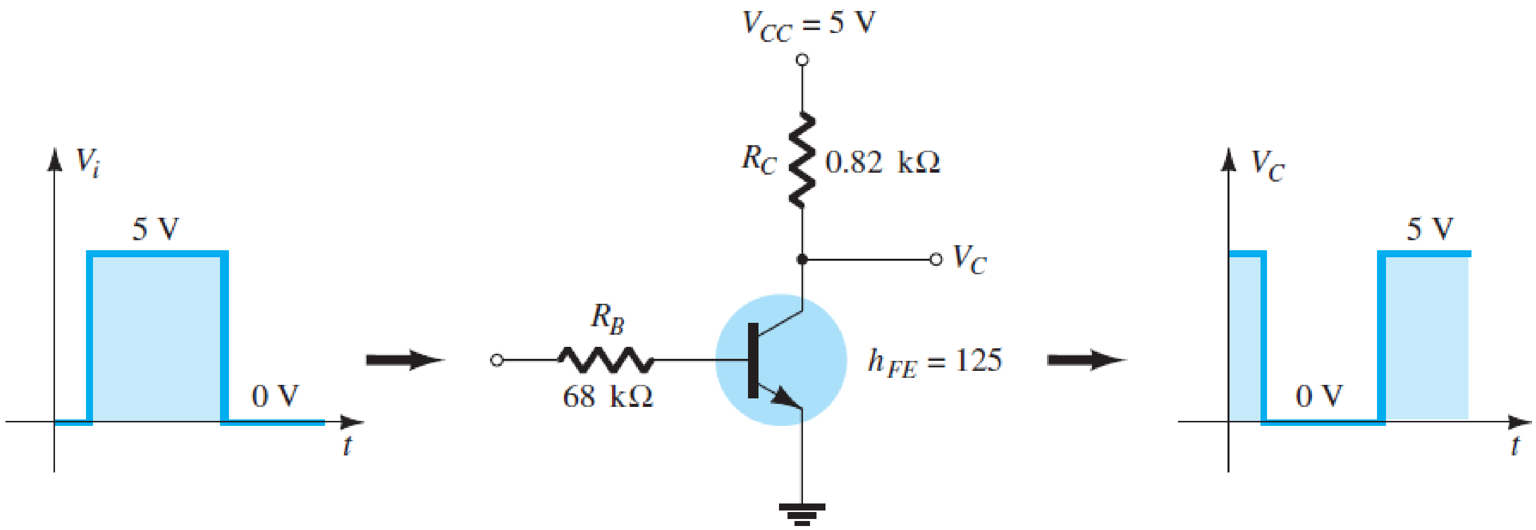
Transistor/Zener Constant-Current Source



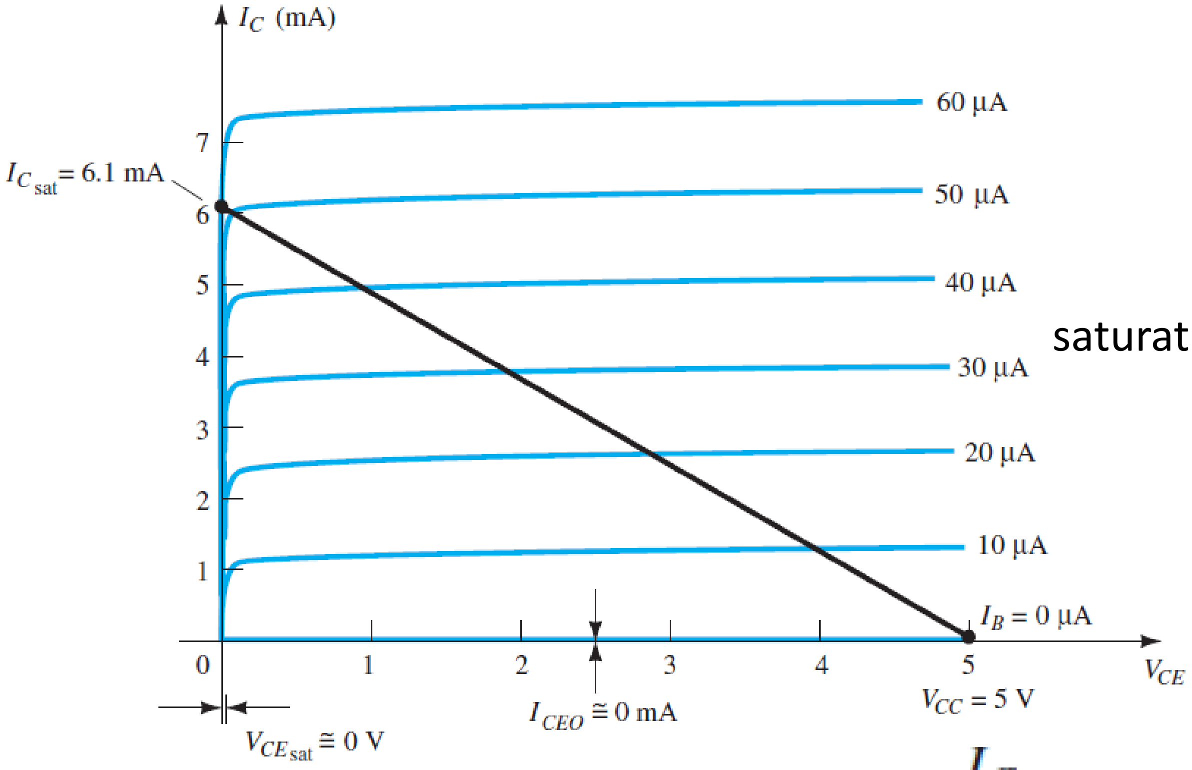


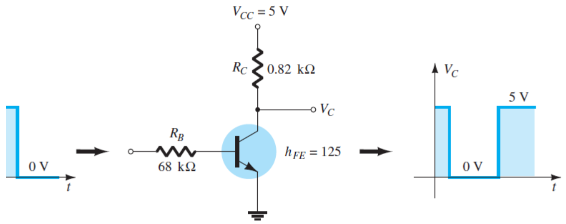
$$I \approx I_E = \frac{V_Z - V_{BE}}{R_E}$$

Transistor switching networks



Transistor switching networks





saturation level for the collector current

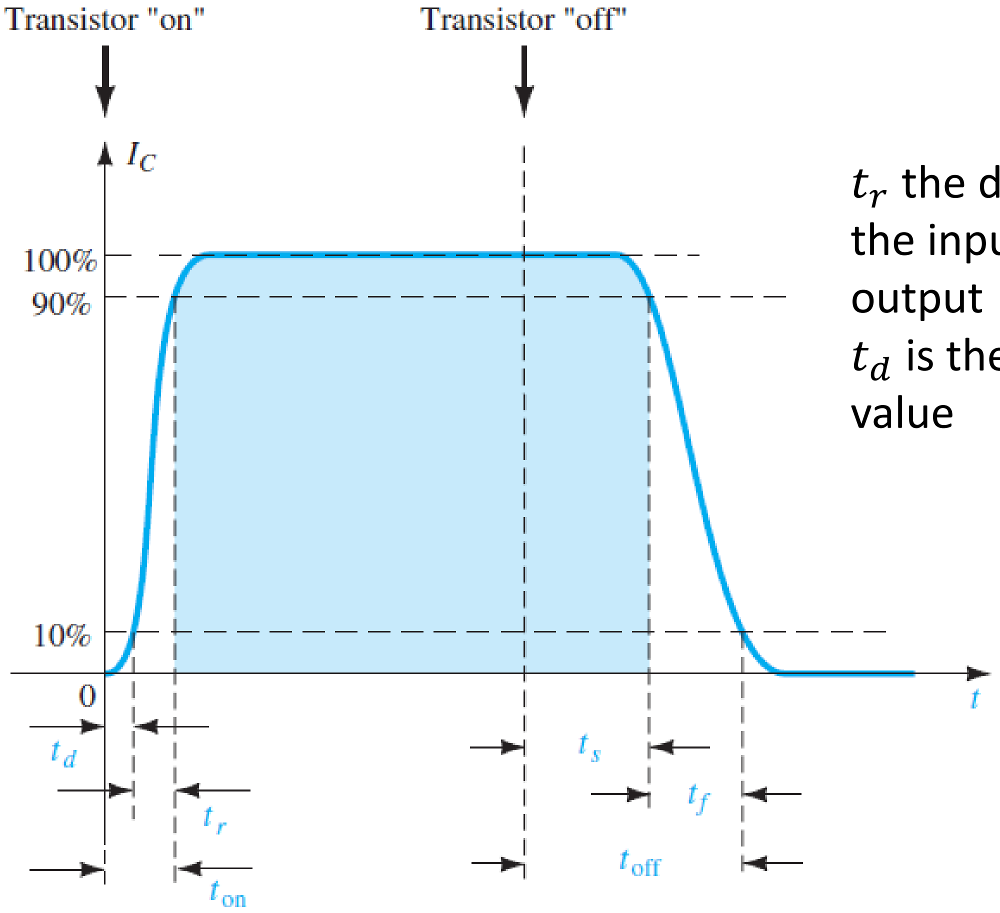
$$I_{C_{sat}} = \frac{V_{CC}}{R_C}$$

$$I_{B_{max}} \cong \frac{I_{C_{sat}}}{\beta_{dc}}$$

$$I_B > \frac{I_{C_{sat}}}{\beta_{dc}}$$

$$R_{sat} = \frac{V_{CE_{sat}}}{I_{C_{sat}}}$$

Transistor switching networks



$$t_{on} = t_r + t_d$$

t_r the delay time between the changing state of the input and the beginning of a response at the output

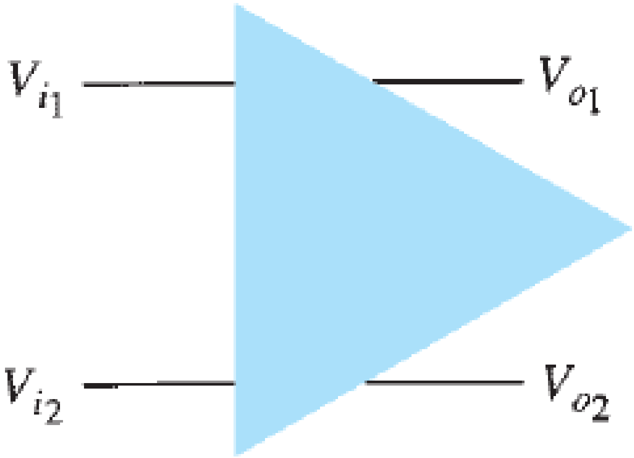
t_d is the rise time from 10% to 90% of the final value

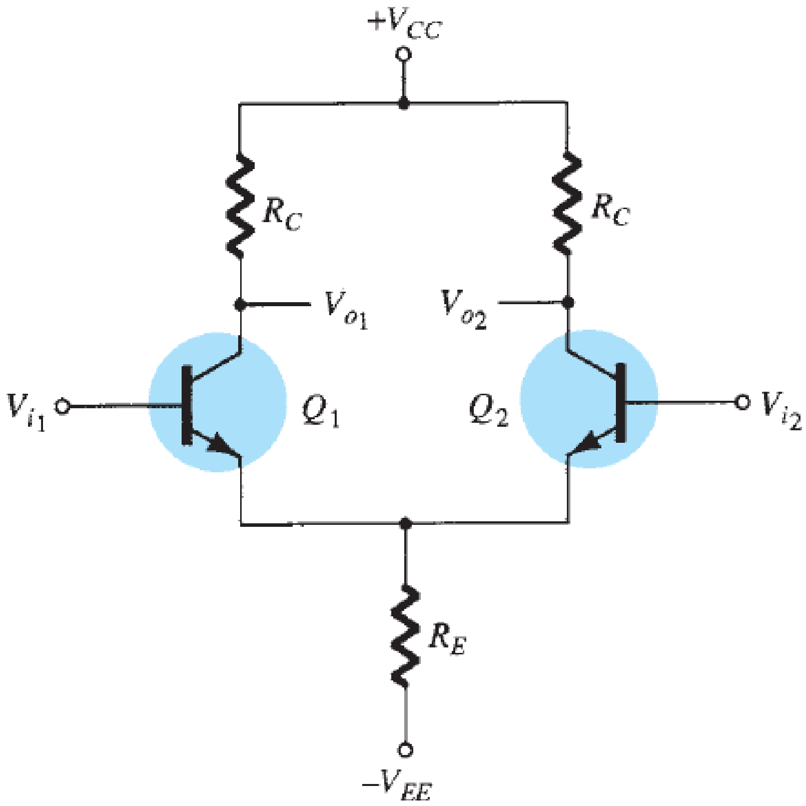
$$t_{off} = t_s + t_f$$

t_s is the storage time

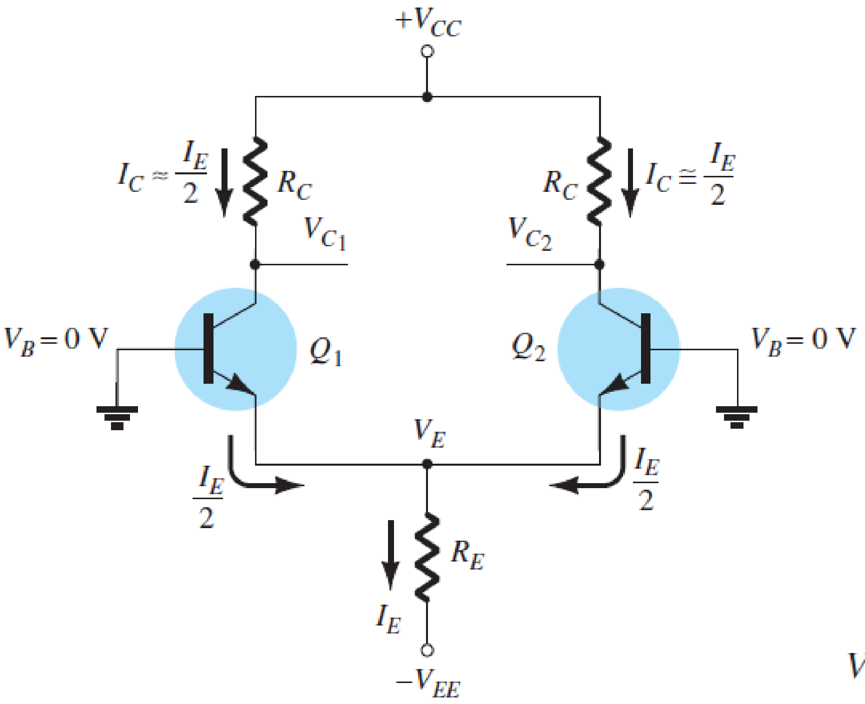
t_f the fall time from 90% to 10% of the initial value

Differential amplifier circuit





Differential amplifier circuit. DC Bias



The emitter dc bias current

$$I_E = \frac{V_E - (-V_{EE})}{R_E} \approx \frac{V_{EE} - 0.7\text{ V}}{R_E}$$

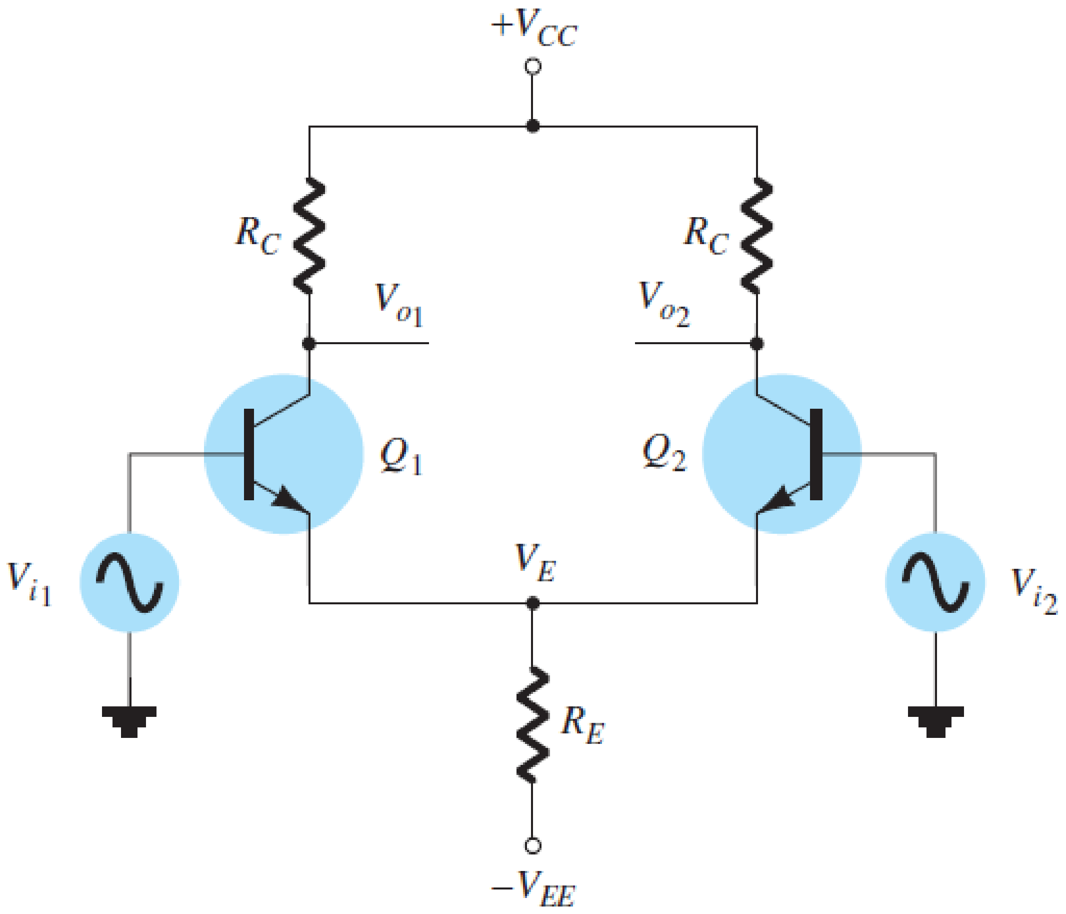
the transistors are well matched (as would occur in an IC unit)

$$I_{C_1} = I_{C_2} = \frac{I_E}{2}$$

collector voltage of

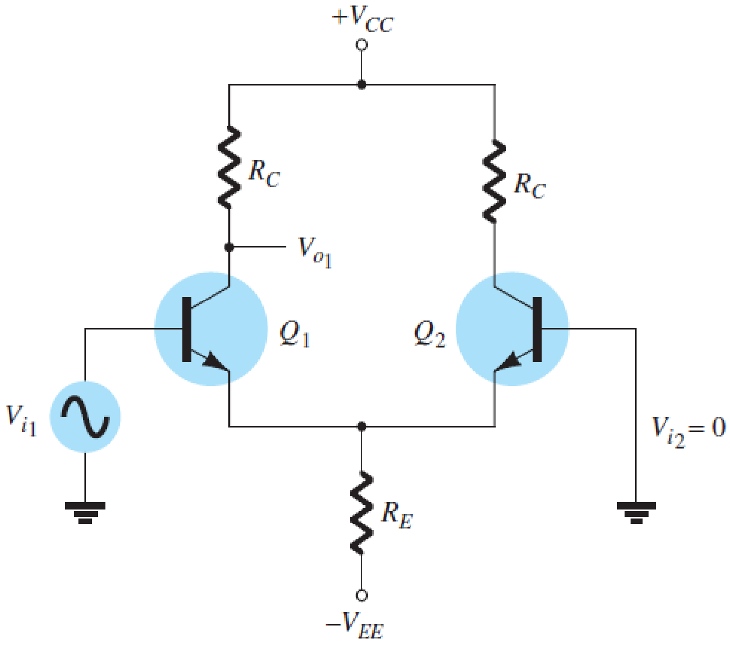
$$V_{C_1} = V_{C_2} = V_{CC} - I_C R_C = V_{CC} - \frac{I_E}{2} R_C$$

Differential amplifier circuit. AC Operation of Circuit



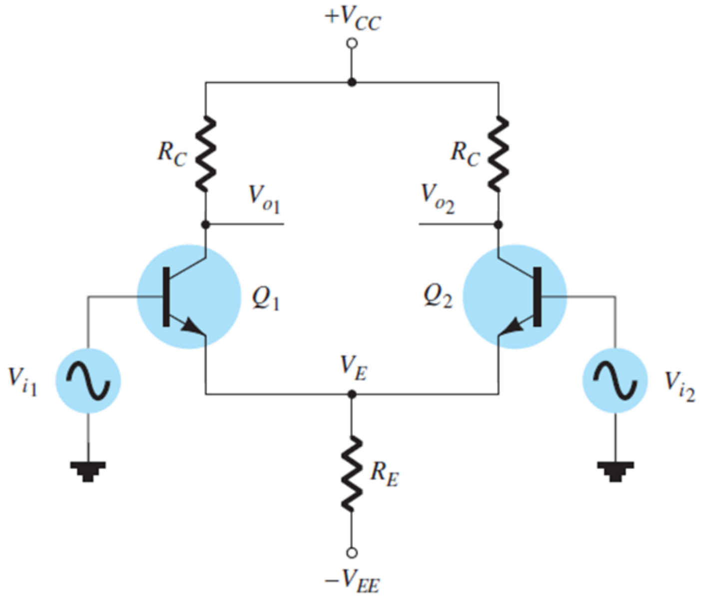
Differential amplifier circuit. AC Voltage Gain

Single-Ended



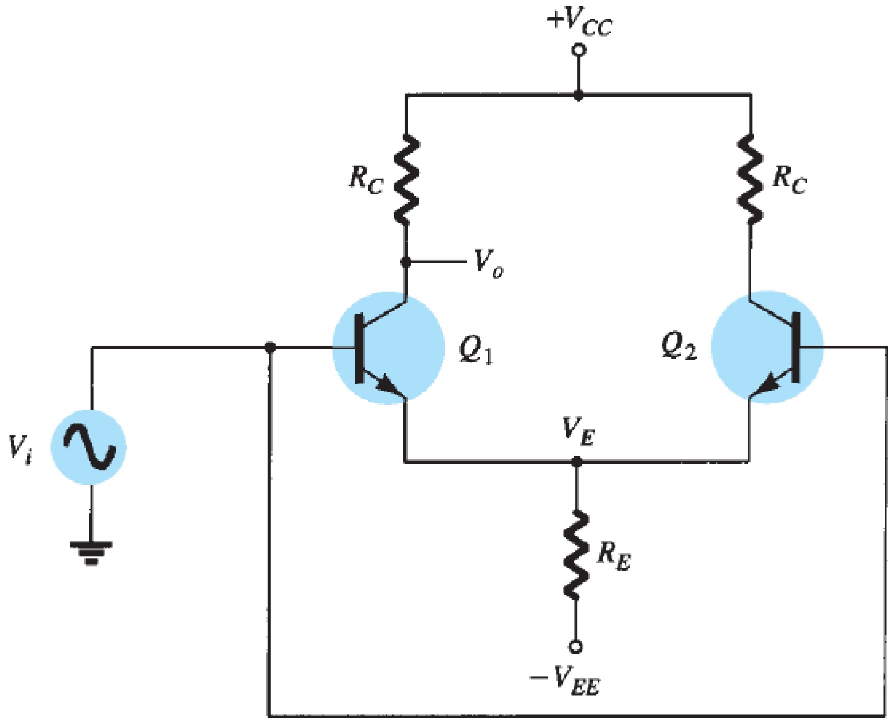
$$A_v = \frac{V_o}{V_i} = \frac{R_C}{2r_e}$$

Double-Ended



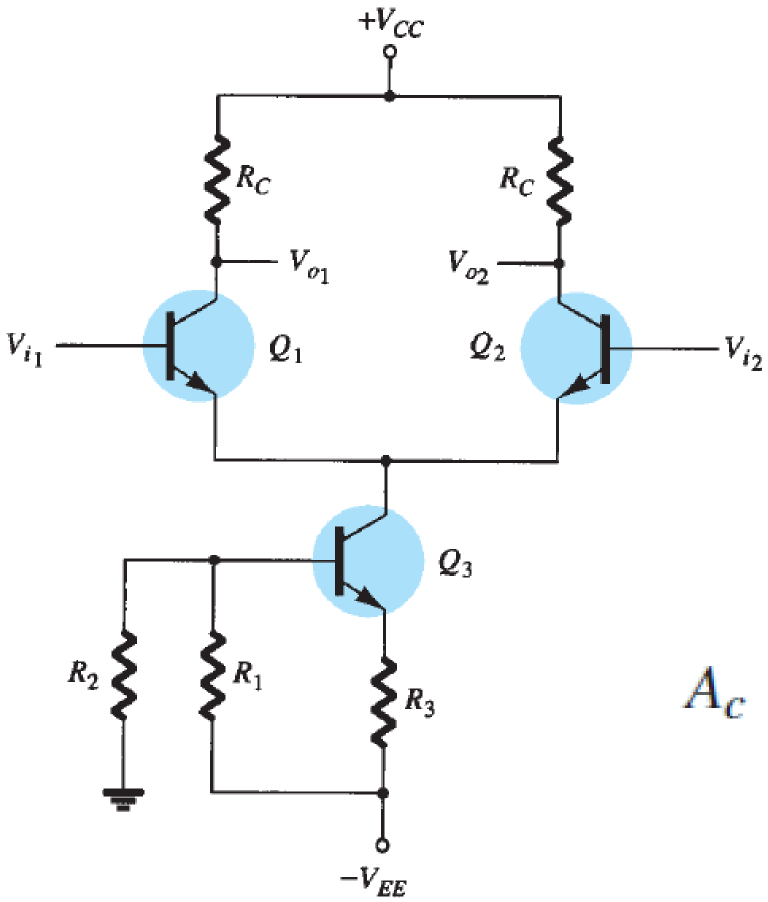
$$A_d = \frac{V_o}{V_d} = \frac{R_C}{r_e}$$

Differential amplifier circuit. Common-Mode Operation



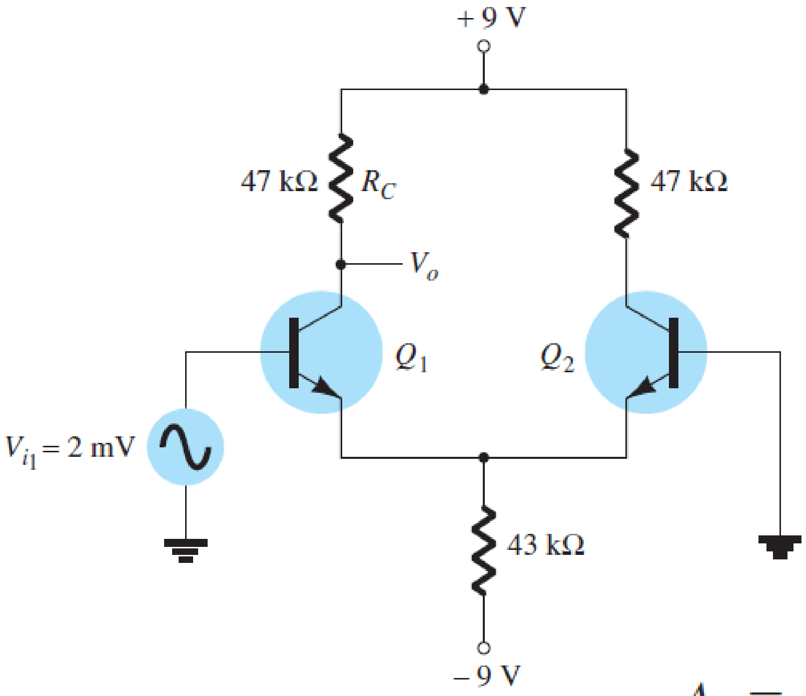
$$A_c = \frac{V_o}{V_i} = \frac{\beta R_C}{r_i + 2(\beta + 1)R_E}$$

Differential amplifier circuit. Constant-Current Source



$$A_c = \frac{V_o}{V_i} = \frac{\beta R_C}{r_i + 2(\beta + 1)R_E}$$

Differential amplifier circuit

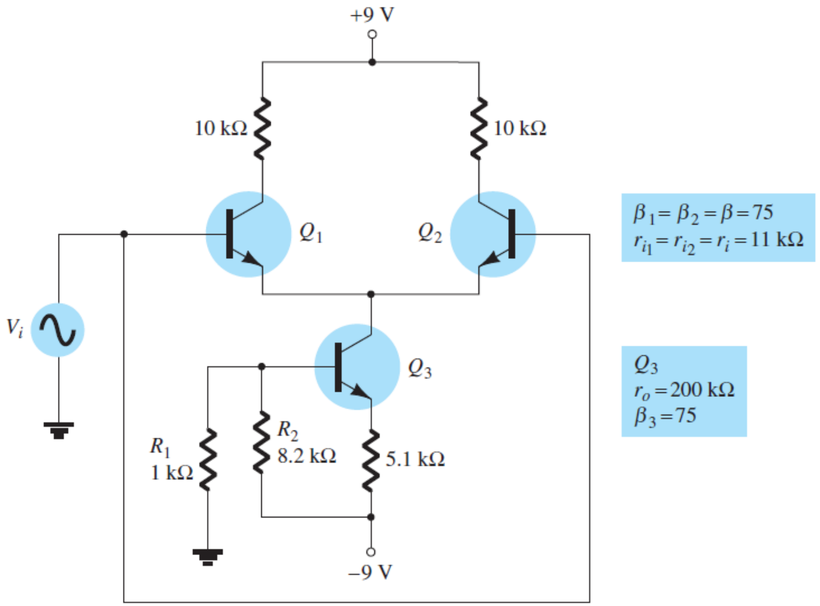


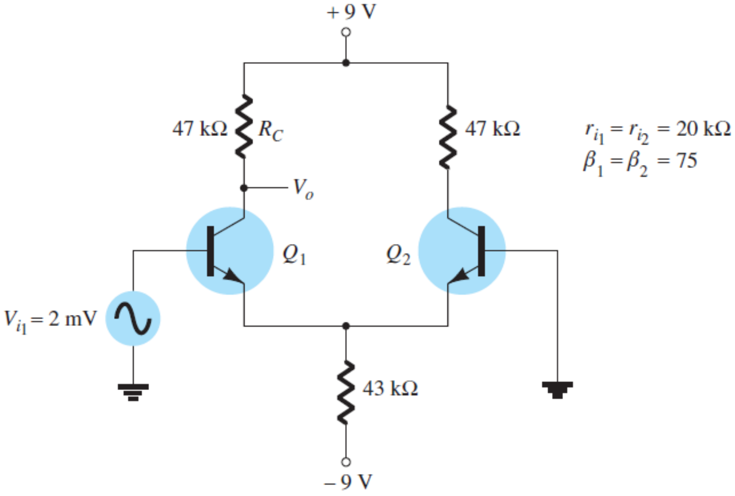
$r_{i_1} = r_{i_2} = 20\ \text{k}\Omega$
$\beta_1 = \beta_2 = 75$

$$A_v = \frac{R_C}{2r_e} = \frac{(47\ \text{k}\Omega)}{2(269\ \Omega)} = 87.4$$

$$A_c = \frac{\beta R_C}{r_i + 2(\beta + 1)R_E} = \frac{75(47\ \text{k}\Omega)}{20\ \text{k}\Omega + 2(76)(43\ \text{k}\Omega)} = \mathbf{0.54}$$

Differential amplifier circuit





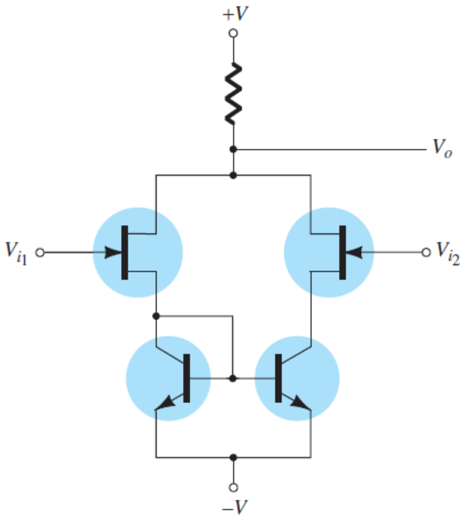
$$A_c = \frac{\beta R_C}{r_i + 2(\beta + 1)R_E} = \frac{75(47\ \text{k}\Omega)}{20\ \text{k}\Omega + 2(76)(43\ \text{k}\Omega)} = \mathbf{0.54}$$

$$A_c = \frac{\beta R_C}{r_i + 2(\beta + 1)R_E} = \frac{75(10\ \text{k}\Omega)}{11\ \text{k}\Omega + 2(76)(200\ \text{k}\Omega)} = \mathbf{24.7 \times 10^{-3}}$$

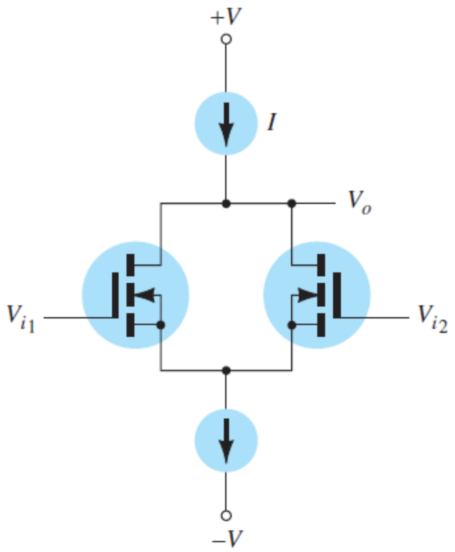
Differential amplifier circuit

BiFET, BiMOS, AND CMOS DIFFERENTIAL AMPLIFIER CIRCUITS

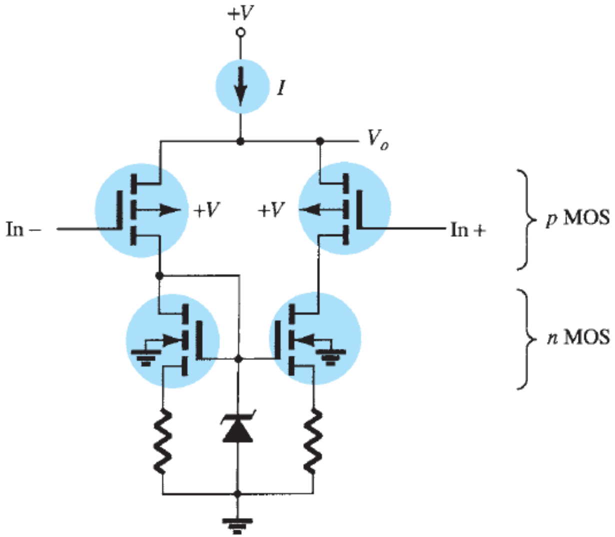
BiFET differential amplifier circuit



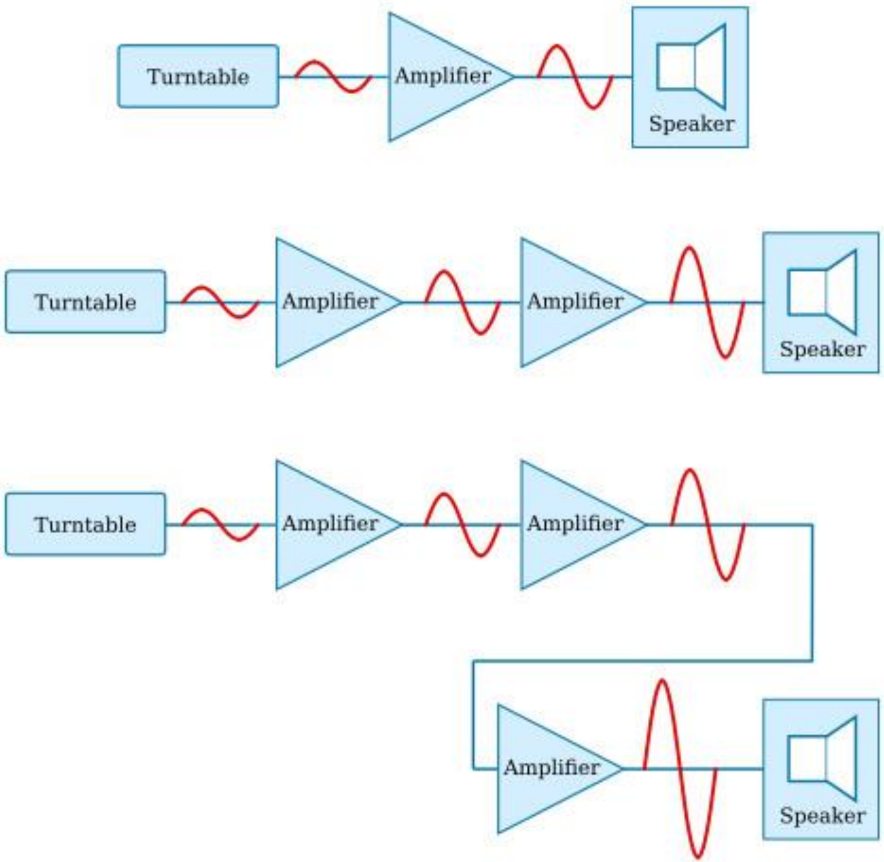
BiMOS differential amplifier circuit.



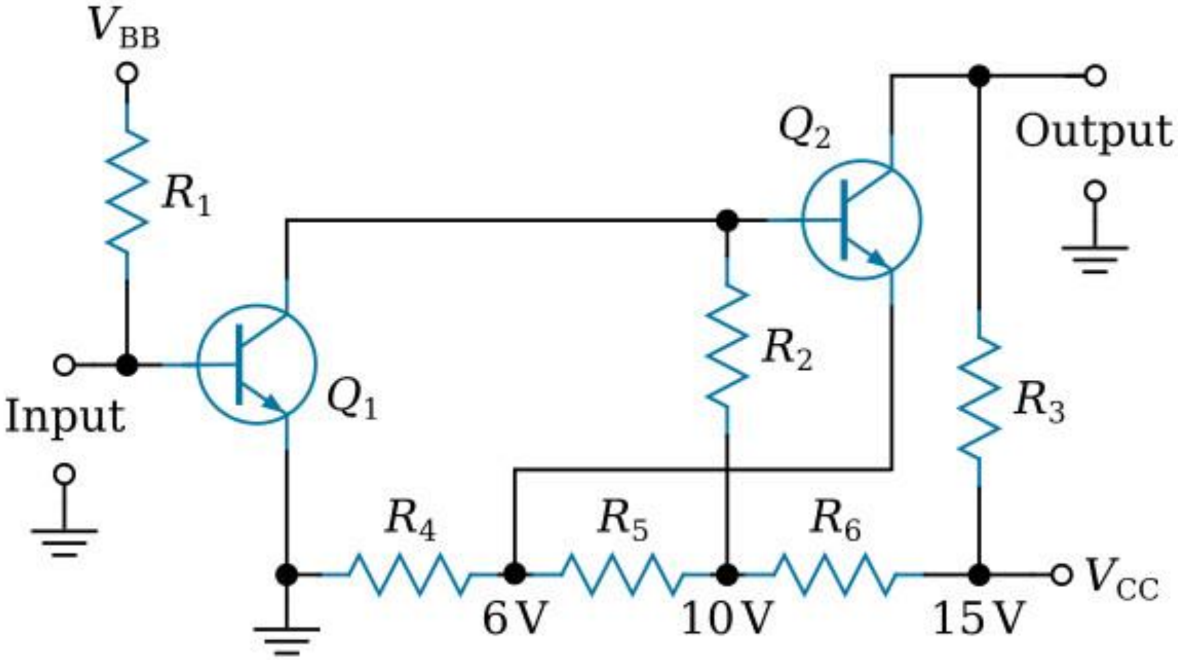
CMOS differential amplifier

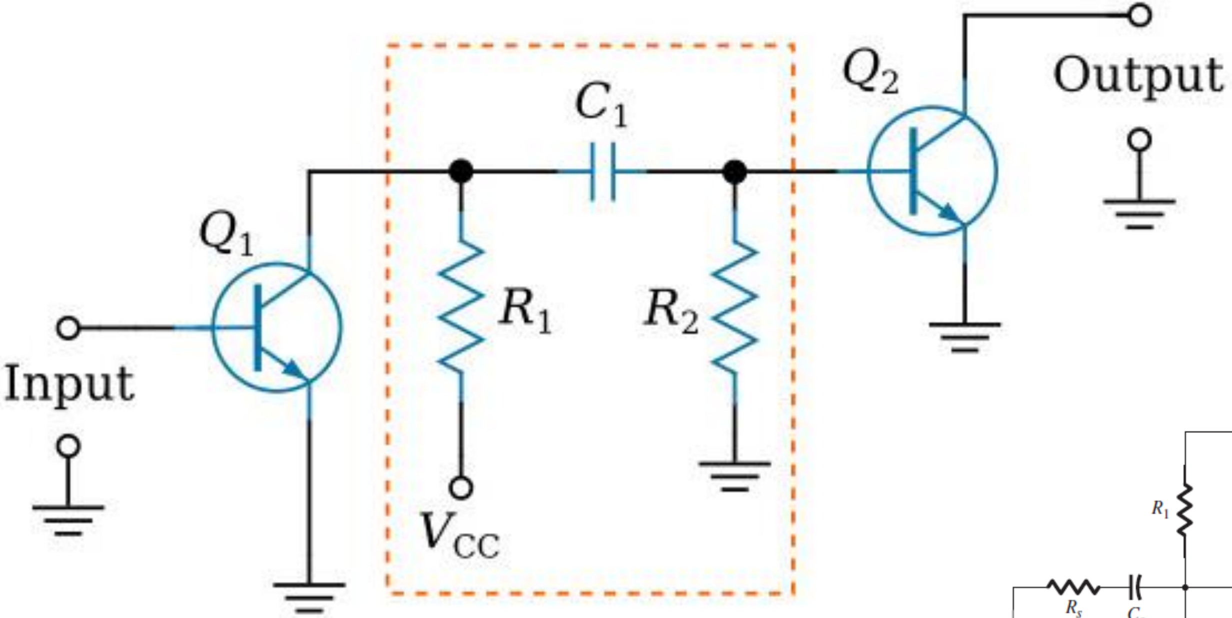


Amplifier Coupling

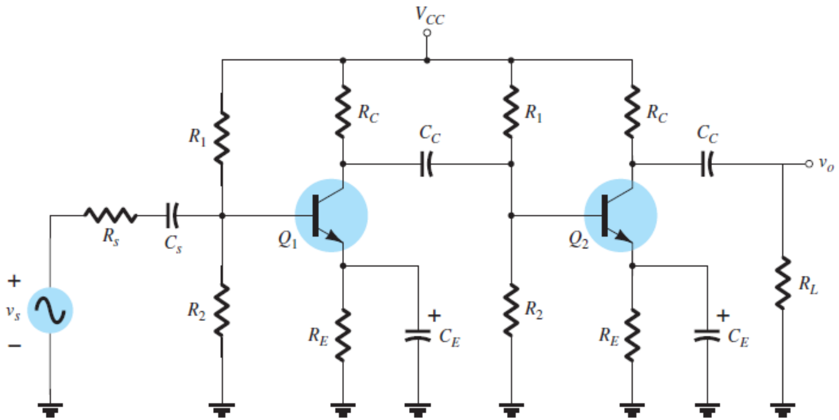


Direct Coupling



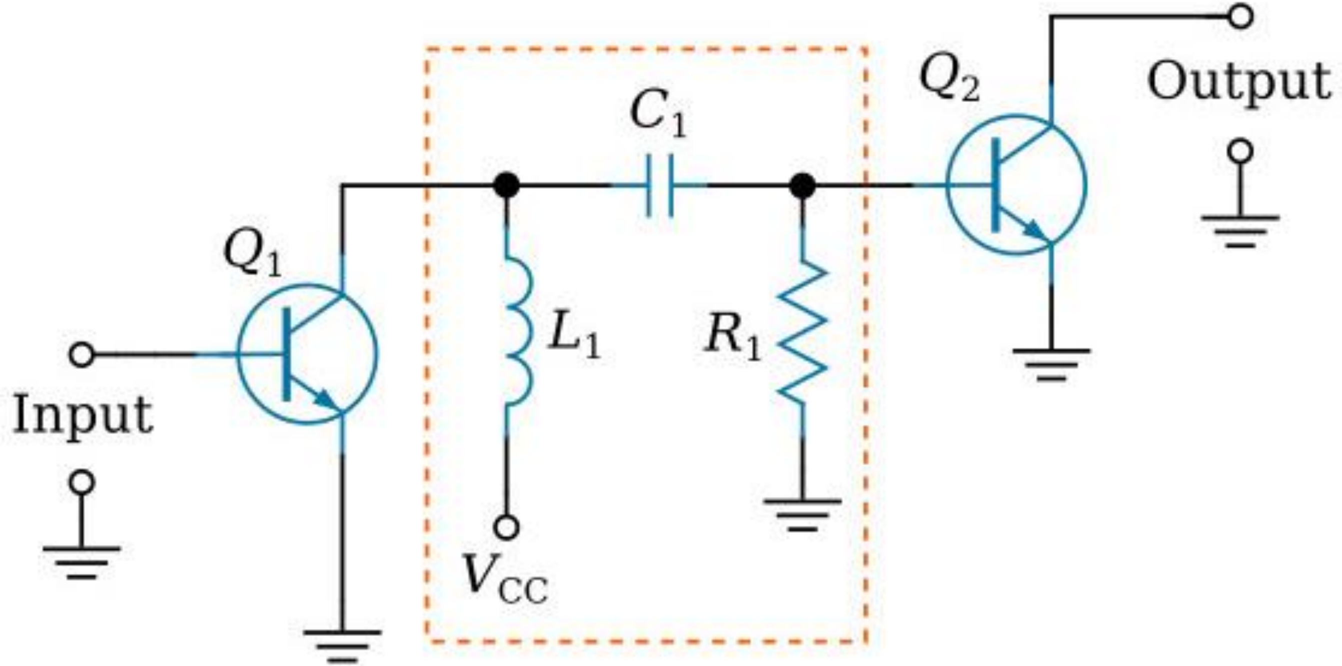


Q_1
Input
R_1
C_1
R_2
V_{CC}
Q_2
Output

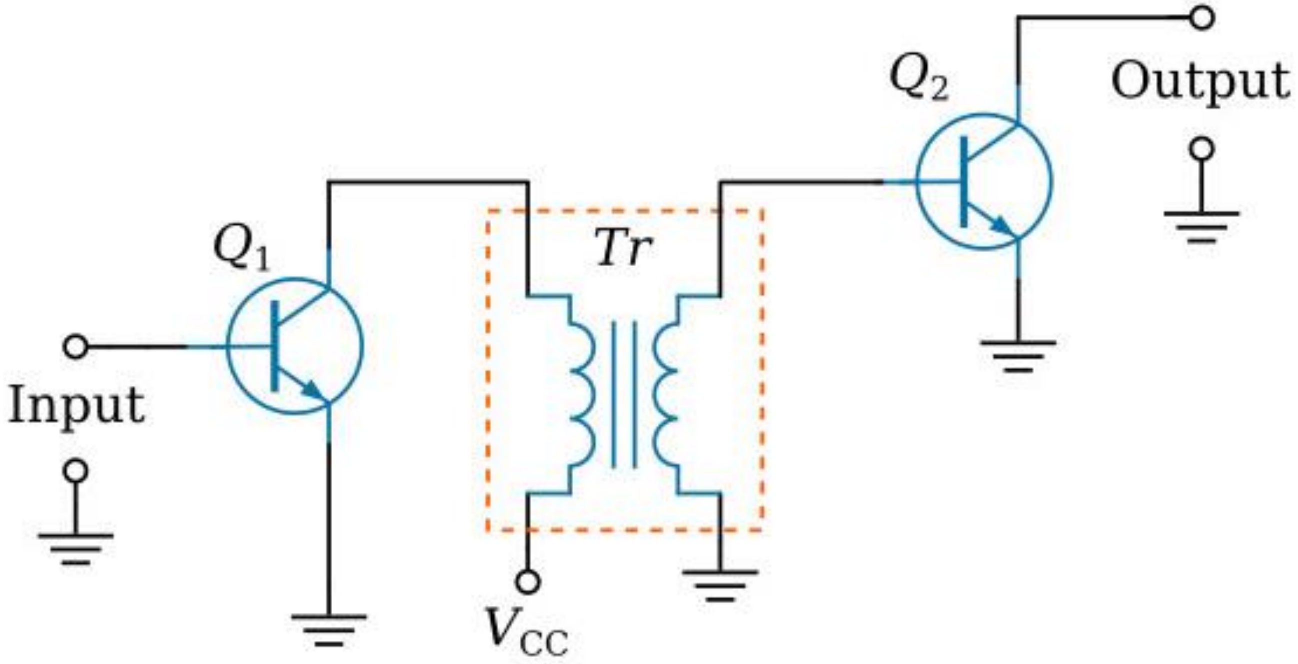


V_{CC}
R_1
R_C
C_C
R_1
R_C
C_C
v_o
R_s
C_s
Q_1
Q_2
+
v_s
−
R_2
R_E
+
C_E
R_2
R_E
+
C_E
R_L

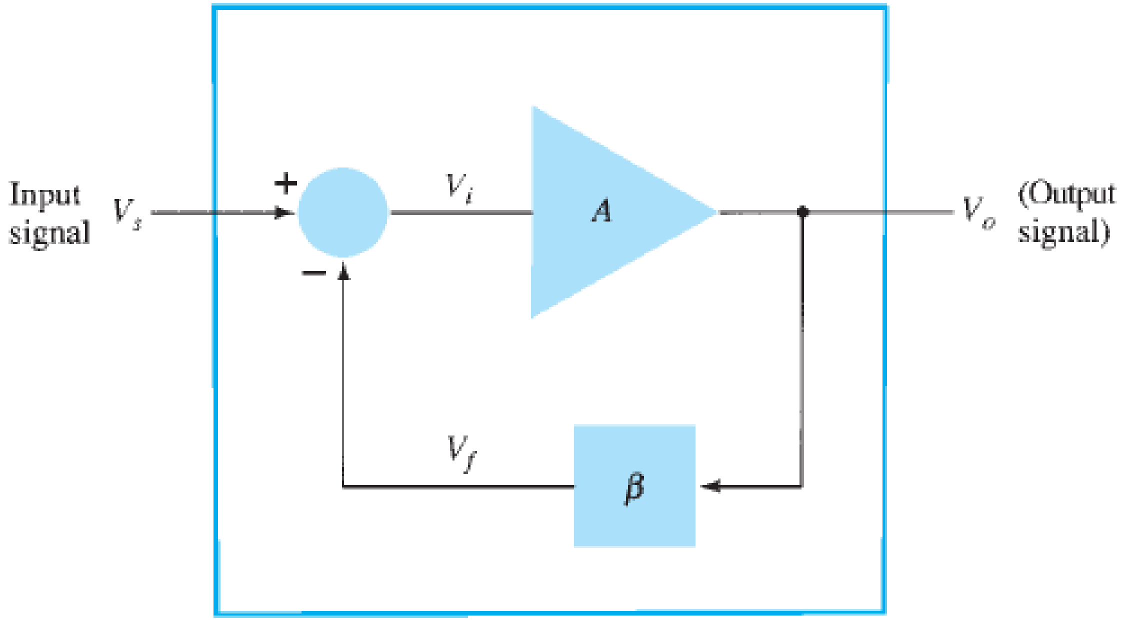
Impedance Coupling



Transformer Coupling

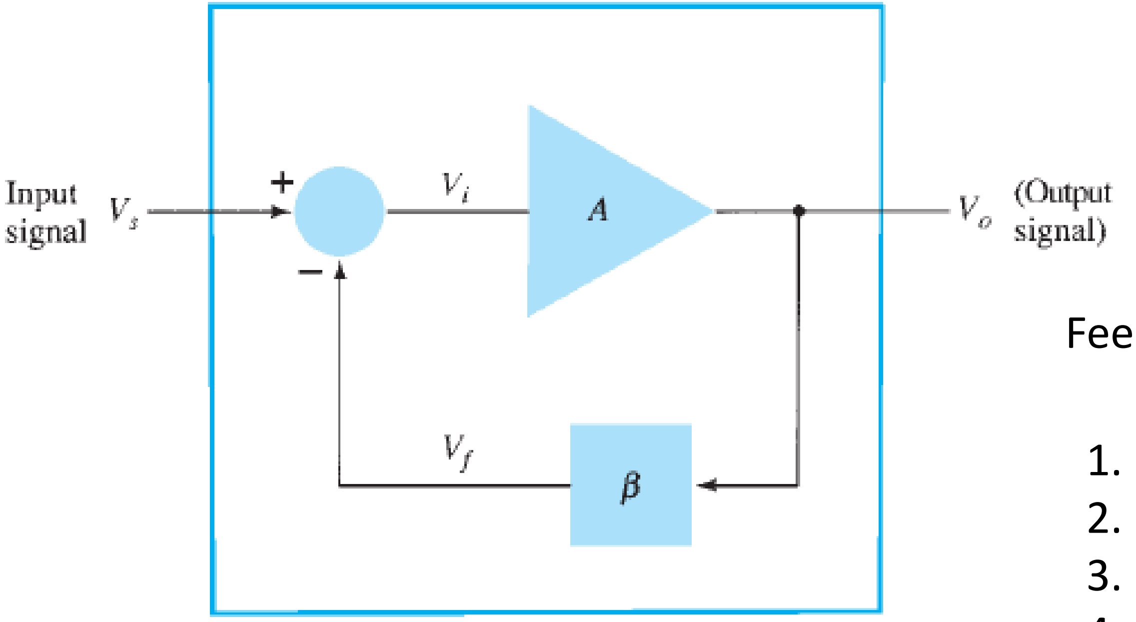


Feedback concepts



Feedback amplifier

Feedback concepts

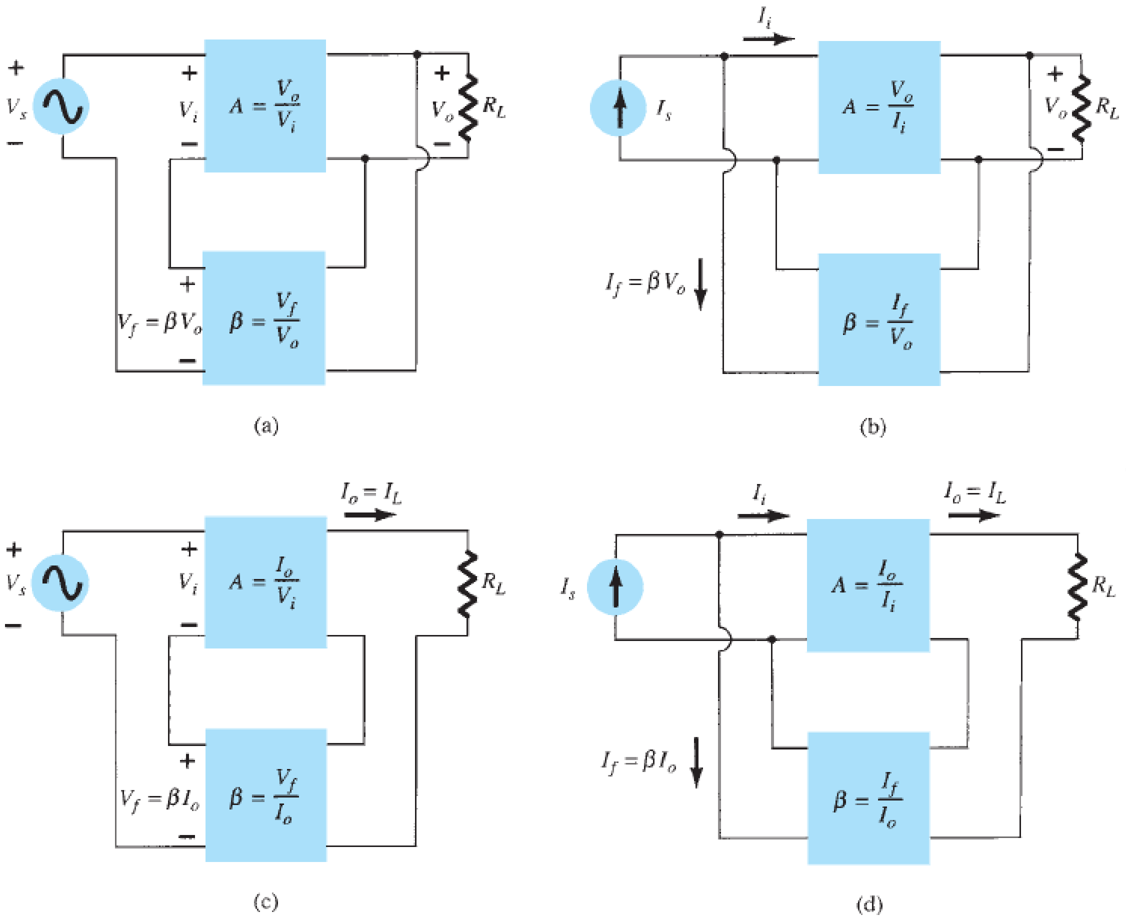


Feedback amplifier

Feedback improvements

1. Higher input impedance.
2. Better stabilized voltage gain.
3. Improved frequency response.
4. Lower output impedance.
5. Reduced noise.
6. More linear operation.

Feedback connection types



1. Voltage-series feedback (a)
2. Voltage-shunt feedback (b).
3. Current-series feedback (c).
4. Current-shunt feedback (d).

Gain with Feedback

		Voltage-Series	Voltage-Shunt	Current-Series	Current-Shunt
Gain without feedback	A	$\dfrac{V_o}{V_i}$	$\dfrac{V_o}{I_i}$	$\dfrac{I_o}{V_i}$	$\dfrac{I_o}{I_i}$
Feedback	β	$\dfrac{V_f}{V_o}$	$\dfrac{I_f}{V_o}$	$\dfrac{V_f}{I_o}$	$\dfrac{I_f}{I_o}$
Gain with feedback	A_f	$\dfrac{V_o}{V_s}$	$\dfrac{V_o}{I_s}$	$\dfrac{I_o}{V_s}$	$\dfrac{I_o}{I_s}$

Voltage-Series Feedback

$$A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A}$$

Voltage-Shunt Feedback

$$A_f = \frac{A}{1 + \beta A}$$

Effect of Feedback Connection on Impedance

Voltage-Series	Current-Series	Voltage-Shunt	Current-Shunt
Z_{if} $Z_i(1 + \beta A)$ (increased)	$Z_i(1 + \beta A)$ (increased)	$\frac{Z_i}{1 + \beta A}$ (decreased)	$\frac{Z_i}{1 + \beta A}$ (decreased)
Z_{of} $\frac{Z_o}{1 + \beta A}$ (decreased)	$Z_o(1 + \beta A)$ (increased)	$\frac{Z_o}{1 + \beta A}$ (decreased)	$Z_o(1 + \beta A)$ (increased)

Effect of Feedback Connection

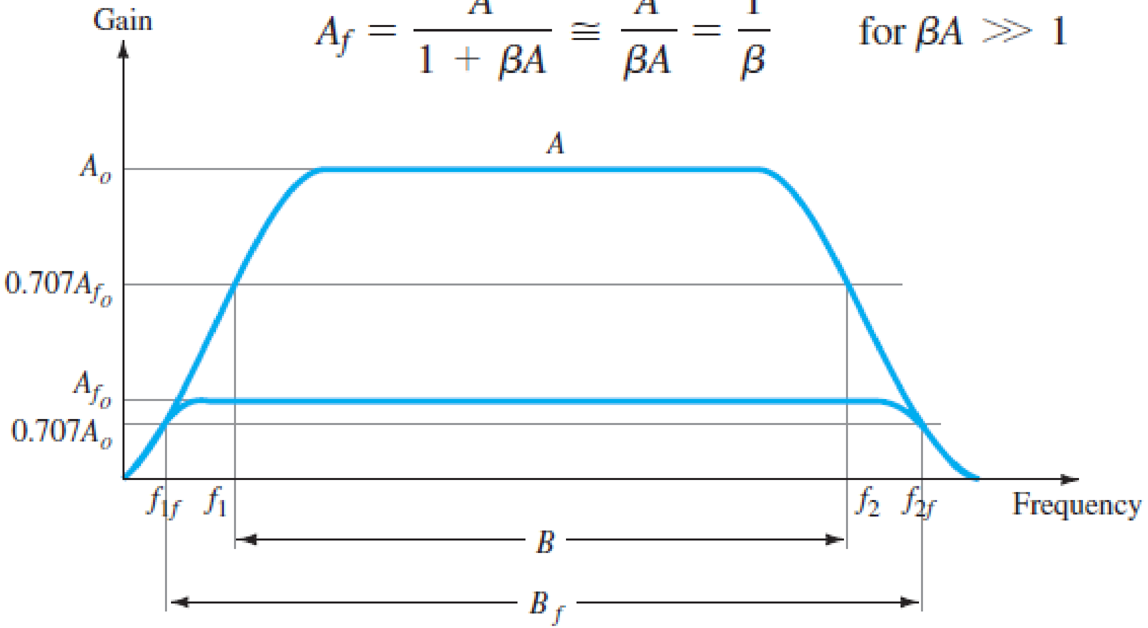
Reduction in Frequency Distortion

Reduction in Noise and Nonlinear Distortion

Effect of Negative Feedback on Gain and Bandwidth

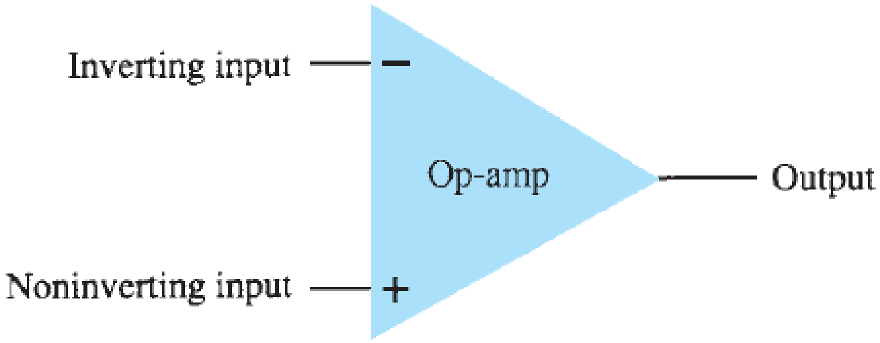
$$A_f = \frac{A}{1 + \beta A} \cong \frac{A}{\beta A} = \frac{1}{\beta} \quad \text{for } \beta A \gg 1$$

$$1 + \beta A$$



OPERATIONAL AMPLIFIERS (OP-AMP)

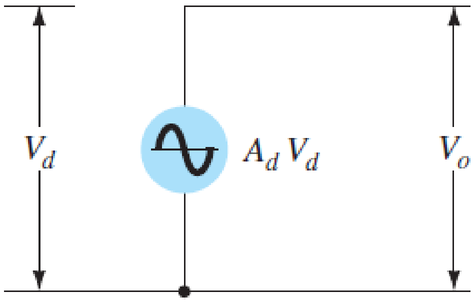
OP-AMP BASICS



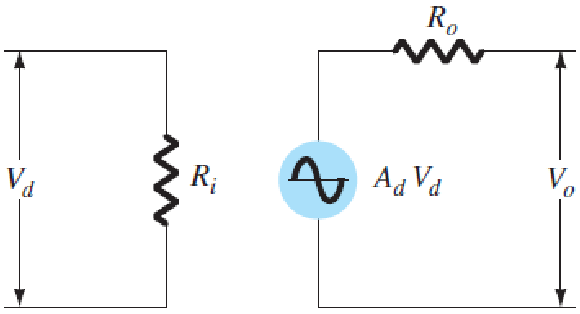
$$V_{out} = K(V_+ - V_-)$$

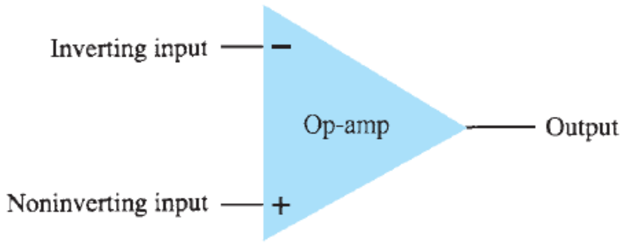
AC equivalent of op-amp circuit

ideal

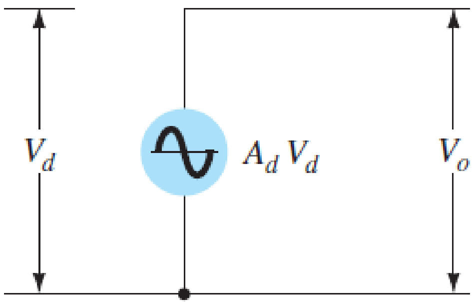


practical





ideal



IDEAL OP AMP ATTRIBUTES

- ✓ Infinite Differential Gain
- ✓ Zero Common Mode Gain
- ✓ Zero Offset Voltage
- ✓ Zero Bias Current
- ✓ Infinite Bandwidth

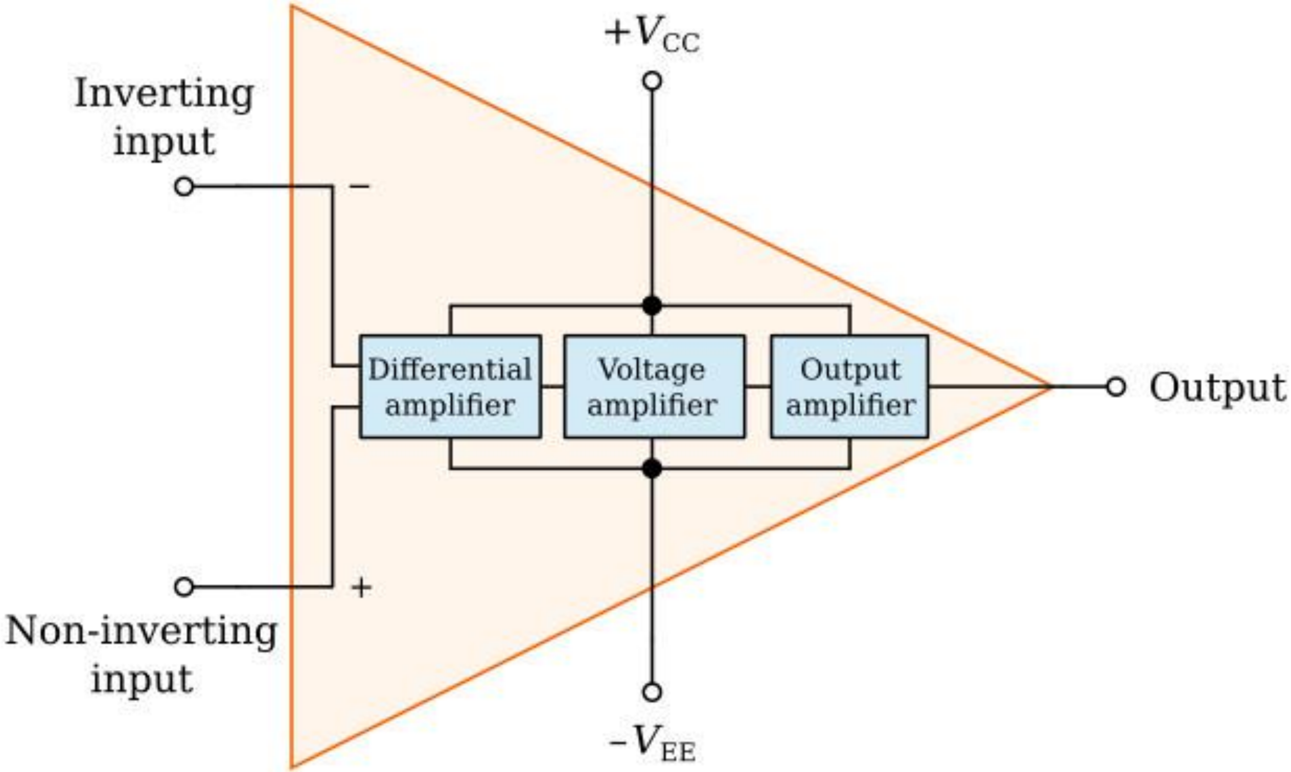
OP AMP INPUT ATTRIBUTES

- ✓ Infinite Impedance
- ✓ Zero Bias Current
- ✓ Respond to Differential Voltages
- ✓ Do Not Respond to Common Mode Voltages

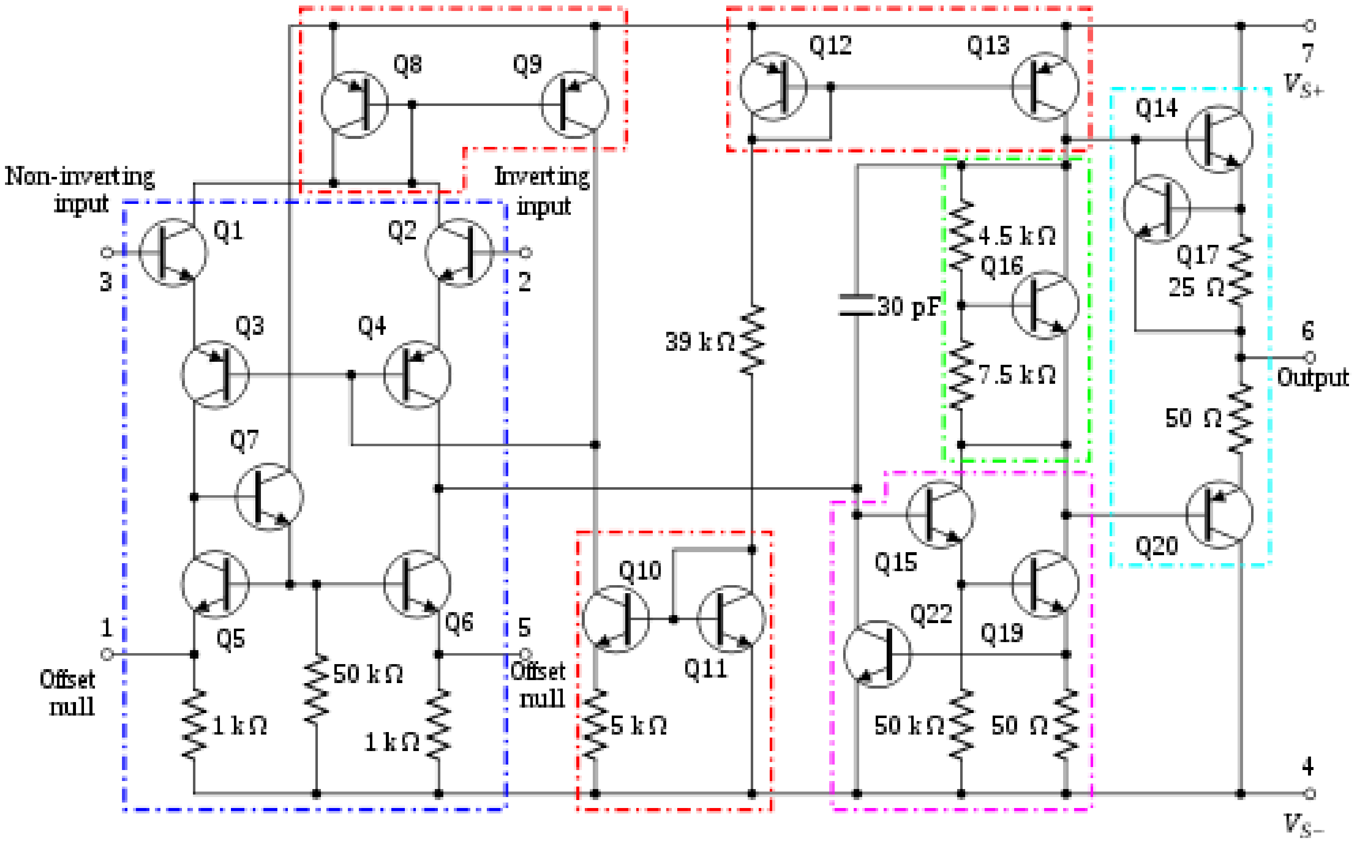
OP AMP OUTPUT ATTRIBITES

- ✓ Zero Impedance

Block Diagram



OP-AMP BASICS



A component-level diagram of the common 741 op amp.

Dotted lines outline:

current mirrors;

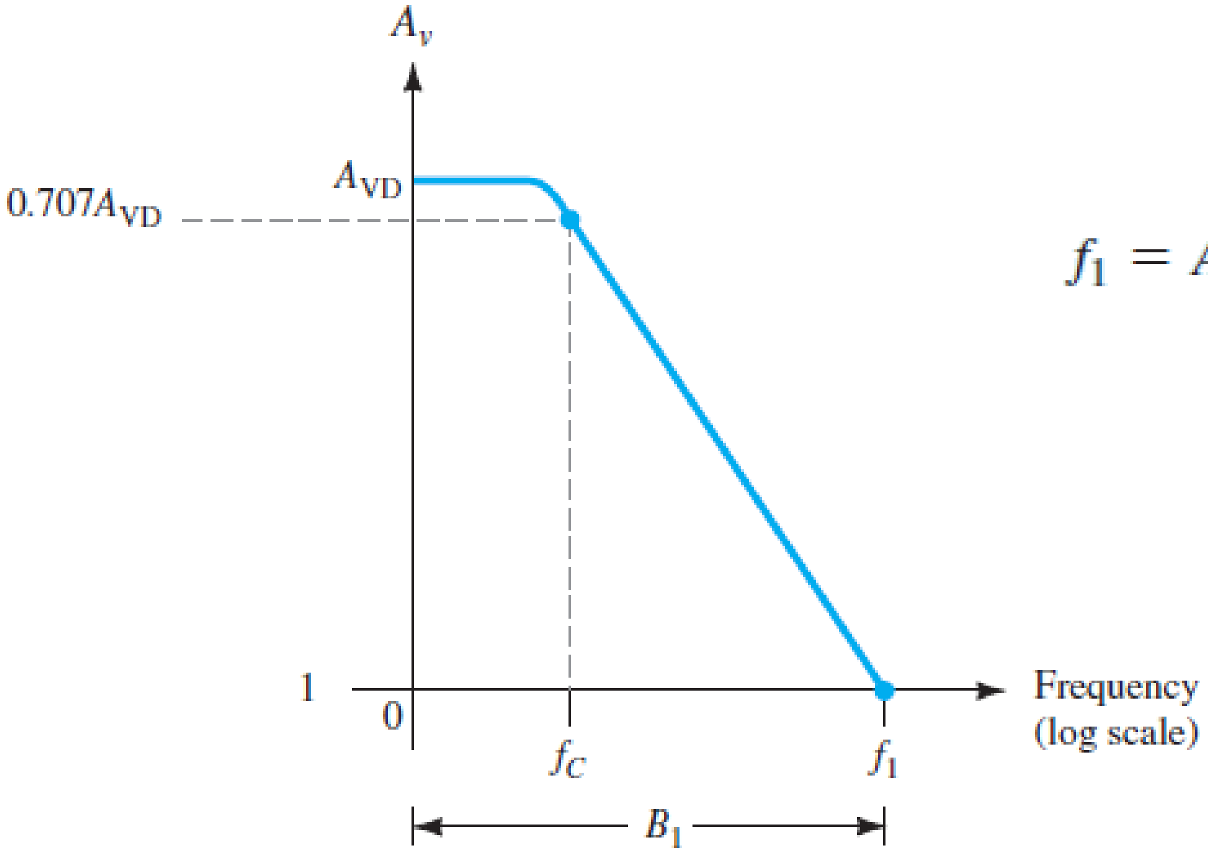
differential amplifier;

class A gain stage;

voltage level shifter;

output stage.

Gain–Bandwidth



$$f_1 = A_{VD} f_C$$

Slew Rate (SR)

Slew rate = maximum rate at which amplifier output can change in volts per microsecond ($V/\mu s$)

Slew rate calculation & formula

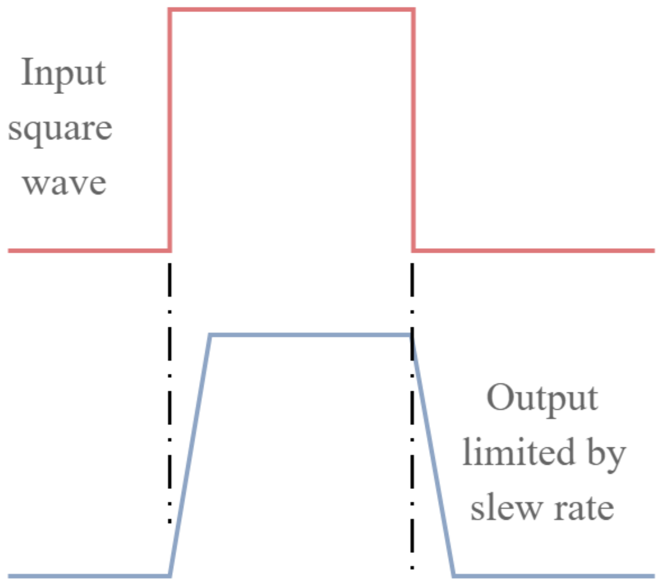
$$\mathrm{SR} = \frac{\Delta V_o}{\Delta t}\ \mathrm{V}/\mu\mathrm{s} \quad \text{or} \quad SR = 2\pi f V$$

Where

Slew Rate (*SR*) is measured in volts / second, although actual measurements are often given in v/µs

f – the highest signal frequency, Hz

V – the maximum peak voltage of the signal.



Maximum Signal Frequency

The maximum frequency at which an op-amp may operate depends on both the bandwidth (BW) and slew rate (SR) parameters of the op-amp. For a sinusoidal signal of general form

$$v_o = K\sin(2\pi ft)$$

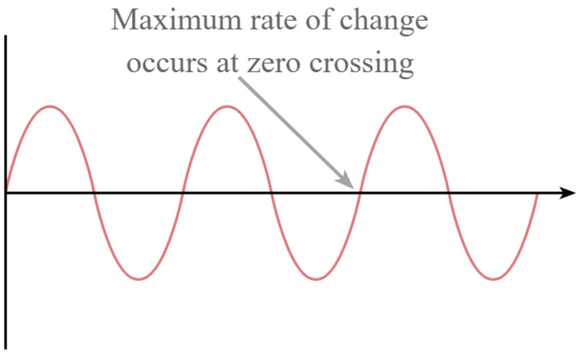
the maximum voltage rate of change can be shown to be

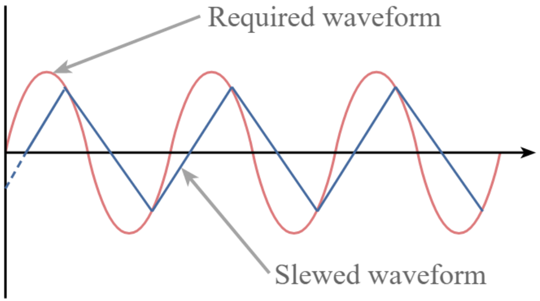
$$\text{signal maximum rate of change} = 2\pi fK\ \text{V/s}$$

To prevent distortion at the output, the rate of change must also be less than the slew rate, that is,

$$2\pi fK \le \text{SR}$$
$$\omega K \le \text{SR}$$

$$\boxed{\begin{array}{ll} f \le \dfrac{\text{SR}}{2\pi K} & \text{Hz} \\ \omega \le \dfrac{\text{SR}}{K} & \text{rad/s} \end{array}}$$





Differential and common-mode operation

Differential Inputs $V_d = V_{i_1} - V_{i_2}$

Common Inputs $V_c = \frac{1}{2}(V_{i_1} + V_{i_2})$

Output Voltage $V_o = A_d V_d + A_c V_c$

Common-Mode Rejection Ratio $\mathrm{CMRR} = \frac{A_d}{A_c}$

References

1. Sarma M. S. Introduction to electrical engineering. – New York : Oxford University Press, 2001. – C. 715-716.
2. Boylestad, Robert L. Electronic devices and circuit theory / Robert L. Boylestad, Louis Nashelsky.—11th ed.
3. ISBN 978-0-13-262226-4Scherz P., Monk S. Practical electronics for inventors. – McGraw-Hill Education, 2016.
4. Horowitz, Paul, and Winfield Hill. "The Art of Electronics. 3rd." *New York, NY, USA: University of Cambridge* (2015).
5. All about circuits (https://www.allaboutcircuits.com/)
6. https://www.electronics-tutorials.ws/
7. https://en.wikipedia.org/

Thank you for your attention!