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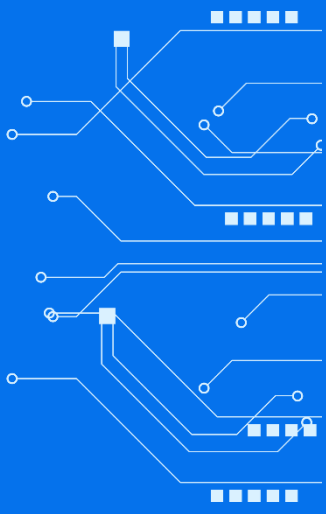
Product Data Sheet

V 1.2 2021/3/24

S3KM111L

Smart mmWave Sensor Series



矽典微 | 南京 上海 苏州

www.iclegend.com | support@iclegend.com

Version History

Version	Date	Contents
1.0	2020/7/24	Initial official release
1.01	2020/9/1	Update frequency range Update the table for Doppler FFT Update the diagram for Doppler FFT
1.02	2020/9/24	Update I^2C timing diagram Add digital data output notice in application tips
1.1	2021/1/28	Update package description and introduction of cascade mode
1.2	2021/3/24	Update Range FFT, Doppler FFT, Doppler FFT Peak data format

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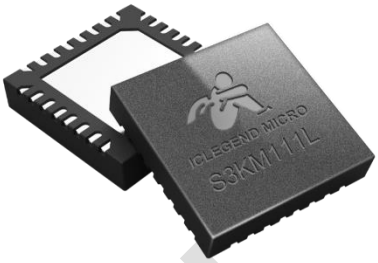
S3KM111L



1 Device Overview

1.1 Main Features

- 24GHz K-band highly integrated FMCW radar sensor SoC
- Up to 1GHz bandwidth FM tuning range
- One transmit channel and one receive channel
- Integrated signal generator and low phase noise PLL
- On-chip 16bits ADCs in receiver
- Hardware accelerator for filtering and FFT
- Integrated temperature sensor
- TX maximum output power: 12dBm
- RX noise figure: 10.5dB
- Phase noise@ 1MHz offset: -97dBc/Hz
- Command I^2C/SPI/UART for chip configuration
- Data SPI/UART for serialized data output
- Single power supply voltage 3.3V
- 4 x 4 mm^2 QFN32 package
- Junction temperature range of –40ºC to 105ºC

1.2 Applications


Motion / Body presence detection


Range / velocity measurement


Gesture recognition


Vital signs monitoring

Figure 1-1 Smart mmWave Sensor's Applications

2 Table of Contents

3 General Description

3.1 Block Diagram

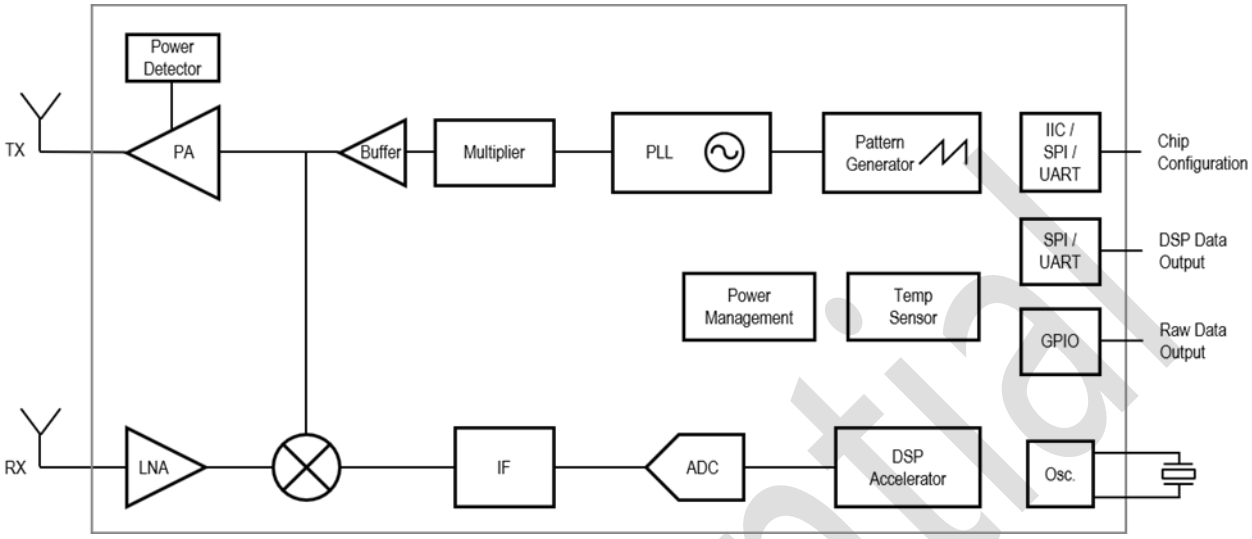


Figure 3-1 S3KM111L Diagram

3.2 Description

The S3KM111L is an integrated single chip mmWave sensor SoC based on FMCW radar technology. It works at 24GHz K-band with up to 1GHz modulation bandwidth in each single frequency sweeping chirp.

The device includes a fully K-band RF transceiver, driven by on-chip pattern generator and PLL. The pattern generator supports multiple frequency sweeping modes with different time-frequency waveforms, e.g. saw-tooth and triangular waveforms. The pattern generator and PLL support fast chirp mode up to 8kHz chirp rate.

The RF and analog subsystem contain one transmitter (TX) and one receiver (RX). Gain controls are applied to both transmitter and receiver to adjust the whole link budget to work in different scenarios. IQ basebands including inter-mediate frequency (IF) amplifiers, filters and ADCs are integrated for the receivers. A built-in DSP accelerator may process the IQ ADC's raw data with FFT or Doppler FFT. The processed data can be serialized outputted through SPI or UART interface.

The S3KM111L requires only a few external components with simple configuration，e.g. the external crystal oscillator and stabilization capacitors due to its high level of integration. Even it can work with a single power supply at 3.3V with the internal power management engine, and the device is fully configurable via I^2C/SPI/UART interfaces. The S3KM111L is an ideal solution for low power, ultra-compact, accurate sensor systems in the AIoT market area.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings [1]

Parameter	Pin Names	Comments	Min	Max	Unit
3.3V power supply	VDD, VDD_A		-0.5	3.7	V
1.6V power supply (when internal DCDC is bypassed)	V_T, V_R, V_A, V_D	Connect to the external power management unit in internal DCDC bypassed mode.	-0.5	3.7	V
RF input voltage	RX, RF_RES_2		-0.32	0.32	V
RF output voltage	TX, RF_RES_1		-2.0	2.0	V
Analog IO voltage	PLL_VC, REXT, XIN, XOUT, DCDC_SW		-0.5	3.7	V
Digital IO voltage	RSTN, I^2C_SDA, I^2C_SCL, C_SPI_MOSI, C_SPI_CSN, RAW_CLK, UART_TXD, SPI_CSN, SPI_MOSI_0, DIG_RES, SPI_SCLK		-0.5	3.7	V
T_j		Operating junction temperature	-40	105	°C

[1] Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability. All integrated circuits need be handled with appropriate care to avoid damages due to ESD.

4.2 ESD Ratings

Table 4-2 ESD Ratings

Model		Vaule	Unit
V_{ESD}	HBM: Human body model	+/- 4000[1]	V
	CDM: Charge device model	+/-1000[2]	V
	MM: Machine Mode	+/- 200[3]	V

[1] Class 3A according ANSI/ESDA/JEDEC standard, Method JS-001-2017

[2] Class C3 according ANSI/ESDA/JEDEC standard, Method JS-002-2014

[3] Class B according JEDEC standard, Method A115-C

4.3 Thermal Resistance

Table 4-3 Thermal Resistance

Parameter	Description	Min	Typ	Max	Units
$R_{\theta JA}$	The junction-to-ambient thermal resistance			47	°C/W

$T_j = T_A + R_{\theta JA} \times P_{total}$, where P_{total} is the power consumption of the chip and T_A is the environment temperature in the still air.

4.4 Recommended Operating Conditions

Table 4-4 Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
VDD_A	3.3V power supply for analog circuits	3.0	3.3	3.6	V
VDD	3.3V power supply for DCDC and digital I/O circuits	3.0	3.3	3.6	V
V_T, V_R, V_A, V_D	1.6V power supply when the internal DCDC is bypassed	1.5	1.6	1.7	V
VIH	Voltage input High	2.3			V
VIL	Voltage input Low			0.8	V
VOH	Voltage output High	2.45			V
VOL	Voltage output Low			0.45	V
CL	Crystal load capacitance		10		pF

4.5 Power Consumption

Data in Table 4-5 are measured under 25°C environment temperature.

Table 4-5 Power Supply and Consumption

Parameter	Description	Min	Typ	Max	Unit
P_{total}	Average power consumption when internal DCDC is used, and all the circuits work at default setting mode and all the circuits are on, with 50% duty cycle chirps.		210		mW

Below data in Table 4-6 are measured under -40°C ~ 85°C environment temperature when the internal DCDC is used.

Table 4-6 Maximum Current Ratings at Power Terminals

Parameter	Supply Name	Min	Typ	Max	Unit
Current	VDD_A			23	mA
	VDD			106	mA

Below data in Table 4-7 are measured under -40°C ~ 85°C environment temperature when the internal DCDC is bypassed.

Table 4-7 Maximum Current Ratings at Power Terminals

Parameter	Supply Name	Min	Typ	Max	Unit
Current	VDD_A			22	mA
	VDD			12	mA
	V_T, V_R, V_A, V_D [1]			200	mA

[1] V_T 128mA, V_R 30mA, V_A 32mA, V_D 10mA.

4.6 Dynamic Performance

Dynamic performance data are measured under 25°C environment temperature.

4.6.1 TX Performance

Table 4-8 TX Performance

Parameter	Description	Min	Typ	Max	Units	Condition
Z_Out	TX output load impedance		50		Ω	
P_{max}_Out	TX maximum output power		12		dBm	
F_Out	TX output frequency range	24		25	GHz	
P_Out	TX output power range	-41.3		12	dBm	

4.6.2 RX Performance

Table 4-9 RX Performance

Parameter	Description	Min	Typ	Max	Units	Condition
Z_In	RX input load impedance		50		Ω	
P_{max}_RF_{in}	max power feed into RX input			0	dBm	
F_In	RX frequency range	24		25	GHz	
S_{11}_RF_{in}	RX input return loss		<-10		dB	
NF	RX noise figure		10.5		dB	SSB，including RF, analog and ADC in RX.
G_RF_{RX}	gain of RF in RX	15		31	dB	

4.6.3 Baseband Performance

Table 4-10 Baseband Performance

Parameter	Description	Min	Typ	Max	Units	Condition
Res_ADC	ADC resolution		16		bit	
Fs	ADC sampling frequency		2.5		MHz	

4.6.4 Pattern Generator and PLL Performance

Table 4-11 Pattern Generator and PLL Performance

Parameter	Description	Min	Typ	Max	Units	Condition
F_Ref	PLL input reference frequency		25		MHz	from crystal
BW_PLL	PLL bandwidth		65		kHz	with off-chip filter parameter as follow : R1=430Ω C1=22nF C2=2.2nF
PN_{1MHz}	phase noise at 1 MHz offset		-97		dBc/Hz	measured @ TX output
BW_Chirp	FMCW chirp bandwidth			1	GHz	@ TX output
R_Ramp	FMCW chirp ramp rate			15	MHz/μs	

4.7 Timing and Switching Characteristics

4.7.1 Power Up Timing and Sequence

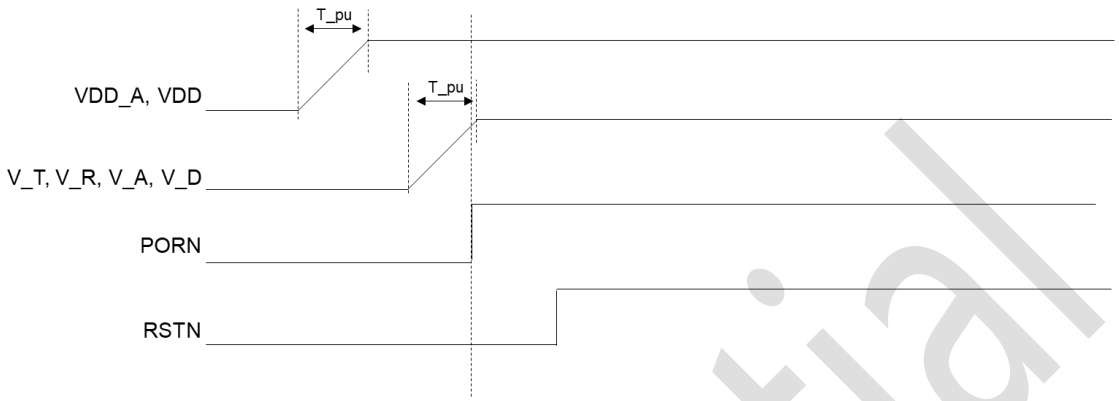


Figure 4-1 Power Up Time and Sequence

No power sequence restriction if V_T/R/A/D are supplied by internal DCDC. For internal DCDC bypass scenarios the V_T/R/A/D should be powered up after VDD if internal DCDC is bypassed. All the power up time T_pu should be between 10μs~100ms. The digital circuits are always reset until both the internal power-on reset and external reset are released.

4.7.2 I²C for Configuration

The command I²C interface is used for chip configuration. Figure 4-2 and Figure 4-3 are its write and read timing map. I²C device address can be 7'b010_0000, 7'b010_0001, 7'b010_0010 or 7'b010_0011, which is determined at reset phase. Please refer to Chapter 5.1 and 5.2 for pin description and configuration mode setup.

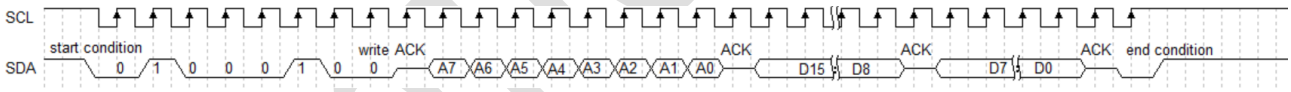


Figure 4-2 I²C Configuration Write

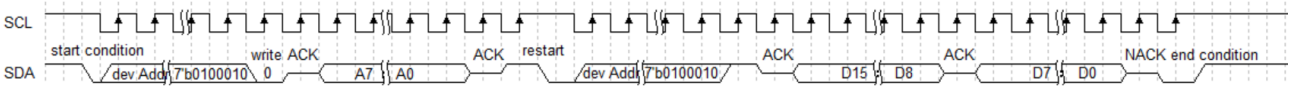


Figure 4-3 I²C Configuration Read

4.7.3 SPI for Configuration

The command SPI interface is used for chip configuration. Figure 4-4 and Figure 4-5 are its write and read timing map. Please refer to Chapter 5.1 and 5.2 for pin description and configuration mode setup.

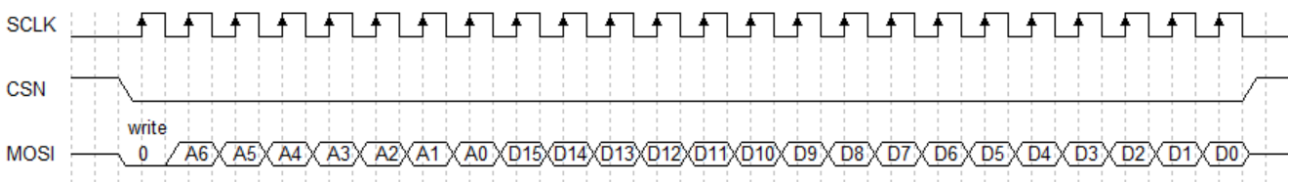


Figure 4-4 SPI Configuration Write

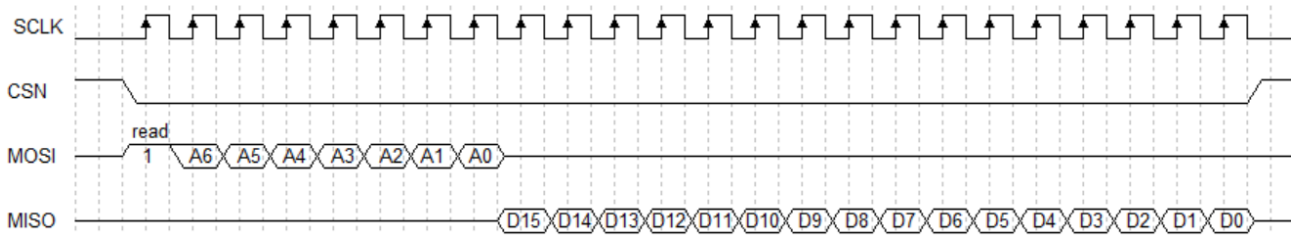


Figure 4-5 SPI Configuration Read

4.7.4 UART for Configuration

The command UART interface is used for chip configuration. Figure 4-6 and Figure 4-7 are its write and read timing map. Please refer to Chapter 5.1 and 5.2 for pin description and configuration mode setup.

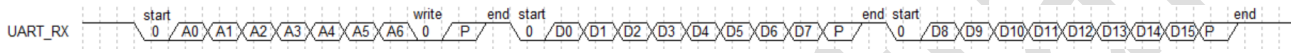


Figure 4-6 UART Configuration Write

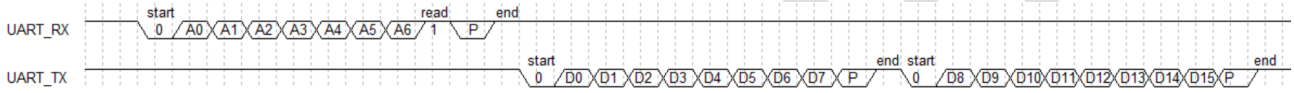


Figure 4-7 UART Configuration Read

4.7.5 SPI Output for Range FFT

When range FFT data SPI output mode is selected, the chip will transfer range FFT data with data SPI (Pin26~Pin29). Please refer to Chapter 5.1 and 5.2 for pin description and data output mode setup.

Figure 4-8 and Table 4-12 show the timing and data format. Pin27 (MOSI[0]) represents RX's data. The head and tail occupy one double word (DW). The transfer is under MSB first sequence and the Doppler FFT data type is signed integer.

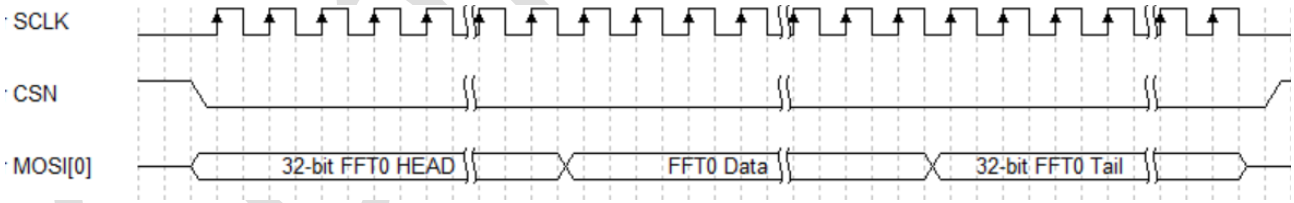


Figure 4-8 Range FFT Data Timing

Table 4-12 Range FFT Data Format

DW	Item	31:24	23:22	21:20	19:16	15:11	10:9	8:0
DW_0	Head	0xAA	0 or 1	3	fft_chirp_index[8:0]		0	cfg_fft_tx_max[8:0] +1

DW	Item	31:16	15:0
DW_1	Data	fft real data 0 [15:0]	fft imag data 0 [15:0]
:		fft real data 1 [15:0]	fft imag data 1 [15:0]
DW_{m-1}		…	…
		fft real data m-2 [15:0]	fft imag data m-2 [15:0]

DW	Item	31:16	15:14	13:12	11:8	7:0
DW_m	Tail	check_sum	0/1	3	fft_chirp_index[3:0]	0x55

[1] if MOSI[0], Head[23:22]=0 & Tail[15:14]=0; if MOSI[1], Head[23:22]=1 & Tail[15:14]=1;

[2] fft_chirp_index: indicate the chirp sequence number in one frame, start from “0” in each frame.

[3] cfg_fft_tx_max: m-1 points FFT transferred

[4] check_sum: sum of all data，which is used for optional redundancy check

4.7.6 SPI Output for Doppler FFT

When Doppler FFT data SPI output mode is selected, the chip will transfer Doppler FFT data with data SPI (Pin26~Pin29). The user can refer to Chapter 5.1 and 5.2 for pin26~pin29 description and data output mode setup, and DFFT is short for “Doppler FFT” in the following diagrams and tables.

Figure 4-9 and Table 4-13 show the timing and data format. Pin27 (MOSI[0]) represents RX’s data. The head and tail occupy one double word (DW). The transfer is under MSB first sequence and the Doppler FFT data type is signed integer.

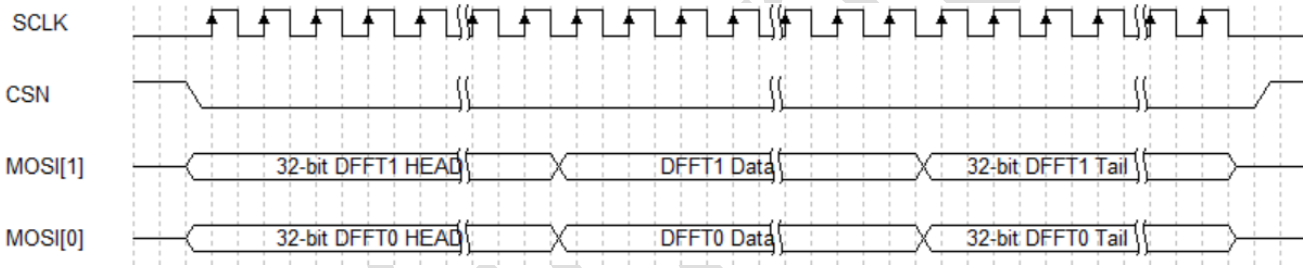


Figure 4-9 Doppler FFT Data Timing

Table 4-13 Doppler FFT Data Format

DW	Item	31:24	23:22	21:20	19:16	15:0
DW_0	Head	0xAA	2 or 3	3	F	dpl_frame_cnt[15:0]

DW	Item	31:16	15:0
DW_1 : DW_{1024}	Data	dfft real data 0 [15:0]	dfft imag data 0 [15:0]
		dfft real data 1 [15:0]	dfft imag data 1 [15:0]
		…	…
		dfft real data 1022 [15:0]	dfft imag data 1022 [15:0]
		dfft real data 1023 [15:0]	dfft imag data 1023 [15:0]

DW	Item	31:16	15:0
DW_{1025}	Tail	check_sum	0x5555

[1] if MOSI[0], Head[23:22]=2; if MOSI[1], Head[23:22]=3

[2] dpl_frame_cnt: Doppler frame cumulative number

[3] check_sum: sum of dfft data，which is used for optional redundancy check

4.7.7 SPI Output for Doppler FFT Peak

The chip can transfer Doppler FFT peak data with data SPI, where Pin27 is the data output bus MOSI[0]. The transfer is under MSB first sequence and the Doppler FFT data type is signed integer.

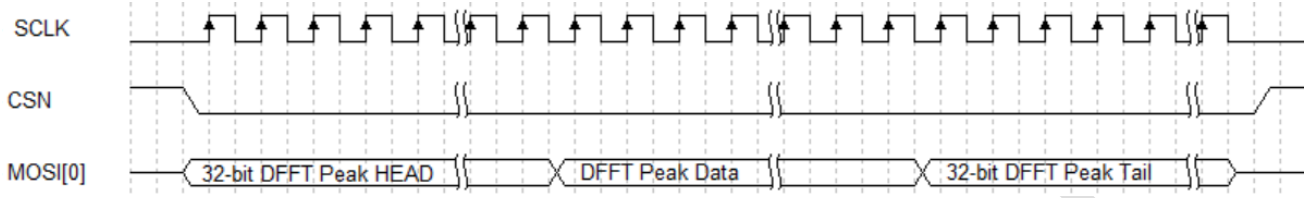


Figure 4-10 Doppler FFT Peak Data Timing

Table 4-14 Doppler FFT Peak Data Format

DW	Item	31:24	23:22	21:20	19: 6	5:0
DW0	HEAD	0xAA	1	0	0	cfg_len_rpt[4:0] +1

DW	Item	31	30:24	23	22:16	15	14:8	7	6:0
DW_1 : DW_{27}	Data	0	dfft0_max0_didx	0	dfft0_max0_ridx	0	dfft1_max0_didx	0	dfft1_max0_ridx
		dfft0_max0_value							
		reserved							
		0	dfft0_max1_didx	0	dfft0_max1_ridx	0	dfft1_max1_didx	0	dfft1_max1_ridx
		dfft0_max1_value							
		reserved							
		:							
		0	dfft0_max8_didx	0	dfft0_max8_ridx	0	dfft1_max8_didx	0	dfft1_max8_ridx
		dfft0_max8_value							
		reserved							

DW	Item	31:16	15:14	13:12	11:8	7:0
DW_{28}	Tail	check_sum	1	0	0	0x55

[1] cfg_len_rpt: length of reported data;

[2] dfft*_max*_didx: dfft peak location, Doppler fft index;

[3] dfft*_max*_ridx: dfft peak location, range fft index;

[4] dfft*_max*_value: dfft peak value; This value is the modulus value of 2ddfft at the corresponding position;

[5] check_sum: sum of all data，used for optional redundancy check

4.7.8 UART Output

The chip can also transfer range FFT data, Doppler FFT data, Doppler FFT peak via UART. The basic timing sequence is shown as below. For details, please contact ICLegend Micro.

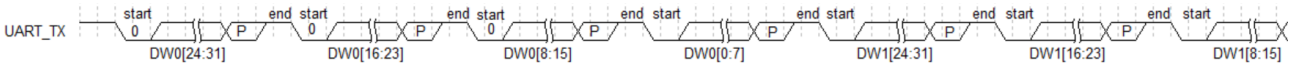


Figure 4-11 UART Output Data Timing

4.7.9 GPIO Output for Raw Data

Raw data GPIO output mode is recommended only for the chip debug and specific applications. When raw ADC data serialized output mode is selected in the chip, GPIO Pin26~Pin27 (raw_d0~raw_d1) will send out the 2 lanes of ADC's real time data (I channel in RX, Q channel in RX).

For details, please contact ICLegend Micro.

5 Pin Description

5.1 Pin Configuration

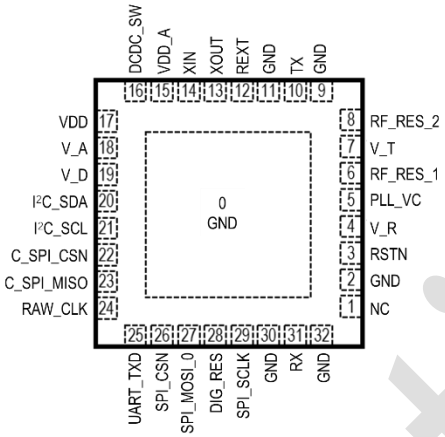


Figure 5-1 Pin Diagram QFN32 (Top View)

Table 5-1 Pin Description

Pin Name	Pin#	Function	Dir.	Type
NC	1	no connection		
RSTN	3	hard reset pin for internal digital circuit, active low	I	
V_R	4	1.6V supply input for RX chain	I	Power
PLL_VC	5	PLL VCO control voltage	I	
RF_RES_1	6	reserved RF pin, which need to be connected to the pin8	O	RF
V_T	7	1.6V supply input for TX chain	I	Power
RF_RES_2	8	reserved RF pin, which need to be connected to the pin6	O	RF
TX	10	Single-ended transmitter output	O	RF
REXT	12	Bias current setting. A resistor must be inserted between this pin and GND to generate the bias current.	I/O	
XOUT	13	Output to drive external crystal	I/O	25MHz
XIN	14	Input to drive external crystal	I/O	25MHz
VDD_A	15	3.3V power supply for analog circuits	I	Power
DCDC_SW	16	Power switching output	I/O	
VDD	17	3.3V power supply for the DCDC converter and analog circuits	I	Power
V_A	18	1.6V supply input for analog circuits	I	Power
V_D	19	1.6V supply input for digital circuits	I	Power
I²C_SDA	20[1]	command_I²C_sda: command I²C bus, sda, open drain	OD	
		command_spi_mosi: command SPI bus, mosi	I	
		command_uart_rx: command UART bus, uart_rx	I	
I²C_SCL	21[1]	command_I²C_scl: command I²C bus, scl	I	
		command_spi_sclk: command SPI bus, sclk	I	

		command_uart_tx: command UART bus, uart_tx	O	
C_SPI_CSN	22[2]	command_spi_csn: command SPI bus, csn	I	
C_SPI_MISO	23[1]	command_spi_miso: command SPI bus, miso	I/O	
		chip strap pin function, see Table 5-2		
RAW_CLK	24[1]	raw_clk, serial raw data bus, data clock	I/O	
		chip strap pin function, see Table 5-3		
UART_TXD	25[1]	data_uart_tx: optionally fft data uart output, 115200 baud rates	I/O	
		raw_ready: serial raw data bus, ready		
		chip strap pin function, see Table 5-4		
SPI_CSN	26[1]	data_spi_csn: fft data SPI bus, csn	O	
		raw_d0: serial raw data bus, I channel data in RX	O	
SPI_MOSI_0	27[1]	data_spi_mosi[0]: fft data SPI bus, mosi[0]	I/O	
		raw_d1: serial raw data bus, Q channel data in RX		
		chip I²C address configuration, see Table 5-5		
DIG_RES	28	reserved digital output pin		
SPI_SCLK	29	data_spi_sclk: fft data SPI bus, sclk	O	
RX	31	Single-ended receiver input	I	RF
GND	0, 2, 9, 11, 30, 32	ground	G	Ground

[1] There are pin multiplexing in Pin20, Pin21, Pin23 ~ Pin27.

[2] Pin22 needs to be pull down to the ground using a 10kΩ resistor.

5.2 Pin Multiplexing

For S3KM111L, Pin20, Pin21, Pin23~Pin27 have multiple functions, where the multiplexing mode is selected automatically according to the strapping pins setup when the chip is powered up. The Pin23 and Pin24 are used to set the chip configuration mode and the Pin25 is used to set the data communication mode. The strapping pin needs to be pulled down to the ground using a 3.3kΩ resistor when it is set to “Low”, while other strapping pins need to be pulled up the power supply using a 10kΩ resistor or floated to the power supply when it is set to “High”.

Table 5-2 Function Mode Selection Setup - Chip Configuration

Pin23	Pin24	Chip Configuration Mode
Low	Low	UART
Low	High	I²C
High	Low	SPI
High	High	SPI

Table 5-3 Function Mode Selection Setup – Data Communication

Pin25	Data Communication Mode
Low	GPIO (Raw Data)
High	SPI/UART

The following table 5-4 describes an example, the chip configuration is set in I²C mode and data communication mode is

set in SPI/UART mode.

Table 5-4 Working Mode and Pin Functions Examples

Pin#	Function	Mode
20	command_I²C_sda	chip configuration - I²C
21	command_I²C_scl	
25	data_uart_tx	data communication – SPI/UART
26	data_spi_csn	
27	data_spi_mosi[0]	
29	data_spi_sclk	

When I²C configuration mode is set, the Pin27 and Pin28 are used to set the slave chip's address, which is determined at reset phase, and at most 4 chips can be combined to the same I²C buses in I²C configuration mode.

Table 5-5 I²C Device Address

Pin27	Pin28	I²C Slave Device Address
Low	Low	7'b010_0000
Low	High	7'b010_0001
High	Low	7'b010_0010
High	High	7'b010_0011

6 Function Block Description

6.1 Waveform Synthesis

S3KM111L integrates a programmable FMCW waveform synthesizer, and users can use it to generate different frequency modulation like triangle or saw FMCW waveforms or CW waves. Together with radar setting software provided by ICLegend Micro or the modification of the chip's registers setting, the user can configure the parameters shown in Figure 6-1 and Figure 6-2.

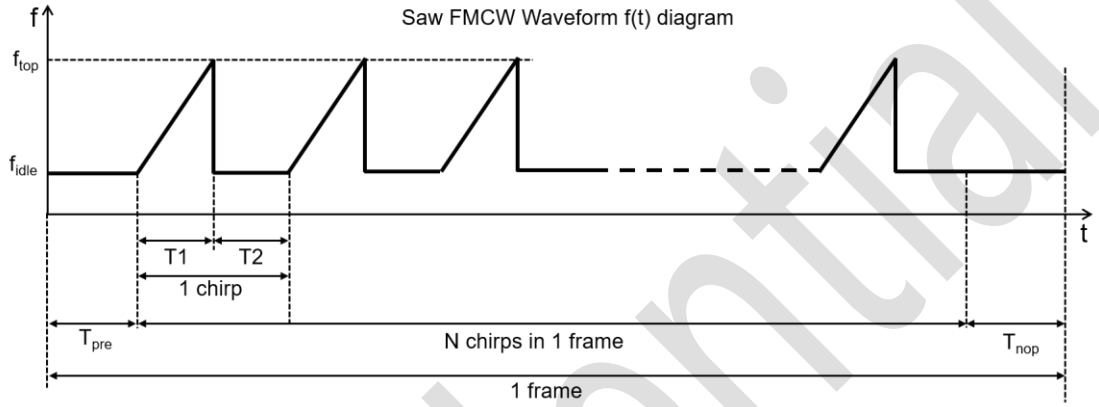


Figure 6-1 Saw FMCW waveform

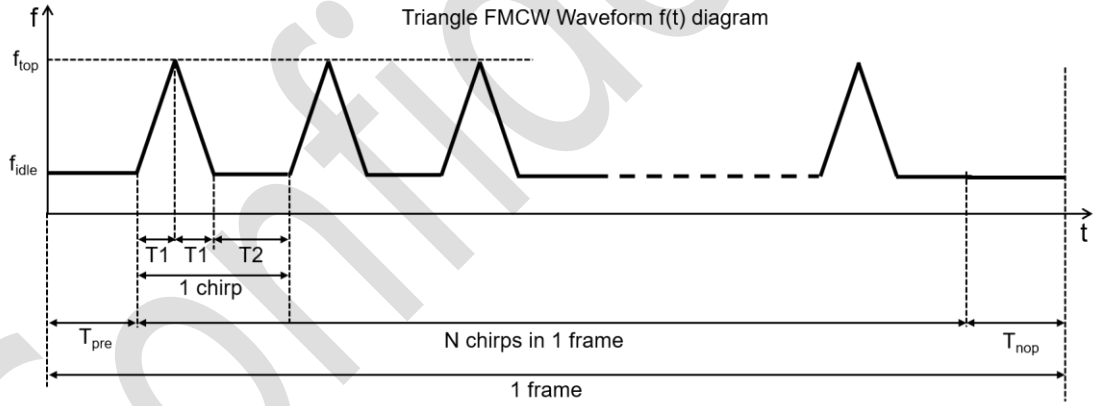


Figure 6-2 Triangle FMCW waveform

6.2 DSP Accelerator

S3KM111L integrates range FFT and Doppler FFT DSP acceleration algorithm. A typical FFT data flow diagram is shown in Figure 6-3.

The I/Q raw data from RX channel 1 ADC outputs can be processed in the DSP accelerator, and then range FFT results, Doppler FFT results or the peaks of the FFT results are sent out according to the chip's configuration.

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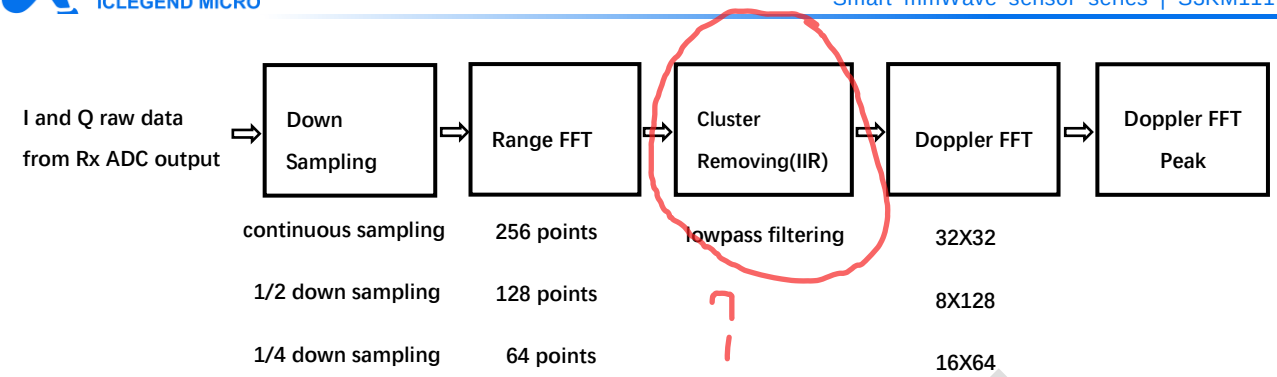


Figure 6-3 DSP Accelerator Data Flow

6.3 Low Power Optimization

S3KM111L provides a low power optimization mode, and users can configure bit register 0x41[4] to be 0 to enter the low power mode. In this mode, the RF transceiver and baseband circuits are power down automatically in every frame NOP time T_{nop} and work normally through each chirp in each frame.

6.4 Register Settings

Please contact ICLegend Micro's support to get the register settings software tool or the register tables file.

7 Application

7.1 Application Schematic

S3KM111L can be used as a standalone 1T1R radar sensor. Figure 7-1 shows the application schematic, and Table 7-1 shows the external components suggestions. Pin22(C_SPI_CSN) need to be pull down to the ground using a 10kΩ resistor.

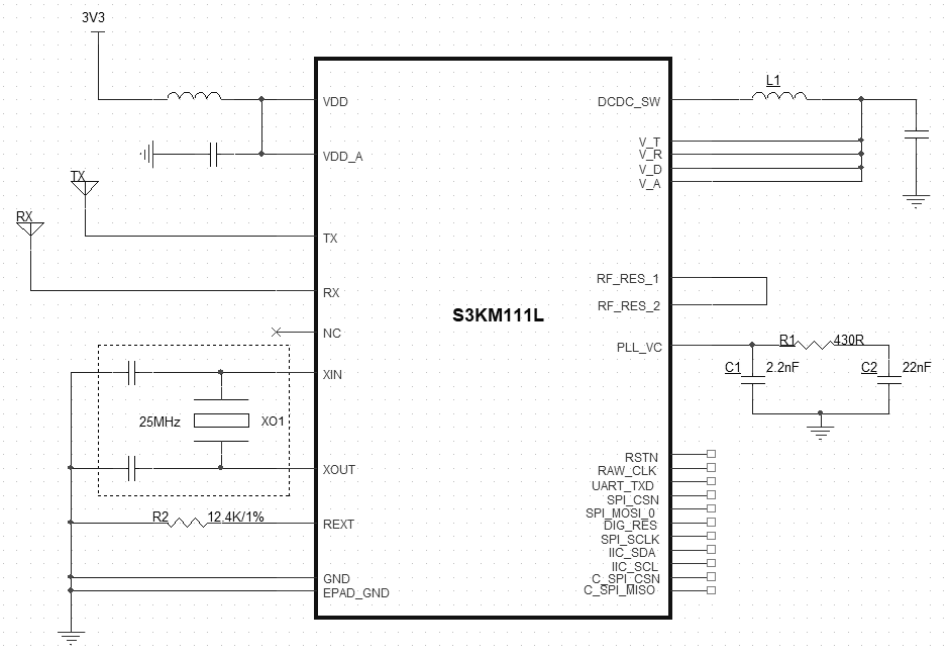


Figure 7-1 mmWave Sensor Application Schematic

Table 7-1 External Component Suggestions

Component	Function	Suggestion
XO1	crystal to generate 25MHz reference clock	<50ppm frequency stability is recommended
R1	0.43kΩ resistor, used as PLL's off-chip filter component	accuracy: ±5%
C1	22nF capacitor, used as PLL's off-chip filter component	accuracy: ±5%
C2	2.2nF capacitor, used as PLL's off-chip filter component	accuracy: ±5%
R2	12.4kΩ resistor, used for the reference current*	accuracy: ±1%
L1	off-chip power inductor for DCDC	low ESR, e.g. SRN4018-330M, SWPA252012S220MT
decoupling capacitors	decoupling and filtering for power supply	accuracy: ±5%

*This reference current decide the work current in SOC, can't guarantee the performance if R2 accuracy >±5% is forbidden.

7.2 Application Tips

7.2.1 Power Pins Decoupling

Please refer the application schematic for the power pin decoupling.

To guarantee the transceiver performance, it is recommended that all power supplies can be decoupled to the ground as close as possible to the power pins on the PCB with a 1μF capacitor in parallel to a 100nF capacitor and a 100pF capacitor. Each incoming power supply is better to be decoupled to the ground at the PCB input terminal by a 1μF tantalum capacitor in parallel with a 100nF chip capacitor.

7.2.2 Digital Data Output

The digital data outputs pins are GPIOs. These pins are ADCs' raw data output or FFT results output, which need not to be terminated and HiZ loading is preferred. When raw data mode is selected, the raw data clock (raw_clk) output frequency is 50MHz, and it is recommended to match the clock wire and data line (raw_d0~raw_d1) length as well as PCB routing. When FFT data output mode is selected, the output clock frequency and data rate are programmable, and the maximum clock frequency is 25MHz at FFT data output mode.).

The data SPI output is not guaranteed during the period of chip configuration.

7.2.3 Strapping Pins

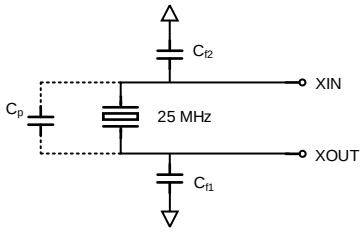
Pin23~25 are strapping pins, and the strapping pins need to be pulled down to the ground using a 3.3kΩ resistor when it is set to “Low”, while other strapping pins need to be pulled up the power using a 10kΩ resistor or floated to the power when it is set to “High”.

7.2.4 Analog IOs

There need to be a 1% accuracy resistor at REXT, whose resistance is around 12.4kΩ, and this resistor is recommended to be placed close to the S3KM111L and to be grounded on the ground plane.

PLL_VC is the pin for external resistor and capacitor of the PLL, and it is recommended to place the surface mounted devices near the pin. The recommended resistors and caps value are labeled in Figure 7-1.

XIN and XOUT are drive ports for reference crystal. Two capacitors (C_{f1} and C_{f2}) are inserted between XIN/XOUT and GND separately. C_{f1} and C_{f2} should be chosen such that the following equation is satisfied. C_L in the equation is the load specified by the crystal manufacture(Cp is the parasitic capacitor between XIN and XOUT). All discrete components used to implement the oscillator circuit should be placed as close as possible to XIN/XOUT pins, otherwise, the Cp cannot be ignored.



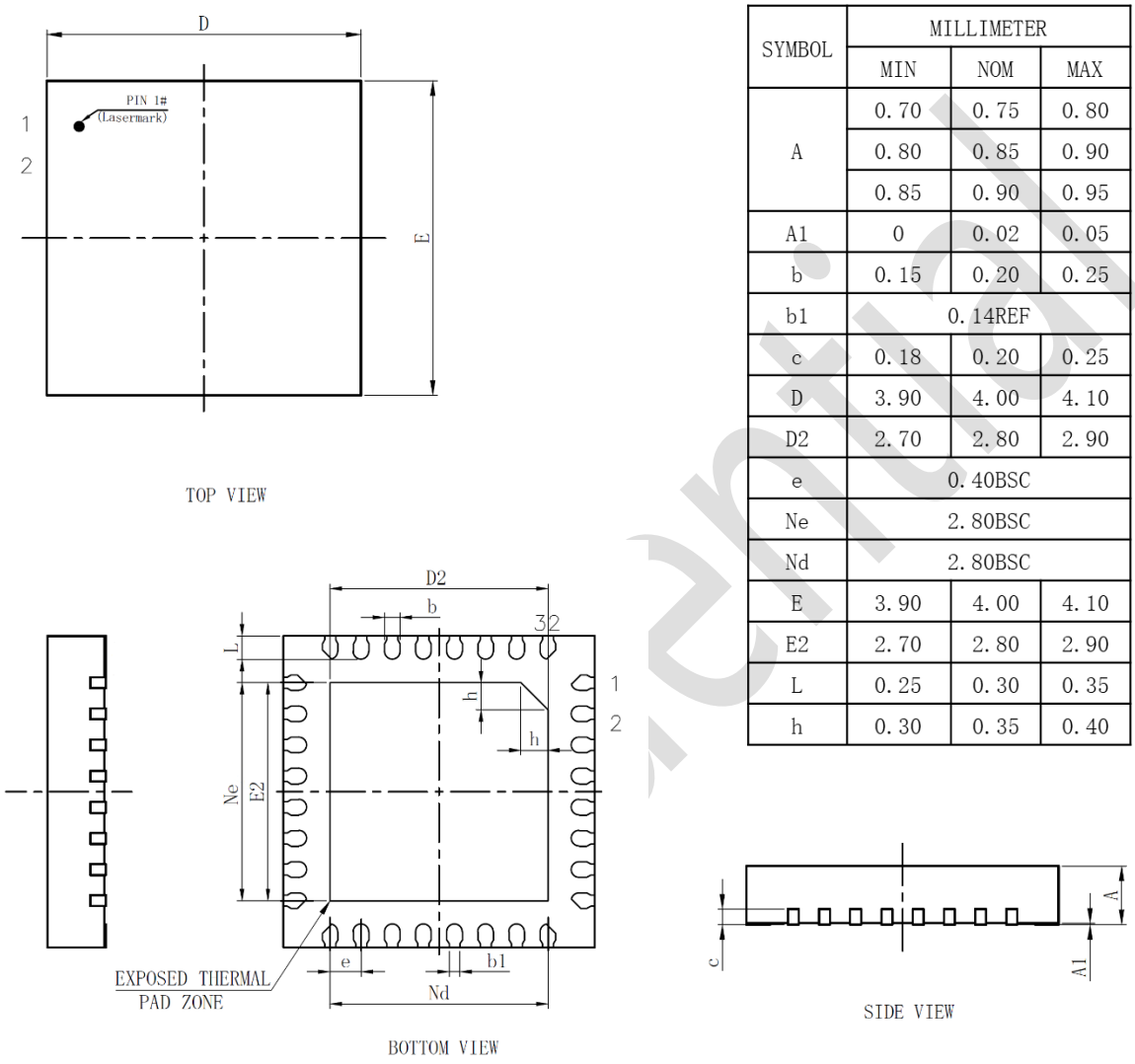
$$C_L = \frac{C_{f1} \times C_{f2}}{C_{f1} + C_{f2}} + C_p$$

Recommendation Value: C_{f1}=C_{f2}=20pf

Figure 7-2 Crystal Implementation and Load Capacitor Equation

DCDC_SW is the pin used for the integrated DCDC buck converter. A low ESR inductor is preferred and two 10μF ceramic capacitors followed the inductor are recommended to filter the switching ripple of the DCDC output.

8 Package Description



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
	0.85	0.90	0.95
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40

Figure 8-1 Package Description

For further information you needed, please contact ICLegend Micro for support .

(END)