SRK1201L 1-transmitter and 2-receiver 24GHz transceiver MMIC

GENERAL DESCRIPTION

The SRK1201L is a fully integrated transceiver MMIC based on the state-of-art silicon germanium process. It operates in the 24 GHz ISM band from 24.00 to 24.25 GHz. It has 1 transmitting path that delivers 9 dBm to the antenna feed and 2 receiving paths each of that provides a 29 dB voltage gain and a 9 dB noise figure. A frequency prescaler is included to generate signals with output frequencies of 1.5 GHz and 23 kHz. On-chip baluns are included to provide single-ended RF interface. The device is controlled via SPI interface. The package is a compact 40-lead, 5 mm x 5 mm QFN.

FEATURES

- 24 GHz ISM band transceiver MMIC with 1 transmitter and 2 receivers
- RX channel voltage conversion gain: 29 dB
- RX channel noise figure: 9 dB
- RX channel input P1dB: -15 dBm
- TX output power: 9 dBm
- VCO phase noise: -103 dBc @ 1 MHz offset
- Integrated balun for single-ended RF interfaces
- Prescaler with 1.5 GHz and 23 kHz outputs
- On-chip power and temperature sensors
- DC power rating: 3.3 V and 230 mA
- 40-lead, 5 mm x 5 mm QFN package
- Fully ESD protection
- AEC-Q100 qualified

APPLICATIONS

- Automotive radars
- Industrial radars
- IoT sensors

FUNCTIONAL BLOCK DIAGRAM

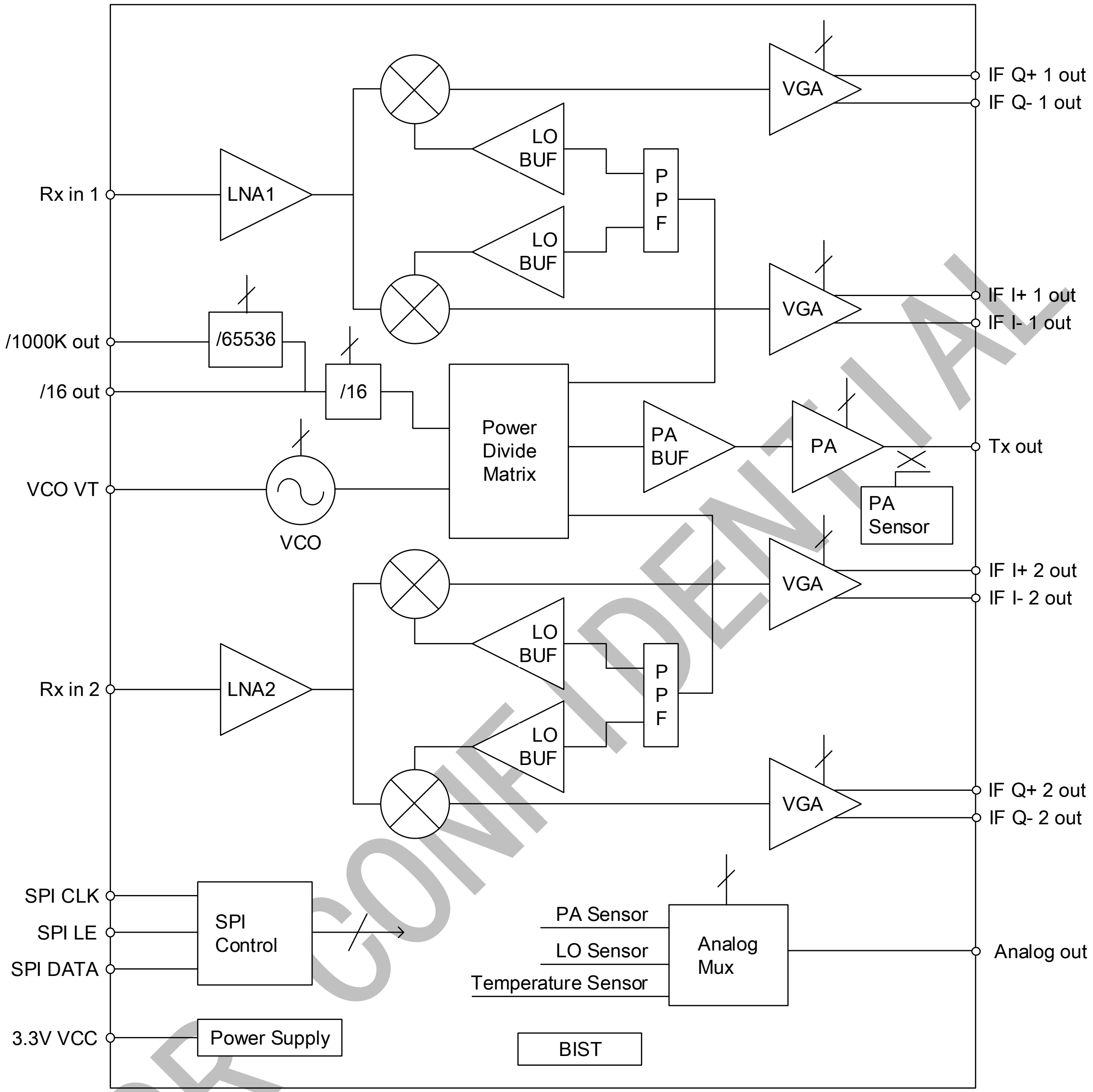

Figure 1 SOC Functional Block Diagram

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SPECIFICATIONS

VCC = 3.3 V, GND = 0 V, dBm referred to 50 Ω, operating temperature is 25 ºC , unless otherwise noted.

Power Supply

Table 1 Power Supply Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Note
Supply voltage	V_{cc}	3.135	3.3	3.465	V	
Supply current	I_{cc}		230		mA	

TX Section

Table 2 TX Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Note
VCO frequency range	f_{vco}	24.00		24.25	GHz	
VCO tuning voltage	V_T	0.25		2.75	V	
VCO tuning slope	$\triangle f/\triangle V_T$		-0.6		MHz/mV	
VCO temperature drift	$\triangle f/\triangle T$		1.4		MHz/ ºC	
VCO phase noise	P_N		-103		dBc/Hz	@ 1 MHz offset
TX port return loss	Γ_{TX}		-15		dB	with PCB matching
Max TX output power	P_{TX}		9		dBm	
TX output power tuning range			18		dB	
Q1 prescaler division ratio	D_{Q1}		16			
Q1 prescaler output power	P_{Q1}		-13		dBm	
Q1 output impedance	Z_{Q1}		50		Ω	
Q2 prescaler division ratio	D_{Q2}		2^{20}			
Q2 prescaler output voltage	P_{Q2}		3		V	Peak-to-peak voltage
Q2 output impedance	Z_{Q2}		1000		Ω	

RX Section

Table 3 RX Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Note
RFIN frequency range	f_{RFIN}	24.00		24.25	GHz	
RFIN port return loss	Γ_{RFIN}		-12		dB	with PCB matching
IF frequency range	f_{IF}	0		10	MHz	
IF output impedance	Z_{IF}		1000		Ω	
TX/RX isolation			-42		dB	

RFIN1 to RFIN2 isolation		-30	dB	
Voltage conversion gain	G_c	29	dB	
DSB noise figure	NF	9	dB	
Input compression point	IP_{1dB}	-15	dBm	
IQ phase imbalance		5	Degree	
IQ amplitude imbalance		1	dB	

Temperature Sensor

Table 4 Temperature Sensor Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Note
Temperature range		-40		105	°C	
Output temperature voltage	$V_{OUT,TEMP}$		1.55		V	@ 25 °C
Sensitivity			4.6		mV/°C	
Overall accuracy error				±15	°C	

Power Sensor

Table 5 Power Sensor Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Note
Power range		-10		15	dBm	
TX power sensor			1.65		V	@10 dBm
LO power sensor			1.32		V	@2 dBm

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

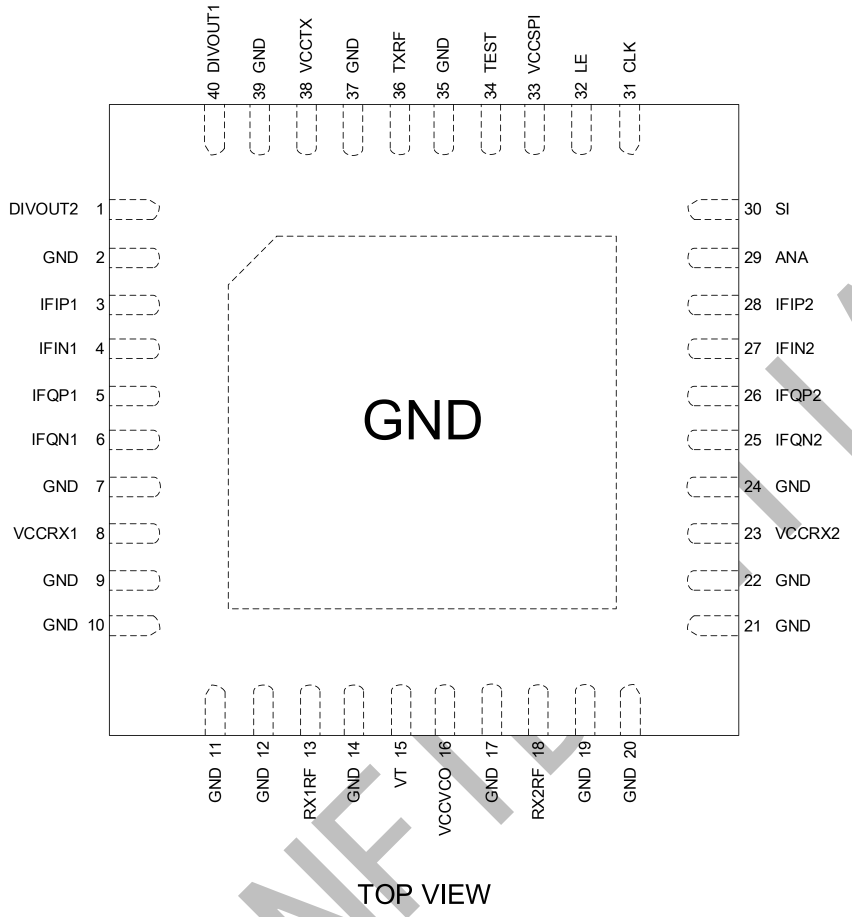


Figure 2 Pin Configuration

Table 5 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DIVOUT2	Prescaler output 23 kHz
2, 7, 9, 10, 11, 12, 14, 17, 19, 20, 21, 22, 24, 35, 37, 39	GND	RF or DC ground
3	IFIP1	In phase IF output at RX1
4	IFIN1	Complementary in phase IF output at RX1
5	IFQP1	Quadrature phase IF output at RX1
6	IFQN1	Complementary quadrature phase IF output at RX1
8	VCCRX1	Supply voltage for RX1
13	RX1RF	RF input at RX1
15	VT	VCO tuning input
16	VCCVCO	Supply voltage for VCO
18	RX2RF	RF input at RX2
23	VCCRX2	Supply voltage for RX2

25	IFQN2	Complementary quadrature phase IF output at RX2
26	IFQP2	Quadrature phase IF output at RX2
27	IFIN2	Complementary in phase IF output at RX2
28	IFIP2	In phase IF output at RX2
29	ANA	Analog output
30	SI	SPI data input
31	CLK	SPI clock input
32	LE	SPI load enable, low active
33	VCCSPI	Supply voltage for SPI
34	TEST	Test pin , be floated
36	TXRF	RF output at TX
38	VCCTX	Supply voltage for TX
40	DIVOUT1	Prescaler output 1.5 GHz

SPI

1. Three control signals : SI(data), CLK(clock), LE(load enable)
2. The data (MSB first) is clocked into the 32-bit input shift register on each rising edge of CLK , and is written in the latches at the rising edge of LE
3. There are totally 8 groups of latches which determined by the state of the last 3 data bits

Register 0

Reserved																					PRESCALE1	VCO	PRESCALE2	PA					ADDRESS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EN	EN	EN	EN	V4	V3	V2	V1	0	0	0

Register 1

Reserved																													ADDRESS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Register 2

Reserved											VGA				LO BUFFER	IQ MIXER												LNA	ADDRESS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	EN	D3	D2	D1	EN	EN	CTRL	DCOC_I5	DCOC_I4	DCOC_I3	DCOC_I2	DCOC_I1	DCOC_Q5	DCOC_Q4	DCOC_Q3	DCOC_Q2	DCOC_Q1	EN	0	1	0

Register 3

Reserved											VGA				LO BUFFER	IQ MIXER												LNA	ADDRESS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	EN	D3	D2	D1	EN	EN	CTRL	DCOC_I5	DCOC_I4	DCOC_I3	DCOC_I2	DCOC_I1	DCOC_Q5	DCOC_Q4	DCOC_Q3	DCOC_Q2	DCOC_Q1	EN	0	1	1

Register 4

Reserved																													ADDRESS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Register 5

Reserved																													ADDRESS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Register 6

Reserved																			MXOUT CONTROL			Reserved			SENSOR ENABLE				ADDRESS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CTRL3	CTRL2	CTRL1	0	0	0	EN4	EN3	EN2	EN1	1	1	0

Register 7

Reserved																													ADDRESS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Figure 3 Register map

Register 0 (TX Control Register)

With Register DB[2:0] set to [0,0,0], the TX control register is programmed as shown in Figure 3.

Prescaler1

Setting DB10 to 1 enables the prescaler1, setting DB10 to 0 disables the prescaler1.

VCO

Setting DB9 to 1 enables the VCO , setting DB9 to 0 disables the VCO.

Prescaler2

Setting DB8 to 1 enables the prescaler2, setting DB8 to 0 disables the prescaler2.

PA

Setting DB7 to 1 enables the PA, setting DB7 to 0 disables the PA.

The PA setting is controlled by DB[6:3]. The truth table is in Table 6.

Table 6 PA setting truth table

V4	V3	V2	V1	SETTING
0	0	0	0	Minimum PA output power
0	0	0	1	PA power increasing progressively
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	Maximum PA output power

Register 2 (RX1 Control Register)

With Register DB[2:0] set to [0,1,0], the RX1 control register is programmed as shown in Figure 3.

VGA

Setting DB20 to 1 enables the VGA, setting DB20 to 0 disables the VGA.

The VGA setting is controlled by DB[19:17]. The truth table is in Table 7.

Table 7 RX1 VGA setting truth table

D3	D2	D1	SETTING
0	0	0	Minimum gain
0	0	1	Gain increasing
0	1	0	
0	1	1	

1	0	0	progressively
1	0	1	
1	1	0	
1	1	1	Maximum gain

LO Buffer

Setting DB16 to 1 enables the LO Buffer, setting DB16 to 0 disables the LO Buffer.

IQ Mixer

Setting DB15 to 1 enables the IQ Mixer, setting DB15 to 0 disables the IQ Mixer.

Setting DB14 to 0, the voltage gain is 6dB; when setting DB14 to 1, the voltage gain is 3dB.

The DB[13:9] control the I path IF value as below truth table Table 8.

Table 8 RX1 *I* path IF value setting truth table

DB13	DB12	DB11	DB10	DB9	IFIP	IFIN
X	0	0	0	0	0	0
0	0	0	0	1	-ΔV	0
1	0	0	0	1	0	-ΔV
0	0	0	1	0	-2ΔV	0
1	0	0	1	0	0	2-ΔV
0	0	0	1	1	-3ΔV	0
1	0	0	1	1	0	-3ΔV
0	0	1	0	0	-4ΔV	0
1	0	1	0	0	0	-4ΔV
0	0	1	0	1	-5ΔV	0
1	0	1	0	1	0	-5ΔV
0	0	1	1	0	-6ΔV	0
1	0	1	1	0	0	-6ΔV
0	0	1	1	1	-7ΔV	0
1	0	1	1	1	0	-7ΔV
0	1	0	0	0	-8ΔV	0
1	1	0	0	0	0	-8ΔV
0	1	0	0	1	-9ΔV	0
1	1	0	0	1	0	-9ΔV
0	1	0	1	0	-10ΔV	0
1	1	0	1	0	0	-10ΔV
0	1	0	1	1	-11ΔV	0
1	1	0	1	1	0	-11ΔV
0	1	1	0	0	-12ΔV	0
1	1	1	0	0	0	-12ΔV
0	1	1	0	1	-13ΔV	0
1	1	1	0	1	0	-13ΔV
0	1	1	1	0	-14ΔV	0

1	1	1	1	0	0	-14ΔV
0	1	1	1	1	-15ΔV	0
1	1	1	1	1	0	-15ΔV

The DB[8:4] control the Q path IF value as below truth table Table 9.

Table 9 RX1 *Q* path IF value setting truth table

DB8	DB7	DB6	DB5	DB4	IFQP	IFQN
X	0	0	0	0	0	0
0	0	0	0	1	-ΔV	0
1	0	0	0	1	0	-ΔV
0	0	0	1	0	-2ΔV	0
1	0	0	1	0	0	2-ΔV
0	0	0	1	1	-3ΔV	0
1	0	0	1	1	0	-3ΔV
0	0	1	0	0	-4ΔV	0
1	0	1	0	0	0	-4ΔV
0	0	1	0	1	-5ΔV	0
1	0	1	0	1	0	-5ΔV
0	0	1	1	0	-6ΔV	0
1	0	1	1	0	0	-6ΔV
0	0	1	1	1	-7ΔV	0
1	0	1	1	1	0	-7ΔV
0	1	0	0	0	-8ΔV	0
1	1	0	0	0	0	-8ΔV
0	1	0	0	1	-9ΔV	0
1	1	0	0	1	0	-9ΔV
0	1	0	1	0	-10ΔV	0
1	1	0	1	0	0	-10ΔV
0	1	0	1	1	-11ΔV	0
1	1	0	1	1	0	-11ΔV
0	1	1	0	0	-12ΔV	0
1	1	1	0	0	0	-12ΔV
0	1	1	0	1	-13ΔV	0
1	1	1	0	1	0	-13ΔV
0	1	1	1	0	-14ΔV	0
1	1	1	1	0	0	-14ΔV
0	1	1	1	1	-15ΔV	0
1	1	1	1	1	0	-15ΔV

LNA

Setting DB3 to 1 enables the LNA, setting DB3 to 0 disables the LNA.

Register 3 (RX2 Control Register)

With Register DB[2:0] set to [0,1,1], the RX2 control register is programmed as shown in Figure 3.

VGA

Setting DB20 to 1 enables the VGA, setting DB20 to 0 disables the VGA.

The VGA setting is controlled by DB[19:17]. The truth table is in Table 10.

Table 10 RX2 VGA setting truth table

D3	D2	D1	SETTING
0	0	0	Minimum gain
0	0	1	Gain increasing progressively
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	Maximum gain

LO Buffer

Setting DB16 to 1 enables the LO Buffer, setting DB16 to 0 disables the LO Buffer.

IQ Mixer

Setting DB15 to 1 enables the IQ Mixer, setting DB15 to 0 disables the IQ Mixer.

Setting DB14 to 0, the voltage gain is 6dB; when setting DB14 to 1, the voltage gain is 3dB.

The DB[13:9] control the I path IF value as below truth table Table 11.

Table 11 RX2 *I* path IF value setting truth table

DB13	DB12	DB11	DB10	DB9	IFIP	IFIN
X	0	0	0	0	0	0
0	0	0	0	1	-ΔV	0
1	0	0	0	1	0	-ΔV
0	0	0	1	0	-2ΔV	0
1	0	0	1	0	0	2-ΔV
0	0	0	1	1	-3ΔV	0
1	0	0	1	1	0	-3ΔV
0	0	1	0	0	-4ΔV	0
1	0	1	0	0	0	-4ΔV
0	0	1	0	1	-5ΔV	0
1	0	1	0	1	0	-5ΔV
0	0	1	1	0	-6ΔV	0
1	0	1	1	0	0	-6ΔV

0	0	1	1	1	-7ΔV	0
1	0	1	1	1	0	-7ΔV
0	1	0	0	0	-8ΔV	0
1	1	0	0	0	0	-8ΔV
0	1	0	0	1	-9ΔV	0
1	1	0	0	1	0	-9ΔV
0	1	0	1	0	-10ΔV	0
1	1	0	1	0	0	-10ΔV
0	1	0	1	1	-11ΔV	0
1	1	0	1	1	0	-11ΔV
0	1	1	0	0	-12ΔV	0
1	1	1	0	0	0	-12ΔV
0	1	1	0	1	-13ΔV	0
1	1	1	0	1	0	-13ΔV
0	1	1	1	0	-14ΔV	0
1	1	1	1	0	0	-14ΔV
0	1	1	1	1	-15ΔV	0
1	1	1	1	1	0	-15ΔV

The DB[8:4] control the Q path IF value as below truth table Table 12.

Table 12 RX2 *Q* path IF value setting truth table

DB8	DB7	DB6	DB5	DB4	IFQP	IFQN
X	0	0	0	0	0	0
0	0	0	0	1	-ΔV	0
1	0	0	0	1	0	-ΔV
0	0	0	1	0	-2ΔV	0
1	0	0	1	0	0	2-ΔV
0	0	0	1	1	-3ΔV	0
1	0	0	1	1	0	-3ΔV
0	0	1	0	0	-4ΔV	0
1	0	1	0	0	0	-4ΔV
0	0	1	0	1	-5ΔV	0
1	0	1	0	1	0	-5ΔV
0	0	1	1	0	-6ΔV	0
1	0	1	1	0	0	-6ΔV
0	0	1	1	1	-7ΔV	0
1	0	1	1	1	0	-7ΔV
0	1	0	0	0	-8ΔV	0
1	1	0	0	0	0	-8ΔV
0	1	0	0	1	-9ΔV	0
1	1	0	0	1	0	-9ΔV

0	1	0	1	0	-10ΔV	0
1	1	0	1	0	0	-10ΔV
0	1	0	1	1	-11ΔV	0
1	1	0	1	1	0	-11ΔV
0	1	1	0	0	-12ΔV	0
1	1	1	0	0	0	-12ΔV
0	1	1	0	1	-13ΔV	0
1	1	1	0	1	0	-13ΔV
0	1	1	1	0	-14ΔV	0
1	1	1	1	0	0	-14ΔV
0	1	1	1	1	-15ΔV	0
1	1	1	1	1	0	-15ΔV

LNA

Setting DB3 to 1 enables the LNA, setting DB3 to 0 disables the LNA.

Register 6 (Sensor enable and ANA output selection)

With Register DB[2:0] set to [1,1,0], the sensor enable and ANA output signal selection is programmed as shown in Figure 3.

Sensor enable

Setting DB6 to 1 enables the power sensor of PPF LO buffer input in RX1, setting DB6 to 0 disable it.

Setting DB5 to 1 enables the power sensor to PPF LO buffer input in RX2, setting DB5 to 0 disable it.

Setting DB4 to 1 enables the power sensor of PA output and temperature sensor nearby PA, setting DB4 to 0 disable them.

Setting DB3 to 1 enables the power sensor of PA buffer input, setting DB3 to 0 disable it.

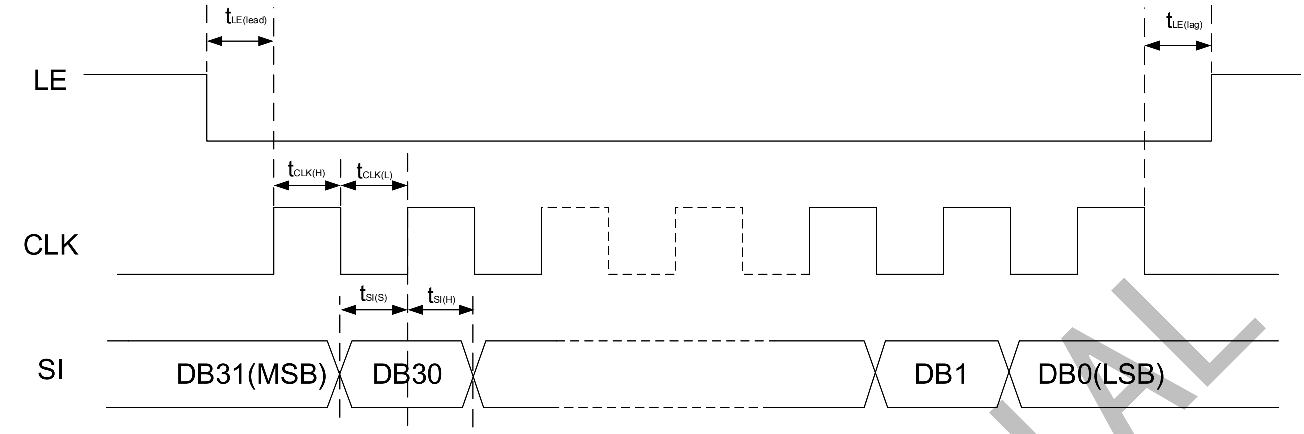
ANA output selection

The DB[12:10] control the ANA output signal selection as below truth table Table 13.

Table 13 ANA output signal selection truth table

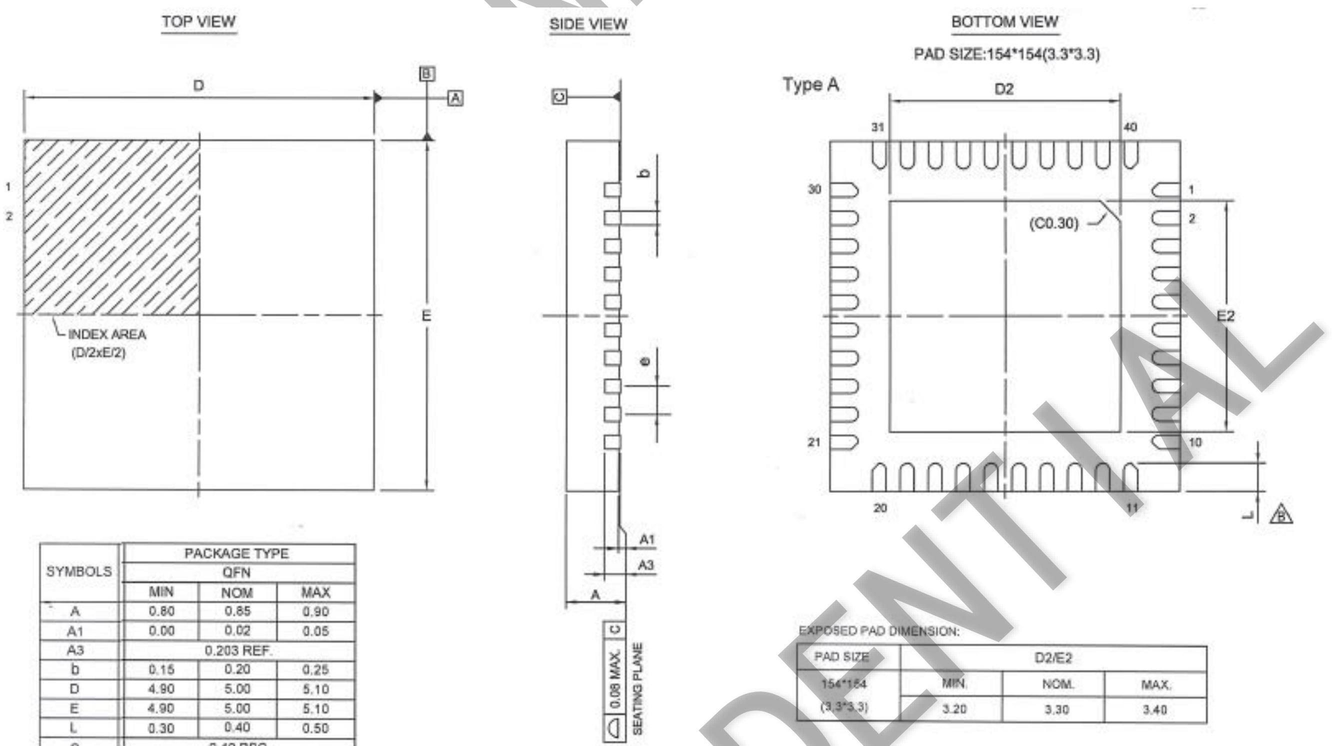
CTRL3	CTRL2	CTRL1	OUTPUT
0	0	0	NA
0	0	1	NA
0	1	0	Power sensor of PA output power
0	1	1	Temperature sensor nearby PA
1	0	0	Power sensor of input to PPF LO Buffer in RX2
1	0	1	Power sensor of input to PPF LO Buffer in RX1
1	1	0	Power sensor of input to PA Buffer
1	1	1	NA

TIMING SPECIFICATIONS



Parameter	Symbol	Min	Max	Unit
CLK frequency	f_{CLK}		50	MHz
LE lead time	$t_{LE(lead)}$	20		ns
LE lag time	$t_{LE(lag)}$	20		ns
CLK high duration	$t_{CLK(H)}$	10		ns
CLK low duration	$t_{CLK(L)}$	10		ns
SI to CLK setup time	$t_{SI(S)}$	10		ns
SI to CLK hold time	$t_{SI(H)}$	10		ns

PACKAGE DIMENSIONS



SYMBOLS	PACKAGE TYPE QFN		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
L	0.30	0.40	0.50
e	0.40 BSC.		

EXPOSED PAD DIMENSION:

PAD SIZE	D2/E2		
154*154 (3.3*3.3)	MIN.	NOM.	MAX.
	3.20	3.30	3.40

Figure 4 40-Lead QFN Package Dimensions

APPLICATION BOARD

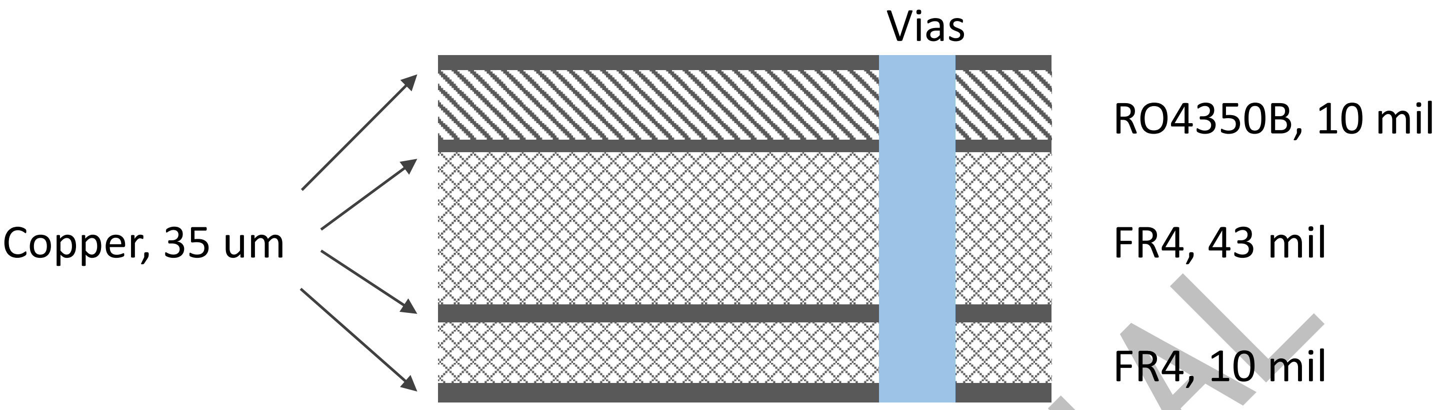


Figure 5 PCB stack profile

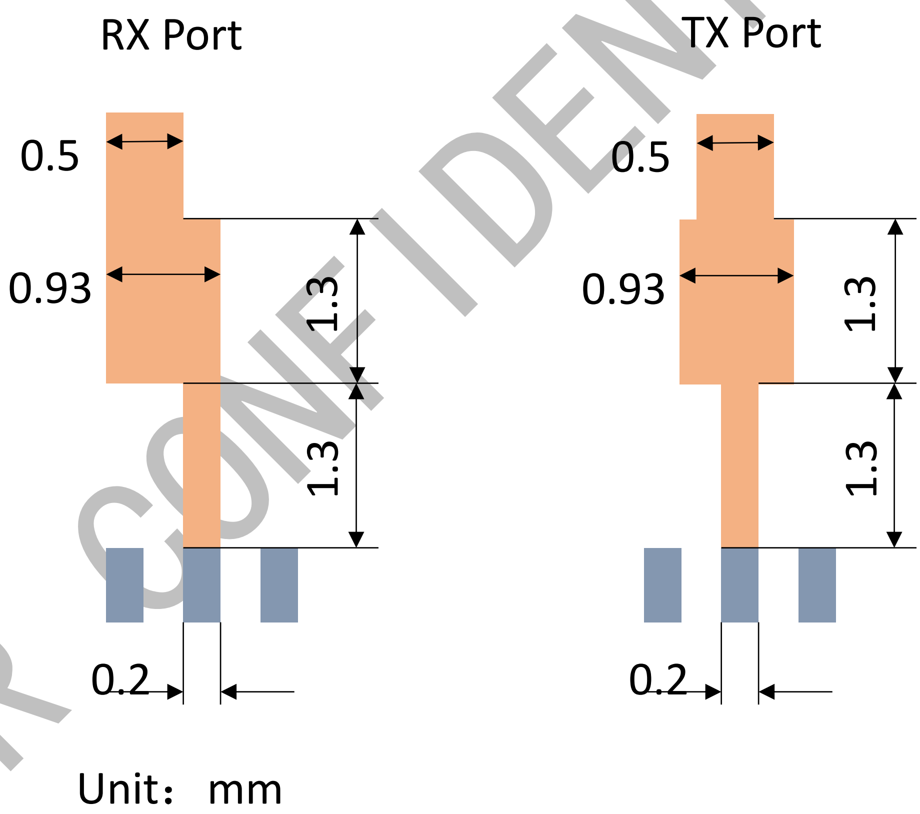


Figure 6 Matching structure dimensions

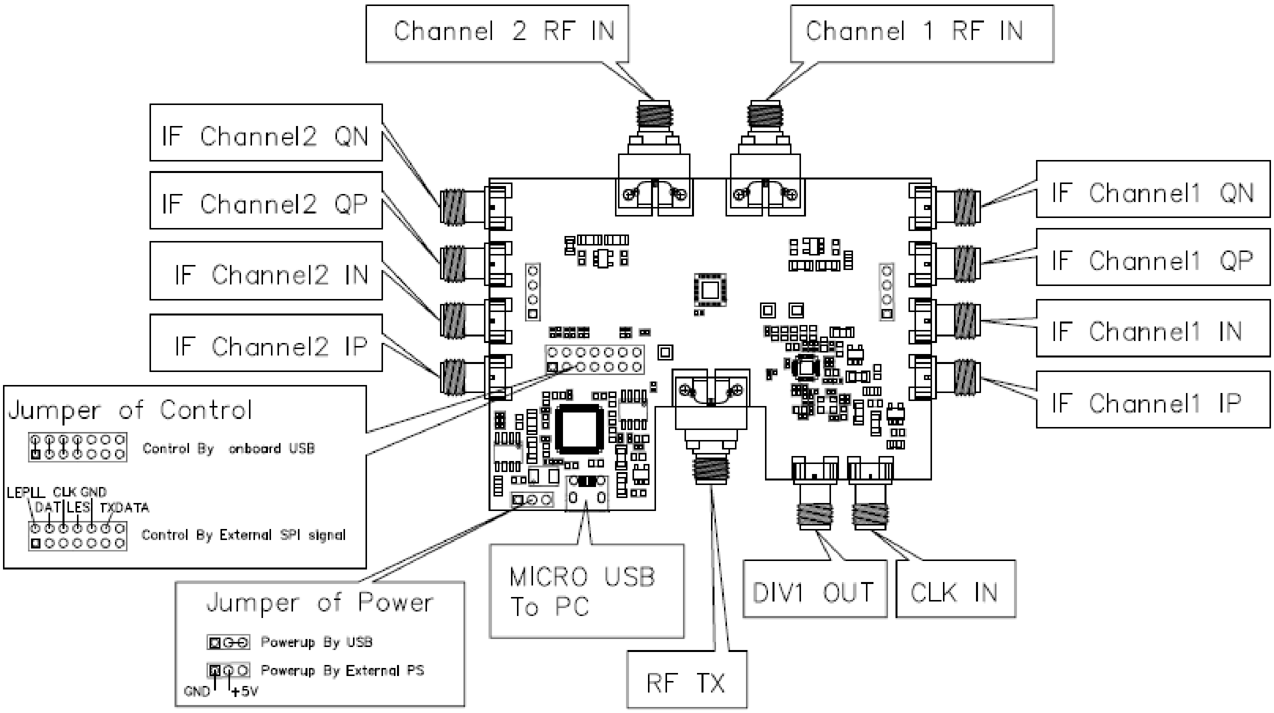


Figure 7 Evaluation board illustration