The Field-Effect Transistor (FET)

MOSFET

- The **metal-oxide-semiconductor field-effect transistor** (MOSFET) becomes a practical reality in the 1970s.
- The MOSFET, compared to BJTs, can be made very small, that is, it occupies a very small area in IC chip.
- In the MOSFET, the current is controlled by an electric field applied perpendicular to both the semiconductor surface and to the direction of current.
- The phenomenon applying an electric field perpendicular to the surface is called the **field effect**.
- Basic MOS capacitor structure

t_{ox}: 氧化層厚度

ε_{ox} : 氧化層介電常數

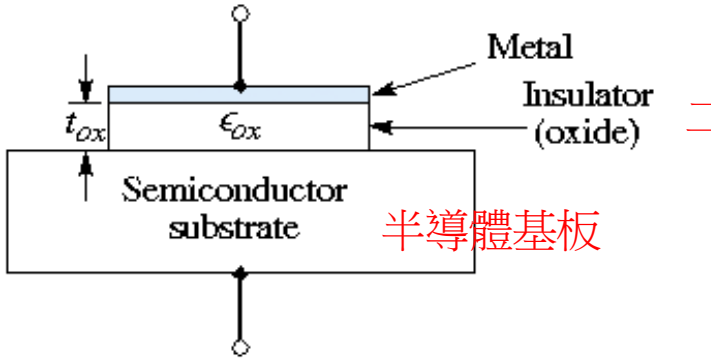


Figure 5.1 The basic MOS capacitor structure

The Physics of the MOS Capacitor

P型基板

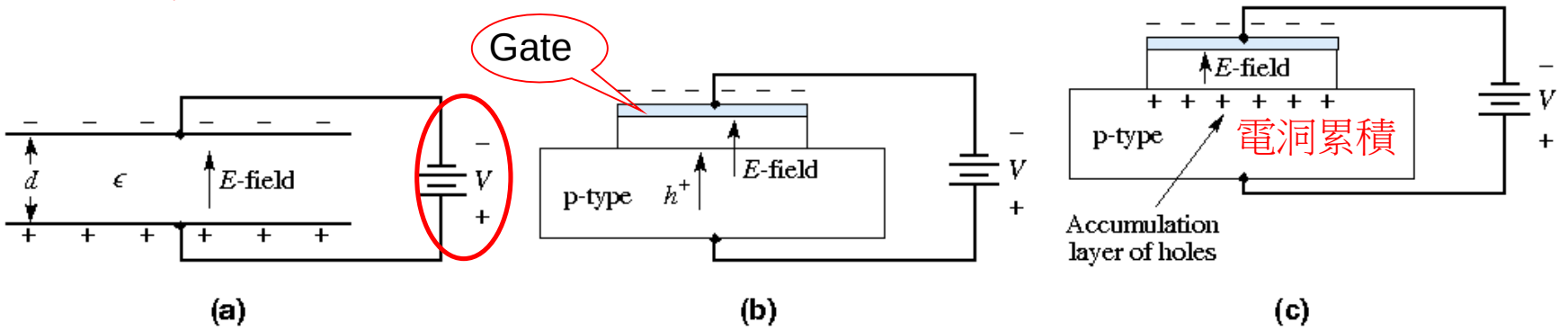


Figure 5.2 (a) A parallel-plate capacitor, showing the electric field and conductor charges, (b) a corresponding MOS capacitor with a negative gate bias, showing the electric field and charge flow, and (c) the MOS capacitor with an accumulation layer of holes

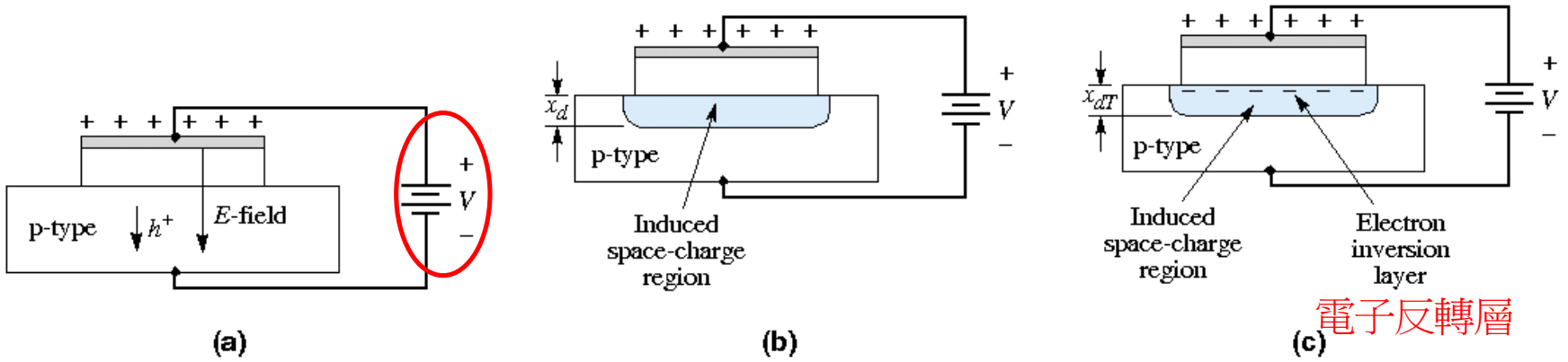
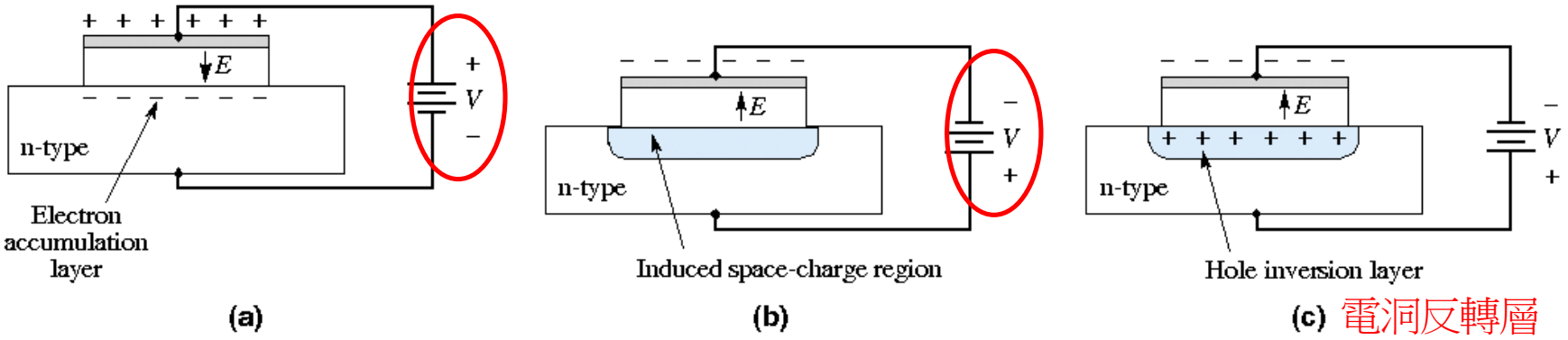


Figure 5.3 The MOS capacitor with p-type substrate: (a) effect of positive gate bias, showing the electric field and charge flow, (b) the MOS capacitor with an induced space-charge region due to a moderate gate bias, and (c) the MOS capacitor with an induced space-charge region and electron inversion layer due to a larger gate bias

The Physics of the MOS Capacitor for N-type Semiconductor Substrate

*N*型基板



電洞反轉層

Figure 5.4 The MOS capacitor with n-type substrate for: (a) a positive gate bias, (b) a moderate negative bias, and (c) a larger negative bias

- Enhancement mode: a voltage must be applied to the gate to create an inversion layer.
  - ✓ P-type: a positive gate voltage must be applied to create the electron inversion layer
  - ✓ N-type: a negative gate voltage must be applied to create the hole inversion layer

NMOS

- Transistor Structure

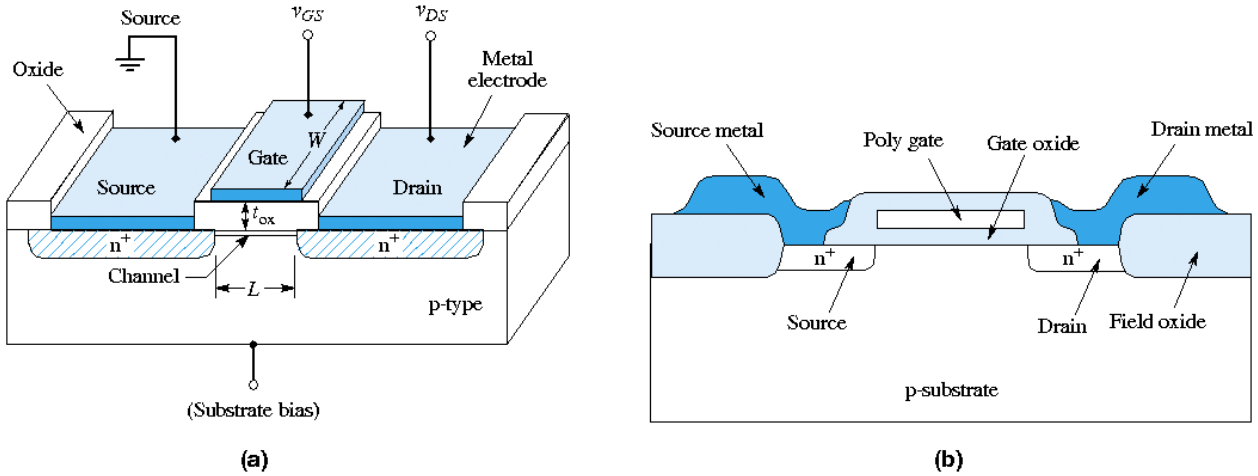
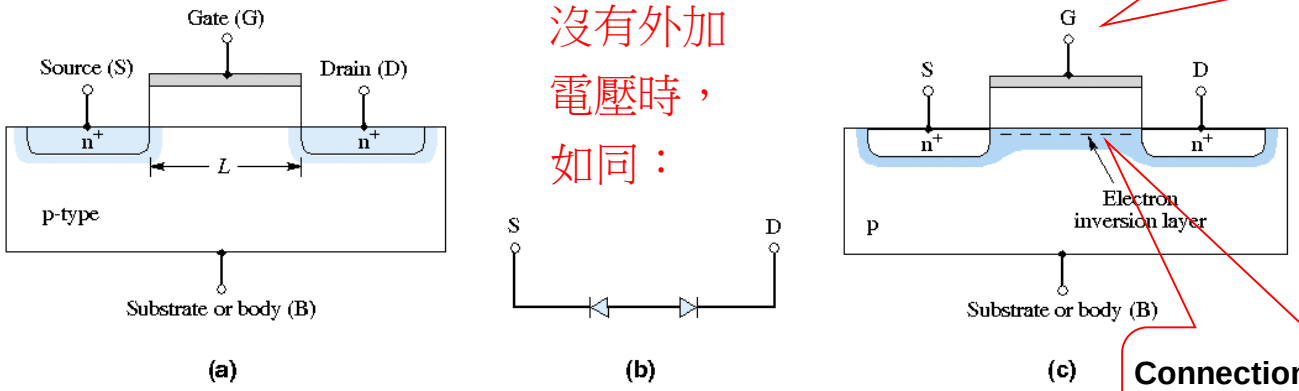


Figure 5.5 (a) Schematic diagram of an n-channel enhancement mode MOSFET and (b) an n-channel MOSFET, showing the field oxide and polysilicon gate

- Transistor Operation



沒有外加電壓時，如同：

Large enough positive voltage induces an electron inversion layer.

Connection between D and S is created so that a current can be generated.

Figure 5.6 (a) Cross section of the n-channel MOSFET prior to the formation of an electron inversion layer, (b) equivalent back-to-back diodes between source and drain when the transistor is in cutoff, and (c) cross section after the formation of an electron inversion layer

MOSFET Current-Voltage Characteristics

- The threshold voltage of the n-channel MOSFET is denoted as V_{TN} and is defined as the applied gate voltage needed to create an inversion charge.
- We can think of the threshold voltage as the gate voltage required to “turn on” the transistor.

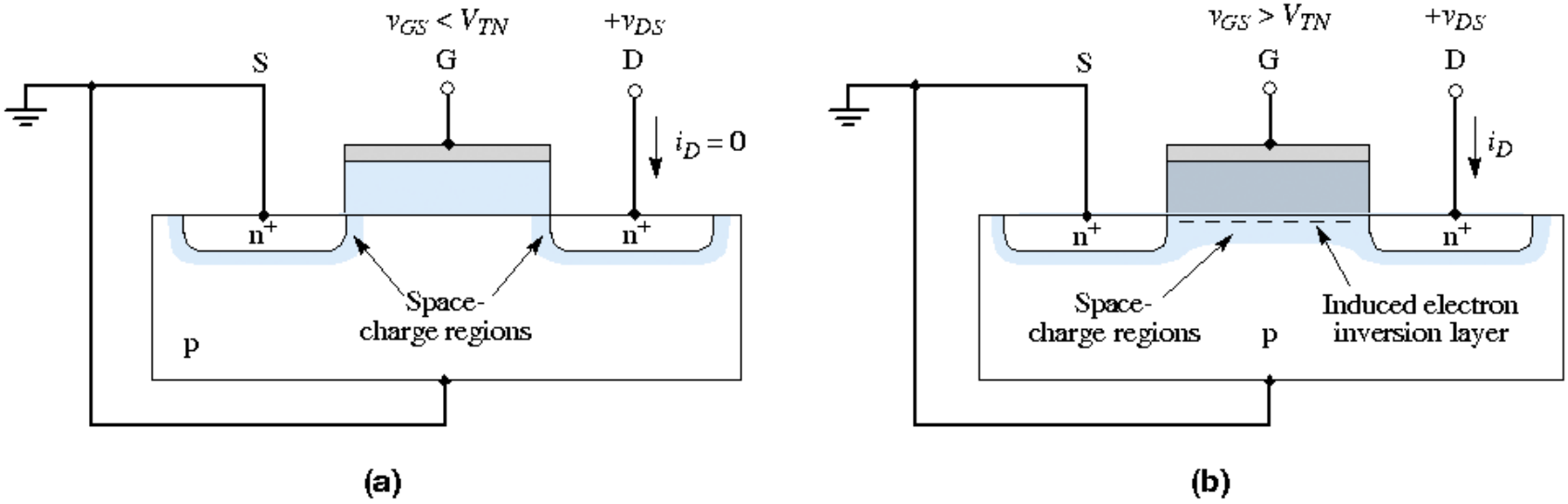


Figure 5.7 The n-channel enhancement-mode MOSFET (a) with an applied gate voltage $v_{GS} < V_{TN}$, and (b) with an applied gate voltage $v_{GS} > V_{TN}$

MOSFET Current-Voltage Characteristics

- The i_D versus v_{DS} characteristics for small values of v_{DS}

"當v_{DS}夠小時"，i_D與v_{DS}關係圖，
$v_{GS} > V_{TN}$時，i_D會隨v_{DS}增加而增加。

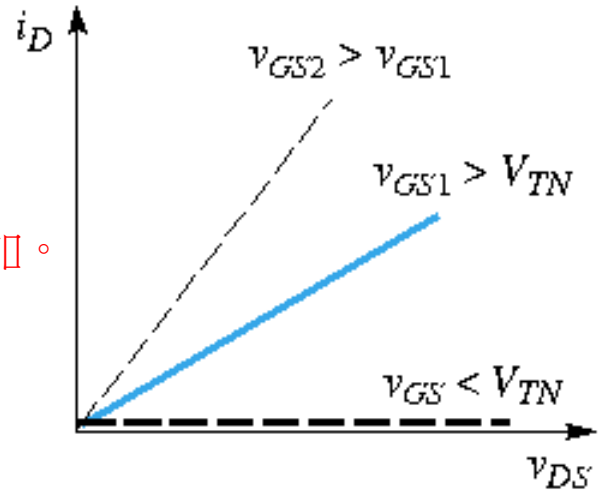
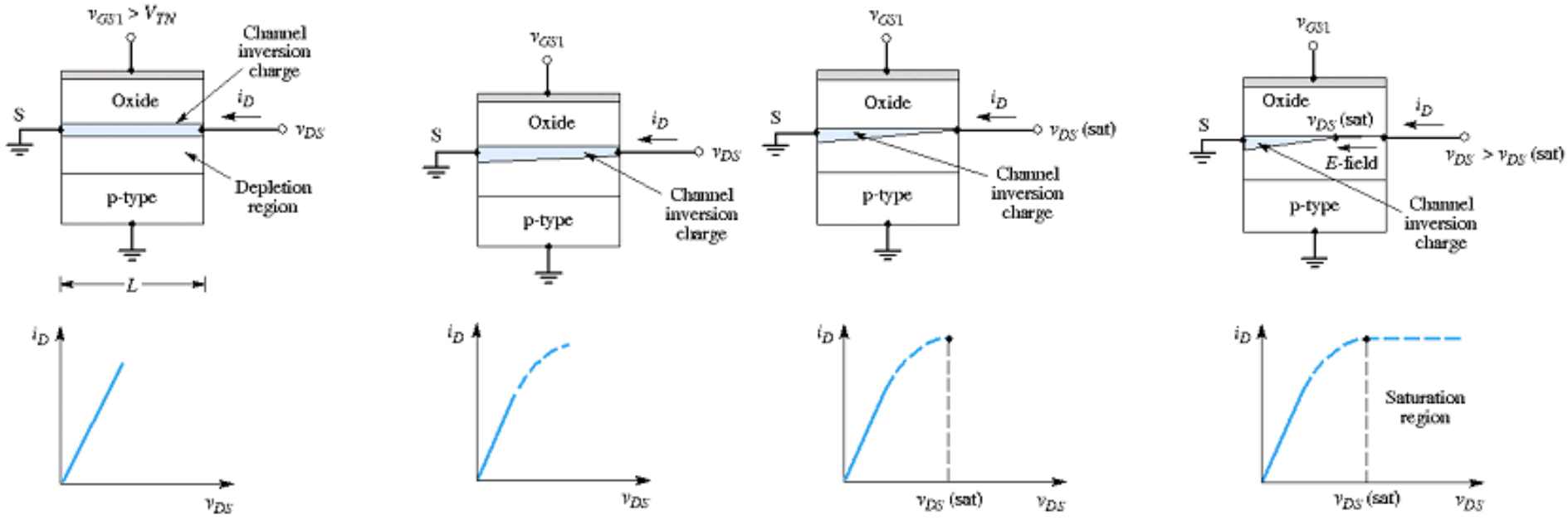


Figure 5.8 Plot of i_D versus v_{DS} characteristic for small values of v_{DS} at three v_{GS} voltages

MOSFET Current-Voltage Characteristics



(a) (b) (c) (d)

當v_{DS}小時。

當v_{DS}持續增加，D和G的壓差變小，反轉層變小。

當v_{DS}增加至$v_{GS}-V_{TN}$時，靠近D端的反轉層密度=0。

當$v_{DS}>v_{DS,sat}$時，i_D飽和。

Figure 5.9 Cross section and i_D versus v_{DS} curve for an n-channel enhancement-mode MOSFET when $v_{GS} > V_{TN}$ for: (a) a small v_{DS} value, (b) a larger v_{DS} value, (c) $v_{DS} = v_{DS}(sat)$, and (d) $v_{DS} > v_{DS}(sat)$

Ideal MOSFET Current-Voltage Characteristics

- Nonsaturation (triode) Region

形成電子反轉層 $\Rightarrow$ *NMOS*

$$v_{DS} < v_{DS(sat)} = v_{GS} - V_{TN}$$

$$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2] = K_n(2v_{DS(sat)}v_{DS} - v_{DS}^2)$$

- Saturation Region

$$v_{DS} > v_{DS(sat)} \quad (\text{also } v_{GS} > V_{TN})$$

$$i_D = K_n(v_{GS} - V_{TN})^2$$

Note: In the saturation region,

$$\frac{1}{r_o} = \partial i_D / \partial v_{DS} = \infty$$

$v_{GS} > V_{TN}$時，可分為

Nonsaturation & Saturation

反之，若$v_{GS} < V_{TN}$時，$i_D = 0$。

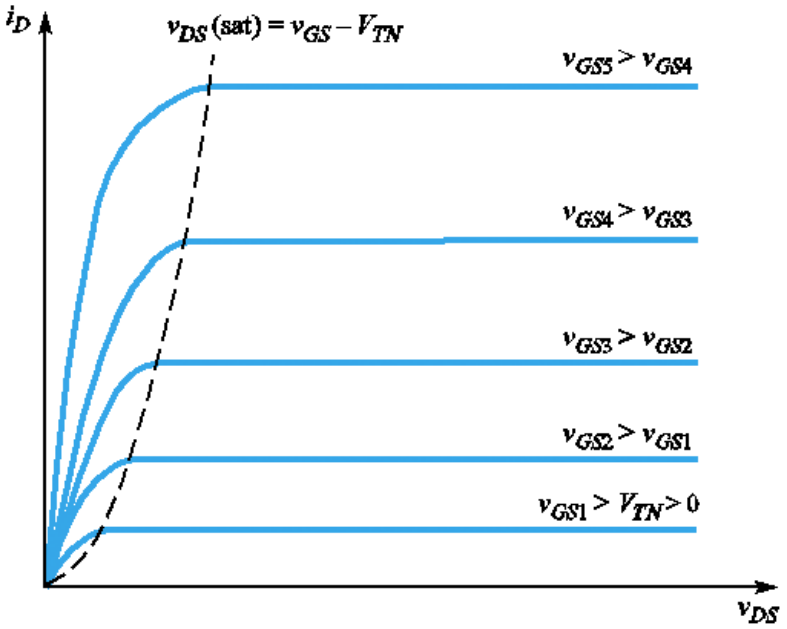


Figure 5.10 Family of i_D versus v_{DS} curves for an n-channel enhancement mode MOSFET

Conduction Parameter

- Conduction Parameter

$$K_n = \frac{W}{L} \cdot \frac{\mu_n C_{ox}}{2} \quad \text{(conduction parameter)}$$

C_{ox} : oxide capacitance per unit area $\qquad C_{ox} \propto \frac{1}{t_{ox}}, \quad t_{ox}$: oxide thickness

μ_n : electron mobility

W : channel width

L : channel length

- The conduction parameter is a function of both electrical and geometric parameters.
  - ✓ **Electrical Parameters**: The oxide capacitance and carrier mobility are essentially constants for a given technology.

$$K_n = \frac{W}{L} \cdot \frac{k_n'}{2} \qquad k_n' : \text{constant} \qquad k_n' = \mu_n C_{ox}$$

  - ✓ **Geometrical Parameters**: The width-to-length ratio (W/L) is a variable in the design of MOSFETs that is used to produce specific current-voltage characteritics in MOSFET circuits. 可用以決定電流－電壓特性。

Example 5.1 **Objective:** Calculate the current in an n-channel MOSFET.

Consider an n-channel enhancement mode MOSFET with the following parameters: $V_{TN} = 0.75\,\text{V}$, $W = 40\,\mu\text{m}$, $L = 4\,\mu\text{m}$, $\mu_n = 650\,\text{cm}^2/\text{V–s}$, $t_{ox} = 450\,\text{Å}$, and $\epsilon_{ox} = (3.9)(8.85 \times 10^{-14})\,\text{F/cm}$. Determine the current when $V_{GS} = 2V_{TN}$, for the transistor biased in the saturation region.

Solution:

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Solution:

$$K_n = \frac{W(\text{cm}) \cdot \mu_n \left(\frac{\text{cm}^2}{\text{V–s}}\right) \epsilon_{ox} \left(\frac{\text{F}}{\text{cm}}\right)}{2\,\text{L(cm)} \cdot \text{t}_{ox}(\text{cm})} = \frac{\text{F}}{\text{V–s}} = \frac{(\text{C/V})}{\text{V–s}} = \frac{\text{A}}{\text{V}^2}$$

$$K_n = \frac{W\mu_n\epsilon_{ox}}{2Lt_{ox}} = \frac{(40\times10^{-4})(650)(3.9)(8.85\times10^{-14})}{2(4\times10^{-4})(450\times10^{-8})}$$

$$= 0.249\,\text{mA/V}^2$$

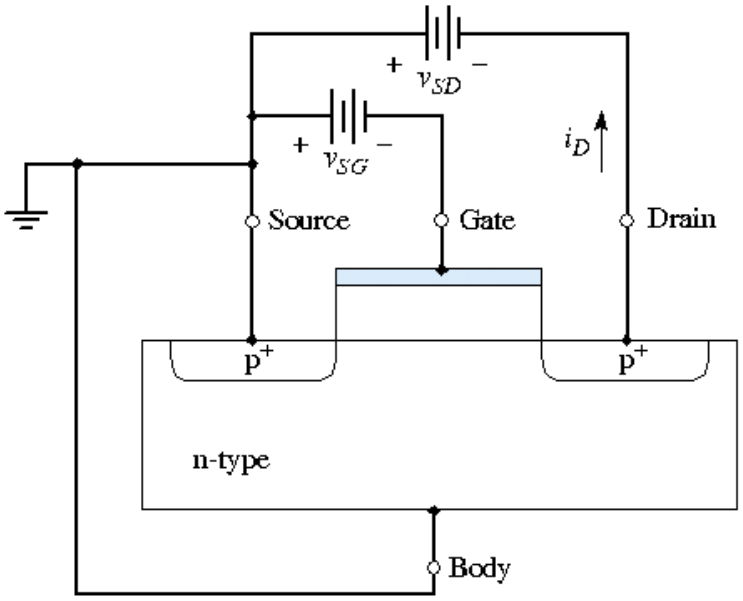
For $v_{GS} = 2V_{TN}$

$$i_D = K_n(v_{GS} - V_{TN})^2 = (0.249)(1.5-0.75)^2 = 0.140\,\text{mA}$$

Comment: The current capability of a transistor can be increased by increasing the conduction parameter. For a given fabrication technology, K_n is adjusted by varying the transistor width W.

形成電洞反轉層 ⇒ *PMOS*　　**PMOS**

- In the p-channel enhancement-mode device, a negative gate-to-source voltage must be applied to create the inversion layer of holes that connects the source and drain regions.
- The threshold voltage, denoted an V_{TP} for the PMOS is negative for an enhancement-mode devices. The threshold voltage is positive for a depletion-mode device.
- Holes flow from the source to the drain, the conventional current enters the source and leaves the drain.



(a)

(1) *G*與*D*要在低(負)電壓。
(2) 形成電洞反轉層。
(3) V_{TP}為負值
(4) 電流由*S*流向*D*。

Figure 5.15 Cross section of p-channel MOSFETs: (a) enhancement-mode and

Ideal PMOS Current-Voltage Relationship

- Nonsaturation (triode) Region

$$\text{when } v_{SD} < v_{SD(sat)} = v_{SG} + V_{TP}:$$

$$i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2] = K_p(2v_{SD(sat)}v_{SD} - v_{SD}^2)$$

- Saturation Region

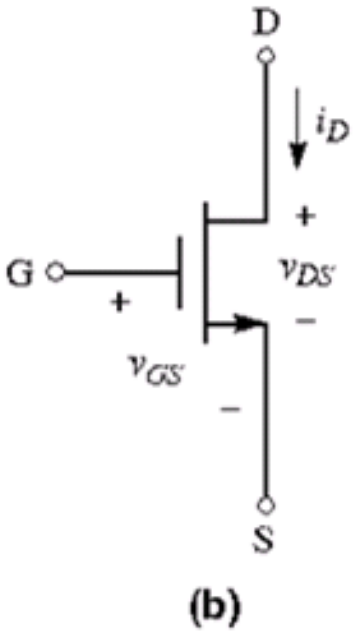
$$\text{when } v_{SD} > v_{SD(sat)} \quad (\text{also } v_{SG} + V_{TP} > 0): \qquad i_D = K_p(v_{SG} + V_{TP})^2$$

$v_{SG} > -V_{TP}$時，可分為

Nonsaturation & Saturation

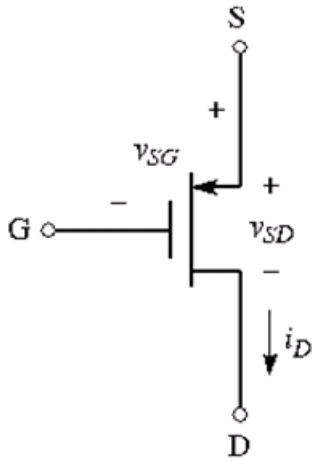
反之，若$v_{SG} < -V_{TP}$時，$i_D = 0$。

Circuit Symbols



(b)

N-channel enhancement-mode MOSFET
(npn)



P-channel enhancement-mode MOSFET
(pnp)

Summary of MOS Transistor Operation

Table 5.1 Summary of the MOSFET current–voltage relationships

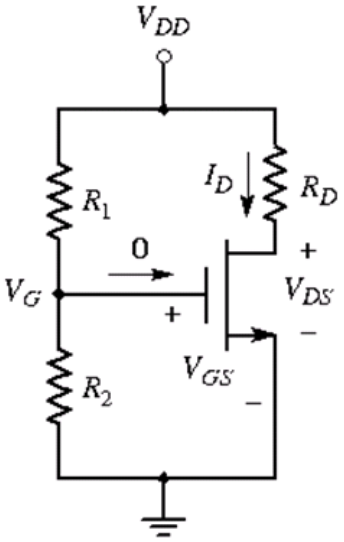
NMOS	PMOS
Nonsaturation region ($v_{DS} < v_{DS}(\text{sat})$)	Nonsaturation region ($v_{SD} < v_{SD}(\text{sat})$)
$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$	$i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2]$
Saturation region ($v_{DS} > v_{DS}(\text{sat})$)	Saturation region ($v_{SD} > v_{SD}(\text{sat})$)
$i_D = K_n(v_{GS} - V_{TN})^2$	$i_D = K_p(v_{SG} + V_{TP})^2$
Transition point	Transition point
$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$	$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$
Enhancement mode	Enhancement mode
$V_{TN} > 0$	$V_{TP} < 0$

NMOS Common-Source Circuit

Example 5.3 **Objective:** Calculate the drain current and drain-to-source voltage of a common-source circuit with an n-channel enhancement-mode MOSFET.

For the circuit shown in Figure 5.24(a), assume that $R_1 = 30\,\text{k}\Omega$, $R_2 = 20\,\text{k}\Omega$, $R_D = 20\,\text{k}\Omega$, $V_{DD} = 5\,\text{V}$, $V_{TN} = 1\,\text{V}$, and $K_n = 0.1\,\text{mA/V}^2$.

Solution:



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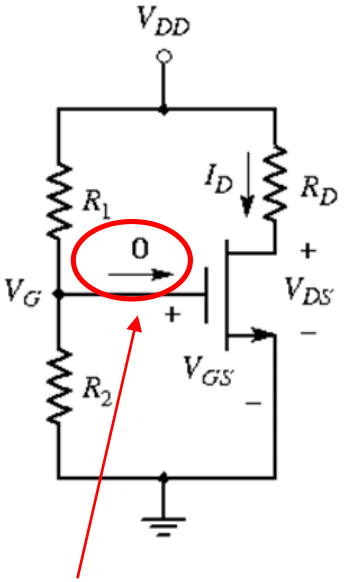


Solution:

① $V_G = V_{GS} = \left(\dfrac{R_2}{R_1 + R_2}\right) V_{DD} = \left(\dfrac{20}{20+30}\right)(5) = 2\,\text{V}$

Assuming the transistor is biased in the saturation region, the drain current is

② $I_D = K_n (V_{GS} - V_{TN})^2 = (0.1)(2-1)^2 = 0.1\text{mA}$

and the drain-to-source voltage is

③ $V_{DS} = V_{DD} - I_D R_D = 5 - (0.1)(20) = 3\,\text{V}$

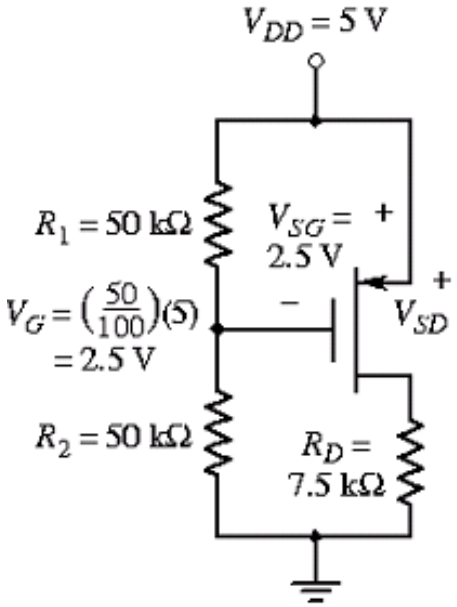
④ Check $V_{DS} > V_{GS} - V_{TN}$ $(= V_{DS,\text{sat}})$

PMOS Common-Source Circuit

Example 5.4 **Objective:** Calculate the drain current and source-to-drain voltage of a common-source circuit with a p-channel enhancement-mode MOSFET.

Consider the circuit shown in Figure 5.25(a). Assume that $R_1 = R_2 = 50\,\text{k}\Omega$, $V_{DD} = 5\,\text{V}$, $R_D = 7.5\,\text{k}\Omega$, $V_{TP} = -0.8\,\text{V}$, and $K_p = 0.2\,\text{mA/V}^2$.

Solution:



PMOS Common-Source Circuit

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Solution:

① $$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD}) = \left(\frac{50}{50+50}\right)(5) = 2.5\,\text{V}$$

The source-to-gate voltage is therefore

② $$V_{SG} = V_{DD} - V_G = 5 - 2.5 = 2.5\,\text{V}$$

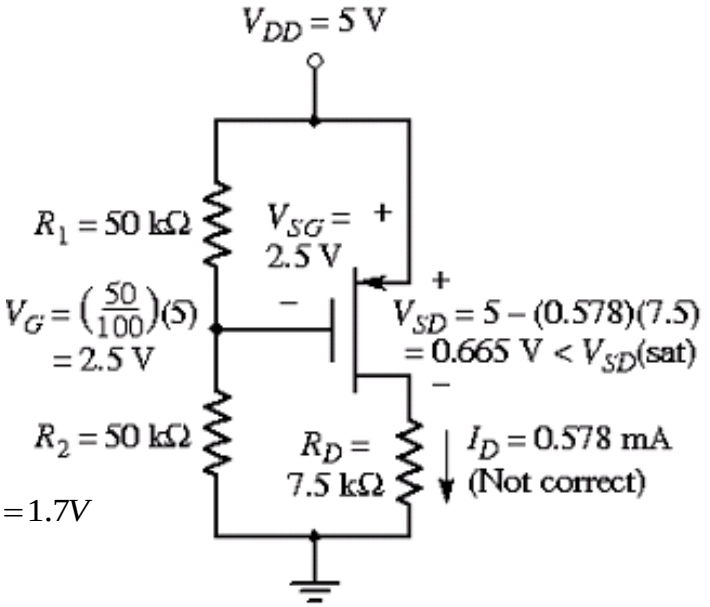
(a) Assuming the transistor is biased in the saturation region, the drain current is

$$I_D = K_p(V_{SG} + V_{TP})^2 = (0.2)(2.5-0.8)^2 = 0.578\,\text{mA}$$

and the source-to-drain voltage is

$$V_{SD} = V_{DD} - I_D R_D = 5 - (0.578)(7.5) = 0.665\,\text{V} < V_{SD,sat} = V_{SG} + V_{TP} = 2.5 - 0.8 = 1.7V$$

(假設矛盾)



(*b*) In the nonsaturation region, the drain current is given by

$$I_D = K_p\left[2(V_{SG} + V_{TP})V_{SD} - V_{SD}^2\right]$$

and the source-to-drain voltage is

$$V_{SD} = V_{DD} - I_D R_D$$

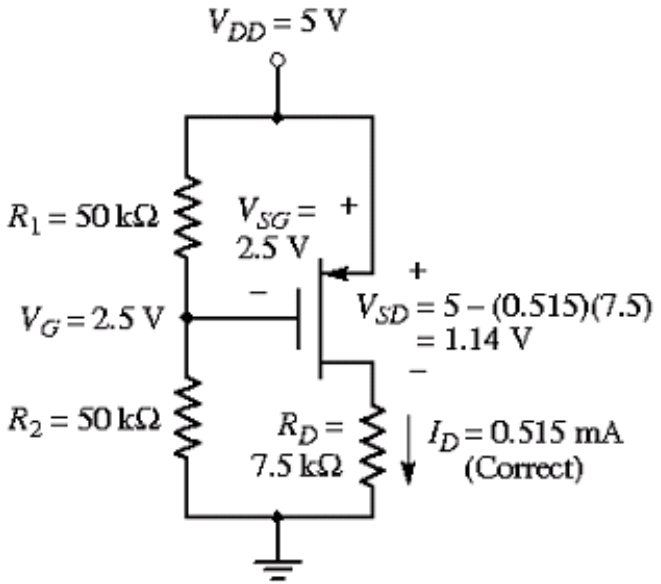
Combining these two equations, we obtain

$$I_D = K_p\left[2(V_{SG} + V_{TP})(V_{DD} - I_D R_D) - (V_{DD} - I_D R_D)^2\right]$$

$$= (0.2)\left[2(2.5-0.8)(5 - I_D(7.5)) - (5 - I_D(7.5))^2\right]$$

$$\Rightarrow I_D = 0.515\ \text{mA}$$

$V_{SD} = 1.14\ \text{V} < V_{SD,\text{sat}}$ (假設成立)



DESIGN EXAMPLE **3.5**

Objective: Design a MOSFET circuit biased with both positive and negative vo ages to meet a set of specifications.

Specifications: The circuit configuration to be designed is shown in Figure 3.2 Design the circuit such that $I_{DQ} = 0.5$ mA and $V_{DSQ} = 4$ V.

Choices: Standard resistors are to be used in the final design. A transistor with no inal parameters of $k_n' = 80\ \mu\text{A/V}^2$, $(W/L) = 6.25$, and $V_{TN} = 1.2$ V is availabl The parameters k_n' and V_{TN} may vary by ± 5 percent.

Solution:

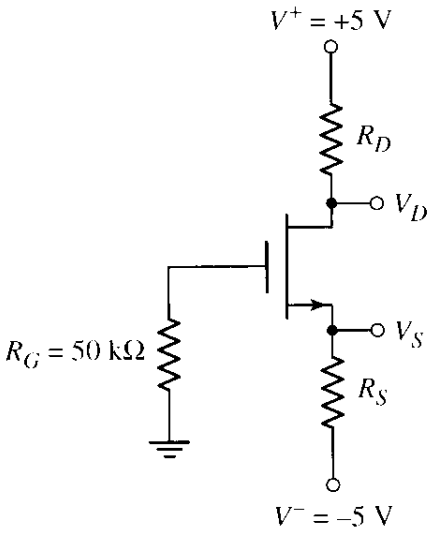


Figure 3.27 Circuit configuration for Example 3.5

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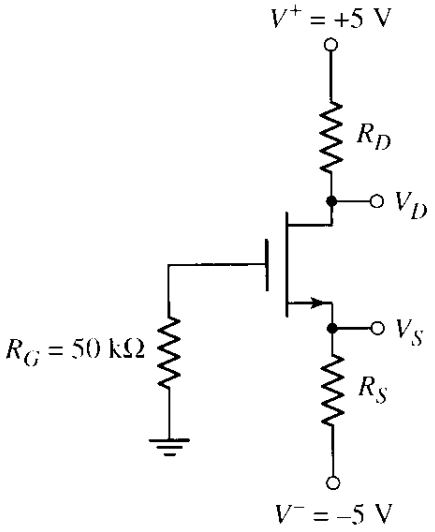


Figure 3.27 Circuit configuration for Example 3.5

Solution:

(a) The conduction parameter: $K_n = \frac{k_n'}{2} \cdot \frac{W}{L} = \frac{0.080}{2} \cdot 6.25 = 0.25\,\text{mA/V}^2$

(b) Assume the transistor is biased in the saturation region

$$I_{DQ} = K_n \left(V_{GS} - V_{TN}\right)^2 \Rightarrow V_{GS} = \sqrt{\frac{I_{DQ}}{K_n}} + V_{TN} = \sqrt{\frac{0.5}{0.25}} + 1.2 = 2.614\,\text{V}$$

(c) $I_G = 0 \Rightarrow V_G = 0 \Rightarrow V_{GS} = V_G - V_S = 0 - V_S \Rightarrow V_S = -V_{GS} = -2.614\text{V}$

(d) $V_S = V^- + I_{DQ} R_S \Rightarrow R_S = \frac{V_S - V^-}{I_{DQ}} = \frac{-2.614 - (-5)}{0.5} = 4.77\,\text{k}\Omega$

(e) $V_{DS} = V_D - V_S \Rightarrow V_D = V_S + V_{DS} = -2.614 + 4 = 1.386\,\text{V}$

(f) $V^+ = V_D + I_{DQ} R_D \Rightarrow R_D = \dfrac{V^+ - V_D}{I_{DQ}} = \dfrac{5 - 1.386}{0.5} = 7.23\,\text{k}\Omega$

(g) Check: $V_{DS} = 4\,V > V_{DS,\text{sat}} = V_{GS} - V_{TN} = 2.61 - 1.2 = 1.41\,\text{V}$

The transisitor is indeed biased in the saturation region.

DESIGN EXAMPLE 3.6

Objective: Design a circuit with a p-channel MOSFET that is biased with both positive and negative voltage supplies to meet a set of specifications.

Specifications: The circuit to be designed is shown in Figure 3.30. Design the circuit such that $I_{DQ} = 100\,\mu\text{A}$, $V_{SDQ} = 3\,\text{V}$, and $V_{RS} = 0.8\,\text{V}$. The value of the larger bias resistor, either R_1 or R_2, is to be $200\,\text{k}\Omega$.

Choices: A transistor with parameters of $K_p = 100\,\mu\text{A/V}^2$ and $V_{TP} = -0.4\,\text{V}$ is available. Standard resistor values are to be used in the final design.

Solution:

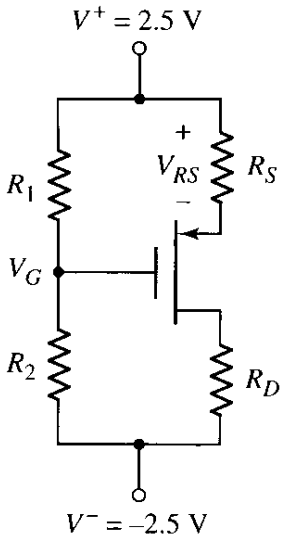


Figure 3.30 Circuit configuration for Example 3.6

DESIGN EXAMPLE 3.6

Objective: Design a circuit with a p-channel MOSFET that is biased with both positive and negative voltage supplies to meet a set of specifications.

Specifications: The circuit to be designed is shown in Figure 3.30. Design the circuit such that $I_{DQ} = 100\,\mu\text{A}$, $V_{SDQ} = 3\,\text{V}$, and $V_{RS} = 0.8\,\text{V}$. The value of the larger bias resistor, either R_1 or R_2, is to be $200\,\text{k}\Omega$.

Choices: A transistor with parameters of $K_p = 100\,\mu\text{A/V}^2$ and $V_{TP} = -0.4\,\text{V}$ is available. Standard resistor values are to be used in the final design.

Solution:

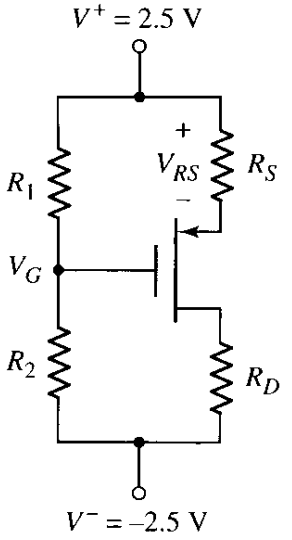


Figure 3.30 Circuit configuration for Example 3.6

(a) Assume the transistor is biased in the saturation region

$$I_{DQ} = K_n\left(V_{SG} + V_{TP}\right)^2 \Rightarrow V_{SG} = \sqrt{\frac{I_{DQ}}{K_p}} - V_{TP} = \sqrt{\frac{100}{100}} - (-0.4) = 1.4\,\text{V}$$

(b) $V_G = V^+ - V_{RS} - V_{SG} = 2.5 - 0.8 - 1.4 = 0.3\text{V}$

(c) Since $V_G = 0.3\,\text{V} > 0\text{V}$, R_2 is chosen as $200\text{k}\Omega$.

(d) $I_{Bias} = I_{R_2} = \dfrac{V_G - V^-}{R_2} = \dfrac{0.3 - (-2.5)}{200} = 0.014\,\text{mA}$

(e) $V^+ = V_G + I_{Bias} R_1 \Rightarrow R_1 = \dfrac{V^+ - V_G}{I_{Bias}} = \dfrac{2.5 - 0.3}{0.014} = 157\,\mathrm{k}\Omega$

(f) $R_S = \dfrac{V_{RS}}{I_{DQ}} = \dfrac{0.8}{0.1} = 8\,\mathrm{k}\Omega$

(g) $V_D = V^+ - V_{RS} - V_{SD} = 2.5 - 0.8 - 3 = -1.3\,\mathrm{V}$

(h) $R_D = \dfrac{V_D - V^-}{I_{DQ}} = \dfrac{-1.3 - (-2.5)}{0.1} = 12\,\mathrm{k}\Omega$

(i) Check: $V_{SD} = 3\,V > V_{SD,\mathrm{sat}} = V_{SG} + V_{TP} = 1.4 + \left(-0.4\right) = 1\,\mathrm{V}$

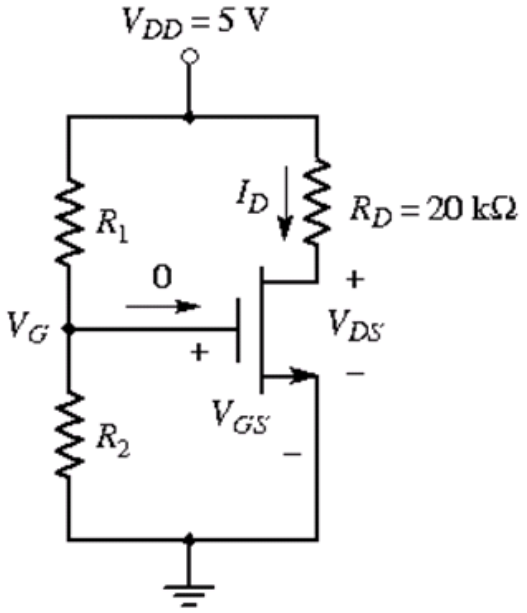
The transisitor is indeed biased in the saturation region.

Load Line

- Load Line

$$V_{DS} = V_{DD} - I_D R_D = 5 - I_D(20)$$

$$I_D = \frac{5}{20} - \frac{V_{DS}}{20}(\text{mA})$$



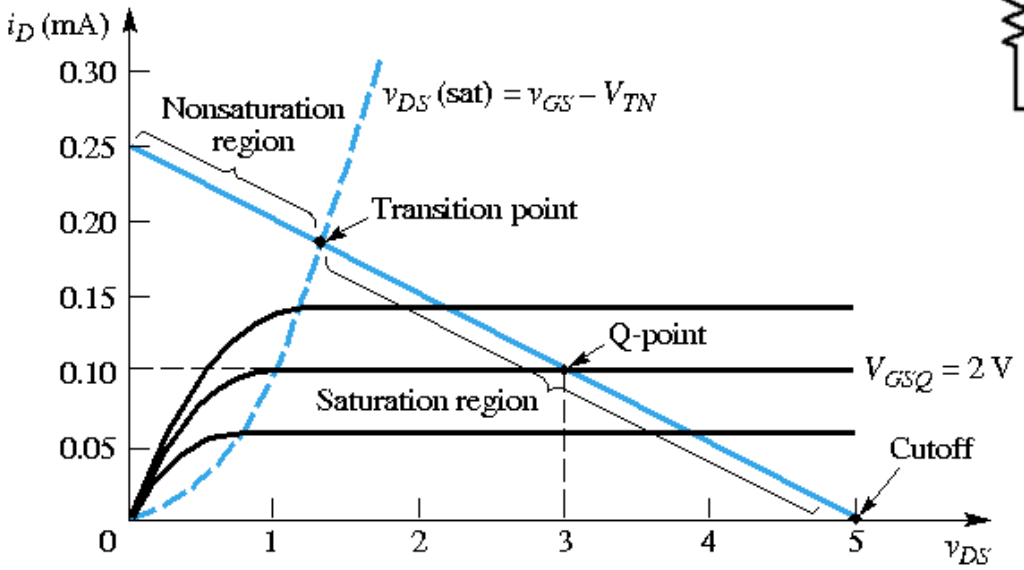
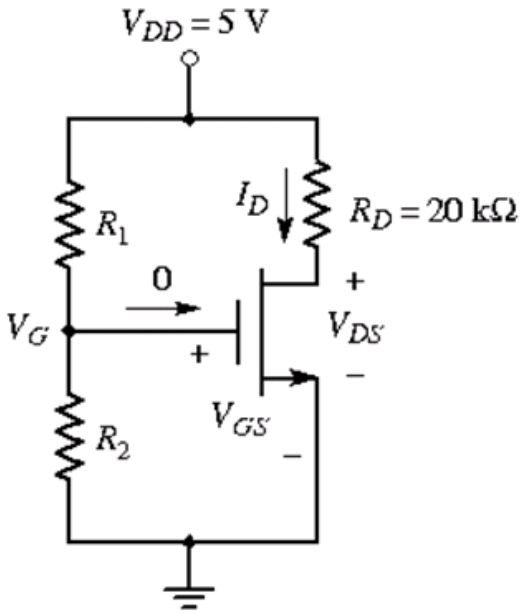


Figure 5.28 Transistor characteristics, v_{DS}(sat) curve, load line, and *Q*-point for the NMOS common-source circuit in Figure 5.24(b)

Example 5.5 **Objective:** Determine the transition point parameters for a common-source circuit.

Consider the circuit shown in Figure 5.24(b). Assume transistor parameters of $V_{TN} = 1\,\text{V}$ and $K_n = 0.1\,\text{mA/V}^2$.

Solution:



Example 5.5 **Objective:** Determine the transition point parameters for a common-source circuit.

Consider the circuit shown in Figure 5.24(b). Assume transistor parameters of $V_{TN} = 1\,\text{V}$ and $K_n = 0.1\,\text{mA/V}^2$.

Solution:

(a) $V_{DS} = V_{DS}(\text{sat}) = V_{GS} - V_{TN} = V_{DD} - I_D R_D$

(b) $I_D = K_n (V_{GS} - V_{TN})^2$

From (a) and (b), we can get

(c) $V_{GS} - V_{TN} = V_{DD} - K_n R_D (V_{GS} - V_{TN})^2$

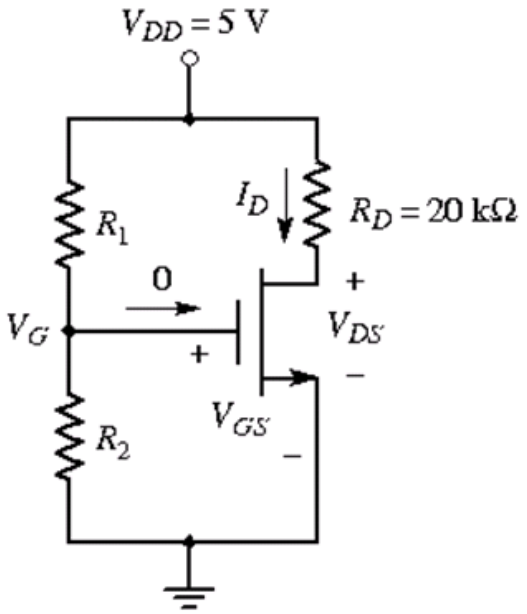
$\Rightarrow K_n R_D (V_{GS} - V_{TN})^2 + (V_{GS} - V_{TN}) - V_{DD} = 0$

$\Rightarrow (0.1)(20)(V_{GS} - V_{TN})^2 + (V_{GS} - V_{TN}) - 5 = 0$

$\Rightarrow V_{GS} - V_{TN} = 1.35\,\text{V} = V_{DS}$

(d) $V_{GS} = 2.35\,\text{V}$

(e) $I_D = (0.1)(2.35 - 1)^2 = 0.182\,\text{mA}$



DESIGN EXAMPLE **3.8**

Objective: Design the dc bias of a MOSFET circuit to meet a set of specifications.

Specifications: The circuit configuration to be designed is shown in Figure 3.34. The quiescent Q-point values are to be $I_{DQ} = 0.25\,\text{mA}$ and $V_{DSQ} = 4\,\text{V}$. The voltage across R_S should be $V_{RS} \cong 1\,\text{V}$. The current in the bias resistors should be approximately 20 μA.

Choices: Discrete resistors are to be used in the final design. A transistor with parameters of $k_n' = 80\ \mu\text{A/V}^2$, $W/L = 4$, and $V_{TN} = 1.2\,\text{V}$ is available. The resistors R_D and R_S have tolerances of ± 10 percent.

Solution:

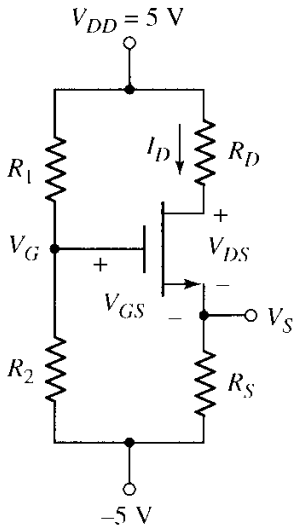


Figure 3.34 NMOS common-source circuit with source resistor

DESIGN EXAMPLE **3.8**

Objective: Design the dc bias of a MOSFET circuit to meet a set of specifications.

Specifications: The circuit configuration to be designed is shown in Figure 3.34. The quiescent Q-point values are to be $I_{DQ} = 0.25\,\text{mA}$ and $V_{DSQ} = 4\,\text{V}$. The voltage across R_S should be $V_{RS} \cong 1\,\text{V}$. The current in the bias resistors should be approximately 20 μA.

Choices: Discrete resistors are to be used in the final design. A transistor with parameters of $k_n' = 80\ \mu\text{A/V}^2$, $W/L = 4$, and $V_{TN} = 1.2\,\text{V}$ is available. The resistors R_D and R_S have tolerances of ± 10 percent.

Solution:

$$\text{(a)}\ R_S = \frac{V_{RS}}{I_{DQ}} = \frac{1}{0.25} = 4\,\text{k}\Omega$$

$$\text{(b)}\ 5 = I_{DQ}R_D + V_{DS} + I_{DQ}R_S - 5$$

$$\Rightarrow 5 = (0.25)R_D + 4 + (0.25)(4) - 5$$

$$\Rightarrow R_D = 20\,\text{k}\Omega$$

$$\text{(c)}\ 5 - (-5) = I_{Bias} \times (R_1 + R_2)$$

$$\Rightarrow R_1 + R_2 = \frac{5+5}{0.020} = 500\,\text{k}\Omega$$

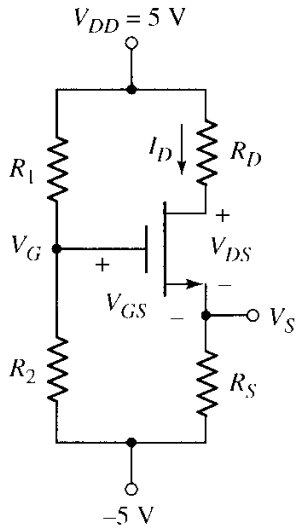


Figure 3.34 NMOS common-source circuit with source resistor

(d) Assume the transistor is in the saturation region

$$I_D = \frac{k_n'}{2}\frac{W}{L}\left(V_{GS} - V_{TN}\right)^2$$

$$\Rightarrow 0.25 = \frac{0.080}{2}\cdot 4(V_{GS} - 1.2)^2$$

$$\Rightarrow V_{GS} = 2.45\,\text{V}$$

(e) $$V_{GS} = V_G - V_S = \left[\left(\frac{R_2}{R_1 + R_2}\right)(10) - 5\right] - \left[I_D R_S - 5\right]$$

$$\Rightarrow 2.45 = \left[\left(\frac{R_2}{500}\right)(10) - 5\right] - \left[(0.25)(4) - 5\right]$$

$$\Rightarrow R_2 = 172.5\,\text{k}\Omega$$

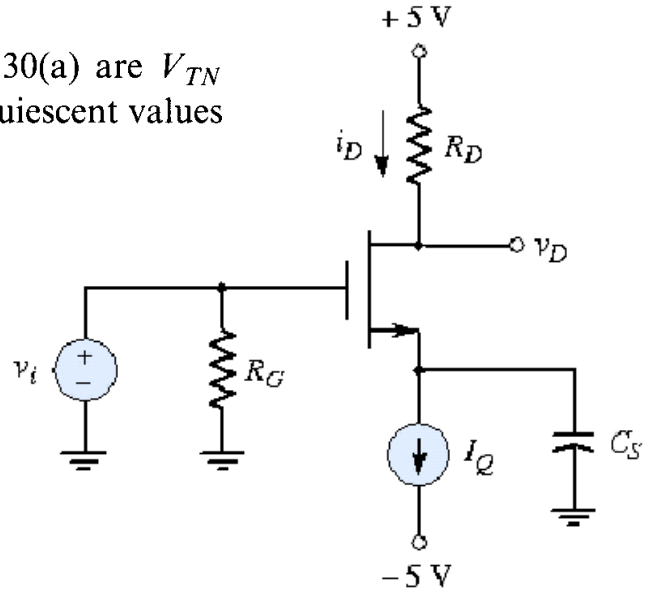
(f) From (c) and (e), we can get

$$R_1 = 327.5\,\text{k}\Omega$$

Design Example 5.7 **Objective:** Design a MOSFET circuit biased with a constant-current source.

The parameters of the transistor in the circuit shown in Figure 5.30(a) are $V_{TN} = 0.8\,\text{V}$, $k_n' = 80\,\mu\text{A/V}^2$, and $W/L = 3$. Design the circuit such that the quiescent values are $I_D = 250\,\mu\text{A}$ and $V_D = 2.5\,\text{V}$.

Solution:



(a)

Design Example 5.7 **Objective:** Design a MOSFET circuit biased with a constant-current source.

The parameters of the transistor in the circuit shown in Figure 5.30(a) are $V_{TN} = 0.8\,\text{V}$, $k_n' = 80\,\mu\text{A/V}^2$, and $W/L = 3$. Design the circuit such that the quiescent values are $I_D = 250\,\mu\text{A}$ and $V_D = 2.5\,\text{V}$.

Solution:

(a) The DC equivalent circuit is shown in Fig (b) by setting $v_i = 0$.

(b) Assume the transistor is in the saturation region

$$I_D = \frac{k_n'}{2}\frac{W}{L}\left(V_{GS} - V_{TN}\right)^2$$

$$\Rightarrow 250 = \left(\frac{80}{2}\right)\cdot(3)(V_{GS} - 0.8)^2$$

$$\Rightarrow V_{GS} = 2.24\,\text{V}$$

(c) $V_{GS} = V_G - V_S = 0 - V_S = 2.24\,\text{V}$

$$\Rightarrow V_S = -2.24\,\text{V}$$

(d) $V_D + I_D R_D = 5$

$$\Rightarrow 2.5 + (0.25)R_D = 5$$

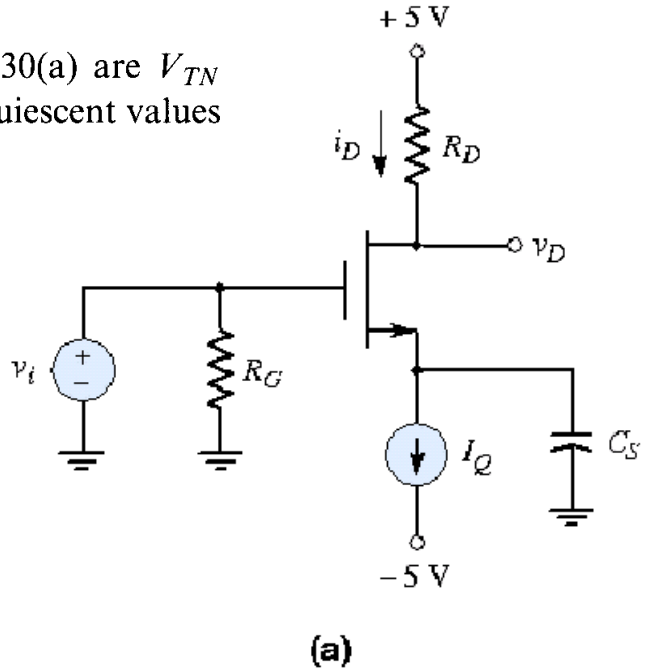
$$\Rightarrow R_D = 10\,\text{k}\Omega$$

(e) $V_{DS} = V_D - V_S = 2.5 - (-2.24) = 4.74\,\text{V}$

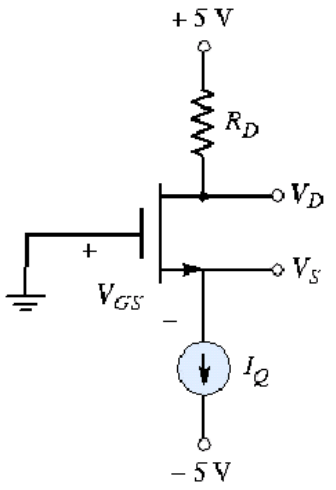
(f) Check: $V_{DS} = V_D - V_S = 2.5 - \left(-2.24\right) = 4.74\,\text{V}$

$$V_{DS,sat} = V_{GS} - V_{TN} = 2.24 - 0.8 = 1.44\text{V}$$

$V_{DS} > V_{DS,sat} \Rightarrow$ The transistor is based the saturation region.



(a)



(b)

Nonlinear Resistor

- An enhancement-mode MOSFET is used as a nonlinear resistor.
- The transistor is always biased in the saturation region and called a load device.

$$v_{DS} = v_{GS} > v_{DS(Sat)} = v_{GS} - V_{TN}, \quad V_{TN} > 0$$

$$i_D = K_n(v_{GS} - V_{TN})^2 = K_n(v_{DS} - V_{TN})^2$$

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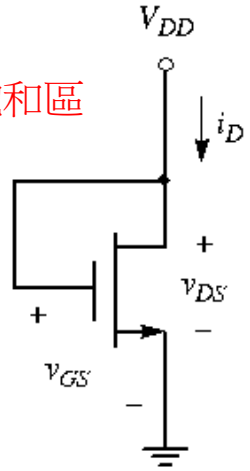


Figure 5.32 Enhancement-mode NMOS device with the gate connected to the drain

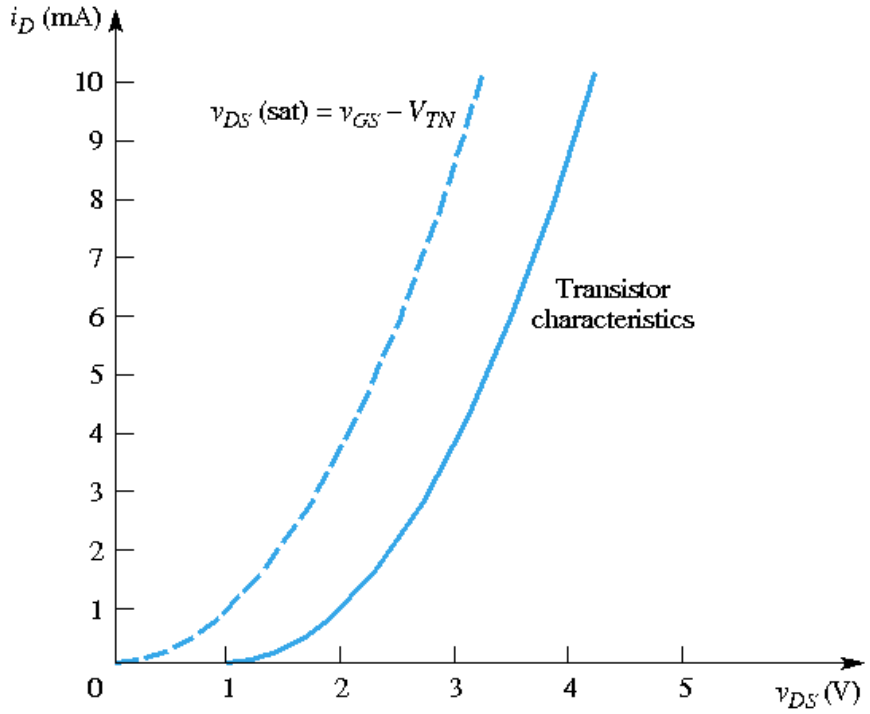


Figure 5.33 Current–voltage characteristic of an enhancement load device

Example 5.8 **Objective:** Calculate the characteristics of a circuit containing an enhancement load device.

Consider the circuit shown in Figure 5.34 with transistor parameters $V_{TN} = 0.8\,\text{V}$ and $K_n = 0.05\,\text{mA/V}^2$.

Solution:

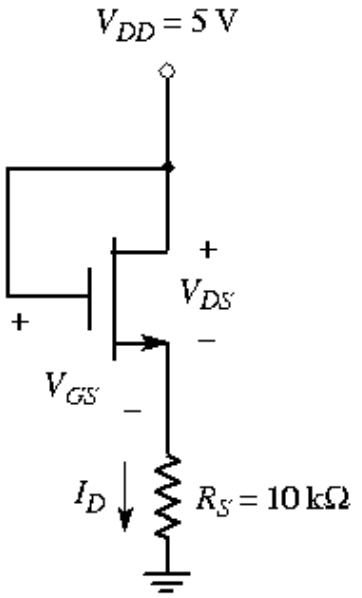


Figure 5.34 Circuit containing an enhancement load device

Example 5.8 **Objective:** Calculate the characteristics of a circuit containing an enhancement load device.

Consider the circuit shown in Figure 5.34 with transistor parameters $V_{TN} = 0.8\,\text{V}$ and $K_n = 0.05\,\text{mA/V}^2$.

Solution:

(a) The transistor must be based in the saturation region

$$I_D = K_n(V_{GS} - V_{TN})^2$$

(b) $V_{DS} = V_{GS} = 5 - I_D R_S$

(c) From (a) and (b), we can get

$$V_{GS} = 5 - K_n R_S (V_{GS} - V_{TN})^2$$

$$\Rightarrow V_{GS} = 5 - (0.05)(10)(V_{GS} - 0.8)^2$$

$$\Rightarrow V_{GS} = -3.27\,\text{V} \text{ (矛盾, } V_{GS} < V_{TN}) \text{ or } V_{GS} = +2.87\,\text{V}$$

(d) $V_{GS} = V_{DS} = 2.87\,\text{V}$ and $I_D = 0.213\,\text{mA}$

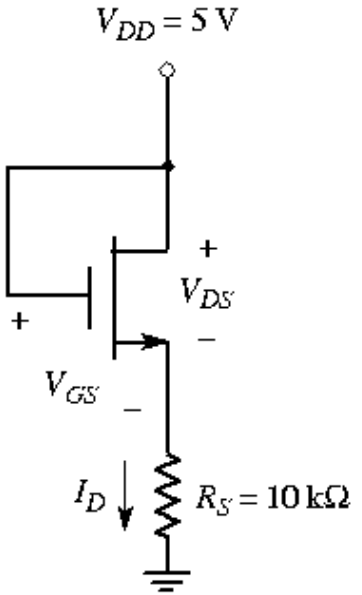
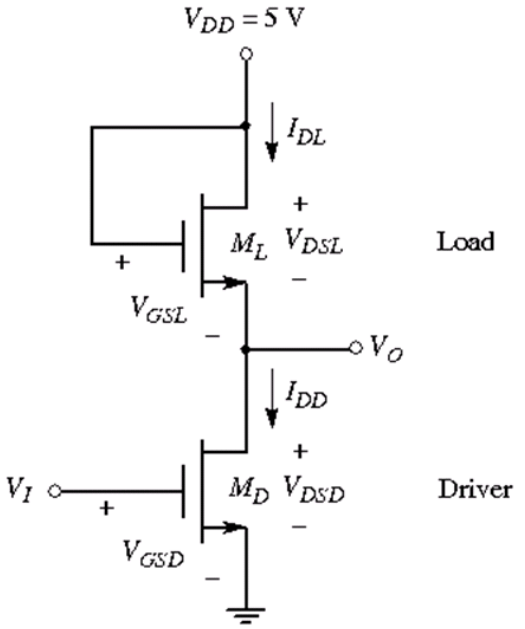


Figure 5.34 Circuit containing an enhancement load device

Example 5.9 **Objective:** Determine the dc transistor currents and voltages in a circuit containing an enhancement load device.

The transistors in the circuit shown in Figure 5.35 have parameters $V_{TND} = V_{TNL} = 1\,\text{V}$, $K_{nD} = 50\,\mu\text{A/V}^2$, and $K_{nL} = 10\,\mu\text{A/V}^2$. (The subscript D applies to the driver transistor and the subscript L applies to the load transistor.) Determine V_O for $V_I = 5\,\text{V}$ and $V_I = 1.5\,\text{V}$.

Solution:



Example 5.9 **Objective:** Determine the dc transistor currents and voltages in a circuit containing an enhancement load device.

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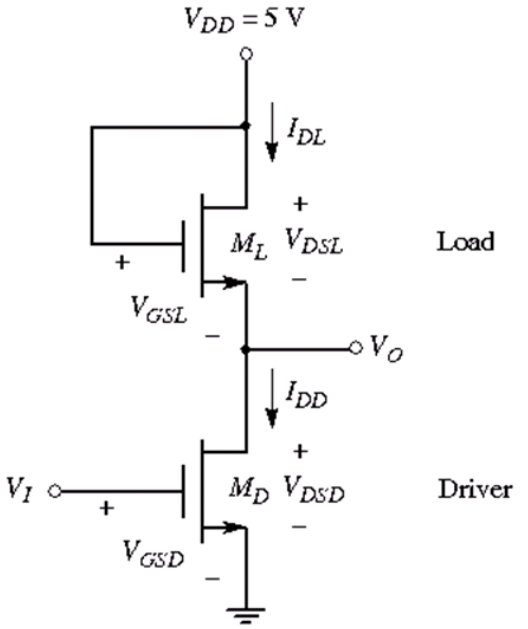


Solution:

(1) $V_I = 5\text{V}$

(a) Assume that the transistor M_D is baised in the non-saturation region.

$$I_{DD} = I_{DL}$$

$$\Rightarrow K_{nD}\left[2\left(V_{GSD} - V_{TND}\right)V_{DSD} - V_{DSD}^2\right] = K_{nL}\left[V_{GSL} - V_{TNL}\right]^2$$

$$\Rightarrow K_{nD}\left[2\left(V_I - V_{TND}\right)V_O - V_O^2\right] = K_{nL}\left[V_{DD} - V_O - V_{TNL}\right]^2$$

$$\Rightarrow (50)\left[2(5-1)V_O - V_O^2\right] = (10)\left[5 - V_O - 1\right]^2$$

$$\Rightarrow 3V_O^2 - 24V_O + 8 = 0$$

$$\Rightarrow V_O = 7.65\,\text{V}\ (\text{矛盾, } V_O > V_{DD}) \quad \text{or} \quad V_O = 0.349\,\text{V}$$

(b) $I_D = K_{nL}\left(V_{GSL} - V_{TNL}\right)^2 = K_{nL}\left(V_{DD} - V_O - V_{TNL}\right)^2$

$$\Rightarrow I_D = (10)(5 - 0.349 - 1)^2 = 133\,\mu\text{A}$$

(c) Check: $V_{DS} = V_O = 0.349\,\text{V}$

$$V_{DS,sat} = V_{GS} - V_{TN} = 5 - 1 = 4\text{V}$$

$V_{DS} < V_{DS,sat} \Rightarrow$ The transistor M_D is based the non-saturation region.

(2) $V_I = 1.5\text{V}$

(a) Assume that the transistor M_D is baised in the saturation region.

$$I_{DD} = I_{DL}$$

$$\Rightarrow K_{nD}\left[V_{GSD} - V_{TND}\right]^2 = K_{nL}\left[V_{GSL} - V_{TNL}\right]^2$$

$$\Rightarrow K_{nD}\left[V_I - V_{TND}\right]^2 = K_{nL}\left[V_{DD} - V_O - V_{TNL}\right]^2$$

$$\Rightarrow \sqrt{50}\left[1.5 - 1\right] = \sqrt{10}\left[5 - V_O - 1\right]$$

(b) $I_D = K_{nD}\left(V_{GSD} - V_{TND}\right)^2 = (50)(1.5-1)^2 = 12.5\,\mu\text{A}$

(c) Check: $V_{DS} = V_O = 2.88\,\text{V}$

$$V_{DS,sat} = V_{GS} - V_{TN} = 1.5 - 1 = 0.5\text{V}$$

$V_{DS} > V_{DS,sat} \Rightarrow$ The transistor M_D is based the saturation region.

NMOS Inverter

- If $v_I < V_{TN}$, the transistor is in cut-off.

$$i_D = 0$$
$$v_O = V_{DD}$$

- If $v_I > V_{TN}$ (and make $v_I - V_{TN} > v_{DS}$), the transistor is biased in the non-saturation region.

$$i_D = K_n[2(v_I - V_{TN})v_O - v_O^2]$$
$$v_O = v_{DD} - i_D R_D$$

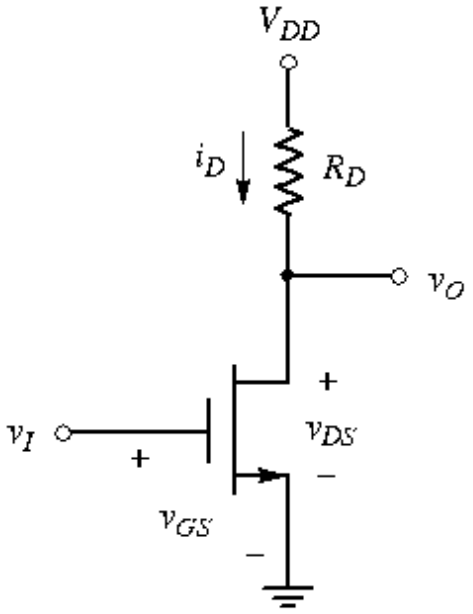
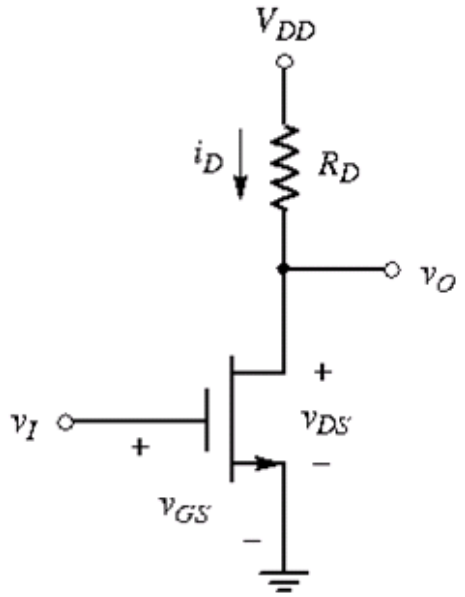


Figure 5.44 NMOS inverter circuit

Design Example 5.14 **Objective:** Design the size of a power MOSFET to meet the specification of a particular switch application.

The load in the inverter circuit in Figure 5.44 is a coil of an electromagnet that requires a current of 0.5 A when turned on. The effective load resistance varies between 8 and 10 Ω, depending on temperature and other variables. A 10 V power supply is available. The transistor parameters are $k_n' = 80\,\mu A/V^2$ and $V_{TN} = 1\,V$.

Solution:



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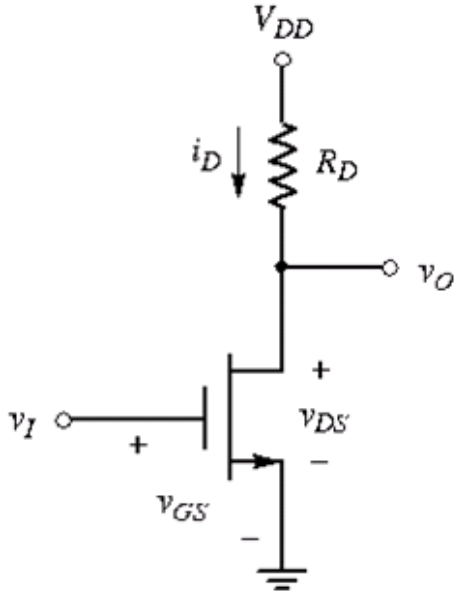
Solution:

(a) The solution is to bias the transistor in the saturation region.

$\Rightarrow$ The current is constant, independent of the load resistence.



(b) $V_0 = V_{DD} - I_D R_D = \begin{cases} 10 - 0.5\times 8 = 6\text{V} \\ 10 - 0.5\times 10 = 5\text{V} \end{cases}$

$V_{DS,\min} = 5\text{V}$

(c) Need $V_{DS,\min} \geq V_{DS,\text{sat}} = V_{GS} - V_{TN}$

$\Rightarrow$ Always in the saturation region

Choose $V_{GS} = 5\text{V}$

(d) $I_D = \frac{k_n'}{2}\frac{W}{L}\left(V_{GS} - V_{TN}\right)^2$

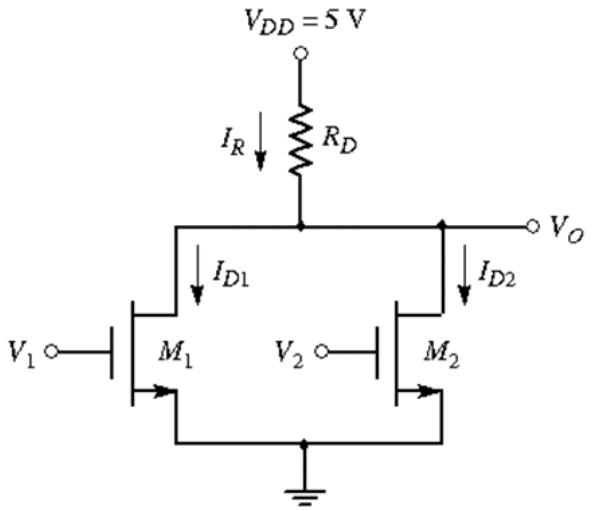
$\Rightarrow 0.5 = \frac{80\times 10^{-6}}{2}\frac{W}{L}(5-1)^2 \Rightarrow \frac{W}{L} = 781$

Digital Logic Gate

Example 5.15 **Objective:** Determine the currents and voltages in a digital logic gate, for various input conditions.

Consider the circuit shown in Figure 5.46 with circuit and transistor parameters $R_D = 20\,\text{k}\Omega$, $K_n = 0.1\,\text{mA/V}^2$, and $V_{TN} = 0.8\,\text{V}$.

Solution:

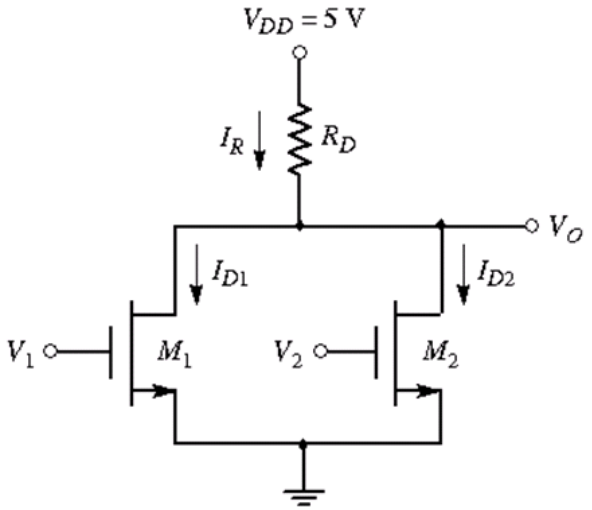


Digital Logic Gate

Digital Logic Gate

Example 5.15 **Objective:** Determine the currents and voltages in a digital logic gate, for various input conditions.

Consider the circuit shown in Figure 5.46 with circuit and transistor parameters $R_D = 20\,\text{k}\Omega$, $K_n = 0.1\,\text{mA/V}^2$, and $V_{TN} = 0.8\,\text{V}$.



Solution:

(a) $V_1 = V_2 = 0\text{V} \Rightarrow M_1, M_2$ are both cut off

$V_0 = V_{DD} = 5\text{V}$

(b) $V_1 = 5\text{V}, V_2 = 0\text{V}$

$\Rightarrow M_2$ is cut off, $I_{D2} = 0$

(1) Assume M_1 is in the saturation region

$$I_{D1} = K_n\left(V_{GS1} - V_{TN}\right)^2 = 0.1(5 - 0.8)^2 = 1.764\text{V}$$

$$I_R = I_{D1} + I_{D2} = I_{D1}$$

$$V_{DS1} = V_0 = V_{DD} - I_R R_D = 5 - 1.764 \times 20 = 1.8\,\text{V}$$

$$V_{DS1} < V_{DS1,\text{sat}} = V_{GS1} - V_{TN} = 4.2\,\text{V}$$ (假設矛盾)

(2) Assume M_1 is in the non-saturation region

$$I_R = I_{D1} \Rightarrow \frac{5 - V_0}{R_D} = K_n\left[2\left(V_1 - V_{TN}\right)V_0 - V_0^2\right]$$

$$V_0 = 0.29\text{V} = V_{DS1},\ I_R = I_{D1} = \frac{5 - V_0}{R_D} = \frac{5 - 0.29}{20} = 0.236\text{mA}$$

$$V_{DS1} < V_{DS1,\text{sat}} = V_{GS1} - V_{TN} = 4.2\,\text{V}$$ (假設成立)

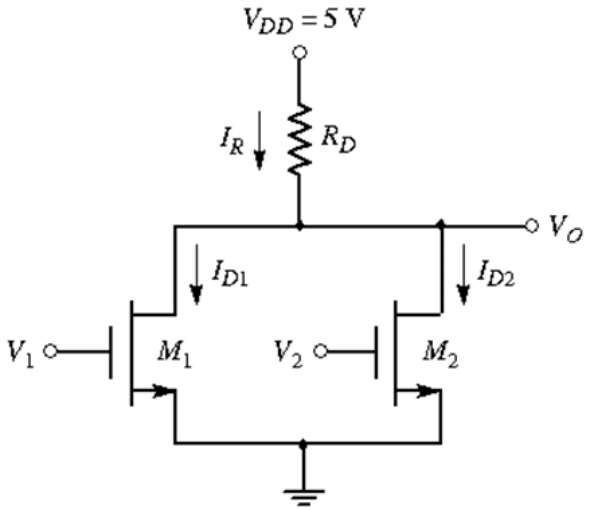
Digital Logic Gate

(c) $V_1 = 0\text{V}, V_2 = 5\text{V}$

M_1 is cut off, $I_{D1} = 0$

M_2 is in the non-saturation region

$\Rightarrow V_0 = 0.29\text{V}, I_R = I_{D2} = 0.236\text{mA}$



(d) $V_1 = 5\text{V}, V_2 = 5\text{V}$

M_1 and M_2 are both in the non-saturation region

$I_R = I_{D1} + I_{D2}$

$$\Rightarrow \frac{5 - V_0}{R_D} = K_n\left[2(V_1 - V_{TN})V_0 - V_0^2\right] + K_n\left[2(V_2 - V_{TN})V_0 - V_0^2\right]$$

$\Rightarrow V_0 = 0.147\text{V}$

$$I_R = \frac{5 - 0.147}{20} = 0.243\text{mA}$$

$$I_{D1} = I_{D2} = \frac{I_R}{2} = 0.121\text{mA}$$

MOS Small-Signal Amplifier

- We can establish a particular Q-point on the load line by designing the ratio of the bias resistors R_1 and R_2.

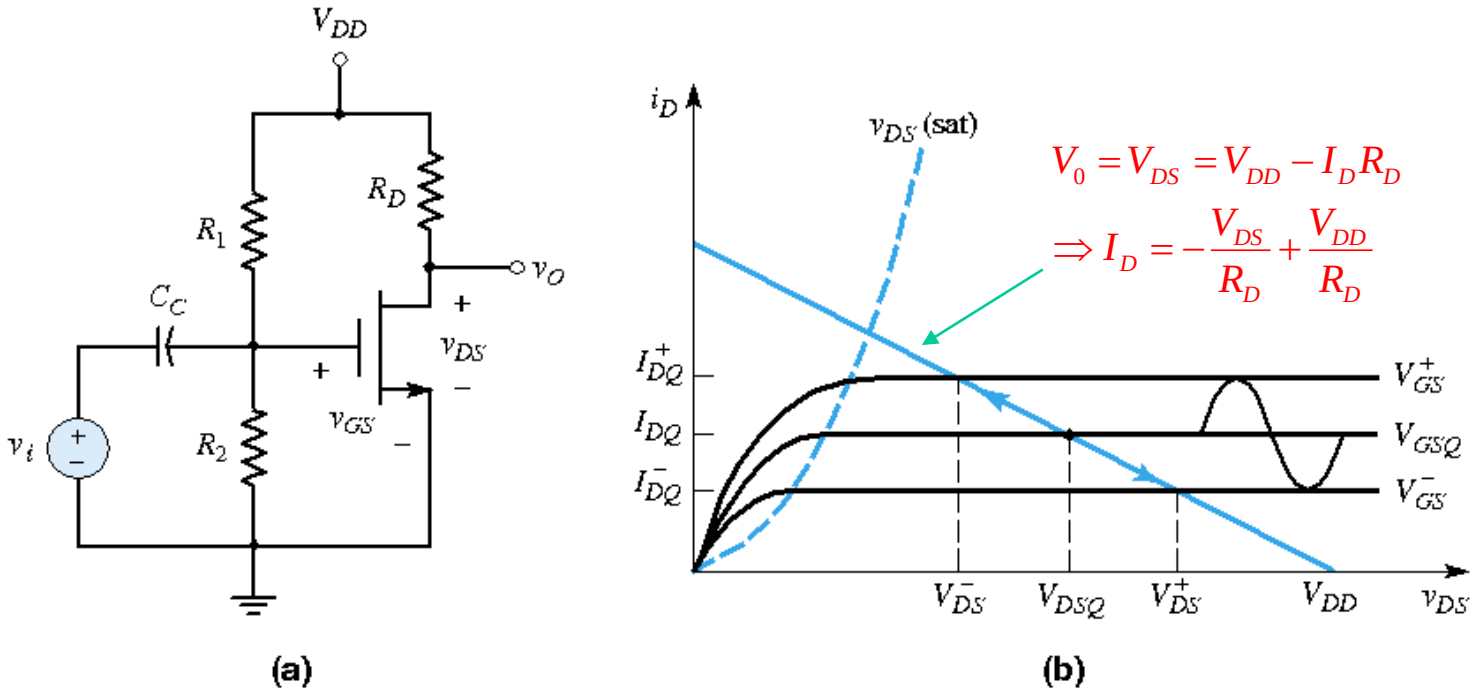


Figure 5.47 (a) An NMOS common-source circuit with a time-varying signal coupled to the gate and (b) transistor characteristics, load line, and superimposed sinusoidal signals

Constant-Current Biasing

EXAMPLE **3.17**

Objective: Analyze the circuit shown in Figure 3.53(a). Determine the bias current I_{Q1}, the gate-to-source voltages of the transistors, and the drain-to-source voltage of M_1.

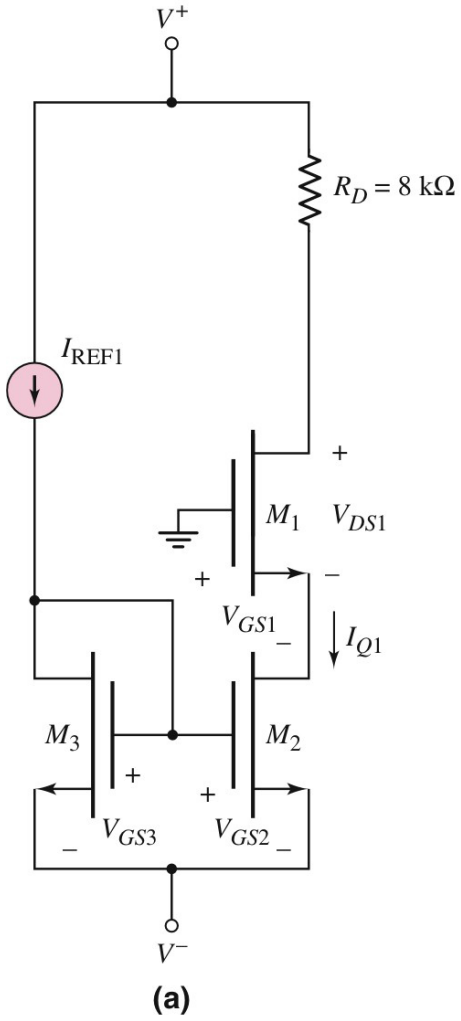
Assume circuit parameters of $I_{REF1} = 200\ \mu A$, $V^+ = 2.5$ V, and $V^- = -2.5$ V. Assume transistor parameters of $V_{TN} = 0.4$ V (all transistors), $\lambda = 0$ (all transistors), $K_{n1} = 0.25$ mA/V^2, and $K_{n2} = K_{n3} = 0.15$ mA/V^2.

Solution:

實際上，於飽和狀態下的電流公式：

$$I_D = K_n\left[\left(V_{GS} - V_{TN}\right)^2\left(1+\lambda V_{DS}\right)\right]$$

但λ值通常很小，可忽略。



(a)

Comment: Since the current mirror transistors M_2 and M_3 are matched (identical parameters) and since the gate-to-source voltages are the same in the two transistors, the bias current, I_{Q1}, is equal to (i.e., mirrors) the reference current, I_{REF1}.

Constant-Current Biasing

EXAMPLE 3.17

Objective: Analyze the circuit shown in Figure 3.53(a). Determine the bias current I_{Q1}, the gate-to-source voltages of the transistors, and the drain-to-source voltage of M_1.

Assume circuit parameters of $I_{REF1} = 200\ \mu A$, $V^+ = 2.5$ V, and $V^- = -2.5$ V. Assume transistor parameters of $V_{TN} = 0.4$ V (all transistors), $\lambda = 0$ (all transistors), $K_{n1} = 0.25$ mA/V^2, and $K_{n2} = K_{n3} = 0.15$ mA/V^2.

Solution:

(a) $I_{D3} = I_{REF1} = 200\mu A$

(b) M_3 must be biased in the saturation region.

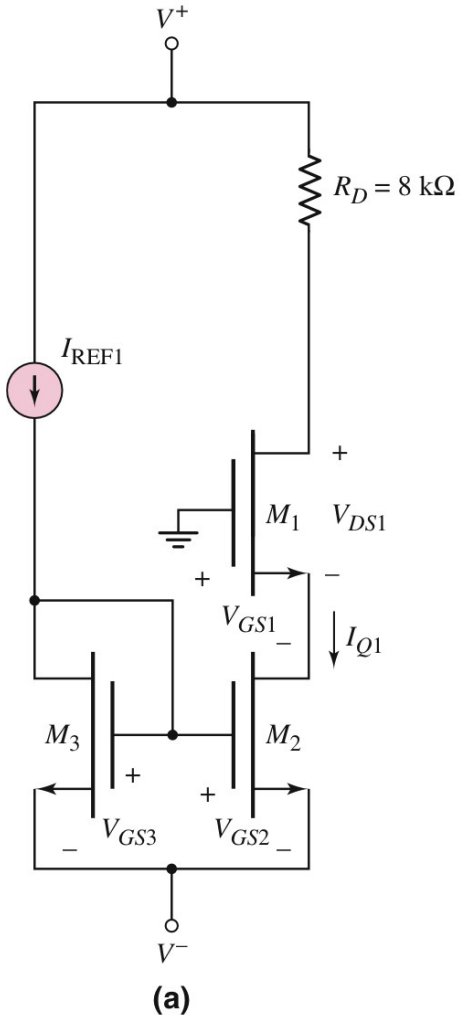
$$I_{D3} = K_{n3}\left(V_{GS3} - V_{TN}\right)^2$$

$$\Rightarrow V_{GS3} = \sqrt{\frac{I_{D3}}{K_{n3}}} + V_{TN} = \sqrt{\frac{0.2}{0.15}} + 0.4 = 1.555V$$

(c) $V_{GS3} = V_{GS2} = 1.555V$

Assume M_2 is biased in the saturation region

$$I_{D2} = I_{Q1} = K_{n2}\left(V_{GS2} - V_{TN}\right)^2 = 0.15\left(1.555 - 0.4\right)^2 = 200\mu A$$



(d) Assume M_1 is biased in the saturation region

$$I_{D1} = I_{Q1} = K_{n1}\left(V_{GS1} - V_{TN}\right)^2$$

$$\Rightarrow V_{GS1} = \sqrt{\frac{I_{Q1}}{K_{n1}}} + V_{TN} = \sqrt{\frac{0.2}{0.25}} + 0.4 = 1.29\,\text{V}$$

(e) $$V_{DS1} = V^+ - I_{Q1}R_D - V_{S1}$$

$$= V^+ - I_{Q1}R_D - (-V_{GS1})$$

$$= 2.5 - (0.2)(8) - (-1.29) = 2.19\,\text{V}$$

(f) Check: $V_{DS1} = 2.19\,\text{V} > V_{DS1,\text{sat}} = V_{GS1} - V_{TN} = 1.29 - 0.4 = 0.89\text{V}$

The transistor M_1 is indeed based the saturation region

$$V_{DS2} = V_{D2} - V_{S2} = V_{S1} - V^- = -1.29 - \left(-2.5\right) = 1.21\text{V}$$

$$V_{DS2} > V_{DS2,\text{sat}} = V_{GS2} - V_{TN} = 1.555 - 0.4 = 1.155\text{V}$$

The transistor M_2 is indeed based the saturation region

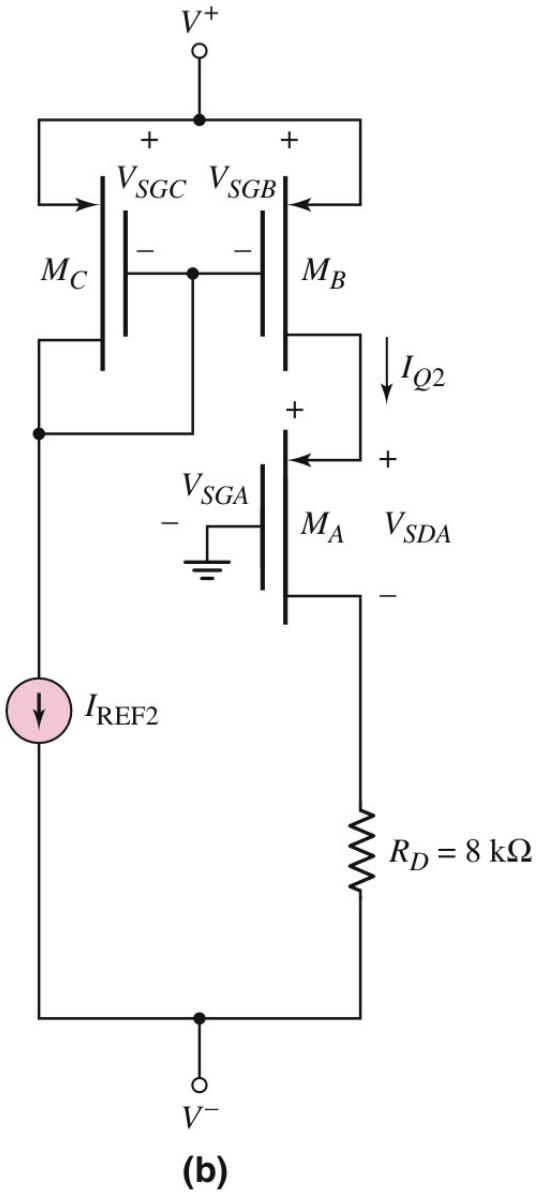
Comment: Since the current mirror transistors M_2 and M_3 are matched (identical parameters) and since the gate-to-source voltages are the same in the two transistors, the bias current, I_{Q1}, is equal to (i.e., mirrors) the reference current, I_{REF1}.

EXAMPLE **3.18**

Objective: Design the circuit shown in Figure 3.53(b) to provide a bias current of $I_{Q2} = 150\ \mu A$.

Assume circuit parameters of $I_{REF2} = 250\ \mu A$, $V^+ = 3$ V, and $V^- = -3$ V. Assume transistor parameters of $V_{TP} = -0.6$ V (all transistors), $\lambda = 0$ (all transistors), $k'_p = 40\ \mu A/V^2$ (all transistors), $W/L_C = 15$, and $W/L_A = 25$.

Solution:



(b)

EXAMPLE 3.18

Objective: Design the circuit shown in Figure 3.53(b) to provide a bias current of $I_{Q2} = 150\ \mu A$.

Assume circuit parameters of $I_{REF2} = 250\ \mu A$, $V^+ = 3$ V, and $V^- = -3$ V. Assume transistor parameters of $V_{TP} = -0.6$ V (all transistors), $\lambda = 0$ (all transistors), $k_p' = 40\ \mu A/V^2$ (all transistors), $W/L_C = 15$, and $W/L_A = 25$.

Solution:

(1) $I_{Q2} \neq I_{REF2} \Rightarrow \left(\frac{W}{L}\right)_B \neq \left(\frac{W}{L}\right)_C$

(2) M_C must be biased in the saturation region.

$$I_{DC} = I_{REF2} = \frac{k_n'}{2} \cdot \left(\frac{W}{L}\right)_C \left(V_{SGC} + V_{TP}\right)^2$$

$$\Rightarrow 250 = \frac{40}{2}(15)\left[V_{SGC} + (-0.6)\right]^2$$

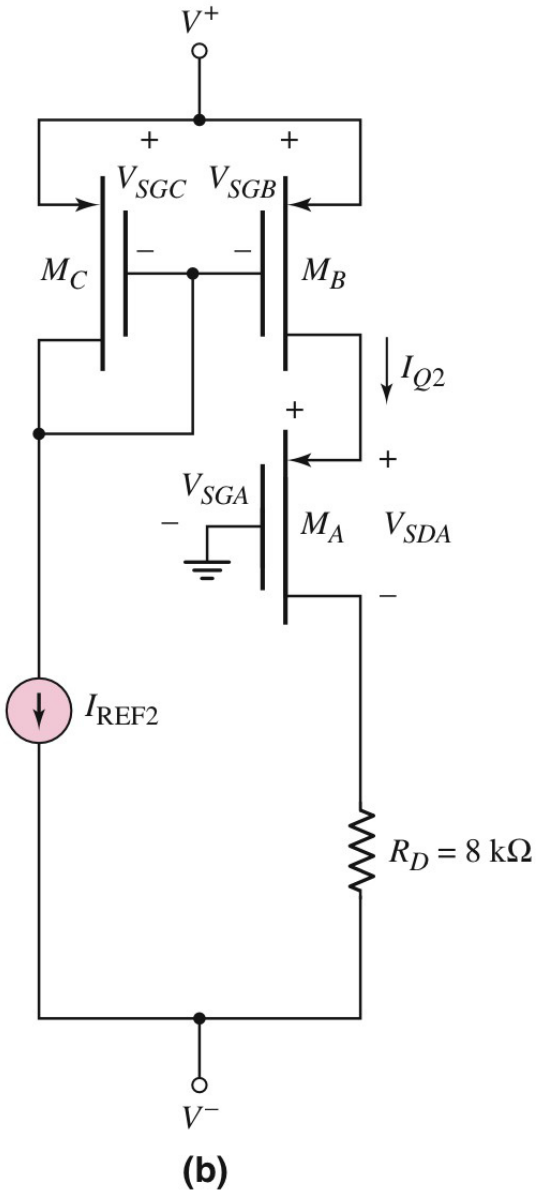
$$\Rightarrow V_{SGC} = \sqrt{\frac{250}{300}} + 0.6 = 1.513\,\text{V}$$

(3) $V_{SGB} = V_{SGC} = 1.513\,\text{V}$

(4) Assume that M_B is biased in the saturation region

$$I_B = I_{Q2} = \frac{k_n'}{2} \cdot \left(\frac{W}{L}\right)_B \left(V_{SGB} + V_{TP}\right)^2$$

$$\Rightarrow 150 = \frac{40}{2} \cdot \left(\frac{W}{L}\right)_B \left[1.513 + (-0.6)\right]^2 \Rightarrow \left(\frac{W}{L}\right)_B = 9$$



(b)

(5) Assume that M_A is biased in the saturation region

$$I_{DA} = I_{Q2} = \frac{k_n'}{2} \cdot \left(\frac{W}{L}\right)_A \left(V_{SGA} + V_{TP}\right)^2$$

$$\Rightarrow 150 = \frac{40}{2}(25)\left(V_{SGA} + (-0.6)\right)^2$$

$$\Rightarrow V_{SGA} = 1.148\,\text{V}$$

(6) $V_{SGA} = V_{SA} - V_{GA} = V_{SA} = 1.148\,\text{V}$

$$V_{SDA} = V_{SA} - I_{Q2}R_D - V^- = 1.148 - (-0.15)(8) - (-3) = 2.95\,\text{V}$$

(7) Check: $V_{SDA} = 2.95\,\text{V} > V_{SDA,\text{sat}} = V_{SGA} + V_{TP} = 1.148 + (-0.6) = 0.548\text{V}$

The transistor M_A is indeed based the saturation region

$$V_{SDB} = V_{SB} - V_{DB} = V^+ - V_S = 3 - 1.148 = 1.852\text{V}$$

$$V_{SDB} > V_{SDB,\text{sat}} = V_{SGB} + V_{TP} = 1.513 + (-0.6) = 0.913\text{V}$$

The transistor M_B is indeed based the saturation region

Constant-Current Biasing

(1) M_3 and M_4 are biased in the saturation region

(2) $K_{n3}(V_{GS3}-V_{TN3})^2 = K_{n4}(V_{GS4}-V_{TN4})^2$

(3) $V_{GS4}+V_{GS3}=-V^-$

(4) $$V_{GS3}=\frac{-V^- - V_{TN4}+V_{TN3}\sqrt{K_{n3}/K_{n4}}}{1+\sqrt{K_{n3}/K_{n4}}}$$

(5) $I_Q = K_{n2}(V_{GS3}-V_{TN2})^2$

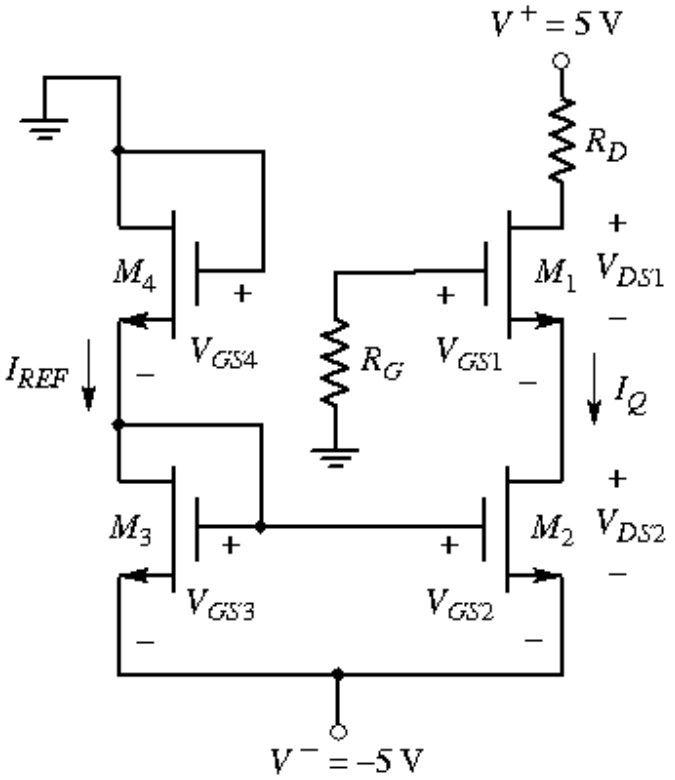


Figure 5.43 Implementation of a MOSFET constant-current source

Example 5.13 **Objective:** Determine the currents and voltages in a MOSFET constant-current source.

For the circuit shown in Figure 5.43, the transistor parameters are: $K_{n1} = 0.2\,\text{mA/V}^2$, $K_{n2} = K_{n3} = K_{n4} = 0.1\,\text{mA/V}^2$, and $V_{TN1} = V_{TN2} = V_{TN3} = V_{TN4} = 1\,\text{V}$.

Solution:

(1) $$V_{GS3} = \frac{\sqrt{\frac{0.1}{0.1}}[5-1]+1}{1+\sqrt{\frac{0.1}{0.1}}} = 2.5\,\text{V}$$

(2) $$I_Q = (0.1)\cdot(2.5-1)^2 = 0.225\,\text{mA}$$

(3) $$I_Q = K_{n1}\left(V_{GS1}-V_{TN1}\right)^2$$

$$\Rightarrow 0.225 = (0.2)\left(V_{GS1}-1\right)^2$$

$$\Rightarrow V_{GS1} = 2.06\,\text{V}$$

(4) $$V_{GS1} = V_{G1} - V_{S1} = 0 - V_{S1} = 2.06\,\text{V} \Rightarrow V_{S1} = -2.06\,\text{V}$$

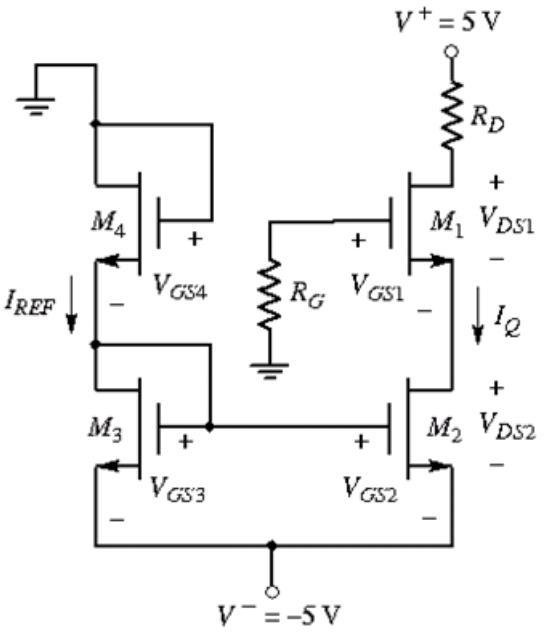
(5) $$V^- + V_{DS2} = V_{S1}$$

$$\Rightarrow V_{DS2} = V_{S1} - V^- = -2.06-(-5) = 2.94\,\text{V}$$

(6) Check: $$V_{DS2} = V_{D2} - V_{S2} = V_{S1} - V^- = -2.06-(-5) = 2.94\text{V}$$

$$V_{DS2} > V_{DS2,\text{sat}} = V_{GS2} - V_{TN2} = 2.5-1 = 1.5\text{V}$$

The transistor M_2 is indeed based the saturation region

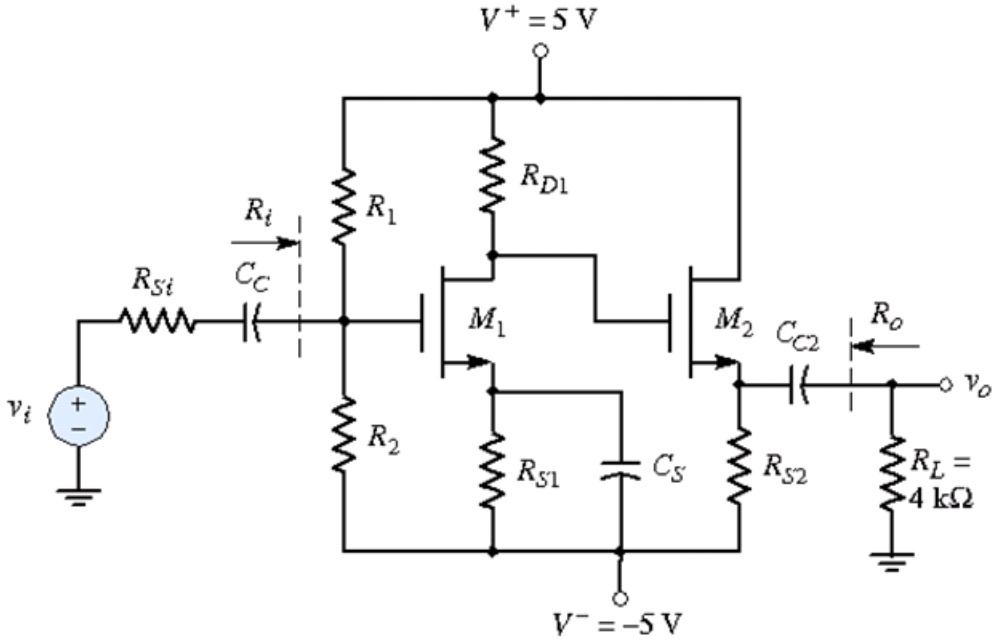


Multitransistor Circuit: Cascade Configuration

Design Example 6.14 **Objective:** Design the biasing of a multistage MOSFET circuit to meet specific requirements.

Consider the circuit shown in Figure 6.49 with transistor parameters $K_{n1} = 500\,\mu A/V^2$, $K_{n2} = 200\,\mu A/V^2$, $V_{TN1} = V_{TN2} = 1.2\,V$, and $\lambda_1 = \lambda_2 = 0$. Design the circuit such that $I_{DQ1} = 0.2\,mA$, $I_{DQ2} = 0.5\,mA$, $V_{DSQ1} = V_{DSQ2} = 6\,V$, and $R_i = 100\,k\Omega$. Let $R_{Si} = 4\,k\Omega$.

Solution:

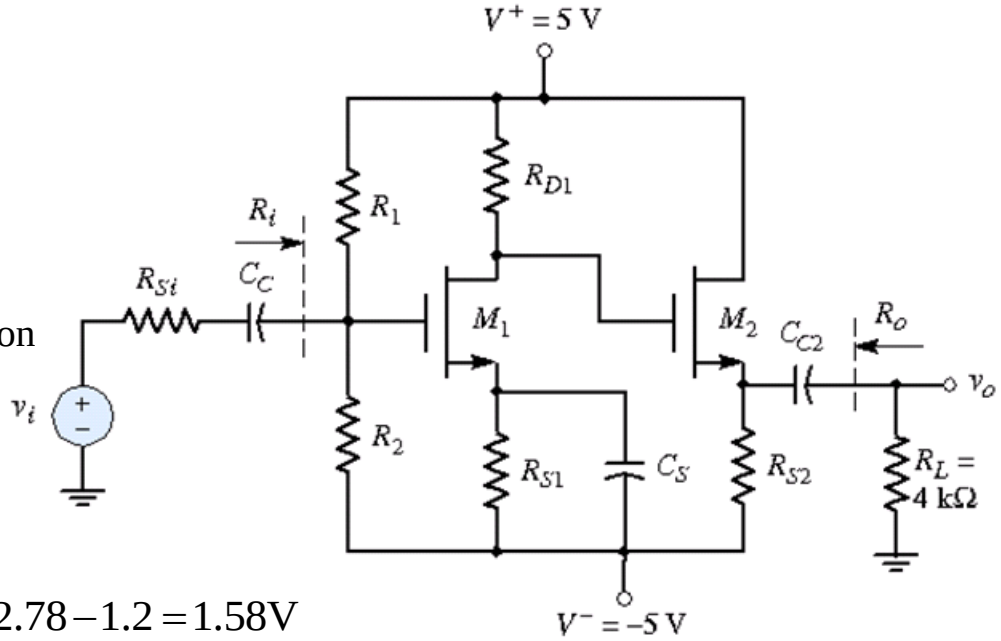


Multitransistor Circuit: Cascade Configuration

Design Example 6.14 **Objective:** Design the biasing of a multistage MOSFET circuit to meet specific requirements.

Consider the circuit shown in Figure 6.49 with transistor parameters $K_{n1} = 500\,\mu A/V^2$, $K_{n2} = 200\,\mu A/V^2$, $V_{TN1} = V_{TN2} = 1.2\,V$, and $\lambda_1 = \lambda_2 = 0$. Design the circuit such that $I_{DQ1} = 0.2\,mA$, $I_{DQ2} = 0.5\,mA$, $V_{DSQ1} = V_{DSQ2} = 6\,V$, and $R_i = 100\,k\Omega$. Let $R_{Si} = 4\,k\Omega$.

Solution:



(1) $V^- + I_{DQ2}R_{S2} + V_{DS2} = V^+$

$\Rightarrow V_{DSQ2} = V^+ - V^- - I_{DQ2}R_{S2}$

$\Rightarrow 6 = 5 - (-5) - (0.5)R_{S2} \Rightarrow R_{S2} = 8k\Omega$

(2) Assume that M_2 is biased in the saturation region

$I_{DQ2} = K_{n2}\left(V_{GS2} - V_{TN2}\right)^2$

$\Rightarrow 0.5 = 0.2\left(V_{GS2} - 1.2\right)^2$

$\Rightarrow V_{GS2} = 2.78\,V$

(3) Check: $V_{DS2} = 6V > V_{DS2,sat} = V_{GS2} - V_{TN2} = 2.78 - 1.2 = 1.58V$

The transistor M_2 is indeed based the saturation region

(4) $V^+ - V_{DS2} = V_{S2} \Rightarrow 5 - 6 = V_{S2} = -1V$

(5) $V_{GS2} = V_{G2} - V_{S2}$

$\Rightarrow 2.78 = V_{G2} - (-1)$

$\Rightarrow V_{G2} = 1.78V$

(6) $V_{G2} = V_{D1} = 1.78V$

$V^+ = V_{D1} + I_{DQ1}R_{D1}$

$\Rightarrow 5 = 1.78 + (0.2)R_{D1}$

$\Rightarrow R_{D1} = 16.1k\Omega$

(7) $V_{DSQ1} = V_{D1} - V_{S1}$

$\Rightarrow V_{S1} = V_{D1} - V_{DSQ1} = 1.78 - 6 = -4.22\,V$

(8) $V_{S1} = V^- + I_{D1}R_{S1}$

$\Rightarrow -4.22 = -5 + (0.2)R_{S1} \Rightarrow R_{S1} = 3.9\text{k}\Omega$

(9) Assume that M_1 is biased in the saturation region

$$I_{DQ1} = K_{n1}\left(V_{GS1} - V_{TN1}\right)^2$$

$$\Rightarrow 0.2 = 0.50\left(V_{GS1} - 1.2\right)^2$$

$$\Rightarrow V_{GS1} = 1.83\,\text{V}$$

(10) $$\frac{R_2}{R_1 + R_2} = \frac{1}{R_1}\cdot\left(\frac{R_1R_2}{R_1 + R_2}\right) = \frac{1}{R_1}\cdot R_i$$

$$V_{GS1} = \left(\frac{R_2}{R_1 + R_2}\right)(10) - I_{DQ1}R_{S1}$$

$$\frac{R_2}{R_1 + R_2} = \frac{1}{R_1}\cdot\left(\frac{R_1R_2}{R_1 + R_2}\right) = \frac{1}{R_1}\cdot R_i$$

$$\Rightarrow 1.83 = \frac{1}{R_1}(100)(10) - (0.2)(3.9)$$

$$\Rightarrow R_1 = 383\text{k}\Omega$$

$$\Rightarrow R_2 = 135\text{k}\Omega$$