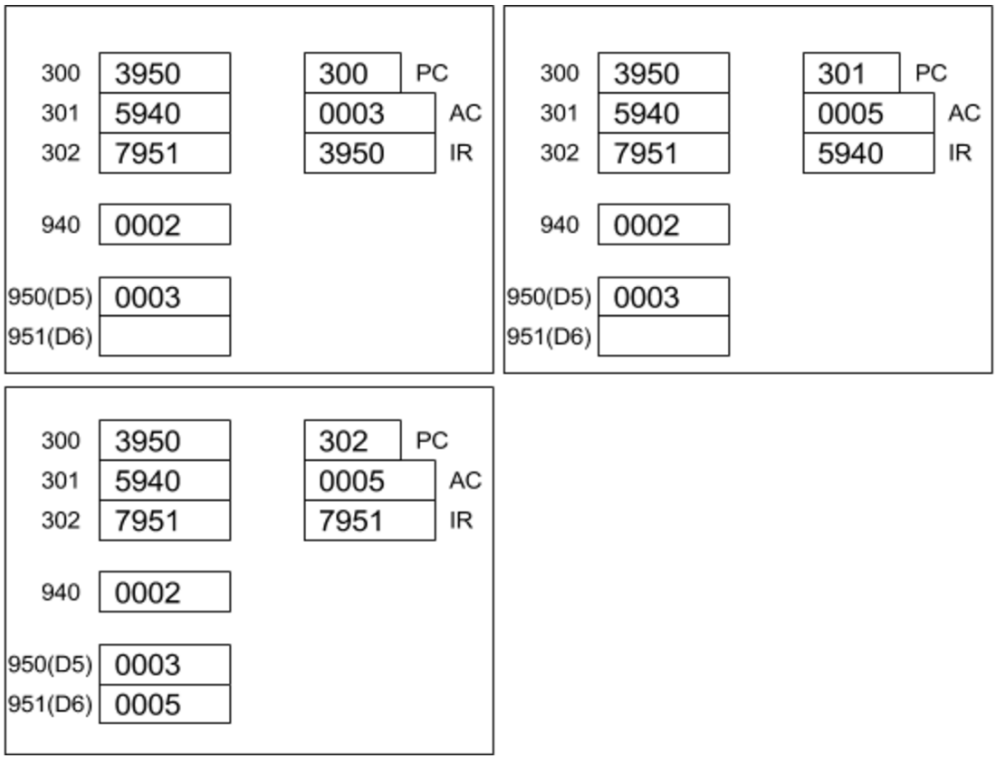
Computer Architecture Homework 3
Chao Chen

1. 1) Disable interrupts: Interrupts are processed sequentially. Other interrupts are in pending state until processor finishes the first interrupt procedure.
   2) Define priorities: Low priority interrupt can be interrupted by higher priority interrupts, and the processor will save the context for later to restore the previous interrupts procedure after finish the higher priority interrupts.

2. Memory connection: Receive address, data and control signals, and output the data to memory.
   IO connection: Receive address, data and control signals, and output control signals, interrupts and data.
   CPU connection: Receive instructions and data, and output data and control signals.

3. QPI Layers:
   Physical Layer: Comprised of physical media and the logic that transmit and receive the physical layer units.
   Link Layer: Operate on the level of FLITs, and perform flow control and CRC check on data transmitting.
   Routing Layer: Perform routing analysis to determine the outbound QPI and possible paths that a packet can follow.
   Protocol Layer: Sends and receives packets, and maintain cache coherency. tran

4.



5. a). Addressable memory space: 2^24 = 16777216 bytes;
   b). 1). For transmitting the 24-bits address, it takes 1 cycles; For 24-bits operand, it takes 2 cycles.
   2). For transmitting the 24-bits address and operand, it takes 2 cycles for both of them; (cycle means bus cycle)

   c). The PC needs to be 24-bits, the IR needs to be 32-bits.

6. speed32= 0.2 + 0.4 + 0.4 = 1, speed16 = 0.2 x 2 + 0.4 + 0.4 = 1.2
   improvement = (1.2 - 1) / 1.2 = 0.17