Influence of the Cache Coherence Protocol on the Miss Rate

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Outline

- Introduction
- Dragon Protocol
- SMP & Parallel Benchmarks
- Experiment
- Analysis
- Conclusion

Introduction

- Research Targets
  - SMP Cache System
  - Cache Coherence Protocols:
    - MSI, MESI and Dragon
  - Write-Invalidate and Write-Update
- Tools
  - SMPCache
  - Parallel Computing Bechmarks:
    - FFT / Simple / Speech / Weather

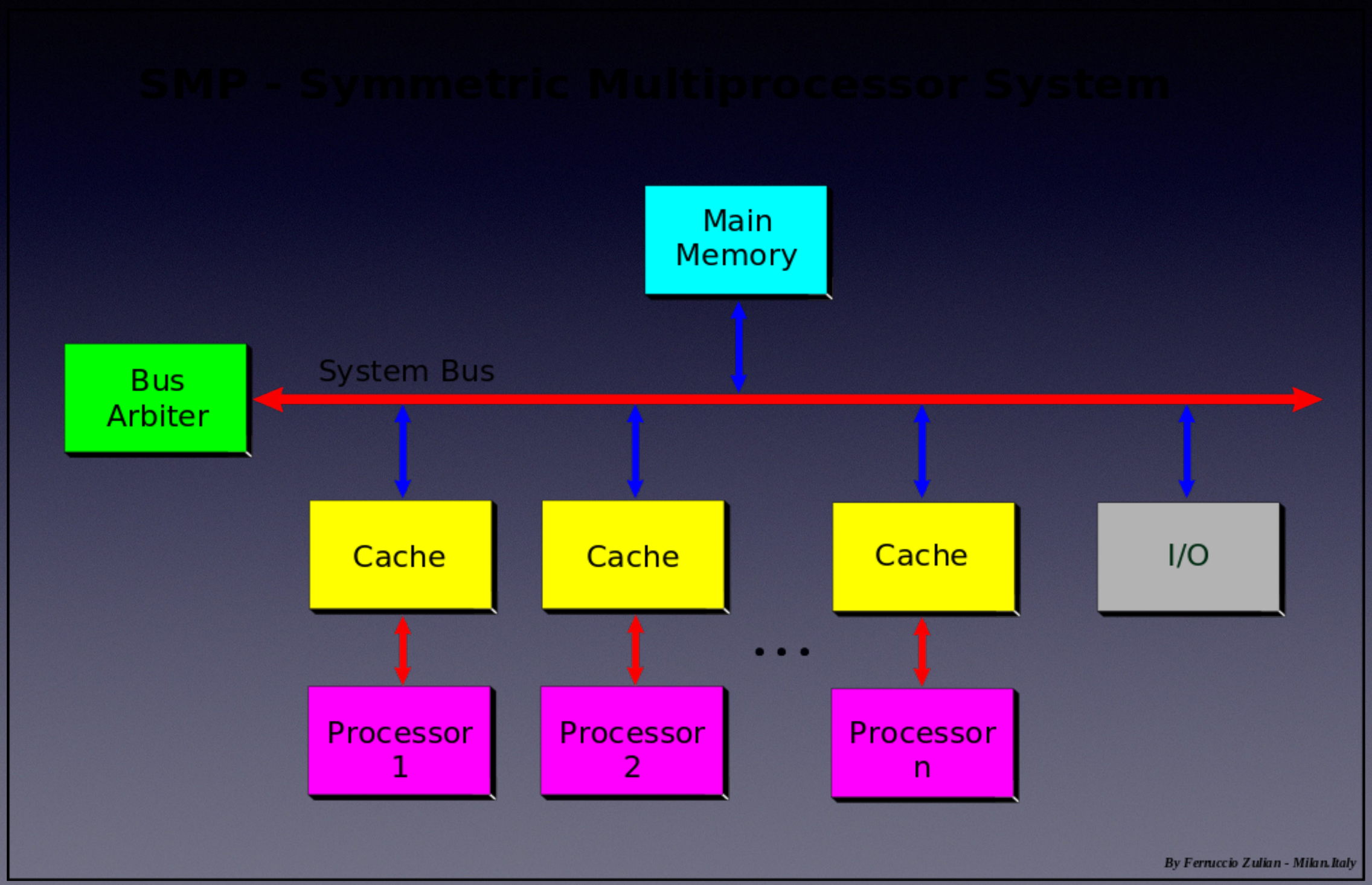
Dragon Protocol

- Developed by Xerox PARC
- Used in Xerox Dragon multiprocessor workstation
  - XDBusses 55 MHz
  - PCI 33 MHz

Dragon Protocol

- Write-Update Policy
- Whenever a write hit happens on shared line, it updates other caches immediately

SMP


SMP - Symmetric Multiprocessor System
Main Memory
Bus Arbiter
System Bus
Cache
Cache
Cache
I/O
Processor 1
Processor 2
Processor n
By Fernuccio Zulian - Milan.Italy

Parallel Benchmarks

- Task is distributed by multi-threading
- Shared Memory / Symmetric Cache Sets
- Bottleneck on Bus Traffic / IO Accessing

Experiment

SMP Configuration:

- Processors in SMP = 8.
- Scheme for bus arbitration = LRU.
- Word wide (bits) = 16.
- Words by block = 32 (block size = 64 bytes).
- Blocks in main memory = 524288 (main memory size = 32 MB).
- Blocks in cache = 256 (cache size = 16 KB).
- Mapping = Set-Associative.
- Cache sets = 64 (four-way set associative caches).
- Replacement policy = LRU.

Experiment

Benchmark	Accesses	Read	Write	Instructions
FFT8	931368	367272	173584	395012
Simple8	3378834	482804	1444689	1451341
Speech8	1473563	1151333	322230	1
Weather8	3970483	1944234	325458	1700791

Experiment

- Hits & Misses

	MSI	MESI	Dragon
FFT	627,839 / 303,529	620,892 / 303,529	869,364 / 62,004
Simple	2,183,451 / 1,195,383	2,182,353 / 1,196,481	2,462,066 / 916,768
Speech	424,905 / 1,048,658	470,959 / 1,002,604	678,755 / 794,808
Weather	2,877,482 / 1,092,991	2,876,625 / 1,093,849	3,104,633 / 865,840

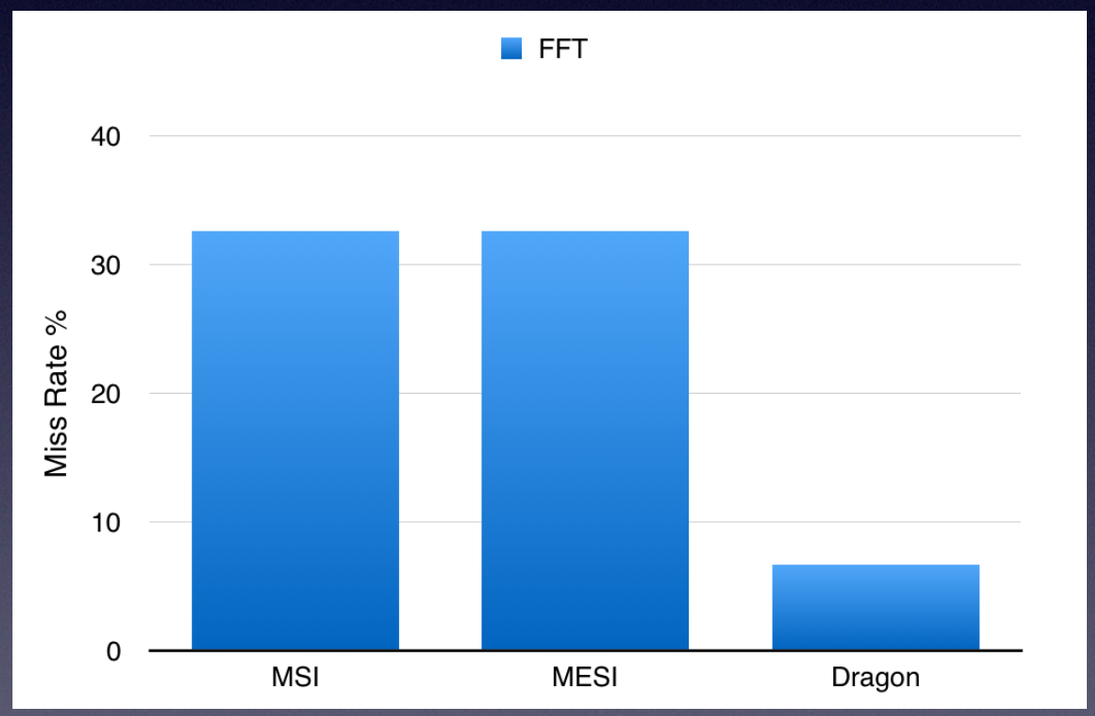
Experiment

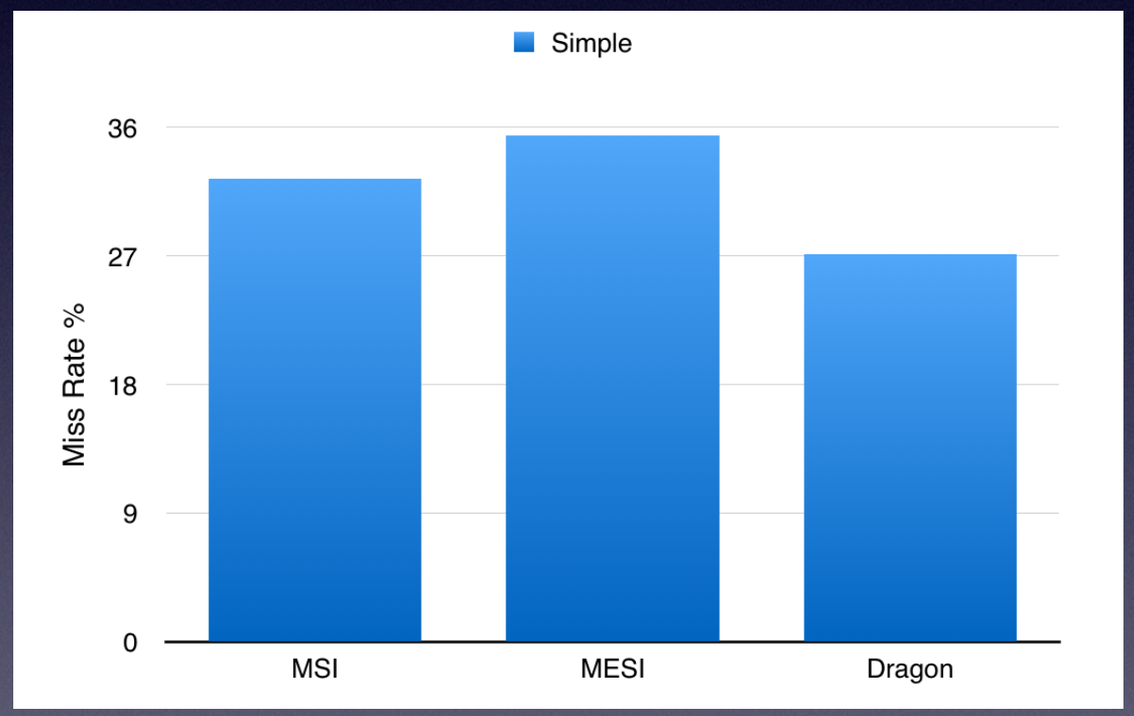
- Miss Rate

	MSI	MESI	Dragon
FFT	32.590%	32.590%	6.657%
Simple	35.379%	35.411%	27.133%
Speech	71.165%	68.039%	53.938%
Weather	27.528%	27.550%	21.807%

Experiment

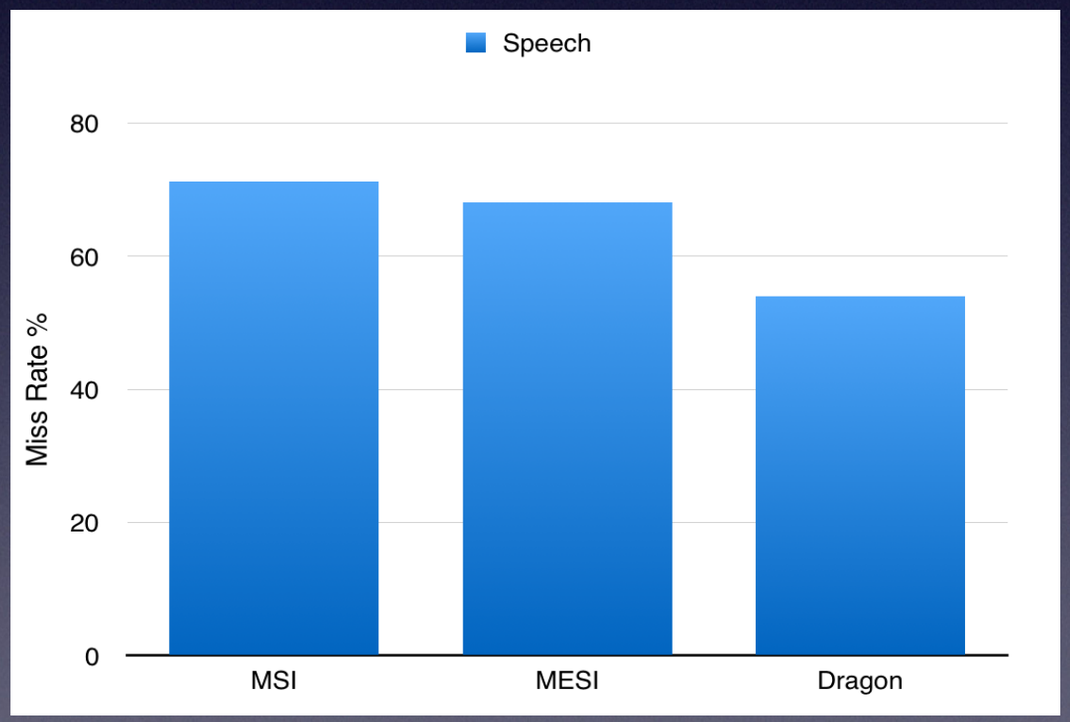
- Cache Coherence Performance

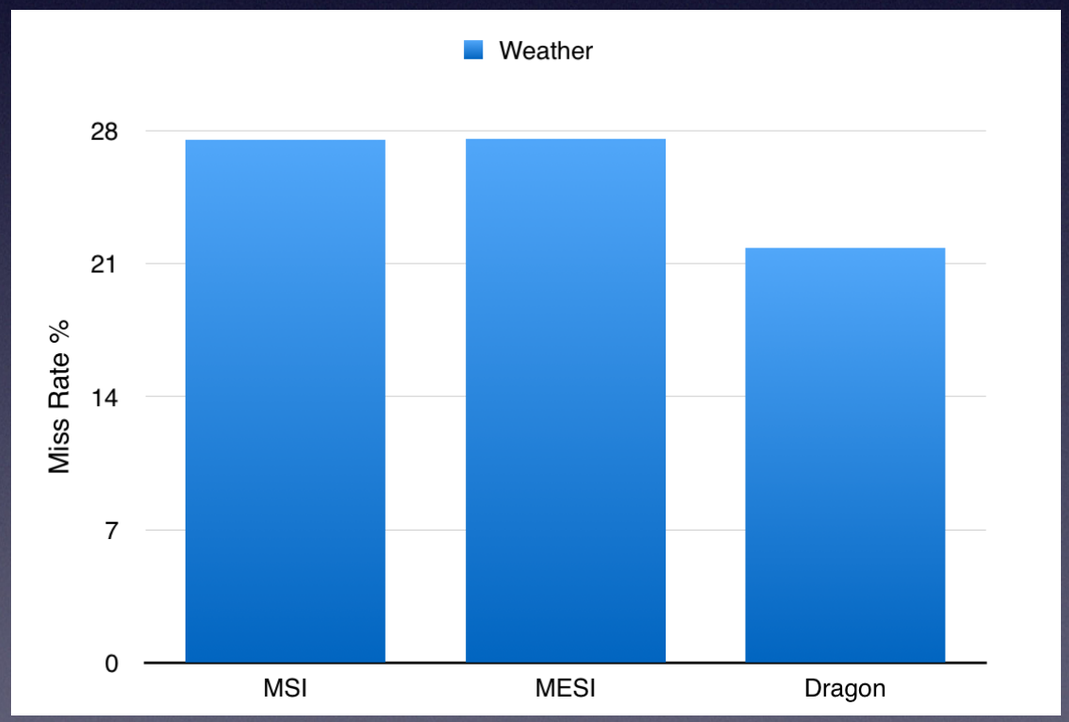




Experiment

- Cache Coherence Performance





Analysis

- Write-Update and Write-Invalidate
    - Write-Update is more aggressive in updating other shared caches
    - Other shared lines always keep up-to-date
    - More overhead over Bus traffic

Analysis

- MSI and MESI
    - Exclusive state is for reducing bus traffic when only one copy of target memory exists.
    - E state affects runtime memory distribution & accessing timing.
    - E state distribution varies with different programs.

Conclusion

- Write-Update based protocols have lower miss rate in most cases
- The miss rate of MSI & MESI may varies with different benchmarks
- Using of concrete protocols does not always improve the cache coherence performance

Thanks