Influence of the Cache Coherence Protocol on the Miss Rate

Instructor

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Reported by

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1. Introduction

This report introduces three different cache coherence protocols, the influence of these protocols on the cache data locality of the symmetric multiprocessor system, as well as the related experiment and analysis.

To better practice and verify the cache coherence knowledge we learned from Computer Architecture class, we conducted the experiment on top of a cache system simulation software SMPCache.

2. Background

2.1 SMPCache

SMPCache is a trace-driven simulator that provides a virtual environment for the cache memory system on symmetric multiprocessors machine [1].

The architecture of the virtual machine is configurable to users. Users can setup a single core or symmetric multi-core virtual machine with different cache/memory structures and hierarchies to study or verify how the cache system works practically.

Trace-driven means the simulation experiments can be conducted through executing the trace files on the configured virtual machine on SMPCache. A trace file is an ASCII data file for a Benchmark programs, which can be obtained from SMPCache website or generated by users' programs.

2.2 MSI, MESI and Dragon

SMPCache supports three types of cache coherence protocols: MSI, MESI and Dragon.

MSI is a basic cache-coherence protocol that operates in multiprocessor systems. The letters M-S-I in the protocol name identify the possible states in which a cache line can be [2].

The MESI protocol is a variant of the MSI protocol. MESI was designed to reduce the amount of traffic in the coherency interconnections(Bus). This is achieved by adding an "Exclusive" state to reduce the bus traffic caused by writing the blocks that only exist in one single cache [3].

Both MSI and MESI protocols are invalidate-based protocol, by which the cache controller invalidate its own copy of the updated memory block when a write operation to the same block is observed through the bus.

The Dragon cache coherence protocol is the schema used in the Xerox Dragon multiprocessor workstation, developed by Xerox PARC. This protocol uses a write-back policy [4]. The Dragon protocol includes five states of cache lines: Invalid, Clean, Shared-Clean, Dirty and Shared-Dirty.

Dragon uses write-update as the cache coherence policy when the updating happens on the shared cache line, which will update the latest copy of the memory block to other cache lines which share copies of the same memory location.

2.3 SMP & Parallel Program

To simulate all the features of symmetric multiprocessor machine, we use some parallel programs for the experiment.

SMP is the abbreviation for symmetric multiprocessor, which involves a symmetric hardware and software architecture where two or more identical processors connect to a single, shared main memory, have full access to all I/O devices, and are controlled by a single operating system instance that treats all processors equally. Most multiprocessor systems today use an SMP architecture [5].

Uniprocessor and SMP systems require different programming methods to achieve maximum performance. Programs running on SMP systems may experience an increase in performance even when they have been written for uniprocessor systems. This is because hardware interrupts usually suspends program execution while the kernel that handles them can execute on an idle processor instead. The effect in most applications is not so much a performance increase as the appearance that the program is running much more smoothly. Some applications, particularly compilers and some distributed computing projects, run faster by a factor of the number of additional processors.

Systems programmers must build support for SMP into the operating system, otherwise, the additional processors remain idle and the system functions as a uniprocessor system. To solve different problems and tasks, SMP applies multiple processors to that one problem, known as parallel programming.

Traditionally, computer software has been written for serial computation. To solve a problem, an algorithm is constructed and implemented as a serial stream of instructions. These instructions are executed on a central processing unit on one computer. Only one instruction may execute at a time after that instruction is finished, the next one is executed [6].
Parallel computing, on the other hand, uses multiple processing elements simultaneously to solve a problem. This is accomplished by breaking the problem into independent parts so that each processing element can execute its part of the algorithm simultaneously with the others. The

processing elements can be diverse and include resources such as a single computer with multiple processors, several networked computers, specialized hardware, or any combination of the above [7].

3. Experiment & Result

The experiment presented in this section is focus on the influence of different cache coherence protocols on the cache accessing miss rate of the parallel benchmark programs when it is running on a symmetric multiprocessor machine.

3.1 Architecture Configuration

We built up a symmetric multiprocessor virtual machine to enable all the parallel computing patterns in the test programs. On top of that, the tests of MSI, MESI and Dragon protocols are conducted to simulate the performance of the cache system.

Below list shows the configuration details of the symmetric multiprocessor virtual machine

- Processors in SMP = 8.
- Scheme for bus arbitration = LRU.
- Word wide (bits) = 16.
- Words by block = 32 (block size = 64 bytes).
- Blocks in main memory = 524288 (main memory size = 32 MB).
- Blocks in cache = 256 (cache size = 16 KB).
- Mapping = Set-Associative.
- Cache sets = 64 (four-way set associative caches).
- Replacement policy = LRU.

3.2 Parallel Bechmark Programs

The experiment uses four different parallel benchmark programs: FFT, Simple, Speech and Weather. As mentioned in Background section, these programs have already been optimized with parallel programming model to fully utilizing the SMP resources.

The FFT program is an application that simulates the fluid dynamics with FFT with parallel programming. The Weather program is the parallel version of the WEATHER application, which is used for weather forecasting. The serial version is from NASA Space Flight Center, Greenbelt, Md [1]. The Simple and Speech benchmark programs are also the parallelized version of some classic benchmark sequential programs.

Since the architecture configuration is 8 processors in SMP, we have to download the specific 8-processors version of the benchmark programs which can be found in SMPCache website.

3.3 Results

Below table shows the **hits/misses** statistics of different cache coherence protocols for different Benchmarks:

	MSI	MESI	Dragon
FFT	627,839 / 303,529	620,892 / 303,529	869,364 / 62,004
Simple	2,183,451 / 1,195,383	2,182,353 / 1,196,481	2,462,066 / 916,768
Speech	424,905 / 1,048,658	470,959 / 1,002,604	678,755 / 794,808
Weather	2,877,482 / 1,092,991	2,876,625 / 1,093,849	3,104,633 / 865,840

Below table shows the **miss rate** of different cache coherence protocols for different Benchmarks:

	MSI	MESI	Dragon
FFT	32.590%	32.590%	6.657%
Simple	35.379%	35.411%	27.133%
Speech	71.165%	68.039%	53.938%
Weather	27.528%	27.550%	21.807%

4. Analysis

From the experiment statistics mentioned in previous section, we generated the bar chart of the miss rate on different cache coherence protocols (See the charts at the end of this section).

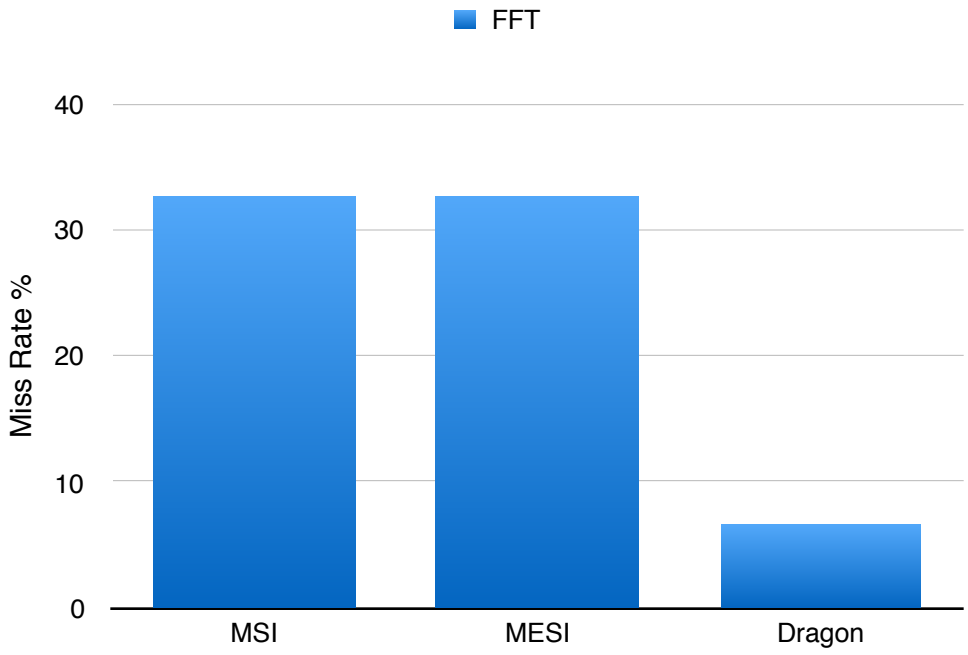
As shown in the figures, the Dragon protocol always has the best performance (lowest miss rate) on cache coherence. This result matches the expectation for the three protocols, which determined by their writing policy.

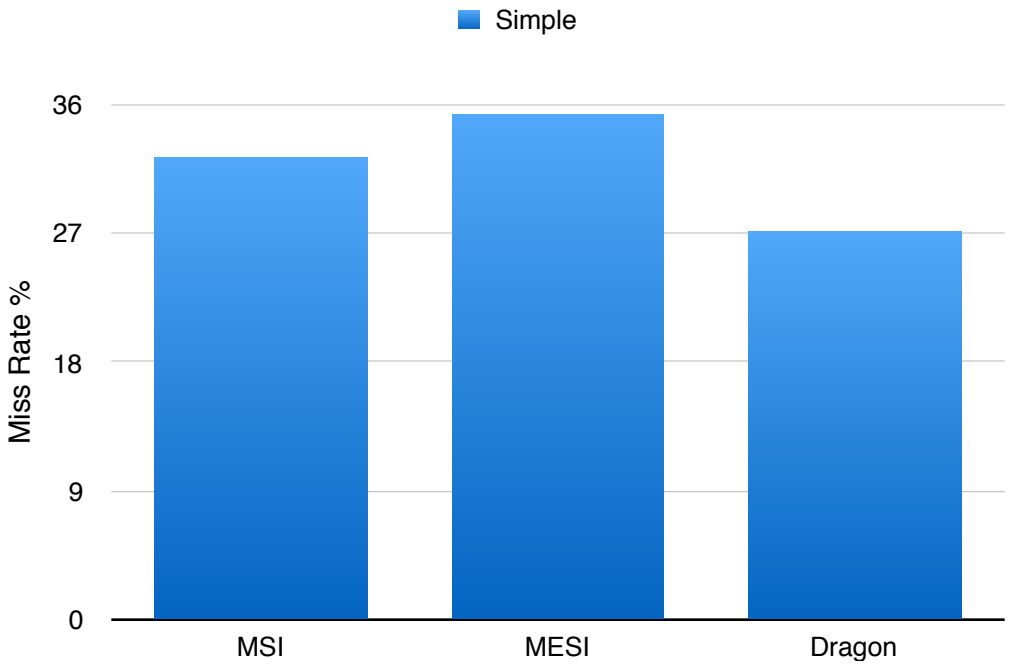
The reason is, as mentioned in Background section, both MSI and MESI are using write-invalidate policy to manage the cache consistence. As a write operation of the shared cache line is observed, invalidate-based protocols only changes the state of the cache lines which share the copy of same memory location to invalid state, and the cache miss happens when other processor access those invalid cache lines. Finally, the missed accessing will force the invalid cache line to update the content from other up-to-date cache line or the main memory and change the state back to shared again.

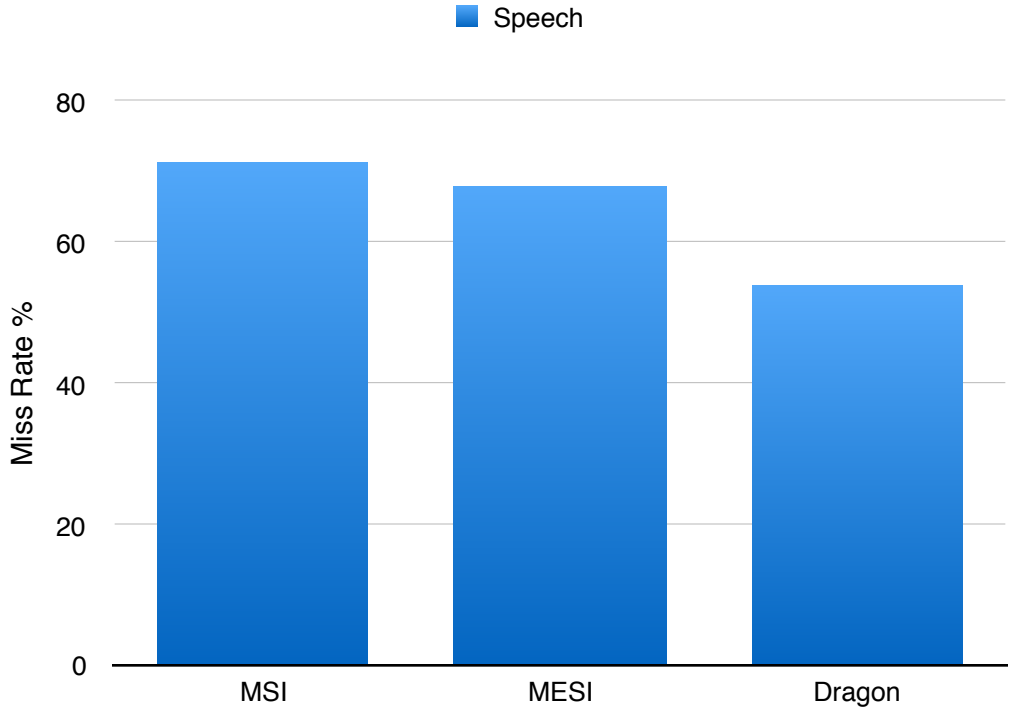
Meanwhile, the Dragon protocol adopts write-update policy. In this updated based policy, it immediately updates other shared cache lines if the updated cache line is in Shared-Clean or Shared-Dirty state. Obviously, comparing with write-invalidate, write-update policy will reduce the miss rate since the cache lines in Shared- states are always up-to-date. However, it may causes some overhead on the bus for the aggressive updating policy.

By comparing MSI and MESI, we can see the performance of these two write-invalidate protocols variant with different benchmark programs. More specifically, MSI and MESI got the same miss rate for the FFT benchmark case, MSI has lower miss rate than MESI in the Simple benchmark, MESI has lower miss rate than MSI in the Speech benchmark, and MSI took the lower miss rate in the Weather benchmark test.

The reason for this variant miss rate of MSI and MESI is that both of are using the same write-invalidate policy. It determines that these two protocols do not take advantages of each other in the cache hits/misses rate. However, comparing with MSI, the MESI protocol has an extra “Exclusive” state which is designed for reducing the bus overhead caused by writing the blocks that only exist in one single cache. This difference makes the behavior pattern of MESI is more complicated than MSI. Since the programming models and algorithms are distinguished among these four different benchmark programs, the number of Exclusive state cache line (the memory block accessed by on one processor at the same time) are also variant. Therefore, the similar but variant performance of the cache miss rate for MSI and MESI protocols make sense.


FFT
40
30
20
10
0
Miss Rate %
MSI
MESI
Dragon


Simple
36
27
18
9
0
Miss Rate %
MSI
MESI
Dragon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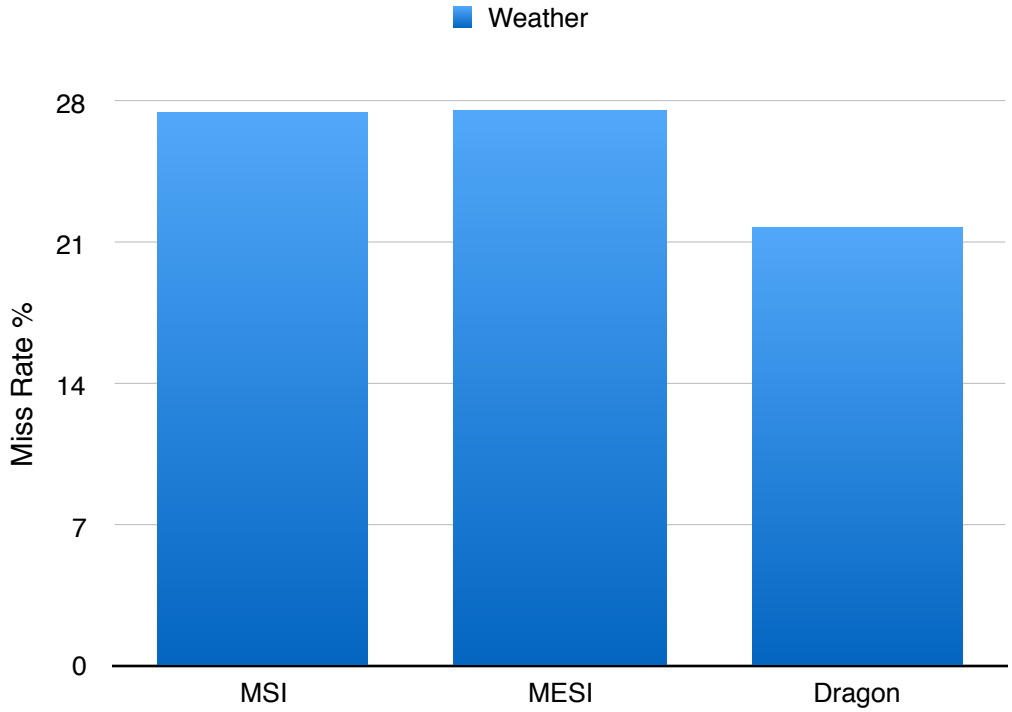
40
20
0
Miss Rate %
MSI
MESI
Dragon


Weather
28
21
14
7
0
Miss Rate %
MSI
MESI
Dragon

5. Conclusion

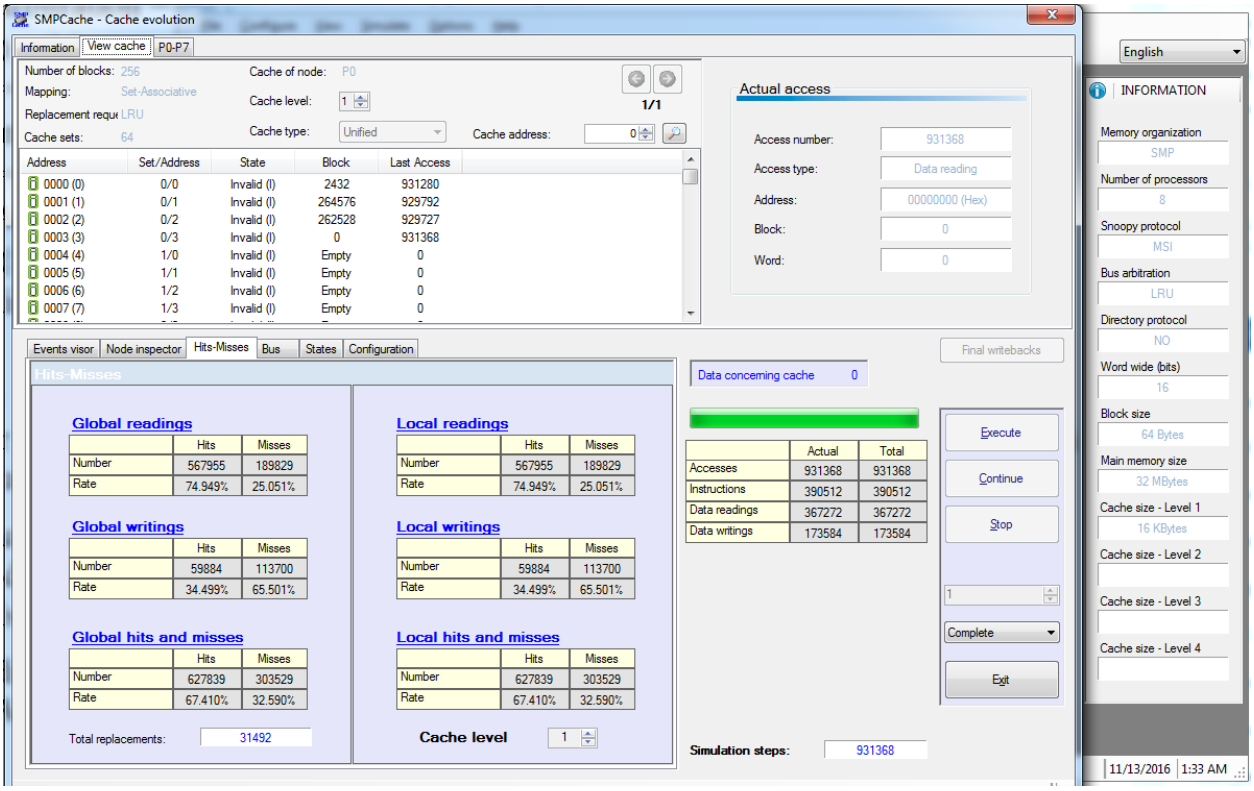
From the experiment and the analysis of the result, we can draw the conclusion.

The update-based protocol always has lower cache miss rate than the invalidation-based protocol. This situation are applicable to general applications. Meanwhile, the miss rate of MSI and MESI are variant with different benchmark programs. The use of concrete cache coherence protocol does not always improve the performance of multiprocessor system. Write-update protocol may reduces the cache miss rate but introduces extra overhead for aggressive and intensive updating policy, while the cache coherence performance of MSI and MESI are variant with different benchmark programs.

6. Reference

[1]. SMPCache http://arco.unex.es/smpcache/
[2]. MSI Protocol https://en.wikipedia.org/wiki/MSI_protocol
[3]. MESI Protocol https://en.wikipedia.org/wiki/MESI_protocol
[4]. Dragon Protocol https://en.wikipedia.org/wiki/Dragon_protocol
[5]. Symmetric multiprocessing https://en.wikipedia.org/wiki/Symmetric_multiprocessing
[6]. Introduction to Parallel Computing Barney Blaise - Lawrence Livermore National Laboratory
[7]. Parallel Computing https://en.wikipedia.org/wiki/Parallel_computing

7. Appendix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Information
View cache
P0-P7
Number of blocks: 256
Mapping: Set-Associative
Replacement requ LRU
Cache sets: 64
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Actual access
Access number: 931368
Access type: Data reading
Address: 00000000 (Hex)
Block: 0
Word: 0
Address | Set/Address | State | Block | Last Access
0000 (0) 0/0 Invalid (I) 2432 931280
0001 (1) 0/1 Invalid (I) 264576 929792
0002 (2) 0/2 Invalid (I) 262528 929727
0003 (3) 0/3 Invalid (I) 0 931368
0004 (4) 1/0 Invalid (I) Empty 0
0005 (5) 1/1 Invalid (I) Empty 0
0006 (6) 1/2 Invalid (I) Empty 0
0007 (7) 1/3 Invalid (I) Empty 0
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Hits-Misses
Data concerning cache 0
Global readings
Hits Misses
Number 567955 189829
Rate 74.949% 25.051%
Local readings
Hits Misses
Number 567955 189829
Rate 74.949% 25.051%
Global writings
Hits Misses
Number 59884 113700
Rate 34.499% 65.501%
Local writings
Hits Misses
Number 59884 113700
Rate 34.499% 65.501%
Global hits and misses
Hits Misses
Number 627839 303529
Rate 67.410% 32.590%
Local hits and misses
Hits Misses
Number 627839 303529
Rate 67.410% 32.590%
Actual Total
Accesses 931368 931368
Instructions 390512 390512
Data readings 367272 367272
Data writings 173584 173584
Execute
Continue
Stop
Complete
Exit
Total replacements: 31492
Cache level 1
Simulation steps: 931368
English
INFORMATION
Memory organization
SMP
Number of processors
8
Snoopy protocol
MSI
Bus arbitration
LRU
Directory protocol
NO
Word wide (bits)
16
Block size
64 Bytes
Main memory size
32 MBytes
Cache size - Level 1
16 KBytes
Cache size - Level 2
Cache size - Level 3
Cache size - Level 4
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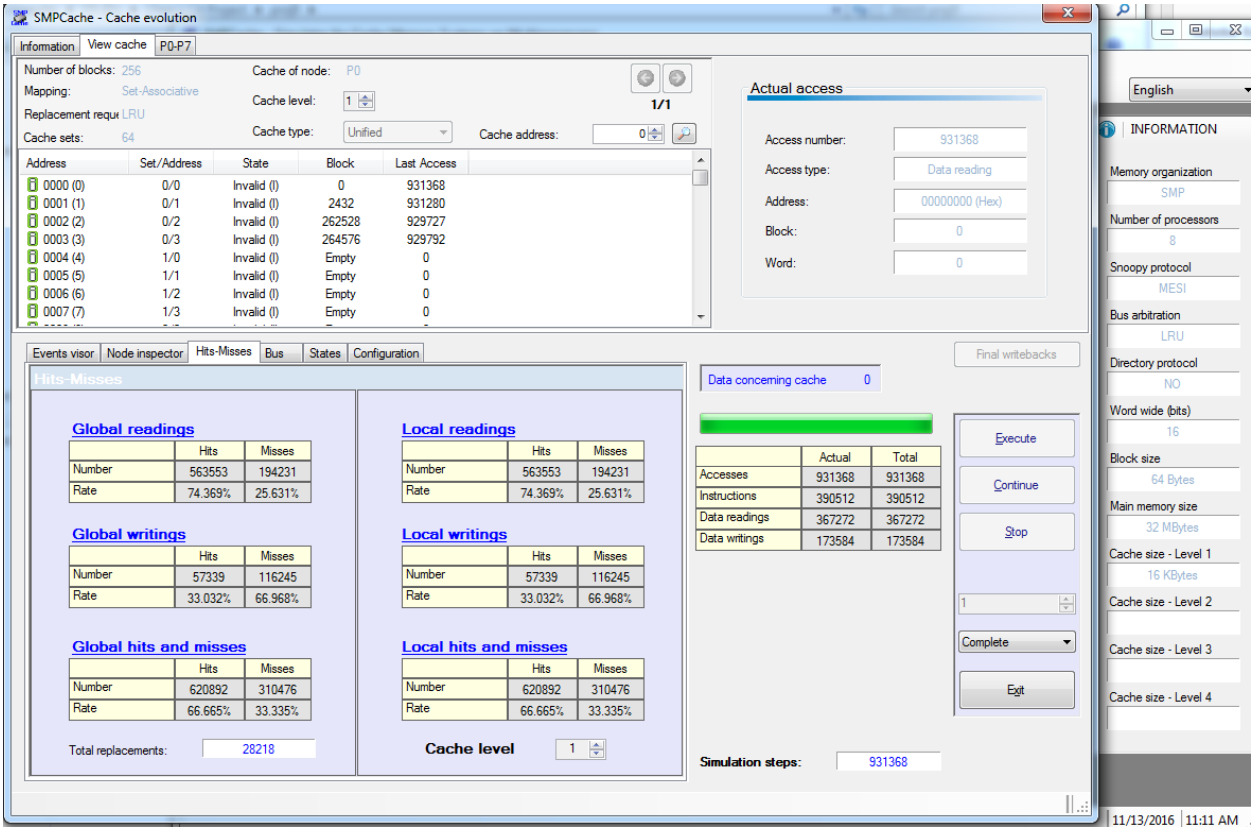
SMPCache - Cache evolution
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View cache
P0-P7
Number of blocks: 256
Mapping: Set-Associative
Replacement requ LRU
Cache sets: 64
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Actual access
Access number: 931368
Access type: Data reading
Address: 00000000 (Hex)
Block: 0
Word: 0
Address | Set/Address | State | Block | Last Access
0000 (0) 0/0 Invalid (I) 0 931368
0001 (1) 0/1 Invalid (I) 2432 931280
0002 (2) 0/2 Invalid (I) 262528 929727
0003 (3) 0/3 Invalid (I) 264576 929792
0004 (4) 1/0 Invalid (I) Empty 0
0005 (5) 1/1 Invalid (I) Empty 0
0006 (6) 1/2 Invalid (I) Empty 0
0007 (7) 1/3 Invalid (I) Empty 0
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Hits-Misses
Data concerning cache 0
Global readings
Hits Misses
Number 563553 194231
Rate 74.369% 25.631%
Local readings
Hits Misses
Number 563553 194231
Rate 74.369% 25.631%
Global writings
Hits Misses
Number 57339 116245
Rate 33.032% 66.968%
Local writings
Hits Misses
Number 57339 116245
Rate 33.032% 66.968%
Global hits and misses
Hits Misses
Number 620892 310476
Rate 66.665% 33.335%
Local hits and misses
Hits Misses
Number 620892 310476
Rate 66.665% 33.335%
Actual Total
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Instructions 390512 390512
Data readings 367272 367272
Data writings 173584 173584
Execute
Continue
Stop
Complete
Exit
Total replacements: 28218
Cache level 1
Simulation steps: 931368
English
INFORMATION
Memory organization
SMP
Number of processors
8
Snoopy protocol
MESI
Bus arbitration
LRU
Directory protocol
NO
Word wide (bits)
16
Block size
64 Bytes
Main memory size
32 MBytes
Cache size - Level 1
16 KBytes
Cache size - Level 2
Cache size - Level 3
Cache size - Level 4
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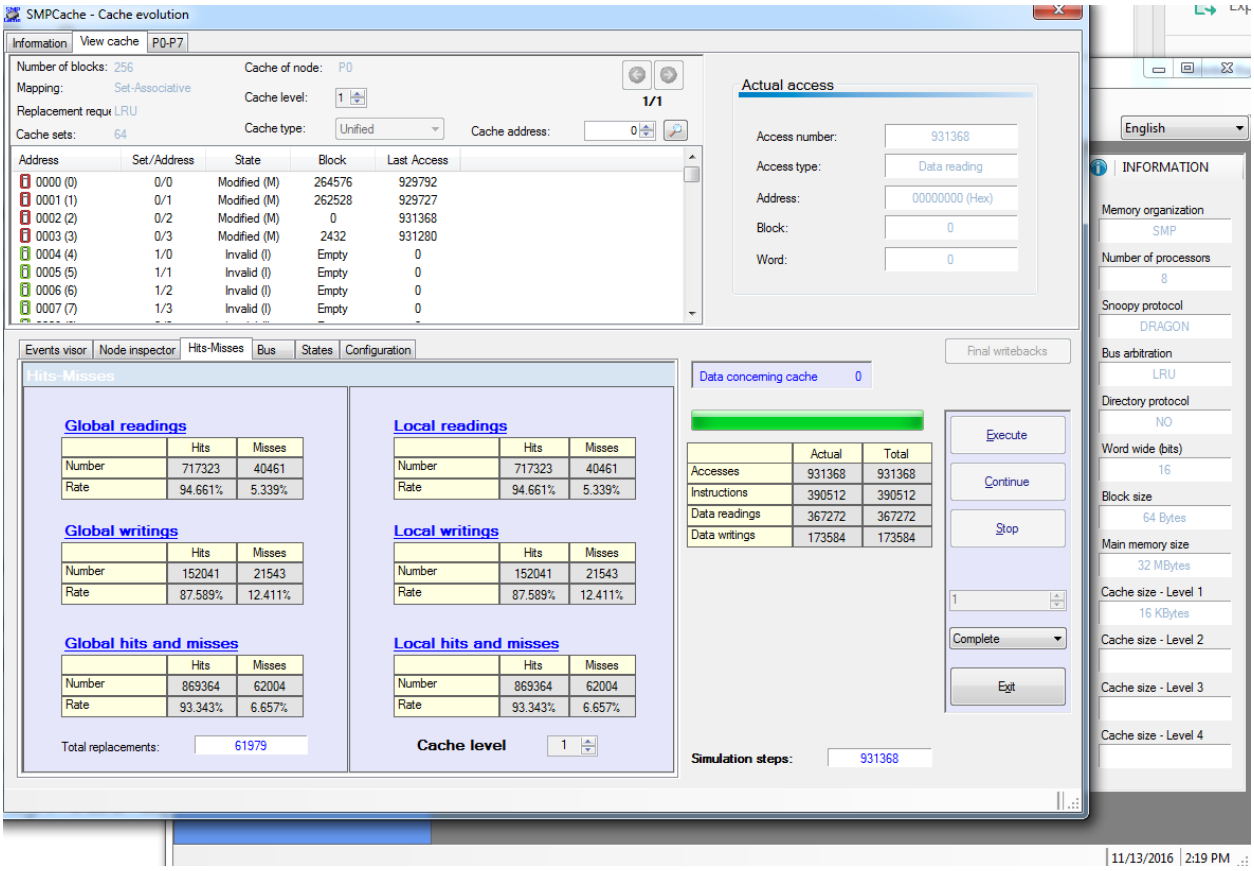
SMPCache - Cache evolution
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View cache
P0-P7
Number of blocks: 256
Mapping: Set-Associative
Replacement requ LRU
Cache sets: 64
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Actual access
Access number: 931368
Access type: Data reading
Address: 00000000 (Hex)
Block: 0
Word: 0
Address | Set/Address | State | Block | Last Access
0000 (0) | 0/0 | Modified (M) | 264576 | 929792
0001 (1) | 0/1 | Modified (M) | 262528 | 929727
0002 (2) | 0/2 | Modified (M) | 0 | 931368
0003 (3) | 0/3 | Modified (M) | 2432 | 931280
0004 (4) | 1/0 | Invalid (I) | Empty | 0
0005 (5) | 1/1 | Invalid (I) | Empty | 0
0006 (6) | 1/2 | Invalid (I) | Empty | 0
0007 (7) | 1/3 | Invalid (I) | Empty | 0
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Hits-Misses
Data concerning cache 0
Global readings
Hits | Misses
Number | 717323 | 40461
Rate | 94.661% | 5.339%
Local readings
Hits | Misses
Number | 717323 | 40461
Rate | 94.661% | 5.339%
Global writings
Hits | Misses
Number | 152041 | 21543
Rate | 87.589% | 12.411%
Local writings
Hits | Misses
Number | 152041 | 21543
Rate | 87.589% | 12.411%
Global hits and misses
Hits | Misses
Number | 869364 | 62004
Rate | 93.343% | 6.657%
Local hits and misses
Hits | Misses
Number | 869364 | 62004
Rate | 93.343% | 6.657%
Total replacements: 61979
Cache level 1
Actual | Total
Accesses | 931368 | 931368
Instructions | 390512 | 390512
Data readings | 367272 | 367272
Data writings | 173584 | 173584
Simulation steps: 931368
Execute
Continue
Stop
1
Complete
Exit
English
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Memory organization
SMP
Number of processors
8
Snoopy protocol
DRAGON
Bus arbitration
LRU
Directory protocol
NO
Word wide (bits)
16
Block size
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Main memory size
32 MBytes
Cache size - Level 1
16 KBytes
Cache size - Level 2
Cache size - Level 3
Cache size - Level 4
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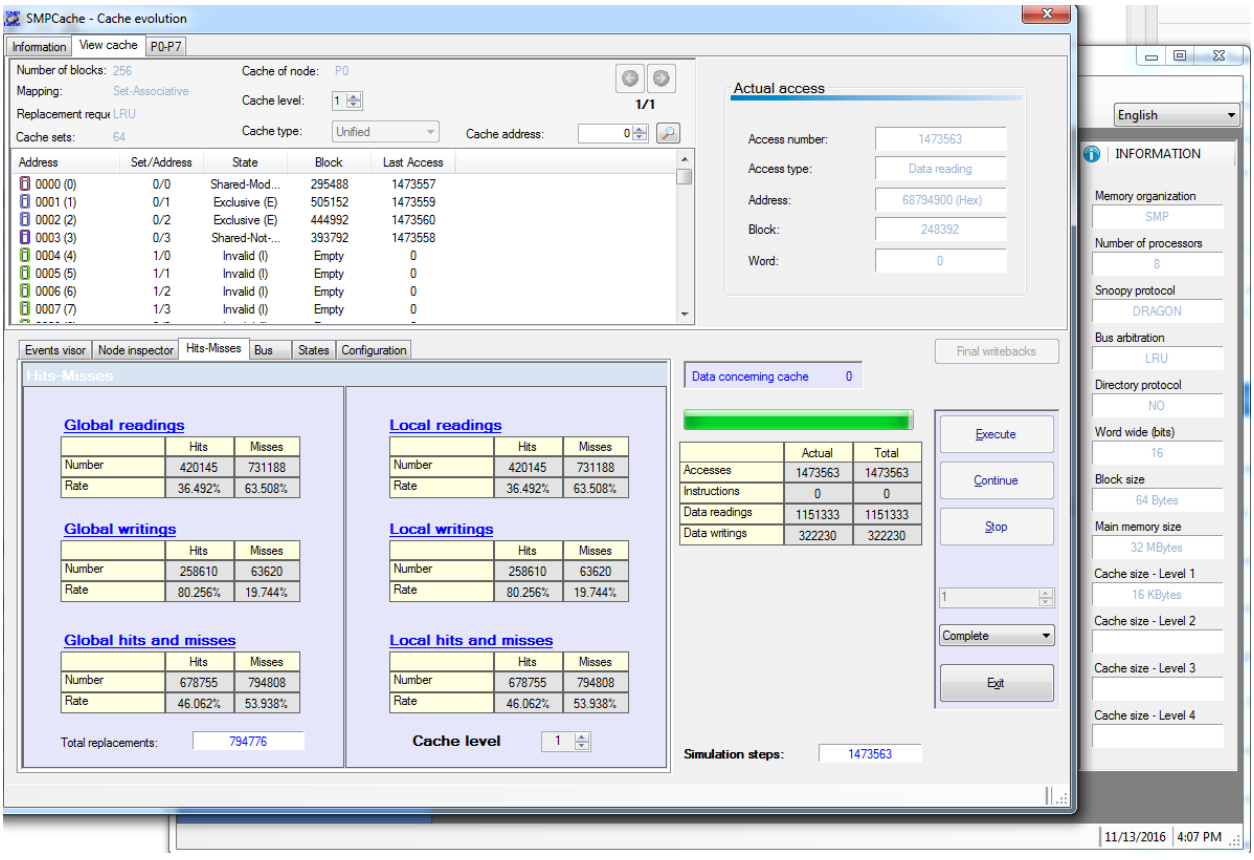
SMPCache - Cache evolution
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View cache
P0-P7
Number of blocks: 256
Mapping: Set-Associative
Replacement requ LRU
Cache sets: 64
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Actual access
Access number: 1473563
Access type: Data reading
Address: 68794900 (Hex)
Block: 248392
Word: 0
Address | Set/Address | State | Block | Last Access
0000 (0) | 0/0 | Shared-Mod... | 295488 | 1473557
0001 (1) | 0/1 | Exclusive (E) | 505152 | 1473559
0002 (2) | 0/2 | Exclusive (E) | 444992 | 1473560
0003 (3) | 0/3 | Shared-Not-... | 393792 | 1473558
0004 (4) | 1/0 | Invalid (I) | Empty | 0
0005 (5) | 1/1 | Invalid (I) | Empty | 0
0006 (6) | 1/2 | Invalid (I) | Empty | 0
0007 (7) | 1/3 | Invalid (I) | Empty | 0
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Hits-Misses
Data concerning cache 0
Global readings
Hits | Misses
Number | 420145 | 731188
Rate | 36.492% | 63.508%
Local readings
Hits | Misses
Number | 420145 | 731188
Rate | 36.492% | 63.508%
Global writings
Hits | Misses
Number | 258610 | 63620
Rate | 80.256% | 19.744%
Local writings
Hits | Misses
Number | 258610 | 63620
Rate | 80.256% | 19.744%
Global hits and misses
Hits | Misses
Number | 678755 | 794808
Rate | 46.062% | 53.938%
Local hits and misses
Hits | Misses
Number | 678755 | 794808
Rate | 46.062% | 53.938%
Total replacements: 794776
Cache level 1
Actual | Total
Accesses | 1473563 | 1473563
Instructions | 0 | 0
Data readings | 1151333 | 1151333
Data writings | 322230 | 322230
Simulation steps: 1473563
Execute
Continue
Stop
1
Complete
Exit
English
INFORMATION
Memory organization
SMP
Number of processors
8
Snoopy protocol
DRAGON
Bus arbitration
LRU
Directory protocol
NO
Word wide (bits)
16
Block size
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Main memory size
32 MBytes
Cache size - Level 1
16 KBytes
Cache size - Level 2
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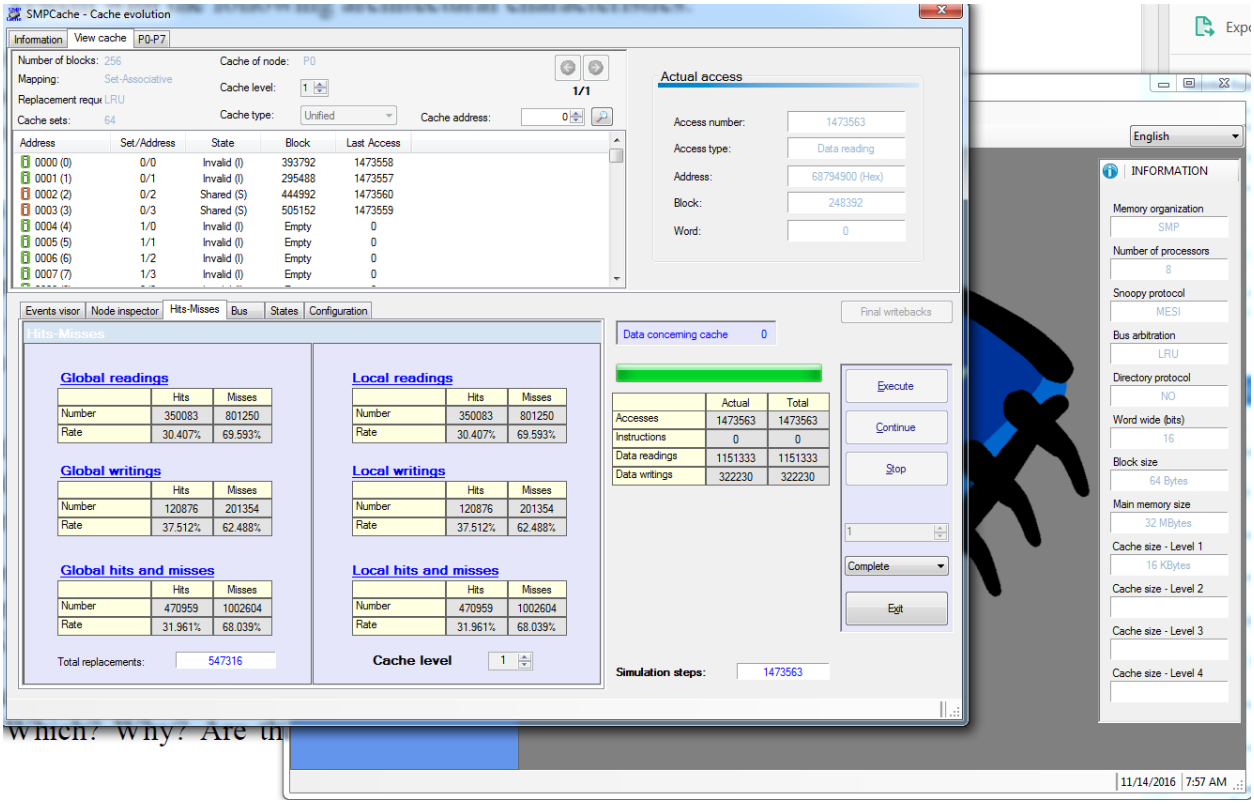

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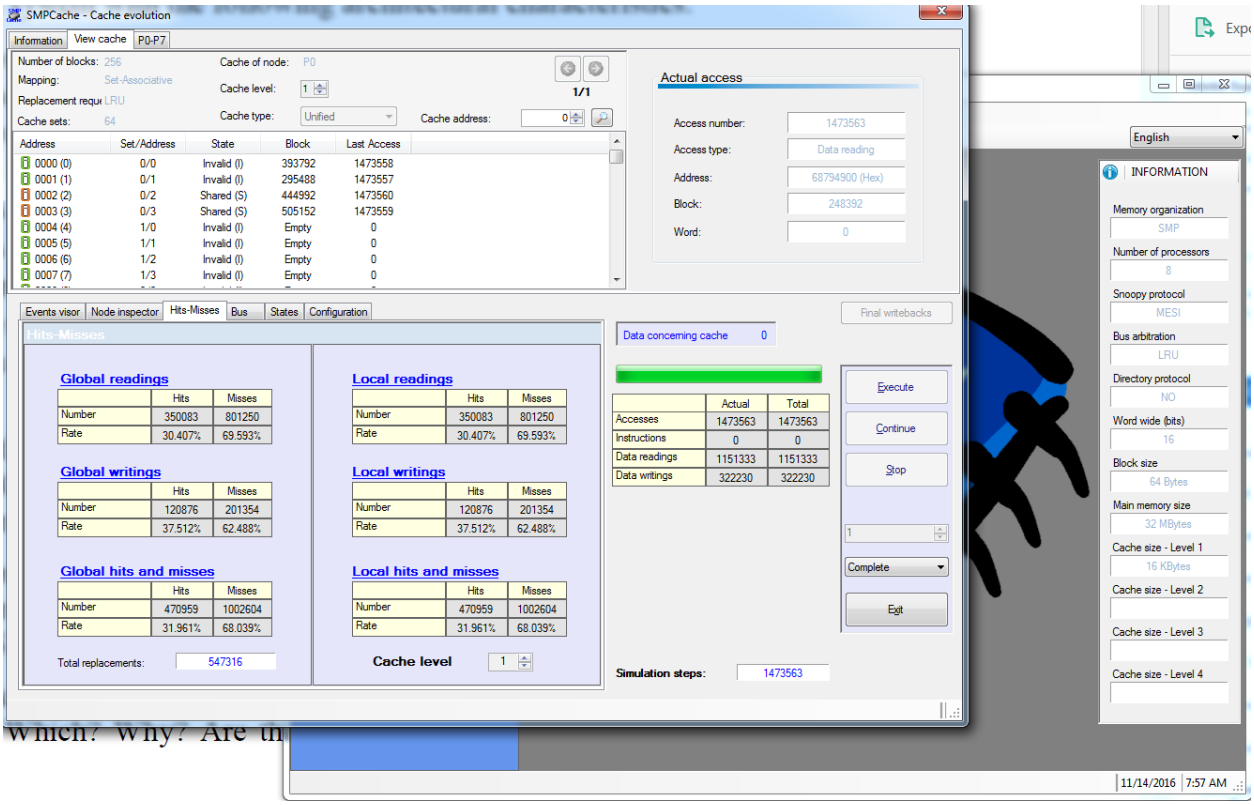

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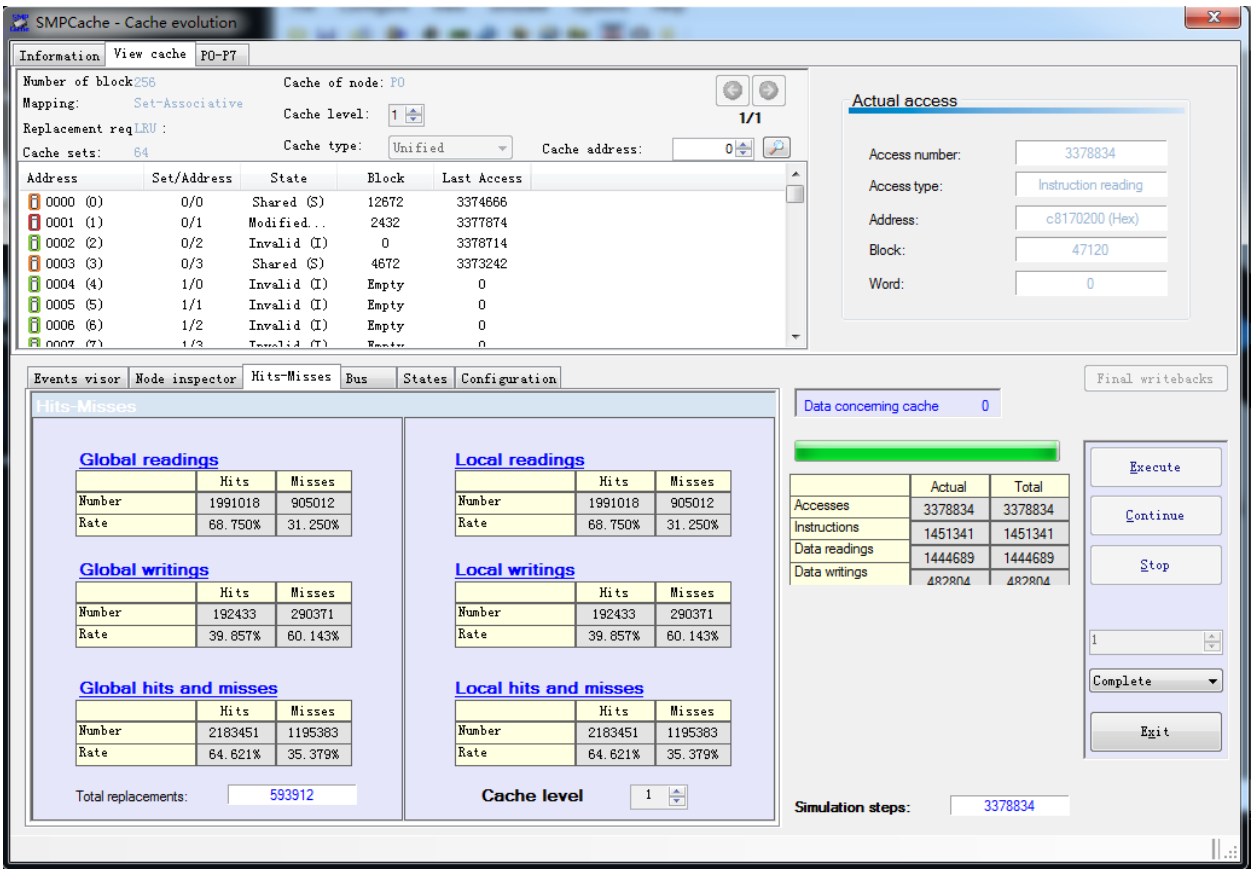
SMPCache - Cache evolution
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P0-P7
Number of block: 256
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Replacement req: LRU
Cache sets: 64
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Actual access
Access number: 3378834
Access type: Instruction reading
Address: c8170200 (Hex)
Block: 47120
Word: 0
Address | Set/Address | State | Block | Last Access
0000 (0) | 0/0 | Shared (S) | 12672 | 3374666
0001 (1) | 0/1 | Modified... | 2432 | 3377874
0002 (2) | 0/2 | Invalid (I) | 0 | 3378714
0003 (3) | 0/3 | Shared (S) | 4672 | 3373242
0004 (4) | 1/0 | Invalid (I) | Empty | 0
0005 (5) | 1/1 | Invalid (I) | Empty | 0
0006 (6) | 1/2 | Invalid (I) | Empty | 0
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Hits-Misses
Data concerning cache 0
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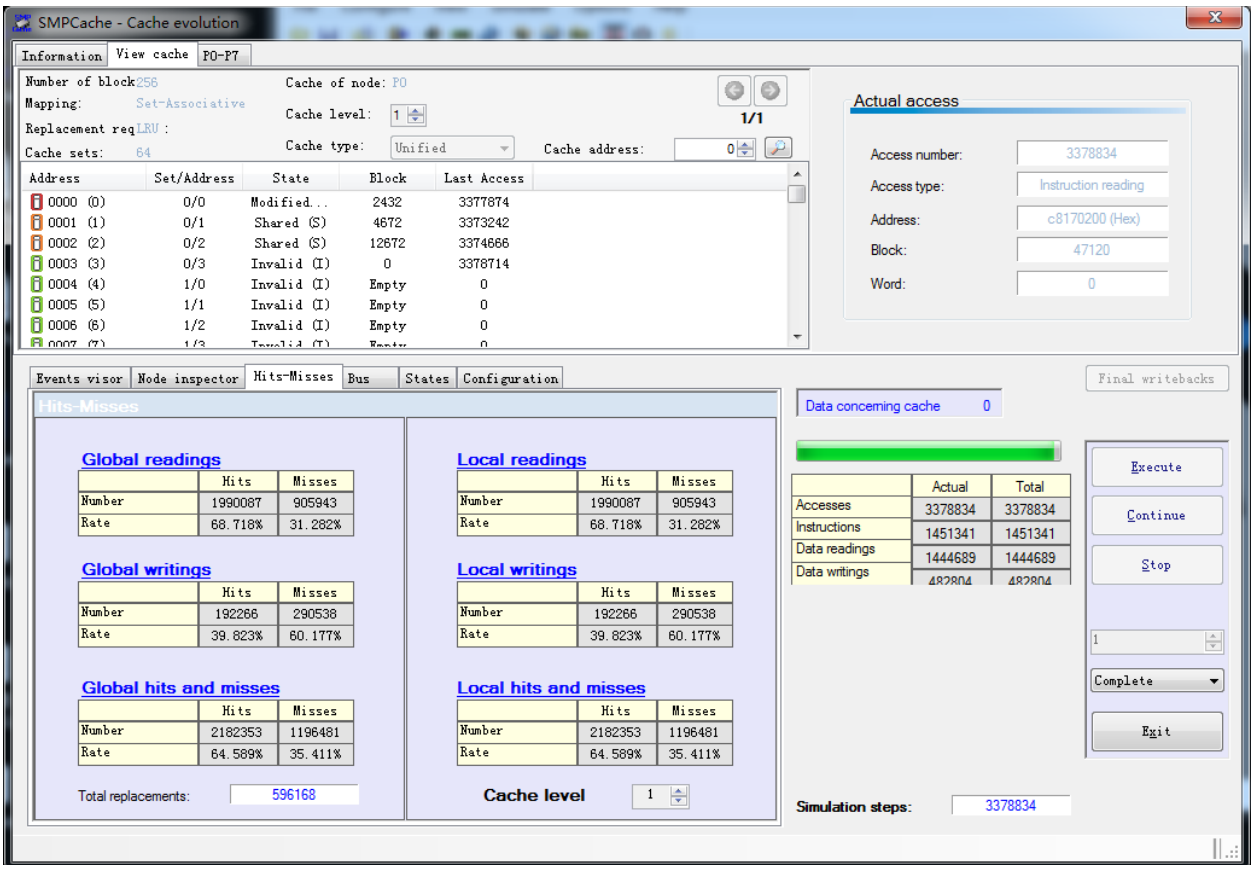
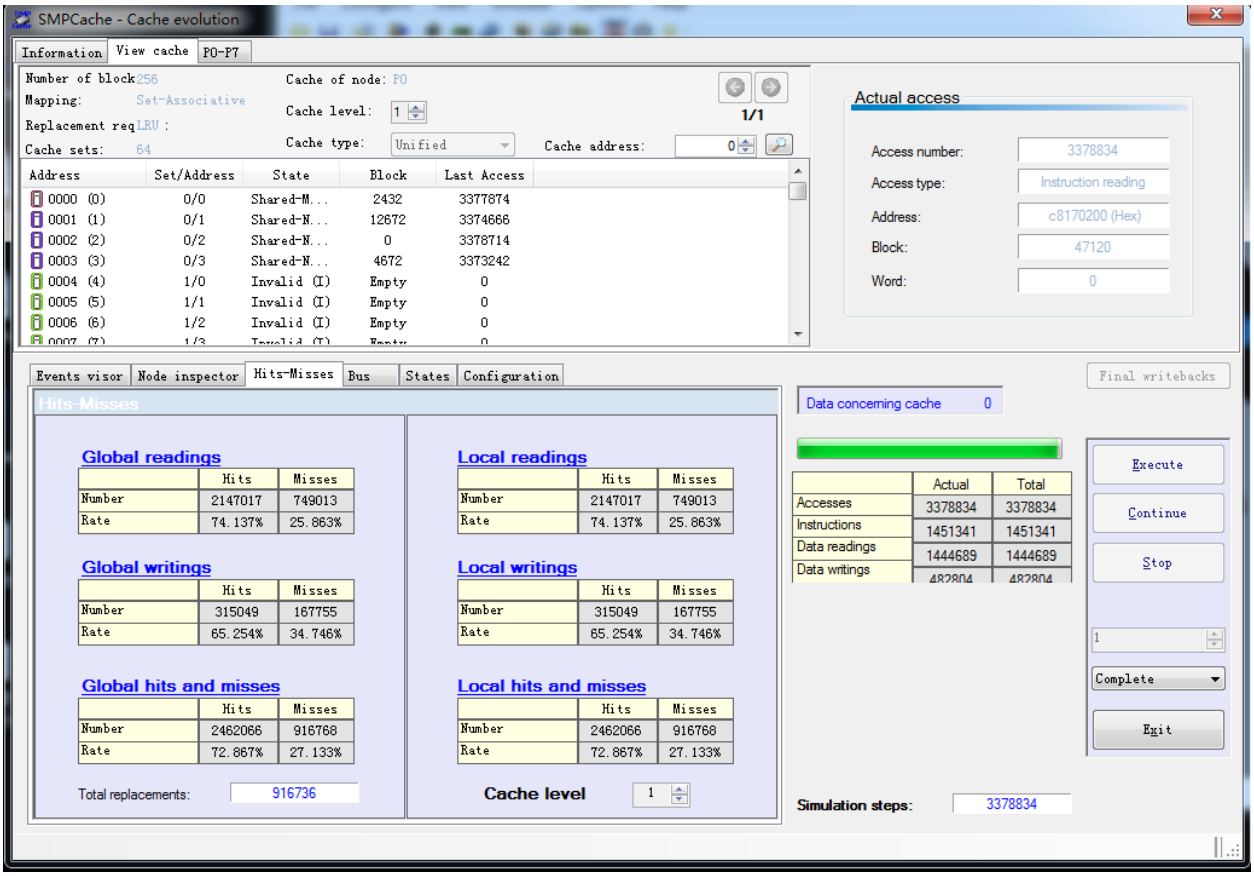
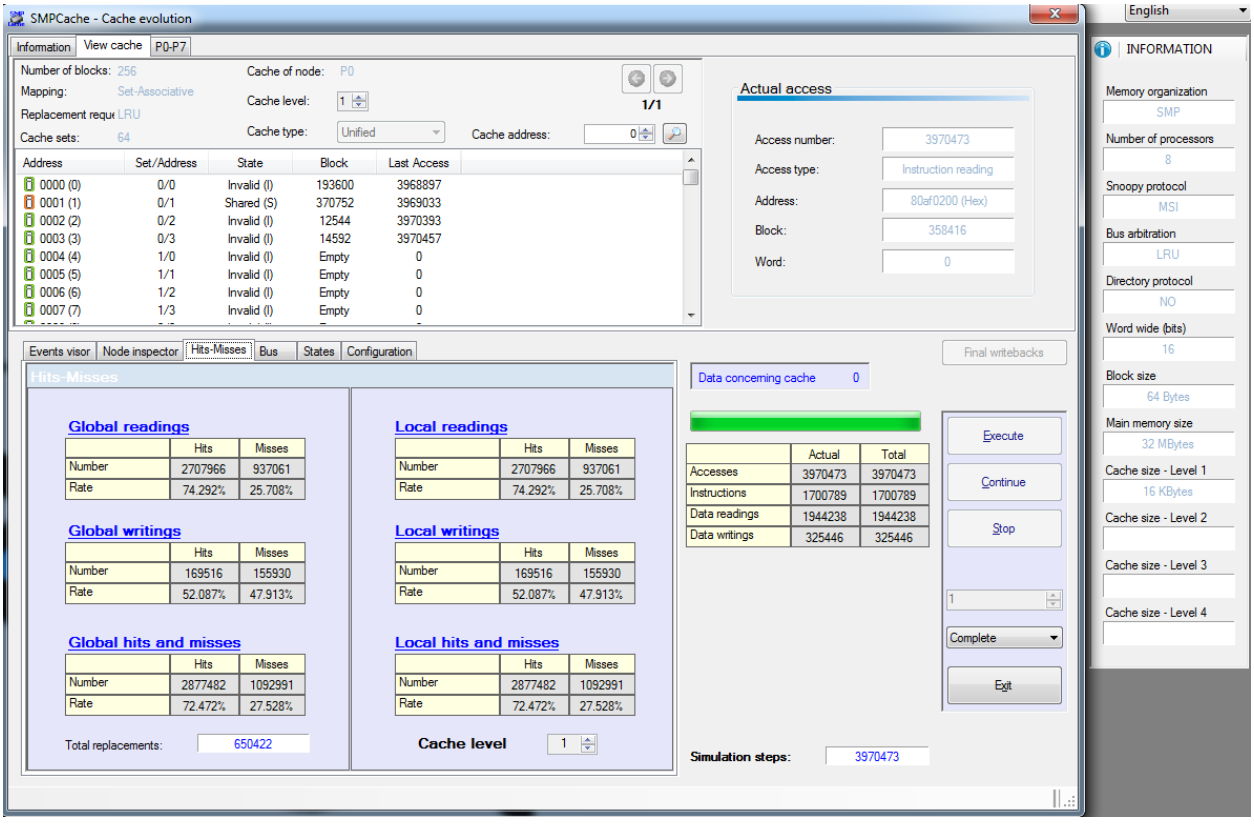
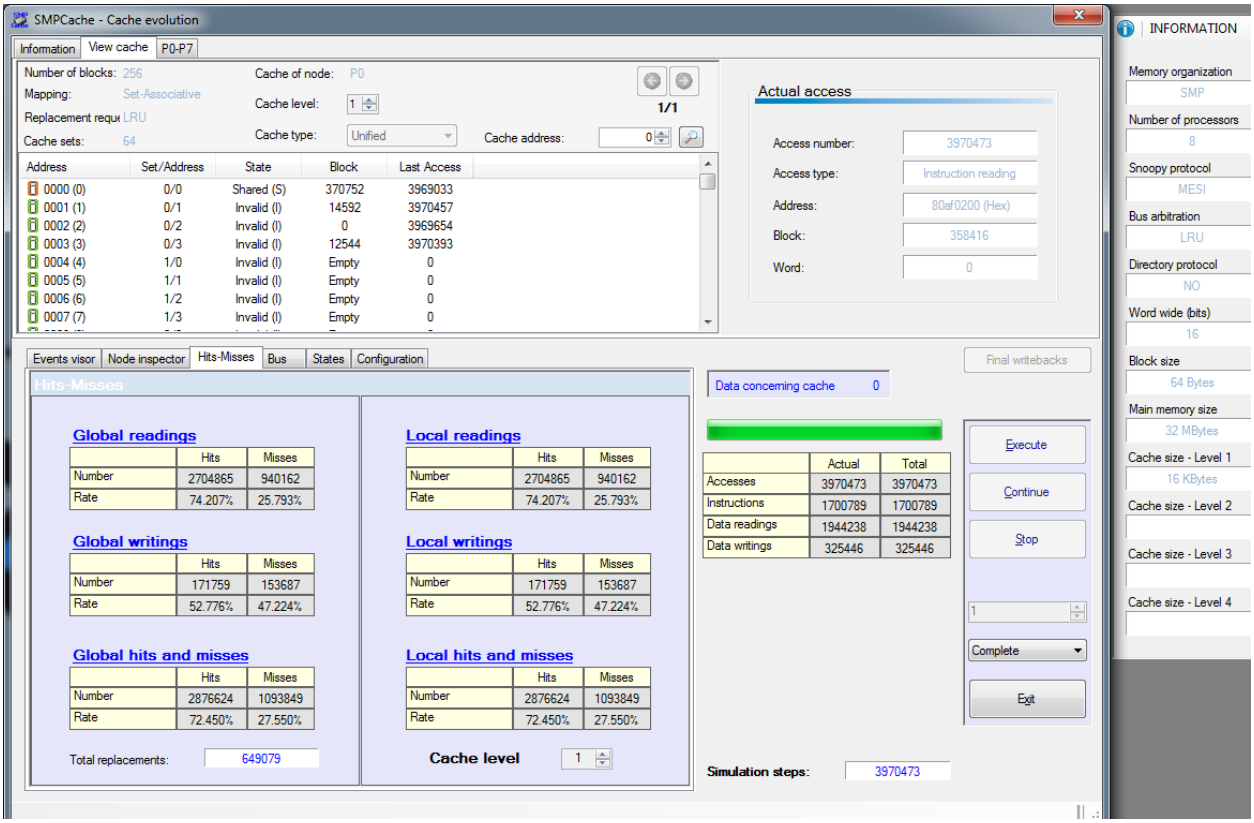
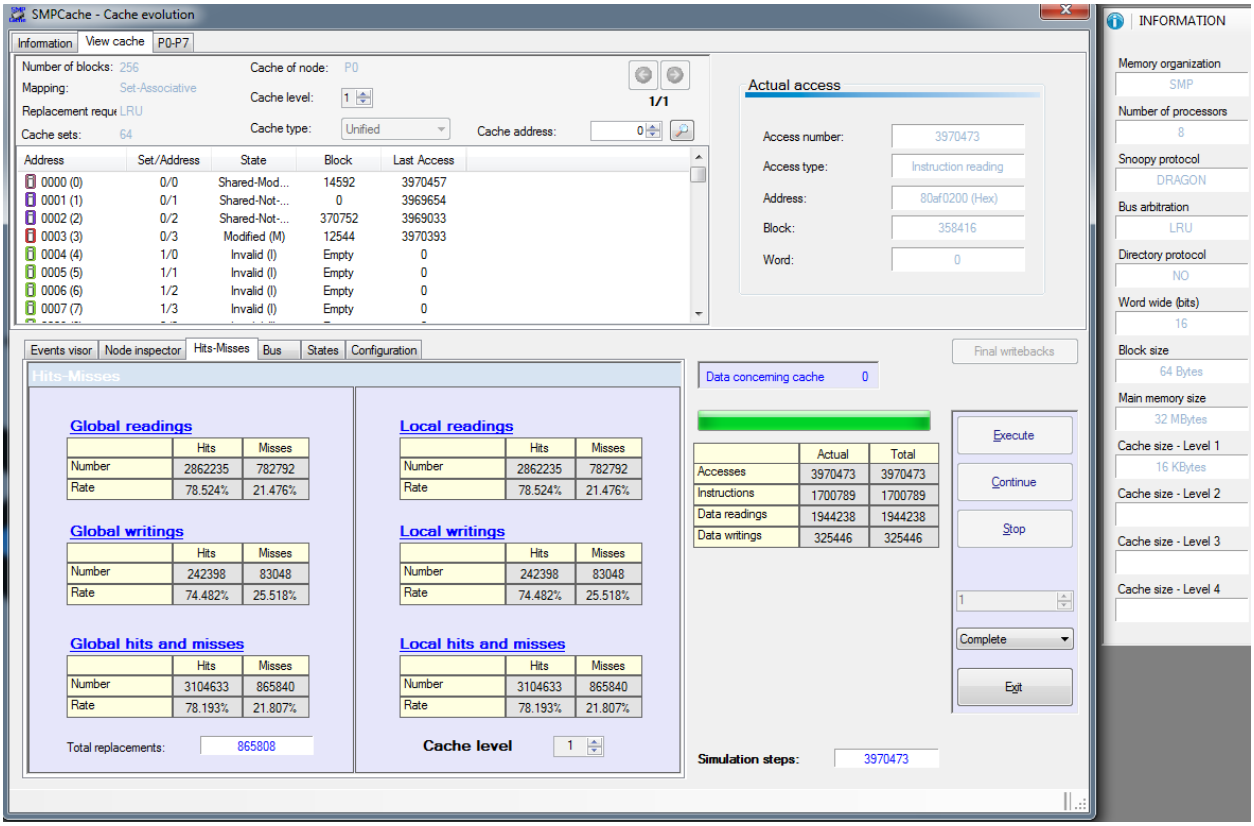
Hits | Misses
Number | 1991018 | 905012
Rate | 68.750% | 31.250%
Local readings
Hits | Misses
Number | 1991018 | 905012
Rate | 68.750% | 31.250%
Global writings
Hits | Misses
Number | 192433 | 290371
Rate | 39.857% | 60.143%
Local writings
Hits | Misses
Number | 192433 | 290371
Rate | 39.857% | 60.143%
Global hits and misses
Hits | Misses
Number | 2183451 | 1195383
Rate | 64.621% | 35.379%
Local hits and misses
Hits | Misses
Number | 2183451 | 1195383
Rate | 64.621% | 35.379%
Actual | Total
Accesses | 3378834 | 3378834
Instructions | 1451341 | 1451341
Data readings | 1444689 | 1444689
Data writings | 482804 | 482804
Execute
Continue
Stop
Complete
Exit
Total replacements: 593912
Cache level 1
Simulation steps: 3378834


SMPCache - Cache evolution
Information
View cache
P0-P7
Number of block: 256
Mapping: Set-Associative
Replacement req: LRU
Cache sets: 64
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Actual access
Access number: 3378834
Access type: Instruction reading
Address: c8170200 (Hex)
Block: 47120
Word: 0
Address | Set/Address | State | Block | Last Access
0000 (0) | 0/0 | Modified... | 2432 | 3377874
0001 (1) | 0/1 | Shared (S) | 4672 | 3373242
0002 (2) | 0/2 | Shared (S) | 12672 | 3374666
0003 (3) | 0/3 | Invalid (I) | 0 | 3378714
0004 (4) | 1/0 | Invalid (I) | Empty | 0
0005 (5) | 1/1 | Invalid (I) | Empty | 0
0006 (6) | 1/2 | Invalid (I) | Empty | 0
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Hits-Misses
Data concerning cache 0
Global readings
Hits | Misses
Number | 1990087 | 905943
Rate | 68.718% | 31.282%
Local readings
Hits | Misses
Number | 1990087 | 905943
Rate | 68.718% | 31.282%
Global writings
Hits | Misses
Number | 192266 | 290538
Rate | 39.823% | 60.177%
Local writings
Hits | Misses
Number | 192266 | 290538
Rate | 39.823% | 60.177%
Global hits and misses
Hits | Misses
Number | 2182353 | 1196481
Rate | 64.589% | 35.411%
Local hits and misses
Hits | Misses
Number | 2182353 | 1196481
Rate | 64.589% | 35.411%
Actual | Total
Accesses | 3378834 | 3378834
Instructions | 1451341 | 1451341
Data readings | 1444689 | 1444689
Data writings | 482804 | 482804
Execute
Continue
Stop
Complete
Exit
Total replacements: 596168
Cache level 1
Simulation steps: 3378834


SMPCache - Cache evolution
Information
View cache
P0-P7
Number of block 256
Mapping: Set-Associative
Replacement req LRU
Cache sets: 64
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Actual access
Access number: 3378834
Access type: Instruction reading
Address: c8170200 (Hex)
Block: 47120
Word: 0
Address | Set/Address | State | Block | Last Access
0000 (0) 0/0 Shared-M... 2432 3377874
0001 (1) 0/1 Shared-N... 12672 3374666
0002 (2) 0/2 Shared-N... 0 3378714
0003 (3) 0/3 Shared-N... 4672 3373242
0004 (4) 1/0 Invalid (I) Empty 0
0005 (5) 1/1 Invalid (I) Empty 0
0006 (6) 1/2 Invalid (I) Empty 0
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Hits-Misses
Data concerning cache 0
Global readings
Hits | Misses
Number 2147017 749013
Rate 74.137% 25.863%
Local readings
Hits | Misses
Number 2147017 749013
Rate 74.137% 25.863%
Global writings
Hits | Misses
Number 315049 167755
Rate 65.254% 34.746%
Local writings
Hits | Misses
Number 315049 167755
Rate 65.254% 34.746%
Global hits and misses
Hits | Misses
Number 2462066 916768
Rate 72.867% 27.133%
Local hits and misses
Hits | Misses
Number 2462066 916768
Rate 72.867% 27.133%
Actual | Total
Accesses 3378834 3378834
Instructions 1451341 1451341
Data readings 1444689 1444689
Data writings 482804 482804
Execute
Continue
Stop
Complete
Exit
Total replacements: 916736
Cache level 1
Simulation steps: 3378834


SMPCache - Cache evolution
English
INFORMATION
Information
View cache
P0-P7
Number of blocks: 256
Mapping: Set-Associative
Replacement requ LRU
Cache sets: 64
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Actual access
Access number: 3970473
Access type: Instruction reading
Address: 80af0200 (Hex)
Block: 358416
Word: 0
Address | Set/Address | State | Block | Last Access
0000 (0) 0/0 Invalid (I) 193600 3968897
0001 (1) 0/1 Shared (S) 370752 3969033
0002 (2) 0/2 Invalid (I) 12544 3970393
0003 (3) 0/3 Invalid (I) 14592 3970457
0004 (4) 1/0 Invalid (I) Empty 0
0005 (5) 1/1 Invalid (I) Empty 0
0006 (6) 1/2 Invalid (I) Empty 0
0007 (7) 1/3 Invalid (I) Empty 0
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Hits-Misses
Data concerning cache 0
Global readings
Hits | Misses
Number 2707966 937061
Rate 74.292% 25.708%
Local readings
Hits | Misses
Number 2707966 937061
Rate 74.292% 25.708%
Global writings
Hits | Misses
Number 169516 155930
Rate 52.087% 47.913%
Local writings
Hits | Misses
Number 169516 155930
Rate 52.087% 47.913%
Global hits and misses
Hits | Misses
Number 2877482 1092991
Rate 72.472% 27.528%
Local hits and misses
Hits | Misses
Number 2877482 1092991
Rate 72.472% 27.528%
Actual | Total
Accesses 3970473 3970473
Instructions 1700789 1700789
Data readings 1944238 1944238
Data writings 325446 325446
Execute
Continue
Stop
Complete
Exit
Total replacements: 650422
Cache level 1
Simulation steps: 3970473
Memory organization
SMP
Number of processors
8
Snoopy protocol
MSI
Bus arbitration
LRU
Directory protocol
NO
Word wide (bits)
16
Block size
64 Bytes
Main memory size
32 MBytes
Cache size - Level 1
16 KBytes
Cache size - Level 2
Cache size - Level 3
Cache size - Level 4


SMPCache - Cache evolution
Information
View cache
P0-P7
Number of blocks: 256
Mapping: Set-Associative
Replacement requ LRU
Cache sets: 64
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address | Set/Address | State | Block | Last Access
0000 (0) 0/0 Shared (S) 370752 3969033
0001 (1) 0/1 Invalid (I) 14592 3970457
0002 (2) 0/2 Invalid (I) 0 3969654
0003 (3) 0/3 Invalid (I) 12544 3970393
0004 (4) 1/0 Invalid (I) Empty 0
0005 (5) 1/1 Invalid (I) Empty 0
0006 (6) 1/2 Invalid (I) Empty 0
0007 (7) 1/3 Invalid (I) Empty 0
Actual access
Access number: 3970473
Access type: Instruction reading
Address: 80af0200 (Hex)
Block: 358416
Word: 0
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Hits-Misses
Global readings
Hits Misses
Number 2704865 940162
Rate 74.207% 25.793%
Global writings
Hits Misses
Number 171759 153687
Rate 52.776% 47.224%
Global hits and misses
Hits Misses
Number 2876624 1093849
Rate 72.450% 27.550%
Total replacements: 649079
Local readings
Hits Misses
Number 2704865 940162
Rate 74.207% 25.793%
Local writings
Hits Misses
Number 171759 153687
Rate 52.776% 47.224%
Local hits and misses
Hits Misses
Number 2876624 1093849
Rate 72.450% 27.550%
Cache level 1
Data concerning cache 0
Actual Total
Accesses 3970473 3970473
Instructions 1700789 1700789
Data readings 1944238 1944238
Data writings 325446 325446
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 3970473
INFORMATION
Memory organization SMP
Number of processors 8
Snoopy protocol MESI
Bus arbitration LRU
Directory protocol NO
Word wide (bits) 16
Block size 64 Bytes
Main memory size 32 MBytes
Cache size - Level 1 16 KBytes
Cache size - Level 2
Cache size - Level 3
Cache size - Level 4


SMPCache - Cache evolution
Information
View cache
P0-P7
Number of blocks: 256
Mapping: Set-Associative
Replacement requ LRU
Cache sets: 64
Cache of node: P0
Cache level: 1
Cache type: Unified
Cache address: 0
1/1
Address | Set/Address | State | Block | Last Access
0000 (0) 0/0 Shared-Mod... 14592 3970457
0001 (1) 0/1 Shared-Not-... 0 3969654
0002 (2) 0/2 Shared-Not-... 370752 3969033
0003 (3) 0/3 Modified (M) 12544 3970393
0004 (4) 1/0 Invalid (I) Empty 0
0005 (5) 1/1 Invalid (I) Empty 0
0006 (6) 1/2 Invalid (I) Empty 0
0007 (7) 1/3 Invalid (I) Empty 0
Actual access
Access number: 3970473
Access type: Instruction reading
Address: 80af0200 (Hex)
Block: 358416
Word: 0
Events visor
Node inspector
Hits-Misses
Bus
States
Configuration
Final writebacks
Hits-Misses
Global readings
Hits Misses
Number 2862235 782792
Rate 78.524% 21.476%
Global writings
Hits Misses
Number 242398 83048
Rate 74.482% 25.518%
Global hits and misses
Hits Misses
Number 3104633 865840
Rate 78.193% 21.807%
Total replacements: 865808
Local readings
Hits Misses
Number 2862235 782792
Rate 78.524% 21.476%
Local writings
Hits Misses
Number 242398 83048
Rate 74.482% 25.518%
Local hits and misses
Hits Misses
Number 3104633 865840
Rate 78.193% 21.807%
Cache level 1
Data concerning cache 0
Actual Total
Accesses 3970473 3970473
Instructions 1700789 1700789
Data readings 1944238 1944238
Data writings 325446 325446
Execute
Continue
Stop
1
Complete
Exit
Simulation steps: 3970473
INFORMATION
Memory organization SMP
Number of processors 8
Snoopy protocol DRAGON
Bus arbitration LRU
Directory protocol NO
Word wide (bits) 16
Block size 64 Bytes
Main memory size 32 MBytes
Cache size - Level 1 16 KBytes
Cache size - Level 2
Cache size - Level 3
Cache size - Level 4